BE-M1000 Microprocessor
Preliminary Datasheet

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1 Introduction

The BE-M1000 is a general purpose *System-on-a-Chip* (**SoC**) for computing systems, such as personal computers, microservers, networking equipment, multimedia and software-defined hardware, embedded systems and controllers that require high performance and low power consumption.

The SoC features eight Arm® Cortex™-A57 cores that operate at 1.5 GHz and support the coherent caches L1, L2, and L3.

The video subsystem includes two video controllers (LVDS and HDMI), and a 4K video decoder. Arm® Mali™-T628 graphics coprocessor contains eight shader cores.

The SoC contains two DDR3/4 memory controllers and a wide range of peripheral interfaces: PCIe Gen3, 10 Gb Ethernet, 1 Gb Ethernet, USB 3.0, USB 2.0, SATA 6G, eMMC/SD, I^2S, SPI, UART, I^2C, GPIO, etc.

The SoC complies with Arm® TrustZone® technology and contains the capabilities necessary to build trusted systems.

1.1 Main Features

Table 1-1 Main Features

Feature	Description
Armv8-A Architecture	8 Arm Cortex-A57 cores operating at 1.5 GHz
	4 core clusters (2 cores and 1 MB L2 cache in a cluster)
Graphics Processing Unit	Arm Mali-T628 *graphics processing unit* (**GPU**) with 8 shader cores (two quad-core clusters) operating at 700 MHz
	128 KB L2 cache in a cluster
L3 Cache	*Cache Coherent Network* (**CCN**) with 8 MB L3 cache memory
External Memory Interface	Two 64-bit *Dynamic Random Access Memory* (**DRAM**) interfaces with support of DDR4-2400/DDR3-1600 and *error correction code* (**ECC**)
High Speed Peripheral Interfaces	Three *PCI Express* (**PCIe**) Gen3: one PCIe x8 and two PCIe x4
	Two *Universal Serial Bus* (**USB**) 3.0/2.0 ports, four USB 2.0 ports
	Two *Serial ATA* (**SATA**) 6G
	Two 10 Gb Ethernet (10GBASE-KX4, 10GBASE-KR)
	Two 1 Gb Ethernet RGMII
	Embedded Multimedia Card (**eMMC**)/*Secure Digital* (**SD**)/*Secure Data Input/Output* (**SDIO**)
Low Speed Peripheral Interfaces	Four peripheral timers
	General Purpose I/O 32-bit (**GPIO*32**)
	Two *Universal Asynchronous Receiver-Transmitters* (**UARTs**)
	Serial Peripheral Interface (**SPI**)
	Enhanced Serial Peripheral Interface (**eSPI**)
	Two *Inter-Integrated Circuits* (**I^{2}Cs**)
	Two *System Management Bus* (**SMBus**)
Multimedia	Video Controller with *low-voltage differential signaling* (**LVDS**) interface
	Video Controller with *high definition* (**HD**) display interface *HD Multimeda Interface* (**HDMI**) 2.0
	4K Video Decoder
	Inter-IC sound (**I^{2}S**) interface
Security	Arm TrustZone architecture
	Two TrustZone controllers
	Secure boot
System Monitoring and Debug	Five PVT controllers
	Arm® CoreSight™ debug and trace architecture
Package	FCBGA-1521 40x40 mm, 1 mm pitch, 1521 pins
Power Consumption	28.5 W max
Technology	CMOS 28 nm

1.2 Block Diagram

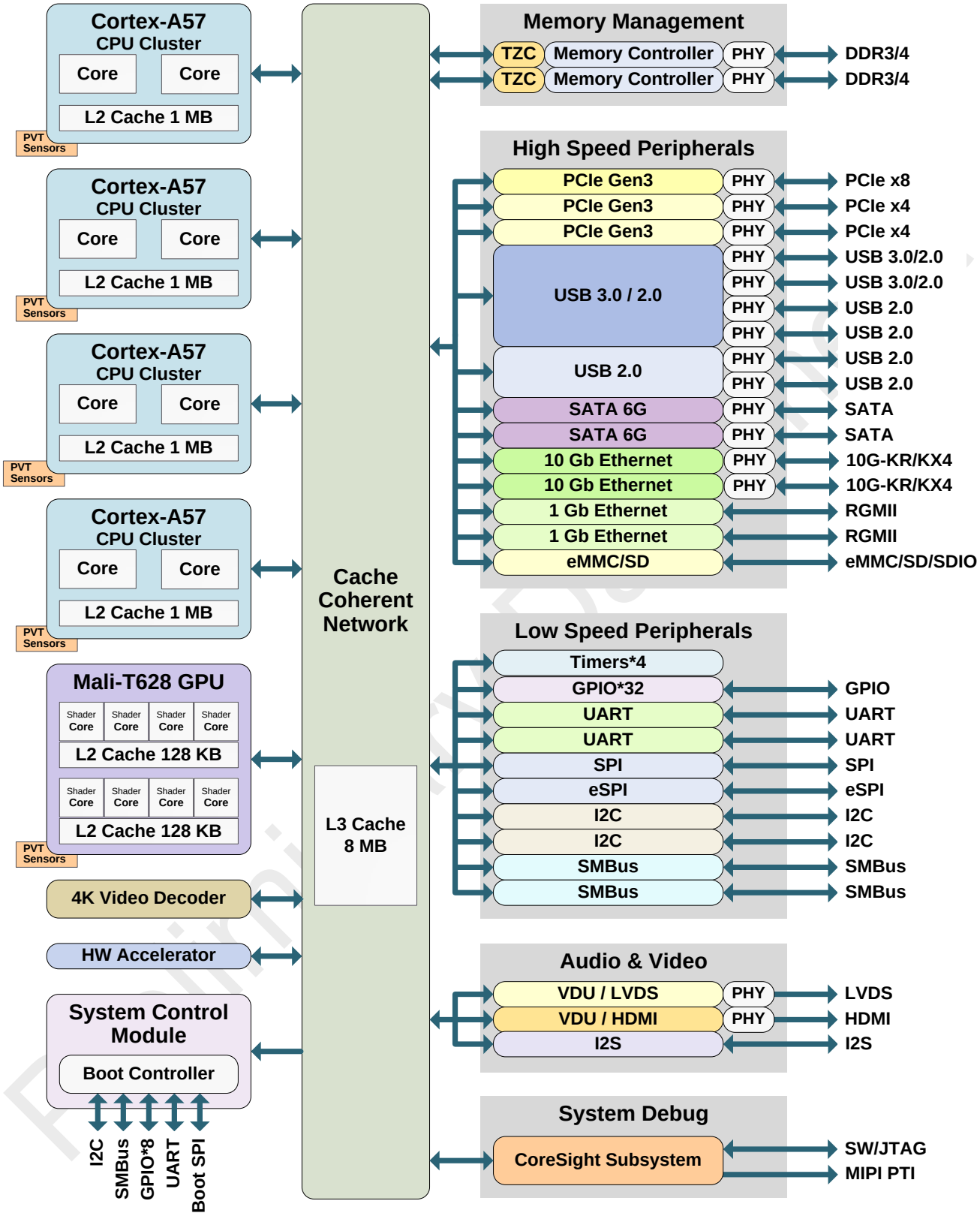


Figure 1-1 Block Diagram

2 Detailed Description

2.1 Arm Cortex-A57 CPU Clusters

The SoC contains 8 Arm Cortex-A57 cores in 4 clusters.

The Cortex-A57 cluster is a high-performance, low-power device that implements the Armv8-A architecture.

Each cluster has two cores (1.5 GHz) and L2 (1 MB) cache.

Each core has 48 KB L1 instruction cache and 32 KB L1 data cache.

A core can operate in one of two possible states, known as the Secure and Non-secure. By propagating the security state of the core through the on-chip interconnect to target based transaction filters, the TrustZone technology is extended into the SoC architecture, creating a robust platform supporting fully isolated Trusted and Non-trusted worlds.

2.2 Memory Management

2.2.1 DDR3/4 Memory Subsystems

DDR memory control subsystems support the following features:

- Up to 2 memory channels
- Up to 64 GB physical memory per channel
- Up to 4 memory ranks per channel
- Integrated PHY
- 64/32-bit DDR3 (speed grades up to DDR3-1600)
- 64/32-bit DDR4 (speed grades up to DDR4-2400)
- ECC: *single error correction/double error detection* (**SEC**/**DED**)
- 1:2 frequency ratio mode
- DDR4U and DDR4L
- Industry standard UDIMMs and RDIMMs
- Low area, low power architecture
- Programmable support for 1T/2T memory command timing
- Software programmable *quality of service* (**QoS**)
- Automatic DDR3/4 low power mode operation

DDR memory control subsystems are combined in the SoC with TrustZone controllers to provide capabilities for building trusted systems.

2.2.2 TrustZone Controllers

There are two *TrustZone controllers* (**TZC**) in the SoC.

A TZC is placed on the path to each DDR controller to implement memory access restrictions according to Arm TrustZone technology.

To provide security address region control functions required for intended application, a TZC includes Control and Filter units.

The TZC Control Unit contains programmable registers to configure a table of rules defining access restrictions for 8 continuous memory regions, particularly specifying if the memory region can be accessible in specific modes: secure or non-secure.

All the memory requests received by the controller are passed through the Filter Unit determining whether the requested address can be accessed by the current transaction, depending on its state, secure or non-

secure. Also, memory access in non-secure mode can be restricted based on the source of the transaction module that initiated the transaction.

2.2.3 DMA Controller for Low Speed Peripherals

The DMA LSP implements capability of direct data transfer between a low speed device, which is connected to a low speed peripheral interface, and memory without CPU usage.

It helps in maximizing system performance by decreasing a load of the SoC cores.

The DMA controller can only work in non-secure mode and has the following main features:

- Handshaking interface with two UARTs, SPI, and two I^2C controllers
- 8 channels, one per source and destination pair
- Unidirectional channels: data transfers in one direction only
- Multi-block transfers
- Single FIFO per channel for source and destination
- Automatic data packing or unpacking to fit FIFO width

2.2.4 DMA Controller for MEM2MEM Transfers

The DMA Controller for MEM2MEM transfers provides direct data transfer between memory blocks of interacting subsystems without CPU usage.

It implements TrustZone secure technology with one APB interface operating in the secure state and the other operating in the Non-secure state. Two APB interfaces enable the operation of the DMA to be partitioned in secure and non-secure modes.

2.2.5 Hardware Accelerator

Designed to improve the performance of computing, the HWA consists of hardware modules, which implement special algorithms of data processing.

2.3 Cache Coherent Network

Based on the Arm® CoreLink™ CCN-504, CCN provides interconnection of the main SoC subsystems and manages the Level 3 cache for these subsystems.

High-performance distributed system cache, 8 MB in capacity, includes an integrated *point-of-serialization* (**PoS**) and *point-of-coherency* (**PoC**) and can be used both for compute and *input/output* (**I/O**) caching.

The CCN provides the following key features:

- Dual simplex ring-bus interconnect topology
- One 128-bit, dual simplex data channel
- Broadcast snoop channel
- DVM message transport between masters
- QoS regulation for shaping traffic profiles
- Monitoring performance-related events
- Error signal gathering using an error bus, with a single point of interrupt coordination on errors
- Separate caches for secure and non-secure transactions

2.4 System Control Module

The System Control Module is used to manage all the SoC subsystems.

It contains the following main blocks:

- *System control processor* (**SCP**) that runs service functions such as:
  - Starts the SoC
  - Provides the initial configuration of all the SoC modules
  - Monitors the state of the SoC
- Boot controller that contains dedicated SPI used for initial boot
- UART, SMBus, GPIO*8, and I^2C controllers used for system control functions
- Clock Management Unit that controls system clock and reset signals

2.5 High Speed Peripherals

2.5.1 PCIe Gen 3.0

The SoC contains three PCIe interfaces: two identical PCIe x4 and one PCIe x8.

Each PCIe contains PCIe Root Complex controller that provides base PCIe functionality in accordance with the ***PCI Express Base Specification 3.0***.

Each PCIe provides the following main features:

- Integrated PHY
- Transfer rates up to 8.0 GT/s (~1GB/s) per single lane
- PCIe *active state power management* (**ASPM**)
- PCIe *advanced error reporting* (**AER**) with Multiple Header Logging
- Internal Address Translation Unit
- Embedded multichannel DMA controller
- Automatic Lane Reversal
- ECRC Generation and Checking
- Maximum Payload Size:
  - 256 bytes for PCIe x4
  - 512 bytes for PCIe x8
- 1 Virtual Channel for PCIe x4, 2 Virtual Channels for PCIe x8

PCIe can work both in secure and non-secure modes.

2.5.2 USB 3.0/2.0

The SoC contains two USB 3.0/2.0 and two USB 2.0 interfaces, each with integrated PHY.

USB 3.0/2.0 controller is compatible with the xHCI specification by Intel Corporation. It is optimized for the Super-Speed applications and systems and supports the following device types:

- Super-Speed devices via USB 3.0 interface (4 Gbps IN and 4 Gbps OUT)
- High-Speed, Full-Speed, and Low-Speed devices via any interface

The controller contains multiple bus instances to support concurrent USB 3.0/2.0 transfers on each port. Therefore in the current configuration (four bus instances for two SS ports and two HS ports), the controller net throughput is 9.92 Gbps (2*4 Gbps + 2*480 Mbps IN and 2*4 Gbps + 2*480 Mbps OUT).

These interfaces is targeted to the next generation of media storage, creation, and playback devices requiring high bandwidth for faster “sync-and-go” functionality between PCs and portable electronic devices, such as flash drives, solid state drives, camcorders, portable media players, and smartphones.

USB 3.0/2.0 can work both in secure and non-secure modes.

2.5.3 USB 2.0

The SoC contains two USB 2.0 interfaces, each with integrated PHY.

USB 2.0 controller is compatible with the xHCI specification by Intel Corporation. It is optimized for the high-bandwidth applications and systems and supports the following device types:

- High-Speed (480 Mbps)
- Full-Speed (12 Mbps)
- Low-Speed (1.5 Mbps)

USB 2.0 can work both in secure and non-secure modes.

2.5.4 SATA 6G

The SoC contains two identical SATA subsystems. Each SATA supports the following features:

- Integrated PHY
- SATA 6.0 Gb/s speeds
- eSATA (external analog logic also needs to support eSATA)
- Compliant with Serial ATA 3.2 and AHCI Revision 1.3 specifications
- 8b/10b encoding/decoding
- *Error correction code* (**ECC**)
- Power management features including automatic partial-to-slumber transition
- *Built-in self-test* (**BIST**) loopback modes
- Internal DMA engine per port

Each SATA can work both in secure and non-secure modes.

2.5.5 10 Gb Ethernet

The SoC contains two identical 10 Gb Ethernet interfaces, which enable to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard for two types of 10 Gb/s Ethernet: 10GBASE-KX4 and 10GBASE-KR.

Each interface contains a *10 Gb Ethernet media access controller* (**XGMAC**) with integrated *10 Gigabit Ethernet Physical Coding Sublayer* (**XPCS**) and 10 Gb Ethernet PHY.

Each XGMAC has the following main features:

- Full-duplex operation at 10 Gbps
- Full compliance with Clause 71 (10GBASE-KX4) and Clause 72 (10GBASE-KR) of the IEEE 802.3-2008 standard
- Full compliance with Clause 78 (*Energy Efficient Ethernet* (**EEE**) feature) of the IEEE 802.3az, standard for 10 Gbps operation
- Programmable frame length, supporting standard or jumbo (extendable to 16 KB) Ethernet frames
- Support for VLAN-tagged frame processing in compliance with the IEEE 802.1Q standard

Each XGMAC can work both in secure and non-secure modes.

2.5.6 1 Gb Ethernet

The module provides two identical *1 Gigabit media access controllers* (**GMAC**).

Each controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

Each GMAC has the following main features:

- 10, 100, and 1000 Mbps data transfer rates with RGMII interface to communicate with an external gigabit PHY
- Full-duplex operation support
- Half-duplex operation support
- Embedded DMA controller with independent Transmit and Receive engines

Each GMAC can work both in secure and non-secure modes.

2.5.7 eMMC/SD

It provides communication with memory cards targeted for the mobile/portable market and adheres to the SD UHS-I and eMMC specifications.

The eMMC/SD supports the following features:

- SD memory and SDIO digital interface protocol, and compliant with SD HCI specification
- eMMC protocols including eMMC 5.1
- SD-HCI Host version 4 mode or less
- Embedded DMA controller
- Software tuning in SD UHS-I and eMMC modes

2.6 Low Speed Peripherals

2.6.1 Peripheral Timers

The module contains four independent peripheral timers.

Each peripheral timer is a 32-bit programmable timer supported “free-running” and “user-defined count” modes.

In “user-defined count” mode, a timer counts down from a programmed value and generates an interrupt when the count reaches zero. Timer interrupt can be detected even when the system bus clock is stopped.

*2.6.2 GPIO*32*

It implements run-time 32-bit programmable interface for external communications. The GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.

The interface contains 32 individually controllable signals in a single port.

2.6.3 UART

There are two identical UARTs in the SoC.

Each UART has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the UART and memory.

Each UART contains registers that control:

- Character length
- Baud rates up to 1.5 Mbaud
- Parity generation/checking
- Interrupt generation

2.6.4 SPI

The SPI is a full-duplex master or slave-synchronous serial interface used for short distance communication with up to four external slave devices (SSx4).

It has a handshaking interface with the DMA LSP that can request and control data transfers between the SPI and memory.

A master (application processor or the DMA LSP) accesses data, control, and status information on the SPI through the APB interface.

The SPI operates as a serial master. It can connect to a serial-slave peripheral device using Motorola SPI interface.

2.6.5 eSPI

The eSPI is a synchronous serial communication interface used for short distance communication with up to eight external slave devices (SSx8).

Additional eSPI signals in compare to SPI Interface:

- `RESET` programmable as input or output
- `ALERT` input interrupts

eSPI device communicates in full-duplex mode using master-slave architecture with up to eight external slave SPI devices (SSx8). It supports Single/Dual/Quad SPI mode of operation.

2.6.6 I^2C

There are two identical general purpose I^2Cs in the SoC.

The I^2C is a programmable serial interface that provides support for the communications link between the devices connected to the bus.

Each I^2C support the following features:

- Three speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (≤ 400 Kb/s) or fast mode plus (≤ 1000 Kb/s)
  - High-speed mode (≤ 3.4 Mb/s)
- Master OR slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers

Each I^2C has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the I^2C and memory.

2.6.7 SMBus

The SoC includes two identical SMBus interfaces.

This interface provides a two-wire bidirectional interface for transfer of bytes of information between multiple compliant I^2C devices, typically with a microprocessor behind the DB-I^2C master/slave controller and one or more master/slave devices.

2.7 Audio & Video

2.7.1 Arm Mali-T628 GPU

Provides a complete graphics acceleration platform based on open standards. It supports 2D graphics, 3D graphics, and *general purpose computing on GPU* (**GPGPU**).

The graphics processor provides the following main features:

- Two clusters
- 4 shader cores operating at 700 MHz per each cluster

- 128KB L2 Cache per each cluster
- Seamless load balancing across active shader cores
- ETC2, EAC1, ETC2-EAC compressed formats are supported
- The following APIs are supported:
  - OpenGL ES 1.1, 2.0, 3.0, 3.1
  - OpenCL 1.1
  - RenderScript
- *Full scene anti-aliasing* (4x**FSAA**, 16x**FSAA**) with minimal performance drop
- *Adaptive scalable texture compression* (**ASTC**): l*ow dynamic range* (**LDR**) and *high dynamic range* (**HDR**) are supported
- Native hardware support for 64-bit scalar and vector, integer and floating-point data types—fundamental to accelerate complex and computationally intensive algorithms

It can work both in secure and non-secure modes.

2.7.2 4K Video Decoder

Used to decode video streams encoded in the following formats:

- H.265 (HEVC): up to 4096x2304 at 30 fps
- H.264, MPEG4, MPEG2, VP8, VP6, VC1, AVS, RealVideo, and JPEG: up to 1080p at 60 fps

The 4KDec loads the encoded video data from the system memory, decodes it and places the information ready to be sent to the video display unit into the frame buffer.

It can work both in secure and non-secure modes.

2.7.3 VDU with Quad LVDS

It is a general purpose display controller used to drive a wide range of display devices varying in size and capability.

The module provides the following main features:

- Wide range of programmable LCD Panel resolutions up to 4K
- Color resolution of up to 24 bpp
- 4-lane LVDS output interface
- Embedded DMA Controller
- Programmable vertical and horizontal timing parameters
- Two overlay windows in addition to the base screen

2.7.4 VDU with HDMI 2.0

It provides a complete HDMI interface for transmitting video and audio data to an HDMI-compliant source device, such as a computer monitor, video projector, digital television, or digital audio device.

The subsystem has the following main features:

- VDU features:
  - Wide range of programmable LCD Panel resolutions up to 2560x1440
  - Color resolution of up to 24 bpp
  - Embedded DMA Controller
  - Programmable vertical and horizontal timing parameters
  - Two overlay windows in addition to the base screen

- Three TMDS data channels with 6 Gbps data rate per channel
- Total maximum throughput of up to 18 Gbps (6 Gbps * 3 channels)
- HDMI 2.0 specification features:
  - All CEA-861-F video formats
  - *Dynamic range and mastering infoframe* (**DRM**)
- Embedded DMA Controller for Audio
- Audio stream bit rate up to 24.576 Mbps
- It can work both in secure and non-secure modes

2.7.5 I²S

I²S is a programmable module used for the serial communication with peripherals.

It is designed to be used in systems that process digital audio signals, such as:

- A/D and D/A converters
- Digital signal processors
- Error correction for compact disc and digital recording
- Digital filters
- Digital input/output interfaces

2.8 System Monitoring and Debug

2.8.1 PVT Controllers

The SoC contains five *Process, Voltage and Temperature* (**PVT**) controllers used to monitor the Cortex-A57 clusters and Mali-T628 GPU.

Each PVT controller provides the following features:

- Measurement readiness is determined by polling data register or listening the interrupt line
- Programmable upper and lower threshold values for the measured PVT parameters to produce out-of-range interrupts
- Programmable timeout value for repetitive PVT parameters monitoring

2.8.2 CoreSight Subsystem

Provides a standard implementation of the Arm Debug Interface for debug tools to work with:

- Serial Wire or JTAG Debug Port
- Trace Port Interface

The subsystem supports the following methods of debugging the SoC:

- “External” debug—conventional debug through the SW/JTAG interface
- “Self-hosted” debug—conventional debug with the processor running using a debug monitor that resides in memory
- Logging of hardware and software events in a trace, which is recorded in memory as well as transmitted through the *trace port interface* (**MIPI PTI**) to an external debug system

It can work both in secure and non-secure modes.

3 Electrical Specifications

NOTE: The electrical characteristics are subject to change and clarification without extra notification

3.1 Power Supply Parameters

BE-M1000 requires six isolated voltage supplies and single unified ground supply as shown in the following table.

Table 3-1 BE-M1000 Power Domains

Supply Type	Package Pin Name	Voltage, V	Max Power, W
Core supply	VDD	0.95 ± 5%	23
0.95V voltage supply	VDD_HDMI_09 VDD_USB2_09 VDD_USB3_0_09 VDD_USB3_1_09 VDD_USB3TX_0_09 VDD_USB3TX_1_09 VDD_USB3_VP_0_09 VDD_USB3_VP_1_09 VDD_PCIE4_0_09 VDD_PCIE4_1_09 VDD_PCIE8_09 VDD_SATA_09 VDD_SATATX_09 VDD_XG0_09 VDD_XG1_09		
PLL supply	VDDPLL_0_09 VDDPLL_1_09 VDDPLL_2_09 VDDPLL_3_09 VDDPLL_HDMI_09	0.9 ± 10%	0.17
DDR supply	VDDQ_DDR0, VDDQ_DDR1	DDR3: 1.5 ± 5% DDR4: 1.2 ± 5%	3.0
1.5V voltage supply	VDD_PCIE4_0_15 VDD_PCIE4_1_15 VDD_PCIE8_15 VDD_XG0_15 VDD_XG1_15	1.5 ± 5%	1.0

Table 3-1 BE-M1000 Power Domains (continued)

Supply Type	Package Pin Name	Voltage, V	Max Power, W
1.8V voltage supply	VDD_DDR0_PLL VDD_DDR1_PLL VDD_HDMI_18 VDD_PVT_18 VDD_SATA_18 VDD_USB2_18 VDDIO	1.8 ± 10%	0.6
3.3V voltage supply	VDD_SD_33 VDD_USB2_0_33 VDD_USB2_1_33 VDD_USB2_2_33 VDD_USB2_3_33 VDD_USB3_33	3.3 -6.9% +4.8%	0.7
Ground	VSS	-	-
Total			**~28.47 W**

3.2 External Clocking

3.2.1 Reference Clock Signals

Table 3-2 Reference Clock Signals

Clock Signal	Pin Names	Frequency	Notes
Reference clock	CLK25M	25 MHz	-
XGbE PHY reference clock	XG0_REF_CLKN XG0_REF_CLKP XG1_REF_CLKN XG1_REF_CLKP	156.25 MHz	Diff. pair
PCIe PHY reference clock	PCIE4_0_REF_CLKN PCIE4_0_REF_CLKP PCIE4_1_REF_CLKN PCIE4_1_REF_CLKP PCIE8_REF_CLKN PCIE8_REF_CLKP	100 MHz	Diff. pair
SATA PHY reference clock	SATA_REFCLKP SATA_REFCLKM	100 MHz	Diff. pair

Table 3-2 Reference Clock Signals (continued)

Clock Signal	Pin Names	Frequency	Notes
USB3 PHY optional reference clock input	USB3_0_REFCLKN USB3_0_REFCLKP USB3_1_REFCLKN USB3_1_REFCLKP	100 MHz (typical)	Diff. pair
USB2 PHY: XI - crystal oscillator XO - crystal oscillator or board reference clock input	USB2_0_XI USB2_0_XO USB2_1_XI USB2_1_XO USB2_2_XI USB2_2_XO USB2_3_XI USB2_3_XO	50 MHz	
HDMI PLL reference clock input	HDMI_PLL_27M	27 MHz	
LVDS PLL reference clock input	LVDS_PLL_27M	27 MHz	

NOTE:

1 If the reference clock pins are unused, they should be tied off to the ground potential

2 Reference clocks connect as needed

3.2.2 Reference Clock Requirements

3.2.2.1 Reference Clock (CLK25M)

Table 3-3 Reference Clock (CLK25M) Requirements

Parameter	Min	Typ	Max	Unit
Frequency range		25		MHz
Reference clock frequency offset	-50		50	ppm
Reference clock random jitter (RMS)		10		ps
Reference clock cycle to cycle jitter		6		ps
Startup time		1.5	3.0	ms
Disable time		20	100	ns
Disable Stand-by current			15	uA

3.2.2.2 SATA PHY Reference Clock

Table 3-4 SATA PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	

Table 3-4 SATA PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock frequency offset	-350		350	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock cycle to cycle jitter			150	ps	DJ across all frequencies
Duty cycle	40		60	%	
Common mode input level	0		vp	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs[1]
Single-ended input logic low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic high	vp-0.3		vp+0.3	V	If single-ended input is used
Input edge rate	0.6			V/ns	
Reference clock skew (±)			200	ps	

3.2.2.3 XGbE PHY Reference Clock

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The chosen reference clock must meet specific requirements for signal swing and jitter. The following table summarizes the requirements of the reference clock provided to the PHY.

Table 3-5 XGbE PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		156.25		MHz	
Frequency stability	-100		100	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12 kHz to 20 MHz
Allowed jitter for 10GBASE-KX4			3.6	ps (rms)	Integrated from 12 kHz to 20 MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples

[1] VDREF_CLK / 4 + VCMREF_CLK ≤ vp + diode forward-biasing voltage and VCMREF_CLK-VDREF_CLK/4 ≥ - diode forward biasing voltage

Table 3-5 XGbE PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

3.2.2.4 PCIe PHY Reference Clock

Table 3-6 PCIe PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Frequency stability	-300		300	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling

NOTE: 100 MHz is the only PCIe standard compliant frequency. When using a 125 MHz frequency, the PHY may not be compliant to all PCIe specifications, such as PLL bandwidth, peaking, and jitter

3.2.2.5 USB3 PHY Reference Clock

The USB 3.0 PHY is designed to handle a wide range of input clock frequencies to support both host and device applications. The following table summarizes the requirements of the reference clock provided to the USB 3.0 PHY to support SuperSpeed only or both SuperSpeed and high-speed operations.

Table 3-7 USB3 PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock frequency	19.2	100	200	MHz	
Reference clock frequency stability	-300		300	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock skew			200	ps	
Reference clock cycle-to-cycle jitter			150	ps	DJ over all frequency
Duty cycle	40		60	%	
Common mode input level	0		1.32	V	Differential inputs

Table 3-7 USB3 PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Differential input swing	0.3			Vpp	Differential inputs[2]
Single-ended input logic: Low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic: High	vp-0.3		vp	V	If single-ended input is used
Input edge rate	0.6		4	V/ns	
Required external reference resistance		200		Ohms	± 1% accuracy

3.2.2.6 USB2 PHY Reference Clock

The USB2 PHY supports the following reference clock sources:

- **Crystal Oscillator connected to the USB2_*_XI and USB2_*_XO pins**: The crystal oscillator must have a frequency tolerance of ±400 ppm, peak jitter of ±100 ps, and an output differential voltage of no less than 500 mV with respect to the XI signal
- **External Clock connected to the USB2_*_XO pin**: The clock must have a fundamental frequency of 50 MHz, with a frequency tolerance of ± 400 ppm, peak jitter of ± 100 ps, duty cycle between 40/60 and 60/40 percent, and signal swing of 1.8V

3.2.2.7 HDMI PLL Reference Clock

Table 3-8 HDMI PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

3.2.2.8 LVDS PLL Reference Clock

Table 3-9 LVDS PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

[2] VDREF_CLK / 4 + VCMREF_CLK ≤ vp + diode forward biasing voltage and VCMREF_CLK – VDREF_CLK / 4 ≥ –diode forward biasing voltage

4 Power-Up/Down

4.1 Power-Up Sequence

The following steps have to be performed to power up the SoC:

1. Provide the RESET_N reset signal (active is low)
2. Apply voltages to power pins according to Power Requirements in the following order:
   - 3.3V voltage supply
   - 1.5V voltage supply
   - PLL supply
   - DDR supply
3. Provide the CS_TRST_N reset signal
4. Provide the TRSTN reset signal
5. Apply voltages to power pins according to Power Requirements in the following order:
   - 1.8V voltage supply
   - Core supply and 0.95V voltage supply
6. Provide all reference clocks
7. Wait at least 16 cycles of the reference clock
8. Deassert the RESET_N signal

Once the RESET_N signal is deasserted, the boot controller provides initialization of clock and reset signals for each SoC subsystem, loads and executes the Boot Loader, which is stored in the Boot SPI Flash.

4.2 Power-Down Sequence

Power-down sequence is the reverse of the power-up sequence.

5 Pin Assignment

5.1 Pinout List

The table below contains the list of I/O pins of the chip including the power-ground supplies.

Legend:

I	Input
O	Output
IO	Input/Output
A	Analog
P	Power supply
G	Ground
NC	Not connected

Table 5-1 Pinout List

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1	AG18	ARC_DBG_TF	SCM	O	VDDIO_18	Indicates that a triple fault exception has occurred
2	AH18	ARC_WDT_RESET	SCM	O	VDDIO_18	Watchdog reset
3	AM18	BOOT_ERR	SCM	O	VDDIO_18	Internal SRAM data loading CRC error
4	A32	CLK24M_OUT	SYSTEM	O	VDDIO_18	Output clock 48 MHz/2, In some USB purposes
5	AJ16	CLK25M	SYSTEM	I	VDDIO_18	PLL Reference Clock 25 MHz
6	AG15	CS_CLK	DEBUG	O	VDDIO_18	Trace port clock
7	AG16	CS_CTRL	DEBUG	O	VDDIO_18	Trace port control
8	AE5	CS_DAT[0]	DEBUG	O	VDDIO_18	Trace port data
9	AE6	CS_DAT[1]	DEBUG	O	VDDIO_18	Trace port data
10	AF12	CS_DAT[10]	DEBUG	O	VDDIO_18	Trace port data
11	AG6	CS_DAT[11]	DEBUG	O	VDDIO_18	Trace port data
12	AG7	CS_DAT[12]	DEBUG	O	VDDIO_18	Trace port data
13	AG8	CS_DAT[13]	DEBUG	O	VDDIO_18	Trace port data
14	AG10	CS_DAT[14]	DEBUG	O	VDDIO_18	Trace port data
15	AG11	CS_DAT[15]	DEBUG	O	VDDIO_18	Trace port data
16	AE9	CS_DAT[2]	DEBUG	O	VDDIO_18	Trace port data
17	AE10	CS_DAT[3]	DEBUG	O	VDDIO_18	Trace port data
18	AE11	CS_DAT[4]	DEBUG	O	VDDIO_18	Trace port data
19	AF6	CS_DAT[5]	DEBUG	O	VDDIO_18	Trace port data
20	AF7	CS_DAT[6]	DEBUG	O	VDDIO_18	Trace port data
21	AF9	CS_DAT[7]	DEBUG	O	VDDIO_18	Trace port data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
22	AF10	CS_DAT[8]	DEBUG	O	VDDIO_18	Trace port data
23	AF11	CS_DAT[9]	DEBUG	O	VDDIO_18	Trace port data
24	AE12	CS_SWCLK_TCK	DEBUG	I	VDDIO_18	Serial wire and TAP clock
25	AF13	CS_SWDIO_TMS	DEBUG	IO	VDDIO_18	Combined serial wire input/output
26	AG13	CS_TDI	DEBUG	I	VDDIO_18	JTAG TAP Data in
27	AH17	CS_TDO	DEBUG	O	VDDIO_18	JTAG TAP Data out
28	AG14	CS_TRST_N	DEBUG	I	VDDIO_18	TAP Asynchronous reset
29	K12	DDR0_A[0]	DDR	O	VDDQ_DDR0	SDRAM Address
30	M13	DDR0_A[1]	DDR	O	VDDQ_DDR0	SDRAM Address
31	AA9	DDR0_A[10]	DDR	O	VDDQ_DDR0	SDRAM Address
32	AC11	DDR0_A[11]	DDR	O	VDDQ_DDR0	SDRAM Address
33	Y13	DDR0_A[12]	DDR	O	VDDQ_DDR0	SDRAM Address
34	AC12	DDR0_A[13]	DDR	O	VDDQ_DDR0	SDRAM Address
35	AA11	DDR0_A[14]	DDR	O	VDDQ_DDR0	SDRAM WE
36	Y10	DDR0_A[15]	DDR	O	VDDQ_DDR0	SDRAM CAS
37	AB11	DDR0_A[16]	DDR	O	VDDQ_DDR0	SDRAM RAS
38	AA8	DDR0_A[17]	DDR	O	VDDQ_DDR0	SDRAM A[17]
39	J12	DDR0_A[2]	DDR	O	VDDQ_DDR0	SDRAM Address
40	T12	DDR0_A[3]	DDR	O	VDDQ_DDR0	SDRAM Address
41	L14	DDR0_A[4]	DDR	O	VDDQ_DDR0	SDRAM Address
42	AB12	DDR0_A[5]	DDR	O	VDDQ_DDR0	SDRAM Address
43	V13	DDR0_A[6]	DDR	O	VDDQ_DDR0	SDRAM Address
44	AB10	DDR0_A[7]	DDR	O	VDDQ_DDR0	SDRAM Address
45	V11	DDR0_A[8]	DDR	O	VDDQ_DDR0	SDRAM Address
46	Y11	DDR0_A[9]	DDR	O	VDDQ_DDR0	SDRAM Address
47	H10	DDR0_ACT_N	DDR	O	VDDQ_DDR0	When low, indicates the activate (open row) command
48	U12	DDR0_ALERT_N	DDR	I	VDDQ_DDR0	SDRAM CRC/Parity Error
49	U11	DDR0_ATO	DDR	A		Analog Test Output (test Pad)
50	J13	DDR0_BA[0]	DDR	O	VDDQ_DDR0	SDRAM Bank Address
51	J10	DDR0_BA[1]	DDR	O	VDDQ_DDR0	SDRAM Bank Address
52	U7	DDR0_BG[0]	DDR	O	VDDQ_DDR0	SDRAM Bank Group

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
53	M12	DDR0_BG[1]	DDR	O	VDDQ_DDR0	SDRAM Bank Group
54	L9	DDR0_CK[0]	DDR	O	VDDQ_DDR0	SDRAM Clock
55	M11	DDR0_CK[1]	DDR	O	VDDQ_DDR0	SDRAM Clock
56	N10	DDR0_CK[2]	DDR	O	VDDQ_DDR0	SDRAM Clock
57	P11	DDR0_CK[3]	DDR	O	VDDQ_DDR0	SDRAM Clock
58	M9	DDR0_CK_N[0]	DDR	O	VDDQ_DDR0	SDRAM Clock
59	L11	DDR0_CK_N[1]	DDR	O	VDDQ_DDR0	SDRAM Clock
60	P10	DDR0_CK_N[2]	DDR	O	VDDQ_DDR0	SDRAM Clock
61	R11	DDR0_CK_N[3]	DDR	O	VDDQ_DDR0	SDRAM Clock
62	R12	DDR0_CKE[0]	DDR	O	VDDQ_DDR0	SDRAM Clock enable
63	N13	DDR0_CKE[1]	DDR	O	VDDQ_DDR0	SDRAM Clock enable
64	AB13	DDR0_CKE[2]	DDR	O	VDDQ_DDR0	SDRAM Clock enable
65	W10	DDR0_CKE[3]	DDR	O	VDDQ_DDR0	SDRAM Clock enable
66	L13	DDR0_CS_N[0]	DDR	O	VDDQ_DDR0	SDRAM Chip Select
67	P13	DDR0_CS_N[1]	DDR	O	VDDQ_DDR0	SDRAM Chip Select
68	W9	DDR0_CS_N[2]	DDR	O	VDDQ_DDR0	SDRAM Chip Select
69	U10	DDR0_CS_N[3]	DDR	O	VDDQ_DDR0	SDRAM Chip Select
70	AB8	DDR0_DM[0]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
71	AC4	DDR0_DM[1]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
72	Y7	DDR0_DM[2]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
73	T2	DDR0_DM[3]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
74	L8	DDR0_DM[4]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
75	N3	DDR0_DM[5]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
76	K7	DDR0_DM[6]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
77	J3	DDR0_DM[7]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
78	P2	DDR0_DM[8]	DDR	IO	VDDQ_DDR0	SDRAM Data Mask
79	AD5	DDR0_DQ[0]	DDR	IO	VDDQ_DDR0	SDRAM Data
80	AB7	DDR0_DQ[1]	DDR	IO	VDDQ_DDR0	SDRAM Data
81	Y3	DDR0_DQ[10]	DDR	IO	VDDQ_DDR0	SDRAM Data
82	Y4	DDR0_DQ[11]	DDR	IO	VDDQ_DDR0	SDRAM Data
83	AB1	DDR0_DQ[12]	DDR	IO	VDDQ_DDR0	SDRAM Data
84	AB2	DDR0_DQ[13]	DDR	IO	VDDQ_DDR0	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
85	AB3	DDR0_DQ[14]	DDR	IO	VDDQ_DDR0	SDRAM Data
86	AB4	DDR0_DQ[15]	DDR	IO	VDDQ_DDR0	SDRAM Data
87	V6	DDR0_DQ[16]	DDR	IO	VDDQ_DDR0	SDRAM Data
88	V5	DDR0_DQ[17]	DDR	IO	VDDQ_DDR0	SDRAM Data
89	Y5	DDR0_DQ[18]	DDR	IO	VDDQ_DDR0	SDRAM Data
90	Y8	DDR0_DQ[19]	DDR	IO	VDDQ_DDR0	SDRAM Data
91	AB6	DDR0_DQ[2]	DDR	IO	VDDQ_DDR0	SDRAM Data
92	V7	DDR0_DQ[20]	DDR	IO	VDDQ_DDR0	SDRAM Data
93	U5	DDR0_DQ[21]	DDR	IO	VDDQ_DDR0	SDRAM Data
94	W8	DDR0_DQ[22]	DDR	IO	VDDQ_DDR0	SDRAM Data
95	Y6	DDR0_DQ[23]	DDR	IO	VDDQ_DDR0	SDRAM Data
96	V3	DDR0_DQ[24]	DDR	IO	VDDQ_DDR0	SDRAM Data
97	V4	DDR0_DQ[25]	DDR	IO	VDDQ_DDR0	SDRAM Data
98	T3	DDR0_DQ[26]	DDR	IO	VDDQ_DDR0	SDRAM Data
99	T1	DDR0_DQ[27]	DDR	IO	VDDQ_DDR0	SDRAM Data
100	V2	DDR0_DQ[28]	DDR	IO	VDDQ_DDR0	SDRAM Data
101	W4	DDR0_DQ[29]	DDR	IO	VDDQ_DDR0	SDRAM Data
102	AB5	DDR0_DQ[3]	DDR	IO	VDDQ_DDR0	SDRAM Data
103	T4	DDR0_DQ[30]	DDR	IO	VDDQ_DDR0	SDRAM Data
104	V1	DDR0_DQ[31]	DDR	IO	VDDQ_DDR0	SDRAM Data
105	L5	DDR0_DQ[32]	DDR	IO	VDDQ_DDR0	SDRAM Data
106	L6	DDR0_DQ[33]	DDR	IO	VDDQ_DDR0	SDRAM Data
107	L7	DDR0_DQ[34]	DDR	IO	VDDQ_DDR0	SDRAM Data
108	M8	DDR0_DQ[35]	DDR	IO	VDDQ_DDR0	SDRAM Data
109	N5	DDR0_DQ[36]	DDR	IO	VDDQ_DDR0	SDRAM Data
110	N6	DDR0_DQ[37]	DDR	IO	VDDQ_DDR0	SDRAM Data
111	N7	DDR0_DQ[38]	DDR	IO	VDDQ_DDR0	SDRAM Data
112	N8	DDR0_DQ[39]	DDR	IO	VDDQ_DDR0	SDRAM Data
113	AD7	DDR0_DQ[4]	DDR	IO	VDDQ_DDR0	SDRAM Data
114	K1	DDR0_DQ[40]	DDR	IO	VDDQ_DDR0	SDRAM Data
115	K2	DDR0_DQ[41]	DDR	IO	VDDQ_DDR0	SDRAM Data
116	K3	DDR0_DQ[42]	DDR	IO	VDDQ_DDR0	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
117	L4	DDR0_DQ[43]	DDR	IO	VDDQ_DDR0	SDRAM Data
118	M1	DDR0_DQ[44]	DDR	IO	VDDQ_DDR0	SDRAM Data
119	M2	DDR0_DQ[45]	DDR	IO	VDDQ_DDR0	SDRAM Data
120	M3	DDR0_DQ[46]	DDR	IO	VDDQ_DDR0	SDRAM Data
121	N4	DDR0_DQ[47]	DDR	IO	VDDQ_DDR0	SDRAM Data
122	J5	DDR0_DQ[48]	DDR	IO	VDDQ_DDR0	SDRAM Data
123	J7	DDR0_DQ[49]	DDR	IO	VDDQ_DDR0	SDRAM Data
124	AD6	DDR0_DQ[5]	DDR	IO	VDDQ_DDR0	SDRAM Data
125	J8	DDR0_DQ[50]	DDR	IO	VDDQ_DDR0	SDRAM Data
126	J6	DDR0_DQ[51]	DDR	IO	VDDQ_DDR0	SDRAM Data
127	G5	DDR0_DQ[52]	DDR	IO	VDDQ_DDR0	SDRAM Data
128	G8	DDR0_DQ[53]	DDR	IO	VDDQ_DDR0	SDRAM Data
129	G6	DDR0_DQ[54]	DDR	IO	VDDQ_DDR0	SDRAM Data
130	G7	DDR0_DQ[55]	DDR	IO	VDDQ_DDR0	SDRAM Data
131	F1	DDR0_DQ[56]	DDR	IO	VDDQ_DDR0	SDRAM Data
132	F2	DDR0_DQ[57]	DDR	IO	VDDQ_DDR0	SDRAM Data
133	F3	DDR0_DQ[58]	DDR	IO	VDDQ_DDR0	SDRAM Data
134	G4	DDR0_DQ[59]	DDR	IO	VDDQ_DDR0	SDRAM Data
135	AD8	DDR0_DQ[6]	DDR	IO	VDDQ_DDR0	SDRAM Data
136	H1	DDR0_DQ[60]	DDR	IO	VDDQ_DDR0	SDRAM Data
137	H2	DDR0_DQ[61]	DDR	IO	VDDQ_DDR0	SDRAM Data
138	H3	DDR0_DQ[62]	DDR	IO	VDDQ_DDR0	SDRAM Data
139	J4	DDR0_DQ[63]	DDR	IO	VDDQ_DDR0	SDRAM Data
140	AC8	DDR0_DQ[7]	DDR	IO	VDDQ_DDR0	SDRAM Data
141	Y1	DDR0_DQ[8]	DDR	IO	VDDQ_DDR0	SDRAM Data
142	Y2	DDR0_DQ[9]	DDR	IO	VDDQ_DDR0	SDRAM Data
143	AC6	DDR0_DQS[0]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
144	AA2	DDR0_DQS[1]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
145	W5	DDR0_DQS[2]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
146	U2	DDR0_DQS[3]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
147	M5	DDR0_DQS[4]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
148	L2	DDR0_DQS[5]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
149	H5	DDR0_DQS[6]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
150	G1	DDR0_DQS[7]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
151	P3	DDR0_DQS[8]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
152	AC5	DDR0_DQS_N[0]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
153	AA1	DDR0_DQS_N[1]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
154	W6	DDR0_DQS_N[2]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
155	U1	DDR0_DQS_N[3]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
156	M6	DDR0_DQS_N[4]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
157	L1	DDR0_DQS_N[5]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
158	H6	DDR0_DQS_N[6]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
159	G2	DDR0_DQS_N[7]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
160	R3	DDR0_DQS_N[8]	DDR	IO	VDDQ_DDR0	SDRAM Data Strobe
161	K10	DDR0_DTO[0]	DDR	O	VDDQ_DDR0	Digital Test Output (test Pad)
162	J9	DDR0_DTO[1]	DDR	O	VDDQ_DDR0	Digital Test Output (test Pad)
163	T6	DDR0_ECC[0]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
164	R6	DDR0_ECC[1]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
165	P6	DDR0_ECC[2]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
166	R5	DDR0_ECC[3]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
167	P1	DDR0_ECC[4]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
168	R1	DDR0_ECC[5]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
169	R2	DDR0_ECC[6]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
170	T5	DDR0_ECC[7]	DDR	IO	VDDQ_DDR0	SDRAM Data ECC
171	K13	DDR0_MIRROR	DDR	O	VDDQ_DDR0	SDRAM Mirror (optional DIMM signal)
172	AA13	DDR0_ODT[0]	DDR	O	VDDQ_DDR0	SDRAM On-Die termination
173	AC9	DDR0_ODT[1]	DDR	O	VDDQ_DDR0	SDRAM On-Die termination
174	V9	DDR0_ODT[2]	DDR	O	VDDQ_DDR0	SDRAM On-Die termination
175	P8	DDR0_ODT[3]	DDR	O	VDDQ_DDR0	SDRAM On-Die termination
176	T10	DDR0_PARITY	DDR	O	VDDQ_DDR0	SDRAM Parity
177	N12	DDR0_QCSEN_N	DDR	O	VDDQ_DDR0	SDRAM Quad CS Enable (optional DIMM signal)
178	J11	DDR0_RAM_RST_N	DDR	O	VDDQ_DDR0	SDRAM Reset
179	V12	DDR0_VREFI[0]	DDR	A		IO ring VREFI net

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
180	AB9	DDR0_VREFI[1]	DDR	A		IO ring VREFI net
181	W12	DDR0_VREFI[2]	DDR	A		IO ring VREFI net
182	T7	DDR0_VREFI[3]	DDR	A		IO ring VREFI net
183	R8	DDR0_VREFI[4]	DDR	A		IO ring VREFI net
184	K8	DDR0_VREFI[5]	DDR	A		IO ring VREFI net
185	P14	DDR0_VREFI[6]	DDR	A		IO ring VREFI net
186	L10	DDR0_VREFI[7]	DDR	A		IO ring VREFI net
187	U8	DDR0_VREFI[8]	DDR	A		IO ring VREFI net
188	T9	DDR0_VREFI[9]	DDR	A		IO ring VREFI net
189	AC10	DDR0_VREFI_ZQ	DDR	A		IO ring VREFI ZQ net
190	AC13	DDR0_ZQ	DDR	A		ZQ Resistor (to external calibration resistor)
191	AM27	DDR1_A[0]	DDR	O	VDDQ_DDR1	SDRAM Address
192	AT22	DDR1_A[1]	DDR	O	VDDQ_DDR1	SDRAM Address
193	AL25	DDR1_A[10]	DDR	O	VDDQ_DDR1	SDRAM Address
194	AL23	DDR1_A[11]	DDR	O	VDDQ_DDR1	SDRAM Address
195	AL32	DDR1_A[12]	DDR	O	VDDQ_DDR1	SDRAM Address
196	AM23	DDR1_A[13]	DDR	O	VDDQ_DDR1	SDRAM Address
197	AK28	DDR1_A[14]	DDR	O	VDDQ_DDR1	SDRAM WE
198	AN32	DDR1_A[15]	DDR	O	VDDQ_DDR1	SDRAM CAS
199	AM26	DDR1_A[16]	DDR	O	VDDQ_DDR1	SDRAM RAS
200	AN31	DDR1_A[17]	DDR	O	VDDQ_DDR1	SDRAM A[17]
201	AR22	DDR1_A[2]	DDR	O	VDDQ_DDR1	SDRAM Address
202	AM24	DDR1_A[3]	DDR	O	VDDQ_DDR1	SDRAM Address
203	AP21	DDR1_A[4]	DDR	O	VDDQ_DDR1	SDRAM Address
204	AL22	DDR1_A[5]	DDR	O	VDDQ_DDR1	SDRAM Address
205	AM31	DDR1_A[6]	DDR	O	VDDQ_DDR1	SDRAM Address
206	AM25	DDR1_A[7]	DDR	O	VDDQ_DDR1	SDRAM Address
207	AK31	DDR1_A[8]	DDR	O	VDDQ_DDR1	SDRAM Address
208	AL31	DDR1_A[9]	DDR	O	VDDQ_DDR1	SDRAM Address
209	AK25	DDR1_ACT_N	DDR	O	VDDQ_DDR1	When low, indicates the activate (open row) command.
210	AN29	DDR1_ALERT_N	DDR	I	VDDQ_DDR1	SDRAM CRC/Parity Error

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
211	AM30	DDR1_ATO	DDR	A		Analog Test Output (test Pad)
212	AP24	DDR1_BA[0]	DDR	O	VDDQ_DDR1	SDRAM Bank Address
213	AK27	DDR1_BA[1]	DDR	O	VDDQ_DDR1	SDRAM Bank Address
214	AK29	DDR1_BG[0]	DDR	O	VDDQ_DDR1	SDRAM Bank Group
215	AP23	DDR1_BG[1]	DDR	O	VDDQ_DDR1	SDRAM Bank Group
216	AT24	DDR1_CK[0]	DDR	O	VDDQ_DDR1	SDRAM Clock
217	AR26	DDR1_CK[1]	DDR	O	VDDQ_DDR1	SDRAM Clock
218	AR25	DDR1_CK[2]	DDR	O	VDDQ_DDR1	SDRAM Clock
219	AR27	DDR1_CK[3]	DDR	O	VDDQ_DDR1	SDRAM Clock
220	AR24	DDR1_CK_N[0]	DDR	O	VDDQ_DDR1	SDRAM Clock
221	AT26	DDR1_CK_N[1]	DDR	O	VDDQ_DDR1	SDRAM Clock
222	AP25	DDR1_CK_N[2]	DDR	O	VDDQ_DDR1	SDRAM Clock
223	AP27	DDR1_CK_N[3]	DDR	O	VDDQ_DDR1	SDRAM Clock
224	AU21	DDR1_CKE[0]	DDR	O	VDDQ_DDR1	SDRAM Clock enable
225	AT21	DDR1_CKE[1]	DDR	O	VDDQ_DDR1	SDRAM Clock enable
226	AN28	DDR1_CKE[2]	DDR	O	VDDQ_DDR1	SDRAM Clock enable
227	AK30	DDR1_CKE[3]	DDR	O	VDDQ_DDR1	SDRAM Clock enable
228	AV22	DDR1_CS_N[0]	DDR	O	VDDQ_DDR1	SDRAM Chip Select
229	AW22	DDR1_CS_N[1]	DDR	O	VDDQ_DDR1	SDRAM Chip Select
230	AV21	DDR1_CS_N[2]	DDR	O	VDDQ_DDR1	SDRAM Chip Select
231	AN26	DDR1_CS_N[3]	DDR	O	VDDQ_DDR1	SDRAM Chip Select
232	AW34	DDR1_DM[0]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
233	AW25	DDR1_DM[1]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
234	AV38	DDR1_DM[2]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
235	AV29	DDR1_DM[3]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
236	AN34	DDR1_DM[4]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
237	AN37	DDR1_DM[5]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
238	AJ36	DDR1_DM[6]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
239	AJ37	DDR1_DM[7]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
240	AR32	DDR1_DM[8]	DDR	IO	VDDQ_DDR1	SDRAM Data Mask
241	AV32	DDR1_DQ[0]	DDR	IO	VDDQ_DDR1	SDRAM Data
242	AW32	DDR1_DQ[1]	DDR	IO	VDDQ_DDR1	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
243	AU25	DDR1_DQ[10]	DDR	IO	VDDQ_DDR1	SDRAM Data
244	AV25	DDR1_DQ[11]	DDR	IO	VDDQ_DDR1	SDRAM Data
245	AU23	DDR1_DQ[12]	DDR	IO	VDDQ_DDR1	SDRAM Data
246	AW23	DDR1_DQ[13]	DDR	IO	VDDQ_DDR1	SDRAM Data
247	AW24	DDR1_DQ[14]	DDR	IO	VDDQ_DDR1	SDRAM Data
248	AV23	DDR1_DQ[15]	DDR	IO	VDDQ_DDR1	SDRAM Data
249	AW36	DDR1_DQ[16]	DDR	IO	VDDQ_DDR1	SDRAM Data
250	AU36	DDR1_DQ[17]	DDR	IO	VDDQ_DDR1	SDRAM Data
251	AV36	DDR1_DQ[18]	DDR	IO	VDDQ_DDR1	SDRAM Data
252	AU38	DDR1_DQ[19]	DDR	IO	VDDQ_DDR1	SDRAM Data
253	AU32	DDR1_DQ[2]	DDR	IO	VDDQ_DDR1	SDRAM Data
254	AV39	DDR1_DQ[20]	DDR	IO	VDDQ_DDR1	SDRAM Data
255	AU39	DDR1_DQ[21]	DDR	IO	VDDQ_DDR1	SDRAM Data
256	AW39	DDR1_DQ[22]	DDR	IO	VDDQ_DDR1	SDRAM Data
257	AW37	DDR1_DQ[23]	DDR	IO	VDDQ_DDR1	SDRAM Data
258	AU27	DDR1_DQ[24]	DDR	IO	VDDQ_DDR1	SDRAM Data
259	AW27	DDR1_DQ[25]	DDR	IO	VDDQ_DDR1	SDRAM Data
260	AV27	DDR1_DQ[26]	DDR	IO	VDDQ_DDR1	SDRAM Data
261	AW28	DDR1_DQ[27]	DDR	IO	VDDQ_DDR1	SDRAM Data
262	AU29	DDR1_DQ[28]	DDR	IO	VDDQ_DDR1	SDRAM Data
263	AU30	DDR1_DQ[29]	DDR	IO	VDDQ_DDR1	SDRAM Data
264	AW33	DDR1_DQ[3]	DDR	IO	VDDQ_DDR1	SDRAM Data
265	AW30	DDR1_DQ[30]	DDR	IO	VDDQ_DDR1	SDRAM Data
266	AV30	DDR1_DQ[31]	DDR	IO	VDDQ_DDR1	SDRAM Data
267	AN35	DDR1_DQ[32]	DDR	IO	VDDQ_DDR1	SDRAM Data
268	AM35	DDR1_DQ[33]	DDR	IO	VDDQ_DDR1	SDRAM Data
269	AM36	DDR1_DQ[34]	DDR	IO	VDDQ_DDR1	SDRAM Data
270	AR36	DDR1_DQ[35]	DDR	IO	VDDQ_DDR1	SDRAM Data
271	AM34	DDR1_DQ[36]	DDR	IO	VDDQ_DDR1	SDRAM Data
272	AR35	DDR1_DQ[37]	DDR	IO	VDDQ_DDR1	SDRAM Data
273	AR34	DDR1_DQ[38]	DDR	IO	VDDQ_DDR1	SDRAM Data
274	AP34	DDR1_DQ[39]	DDR	IO	VDDQ_DDR1	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
275	AU34	DDR1_DQ[4]	DDR	IO	VDDQ_DDR1	SDRAM Data
276	AP37	DDR1_DQ[40]	DDR	IO	VDDQ_DDR1	SDRAM Data
277	AR37	DDR1_DQ[41]	DDR	IO	VDDQ_DDR1	SDRAM Data
278	AR38	DDR1_DQ[42]	DDR	IO	VDDQ_DDR1	SDRAM Data
279	AR39	DDR1_DQ[43]	DDR	IO	VDDQ_DDR1	SDRAM Data
280	AM37	DDR1_DQ[44]	DDR	IO	VDDQ_DDR1	SDRAM Data
281	AN39	DDR1_DQ[45]	DDR	IO	VDDQ_DDR1	SDRAM Data
282	AN38	DDR1_DQ[46]	DDR	IO	VDDQ_DDR1	SDRAM Data
283	AM38	DDR1_DQ[47]	DDR	IO	VDDQ_DDR1	SDRAM Data
284	AH34	DDR1_DQ[48]	DDR	IO	VDDQ_DDR1	SDRAM Data
285	AL36	DDR1_DQ[49]	DDR	IO	VDDQ_DDR1	SDRAM Data
286	AV34	DDR1_DQ[5]	DDR	IO	VDDQ_DDR1	SDRAM Data
287	AL34	DDR1_DQ[50]	DDR	IO	VDDQ_DDR1	SDRAM Data
288	AK34	DDR1_DQ[51]	DDR	IO	VDDQ_DDR1	SDRAM Data
289	AL35	DDR1_DQ[52]	DDR	IO	VDDQ_DDR1	SDRAM Data
290	AH36	DDR1_DQ[53]	DDR	IO	VDDQ_DDR1	SDRAM Data
291	AH35	DDR1_DQ[54]	DDR	IO	VDDQ_DDR1	SDRAM Data
292	AJ34	DDR1_DQ[55]	DDR	IO	VDDQ_DDR1	SDRAM Data
293	AH37	DDR1_DQ[56]	DDR	IO	VDDQ_DDR1	SDRAM Data
294	AL37	DDR1_DQ[57]	DDR	IO	VDDQ_DDR1	SDRAM Data
295	AL38	DDR1_DQ[58]	DDR	IO	VDDQ_DDR1	SDRAM Data
296	AL39	DDR1_DQ[59]	DDR	IO	VDDQ_DDR1	SDRAM Data
297	AU35	DDR1_DQ[6]	DDR	IO	VDDQ_DDR1	SDRAM Data
298	AH38	DDR1_DQ[60]	DDR	IO	VDDQ_DDR1	SDRAM Data
299	AK37	DDR1_DQ[61]	DDR	IO	VDDQ_DDR1	SDRAM Data
300	AJ38	DDR1_DQ[62]	DDR	IO	VDDQ_DDR1	SDRAM Data
301	AH39	DDR1_DQ[63]	DDR	IO	VDDQ_DDR1	SDRAM Data
302	AV35	DDR1_DQ[7]	DDR	IO	VDDQ_DDR1	SDRAM Data
303	AU26	DDR1_DQ[8]	DDR	IO	VDDQ_DDR1	SDRAM Data
304	AV26	DDR1_DQ[9]	DDR	IO	VDDQ_DDR1	SDRAM Data
305	AU33	DDR1_DQS[0]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
306	AU24	DDR1_DQS[1]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
307	AU37	DDR1_DQS[2]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
308	AU28	DDR1_DQS[3]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
309	AP36	DDR1_DQS[4]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
310	AP38	DDR1_DQS[5]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
311	AJ35	DDR1_DQS[6]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
312	AK38	DDR1_DQS[7]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
313	AR30	DDR1_DQS[8]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
314	AV33	DDR1_DQS_N[0]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
315	AV24	DDR1_DQS_N[1]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
316	AV37	DDR1_DQS_N[2]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
317	AV28	DDR1_DQS_N[3]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
318	AP35	DDR1_DQS_N[4]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
319	AP39	DDR1_DQS_N[5]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
320	AK35	DDR1_DQS_N[6]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
321	AK39	DDR1_DQS_N[7]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
322	AP30	DDR1_DQS_N[8]	DDR	IO	VDDQ_DDR1	SDRAM Data Strobe
323	AK26	DDR1_DTO[0]	DDR	O	VDDQ_DDR1	Digital Test Output (test Pad)
324	AK24	DDR1_DTO[1]	DDR	O	VDDQ_DDR1	Digital Test Output (test Pad)
325	AT30	DDR1_ECC[0]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
326	AR29	DDR1_ECC[1]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
327	AT29	DDR1_ECC[2]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
328	AT31	DDR1_ECC[3]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
329	AP29	DDR1_ECC[4]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
330	AP31	DDR1_ECC[5]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
331	AT32	DDR1_ECC[6]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
332	AP32	DDR1_ECC[7]	DDR	IO	VDDQ_DDR1	SDRAM Data ECC
333	AP22	DDR1_MIRROR	DDR	O	VDDQ_DDR1	SDRAM Mirror (optional DIMM signal)
334	AK22	DDR1_ODT[0]	DDR	O	VDDQ_DDR1	SDRAM On-Die termination
335	AM28	DDR1_ODT[1]	DDR	O	VDDQ_DDR1	SDRAM On-Die termination
336	AW21	DDR1_ODT[2]	DDR	O	VDDQ_DDR1	SDRAM On-Die termination
337	AM22	DDR1_ODT[3]	DDR	O	VDDQ_DDR1	SDRAM On-Die termination

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
338	AL27	DDR1_PARITY	DDR	O	VDDQ_DDR1	SDRAM Parity
339	AN22	DDR1_QCSEN_N	DDR	O	VDDQ_DDR1	SDRAM Quad CS Enable (optional DIMM signal)
340	AN24	DDR1_RAM_RST_N	DDR	O	VDDQ_DDR1	SDRAM Reset
341	AJ22	DDR1_VREFI[0]	DDR	A		IO ring VREFI net
342	AG23	DDR1_VREFI[1]	DDR	A		IO ring VREFI net
343	AG24	DDR1_VREFI[2]	DDR	A		IO ring VREFI net
344	AG25	DDR1_VREFI[3]	DDR	A		IO ring VREFI net
345	AG26	DDR1_VREFI[4]	DDR	A		IO ring VREFI net
346	AH27	DDR1_VREFI[5]	DDR	A		IO ring VREFI net
347	AH26	DDR1_VREFI[6]	DDR	A		IO ring VREFI net
348	AJ25	DDR1_VREFI[7]	DDR	A		IO ring VREFI net
349	AJ24	DDR1_VREFI[8]	DDR	A		IO ring VREFI net
350	AH23	DDR1_VREFI[9]	DDR	A		IO ring VREFI net
351	AH22	DDR1_VREFI_ZQ	DDR	A		IO ring VREFI ZQ net
352	AG22	DDR1_ZQ	DDR	A		ZQ Resistor (to external calibration resistor)
353	C35	ESPI_ALERT[0]	LSP	I	VDDIO_18	eSPI Alert
354	C37	ESPI_ALERT[1]	LSP	I	VDDIO_18	eSPI Alert
355	C38	ESPI_ALERT[2]	LSP	I	VDDIO_18	eSPI Alert
356	D35	ESPI_ALERT[3]	LSP	I	VDDIO_18	eSPI Alert
357	D36	ESPI_ALERT[4]	LSP	I	VDDIO_18	eSPI Alert
358	D37	ESPI_ALERT[5]	LSP	I	VDDIO_18	eSPI Alert
359	E35	ESPI_ALERT[6]	LSP	I	VDDIO_18	eSPI Alert
360	E34	ESPI_ALERT[7]	LSP	I	VDDIO_18	eSPI Alert
361	A38	ESPI_CLK	LSP	IO	VDDIO_18	eSPI clock
362	A39	ESPI_DAT[0]	LSP	IO	VDDIO_18	eSPI data
363	B39	ESPI_DAT[1]	LSP	IO	VDDIO_18	eSPI data
364	C39	ESPI_DAT[2]	LSP	IO	VDDIO_18	eSPI data
365	D39	ESPI_DAT[3]	LSP	IO	VDDIO_18	eSPI data
366	D34	ESPI_RST	LSP	IO	VDDIO_18	eSPI reset
367	A35	ESPI_SS_N[0]	LSP	IO	VDDIO_18	eSPI Slave Select
368	A36	ESPI_SS_N[1]	LSP	IO	VDDIO_18	eSPI Slave Select
369	A37	ESPI_SS_N[2]	LSP	IO	VDDIO_18	eSPI Slave Select

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
370	B35	ESPI_SS_N[3]	LSP	IO	VDDIO_18	eSPI Slave Select
371	B36	ESPI_SS_N[4]	LSP	IO	VDDIO_18	eSPI Slave Select
372	B37	ESPI_SS_N[5]	LSP	IO	VDDIO_18	eSPI Slave Select
373	C33	ESPI_SS_N[6]	LSP	IO	VDDIO_18	eSPI Slave Select
374	C34	ESPI_SS_N[7]	LSP	IO	VDDIO_18	eSPI Slave Select
375	E4	G0_GP_IN	GMAC	I	VDDIO_18	GPIO
376	E3	G0_GP_OUT	GMAC	O	VDDIO_18	GPIO
377	E1	G0_MDC	GMAC	O	VDDIO_18	MDIO Interface
378	E2	G0_MDIO	GMAC	IO	VDDIO_18	MDIO Interface
379	C7	G0_RX_CLK	GMAC	I	VDDIO_18	Receive reference clock
380	C5	G0_RX_DAT[0]	GMAC	I	VDDIO_18	Receive Data
381	C6	G0_RX_DAT[1]	GMAC	I	VDDIO_18	Receive Data
382	D5	G0_RX_DAT[2]	GMAC	I	VDDIO_18	Receive Data
383	D6	G0_RX_DAT[3]	GMAC	I	VDDIO_18	Receive Data
384	D7	G0_RX_DEN	GMAC	I	VDDIO_18	Receive Data Enable
385	C4	G0_TX_CLK	GMAC	O	VDDIO_18	Transmit reference clock
386	C1	G0_TX_DAT[0]	GMAC	O	VDDIO_18	Transmit Data
387	C2	G0_TX_DAT[1]	GMAC	O	VDDIO_18	Transmit Data
388	C3	G0_TX_DAT[2]	GMAC	O	VDDIO_18	Transmit Data
389	D2	G0_TX_DAT[3]	GMAC	O	VDDIO_18	Transmit Data
390	D4	G0_TX_DEN	GMAC	O	VDDIO_18	Transmit Data Enable
391	E7	G1_GP_IN	GMAC	I	VDDIO_18	GPIO
392	E8	G1_GP_OUT	GMAC	O	VDDIO_18	GPIO
393	E5	G1_MDC	GMAC	O	VDDIO_18	MDIO Interface
394	E6	G1_MDIO	GMAC	IO	VDDIO_18	MDIO Interface
395	A7	G1_RX_CLK	GMAC	I	VDDIO_18	Receive reference clock
396	A5	G1_RX_DAT[0]	GMAC	I	VDDIO_18	Receive Data
397	A6	G1_RX_DAT[1]	GMAC	I	VDDIO_18	Receive Data
398	B5	G1_RX_DAT[2]	GMAC	I	VDDIO_18	Receive Data
399	B6	G1_RX_DAT[3]	GMAC	I	VDDIO_18	Receive Data
400	B7	G1_RX_DEN	GMAC	I	VDDIO_18	Receive Data Enable
401	A3	G1_TX_CLK	GMAC	O	VDDIO_18	Transmit reference clock

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
402	A1	G1_TX_DAT[0]	GMAC	O	VDDIO_18	Transmit Data
403	A2	G1_TX_DAT[1]	GMAC	O	VDDIO_18	Transmit Data
404	B1	G1_TX_DAT[2]	GMAC	O	VDDIO_18	Transmit Data
405	B2	G1_TX_DAT[3]	GMAC	O	VDDIO_18	Transmit Data
406	B3	G1_TX_DEN	GMAC	O	VDDIO_18	Transmit Data Enable
407	G35	GPIO32[0]	LSP	IO	VDDIO_18	GPIO Data
408	G36	GPIO32[1]	LSP	IO	VDDIO_18	GPIO Data
409	J36	GPIO32[10]	LSP	IO	VDDIO_18	GPIO Data
410	K31	GPIO32[11]	LSP	IO	VDDIO_18	GPIO Data
411	K32	GPIO32[12]	LSP	IO	VDDIO_18	GPIO Data
412	L31	GPIO32[13]	LSP	IO	VDDIO_18	GPIO Data
413	L32	GPIO32[14]	LSP	IO	VDDIO_18	GPIO Data
414	L33	GPIO32[15]	LSP	IO	VDDIO_18	GPIO Data
415	M29	GPIO32[16]	LSP	IO	VDDIO_18	GPIO Data
416	M30	GPIO32[17]	LSP	IO	VDDIO_18	GPIO Data
417	M31	GPIO32[18]	LSP	IO	VDDIO_18	GPIO Data
418	N30	GPIO32[19]	LSP	IO	VDDIO_18	GPIO Data
419	G37	GPIO32[2]	LSP	IO	VDDIO_18	GPIO Data
420	N31	GPIO32[20]	LSP	IO	VDDIO_18	GPIO Data
421	N32	GPIO32[21]	LSP	IO	VDDIO_18	GPIO Data
422	P32	GPIO32[22]	LSP	IO	VDDIO_18	GPIO Data
423	P33	GPIO32[23]	LSP	IO	VDDIO_18	GPIO Data
424	R28	GPIO32[24]	LSP	IO	VDDIO_18	GPIO Data
425	R29	GPIO32[25]	LSP	IO	VDDIO_18	GPIO Data
426	R30	GPIO32[26]	LSP	IO	VDDIO_18	GPIO Data
427	R31	GPIO32[27]	LSP	IO	VDDIO_18	GPIO Data
428	R33	GPIO32[28]	LSP	IO	VDDIO_18	GPIO Data
429	R34	GPIO32[29]	LSP	IO	VDDIO_18	GPIO Data
430	H32	GPIO32[3]	LSP	IO	VDDIO_18	GPIO Data
431	T32	GPIO32[30]	LSP	IO	VDDIO_18	GPIO Data
432	T33	GPIO32[31]	LSP	IO	VDDIO_18	GPIO Data
433	H33	GPIO32[4]	LSP	IO	VDDIO_18	GPIO Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
434	H34	GPIO32[5]	LSP	IO	VDDIO_18	GPIO Data
435	H36	GPIO32[6]	LSP	IO	VDDIO_18	GPIO Data
436	H37	GPIO32[7]	LSP	IO	VDDIO_18	GPIO Data
437	J34	GPIO32[8]	LSP	IO	VDDIO_18	GPIO Data
438	J35	GPIO32[9]	LSP	IO	VDDIO_18	GPIO Data
439	AN17	GPIO8[0]	SM	IO	VDDIO_18	SM GPIO Data
440	AM17	GPIO8[1]	SM	IO	VDDIO_18	SM GPIO Data
441	AK17	GPIO8[2]	SM	IO	VDDIO_18	SM GPIO Data
442	AJ18	GPIO8[3]	SM	IO	VDDIO_18	SM GPIO Data
443	AJ19	GPIO8[4]	SM	IO	VDDIO_18	SM GPIO Data
444	AJ20	GPIO8[5]	SM	IO	VDDIO_18	SM GPIO Data
445	AH19	GPIO8[6]	SM	IO	VDDIO_18	SM GPIO Data
446	AH20	GPIO8[7]	SM	IO	VDDIO_18	SM GPIO Data
447	B8	HDMI_CLKN	MEDIA	O		TMDS clock
448	C8	HDMI_CLKP	MEDIA	O		TMDS clock
449	B9	HDMI_DATN[0]	MEDIA	O		TMDS data
450	E9	HDMI_DATN[1]	MEDIA	O		TMDS data
451	C10	HDMI_DATN[2]	MEDIA	O		TMDS data
452	A9	HDMI_DATP[0]	MEDIA	O		TMDS data
453	D9	HDMI_DATP[1]	MEDIA	O		TMDS data
454	B10	HDMI_DATP[2]	MEDIA	O		TMDS data
455	K18	HDMI_DB_BISTDONE	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
456	J18	HDMI_DB_BISTEN	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
457	L17	HDMI_DB_BISTOK	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
458	M16	HDMI_DB_DAT[0]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
459	N16	HDMI_DB_DAT[1]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
460	M17	HDMI_DB_DAT[2]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
461	N17	HDMI_DB_DAT[3]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
462	N18	HDMI_DB_DAT[4]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
463	P18	HDMI_DB_DAT[5]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
464	M19	HDMI_DB_DAT[6]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
465	N19	HDMI_DB_DAT[7]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
466	P19	HDMI_DB_DAT[8]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
467	M20	HDMI_DB_DAT[9]	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
468	N20	HDMI_DB_EN	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
469	P20	HDMI_DB_ENHPDRXSENSE	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
470	H22	HDMI_DB_EXTERNAL	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
471	N21	HDMI_DB_PDDQ	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
472	J22	HDMI_DB_PHY_RESET	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
473	K22	HDMI_DB_PHYDTB0	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
474	M21	HDMI_DB_PHYDTB1	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
475	P21	HDMI_DB_RXSENSE	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
476	N22	HDMI_DB_SNK_DET_I	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
477	P22	HDMI_DB_SVSRET_MODEZ	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
478	R22	HDMI_DB_TX_PWRON	MEDIA	I	VDDIO_18	HDMI PHY Debug Interface
479	R16	HDMI_DB_TX_READY	MEDIA	O	VDDIO_18	HDMI PHY Debug Interface
480	D10	HDMI_DDCCEC	MEDIA	IO		Ground reference for the Hot Plug Detect signal
481	H9	HDMI_HPD	MEDIA	IO		Hot Plug Detect signal for HDMI
482	T14	HDMI_PLL_27M	MEDIA	I	VDDIO_18	PLL Reference Clock 27MHz IN - HDMI
483	E10	HDMI_RESREF	MEDIA	A		Reference resistor connection
484	G9	HDMI_SCL	MEDIA	IO	VDDIO_18	HDMI I2C clock input
485	G10	HDMI_SDA	MEDIA	IO	VDDIO_18	HDMI I2C data input
486	AL20	I2C0_SCL	SM	IO	VDDIO_18	SM I2C clock
487	AL19	I2C0_SDA	SM	IO	VDDIO_18	SM I2C data
488	G33	I2C1_SCL	LSP	IO	VDDIO_18	LSP I2C1 clock
489	G32	I2C1_SDA	LSP	IO	VDDIO_18	LSP I2C1 data
490	K30	I2C2_SCL	LSP	IO	VDDIO_18	LSP I2C2 clock
491	H30	I2C2_SDA	LSP	IO	VDDIO_18	LSP I2C2 data
492	F32	I2S_SCK	MEDIA	I	VDDIO_18	I2S continuous serial clock
493	G31	I2S_SDI	MEDIA	I	VDDIO_18	I2S serial data input

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
494	F33	I2S_SDO	MEDIA	O	VDDIO_18	I2S serial data output
495	E33	I2S_WS	MEDIA	I	VDDIO_18	I2S word select
496	V33	LED_PWM	MEDIA	O	VDDIO_18	Brightness Control
497	AC39	LVDS_L0_CLKN	MEDIA	O	VDDIO_18	LVDS clock
498	AC38	LVDS_L0_CLKP	MEDIA	O	VDDIO_18	LVDS clock
499	AF37	LVDS_L0_DATN[0]	MEDIA	O	VDDIO_18	LVDS data
500	AE38	LVDS_L0_DATN[1]	MEDIA	O	VDDIO_18	LVDS data
501	AD38	LVDS_L0_DATN[2]	MEDIA	O	VDDIO_18	LVDS data
502	AB37	LVDS_L0_DATN[3]	MEDIA	O	VDDIO_18	LVDS data
503	AA38	LVDS_L0_DATN[4]	MEDIA	O	VDDIO_18	LVDS data
504	AF38	LVDS_L0_DATP[0]	MEDIA	O	VDDIO_18	LVDS data
505	AE39	LVDS_L0_DATP[1]	MEDIA	O	VDDIO_18	LVDS data
506	AD37	LVDS_L0_DATP[2]	MEDIA	O	VDDIO_18	LVDS data
507	AB38	LVDS_L0_DATP[3]	MEDIA	O	VDDIO_18	LVDS data
508	AA39	LVDS_L0_DATP[4]	MEDIA	O	VDDIO_18	LVDS data
509	U39	LVDS_L1_CLKN	MEDIA	O	VDDIO_18	LVDS clock
510	U38	LVDS_L1_CLKP	MEDIA	O	VDDIO_18	LVDS clock
511	Y37	LVDS_L1_DATN[0]	MEDIA	O	VDDIO_18	LVDS data
512	W39	LVDS_L1_DATN[1]	MEDIA	O	VDDIO_18	LVDS data
513	V37	LVDS_L1_DATN[2]	MEDIA	O	VDDIO_18	LVDS data
514	T38	LVDS_L1_DATN[3]	MEDIA	O	VDDIO_18	LVDS data
515	R38	LVDS_L1_DATN[4]	MEDIA	O	VDDIO_18	LVDS data
516	Y38	LVDS_L1_DATP[0]	MEDIA	O	VDDIO_18	LVDS data
517	W38	LVDS_L1_DATP[1]	MEDIA	O	VDDIO_18	LVDS data
518	V38	LVDS_L1_DATP[2]	MEDIA	O	VDDIO_18	LVDS data
519	T37	LVDS_L1_DATP[3]	MEDIA	O	VDDIO_18	LVDS data
520	R39	LVDS_L1_DATP[4]	MEDIA	O	VDDIO_18	LVDS data
521	AC36	LVDS_L2_CLKN	MEDIA	O	VDDIO_18	LVDS clock
522	AC35	LVDS_L2_CLKP	MEDIA	O	VDDIO_18	LVDS clock
523	AF35	LVDS_L2_DATN[0]	MEDIA	O	VDDIO_18	LVDS data
524	AE35	LVDS_L2_DATN[1]	MEDIA	O	VDDIO_18	LVDS data
525	AD35	LVDS_L2_DATN[2]	MEDIA	O	VDDIO_18	LVDS data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
526	AB34	LVDS_L2_DATN[3]	MEDIA	O	VDDIO_18	LVDS data
527	AA35	LVDS_L2_DATN[4]	MEDIA	O	VDDIO_18	LVDS data
528	AF34	LVDS_L2_DATP[0]	MEDIA	O	VDDIO_18	LVDS data
529	AE36	LVDS_L2_DATP[1]	MEDIA	O	VDDIO_18	LVDS data
530	AD34	LVDS_L2_DATP[2]	MEDIA	O	VDDIO_18	LVDS data
531	AB35	LVDS_L2_DATP[3]	MEDIA	O	VDDIO_18	LVDS data
532	AA36	LVDS_L2_DATP[4]	MEDIA	O	VDDIO_18	LVDS data
533	U36	LVDS_L3_CLKN	MEDIA	O	VDDIO_18	LVDS clock
534	U35	LVDS_L3_CLKP	MEDIA	O	VDDIO_18	LVDS clock
535	Y34	LVDS_L3_DATN[0]	MEDIA	O	VDDIO_18	LVDS data
536	W35	LVDS_L3_DATN[1]	MEDIA	O	VDDIO_18	LVDS data
537	V34	LVDS_L3_DATN[2]	MEDIA	O	VDDIO_18	LVDS data
538	T34	LVDS_L3_DATN[3]	MEDIA	O	VDDIO_18	LVDS data
539	R35	LVDS_L3_DATN[4]	MEDIA	O	VDDIO_18	LVDS data
540	Y35	LVDS_L3_DATP[0]	MEDIA	O	VDDIO_18	LVDS data
541	W36	LVDS_L3_DATP[1]	MEDIA	O	VDDIO_18	LVDS data
542	V35	LVDS_L3_DATP[2]	MEDIA	O	VDDIO_18	LVDS data
543	T35	LVDS_L3_DATP[3]	MEDIA	O	VDDIO_18	LVDS data
544	R36	LVDS_L3_DATP[4]	MEDIA	O	VDDIO_18	LVDS data
545	AF24	LVDS_PLL_27M	MEDIA	I	VDDIO_18	PLL Reference Clock 27MHz IN - LVDS
546	AD33	LVDS_VREF	MEDIA	A		Signal reference
547	AT16	PCIE4_0_AMON	PCIe	O	VDD_PCIE4_0_15	Analog monitor bump
548	AU15	PCIE4_0_ATT_BUT	PCIe	I	VDDIO_18	Attention button pressed
549	AR11	PCIE4_0_ATT_IND[0]	PCIe	O	VDDIO_18	Controls the system attention indicator
550	AM16	PCIE4_0_ATT_IND[1]	PCIe	O	VDDIO_18	Controls the system attention indicator
551	AR16	PCIE4_0_CMD_INT	PCIe	I	VDDIO_18	Hot-plug controller command completed interrupt
552	AL15	PCIE4_0_DMON	PCIe	O	VDD_PCIE4_0_09	Differential digital monitor bump
553	AM15	PCIE4_0_DMONB	PCIe	O	VDD_PCIE4_0_09	Differential digital monitor bump
554	AT18	PCIE4_0_INTRL_CTRL	PCIe	O	VDDIO_18	Electromechanical Interlock Control
555	AT17	PCIE4_0_INTRL_ENG	PCIe	I	VDDIO_18	SystemElectromechanical Interlock Engaged
556	AP17	PCIE4_0_MRL_SENS	PCIe	I	VDDIO_18	MRL sensor state

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
557	AU16	PCIE4_0_PRES_ST	PCIe	I	VDDIO_18	Presence detect state
558	AP16	PCIE4_0_PWR_CTRL	PCIe	O	VDDIO_18	Controls the system power controller
559	AR9	PCIE4_0_PWR_FAULT	PCIe	I	VDDIO_18	Power fault detect
560	AP10	PCIE4_0_PWR_IND[0]	PCIe	O	VDDIO_18	Controls the system power indicator
561	AP11	PCIE4_0_PWR_IND[1]	PCIe	O	VDDIO_18	Controls the system power indicator
562	AV17	PCIE4_0_RBIAS	PCIe	IO	VDD_PCIE4_0_15	Bias resistor bump
563	AW15	PCIE4_0_REF_CLKN	PCIe	I	VDD_PCIE4_0_15	Differential reference clocks from pads
564	AW16	PCIE4_0_REF_CLKP	PCIe	I	VDD_PCIE4_0_15	Differential reference clocks from pads
565	AV14	PCIE4_0_RXN[0]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
566	AW12	PCIE4_0_RXN[1]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
567	AV10	PCIE4_0_RXN[2]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
568	AW9	PCIE4_0_RXN[3]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
569	AV13	PCIE4_0_RXP[0]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
570	AW13	PCIE4_0_RXP[1]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
571	AV11	PCIE4_0_RXP[2]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
572	AW10	PCIE4_0_RXP[3]	PCIe	I	VDD_PCIE4_0_15	Receive data diff pair
573	AT14	PCIE4_0_TXN[0]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
574	AU13	PCIE4_0_TXN[1]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
575	AT11	PCIE4_0_TXN[2]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
576	AU10	PCIE4_0_TXN[3]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
577	AT13	PCIE4_0_TXP[0]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
578	AU12	PCIE4_0_TXP[1]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
579	AT10	PCIE4_0_TXP[2]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
580	AU9	PCIE4_0_TXP[3]	PCIe	O	VDD_PCIE4_0_15	Transmit data diff pair
581	AP13	PCIE4_1_AMON	PCIe	O	VDD_PCIE4_1_15	Analog monitor bump
582	AR7	PCIE4_1_ATT_BUT	PCIe	I	VDDIO_18	Attention button pressed
583	AM12	PCIE4_1_ATT_IND[0]	PCIe	O	VDDIO_18	Controls the system attention indicator
584	AN13	PCIE4_1_ATT_IND[1]	PCIe	O	VDDIO_18	Controls the system attention indicator
585	AJ13	PCIE4_1_CMD_INT	PCIe	I	VDDIO_18	Hot-plug controller command completed interrupt
586	AR12	PCIE4_1_DMON	PCIe	O	VDD_PCIE4_1_09	Differential digital monitor bump

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
587	AP12	PCIE4_1_DMONB	PCIe	O	VDD_PCIE4_1_09	Differential digital monitor bump
588	AP9	PCIE4_1_INTRL_CTRL	PCIe	O	VDDIO_18	Electromechanical Interlock Control
589	AU8	PCIE4_1_INTRL_ENG	PCIe	I	VDDIO_18	SystemElectromechanical Interlock Engaged
590	AK14	PCIE4_1_MRL_SENS	PCIe	I	VDDIO_18	MRL sensor state
591	AT8	PCIE4_1_PRES_ST	PCIe	I	VDDIO_18	Presence detect state
592	AL11	PCIE4_1_PWR_CTRL	PCIe	O	VDDIO_18	Controls the system power controller
593	AK13	PCIE4_1_PWR_FAULT	PCIe	I	VDDIO_18	Power fault detect
594	AL12	PCIE4_1_PWR_IND[0]	PCIe	O	VDDIO_18	Controls the system power indicator
595	AM13	PCIE4_1_PWR_IND[1]	PCIe	O	VDDIO_18	Controls the system power indicator
596	AV8	PCIE4_1_RBIAS	PCIe	IO	VDD_PCIE4_1_15	Bias resistor bump
597	AV7	PCIE4_1_REF_CLKN	PCIe	I	VDD_PCIE4_1_15	Differential reference clocks from pads
598	AW7	PCIE4_1_REF_CLKP	PCIe	I	VDD_PCIE4_1_15	Differential reference clocks from pads
599	AV6	PCIE4_1_RXN[0]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
600	AW5	PCIE4_1_RXN[1]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
601	AV3	PCIE4_1_RXN[2]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
602	AW2	PCIE4_1_RXN[3]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
603	AV5	PCIE4_1_RXP[0]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
604	AW4	PCIE4_1_RXP[1]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
605	AV2	PCIE4_1_RXP[2]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
606	AW1	PCIE4_1_RXP[3]	PCIe	I	VDD_PCIE4_1_15	Receive data diff pair
607	AT6	PCIE4_1_TXN[0]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
608	AU5	PCIE4_1_TXN[1]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
609	AT3	PCIE4_1_TXN[2]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
610	AU2	PCIE4_1_TXN[3]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
611	AT5	PCIE4_1_TXP[0]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
612	AU4	PCIE4_1_TXP[1]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
613	AT2	PCIE4_1_TXP[2]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
614	AU1	PCIE4_1_TXP[3]	PCIe	O	VDD_PCIE4_1_15	Transmit data diff pair
615	AK6	PCIE8_AMON0	PCIe	O	VDD_PCIE8_15	Analog monitor bump
616	AJ8	PCIE8_AMON1	PCIe	O	VDD_PCIE8_15	Analog monitor bump
617	AM9	PCIE8_ATT_BUT	PCIe	I	VDDIO_18	Attention button pressed

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
618	AN7	PCIE8_ATT_IND[0]	PCIe	O	VDDIO_18	Controls the system attention indicator
619	AN8	PCIE8_ATT_IND[1]	PCIe	O	VDDIO_18	Controls the system attention indicator
620	AJ5	PCIE8_CMD_INT	PCIe	I	VDDIO_18	Hot-plug controller command completed interrupt
621	AL8	PCIE8_DMON0	PCIe	O	VDD_PCIE8_09	Differential digital monitor bump
622	AK9	PCIE8_DMON1	PCIe	O	VDD_PCIE8_09	Differential digital monitor bump
623	AL9	PCIE8_DMONB0	PCIe	O	VDD_PCIE8_09	Differential digital monitor bump
624	AK8	PCIE8_DMONB1	PCIe	O	VDD_PCIE8_09	Differential digital monitor bump
625	AM8	PCIE8_INTRL_CTRL	PCIe	O	VDDIO_18	Electromechanical Interlock Control
626	AM7	PCIE8_INTRL_ENG	PCIe	I	VDDIO_18	SystemElectromechanical Interlock Engaged
627	AH9	PCIE8_MRL_SENS	PCIe	I	VDDIO_18	MRL sensor state
628	AL10	PCIE8_PRES_ST	PCIe	I	VDDIO_18	Presence detect state
629	AJ6	PCIE8_PWR_CTRL	PCIe	O	VDDIO_18	Controls the system power controller
630	AJ7	PCIE8_PWR_FAULT	PCIe	I	VDDIO_18	Power fault detect
631	AH7	PCIE8_PWR_IND[0]	PCIe	O	VDDIO_18	Controls the system power indicator
632	AH8	PCIE8_PWR_IND[1]	PCIe	O	VDDIO_18	Controls the system power indicator
633	AN5	PCIE8_RBIAS0	PCIe	IO	VDD_PCIE8_15	Bias resistor bump
634	AP6	PCIE8_RBIAS1	PCIe	IO	VDD_PCIE8_15	Bias resistor bump
635	AL5	PCIE8_REF_CLKN	PCIe	I	VDD_PCIE8_15	Differential reference clocks from pads
636	AL6	PCIE8_REF_CLKP	PCIe	I	VDD_PCIE8_15	Differential reference clocks from pads
637	AR1	PCIE8_RXN[0]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
638	AP2	PCIE8_RXN[1]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
639	AM1	PCIE8_RXN[2]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
640	AL2	PCIE8_RXN[3]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
641	AH1	PCIE8_RXN[4]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
642	AG2	PCIE8_RXN[5]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
643	AE1	PCIE8_RXN[6]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
644	AD2	PCIE8_RXN[7]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
645	AP1	PCIE8_RXP[0]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
646	AN2	PCIE8_RXP[1]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
647	AL1	PCIE8_RXP[2]	PCIe	I	VDD_PCIE8_15	Receive data diff pair

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
648	AK2	PCIE8_RXP[3]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
649	AJ1	PCIE8_RXP[4]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
650	AH2	PCIE8_RXP[5]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
651	AF1	PCIE8_RXP[6]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
652	AE2	PCIE8_RXP[7]	PCIe	I	VDD_PCIE8_15	Receive data diff pair
653	AR4	PCIE8_TXN[0]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
654	AP3	PCIE8_TXN[1]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
655	AM4	PCIE8_TXN[2]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
656	AL3	PCIE8_TXN[3]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
657	AH4	PCIE8_TXN[4]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
658	AG3	PCIE8_TXN[5]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
659	AE4	PCIE8_TXN[6]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
660	AD3	PCIE8_TXN[7]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
661	AP4	PCIE8_TXP[0]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
662	AN3	PCIE8_TXP[1]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
663	AL4	PCIE8_TXP[2]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
664	AK3	PCIE8_TXP[3]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
665	AJ4	PCIE8_TXP[4]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
666	AH3	PCIE8_TXP[5]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
667	AF4	PCIE8_TXP[6]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
668	AE3	PCIE8_TXP[7]	PCIe	O	VDD_PCIE8_15	Transmit data diff pair
669	AJ15	RESET_N	SYSTEM	I	VDDIO_18	System Reset, active low
670	D31	SATA_P0ACTLED	SATA	O	VDDIO_18	P0 Activity LED
671	E31	SATA_P0CPDET	SATA	I	VDDIO_18	Cold Presence Detect P0
672	E30	SATA_P0CPPOD	SATA	O	VDDIO_18	Cold Presence Power-On Device P0
673	F30	SATA_P0MPSW	SATA	I	VDDIO_18	Mechanical Presence Switch P0
674	F29	SATA_P1ACTLED	SATA	O	VDDIO_18	P1 Activity LED
675	G29	SATA_P1CPDET	SATA	I	VDDIO_18	Cold Presence Detect P1
676	F28	SATA_P1CPPOD	SATA	O	VDDIO_18	Cold Presence Power-On Device P1
677	G28	SATA_P1MPSW	SATA	I	VDDIO_18	Mechanical Presence Switch P1
678	A31	SATA_REFCLKM	SATA	I	VDD_SATA_09	Reference clk diff pair

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
679	B31	SATA_REFCLKP	SATA	I	VDD_SATA_09	Reference clk diff pair
680	D29	SATA_RESREF	SATA	A		Reference Resistor
681	C30	SATA_RXN[0]	SATA	I	VDD_SATA_09	Receive data diff pair port 0
682	B28	SATA_RXN[1]	SATA	I	VDD_SATA_09	Receive data diff pair port 1
683	B30	SATA_RXP[0]	SATA	I	VDD_SATA_09	Receive data diff pair port 0
684	C28	SATA_RXP[1]	SATA	I	VDD_SATA_09	Receive data diff pair port 1
685	B29	SATA_TXN[0]	SATA	O	VDD_SATATX_09	Transmit data diff pair port 0
686	A27	SATA_TXN[1]	SATA	O	VDD_SATATX_09	Transmit data diff pair port 1
687	A29	SATA_TXP[0]	SATA	O	VDD_SATATX_09	Transmit data diff pair port 0
688	B27	SATA_TXP[1]	SATA	O	VDD_SATATX_09	Transmit data diff pair port 1
689	L36	SD_CAP0	eMMC/SD	A		Connected to 1uF capacitor for stabilyzing LDO output voltage
690	M35	SD_CAP1	eMMC/SD	A		Connected to 1uF capacitor for stabilyzing LDO output voltage
691	K36	SD_CARD_DETECT_N	eMMC/SD	I	VDDIO_18	Card Detect, active low
692	N39	SD_CLK	eMMC/SD	O	VDD_SD_33	SD card transmit/receive clock
693	K34	SD_CMD	eMMC/SD	IO	VDD_SD_33	SD card Command
694	L38	SD_DAT[0]	eMMC/SD	IO	VDD_SD_33	SD card Data
695	L37	SD_DAT[1]	eMMC/SD	IO	VDD_SD_33	SD card Data
696	M39	SD_DAT[2]	eMMC/SD	IO	VDD_SD_33	SD card Data
697	M38	SD_DAT[3]	eMMC/SD	IO	VDD_SD_33	SD card Data
698	M37	SD_DAT[4]	eMMC/SD	IO	VDD_SD_33	SD card Data
699	N38	SD_DAT[5]	eMMC/SD	IO	VDD_SD_33	SD card Data
700	N37	SD_DAT[6]	eMMC/SD	IO	VDD_SD_33	SD card Data
701	N36	SD_DAT[7]	eMMC/SD	IO	VDD_SD_33	SD card Data
702	M34	SD_LED_CTRL	eMMC/SD	O	VDDIO_18	SD card LED control
703	N34	SD_REG_VOL_STABLE	eMMC/SD	I	VDDIO_18	Voltage regulator voltage stable
704	P36	SD_RST_N	eMMC/SD	O	VDD_SD_33	eMMC device reset, active low
705	L34	SD_VDD_ON	eMMC/SD	O	VDDIO_18	Voltage regulator VDD1 enable
706	M33	SD_VDD_SEL[0]	eMMC/SD	O	VDDIO_18	Voltage regulator VDD1 select
707	N33	SD_VDD_SEL[1]	eMMC/SD	O	VDDIO_18	Voltage regulator VDD1 select

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
708	P34	SD_VDD_SEL[2]	eMMC/SD	O	VDDIO_18	Voltage regulator VDD1 select
709	K35	SD_WRITE_PROT	eMMC/SD	I	VDDIO_18	Card Write Protect, active high
710	AV18	SMB0_CLK	SM	IO	VDDIO_18	SM SMBus clock
711	AW18	SMB0_DAT	SM	IO	VDDIO_18	SM SMBus data
712	G39	SMB1_CLK	LSP	IO	VDDIO_18	LSP SMBus1 clock
713	H39	SMB1_DAT	LSP	IO	VDDIO_18	LSP SMBus1 data
714	G38	SMB2_CLK	LSP	IO	VDDIO_18	LSP SMBus2 clock
715	H38	SMB2_DAT	LSP	IO	VDDIO_18	LSP SMBus2 data
716	AW19	SPI0_CLK	SM	O	VDDIO_18	Output Clock
717	AT19	SPI0_RXD	SM	I	VDDIO_18	Receive data
718	AR19	SPI0_SS_N[0]	SM	O	VDDIO_18	Slave Select
719	AP19	SPI0_SS_N[1]	SM	O	VDDIO_18	Slave Select
720	AN20	SPI0_SS_N[2]	SM	O	VDDIO_18	Slave Select
721	AM20	SPI0_SS_N[3]	SM	O	VDDIO_18	Slave Select
722	AU19	SPI0_TXD	SM	O	VDDIO_18	Transmit data
723	F39	SPI1_CLK	LSP	O	VDDIO_18	Output Clock
724	E38	SPI1_RXD	LSP	I	VDDIO_18	Receive data
725	E37	SPI1_SS_N[0]	LSP	O	VDDIO_18	Slave Select
726	F37	SPI1_SS_N[1]	LSP	O	VDDIO_18	Slave Select
727	F36	SPI1_SS_N[2]	LSP	O	VDDIO_18	Slave Select
728	F35	SPI1_SS_N[3]	LSP	O	VDDIO_18	Slave Select
729	E39	SPI1_TXD	LSP	O	VDDIO_18	Transmit data
730	AM19	TEST_0	SM	I	VDDIO_18	Test point 0
731	AL18	TEST_1	SM	I	VDDIO_18	Test point 1
732	AH13	TRSTN	SYSTEM	I	VDDIO_18	Test reset
733	AK18	UART0_RXD	SM	I	VDDIO_18	Receive data
734	AK19	UART0_TXD	SM	O	VDDIO_18	Transmit data
735	J38	UART1_RXD	LSP	I	VDDIO_18	Receive data
736	J39	UART1_TXD	LSP	O	VDDIO_18	Transmit data
737	K38	UART2_RXD	LSP	I	VDDIO_18	Receive data
738	K39	UART2_TXD	LSP	O	VDDIO_18	Transmit data
739	K27	USB2_0_CTRL	USB	O	VDDIO_18	Port Power Control

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
740	D19	USB2_0_DM0	USB	IO	VDD_USB2_0_33	USB D- Signal
741	E19	USB2_0_DP0	USB	IO	VDD_USB2_0_33	USB D+ Signal
742	P24	USB2_0_ID0	USB	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
743	P23	USB2_0_OVCUR	USB	I	VDDIO_18	Port Overcurrent
744	N23	USB2_0_RT	USB	IO	VDD_USB2_18	Trasmitter Resistor Tune Pin
745	M23	USB2_0_VBUS0	USB	A		USB 5 V Signal
746	F20	USB2_0_XI	USB	I	VDD_USB2_18	Crystal Oscillator XI Pin
747	G20	USB2_0_XO	USB	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
748	K28	USB2_1_CTRL	USB	O	VDDIO_18	Port Power Control
749	E22	USB2_1_DM0	USB	IO	VDD_USB2_1_33	USB D- Signal
750	F22	USB2_1_DP0	USB	IO	VDD_USB2_1_33	USB D+ Signal
751	N27	USB2_1_ID0	USB	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
752	N24	USB2_1_OVCUR	USB	I	VDDIO_18	Port Overcurrent
753	N25	USB2_1_RT	USB	IO	VDD_USB2_18	Trasmitter Resistor Tune Pin
754	M25	USB2_1_VBUS0	USB	A		USB 5 V Signal
755	F21	USB2_1_XI	USB	I	VDD_USB2_18	Crystal Oscillator XI Pin
756	G21	USB2_1_XO	USB	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
757	H28	USB2_2_CTRL	USB	O	VDDIO_18	Port Power Control
758	D23	USB2_2_DM0	USB	IO	VDD_USB2_2_33	USB D- Signal
759	E23	USB2_2_DP0	USB	IO	VDD_USB2_2_33	USB D+ Signal
760	N26	USB2_2_ID0	USB	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
761	M26	USB2_2_OVCUR	USB	I	VDDIO_18	Port Overcurrent
762	H26	USB2_2_RT	USB	IO	VDD_USB2_18	Trasmitter Resistor Tune Pin
763	G26	USB2_2_VBUS0	USB	A		USB 5 V Signal
764	F24	USB2_2_XI	USB	I	VDD_USB2_18	Crystal Oscillator XI Pin
765	G24	USB2_2_XO	USB	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
766	H29	USB2_3_CTRL	USB	O	VDDIO_18	Port Power Control
767	D26	USB2_3_DM0	USB	IO	VDD_USB2_3_33	USB D- Signal
768	E26	USB2_3_DP0	USB	IO	VDD_USB2_3_33	USB D+ Signal

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
769	G27	USB2_3_ID0	USB	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
770	E28	USB2_3_OVCUR	USB	I	VDDIO_18	Port Overcurrent
771	F27	USB2_3_RT	USB	IO		Trasmitter Resistor Tune Pin
772	E27	USB2_3_VBUS0	USB	A		USB 5 V Signal
773	F25	USB2_3_XI	USB	I	VDD_USB2_18	Crystal Oscillator XI Pin
774	G25	USB2_3_XO	USB	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
775	K25	USB2_4_CTRL	USB	O	VDDIO_18	Port Power Control - USB2 part
776	L24	USB2_4_OVCUR	USB	I	VDDIO_18	Port Overcurrent - USB2 part
777	J20	USB2_5_CTRL	USB	O	VDDIO_18	Port Power Control - USB2 part
778	L19	USB2_5_OVCUR	USB	I	VDDIO_18	Port Overcurrent - USB2 part
779	J24	USB3_0_CTRL	USB	O	VDDIO_18	Port Power Control - USB3 part
780	C26	USB3_0_DM0	USB	IO	VDD_USB3_33	USB2 D- Signal
781	B26	USB3_0_DP0	USB	IO	VDD_USB3_33	USB2 D+ Signal
782	L23	USB3_0_ID0	USB	IO		USB2 Mini-Receptacle Identifier
783	K24	USB3_0_OVCUR	USB	I	VDDIO_18	Port Overcurrent - USB3 part
784	B25	USB3_0_REFCLKN	USB	I	VDD_USB3VP_0_09	USB3 Optional Reference Clock Input
785	A25	USB3_0_REFCLKP	USB	I	VDD_USB3VP_0_09	USB3 Optional Reference Clock Input
786	J23	USB3_0_RESREF	USB	A		USB3 External Reference Resistor
787	A23	USB3_0_RXON	USB	I	VDD_USB3VP_0_09	USB3 Receive Pin
788	B23	USB3_0_RXOP	USB	I	VDD_USB3VP_0_09	USB3 Receive Pin
789	B24	USB3_0_TXON	USB	O	VDD_USB3TX_0_09	USB3 Transmit Pin
790	C24	USB3_0_TXOP	USB	O	VDD_USB3TX_0_09	USB3 Transmit Pin
791	D24	USB3_0_VBUS0	USB	A		USB 5 V Power Supply Pin
792	J19	USB3_1_CTRL	USB	O	VDDIO_18	Port Power Control - USB3 part
793	C22	USB3_1_DM0	USB	IO	VDD_USB3_33	USB2 D- Signal
794	B22	USB3_1_DP0	USB	IO	VDD_USB3_33	USB2 D+ Signal
795	H19	USB3_1_ID0	USB	IO		USB2 Mini-Receptacle Identifier
796	K19	USB3_1_OVCUR	USB	I	VDDIO_18	Port Overcurrent - USB3 part
797	B21	USB3_1_REFCLKN	USB	I	VDD_USB3VP_1_09	USB3 Optional Reference Clock Input

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
798	A21	USB3_1_REFCLKP	USB	I	VDD_USB3VP_1_09	USB3 Optional Reference Clock Input
799	H20	USB3_1_RESREF	USB	A		USB3 External Reference Resistor
800	A19	USB3_1_RXON	USB	I	VDD_USB3VP_1_09	USB3 Receive Pin
801	B19	USB3_1_RXOP	USB	I	VDD_USB3VP_1_09	USB3 Receive Pin
802	B20	USB3_1_TXON	USB	O	VDD_USB3TX_1_09	USB3 Transmit Pin
803	C20	USB3_1_TXOP	USB	O	VDD_USB3TX_1_09	USB3 Transmit Pin
804	D20	USB3_1_VBUS0	USB	A		USB 5 V Power Supply Pin
805	H14	XG0_AMON	XGBE	O	VDD_XG0_15	Analog monitor bump
806	G13	XG0_DMON	XGBE	O	VDD_XG0_09	Differential digital monitor bump
807	H13	XG0_DMONB	XGBE	O	VDD_XG0_09	Differential digital monitor bump
808	H15	XG0_RBIAS	XGBE	IO	VDD_XG0_15	Bias resistor bump
809	H12	XG0_REF_CLKN	XGBE	I	VDD_XG0_15	Differential reference clocks from pads
810	G12	XG0_REF_CLKP	XGBE	I	VDD_XG0_15	Differential reference clocks from pads
811	A11	XG0_RXN[0]	XGBE	I	VDD_XG0_15	Receive data diff pair
812	B12	XG0_RXN[1]	XGBE	I	VDD_XG0_15	Receive data diff pair
813	A13	XG0_RXN[2]	XGBE	I	VDD_XG0_15	Receive data diff pair
814	B14	XG0_RXN[3]	XGBE	I	VDD_XG0_15	Receive data diff pair
815	B11	XG0_RXP[0]	XGBE	I	VDD_XG0_15	Receive data diff pair
816	C12	XG0_RXP[1]	XGBE	I	VDD_XG0_15	Receive data diff pair
817	B13	XG0_RXP[2]	XGBE	I	VDD_XG0_15	Receive data diff pair
818	C14	XG0_RXP[3]	XGBE	I	VDD_XG0_15	Receive data diff pair
819	D11	XG0_TXN[0]	XGBE	O	VDD_XG0_15	Transmit data diff pair
820	E12	XG0_TXN[1]	XGBE	O	VDD_XG0_15	Transmit data diff pair
821	D13	XG0_TXN[2]	XGBE	O	VDD_XG0_15	Transmit data diff pair
822	E14	XG0_TXN[3]	XGBE	O	VDD_XG0_15	Transmit data diff pair
823	E11	XG0_TXP[0]	XGBE	O	VDD_XG0_15	Transmit data diff pair
824	F12	XG0_TXP[1]	XGBE	O	VDD_XG0_15	Transmit data diff pair
825	E13	XG0_TXP[2]	XGBE	O	VDD_XG0_15	Transmit data diff pair
826	F14	XG0_TXP[3]	XGBE	O	VDD_XG0_15	Transmit data diff pair
827	H18	XG1_AMON	XGBE	O	VDD_XG1_15	Analog monitor bump
828	G17	XG1_DMON	XGBE	O	VDD_XG1_09	Differential digital monitor bump

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
829	H17	XG1_DMONB	XGBE	O	VDD_XG1_09	Differential digital monitor bump
830	G15	XG1_RBIAS	XGBE	IO	VDD_XG1_15	Bias resistor bump
831	J16	XG1_REF_CLKN	XGBE	I	VDD_XG1_15	Differential reference clocks from pads
832	H16	XG1_REF_CLKP	XGBE	I	VDD_XG1_15	Differential reference clocks from pads
833	B18	XG1_RXN[0]	XGBE	I	VDD_XG1_15	Receive data diff pair
834	A17	XG1_RXN[1]	XGBE	I	VDD_XG1_15	Receive data diff pair
835	B16	XG1_RXN[2]	XGBE	I	VDD_XG1_15	Receive data diff pair
836	A15	XG1_RXN[3]	XGBE	I	VDD_XG1_15	Receive data diff pair
837	C18	XG1_RXP[0]	XGBE	I	VDD_XG1_15	Receive data diff pair
838	B17	XG1_RXP[1]	XGBE	I	VDD_XG1_15	Receive data diff pair
839	C16	XG1_RXP[2]	XGBE	I	VDD_XG1_15	Receive data diff pair
840	B15	XG1_RXP[3]	XGBE	I	VDD_XG1_15	Receive data diff pair
841	E18	XG1_TXN[0]	XGBE	O	VDD_XG1_15	Transmit data diff pair
842	D17	XG1_TXN[1]	XGBE	O	VDD_XG1_15	Transmit data diff pair
843	E16	XG1_TXN[2]	XGBE	O	VDD_XG1_15	Transmit data diff pair
844	D15	XG1_TXN[3]	XGBE	O	VDD_XG1_15	Transmit data diff pair
845	F18	XG1_TXP[0]	XGBE	O	VDD_XG1_15	Transmit data diff pair
846	E17	XG1_TXP[1]	XGBE	O	VDD_XG1_15	Transmit data diff pair
847	F16	XG1_TXP[2]	XGBE	O	VDD_XG1_15	Transmit data diff pair
848	E15	XG1_TXP[3]	XGBE	O	VDD_XG1_15	Transmit data diff pair
849	AB16	VDD	POWER	P		Core power
850	AB17	VDD	POWER	P		Core power
851	AB18	VDD	POWER	P		Core power
852	AB19	VDD	POWER	P		Core power
853	AB20	VDD	POWER	P		Core power
854	AB21	VDD	POWER	P		Core power
855	AB22	VDD	POWER	P		Core power
856	AB23	VDD	POWER	P		Core power
857	AB24	VDD	POWER	P		Core power
858	AB25	VDD	POWER	P		Core power
859	AB26	VDD	POWER	P		Core power
860	AB27	VDD	POWER	P		Core power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
861	AB28	VDD	POWER	P		Core power
862	AB29	VDD	POWER	P		Core power
863	AD14	VDD	POWER	P		Core power
864	AD15	VDD	POWER	P		Core power
865	AD16	VDD	POWER	P		Core power
866	AD17	VDD	POWER	P		Core power
867	AD18	VDD	POWER	P		Core power
868	AD19	VDD	POWER	P		Core power
869	AD20	VDD	POWER	P		Core power
870	AD21	VDD	POWER	P		Core power
871	AD22	VDD	POWER	P		Core power
872	AD23	VDD	POWER	P		Core power
873	AD24	VDD	POWER	P		Core power
874	AD25	VDD	POWER	P		Core power
875	AD26	VDD	POWER	P		Core power
876	AD27	VDD	POWER	P		Core power
877	AD28	VDD	POWER	P		Core power
878	AD29	VDD	POWER	P		Core power
879	AD30	VDD	POWER	P		Core power
880	AD31	VDD	POWER	P		Core power
881	AD32	VDD	POWER	P		Core power
882	AF26	VDD	POWER	P		Core power
883	AF27	VDD	POWER	P		Core power
884	AF30	VDD	POWER	P		Core power
885	AG28	VDD	POWER	P		Core power
886	T15	VDD	POWER	P		Core power
887	T16	VDD	POWER	P		Core power
888	T17	VDD	POWER	P		Core power
889	T18	VDD	POWER	P		Core power
890	T19	VDD	POWER	P		Core power
891	T20	VDD	POWER	P		Core power
892	T21	VDD	POWER	P		Core power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
893	T22	VDD	POWER	P		Core power
894	T23	VDD	POWER	P		Core power
895	T24	VDD	POWER	P		Core power
896	T25	VDD	POWER	P		Core power
897	T26	VDD	POWER	P		Core power
898	T27	VDD	POWER	P		Core power
899	T28	VDD	POWER	P		Core power
900	T29	VDD	POWER	P		Core power
901	T30	VDD	POWER	P		Core power
902	V15	VDD	POWER	P		Core power
903	V16	VDD	POWER	P		Core power
904	V17	VDD	POWER	P		Core power
905	V18	VDD	POWER	P		Core power
906	V19	VDD	POWER	P		Core power
907	V20	VDD	POWER	P		Core power
908	V21	VDD	POWER	P		Core power
909	V22	VDD	POWER	P		Core power
910	V23	VDD	POWER	P		Core power
911	V24	VDD	POWER	P		Core power
912	V25	VDD	POWER	P		Core power
913	V26	VDD	POWER	P		Core power
914	V27	VDD	POWER	P		Core power
915	V28	VDD	POWER	P		Core power
916	Y16	VDD	POWER	P		Core power
917	Y17	VDD	POWER	P		Core power
918	Y18	VDD	POWER	P		Core power
919	Y19	VDD	POWER	P		Core power
920	Y20	VDD	POWER	P		Core power
921	Y21	VDD	POWER	P		Core power
922	Y22	VDD	POWER	P		Core power
923	Y23	VDD	POWER	P		Core power
924	Y24	VDD	POWER	P		Core power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
925	Y25	VDD	POWER	P		Core power
926	Y26	VDD	POWER	P		Core power
927	Y27	VDD	POWER	P		Core power
928	Y28	VDD	POWER	P		Core power
929	Y29	VDD	POWER	P		Core power
930	AF21	VDD_18	POWER	P		SM power supply
931	AB14	VDD_DDR0_PLL	POWER	P		PLL power supply
932	AB15	VDD_DDR0_PLL	POWER	P		PLL power supply
933	AD13	VDD_DDR0_PLL	POWER	P		PLL power supply
934	V14	VDD_DDR0_PLL	POWER	P		PLL power supply
935	Y14	VDD_DDR0_PLL	POWER	P		PLL power supply
936	Y15	VDD_DDR0_PLL	POWER	P		PLL power supply
937	AG29	VDD_DDR1_PLL	POWER	P		PLL power supply
938	AG30	VDD_DDR1_PLL	POWER	P		PLL power supply
939	AH28	VDD_DDR1_PLL	POWER	P		PLL power supply
940	AH29	VDD_DDR1_PLL	POWER	P		PLL power supply
941	AH30	VDD_DDR1_PLL	POWER	P		PLL power supply
942	AJ29	VDD_DDR1_PLL	POWER	P		PLL power supply
943	F9	VDD_HDMI_09	POWER	P		0.9 V analog power supply
944	F10	VDD_HDMI_18	POWER	P		1.8V analog power supply
945	AN14	VDD_PCIE4_0_09	POWER	P		PCIe PHY analog 0.95V
946	AP14	VDD_PCIE4_0_09	POWER	P		PCIe PHY analog 0.95V
947	AR15	VDD_PCIE4_0_09	POWER	P		PCIe PHY analog 0.95V
948	AR8	VDD_PCIE4_0_15	POWER	P		PCIe PHY IO 1.5V
949	AM10	VDD_PCIE4_1_09	POWER	P		PCIe PHY analog 0.95V
950	AN10	VDD_PCIE4_1_09	POWER	P		PCIe PHY analog 0.95V
951	AN11	VDD_PCIE4_1_09	POWER	P		PCIe PHY analog 0.95V
952	AP8	VDD_PCIE4_1_15	POWER	P		PCIe PHY IO 1.5V
953	AF5	VDD_PCIE8_09	POWER	P		PCIe PHY analog 0.95V
954	AH5	VDD_PCIE8_09	POWER	P		PCIe PHY analog 0.95V
955	AM6	VDD_PCIE8_09	POWER	P		PCIe PHY analog 0.95V
956	AP5	VDD_PCIE8_09	POWER	P		PCIe PHY analog 0.95V

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
957	AP7	VDD_PCIE8_09	POWER	P		PCIe PHY analog 0.95V
958	AR6	VDD_PCIE8_09	POWER	P		PCIe PHY analog 0.95V
959	AJ10	VDD_PCIE8_15	POWER	P		PCIe PHY IO 1.5V
960	AJ11	VDD_PCIE8_15	POWER	P		PCIe PHY IO 1.5V
961	M27	VDD_PVT_18	POWER	P		PVT sensor power
962	J26	VDD_SATA_09	POWER	P		SATA PHY analog and digital supply
963	K26	VDD_SATA_18	POWER	P		SATA PHY High-voltage power supply
964	J27	VDD_SATATX_09	POWER	P		SATA PHY transmit supply
965	P37	VDD_SD_33	POWER	P		3.3V SD Supply
966	P38	VDD_SD_33	POWER	P		3.3V SD Supply
967	F19	VDD_USB2_0_33	POWER	P		3.3V Analog Power Supply
968	J21	VDD_USB2_09	POWER	P		Digital Power Supply
969	K21	VDD_USB2_09	POWER	P		Digital Power Supply
970	G19	VDD_USB2_1_33	POWER	P		3.3V Analog Power Supply
971	G23	VDD_USB2_18	POWER	P		1.8V Analog Power Supply
972	H23	VDD_USB2_18	POWER	P		1.8V Analog Power Supply
973	H24	VDD_USB2_2_33	POWER	P		3.3V Analog Power Supply
974	H25	VDD_USB2_3_33	POWER	P		3.3V Analog Power Supply
975	A20	VDD_USB3_0_09	POWER	P		0.9 V PHY analog and digital high-speed supply
976	A24	VDD_USB3_1_09	POWER	P		0.9 V PHY analog and digital high-speed supply
977	K20	VDD_USB3_33	POWER	P		3.3V High supply for HS operation & SS operation
978	K23	VDD_USB3_33	POWER	P		3.3V High supply for HS operation & SS operation
979	L18	VDD_USB3_33	POWER	P		3.3V High supply for HS operation & SS operation
980	M22	VDD_USB3_33	POWER	P		3.3V High supply for HS operation & SS operation
981	D25	VDD_USB3TX_0_09	POWER	P		0.9 V PHY transmit supply
982	C21	VDD_USB3TX_1_09	POWER	P		0.9 V PHY transmit supply

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
983	E25	VDD_USB3VP_0_09	POWER	P		0.9 V PHY analog and digital SuperSpeed supply
984	D21	VDD_USB3VP_1_09	POWER	P		0.9 V PHY analog and digital SuperSpeed supply
985	F11	VDD_XG0_09	POWER	P		XGbE PHY analog 0.95V
986	G11	VDD_XG0_09	POWER	P		XGbE PHY analog 0.95V
987	H11	VDD_XG0_09	POWER	P		XGbE PHY analog 0.95V
988	F13	VDD_XG0_15	POWER	P		XGbE PHY IO 1.5V
989	K16	VDD_XG1_09	POWER	P		XGbE PHY analog 0.95V
990	K17	VDD_XG1_09	POWER	P		XGbE PHY analog 0.95V
991	L16	VDD_XG1_09	POWER	P		XGbE PHY analog 0.95V
992	J17	VDD_XG1_15	POWER	P		XGbE PHY IO 1.5V
993	AB30	VDDIO_18	POWER	P		IO power
994	AB31	VDDIO_18	POWER	P		IO power
995	AF14	VDDIO_18	POWER	P		IO power
996	AF15	VDDIO_18	POWER	P		IO power
997	AF16	VDDIO_18	POWER	P		IO power
998	AF17	VDDIO_18	POWER	P		IO power
999	AF18	VDDIO_18	POWER	P		IO power
1000	AF19	VDDIO_18	POWER	P		IO power
1001	J15	VDDIO_18	POWER	P		IO power
1002	K15	VDDIO_18	POWER	P		IO power
1003	V29	VDDIO_18	POWER	P		IO power
1004	V30	VDDIO_18	POWER	P		IO power
1005	V31	VDDIO_18	POWER	P		IO power
1006	V32	VDDIO_18	POWER	P		IO power
1007	Y30	VDDIO_18	POWER	P		IO power
1008	Y31	VDDIO_18	POWER	P		Output driver power, 1.8V
1009	Y32	VDDIO_18	POWER	P		IO power
1010	Y33	VDDIO_18	POWER	P		IO power
1011	P16	VDDPLL_0_09	POWER	P		PLL power
1012	W31	VDDPLL_1_09	POWER	P		PLL power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1013	AF32	VDDPLL_2_09	POWER	P		PLL power
1014	AN19	VDDPLL_3_09	POWER	P		PLL power
1015	J14	VDDPLL_HDMI_09	POWER	P		HDMI PLL power
1016	AA10	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1017	AC7	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1018	K11	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1019	K9	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1020	L12	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1021	L15	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1022	N14	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1023	N15	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1024	P9	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1025	R14	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1026	R15	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1027	R7	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1028	R9	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1029	T13	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1030	U13	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1031	U9	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1032	V10	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1033	V8	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1034	Y12	VDDQ_DDR0	POWER	P		VDDQ voltage supply
1035	AG34	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1036	AG36	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1037	AH31	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1038	AH33	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1039	AJ30	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1040	AJ32	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1041	AK21	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1042	AL29	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1043	AL33	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1044	AM21	VDDQ_DDR1	POWER	P		VDDQ voltage supply

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1045	AM32	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1046	AN21	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1047	AN30	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1048	AP33	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1049	AR28	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1050	AT34	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1051	AT36	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1052	AT38	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1053	AU31	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1054	AW31	VDDQ_DDR1	POWER	P		VDDQ voltage supply
1055	A10	VSS	POWER	G		eMMC/SD ground
1056	A12	VSS	POWER	G		eMMC/SD ground
1057	A14	VSS	POWER	G		DDR 0 ground
1058	A16	VSS	POWER	G		DDR 1 ground
1059	A18	VSS	POWER	G		HDMI ground
1060	A22	VSS	POWER	G		Core ground
1061	A26	VSS	POWER	G		Core ground
1062	A28	VSS	POWER	G		Core ground
1063	A30	VSS	POWER	G		Core ground
1064	A8	VSS	POWER	G		Core ground
1065	AA12	VSS	POWER	G		Core ground
1066	AA14	VSS	POWER	G		Core ground
1067	AA15	VSS	POWER	G		Core ground
1068	AA16	VSS	POWER	G		Core ground
1069	AA17	VSS	POWER	G		Core ground
1070	AA18	VSS	POWER	G		Core ground
1071	AA19	VSS	POWER	G		Core ground
1072	AA20	VSS	POWER	G		Core ground
1073	AA21	VSS	POWER	G		Core ground
1074	AA22	VSS	POWER	G		Core ground
1075	AA23	VSS	POWER	G		Core ground
1076	AA24	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1077	AA25	VSS	POWER	G		Core ground
1078	AA26	VSS	POWER	G		Core ground
1079	AA27	VSS	POWER	G		Core ground
1080	AA3	VSS	POWER	G		Core ground
1081	AA32	VSS	POWER	G		Core ground
1082	AA33	VSS	POWER	G		Core ground
1083	AA34	VSS	POWER	G		Core ground
1084	AA37	VSS	POWER	G		Core ground
1085	AA4	VSS	POWER	G		Core ground
1086	AA5	VSS	POWER	G		Core ground
1087	AA6	VSS	POWER	G		Core ground
1088	AA7	VSS	POWER	G		Core ground
1089	AB32	VSS	POWER	G		Core ground
1090	AB33	VSS	POWER	G		Core ground
1091	AB36	VSS	POWER	G		Core ground
1092	AB39	VSS	POWER	G		Core ground
1093	AC1	VSS	POWER	G		Core ground
1094	AC14	VSS	POWER	G		Core ground
1095	AC16	VSS	POWER	G		Core ground
1096	AC17	VSS	POWER	G		Core ground
1097	AC18	VSS	POWER	G		Core ground
1098	AC19	VSS	POWER	G		Core ground
1099	AC2	VSS	POWER	G		Core ground
1100	AC20	VSS	POWER	G		Core ground
1101	AC21	VSS	POWER	G		Core ground
1102	AC22	VSS	POWER	G		Core ground
1103	AC23	VSS	POWER	G		Core ground
1104	AC24	VSS	POWER	G		Core ground
1105	AC25	VSS	POWER	G		Core ground
1106	AC26	VSS	POWER	G		Core ground
1107	AC27	VSS	POWER	G		Core ground
1108	AC3	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1109	AC32	VSS	POWER	G		Core ground
1110	AC33	VSS	POWER	G		Core ground
1111	AC34	VSS	POWER	G		Core ground
1112	AC37	VSS	POWER	G		Core ground
1113	AD1	VSS	POWER	G		Core ground
1114	AD11	VSS	POWER	G		Core ground
1115	AD36	VSS	POWER	G		Core ground
1116	AD39	VSS	POWER	G		Core ground
1117	AD4	VSS	POWER	G		Core ground
1118	AD9	VSS	POWER	G		Core ground
1119	AE13	VSS	POWER	G		Core ground
1120	AE14	VSS	POWER	G		Core ground
1121	AE15	VSS	POWER	G		Core ground
1122	AE16	VSS	POWER	G		Core ground
1123	AE17	VSS	POWER	G		Core ground
1124	AE18	VSS	POWER	G		Core ground
1125	AE19	VSS	POWER	G		Core ground
1126	AE20	VSS	POWER	G		Core ground
1127	AE21	VSS	POWER	G		Core ground
1128	AE22	VSS	POWER	G		Core ground
1129	AE23	VSS	POWER	G		Core ground
1130	AE24	VSS	POWER	G		Core ground
1131	AE25	VSS	POWER	G		Core ground
1132	AE26	VSS	POWER	G		Core ground
1133	AE27	VSS	POWER	G		Core ground
1134	AE28	VSS	POWER	G		Core ground
1135	AE29	VSS	POWER	G		Core ground
1136	AE30	VSS	POWER	G		Core ground
1137	AE31	VSS	POWER	G		Core ground
1138	AE32	VSS	POWER	G		Core ground
1139	AE33	VSS	POWER	G		Core ground
1140	AE34	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1141	AE37	VSS	POWER	G		Core ground
1142	AE8	VSS	POWER	G		Core ground
1143	AF2	VSS	POWER	G		Core ground
1144	AF20	VSS	POWER	G		Core ground
1145	AF22	VSS	POWER	G		Core ground
1146	AF23	VSS	POWER	G		Core ground
1147	AF25	VSS	POWER	G		Core ground
1148	AF28	VSS	POWER	G		Core ground
1149	AF29	VSS	POWER	G		Core ground
1150	AF3	VSS	POWER	G		Core ground
1151	AF31	VSS	POWER	G		Core ground
1152	AF36	VSS	POWER	G		Core ground
1153	AF39	VSS	POWER	G		Core ground
1154	AG1	VSS	POWER	G		Core ground
1155	AG12	VSS	POWER	G		Core ground
1156	AG17	VSS	POWER	G		Core ground
1157	AG19	VSS	POWER	G		Core ground
1158	AG20	VSS	POWER	G		Core ground
1159	AG21	VSS	POWER	G		Core ground
1160	AG27	VSS	POWER	G		Core ground
1161	AG31	VSS	POWER	G		Core ground
1162	AG32	VSS	POWER	G		Core ground
1163	AG33	VSS	POWER	G		Core ground
1164	AG35	VSS	POWER	G		Core ground
1165	AG37	VSS	POWER	G		Core ground
1166	AG38	VSS	POWER	G		Core ground
1167	AG39	VSS	POWER	G		Core ground
1168	AG4	VSS	POWER	G		Core ground
1169	AG5	VSS	POWER	G		Core ground
1170	AH10	VSS	POWER	G		Core ground
1171	AH15	VSS	POWER	G		Core ground
1172	AH16	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1173	AH21	VSS	POWER	G		Core ground
1174	AH24	VSS	POWER	G		Core ground
1175	AH25	VSS	POWER	G		Core ground
1176	AH32	VSS	POWER	G		Core ground
1177	AH6	VSS	POWER	G		Core ground
1178	AJ14	VSS	POWER	G		Core ground
1179	AJ17	VSS	POWER	G		Core ground
1180	AJ2	VSS	POWER	G		Core ground
1181	AJ21	VSS	POWER	G		Core ground
1182	AJ23	VSS	POWER	G		Core ground
1183	AJ26	VSS	POWER	G		Core ground
1184	AJ27	VSS	POWER	G		Core ground
1185	AJ28	VSS	POWER	G		Core ground
1186	AJ3	VSS	POWER	G		Core ground
1187	AJ31	VSS	POWER	G		Core ground
1188	AJ33	VSS	POWER	G		Core ground
1189	AJ39	VSS	POWER	G		Core ground
1190	AJ9	VSS	POWER	G		Core ground
1191	AK1	VSS	POWER	G		Core ground
1192	AK10	VSS	POWER	G		Core ground
1193	AK11	VSS	POWER	G		Core ground
1194	AK12	VSS	POWER	G		Core ground
1195	AK15	VSS	POWER	G		Core ground
1196	AK16	VSS	POWER	G		Core ground
1197	AK20	VSS	POWER	G		Core ground
1198	AK23	VSS	POWER	G		Core ground
1199	AK32	VSS	POWER	G		Core ground
1200	AK33	VSS	POWER	G		Core ground
1201	AK36	VSS	POWER	G		Core ground
1202	AK4	VSS	POWER	G		Core ground
1203	AK5	VSS	POWER	G		Core ground
1204	AK7	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1205	AL13	VSS	POWER	G		Core ground
1206	AL14	VSS	POWER	G		Core ground
1207	AL16	VSS	POWER	G		Core ground
1208	AL17	VSS	POWER	G		Core ground
1209	AL21	VSS	POWER	G		Core ground
1210	AL24	VSS	POWER	G		Core ground
1211	AL26	VSS	POWER	G		Core ground
1212	AL28	VSS	POWER	G		Core ground
1213	AL30	VSS	POWER	G		Core ground
1214	AL7	VSS	POWER	G		Core ground
1215	AM11	VSS	POWER	G		Core ground
1216	AM14	VSS	POWER	G		Core ground
1217	AM2	VSS	POWER	G		Core ground
1218	AM29	VSS	POWER	G		Core ground
1219	AM3	VSS	POWER	G		Core ground
1220	AM33	VSS	POWER	G		Core ground
1221	AM39	VSS	POWER	G		Core ground
1222	AM5	VSS	POWER	G		Core ground
1223	AN1	VSS	POWER	G		Core ground
1224	AN12	VSS	POWER	G		Core ground
1225	AN15	VSS	POWER	G		Core ground
1226	AN16	VSS	POWER	G		Core ground
1227	AN18	VSS	POWER	G		Core ground
1228	AN23	VSS	POWER	G		Core ground
1229	AN25	VSS	POWER	G		Core ground
1230	AN27	VSS	POWER	G		Core ground
1231	AN33	VSS	POWER	G		Core ground
1232	AN36	VSS	POWER	G		Core ground
1233	AN4	VSS	POWER	G		Core ground
1234	AN6	VSS	POWER	G		Core ground
1235	AN9	VSS	POWER	G		Core ground
1236	AP15	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1237	AP20	VSS	POWER	G		Core ground
1238	AP26	VSS	POWER	G		Core ground
1239	AP28	VSS	POWER	G		Core ground
1240	AR10	VSS	POWER	G		Core ground
1241	AR13	VSS	POWER	G		Core ground
1242	AR14	VSS	POWER	G		Core ground
1243	AR17	VSS	POWER	G		Core ground
1244	AR18	VSS	POWER	G		Core ground
1245	AR2	VSS	POWER	G		Core ground
1246	AR20	VSS	POWER	G		Core ground
1247	AR21	VSS	POWER	G		Core ground
1248	AR23	VSS	POWER	G		Core ground
1249	AR3	VSS	POWER	G		Core ground
1250	AR31	VSS	POWER	G		Core ground
1251	AR33	VSS	POWER	G		Core ground
1252	AR5	VSS	POWER	G		Core ground
1253	AT1	VSS	POWER	G		Core ground
1254	AT12	VSS	POWER	G		Core ground
1255	AT15	VSS	POWER	G		Core ground
1256	AT20	VSS	POWER	G		Core ground
1257	AT23	VSS	POWER	G		Core ground
1258	AT25	VSS	POWER	G		Core ground
1259	AT27	VSS	POWER	G		Core ground
1260	AT28	VSS	POWER	G		Core ground
1261	AT33	VSS	POWER	G		Core ground
1262	AT35	VSS	POWER	G		Core ground
1263	AT37	VSS	POWER	G		Core ground
1264	AT39	VSS	POWER	G		Core ground
1265	AT4	VSS	POWER	G		Core ground
1266	AT7	VSS	POWER	G		Core ground
1267	AT9	VSS	POWER	G		Core ground
1268	AU11	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1269	AU14	VSS	POWER	G		Core ground
1270	AU17	VSS	POWER	G		Core ground
1271	AU18	VSS	POWER	G		Core ground
1272	AU20	VSS	POWER	G		Core ground
1273	AU22	VSS	POWER	G		Core ground
1274	AU3	VSS	POWER	G		Core ground
1275	AU6	VSS	POWER	G		Core ground
1276	AU7	VSS	POWER	G		Core ground
1277	AV1	VSS	POWER	G		Core ground
1278	AV12	VSS	POWER	G		Core ground
1279	AV15	VSS	POWER	G		Core ground
1280	AV16	VSS	POWER	G		Core ground
1281	AV19	VSS	POWER	G		Core ground
1282	AV20	VSS	POWER	G		Core ground
1283	AV31	VSS	POWER	G		Core ground
1284	AV4	VSS	POWER	G		Core ground
1285	AV9	VSS	POWER	G		Core ground
1286	AW11	VSS	POWER	G		Core ground
1287	AW14	VSS	POWER	G		Core ground
1288	AW17	VSS	POWER	G		Core ground
1289	AW20	VSS	POWER	G		Core ground
1290	AW26	VSS	POWER	G		Core ground
1291	AW29	VSS	POWER	G		Core ground
1292	AW3	VSS	POWER	G		Core ground
1293	AW35	VSS	POWER	G		Core ground
1294	AW38	VSS	POWER	G		Core ground
1295	AW6	VSS	POWER	G		Core ground
1296	AW8	VSS	POWER	G		Core ground
1297	B34	VSS	POWER	G		Core ground
1298	B38	VSS	POWER	G		Core ground
1299	C11	VSS	POWER	G		Core ground
1300	C13	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1301	C15	VSS	POWER	G		Core ground
1302	C17	VSS	POWER	G		Core ground
1303	C19	VSS	POWER	G		Core ground
1304	C23	VSS	POWER	G		Core ground
1305	C25	VSS	POWER	G		Core ground
1306	C27	VSS	POWER	G		Core ground
1307	C29	VSS	POWER	G		Core ground
1308	C31	VSS	POWER	G		Core ground
1309	C36	VSS	POWER	G		Core ground
1310	C9	VSS	POWER	G		Core ground
1311	D12	VSS	POWER	G		Core ground
1312	D14	VSS	POWER	G		Core ground
1313	D16	VSS	POWER	G		Core ground
1314	D18	VSS	POWER	G		Core ground
1315	D22	VSS	POWER	G		Core ground
1316	D27	VSS	POWER	G		Core ground
1317	D28	VSS	POWER	G		Core ground
1318	D30	VSS	POWER	G		Core ground
1319	D38	VSS	POWER	G		Core ground
1320	D8	VSS	POWER	G		Core ground
1321	E20	VSS	POWER	G		Core ground
1322	E21	VSS	POWER	G		Core ground
1323	E24	VSS	POWER	G		Core ground
1324	E29	VSS	POWER	G		Core ground
1325	E32	VSS	POWER	G		Core ground
1326	E36	VSS	POWER	G		Core ground
1327	F15	VSS	POWER	G		Core ground
1328	F17	VSS	POWER	G		Core ground
1329	F23	VSS	POWER	G		Core ground
1330	F26	VSS	POWER	G		Core ground
1331	F31	VSS	POWER	G		Core ground
1332	F34	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1333	F38	VSS	POWER	G		Core ground
1334	F4	VSS	POWER	G		Core ground
1335	F5	VSS	POWER	G		Core ground
1336	F6	VSS	POWER	G		Core ground
1337	F7	VSS	POWER	G		Core ground
1338	F8	VSS	POWER	G		Core ground
1339	G14	VSS	POWER	G		Core ground
1340	G16	VSS	POWER	G		Core ground
1341	G18	VSS	POWER	G		Core ground
1342	G22	VSS	POWER	G		Core ground
1343	G3	VSS	POWER	G		Core ground
1344	G30	VSS	POWER	G		Core ground
1345	G34	VSS	POWER	G		Core ground
1346	H21	VSS	POWER	G		Core ground
1347	H27	VSS	POWER	G		Core ground
1348	H31	VSS	POWER	G		Core ground
1349	H4	VSS	POWER	G		Core ground
1350	H7	VSS	POWER	G		Core ground
1351	H8	VSS	POWER	G		Core ground
1352	J1	VSS	POWER	G		Core ground
1353	J2	VSS	POWER	G		Core ground
1354	J25	VSS	POWER	G		Core ground
1355	J28	VSS	POWER	G		Core ground
1356	J29	VSS	POWER	G		Core ground
1357	J30	VSS	POWER	G		Core ground
1358	J31	VSS	POWER	G		Core ground
1359	J32	VSS	POWER	G		Core ground
1360	K29	VSS	POWER	G		Core ground
1361	K33	VSS	POWER	G		Core ground
1362	K37	VSS	POWER	G		Core ground
1363	K4	VSS	POWER	G		Core ground
1364	K5	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1365	K6	VSS	POWER	G		Core ground
1366	L20	VSS	POWER	G		Core ground
1367	L21	VSS	POWER	G		Core ground
1368	L22	VSS	POWER	G		Core ground
1369	L25	VSS	POWER	G		Core ground
1370	L26	VSS	POWER	G		Core ground
1371	L27	VSS	POWER	G		Core ground
1372	L28	VSS	POWER	G		Core ground
1373	L29	VSS	POWER	G		Core ground
1374	L3	VSS	POWER	G		Core ground
1375	L35	VSS	POWER	G		Core ground
1376	L39	VSS	POWER	G		Core ground
1377	M10	VSS	POWER	G		Core ground
1378	M14	VSS	POWER	G		Core ground
1379	M15	VSS	POWER	G		Core ground
1380	M18	VSS	POWER	G		Core ground
1381	M24	VSS	POWER	G		Core ground
1382	M36	VSS	POWER	G		Core ground
1383	M4	VSS	POWER	G		Core ground
1384	M7	VSS	POWER	G		Core ground
1385	N1	VSS	POWER	G		Core ground
1386	N11	VSS	POWER	G		Core ground
1387	N2	VSS	POWER	G		Core ground
1388	N28	VSS	POWER	G		Core ground
1389	N35	VSS	POWER	G		Core ground
1390	N9	VSS	POWER	G		Core ground
1391	P12	VSS	POWER	G		Core ground
1392	P25	VSS	POWER	G		Core ground
1393	P26	VSS	POWER	G		Core ground
1394	P27	VSS	POWER	G		Core ground
1395	P28	VSS	POWER	G		Core ground
1396	P29	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1397	P30	VSS	POWER	G		Core ground
1398	P35	VSS	POWER	G		Core ground
1399	P39	VSS	POWER	G		Core ground
1400	P4	VSS	POWER	G		Core ground
1401	P5	VSS	POWER	G		Core ground
1402	P7	VSS	POWER	G		Core ground
1403	R10	VSS	POWER	G		Core ground
1404	R13	VSS	POWER	G		Core ground
1405	R17	VSS	POWER	G		Core ground
1406	R23	VSS	POWER	G		Core ground
1407	R24	VSS	POWER	G		Core ground
1408	R25	VSS	POWER	G		Core ground
1409	R26	VSS	POWER	G		Core ground
1410	R27	VSS	POWER	G		Core ground
1411	R37	VSS	POWER	G		Core ground
1412	R4	VSS	POWER	G		Core ground
1413	T11	VSS	POWER	G		Core ground
1414	T31	VSS	POWER	G		Core ground
1415	T36	VSS	POWER	G		Core ground
1416	T39	VSS	POWER	G		Core ground
1417	T8	VSS	POWER	G		Core ground
1418	U14	VSS	POWER	G		Core ground
1419	U15	VSS	POWER	G		Core ground
1420	U16	VSS	POWER	G		Core ground
1421	U17	VSS	POWER	G		Core ground
1422	U18	VSS	POWER	G		Core ground
1423	U19	VSS	POWER	G		Core ground
1424	U20	VSS	POWER	G		Core ground
1425	U21	VSS	POWER	G		Core ground
1426	U22	VSS	POWER	G		Core ground
1427	U23	VSS	POWER	G		Core ground
1428	U24	VSS	POWER	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1429	U25	VSS	POWER	G		Core ground
1430	U26	VSS	POWER	G		Core ground
1431	U27	VSS	POWER	G		Core ground
1432	U3	VSS	POWER	G		Core ground
1433	U32	VSS	POWER	G		Core ground
1434	U33	VSS	POWER	G		Core ground
1435	U34	VSS	POWER	G		Core ground
1436	U37	VSS	POWER	G		Core ground
1437	U4	VSS	POWER	G		Core ground
1438	U6	VSS	POWER	G		Core ground
1439	V36	VSS	POWER	G		PCIe x4 0 ground
1440	V39	VSS	POWER	G		PCIe x4 0 ground
1441	W1	VSS	POWER	G		PCIe x4 0 ground
1442	W11	VSS	POWER	G		PCIe x4 1 ground
1443	W13	VSS	POWER	G		PCIe x4 1 ground
1444	W14	VSS	POWER	G		PCIe x4 1 ground
1445	W15	VSS	POWER	G		PCIe x8 ground
1446	W16	VSS	POWER	G		PCIe x8 ground
1447	W17	VSS	POWER	G		PCIe x8 ground
1448	W18	VSS	POWER	G		PCIe x8 ground
1449	W19	VSS	POWER	G		PCIe x8 ground
1450	W2	VSS	POWER	G		PCIe x8 ground
1451	W20	VSS	POWER	G		SATA (PHY) ground
1452	W21	VSS	POWER	G		USB 2 0 ground
1453	W22	VSS	POWER	G		USB 2 0 ground
1454	W23	VSS	POWER	G		USB 2 1 ground
1455	W24	VSS	POWER	G		USB 2 2 ground
1456	W25	VSS	POWER	G		USB 2 3 ground
1457	W26	VSS	POWER	G		USB 3 0 PHY ground
1458	W27	VSS	POWER	G		USB 3 1 PHY ground
1459	W3	VSS	POWER	G		USB 3 0 PHY ground
1460	W33	VSS	POWER	G		USB 3 1 PHY ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1461	W34	VSS	POWER	G		XGbE 0 ground
1462	W37	VSS	POWER	G		XGbE 0 ground
1463	W7	VSS	POWER	G		XGbE 0 ground
1464	Y36	VSS	POWER	G		XGbE 1 ground
1465	Y39	VSS	POWER	G		XGbE 1 ground
1466	Y9	VSS	POWER	G		XGbE 1 ground
1467	M28	VSS_PVT	POWER	G		PVT sensor ground
1468	A4	VSSIO	POWER	G		IO ground
1469	AA28	VSSIO	POWER	G		IO ground
1470	AA29	VSSIO	POWER	G		IO ground
1471	AA30	VSSIO	POWER	G		IO ground
1472	AA31	VSSIO	POWER	G		IO ground
1473	AC15	VSSIO	POWER	G		IO ground
1474	AC28	VSSIO	POWER	G		IO ground
1475	AC29	VSSIO	POWER	G		IO ground
1476	AC30	VSSIO	POWER	G		IO ground
1477	AC31	VSSIO	POWER	G		IO ground
1478	AD10	VSSIO	POWER	G		IO ground
1479	AD12	VSSIO	POWER	G		IO ground
1480	AE7	VSSIO	POWER	G		IO ground
1481	AF8	VSSIO	POWER	G		IO ground
1482	AG9	VSSIO	POWER	G		IO ground
1483	B4	VSSIO	POWER	G		IO ground
1484	D1	VSSIO	POWER	G		IO ground
1485	D3	VSSIO	POWER	G		IO ground
1486	H35	VSSIO	POWER	G		IO ground
1487	J33	VSSIO	POWER	G		IO ground
1488	J37	VSSIO	POWER	G		IO ground
1489	L30	VSSIO	POWER	G		IO ground
1490	M32	VSSIO	POWER	G		IO ground
1491	N29	VSSIO	POWER	G		IO ground
1492	P15	VSSIO	POWER	G		IO ground

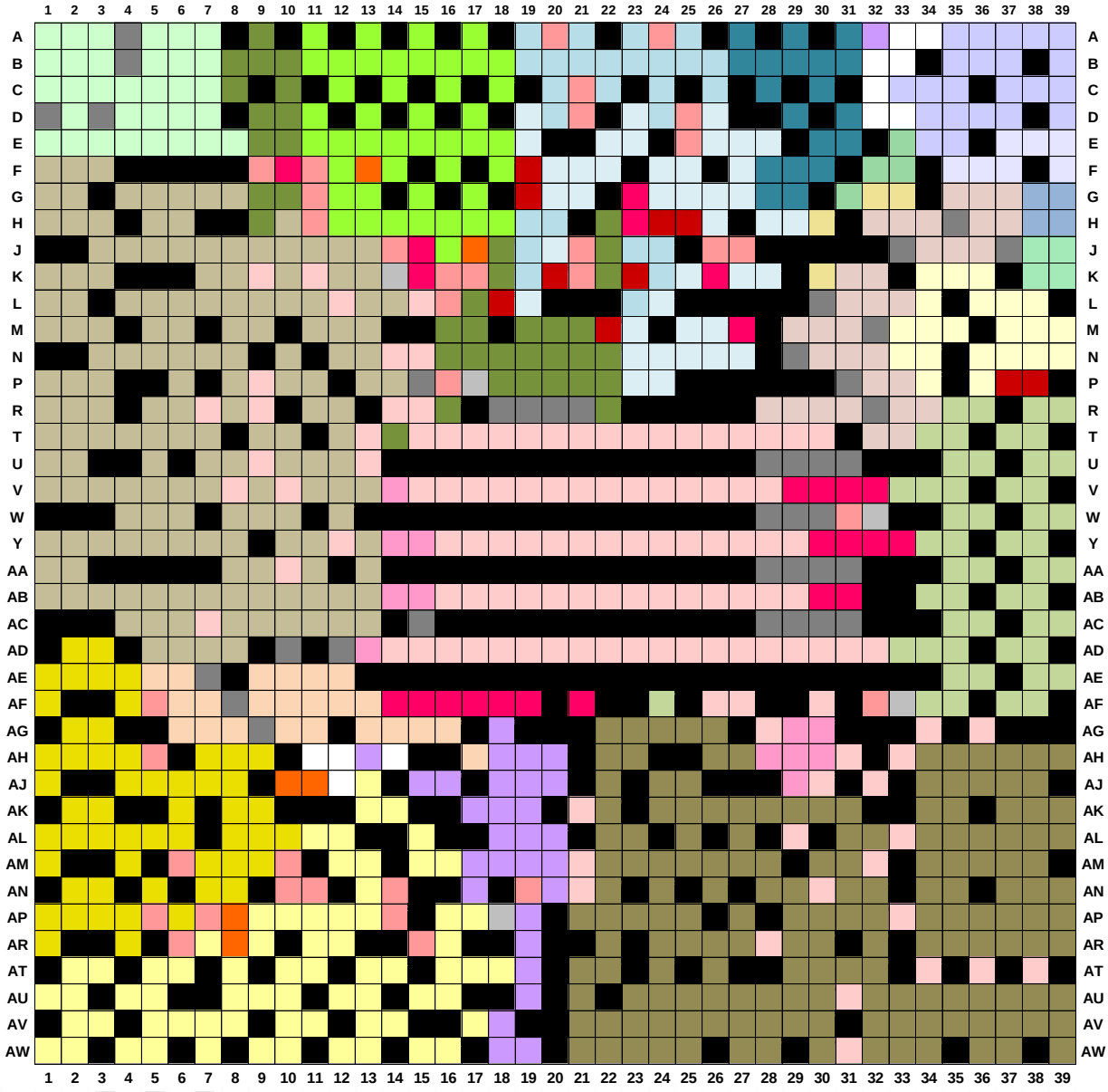
Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1493	P31	VSSIO	POWER	G		IO ground
1494	R18	VSSIO	POWER	G		IO ground
1495	R19	VSSIO	POWER	G		IO ground
1496	R20	VSSIO	POWER	G		IO ground
1497	R21	VSSIO	POWER	G		IO ground
1498	R32	VSSIO	POWER	G		IO ground
1499	U28	VSSIO	POWER	G		IO ground
1500	U29	VSSIO	POWER	G		IO ground
1501	U30	VSSIO	POWER	G		IO ground
1502	U31	VSSIO	POWER	G		IO ground
1503	W28	VSSIO	POWER	G		IO ground
1504	W29	VSSIO	POWER	G		IO ground
1505	W30	VSSIO	POWER	G		IO ground
1506	P17	VSSPLL_0	POWER	G		PLL ground
1507	W32	VSSPLL_1	POWER	G		PLL ground
1508	AF33	VSSPLL_2	POWER	G		PLL ground
1509	AP18	VSSPLL_3	POWER	G		PLL ground
1510	K14	VSSPLL_HDMI	POWER	G		HDMI PLL ground
1511	C32		N/C	NC		Reserved
1512	D32		N/C	NC		Reserved
1513	A34		N/C	NC		Reserved
1514	B33		N/C	NC		Reserved
1515	A33		N/C	NC		Reserved
1516	B32		N/C	NC		Reserved
1517	D33		N/C	NC		Reserved
1518	AJ12		N/C	NC		Reserved
1519	AH11		N/C	NC		Reserved
1520	AH12		N/C	NC		Reserved
1521	AH14		N/C	NC		Reserved

NOTE: Reserved pins should be left floating

5.2 Package Ball Map

The diagrams below show pinout from the top view of the package.



Power & Ground

	VDD
	VDD 0.9V, 0.95V
	VDD 1.2V, 1.5V
	VDD 1.8V
	VDD 3.3V
	VDD DDR PLL
	VSS
	VSSIO
	VSSPLL

Audio & Video

	LVDS
	HDMI
	I2S

High Speed Peripherals

	PCIE x8
	PCIE x4_0, PCIE x4_1
	USB 3.0/2.0
	USB 2.0
	SATA_0, SATA_1
	XGMAC0, XGMAC1
	GMAC0, GMAC1
	eMMC/SD

Low Speed Peripherals

	GPIO*32
	UART_1, UART_2
	SPI
	eSPI
	I2C_1, I2C_2
	SMBus_1, SMBus_2

Memory

	DDR0
	DDR1

System Control & Debug

	System Control
	System Debug

Figure 5-1 Ball Map

5.2.1 Power and Ground

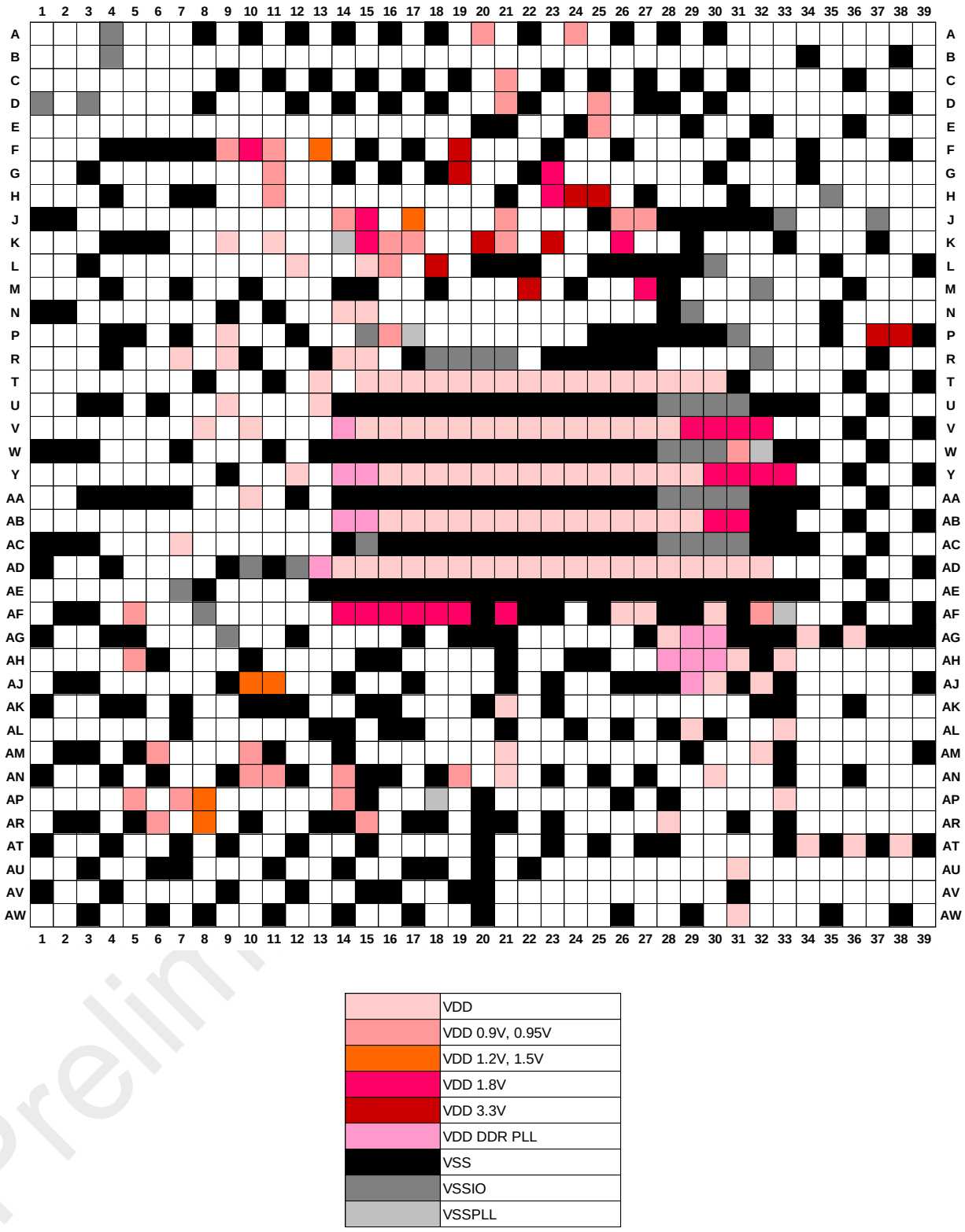


Figure 5-2 Power and Ground Pin Placement

5.2.2 High Speed Peripherals

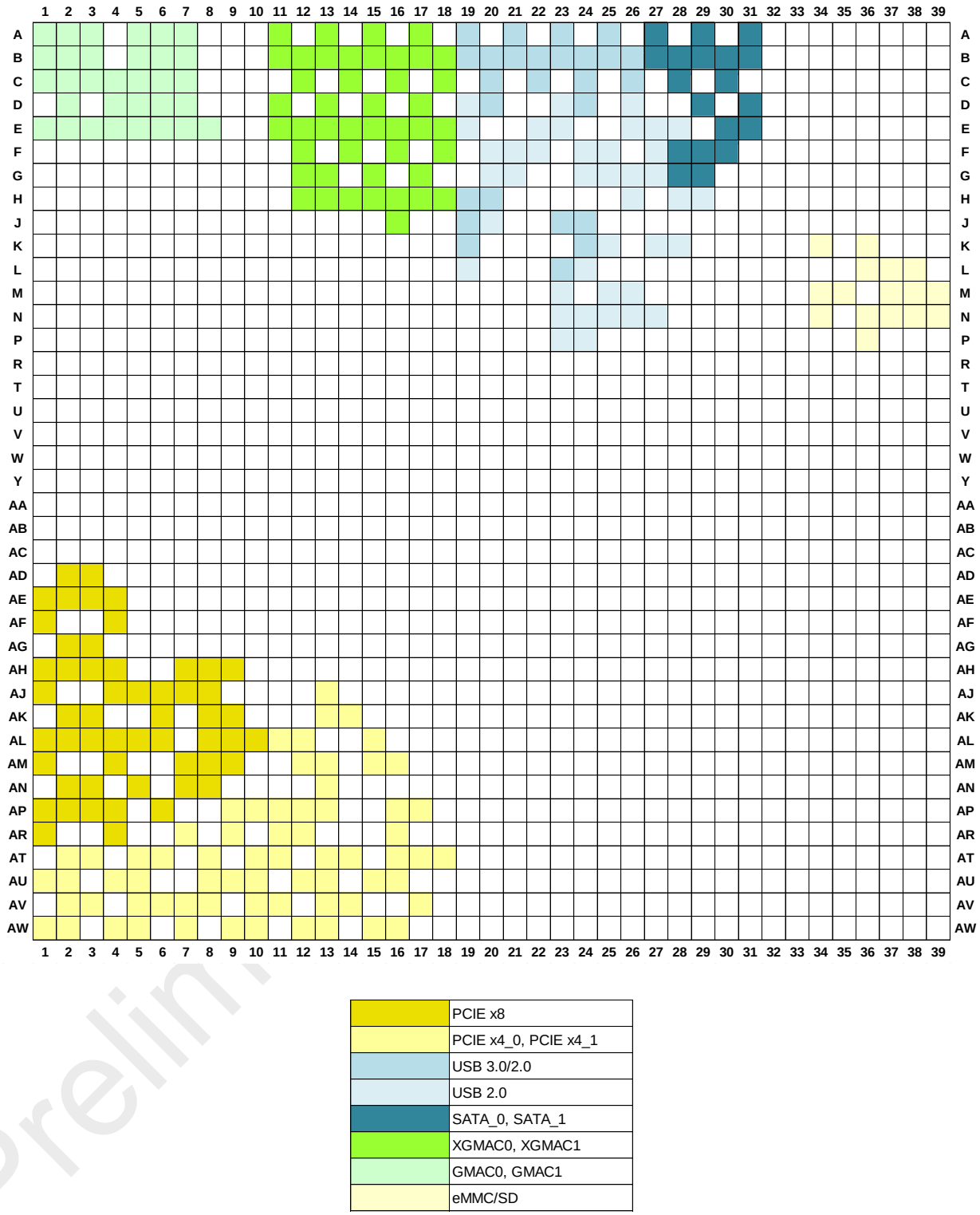


Figure 5-3 High Speed Peripherals Pin Placement

5.2.3 Low Speed Peripherals

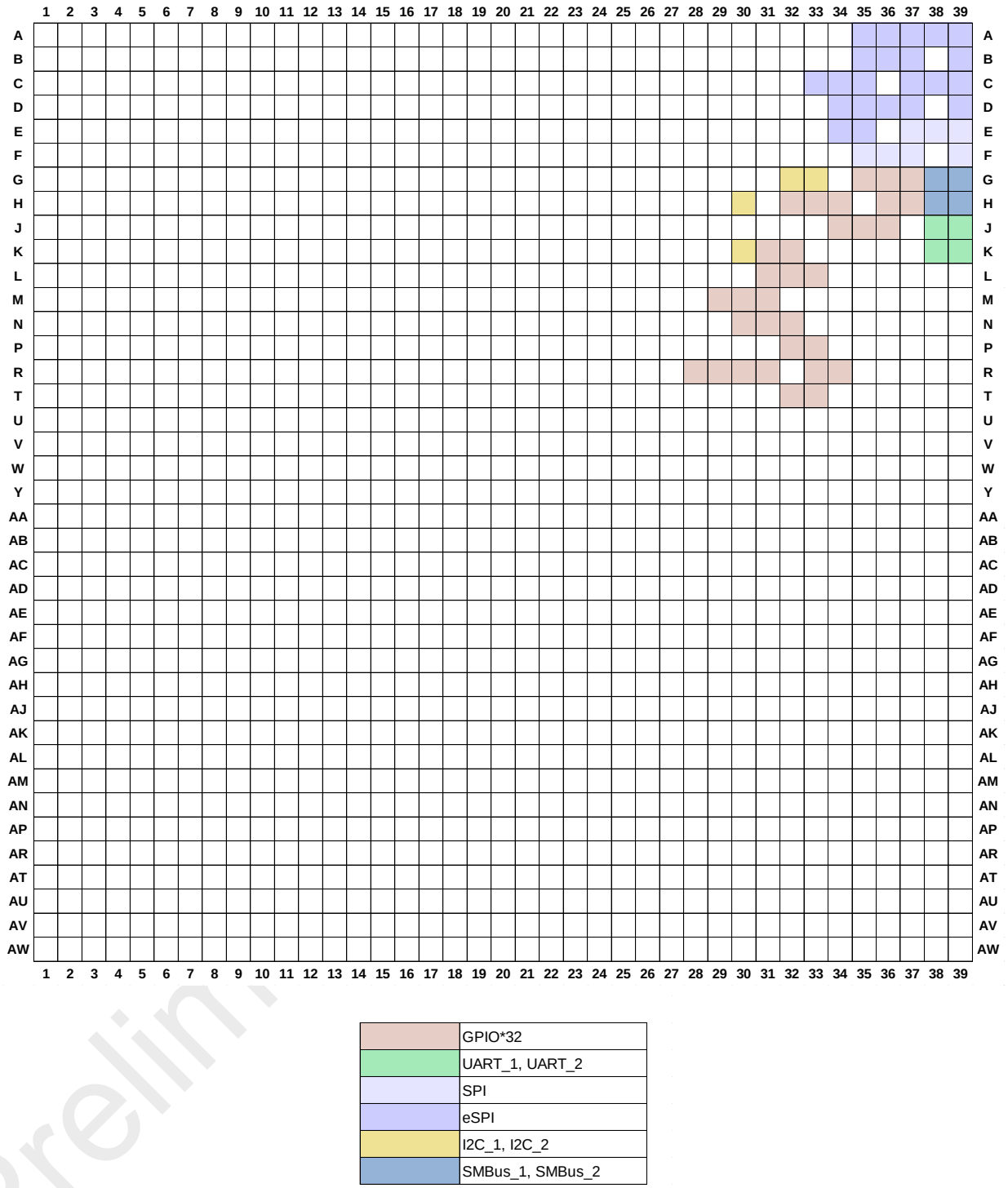


Figure 5-4 Low Speed Peripherals Pin Placement

5.2.4 Memory

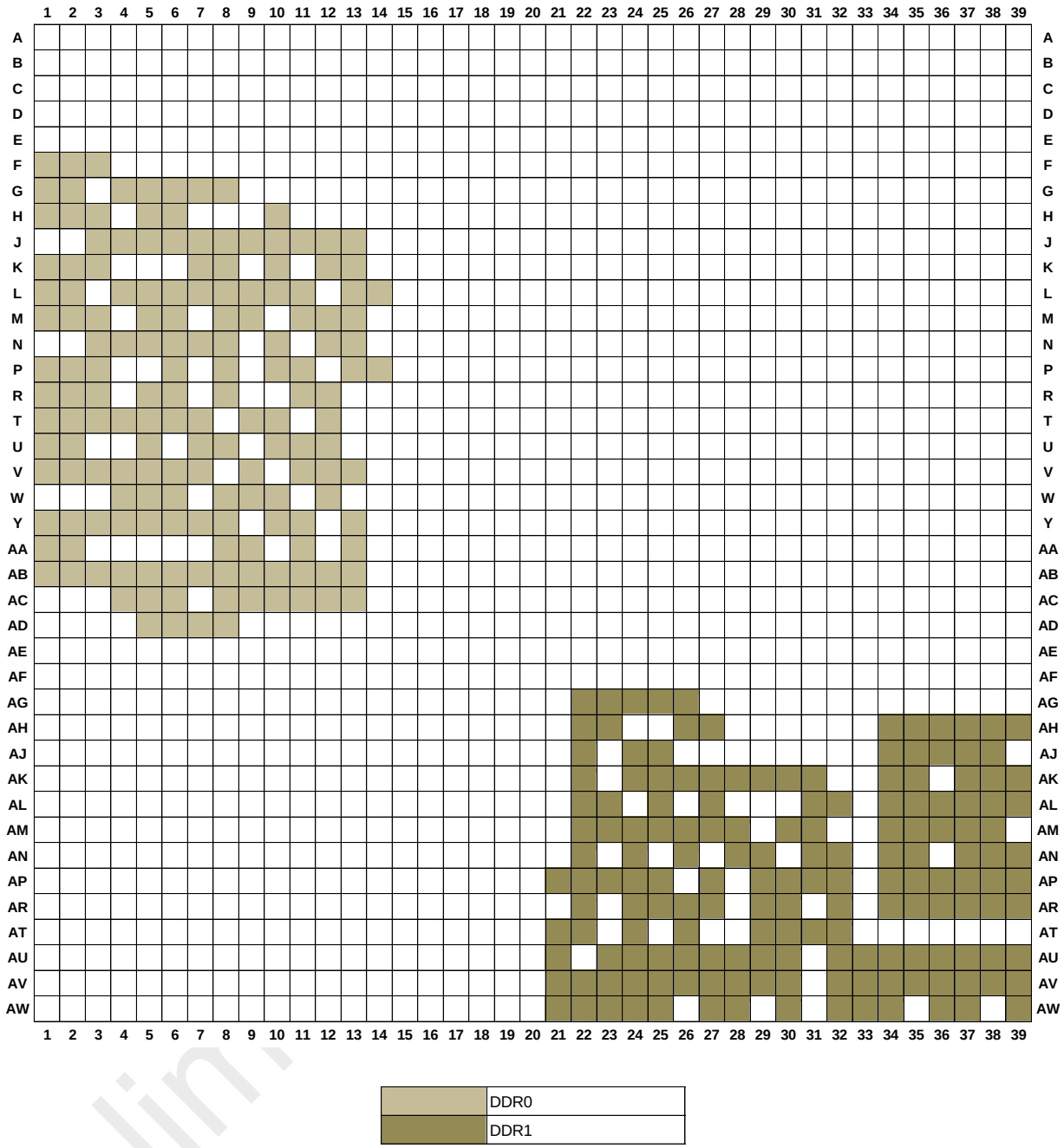


Figure 5-5 Memory Pin Placement

5.2.5 Audio and Video

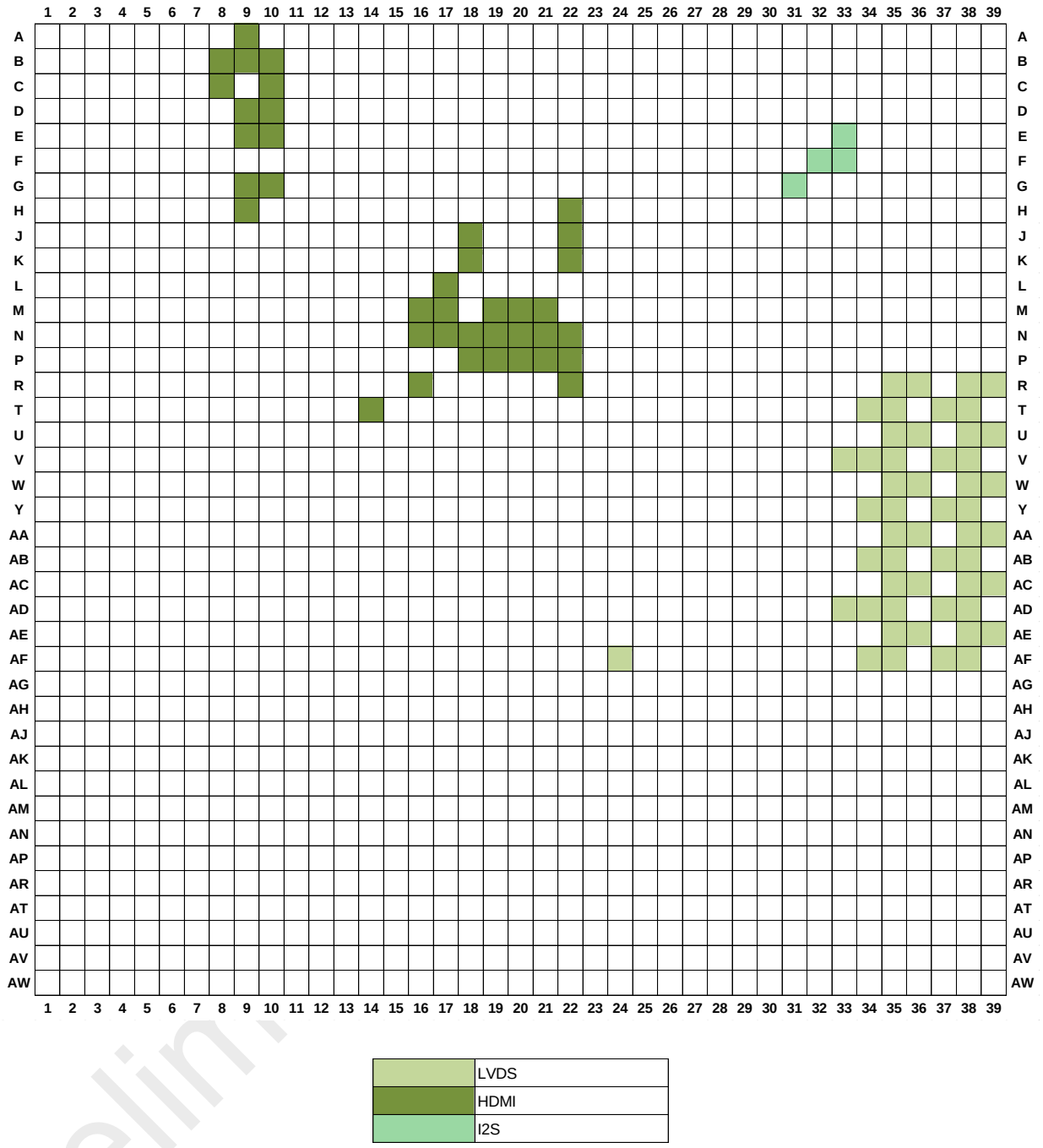


Figure 5-6 Audio and Video Pin Placement

5.2.6 System Control and Debug

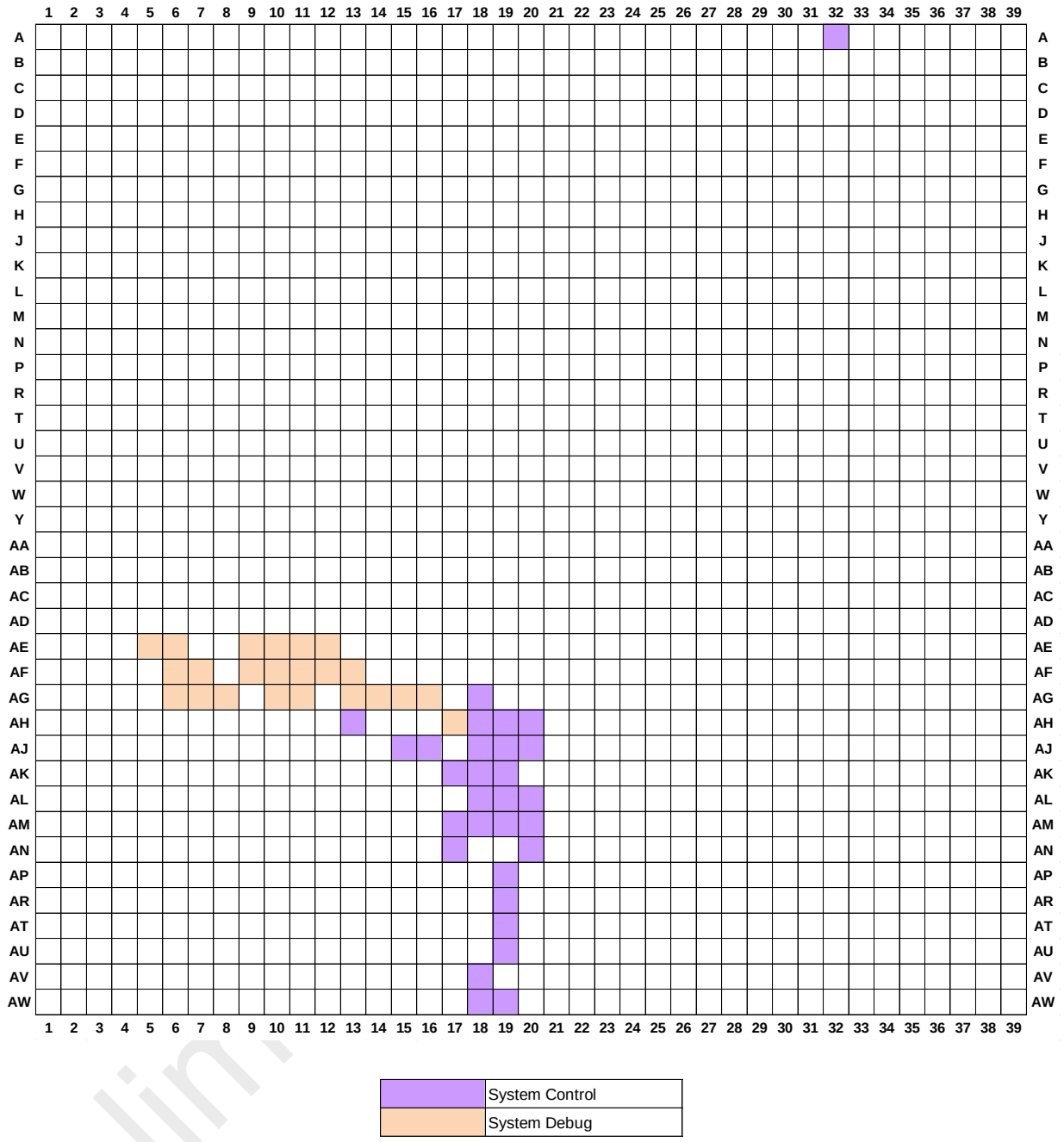


Figure 5-7 System Control and Debug Pin Placement

6 Package Information

6.1 FCBGA-1521 Package

SoC is mounted into FCBGA-1521 package. Main package parameters are shown it the figures and table below.

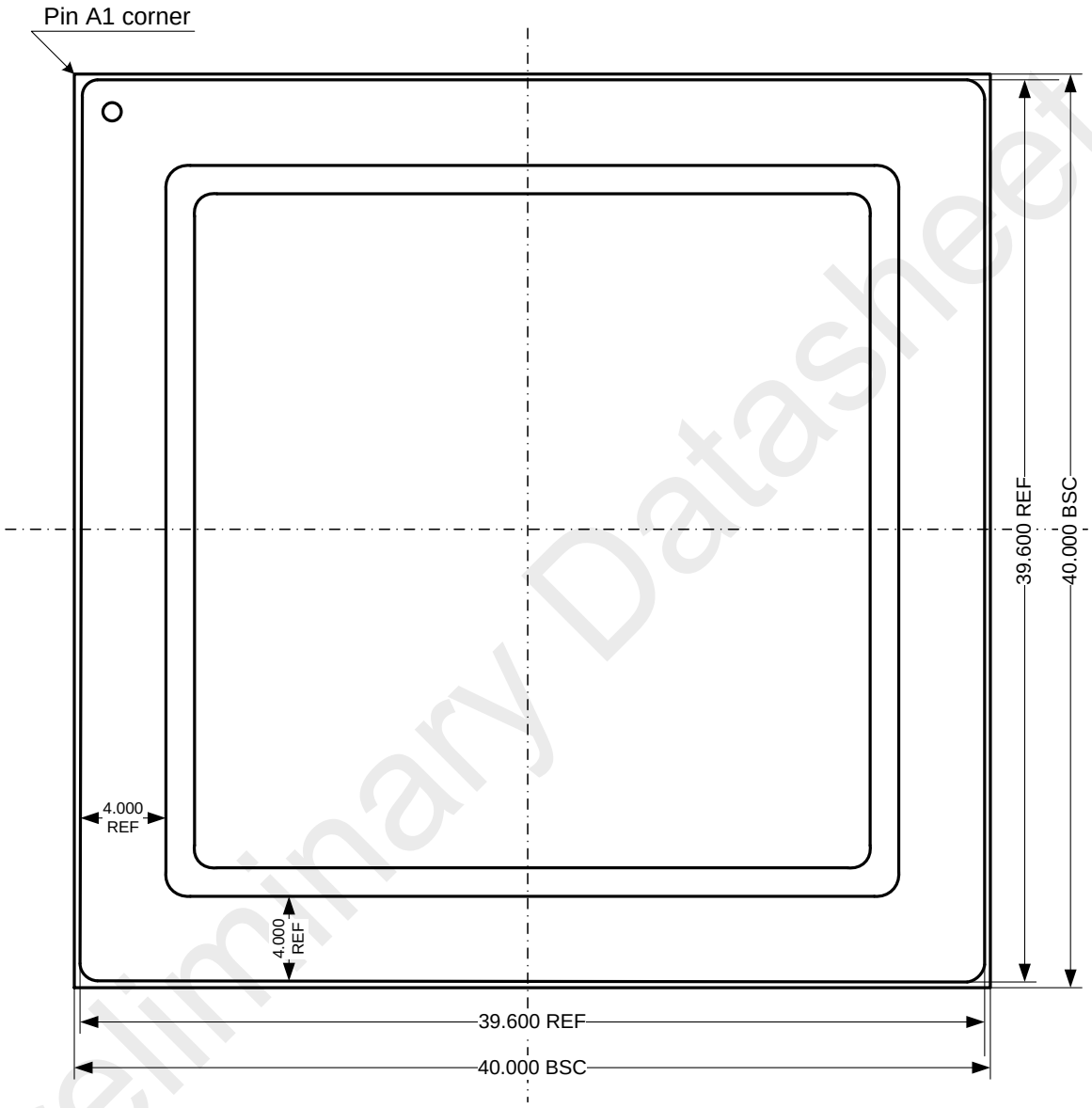


Figure 6-1 SoC package. Top View

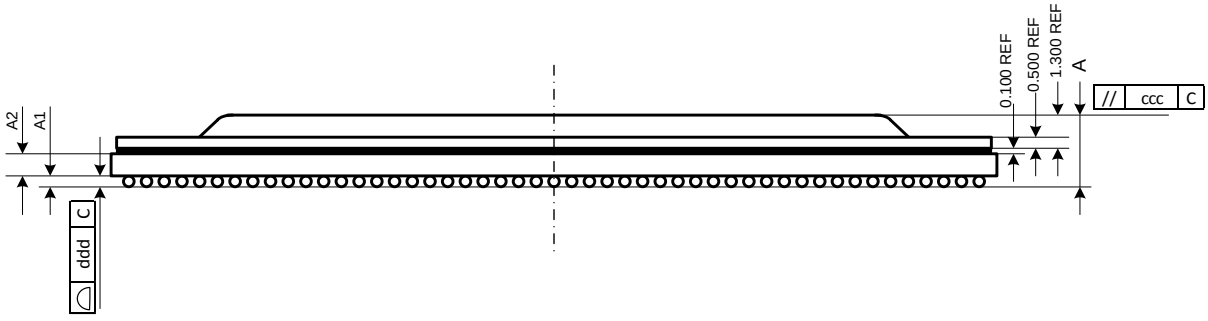


Figure 6-2 SoC package. Side View

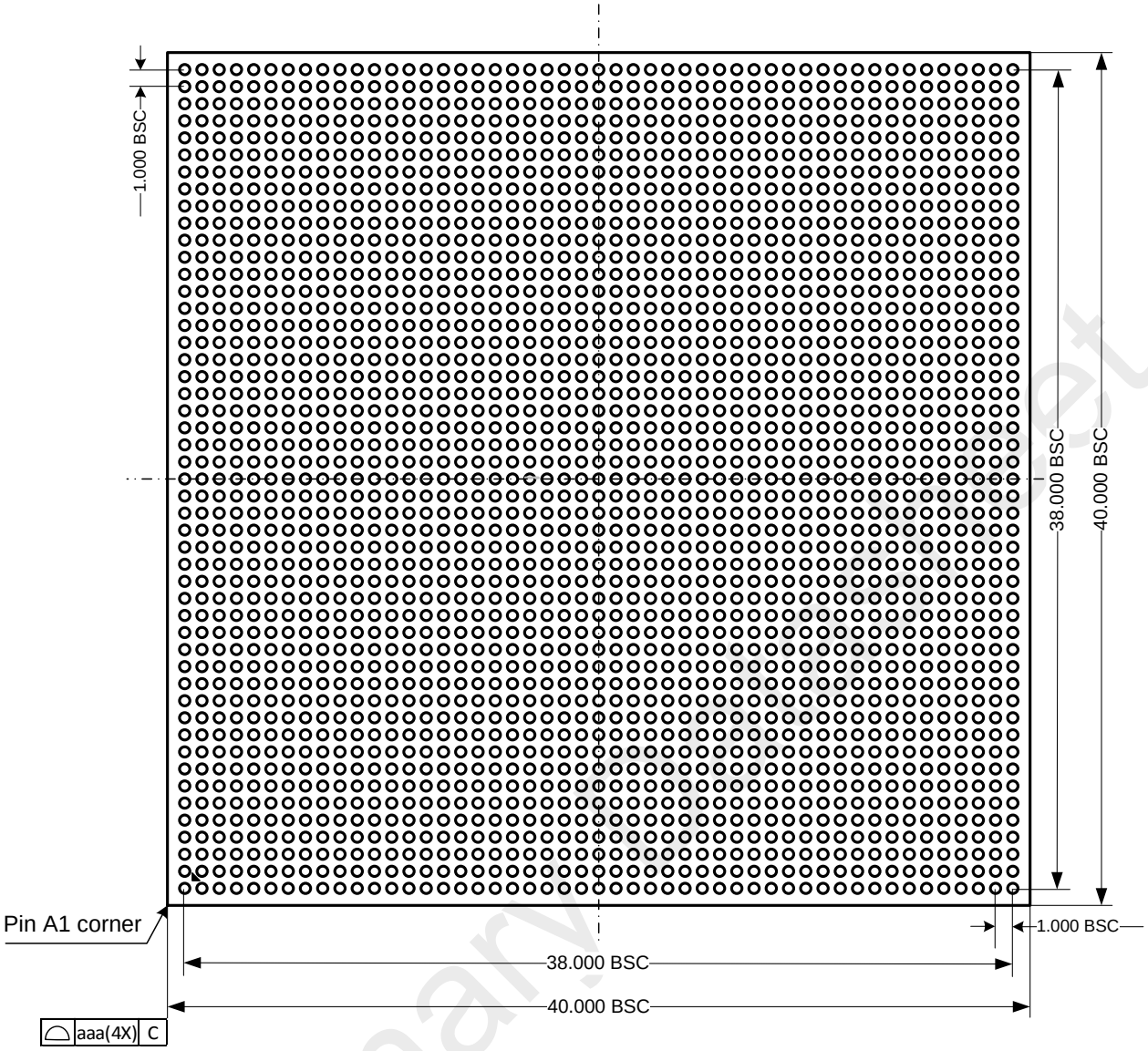


Figure 6-3 SoC package. Bottom View

The following table shows the package parameters.

Table 6-1 Package Parameters

Dimension	Symbol	Value		
		Min.	Nom.	Max.
Total thickness	A	2.676	2.976	3.176
Stand off	A1	0.400	-	0.600
Substrate thickness	A2	1.026 REF		
Body size		40.000 BSC		
		40.000 BSC		
Ball diameter		0.600		
Ball width		0.500	-	0.700
Ball pitch		1.000 BSC		

Table 6-1 Package Parameters (continued)

Dimension	Symbol	Value
Ball count		1521
Edge ball center to center		38.000 BSC
		38.000 BSC
Package edge tolerance	aaa	0.200
Top parallelism	ccc	0.350
Coplanarity	ddd	0.200

6.2 Soldering

SoC mounting to PCB should be accomplished in accordance to the soldering profile recommended for Pb-Free packages. Corresponding modes and temperatures are described in the following table and figure.

Table 6-2 Temperature Profile for SoC Soldering to PCB

Profile Feature	Description	Temperature	Duration
A	Preheat stage	150-200°C	60-120 seconds
B	Melting stage	>217°C	60-150 seconds
C	Ramp-up rate	3°C/sec max.	
D	Peak temperature	245°C	
E	Soldering stage	>240°C	30 seconds min.
F	Time from room temperature to peak temperature		< 8 minutes max.
G	Ramp-down rate	6°C/sec max.	

All temperatures refer to topside of the package, measured on the package body surface.

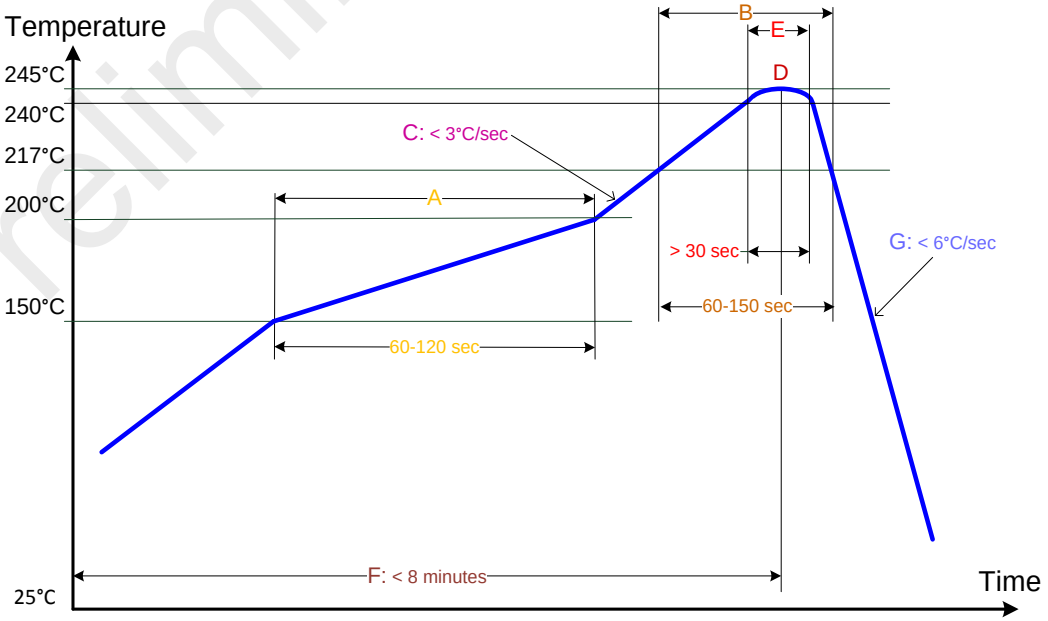


Figure 6-4 Soldering Profile

7 Ordering Information

BE-M1000 is orderable part number. Designation of each field in the part number is shown in a table below.

Table 7-1 Ordering information

BE	-	M	1	0	0	0
Baikal Electronics	field delimiter	product line	generation	modification	reserved field	packaging

BE-M1000 is the first product in BE-M product line.

To order BE-M1000 please contact Baikal Electronics company referred in the next page.

Contact Info

Baikal Electronics: https://www.baikalelectronics.com/

Head Office: https://www.baikalelectronics.com/contacts/

Mail: info@baikalelectronics.ru

Phone: +7 495 221-39-47

Revision History

Revision	Date	Substantive change(s)
0.65	02.07.2019	Initial version
0.70	01.11.2019	The Section 4 has some corrections: • Correction of power-up order • The information about power-up sequence
0.72	11.12.2019	The Section 4 has the information about power-down. The Section 5 has new information about pins AM19 and AL18
0.73	16.12.2019	The following pins changed pin IDs: DDR0_DQ[18], DDR0_DQ[19], DDR0_DQ[20], DDR0_DQ[21], DDR0_DQ[26], DDR0_DQ[27], DDR0_DQ[28], DDR0_DQ[29], DDR0_DQ[41], DDR0_DQ[44], DDR0_DQ[48], DDR0_DQ[51], DDR0_DQ[52], DDR0_DQ[53], DDR0_DQ[56], DDR0_DQ[63]
0.74	04.03.2020	The Section 2.4 has the information about unaccessability of boot controller's dedicated interfaces for Cortex-A57 cores
0.82	25.05.2020	The Section 4.1 has new steps between DDR supply and 1.8V voltage supply
0.83	13.07.2020	The operating frequency value of Arm Mali T-628 GPU shader cores changed from 500 MHz to 700 MHz