

Lab 2 注意事项

- 硬件: xc7a35tcpg236-1 (Basys3)
- 软件: Vivado 2014.4
- 实验附件: tutorial.zip
- 修改tutorial.sv文件
- 实验结果与视频对比一致后, 找助教检查登记

修改tutorial.sv文件

Behavioral Simulation - Functional - sim_1 - tutorial_tb

Sources

Messages: 4 critical warnings

Design Sources (2)

- Syntax Error Files (1)
- Non-module Files (1)

Constraints (1)

- constrs_1 (1)
 - Basys3_Master.xdc

Simulation Sources (3)

- sim_1 (3)
 - Syntax Error Files (1)

Hierarchy Libraries Compile Order

Scope Sources

Source File Properties

tutorial.sv

D:/code/hdl/LAB2/tutorial.sv

```
timescale 1ns / 1ps
// Module Name: tutorial
module tutorial(
    input logic [7:0] swt,
    output logic [7:0] led
);
    assign led[0] = // TODO
    assign led[1] = // TODO
    assign led[3] = // TODO
    assign led[2] = led[1] | led[3];
    assign led[7:4] = // TODO
endmodule
```