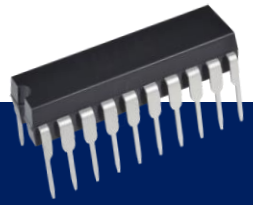

Computer System (I)

MIPS
SLL Implementation

朱金辉

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SLL (shift left logical)

Table B.2 R-type instructions, sorted by funct field

Funct	Name	Description	Operation
000000 (0)	`sll rd, rt, shamt`	shift left logical	`[rd] = [rt] << shamt`

R-Type

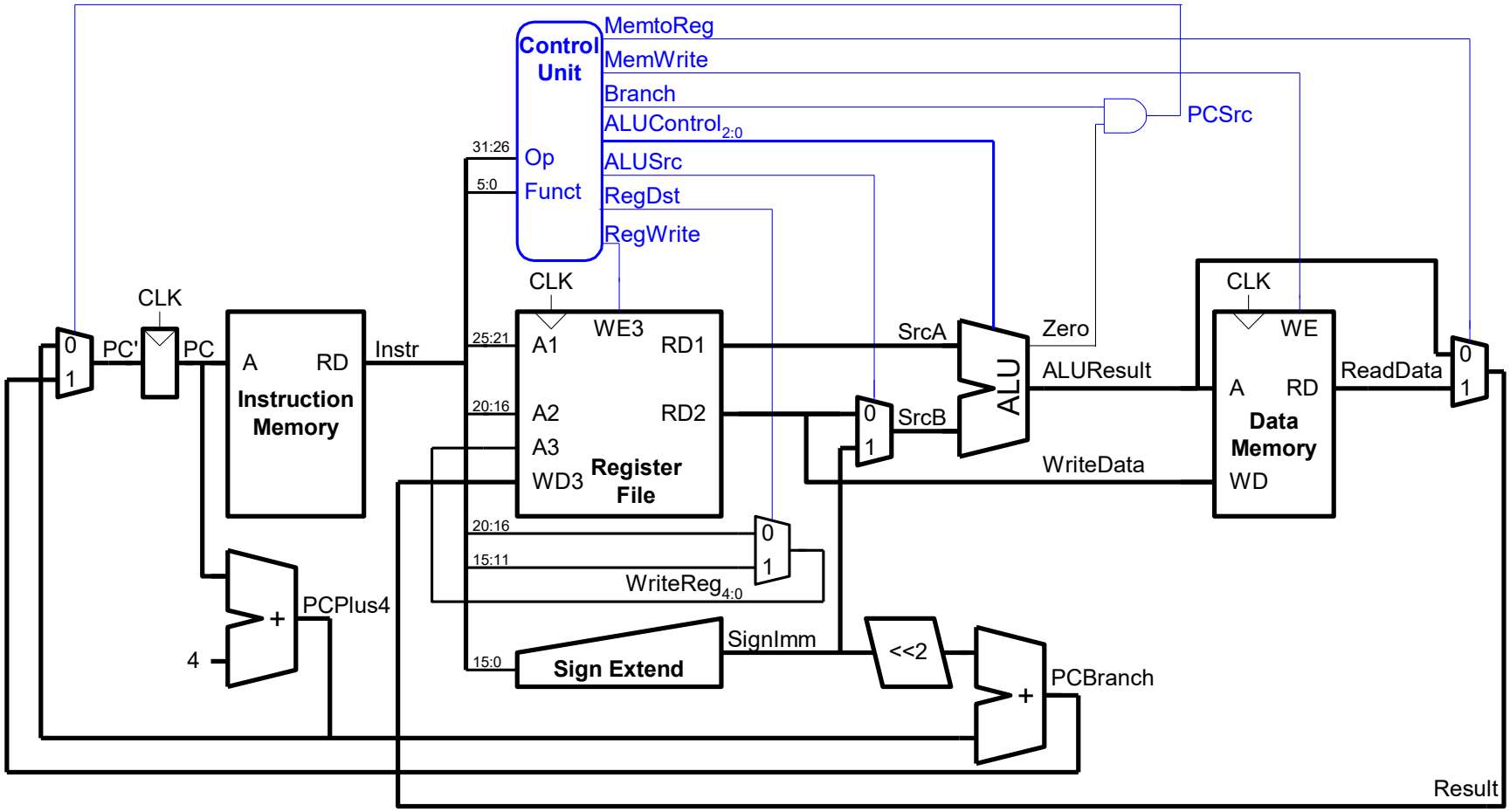
Assembly code
sll $0,$0,0

Machine Code
0x00000000

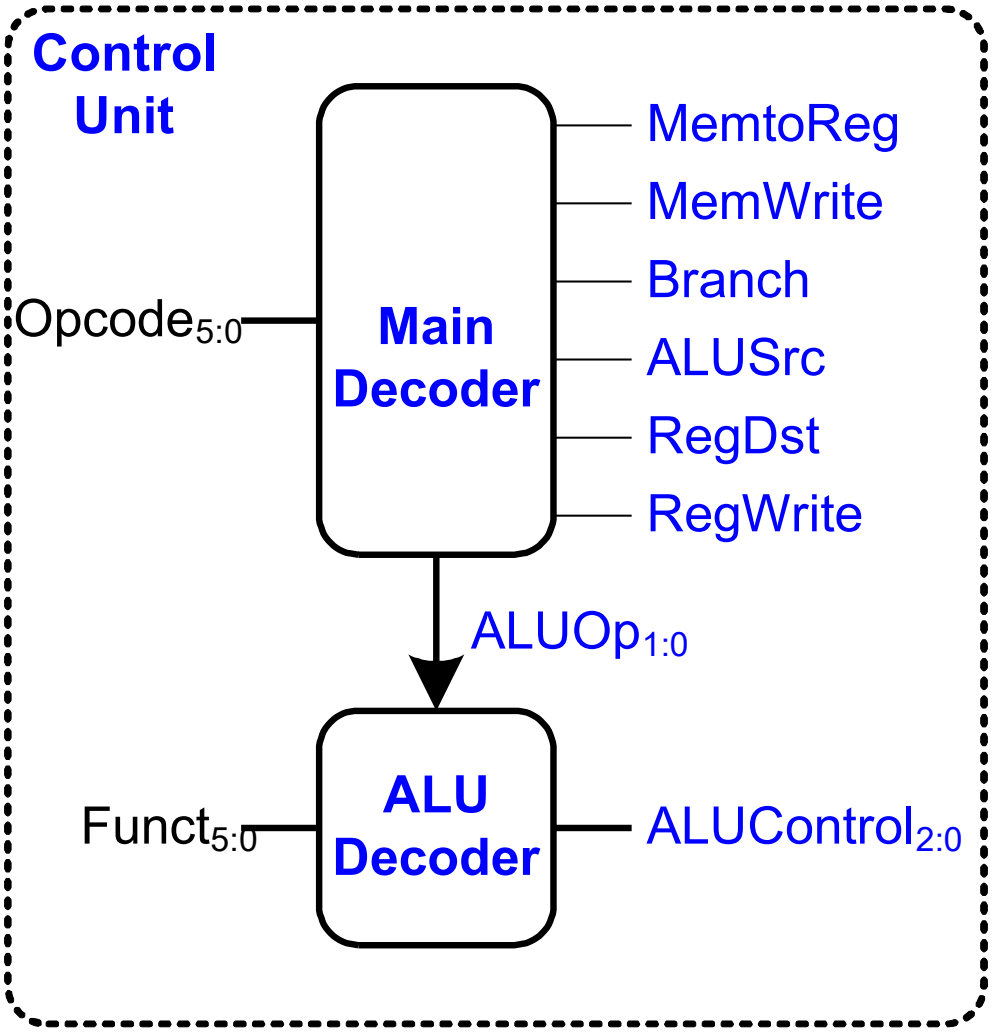
Assembly code
sll $8, $9, 1

Machine Code
0x00094040
000000 00000 01001 01000 00001 000000

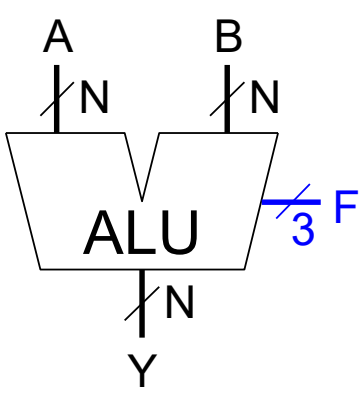
Review: Single-Cycle Processor

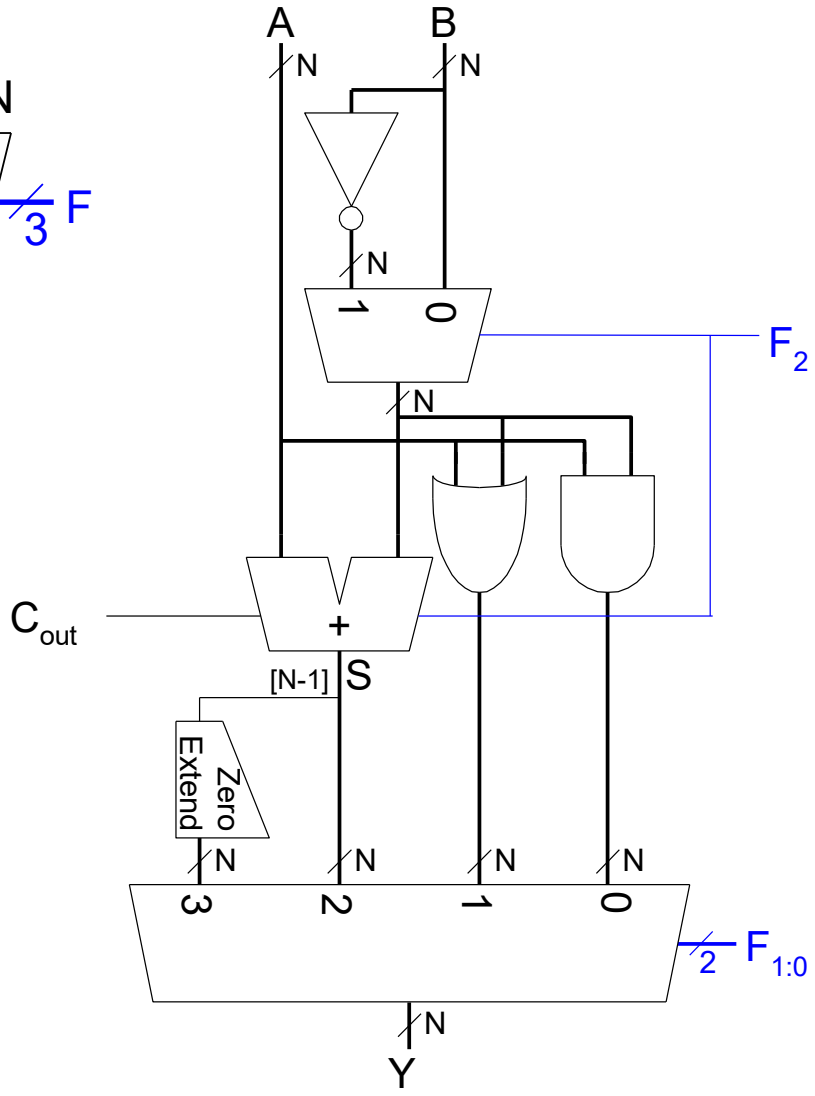


Review: Single-Cycle Control



Review: ALU

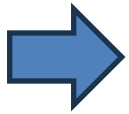




$F_{2:0}$	Function
000	A & B
001	A | B
010	A + B
011	not used
100	A & ~B
101	A | ~B
110	A - B
111	SLT

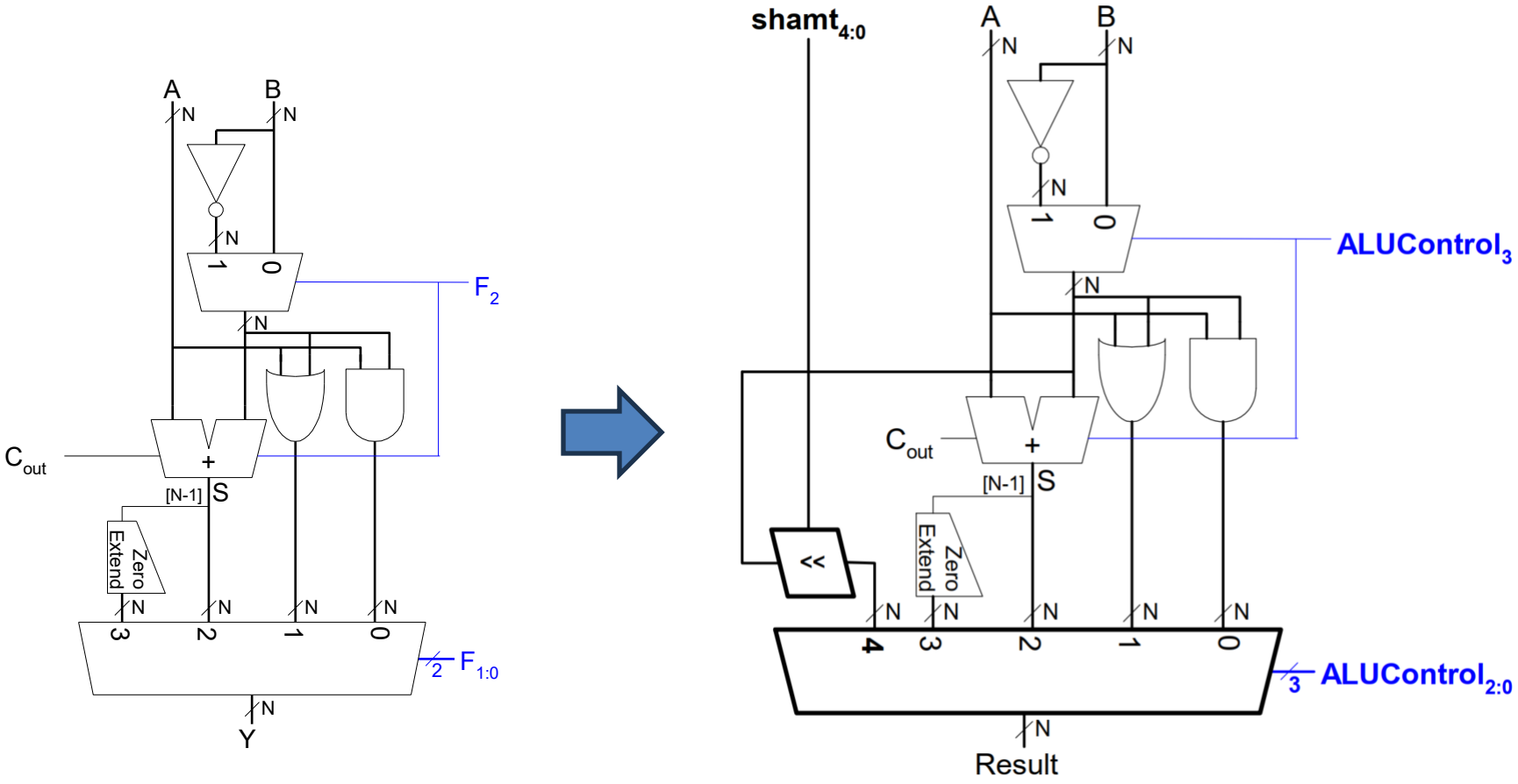
Modified ALU to support sll

$F_{2:0}$	Function
000	A & B
001	A | B
010	A + B
011	not used
100	A & ~B
101	A | ~B
110	A - B
111	SLT



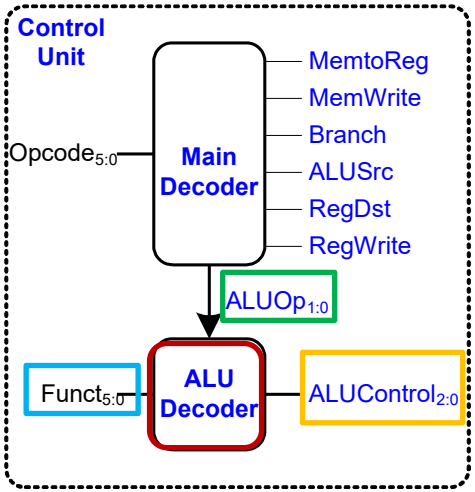
$ALUControl_{3:0}$	Function
0000	A & B
0001	A | B
0010	A + B
0011	not used
1000	A & ~B
1001	A | ~B
1010	A - B
1011	SLT
0100	SLL

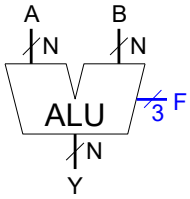
Modified ALU to support sll



Review Control Unit: ALU Decoder

$ALUOp_{1:0}$	Meaning
00	Add
01	Subtract
10	Look at Funct
11	Not Used





$ALUOp_{1:0}$	$Funct_{5:0}$	$ALUControl_{2:0}$
00	X	010 (Add)
01	X	110 (Subtract)
10	100000 (`add`)	010 (Add)
10	100010 (`sub`)	110 (Subtract)
10	100100 (`and`)	000 (And)
10	100101 (`or`)	001 (Or)
10	101010 (`slt`)	111 (SLT)

Modified ALU Decoder

$ALUOp_{1:0}$	$Funct_{5:0}$	$ALUControl_{3:0}$
00	X	0010 (Add)
01	X	1010 (Subtract)
10	100000 (`add`)	0010 (Add)
10	100010 (`sub`)	1010 (Subtract)
10	100100 (`and`)	0000 (And)
10	100101 (`or`)	0001 (Or)
10	101010 (`slt`)	1011 (SLT)
10	000000 (`sll`)	0100 (SLL)

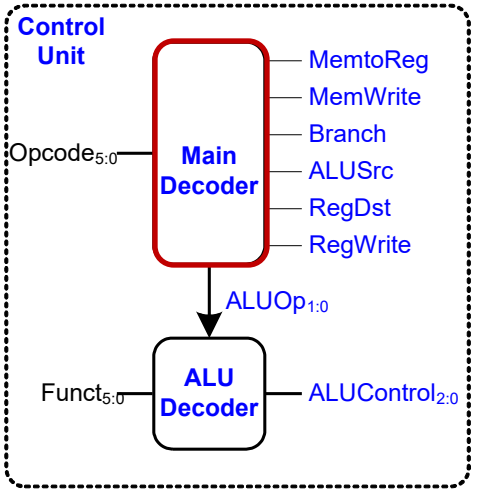
$ALUControl_{3:0}$	Function
0000	A & B
0001	A | B
0010	A + B
0011	not used
1000	A & ~B
1001	A | ~B
1010	A - B
1011	SLT
0100	SLL

Review Control Unit: Main Decoder

Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	$ALUOp_{1:0}$
R-type	000000	1	1	0	0	0	0	10
`lw`	100011	1	0	1	0	0	1	00
`sw`	101011	0	X	1	0	1	X	00
`beq`	000100	0	X	0	1	0	X	01

R-Type

No change Main Decoder



Modified processor with sll