Advanced Interface Bus for Standard Packaging (AIB-O) Specification

2021.8.3

Revision 0.7

Revision History

Date	Version	Summary Of Changes	
8/3/2021	0.7	30	Add standard packaging AIB-O support
		33	Updated AIB-O bump map again
		36	Replaced AIB-O sideband with link registers and link controller
		37	Removed requirement for AIB-O gap every 6 channels
		38	Pull AIB-O into its own specification

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1 Introduction, AIB on Standard Packaging (AIB-O)

AIB on Standard Packaging, or AIB-O, is an AIB 2.0 variant for applications that desire a high bandwidth parallel interface without using advanced high-density packaging technology.

AIB-O is intended for chip-to-chip interconnect within a package with typical signal distances of 5 millimeters or less. There is no maximum interconnect distance specified; instead, the AIB-O electrical requirements must be met.

AIB-O shares all requirements of AIB 2.0 Gen2 except as defined in this document. Please refer to “Advanced Interface Bus (AIB) Specification” for the base of requirements.

1.1 AIB-O Interface

1.1.1 AIB-O Channel

AIB-O uses a subset of the AIB channel signals:

- Data signals
  - Inputs (*RX*): data input signals received by the interface
  - Outputs (*TX*): data output signals transmitted from the interface
- Clocks
  - Data clock out (*ns_fwd_clk*), sent by the near side chiplet to the far side chiplet
  - Data clock in (*fs_fwd_clk*): received by the near side chiplet from the far side chiplet

The functions of other AIB Gen2 signals are performed by sideband control shift register as described in section 1.6.

An AIB-O channel shall have the signal counts as shown in Table 1.

Bump pitch (µm)	Range of data signals per channel (Increments)					
	TX			RX		
	Balanced	All-TX	All-RX	Balanced	All-TX	All-RX
≤110	10-20 (10)	10-40 (10)	0	10-20 (10)	0	10-40 (10)

Table 1. AIB-O Number of Data Signals per Channel

1.1.2 AIB-O to MAC Interface

An AIB-O PHY has the same interface to the MAC as described in the “MAC Interface” table of AIB 2.0..

1.1.3 AIB-O Reset

AIB-O shall use the same requirements as in the “Power-on Reset” section of the AIB 2.0 specification for *CONF_DONE, power_on_reset* and *device_detect* signals.

The AIB-O link controller of section 1.6 communicates the status between leader and follower for AIB-O per-channel reset, calibration and link ready.

1.2 AIB-O Electrical Specification

Signals (data, clock, and active control signals) shall meet the voltage and timing specifications provided in Table 2.

- Delays are specified in terms of *unit interval*, or *UI*. This refers to the minimum interval between data changes, and it is therefore a function of the clock frequency.
- The near-end timing specifications are for a 0.63pF capacitive load.
- The “trace” timing specifications in Table 2 reference a channel that has 2dB loss at 2GHz.
- Skew parameters are measured from the center of the eye.
- Jitter margin shall include all possible jitter contributors within the chiplet, including but not limited to reference clock jitter; intrinsic jitter contributed by any phase-locked loop, clock-data recovery, delay-lock loop, or the clock network; jitter caused by power-supply noise; and jitter caused by switching noise.

Symbol	Parameter	Near end	Trace	Far end
V_{EH}	Minimum difference between LO and HI (eye diagram height)			+/-100 mV
V_{OS}	Minimum output swing Typical output swing Maximum output swing	0.735 V 0.8 V 0.88V		
V_{CM}[1]	Common mode voltage	TBD		
t_{EW}	Minimum duration of valid output (eye diagram width) for data and forwarded clock			0.35 UI

1. V_{CM} tolerance includes all board level effects, with power supply variation (e.g. regulator) within 5%.

Table 2. AIB-O Electrical signal specifications

1.3 AIB-O Bump Configuration

The bump pattern for AIB-O is shown in Figure 1.

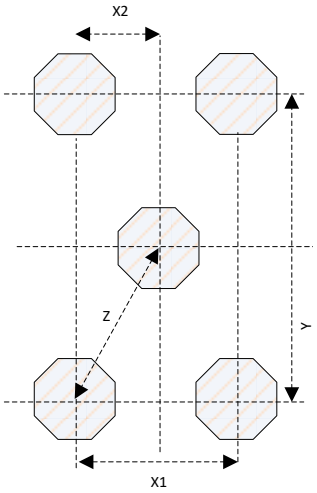

Figure 1. AIB-O Bump Spacing

The spacing of the bump array shall meet the Table 3 specifications. The X1 dimension may be reduced or expanded and may vary within the array. The Y dimension is parallel to the die edge. The AIB-O channel height shall be fixed at 312.48 µm, the same as AIB.

Symbol	Description	AIB-O
X1	Aligned-row bump-to-bump pitch	156.24u or ≥ minimum bump pitch such that Z minimum is met
X2	Staggered-row bump-to-bump pitch	X1÷2 (typical)
Z	Diagonal bump-to-bump pitch	≥ minimum bump pitch
Y	Aligned-column bump-to-bump pitch	156.24u

Table 3. AIB-O Bump Spacing Specifications

1.4 AIB-O Signal Bump Assignment

1.4.1 AIB-O Example Bump Table

Bump ID	Bump Name	IO
A1	TX_A	out
A3	TX_B	out
B2	TX_C	out
B4	TX_D	out
C1	TX_E	out
C3	GND	n/a
D2	TX_F	out
D4	TX_G	out
E1	TX_H	n/a
E3	VCCIO	n/a
F2	TX_I	out
F4	VCCIO	n/a
G1	TX_J	out
G3	ns_fwd_clk	out
H2	RX_I	in
H4	RX_J	in
I1	GND	n/a
I3	RX_H	in
J2	fx_fwd_clk	in
J4	RX_G	in
K1	RX_F	in
K3	VCCIO	n/a
L2	GND	n/a
L4	RX_E	in
M1	RX_C	in
M3	RX_D	in
N2	RX_A	in
N4	RX_B	in

Table 4. AIB-O Example Bump Table, 20 I/Os, Balanced

1.4.2 AIB-O Example Bump Map

	1	2	3	4
	Edge of Chiplet			
A	TX_A		TX_B	
B		TX_C		TX_D
C	TX_E		GND	
D		TX_F		TX_G
E	TX_H		VCCIO	
F		TX_I		VCCIO
G	TX_J		ns_fwd_clk	
H		RX_I		RX_J
I	GND		RX_H	
J		fs_fwd_clk		RX_G
K	RX_F		VCCIO	
L		GND		RX_E
M	RX_C		RX_D	
N		RX_A		RX_B

Figure 2. AIB-O Example Bump Map, 20 I/Os, Balanced

1.4.3 AIB-O Example Bump Names to Signal Mapping

AIB-O has a different assignment of RX and TX bits depending on the AIB-O interface orientation. Table 5 shows the assignment of TX and RX data bits to the bump names of **Error! Reference source not found.**.

TX			RX		
Data Bit	East Bump	West Bump	Data Bit	East Bump	West Bump
TX_0	TX_A	TX_B	RX_0	RX_A	RX_B
TX_1	TX_B	TX_A	RX_1	RX_B	RX_A
TX_2	TX_C	TX_D	RX_2	RX_C	RX_D
TX_3	TX_D	TX_C	RX_3	RX_D	RX_C
TX_4	TX_E	TX_E	RX_4	RX_E	RX_E
TX_5	TX_F	TX_G	RX_5	RX_F	RX_G
TX_6	TX_G	TX_F	RX_6	RX_G	RX_F
TX_7	TX_H	TX_J	RX_7	RX_H	RX_J
TX_8	TX_I	TX_I	RX_8	RX_I	RX_I
TX_9	TX_J	TX_H	RX_9	RX_J	RX_H

Table 5. AIB-O Bump Names to Signal Mapping

1.5 Gen2 Features Not in AIB-O

Redundancy is not supported by AIB-O. As AIB-O uses standard packaging technology instead of microbumps, redundancy is unnecessary.

Data Bus Inversion (DBI) is not supported by AIB-O.

1.6 AIB-O Link Control

Rather than defining the link control as split between leader and follower as in AIB 2.0, AIB-O requires a Link Controller function. The link controller may reside with the leader, the follower or at another location. Communication is required between the link controller and the leader AIB interface and between the link controller and follower AIB interface to control channel reset, calibration and transfer status for each channel.

1.6.1 AIB-O Link Registers

Each AIB interface shall provide for each channel a set of status registers as shown in Table 6 and a set of control registers as shown in Table 7, all accessible by the link controller.

Status Registers per Channel	Description
ns_mac_rdy	Same as the MAC interface input
ns_adapter_rstn[1]	Same as the MAC interface input
tx_dcc_cal_done[2]	Same as the sideband control signals of AIB 2.0 specification section 3.
rx_dll_lock[2]	Same as the sideband control signals of AIB 2.0 specification section 3.
rx_align_done	Same as the MAC interface output *m_rx_align_done*
ns_tx_transfer_en	Same as the MAC interface output *ms_tx_transfer_en* or *sl_tx_transfer_en*, whichever refers to the interface's near side TX

1. By convention only the follower sets this register HI.
2. Coming from the leader, these registers have the same definition as "ms_" + the signal name. Coming from the follower, these registers have the same definition as "sl_" + the signal name.

Table 6. AIB-O Link Status Registers

Control Register per Channel	Description
fs_adapter_rstn[1]	Same as the AIB interface signal
tx_dcc_dll_lock_req[2]	Same as the sideband control signals of AIB 2.0 specification section 3.
rx_dcc_dll_lock_req[2]	Same as the sideband control signals of AIB 2.0 specification section 3.
tx_wm_en	Enables word marking when HI. No word marking when LO.
rx_transfer_en[2]	Same as the sideband control signals of AIB 2.0 specification section 3.
fs_tx_transfer_en	Controls the MAC interface output *ms_tx_transfer_en* or *sl_tx_transfer_en*, whichever refers to the far side TX

1. By convention only the leader is controlled by this register.
2. Coming from the leader, these signals have the same definition as "ms_" + the signal name. Coming from the follower, these signals have the same definition as "sl_" + the signal name.

Table 7. AIB-O Link Control Signals

The link controller shall use the link status and link control registers to bring up the links between leader and follower channels.

1.6.2 AIB-O Link Reset

Figure 3 shows the reset actions by the link controller. Following these steps, the link controller proceeds to the link initialization steps of Figure 4.

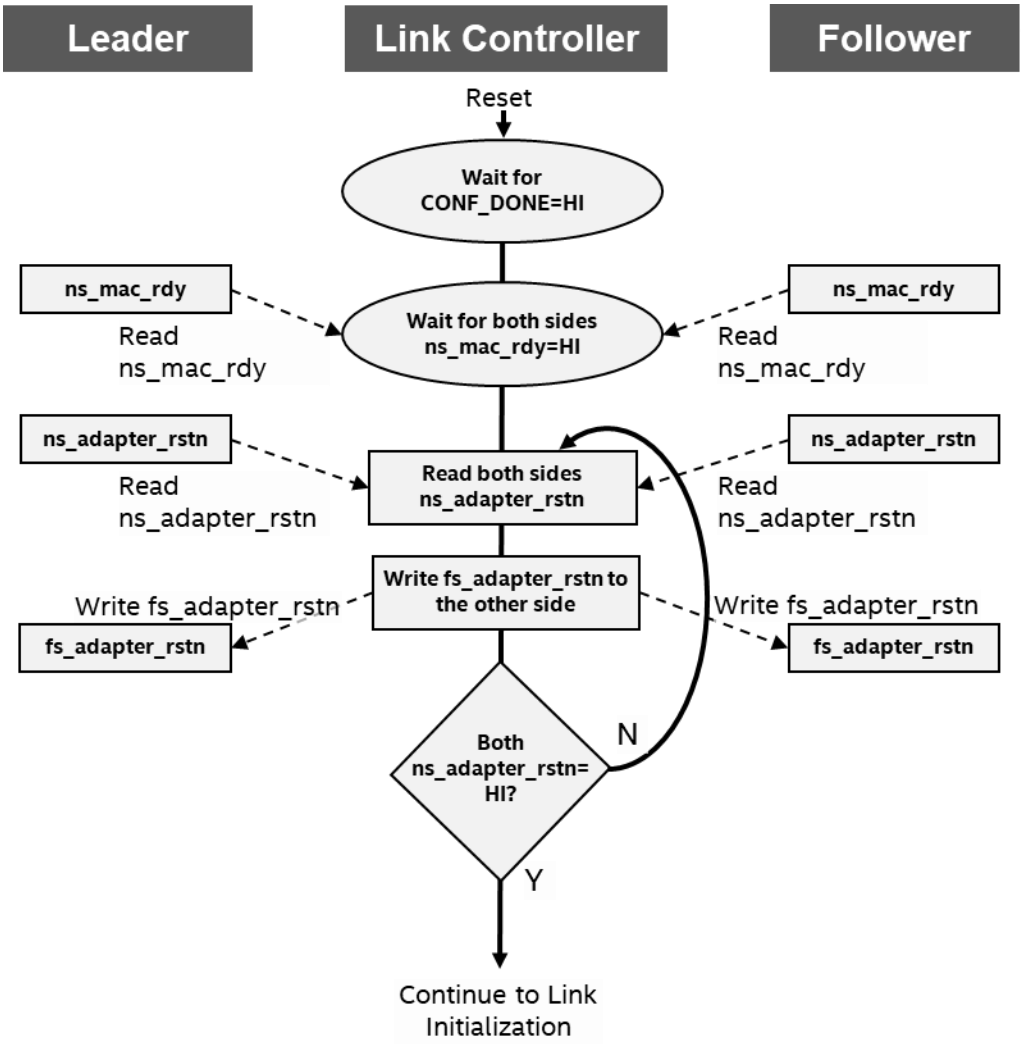

Figure 3. AIB-O Link Reset

At any point the link may be reset by setting ns_adapter_rstn LO, by convention on the follower side, and then by resetting the link controller.

1.6.3 AIB-O Link Initialization

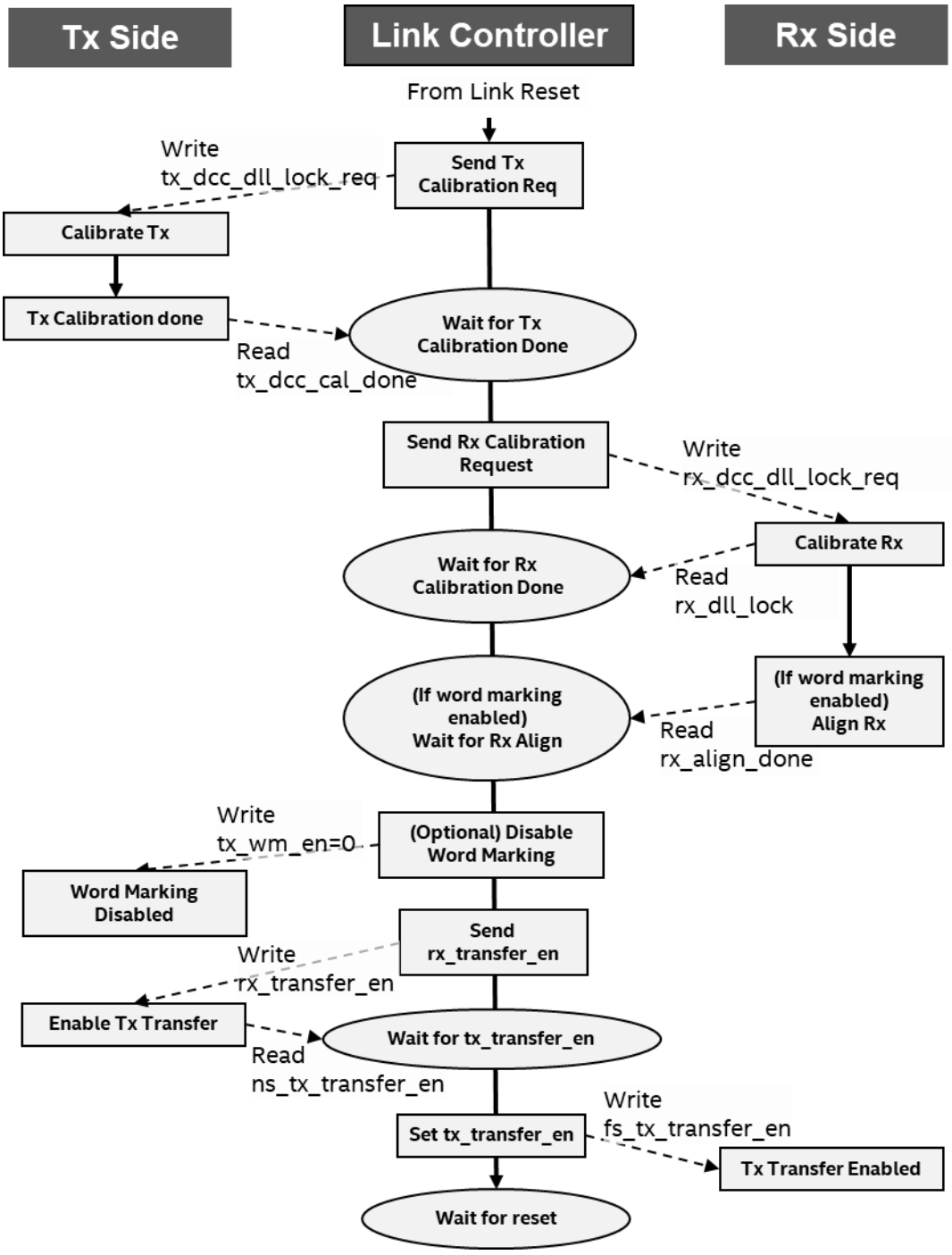

Figure 4. AIB-O Link Initialization

Figure 4 is the initialization for a simplex link, one Tx and one Rx. For a full duplex AIB link the link controller shall perform the link initialization in parallel for each direction.

The steps that indicate a wait require that the link controller repeatedly reads the indicated status register until its value is HI. After the register is HI the link controller

proceeds to the next step. For the steps that indicate a control register write the link controller shall set the control register HI.