Advanced Interface Bus for 3D (AIB-3D) Specification

2021.09.21

Revision 0.5

Revision History

Date	Version	Summary of Changes
09/21/21	0.5	Update based on working group review and complete 0.5 draft version

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Definition of Terms

This section defines phrases and acronyms that may not defined within the specification.

AIB	Advanced Interface Bus
DDR	Double data rate. Data is captured on both edges of the clock.
Far-side	AIB-3D interface being connected to by the chiplet designer
Follower	Follower shall be responsible for providing/receiving the clock signal from the Leader.
Leader	Leader shall be responsible for providing/receiving a clock signal
Near-side	AIB-3D interface being created by the chiplet designer
PHY	Physical layer. The bottom-most layer of the OSI reference model. It specifies electrical and basic signaling requirements.
RX	Receive. Applies to the inputs of a communications interface
SDR	Single data rate. Data is captured on one edge of the clock.
TX	Transmit. Applies to the outputs of a communications interface.
Weak Pull-up/down	An active or passive component connecting a signal to V_{DD}/ground to ensure that the signal, when not driven, will not float. The signal will be pulled to a HI/LO value. The term “weak” indicates that the pull-up/down component will pass limited current.

Introduction

This specification describes the three-dimensional (3D) extension to the Advanced Interconnect Bus (AIB) architecture known as *AIB-3D*. Herein are described the interconnect attributes, signal management, and the configuration interface required to design and build systems and peripherals that are compliant with the AIB-3D specification. The AIB-3D PHY is intended for interconnecting chiplets mounted within a package with signal distances of 1 millimeter (mm) or less in the vertical direction. The specification for AIB-3D leverages the AIB2.0 specification [1] as much as possible and where there is overlap with AIB2.0, the reader is referred to the AIB2.0 specification.

The specification is intended to provide interoperation between compliant chiplets that are interconnected in a 3D stack as shown in Figure 1. Choices made by the chiplet designer with respect to such elements as number and type of data signals, maximum supported clock speed, and any functionality that exceeds the minimum requirements established in the AIB-3D specification should be documented in the chiplet datasheet.

The initial version of the AIB-3D PHY specification focuses on interfaces between digital chiplets in a point-to-point connection using single data rate (SDR) mode. Future revisions of the AIB-3D PHY specification may consider options that include double data rate (DDR) mode and a 3D die-to-die (D2D) PHY interface that focuses on an interface using a wireless analog link: *AIB-3D Wireless*.

AIB-3D is a physical interconnect. Link, protocol, and application layers are implemented on top of the AIB-3D interface.

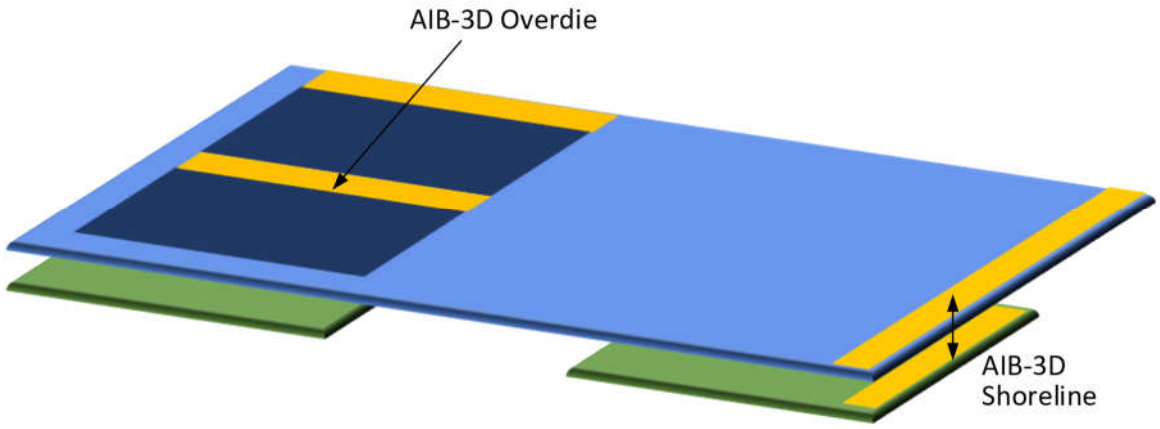

Figure 1. Chiplets interconnected in 3D stack using AIB-3D

1.1 Motivation

There has been a recent increase in the use of 3D integration outside of stacked memories, where recent publication show the increasing use of vertical integration of chiplets that are a mix of logic-on-logic or logic-on-memory. For example, the Intel Lakefield processor presented at ISSCC 2020 [2] is a logic-on-logic microprocessor platform that leverages vertical integration to obtain significant energy reduction. A 3D

integrated circuit (IC) uses stacked silicon wafers or dies that are interconnected using through-silicon vias (TSVs) or copper-to-copper connections. These 3D-integrated ICs are typically designed together by the same team or organization as the entire system is treated like a monolithic system. These systems have typically used simple or proprietary interfaces.

However, recently the industry has seen a rise in demand for creating a chiplet ecosystem in the vertical direction where IP providers would like to integrate 3rd party chiplets in a 3D stack to improve latency, increase bandwidth and/or save power. AIB1.0 and AIB2.0 are opensource die-to-die (D2D) PHY interfaces that enable high-performance interconnect, and they are used as a basis for the AIB-3D PHY D2D interface. The AIB-3D interface IP is considered a soft-macro that will be open-sourced as a combination of digital behavioral RTL models and analog/mixed-signal generators to allow ease of portability across process, different types of applications, and 3D integration solutions.

1.2 AIB-3D PHY Requirements

The new high-level requirements of the AIB-3D PHY interconnect are:

- Scalable across wide range of micro-bump and TSV pitch to allow the standard to be future-proof across pitch scaling.
- Single data rate to enable minimal circuit footprint
- Programmable half-duplex and full-duplex operation modes
- Programmable point-to-point or point-to-multipoint signaling
- Support for Logic-on-Logic or Logic-on-Memory die stacking
- Integrated DLL for clock phase alignment
- Scalable number of channels
- Lane repair for reliability
- Built-in test and pattern checker to enable automatic verification of connectivity
- Synthesizable or generator based soft-macro
- Non-intrusive power delivery
- Compatibility with AIB2.0 interface

Table 1 summarizes the features of AIB-3D.

1.3 Clarification on Requirements

This section clarifies some of the requirements listed that are specific to AIB-3D.

1.3.1 Non-intrusive Power Delivery

Non-intrusive power delivery requirement means that it is not expected that the designer of the Near-side AIB-3D PHY will accommodate power delivery to the Far-side AIB-3D and/or the Far-side chiplet. It is the responsibility of the designer of the Near-side and Far-side chiplets to accommodate power delivery without compromising the integrity of the AIB-3D patch or channel.

Requirement	AIB-3D
Data Rate per bump	**Minimum**: 1Mbps; **Typical**: 2Gbps – 3Gbps
Data transfer	Single Data Rate (SDR)
	Half-duplex and Full-Duplex
IO Voltage Output Swing	0.6V – 0.9V
Electrical and Timing	See Table 10 for Electrical Signal Specifications
Compatibility	AIB2.0

Table 1. AIB-3D Features

1.3.2 Half-Duplex Operation

Half-duplex operation requirement is added to the AIB-3D to support potential connection to Far-side chiplets or IPs on passive interposer and to access single-port memories on the Far-side chiplet. Far-side IPs or chiplets on passive interposer may also be accessed via the asynchronous interface (Section 1.5.4).

1.4 Compliance Summary

Table 2 summarizes the compliance points that shall be met in order to meet the AIB-3D requirements. Each of the compliance points is discussed in the specification. The table below will be completed after the AIB-3D specification is completed and reviewed.

Compliance Point	Required
Leader mode	✓
Follower mode	✓
Redundancy	
Bump assignment	✓
SDR	✓
Half Duplex modes	✓
Full Duplex modes	✓
Latency specification	✓
Data-transfer ready	✓

Compliance Point	Required
Conf_done	TBD

Table 2. AIB-3D Design Feature Summary

1.5 AIB-3D Architecture

The AIB-3D implements a physical-layer, or PHY, interconnect scheme, occupying Layer 1 on the OSI Reference Model, as shown in Figure 2.

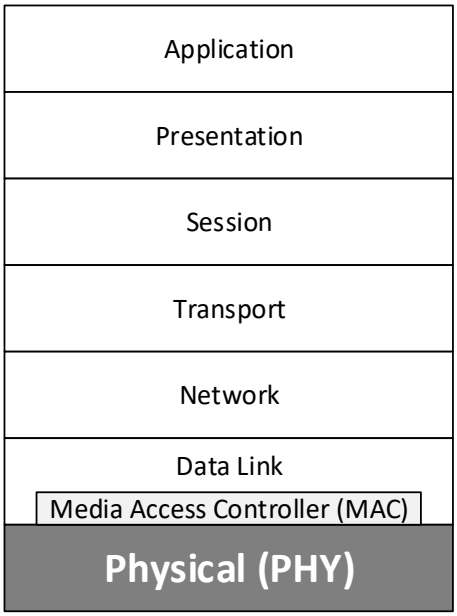

Figure 2. AIB-3D in the OSI Reference Model

1.5.1 AIB-3D Configurations

The initial release of AIB-3D focuses on only one configuration which is a simple interface employing SDR with a forwarded clock from the Leader and Follower AIB-3D interface which may be located either on the Near-side or Far-side. Depending the Leader or Follower designation of the AIB-3D channel, different channel configurations may be required. In future, DDR may be an additional configuration that is added to AIB-3D: AIB-3D DDR. A third option that may be added in the future is a wireless option: AIB-3D Wireless. Figure 3 below shows an example of Near-side as Leader and Far-side as Follower. It is also possible to configure the Near-side as Follower and Far-side as Leader.

1.5.1.1 AIB-3D SDR

There is no maximum data rate per signal specified for AIB-3D. In the interest of interoperability, minimum rates are specified in Table 3 along with typical rates to provide a range likely to be supported by multiple chiplets. The full range of operating data rates should be documented in the chiplet data sheet.

The AIB-3D SDR channel shall transfer the data using a single data rate (SDR) format. (Section 2.1.3.1). In a possible future DDR mode, AIB-3D shall transfer data using double data rate (DDR) format. In another future wireless mode, AIB-3D shall transfer data using a simple wireless chip-to-chip transfer protocol that will be determined at that the time of specification.

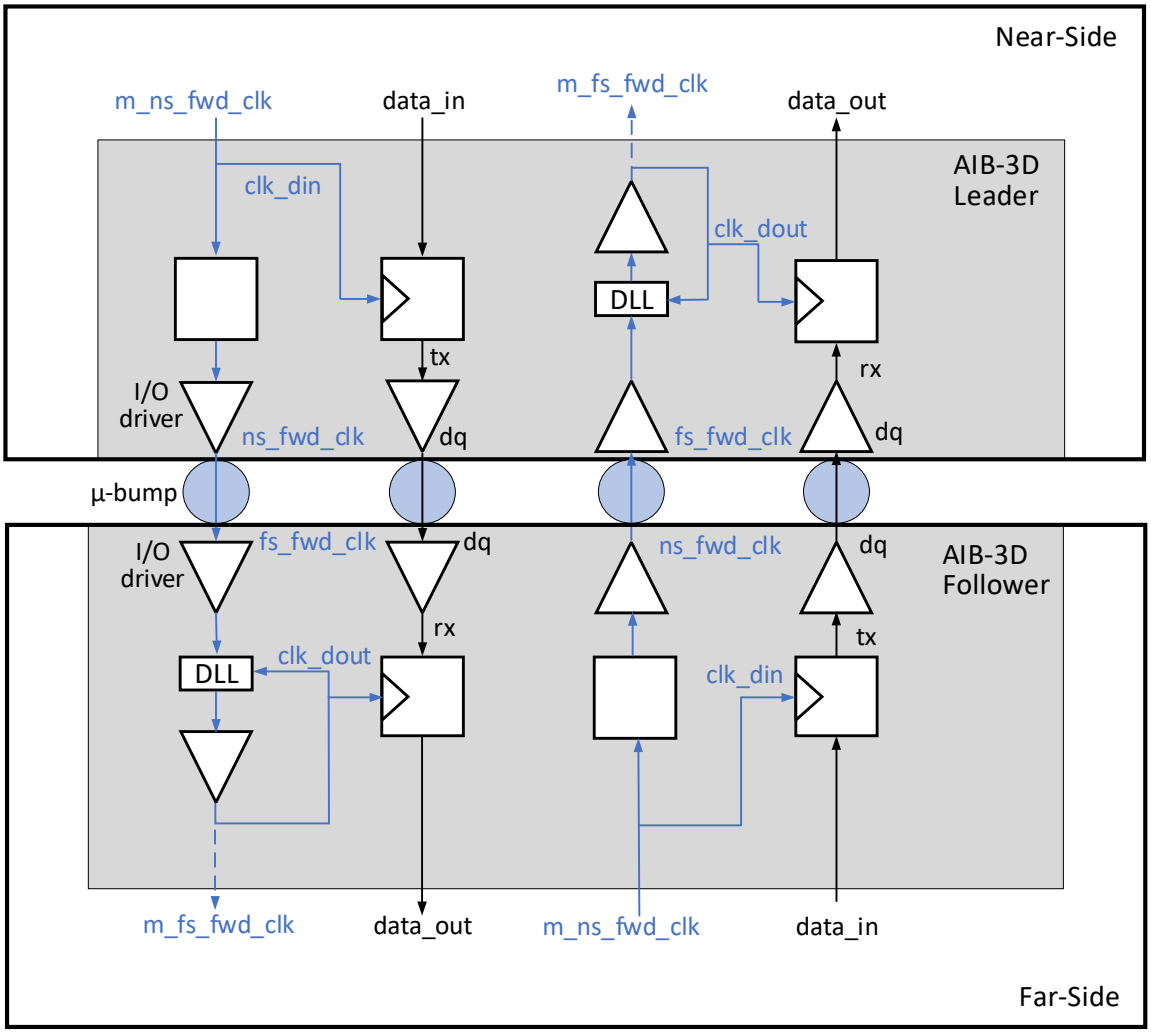

Figure 3. AIB-3D SDR Channel Configuration Example

Table 3. AIB-3D Data Rates

Data Format	Data Rates Supported Per Signal Bump
SDR	Minimum: 1Mbps; Typical: 2Gbps – 3Gpbs
DDR	TBD
Wireless	TBD

1.5.1.2 AIB-3D DDR

May be defined at a future time.

1.5.1.3 AIB-3D Wireless

May be defined at a future time.

1.5.2 Near-side and Far-side Interfaces

AIB-3D specifies an interface for one chiplet that can be connected to a compatible interface on a different chiplet that are both integrated vertically. An AIB-3D interface is one side of the connection. A chiplet designer may be creating only one of those AIB-3D interfaces; the AIB-3D interface to which it will connect is assumed to have been created by a different designer, putting it beyond the control of the designer.

In order to provide a clear distinction between behavior that the designer shall implement and behavior that the designer shall expect from the AIB-3D interface to which it will connect, the AIB-3D interface being created will be referred to as the Near-side interface. The AIB interface to which the Near-side interface will connect will be called the Far-side interface. Signal names that reflect the signal origin will be prefixed with *ns_* or *fs_* as shown in Table 4, similarly to AIB2.0. It is possible to include both AIB2.0 and AIB-3D in the same chiplet. Figure 3 provides an example of how AIB2.0 and AIB-3D may interact.

Table 4. Signal Prefix Naming Conventions

Signal Prefix	Purpose
*ns_*	**Near-side**: chiplet AIB-3D interface being created by designer
*fs_*	**Far-side**: chiplet AIB-3D interface created by a different designer that the Near-side interface will connect to

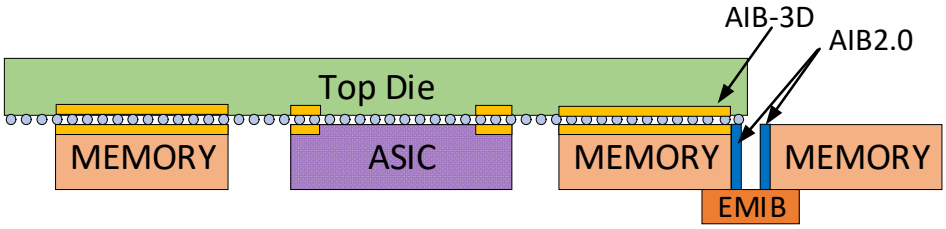

Figure 4. Example of AIB-3D usage with AIB2.0

In the example of Figure 5(a), Chiplet A is the subject chiplet under design and integrated as a base die. Chiplet A will eventually connect to Chiplet B, which is integrated as a top die, furthest from the package substrate. From the reference of Chiplet A, Chiplet A is the *Near-side* and Chiplet B is the *Far-side*. In the example of Figure 5(b), Chiplet D is

the subject chiplet under design and integrated as a top die. Chiplet D will eventually connect to Chiplet C which is integrated closest to the package substrate. From the reference of Chiplet D, Chiplet D is the *Near-side* and Chiplet C is the *Far-side*. The chiplet under design may be configured as either Leader or Follower.

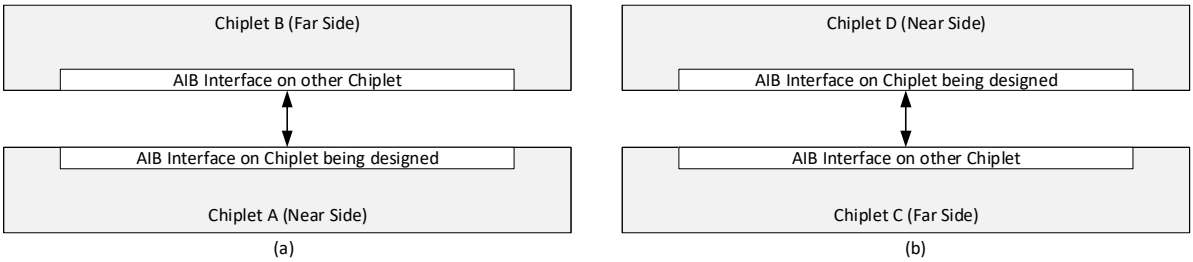

Figure 5. AIB-3D Configurations

1.5.3 Leader and Follower Interfaces

An AIB-3D interface pair has a Leader and a Follower. Leaders and Followers shall have specific roles during initialization and operation. Specifically:

- The Leader shall be responsible for providing/receiving a clock signal (Section 3.2.1)
- The Follower shall be responsible for providing/receiving a clock signal (Section 3.2.1)
- The Follower shall provide a *patch_detect* signal (Section 3.2.1).
- The Leader shall provide a *patch_reset* signal (Section 3.2.1).
- An AIB-3D interface configured as a Leader shall be designed to connect to a Follower; an AIB-3D interface configured as a Follower shall be designed to connect to a Leader.

The Leader/Follower property of an interface is independent of the Near-side/Far-side properties. A Near-side interface can be either a Leader or Follower, as can a Far-side interface.

An AIB-3D interface shall be configured as Leader or Follower by designing the interface as a Leader or Follower, referred to as a fixed interface.

Dual-mode interfaces are not presented in the first version of this specification and may be included in a later revision.

1.5.3.1 Fixed Interfaces

For fixed interfaces, the configuration of an interface as Leader or Follower shall be implemented by the chiplet designer and should be documented in the chiplet data sheet.

In the first version of the AIB-3D specification, point to multi-point connections are not supported. However, they may be enabled in future revision of the AIB-3D specification. A chiplet may contain one or more Leaders, one or more Followers, or a mixture of Leaders and Followers. In addition, a chiplet may also contain one or more 2.5D AIB

interfaces configured as a mix of Leaders and Followers. Figure 6 shows examples of the fixed Leader/Follower interfaces.

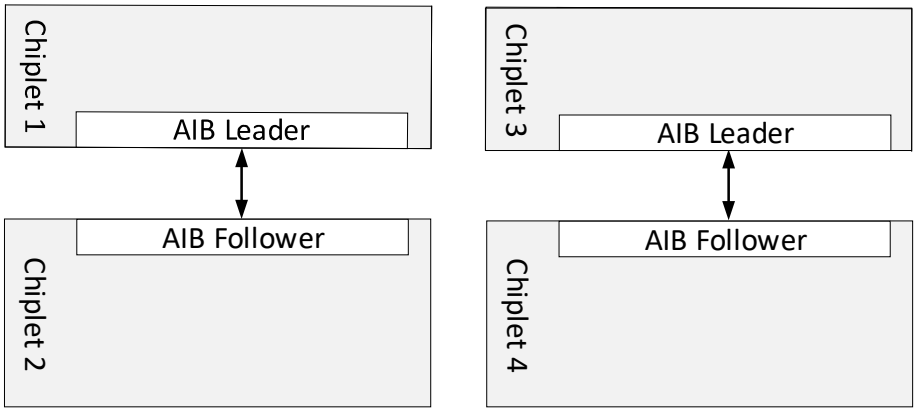

Figure 6. Fixed Leader and Follower Interfaces

1.5.3.2 Dual-mode Interfaces

May be defined in a later revision.

1.5.4 AIB-3D Interface

The AIB-3D interface defines three signal types, depicted in Figure 7:

- Data signals
  - Inputs (*RX*): data input signals received by the interface
  - Outputs (*TX*): data output signals transmitted from the interface
- Clock
  - Data clock out (*ns_fwd_clk*), sent by the Near-side chiplet to the Far-side chiplet. The clock is sent only from Leader chiplet.
  - Data clock in (*fs_fwd_clk*), received by the Near-side chiplet from the Far-side chiplet. The clock is sent only from Leader chiplet.
- Asynchronous
  - *patch_reset*: indicates whether a chiplet has completed power-on reset
  - *patch_detect*: used to verify presence of the Leader

MAC interfaces are not defined in the first version of the AIB-3D specification.

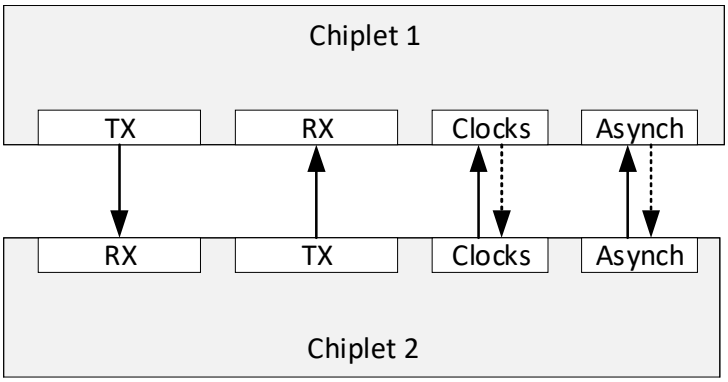

Figure 7. AIB-3D Signal Types

Two interconnected chiplets will have the same set of signals. Signals from the chiplet further away from the external I/Os or package substrate and nearest to the external I/Os or package substrate (Die 1) will be connected, such as *ns_fwd_clk* and *fs_fwd_clk*. Near-side signals should not be interconnected (e.g., *ns_fwd_clk* from one chiplet should not be connected to *ns_fwd_clk* from the other chiplet). Far-side signals should not be interconnected (e.g., *fs_fwd_clk* from one chiplet should not be connected to *fs_fwd_clk* from the other chiplet. This is indicated in Figure 8, but the crossed wires are for illustration only. Micro-bump locations (Section 6.3) ensure that connections will be straight lines. Table 5 summarizes the AIB-3D interface signals for a single channel.

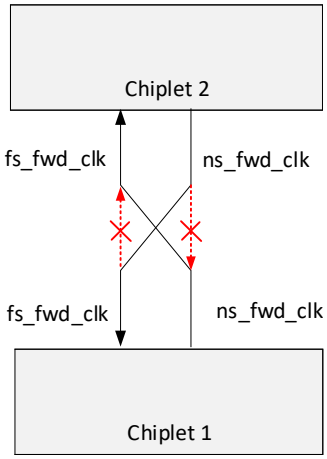

Figure 8. Interconnecting Far-side and Near-side Signals

Signal	Description	AIB-3D SDR	AIB-3D DDR	AIB-3D Wireless
TX	Synchronous data transmitted from the Near-side (Section 2.1.1)	✓	✓	✓
RX	Synchronous data received from the Far-side (Section 2.1.2)	✓	✓	✓
ns_fwd_clk /	Near-side transfer clock, forwarded	✓	✓	TBD

Signal	Description	AIB-3D SDR	AIB-3D DDR	AIB-3D Wireless
ns_fwd_clkb	from the Near-side to the Far-side for capturing received data (Section 2.1.6.3)			
fs_fwd_clk / fs_fwd_clkb	Far-side transfer clock, forwarded from the Far-side to the Near-side for capturing received data (Section 2.1.6.3)	✓	✓	TBD
m_ns_fwd_clk	Chiplet clock Near-side input for transmitting data from the Near-side to the Far-side	✓	✓	TBD
m_fs_fwd_clk	Chiplet clock Near-side output received from the Far-side and converted from quasi-differential to single-ended	✓	✓	TBD
fs_transfer_en	Far-side control signal to Near-side to indicate that transfer of data from Near-side can begin; Far-side is Follower	✓	TBD	TBD
ns_transfer_reset	Near-side transfer reset to indicate a new transfer is to start; Near-side is Leader.	✓	TBD	TBD
ns_transfer_en	Near-side control signal to Far-side to indicate that transfer of data from Far-side can begin; Near-side is Follower.	✓	TBD	TBD
fs_transfer_reset	Far-side transfer reset to indicate a new transfer is to start; Far-side is Leader.	✓	TBD	TBD
patch_detect	Used to verify presence of the Leader. Follower output to Leader.	✓	TBD	TBD
patch_reset	Control signal from Leader that is input to the Follower that indicates whether a chiplet has completed power-on reset.	✓	TBD	TBD

Table 5. AIB-3D Interface Signals in AIB-3D Channel

1.5.4.1 AIB-3D Channel

AIB-3D signals shall be grouped into AIB-3D channels. An AIB-3D channel is a two-dimensional array of data signals that do not exceed a limit determined by the micro-bump or TSV pitch of the chiplet. The chiplets being integrated together in a 3D stack must have the same micro-bump or TSV pitch and must be aligned vertically. The data signals may consist of half TX and half RX signals (i.e., "*balanced*" interface), all TX signals ("*all-TX*" interface) or all RX signals ("*all-RX*" interface). A conceptual depiction of a 512-bit AIB-3D channel using 25µm micro-bump pitch is shown in Figure 9.

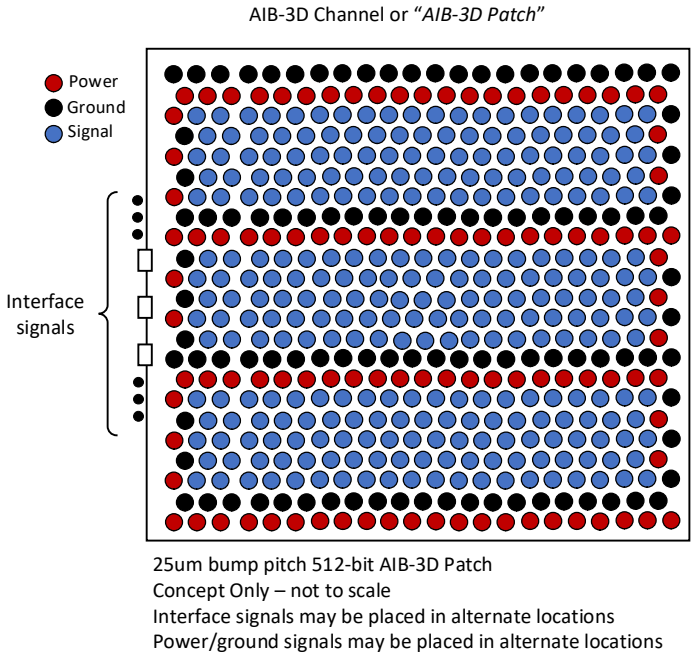

Figure 9. AIB-3D Channel Concept

An unbalanced interface where there are unequal number of TX and RX data signals is supported in AIB-3D. For example, there may be 128 TX data signals, and 384 RX data signals. This is achieved by configuring the data I/O direction in either TX or RX mode.

Micro-bump pitch (µm)	Range of data signals per channel (Increments)					
	TX			RX		
	Balanced	All-TX	All-RX	Balanced	All-TX	All-RX
25	16 – 256 (16)	16 – 512 (16)	0	16 – 256 (16)	0	16 – 512 (16)
10	16 – 512 (16)	16 – 1024 (16)	0	16 – 512 (16)	0	16 – 1024 (16)

Table 6. Number of Data Signals per Channel

1.5.4.2 AIB-3D Channel Array

AIB-3D channels shall be grouped into an AIB-3D array. The AIB-3D channels can be tiled horizontally and vertically. The grouped AIB-3D channels shall have the same configuration and the same number of data signals. AUX blocks are not supported in AIB-3D, however, the AUX signals such as *patch_detect* and *patch_reset* are incorporated as part of the control signals per AIB-3D channel. The number of channels maximally tiled horizontally and vertically are constrained by the chiplet clocking, available routing channels, power delivery network, and thermal considerations. It is possible to tile "*half-channels*". For example, if distributed memory die is placed under a logic die with available routing channels and the area is small enough to enable robust clock distribution without incurring high latency that would adversely affect the AIB-3D operation, then a configuration like the one shown in Figure 10 may be possible.

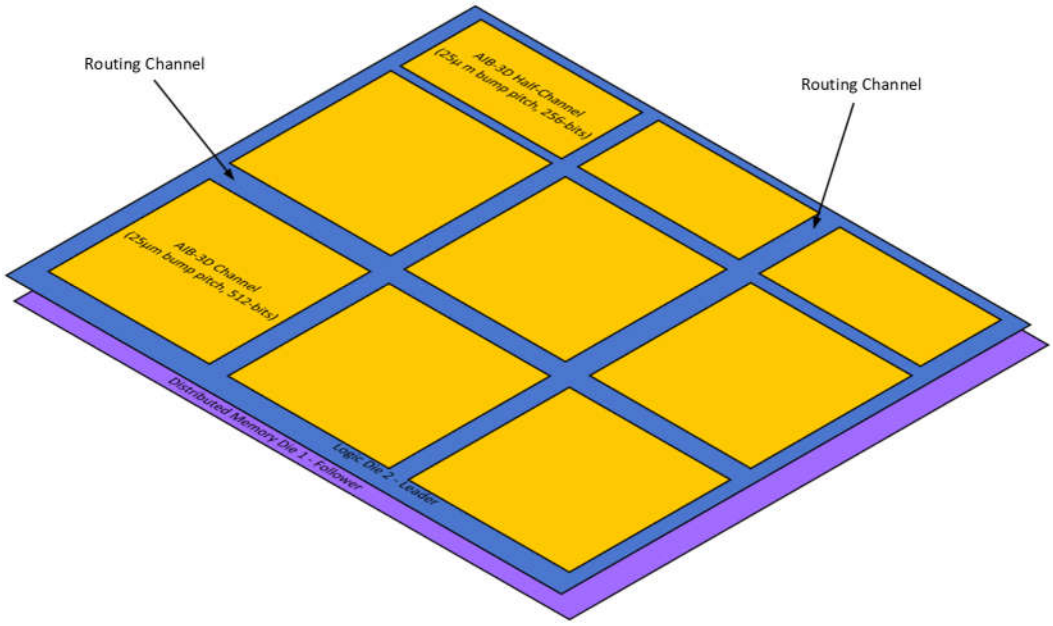

Figure 10. AIB-3D Channel Array: Tiling Example

1.5.4.3 AIB-3D data paths

Each data path within a channel shall be composed of an I/O block (Section 2.1), where data that is to be transmitted or received shall pass through an I/O block.

1.5.5 AIB-3D to MAC Interface

To be defined in a future revision.

1.5.6 AIB-3D to Application Interface

To be defined in a future revision.

2 Functional Specification

2.1 I/O Blocks

I/O blocks are divided into one of two types: *RX* or *TX*.

2.1.1 TX Block

A TX block shall register data before transmission. The transfer mode will be SDR as shown in Figure 11. Inputs to the I/O block shall be mapped according to Figure 12.

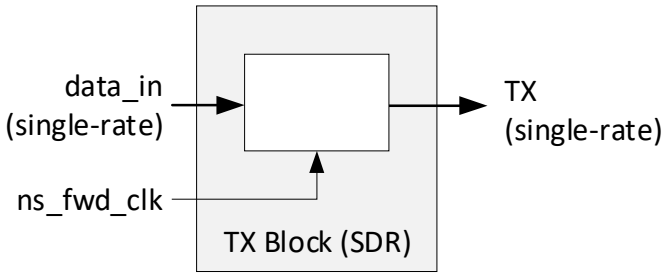

Figure 11. SDR TX Block

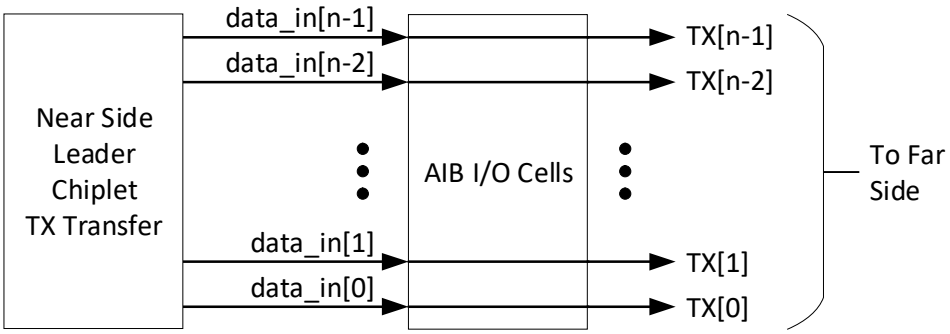

Figure 12. I/O Mapping: SDR Transmit

2.1.2 RX Block

An RX block shall register incoming data using the forwarded clock as shown in Figure 13. Outputs from the I/O block shall be mapped according to Figure 14.

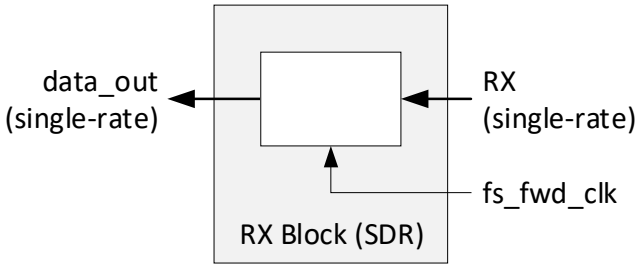

Figure 13. SDR RX Blocks

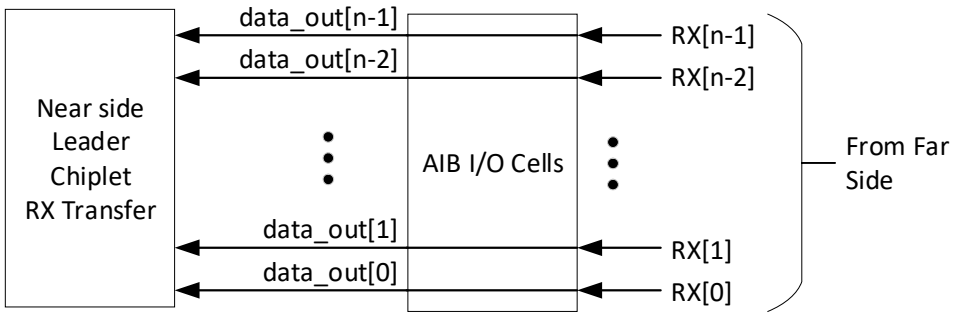

Figure 14. I/O Mapping: Receive

2.1.3 Data Exchange

AIB-3D data signals shall be exchanged as SDR.

All data signals within an AIB channel shall use the same data exchange format.

2.1.3.1 SDR Data Exchange

AIB-3D interfaces shall exchange data using a SDR relationship between the clock and data. Data shall be transmitted on the falling edge of the clock as shown in Figure 15.

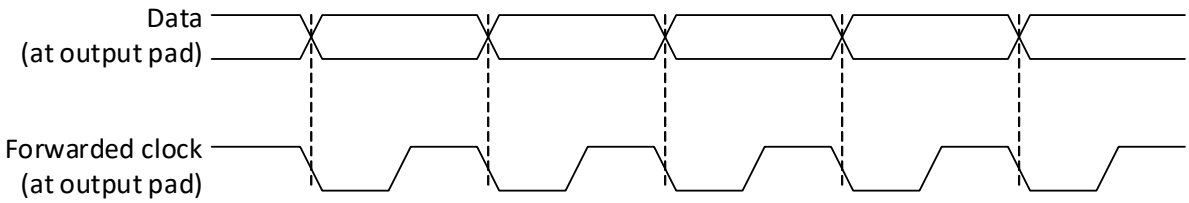

Figure 15. SDR Data/Clock Timing

Example timing diagram is shown in Figure 16 for the system depicted in Figure 3.

2.1.3.2 Signal Skew

Skew between data edges within a channel and between clock and data edges within a channel shall meet the following specification, where a unit interval (UI) is illustrated in Figure 17. Skew relationships are also illustrated in Figure 17. These relationships and specifications shall be met by TX signals *ns_fwd_clk*, and *ns_fwd_clkb*.

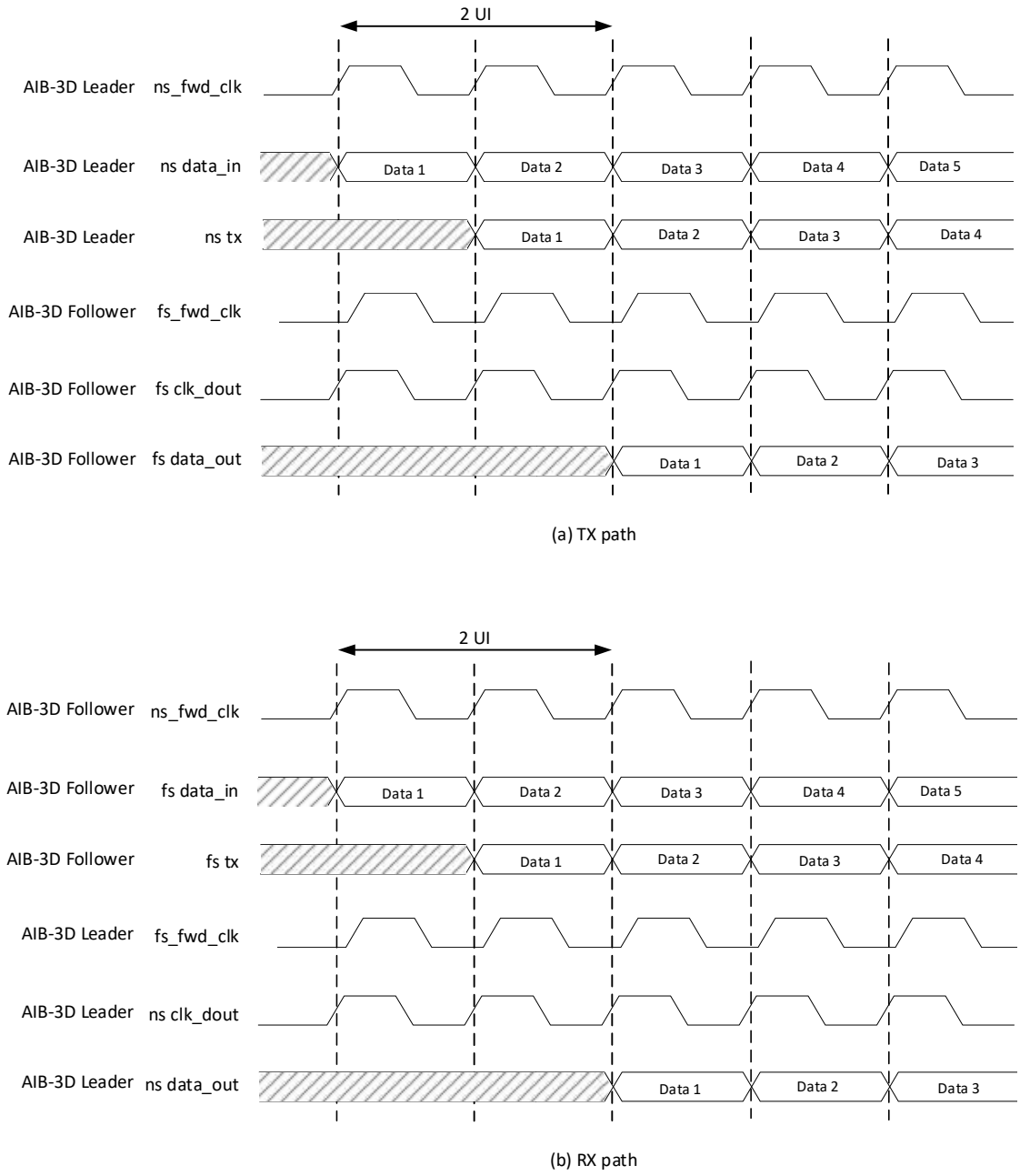

Figure 16. Example timing diagram for (a) forward and (b) return path

Symbol	Parameter	AIB-3D	
		Measured at Near-side output	Measured at Far-side input
t_{DS}	Maximum data-to-data skew	0.04UI	0.05UI
t_{DCS}	Maximum data-to-clock skew	0.02UI	0.025UI

Table 7. Skew Specifications

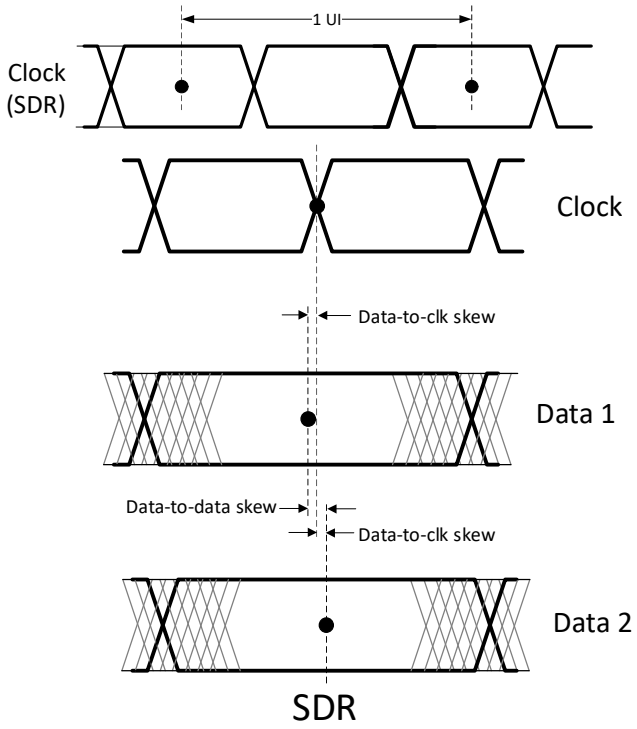

Figure 17. Unit Intervals for SDR Clocks and Skew Relationships

2.1.3.3 Half-Duplex and Full-Duplex Modes

In the initial version of the specification, focus will be on full-duplex mode. Half-duplex mode will be presented in a future revision. In full-duplex mode, balanced mode, 50% of the 512-bit AIB-3D channel will be configured as RX data (256-bits) and other 50% will be TX data (256-bit).

Half-duplex mode will enable 100% of the channel to be unidirectional, either TX or RX. The details of how this will be enabled will be provided in a future revision.

2.1.3.4 Balanced and Unbalanced Data Transfer

Balanced data transfer as shown in Table 6 shall configure 256-bits of the AIB-3D channel

or patch as TX data and the other 256-bits as RX data, as conceptualized in Figure 18. Unbalanced data transfer shall be enabled by allowing configuration of a 16-bit sub-patch to be either TX or RX. Details of how this will be enabled will be provided in a future revision. The unbalanced data transfer is conceptualized in Figure 19.

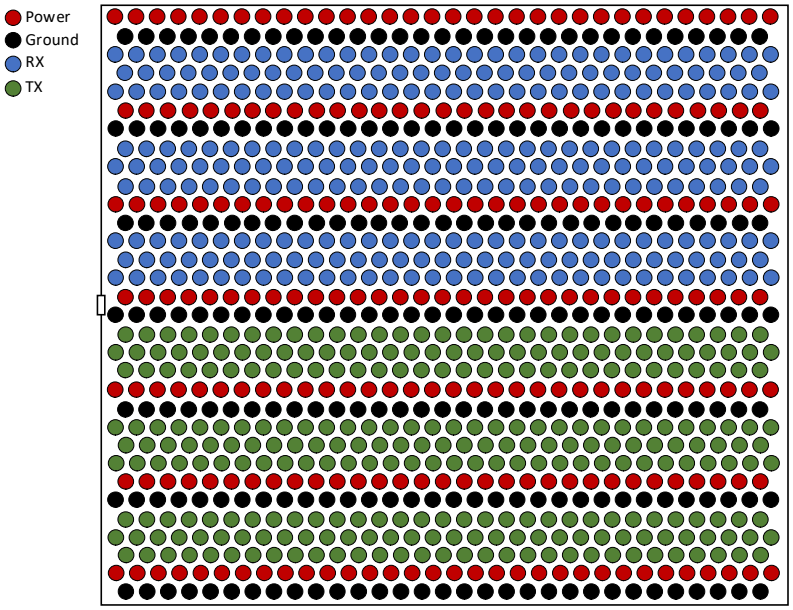

Figure 18. Balanced full-duplex data exchange concept

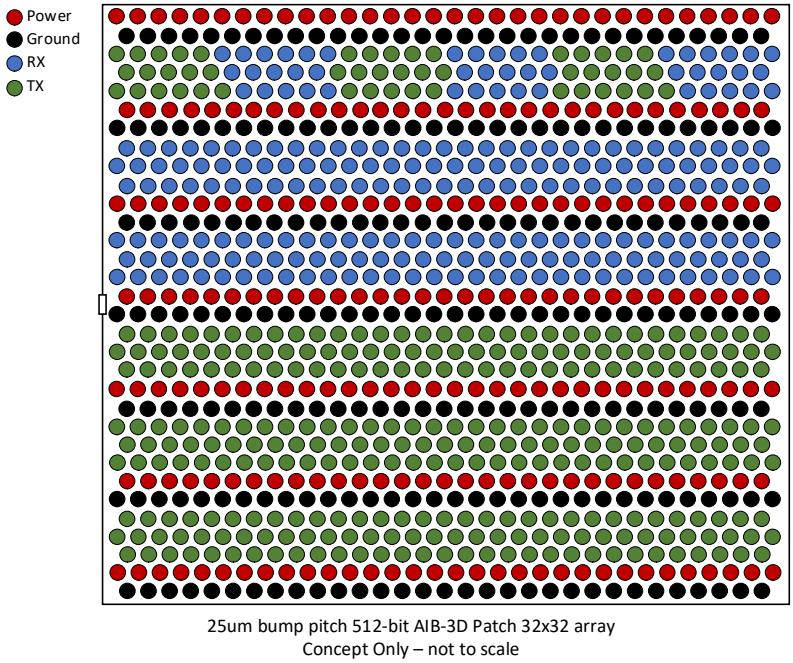

Figure 19. Unbalanced full-duplex data exchange concept

2.1.4 Tristate

All output signals shall be capable of being put into tristate.

2.1.5 Weak Pull-Up and Pull-Down

All inputs and outputs shall have an associated weak pull-up and weak pull-down with the equivalent driving strength of 10 – 20 kΩ. The inputs and outputs shall be configurable either with the pull-up, with the pull-down, or with neither the pull-up nor the pull-down. Data and clock signals that are put into standby require weak pull-up or pull-down.

2.1.6 Data-clock operation

2.1.6.1 Transmit Clock

The AIB-3D channel shall receive a transmit clock, *ns_fwd_clk* from the Near-side chiplet. That clock shall be used to transmit data and it shall be forwarded to the Far-side (Section 2.1.6.3).

2.1.6.2 Forwarded Transmit Clock

An AIB-3D channel shall forward its transmit clock to the Far-side. The clock signal shall be quasi-differential when moving from one chiplet to the other. The Near-side shall receive the forwarded clock, *fs_fwd_clk*, from the Far-side. Once converted from quasi-differential to single-ended, the clock can be made available to the chiplet.

It should be noted that in the case of AIB-3D, a choice is provided to the implementer to either use a forwarded clock from the Far-side to receive data on the Near-side or use the Near-side *ns_fwd_clk* to receive the data coming from the Far-side. The choice is based on design need. If the designer decides that there is a large amount of PVT variations between the two chiplets, then the designer may choose to use the *fs_fwd_clk* to receive the data from the Far-side. This may incur additional latency. A delay-locked loop (DLL) is recommended for phase correction before clocking the capture register if necessary, to ensure correct data sampling under all conditions of voltage and temperature (see Figure 3 and Figure 20).

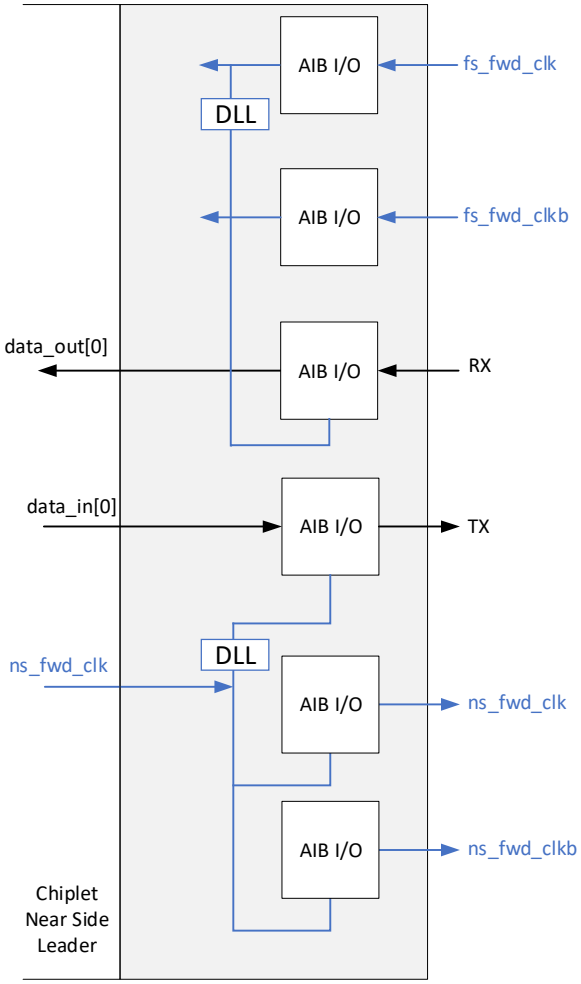

Figure 20. Forwarded Clock – Transmit and Receive

2.1.6.3 Clock Duty Cycle Requirements

The forwarded clock signal shall meet the following duty-cycle specification.

Symbol	Parameter		Top end
t_{FDCD}	Maximum forwarded-clock DCD	SDR	±10%
t_{RDCD}	Maximum receive-domain clock DCD	SDR	±10%

Table 8. Clock Duty-Cycle Requirements

2.1.7 Latency

Latency path	AIB-3D
Transmitting	1.5 – 2 CLK cycle (1.5 – 2 UI)
Receiving	1.5 – 2 CLK cycle (1.5 – 2 UI)

Table 9. Latency Specification

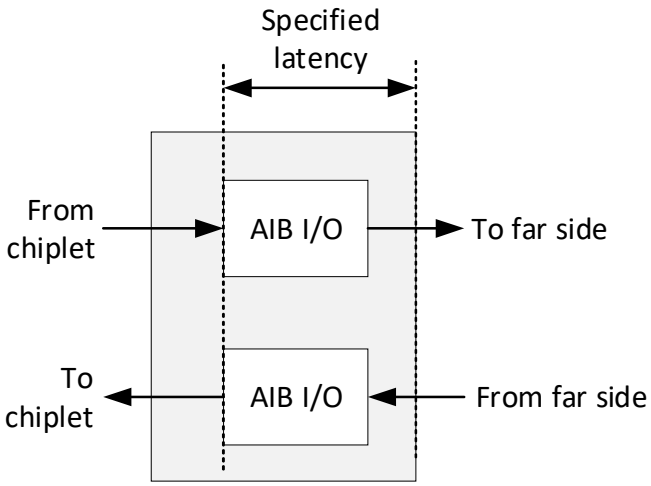

Figure 21. Latency Measurement

2.1.8 Asynchronous mode

I/O blocks that pass control signals from one chiplet to the other shall operate in asynchronous mode.

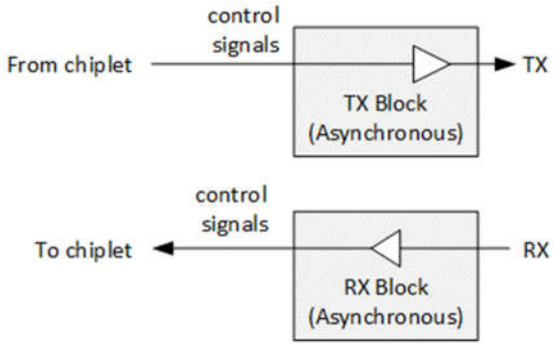

Figure 22. Asynchronous I/O Mode.

2.1.9 Mismatched Interfaces

The Near-side shall interoperate with a Far-side having a different number of I/Os than the Near-side provided:

- The two interfaces are of the same type
- The interfaces are aligned on the *spare* bumps.

If a Near-side interface is connected to a Far-side interface having fewer I/Os per channel than the top-side interface, then the unused I/Os in the Far-side interface shall be placed into standby mode. The Near-side chiplet should be able capable of handling the minimum number of I/Os in Table 6 within the larger full number of bits in the Near-side's AIB-3D to chiplet *data_in* and *data_out* signals. The Near-side chiplet should be configurable for operation with the minimum number of I/Os or with the chiplet's larger full number. Figure 23 shows the concept of a mismatched interface.

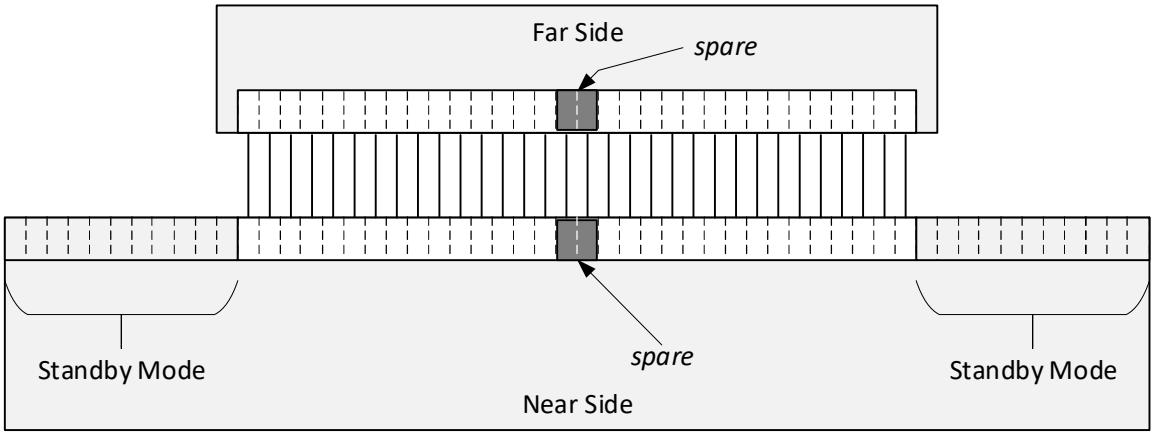

Figure 23. Mismatched Interfaces, One Channel

2.1.10 Unused Channels

Any unused channels shall have the same number of data signals as the used channels. The data signals in the unused channels shall be put into standby mode.

3 Reset and Initialization

3.1 Data-Transfer Ready

A data-transfer ready signal (*ns_transfer_en*, *fs_transfer_en*) shall be made available for control by the chiplet. The data-transfer ready signal may be de-asserted due to application-driven changes, including but not limited to:

- An intentional change in clock frequency
- Receipt of bad data

De-asserting the data-transfer ready signal may also be necessary due to conditions with the AIB-3D interface, which may include but are not limited to:

- Completion of configuration during power-up
- Initiation of reset by the Far-side
- Loss of DLL lock

Internal AIB-3D conditions indicating the need for de-assertion of the data-transfer ready signal shall be sent to the chiplet so the chiplet can de-assert the data-transfer ready

signal.

3.1.1 Standby Mode

A signal shall be placed into standby mode by one of the following means:

- Driving the signal LO
- Putting the signal into tristate and enabling the weak pull-down

During initialization, data outputs shall be placed into standby mode.

3.1.2 Data Transfer Ready Signals

Each AIB-3D channel or patch shall have an *ns_transfer_en* signal that is controlled by the Near-side chiplet. When the *ns_transfer_en* is asserted HI by the chiplet, it shall indicate that the Near-side is ready for calibration and data transfer. De-assertion of *ns_transfer_en* shall affect only its own channel; other channels my continue transmitting data.

3.1.3 Effects of De-asserting Data Transfer Ready Signals

While the *ns_transfer_en* is de-asserted:

- Data transmission shall halt
- Data outputs shall be placed into standby mode (Section 3.1.1)
- The clock output *ns_fwd_clk* shall go into standby mode
- The *ns_transfer_en* shall be sent to the Far-side interface to communicate that data transmission has been halted to allow the Far-side to be reset

The contents of the retiming registers shall be undefined following de-assertion of data-transfer ready. De-assertion of the data-transfer ready signal shall not affect the clock signals.

3.1.4 Data Transfer Reset

The data transfer is reset on Near-side and Far-side by asserting the *ns_transfer_reset* or *fs_transfer_reset* signals to reset the AIB-3D channel. All transfers are halted, and all input/output flops are reset. Data outputs are placed in standby mode and clock outputs are put into standby mode.

3.2 Initialization

Initialization will consist of two steps in sequence:

- Power-on reset synchronization
- Calibration

This is shown in Figure 24. If there are multiple AIB-3D interfaces on a single chiplet, they shall come out of configuration at the same time, but they may complete reset and calibration at different times depending on implementation.

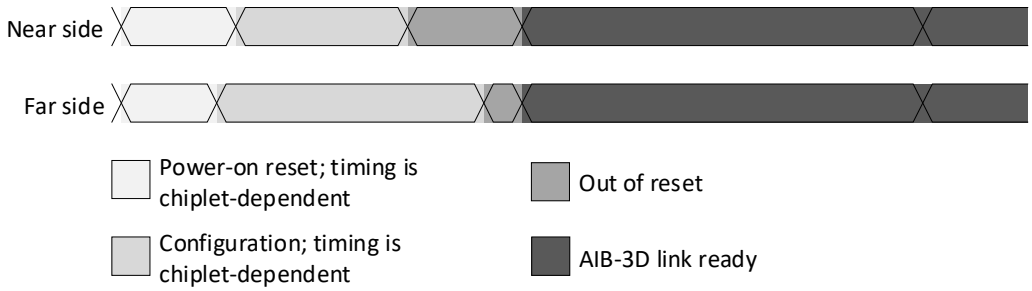

Figure 24. AIB-3D Initialization

3.2.1 Power-on Reset Synchronization

Power-on reset, being the first step in initialization, shall not require any features enabled by configuration (in the manner that the SDR option is configured, for example), since configuration will not occur until after power-on reset.

3.2.1.1 Power-on Reset Signals

Two signals shall participate in power-on reset: *patch_reset* and *patch_detect*. Their function shall depend on whether the interface is a Leader, a Follower, or dual-mode (Section 1.5.3.2).

For Leader interfaces:

- *patch_reset* shall be implemented as an input
- *patch_detect* shall be implemented as an output

For Follower interfaces:

- *patch_reset* shall be implemented as an output
- *patch_detect* shall be implemented as an input

Dual-mode interface operation will be defined in a future revision.

3.2.1.2 Power-on Reset Sequence

During power-on reset, all input and output signals shall be placed in standby mode (Section 3.1.1). The power-on reset sequence shall proceed as follows:

1. The Leader interface shall assert its *patch_detect* signal HI to indicate its presence to Follower interfaces on different chiplets. If no *patch_detect* signal is detected by the Follower, then the Follower may act to ensure that it is in a safe state.
2. Each chiplet shall implement its own power-on reset routine. At the beginning of the routing, Follower interfaces shall assert their *patch_reset* signals HI.
3. When a chiplet completes its power-on reset sequence:
    a. Leader interfaces shall begin the configuration stage.
    b. Follower interfaces shall de-assert their *patch_reset* signals LO and begin the configuration stage. The system designer should ensure that *patch_reset* from the Follower is not de-asserted before the Leader has completed its power-on reset routine.

Figure 25 shows the power-on reset synchronization.

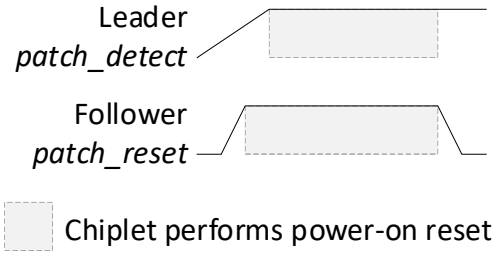

Figure 25. Power-on reset synchronization

3.2.1.3 Unused Interfaces

In order to ensure correct operation for chiplets with unused Leader interfaces, the *patch_reset* inputs for those unused interfaces shall have weak pull-ups.

In order to ensure correct operation for chiplets with unused Follower interfaces, the *patch_detect* inputs for those unused interfaces shall have weak pull-downs.

3.2.1.4 Test Provision

In order to test the power-on reset sequence at the wafer level, two signals shall be provided for use by automated test equipment to override the *patch_reset* and *patch_detect* signals when there is no Leader/Follower pair available. *patch_reset_ovrd* overrides the *patch_reset signal*, and *patch_detect_ovrd* overrides the *device_detect* signal. Figure 26 shows how each override is used when the chiplet is not connected as a pair.

The signal *dual_mode_select* = LO is a Follower interface and *dual_mode_select* = HI is a Leader interface. A fixed Leader or Follower interface may implement *patch_reset* and *patch_detect* as input only and output only according to the Leader and Follower requirements.

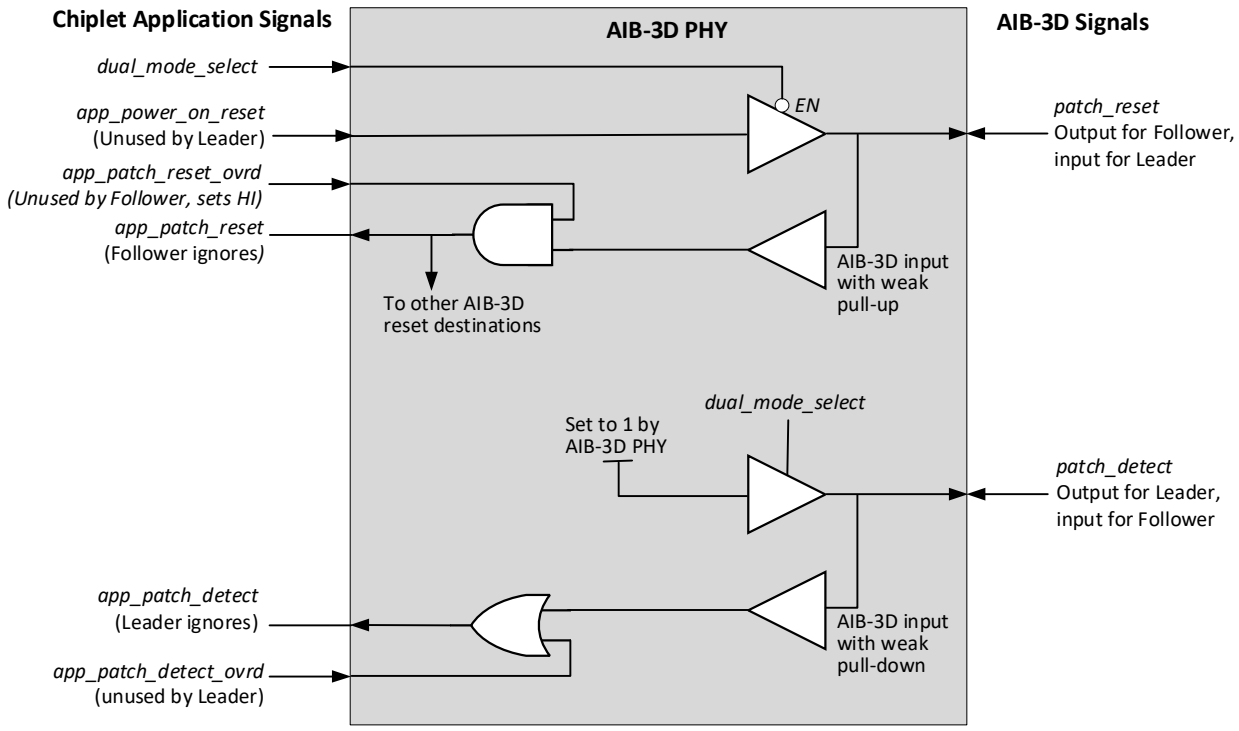

Figure 26. Patch reset and patch detect test provision

3.2.1.5 Reset Summary

To be summarized in a future revision.

3.2.2 Configuration

Configuration may include:

- Host chiplet configuration
- AIB-3D interface configuration
- AIB-3D redundancy activation

The clock input should be stable prior to assertion of *ns_transfer_en*.

3.2.2.1 Output State During Configuration

All outputs, including data outputs, and reset outputs shall be in standby mode during configuration. The reset outputs must come out of standby mode upon completion of configuration.

3.2.2.2 Chiplet Configuration

Configuration of any non-AIB-3D aspects of the chiplet is outside the scope of this specification.

3.2.2.3 AIB-3D Interface Configuration

To be completed in next revision.

3.2.2.3.1 Power-up Configuration

To be completed in next revision.

3.2.2.3.2 Configuration Completion Signals

To be completed in next revision.

3.2.2.3.3 DLL Calibration

To be completed in next revision.

3.2.3 AIB-3D Link Ready

To be completed in next revision.

3.3 Redundancy

To be completed in next revision.

4 Electrical Specification

To be completed in the next revision.

4.1 Eye Diagram

Compliance of data and clock signals shall be verified using a compliance mask on an eye diagram that specifies the minimum voltage swing (HI – LO), the minimum duration during which the output voltage will be stable, and the maximum allowed over- and undershoot.

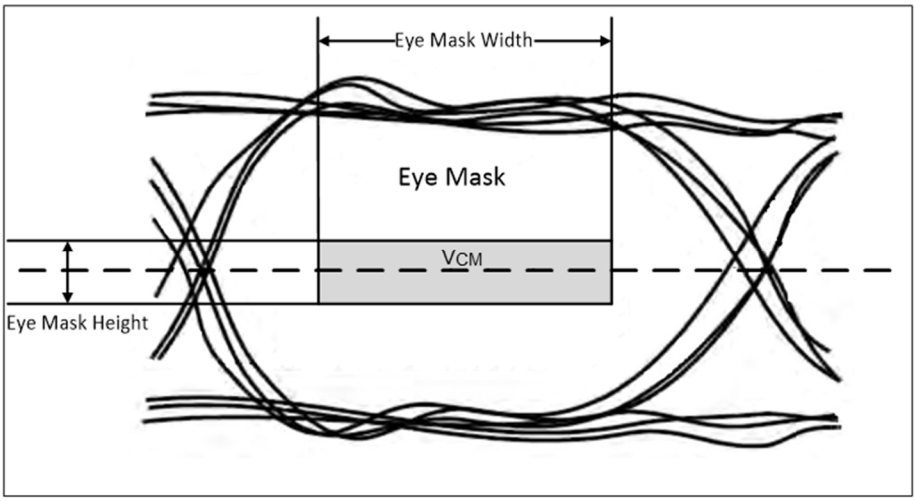

Figure 27. Compliance Eye Mask

Compliance is measured both at output bumps and at input bumps. It is applicable to both DDR/SDR modes for data, clocks, or active control signals. The connection between the near end and the far end is referred to as the *trace*.

Signals (data, clock, and active control signals) shall meet the voltage and timing specifications provided in Table 10.

- Delays are specified in terms of *unit interval*, or *UI*. This refers to the minimum interval between data changes, and it is therefore a function of the clock frequency.
- 25µm bumps are considered medium to high density.
- The “trace” timing specifications in Table 10 reference a channel that has 2dB loss at 2GHz.
- Skew parameters are measured from the center of the eye.
- Jitter margin shall include all possible jitter contributors within the chiplet, including but not limited to reference clock jitter; intrinsic jitter contributed by any phase-locked loop, clock-data recovery, delay-lock loop, or the clock network; jitter caused by power-supply noise; and jitter caused by switching noise.

Symbol	Parameter	AIB-3D		
		Near end	Trace	Far end
V_{EH}	Minimum difference between LO and HI (eye diagram height)			TBD
V_{HI}	Minimum output voltage for HI state	0.6 V		
V_{LO}	Maximum output voltage for LO state	0 V		
V_{OS}	Typical output swing	0.9 V		
V_{CM}	Common mode voltage	V_{OS} / 2		
t_{EW}	Minimum duration of valid output (eye diagram width) for data and forwarded clock	TBD UI	TBD UI	TBD UI
t_{BEW}	Minimum duration of valid output (eye diagram width) for receive-domain clock	TBD UI	TBD UI	TBD UI

1. V_{CM} tolerance includes all board level effects, with power supply variation (e.g., regulator) within 5%.

Table 10. Electrical signal specifications

4.2 Overshoot and Undershoot

Signal overshoot and undershoot at the receiver shall meet the specification in Table 11, where the symbols are illustrated in Figure 28.

Symbol	Parameter	Level	Units
V_{OA}	Maximum peak overshoot amplitude	TBD*Vos	V
V_{UA}	Maximum peak undershoot amplitude	TBD*Vos	V
T_{OD}	Maximum overshoot duration	TBD	ns
T_{UD}	Maximum undershoot duration	TBD	ns

Table 11. Overshoot and Undershoot Specifications

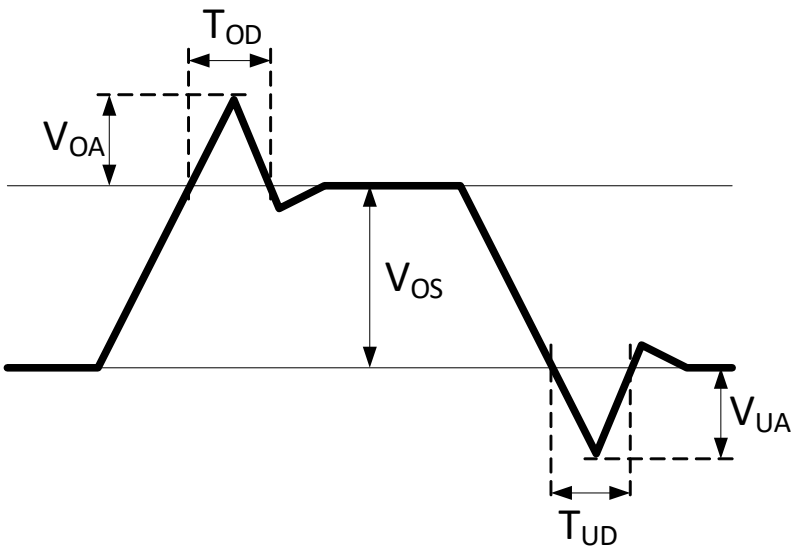

Figure 28. Overshoot and Undershoot at the Receiver

4.3 Electrostatic Discharge (ESD) Protection

AIB-3D IOs shall meet the ESD specifications in Table 12.

Parameter	Minimum
Discharge voltage (CDM)	TBD
Discharge current	TBD

Table 12. ESD Specifications

5 Design for Test

To be completed in the next revision and will leverage IEEE 1838 standard [3] as much as possible.

5.1 Automatic AIB-3D Patch Detection

5.2 Loopback

The AIB-3D interface shall have a Near-side and Far-side data loopback modes usable for test. The nature of the loopback behavior will be defined in the next revision of this specification.

6 Physical Signal Arrangement

To be completed in next revision.

6.1 Interface Orientation

6.2 Bump Configuration

6.3 Bump Assignment Process

6.4 Channel-Number Semantics

6.5 Alternate Bump Maps

7 References

[1] AIB2.0 Specification

[2] W. Gomes, et al., ISSCC 2020

[3] IEEE 1838 Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits, 2019

8 Appendices

To be used in future revision.