UCIe and AIB Interoperability Guide

8/2022

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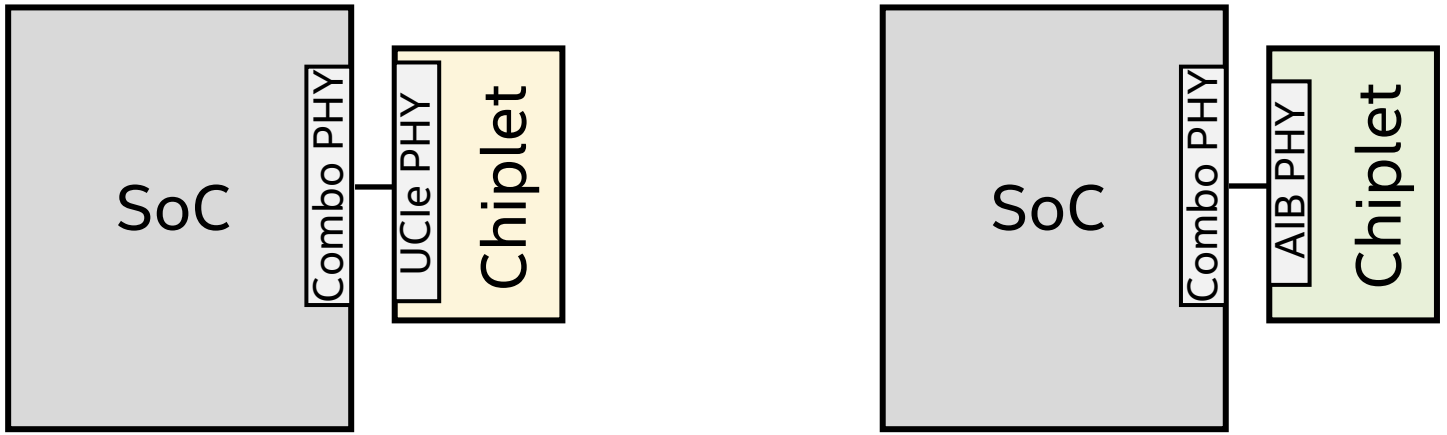
Interoperability Guide Outline

- Scope
- Physical Layer
  - AIB to UCIe ComboPHY Signal Connection
  - Electrical
  - Clocking
  - Data Format
- AIB Adapter
  - AIB Adapter and AIB Sideband
- Other AIB Requirements

Scope of This Guide

- This guide describes requirements of a ComboPHY for interoperating with a UCIe Advanced Packaging PHY or an AIB PHY.
- A ComboPHY uses Advanced Packaging consistent with AIB 1.0, AIB 2.0 and UCIe specifications.
- This guide is not a design specification. It does not describe how to build a ComboPHY or how to build advanced packaging to connect PHYs. The intent is to outline technical areas to consider when designing for UCIe and AIB interoperability.



Combo PHY provides SoC to UCIe chiplet operation, and SoC to AIB chiplet operation

Physical Layer

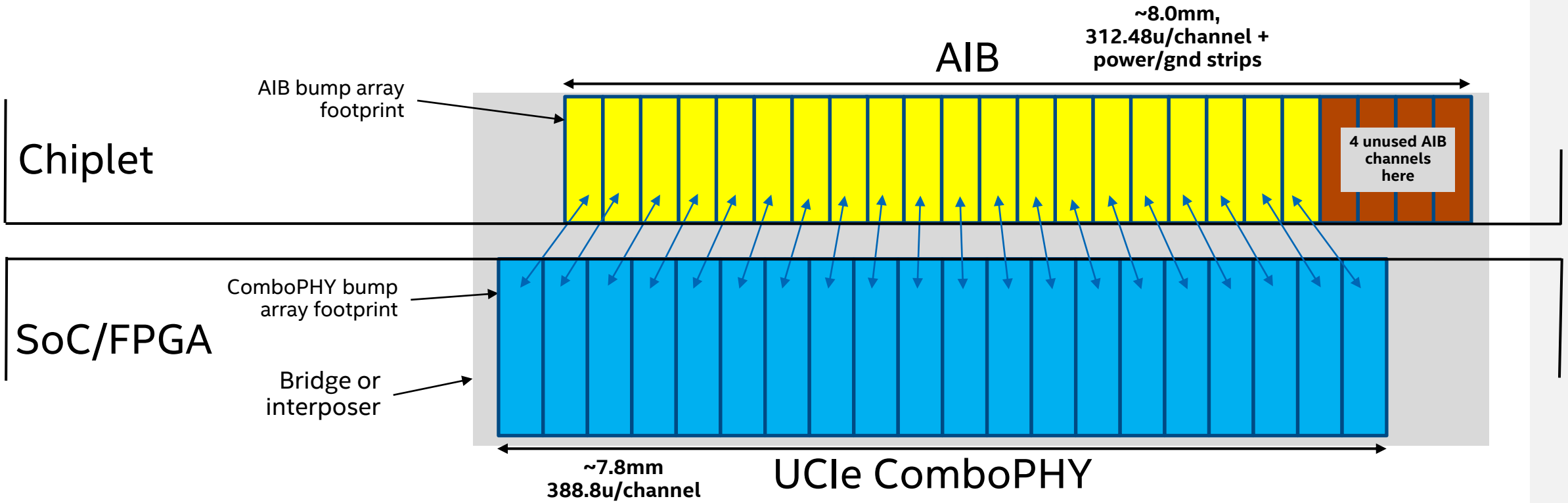
AIB to ComboPHY Signal Connections

- Refer to *Universal Chiplet Interconnect Express (UCIe) Specification Revision 1.0*, Appendix C, and *Advanced Interface Bus (AIB) Specification Revision 2.0.3*.
- ComboPHY shall support AIB Follower mode. Chiplet must use AIB Leader mode.
- ns_rcv_clk/b from the chiplet are not connected to the ComboPHY
  - The application must supply the ComboPHY with MAC to PHY clocks m_ns_fwd_clk, m_wr_clk and m_rd_clk that use a common reference as the AIB chiplet's ns_fwd_clk/b (0 PPM difference)
- AIB chiplet must observe the convention that the SoC/FPGA controls reset through fs_adapter_rstn to the chiplet
  - Generally observed by AIB chiplets that interface to an FPGA
- AIB chiplet must be able to set weak pulldowns on fs_rcv_clk/n
- AIB 1.0 Legacy "div2" clocks are not connected
- ComboPHY shall be able to avoid floating inputs on pins not used

Chiplet AIB Name	Connects to SoC UCIe Name	In to ComboPHY or Out	Note
RX[n]	TXDATA[n]	Out	For an AIB 2.0 Gen1 chiplet or AIB 1.0 chiplet, n ranges 0-19. For an AIB 2.0 Gen2 chiplet, n ranges from 0-39.
fs_sr_clk	TXDATA[40]	Out	Asynchronous at ComboPHY I/O, used as clock at ComboPHY AIB adapter
fs_sr_clkb	TXDATA[41]	Out	Asynchronous at ComboPHY I/O, used as clock at ComboPHY AIB adapter
fs_sr_data	TXDATA[42]	Out	Asynchronous at ComboPHY I/O, clocked by fs_sr_clk/b at ComboPHY AIB adapter
fs_sr_load	TXDATA[43]	Out	Asynchronous at ComboPHY I/O, clocked by fs_sr_clk/b at ComboPHY AIB adapter
fs_mac_rdy	TXDATA[44]	Out	Asynchronous at ComboPHY I/O
fs_adapter_rstn	TXDATA[45]	Out	Asynchronous at ComboPHY I/O
fs_rcv_clk	No connect	Out	AIB PHY to set to standby
fs_rcv_clkb	No connect	Out	AIB PHY to set to standby
fs_fwd_clk	TXCKN	Out	
fs_fwd_clkb	TXCKP	Out	
ns_fwd_clk	RXCKN	In	
ns_fwd_clkb	RXCKP	In	
TX[n]	RXDATA[n]	In	For an AIB 2.0 Gen1 chiplet or AIB 1.0 chiplet, n ranges 0-19. For an AIB 2.0 Gen2 chiplet, n ranges from 0-39.
ns_sr_clk	RXDATA[40]	In	Asynchronous at ComboPHY I/O, sourced as clock from ComboPHY AIB adapter
ns_sr_clkb	RXDATA[41]	In	Asynchronous at ComboPHY I/O, sourced as clock from ComboPHY AIB adapter
ns_sr_data	RXDATA[42]	In	Asynchronous at ComboPHY I/O, clocked by ns_sr_clk in ComboPHY AIB adapter
ns_sr_load	RXDATA[43]	In	Asynchronous at ComboPHY I/O, clocked by ns_sr_clk in ComboPHY AIB adapter
ns_mac_rdy	RXDATA[44]	In	Asynchronous at ComboPHY I/O
ns_adapter_rstn	No connect	In	AIB PHY to set to standby
ns_rcv_clk	No connect	In	AIB PHY to set to standby
ns_rcv_clkb	No connect	In	AIB PHY to set to standby
spare[0]	No connect	In/Out	AIB PHY to set to standby
spare[1]	No connect	In/Out	AIB PHY to set to standby

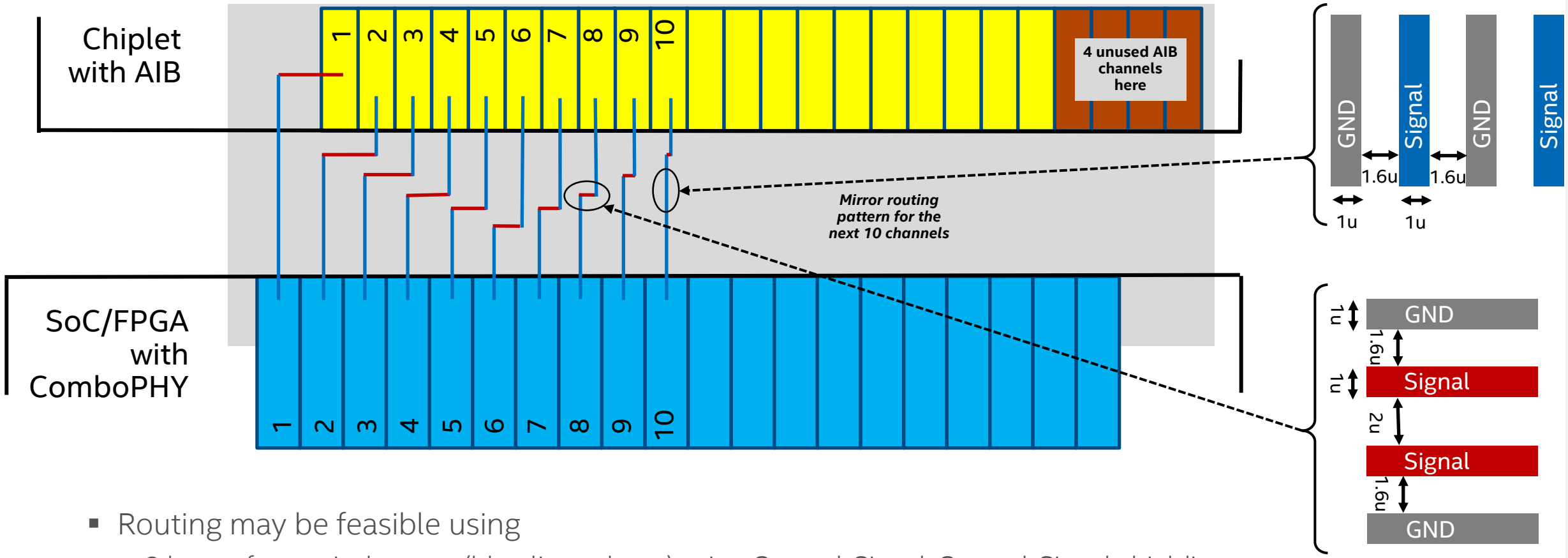
96 signal connections (to AIB 2.0 Gen2), 56 signal connections (to AIB 1.0 Legacy)

Example UCIe to AIB Interface: Bump Array Connections



- The example assumes that AIB chiplet can function with no more than 20 AIB channels
  - This guide anticipates that the maximum UCIe ComboPHY interface will be 20 UCIe channels
- Bridge or interposer routing must deal with the AIB and UCIe channel size mismatch (see following)

Example UCIe to AIB Interface: Bump Array Connections



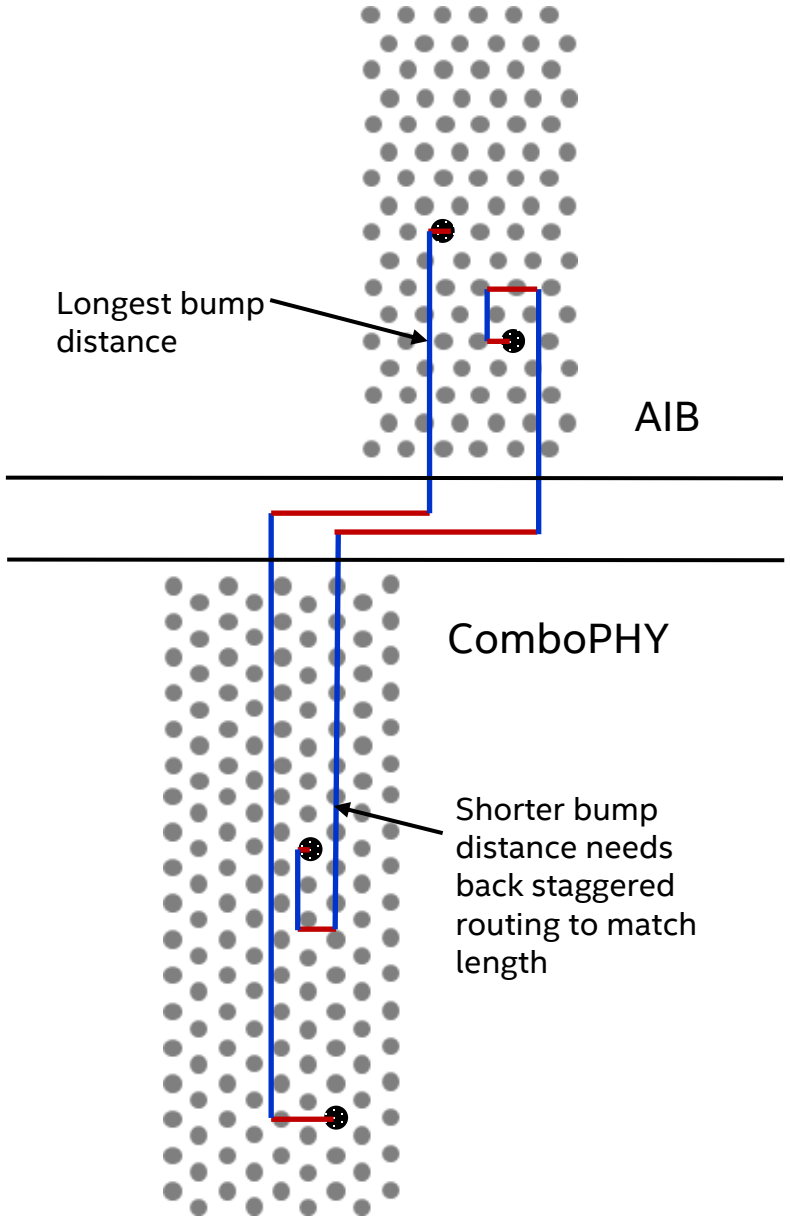
- Routing may be feasible using
  - 2 layers for vertical routes (blue lines above) using Ground-Signal-Ground-Signal shielding
  - 3 layers for horizontal routes (red jog lines above) using Ground-Signal-Signal-Ground shielding
- Target chiplet to FPGA microbump spacing (die-to-die spacing) of this example: 480u
- Target maximum trace length of this example: 3mm

Example UCIe to AIB Interface: Bump Array Connections

Symbol	Parameter	Gen1		Gen2	
		Measured at near-side output	Measured at far-side input	Measured at near-side output	Measured at far-side input
t_{DS}	Maximum data-to-data skew	0.04 UI	0.06 UI	0.04 UI	0.05 UI
t_{DCS}	Maximum data-to-clock skew	0.02 UI	0.03 UI	0.02 UI	0.025 UI

Table 9. Skew Specifications *Source: AIB Specification*

- Within a channel one must meet AIB skew requirements
  - Route length mismatch of signals is one component of skew
- Since the bump map for AIB does not match the bump map for UCIe, one strategy is to use "back staggered" routing to match lengths



ComboPHY Electrical Requirements

- The ComboPHY shall meet both AIB and UCIe Advanced Packaging electrical specifications with exception as noted following
- Only one mode (AIB or UCIe) is required to be supported by the ComboPHY in a specific MCP implementation
- The following table is an example of specifications that a ComboPHY may implement
  - The design point selected for this example is at 8Gbps UCIe, 4Gbps AIB
  - A design point at 12, 16 or 32Gbps UCIe could be selected, with the implementation correspondingly more elaborate
  - 8Gbps allows simplifications for pad capacitance, impedance range, termination and BER

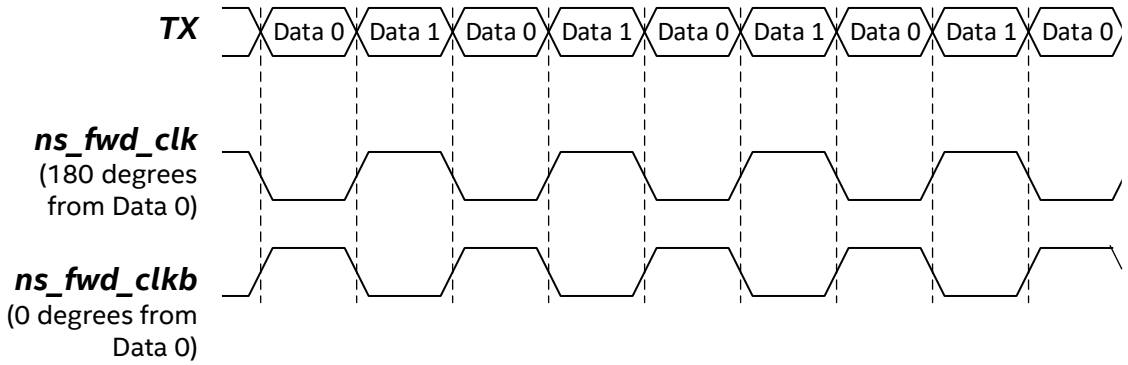
ComboPHY Electrical

Metric	Unit	AIB for reference	UCIe Advanced Packaging for reference	ComboPHY
Typical output swing	mV	850 (Use full swing in both Gen1 and Gen2 modes)*	Various	**800**
Data rate	Gbps	0.1 - 4	4 - 32	**0.1 – 8** (AIB clocking only below 4Gbps)
Latency Target (Tx+Rx)	UI	Not specified for AIB Adapter	12 (for up to 12Gbps)	**13.5**
Channel Reach	mm	Not specified	2	**3**
ESD CDM	V	35	30	**5** (Assembly must be able to meet)
Tx Impedance (min/typ/max)	Ohm	Specified through eye mask	22/25/28	**20/25/30** (UCIe is spec'd for 32Gbps, ComboPHY is 8Gbps)
Tx & Rx Pad Capacitance	ff	300	300 (for 8Gbps)	**300**
Data-rate requiring Termination	Gbps	No termination	No termination (for 8Gbps)	**No termination**
BER for data rate up to 8Gbps		Specified through eye mask	1e-27	**1e-23** (Resolve difference with UCIe spec through a FIT rate analysis)
Eye Height	mV	180	250 (Tightly coupled mode)	**200** (UCIe is spec'd for 16Gbps, ComboPHY is 8Gbps)
Eye Width	UI	0.8 (1.0 – 0.2 Trace)	0.75	**0.8**

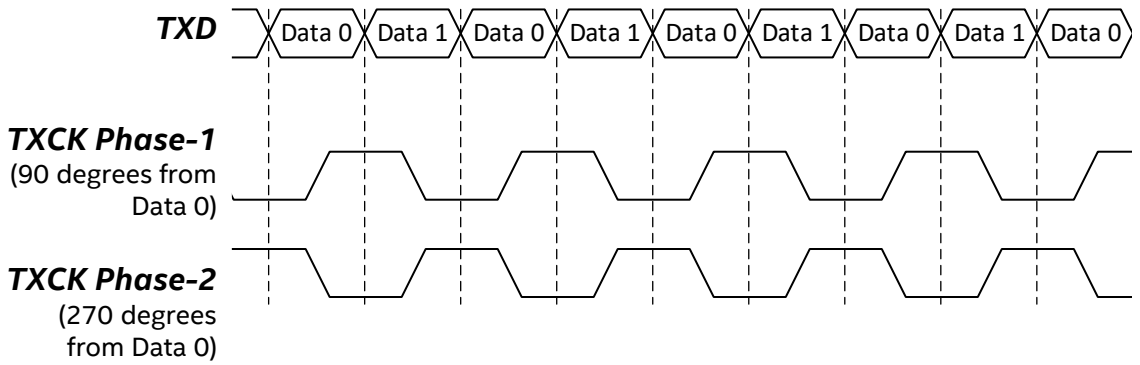
* The AIB2.0 Gen2 output is low-swing. An AIB2.0 PHY is required to interoperate in Gen1 mode with a full-swing AIB1.0 PHY. This guide assumes that an AIB2.0 PHY will operate in Gen2 mode using full-swing outputs, even though that is not required by the AIB2.0 specification.

Clocking

AIB Data Transfer clocking

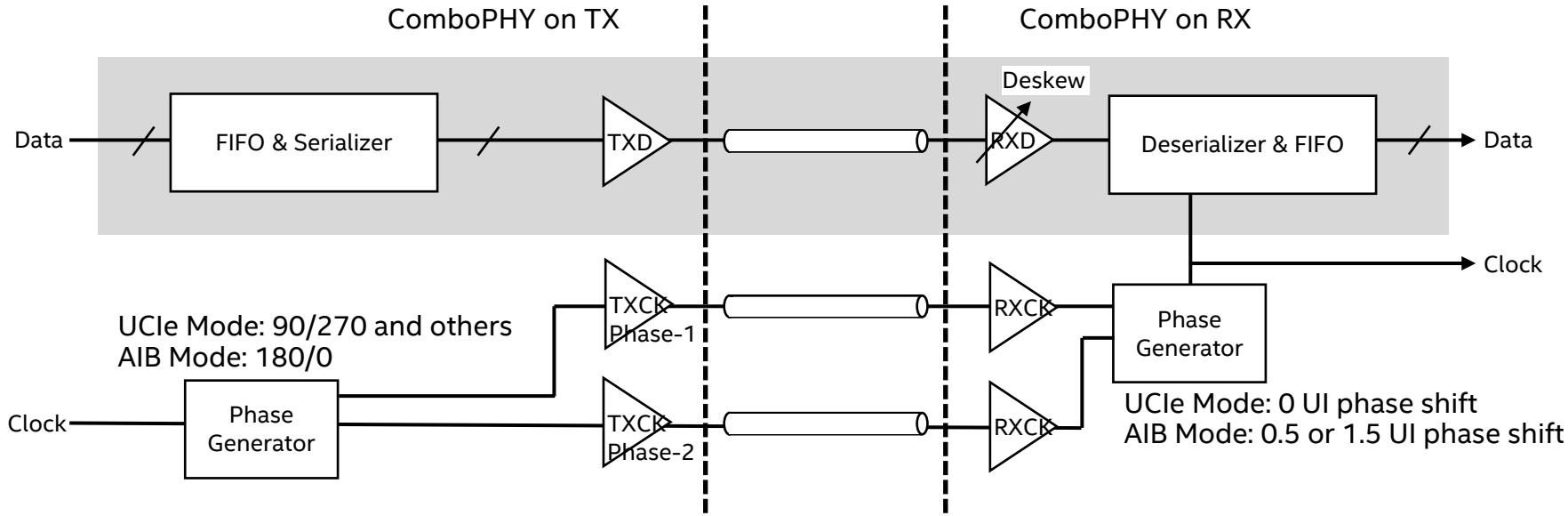


UCIe Data Transfer clocking



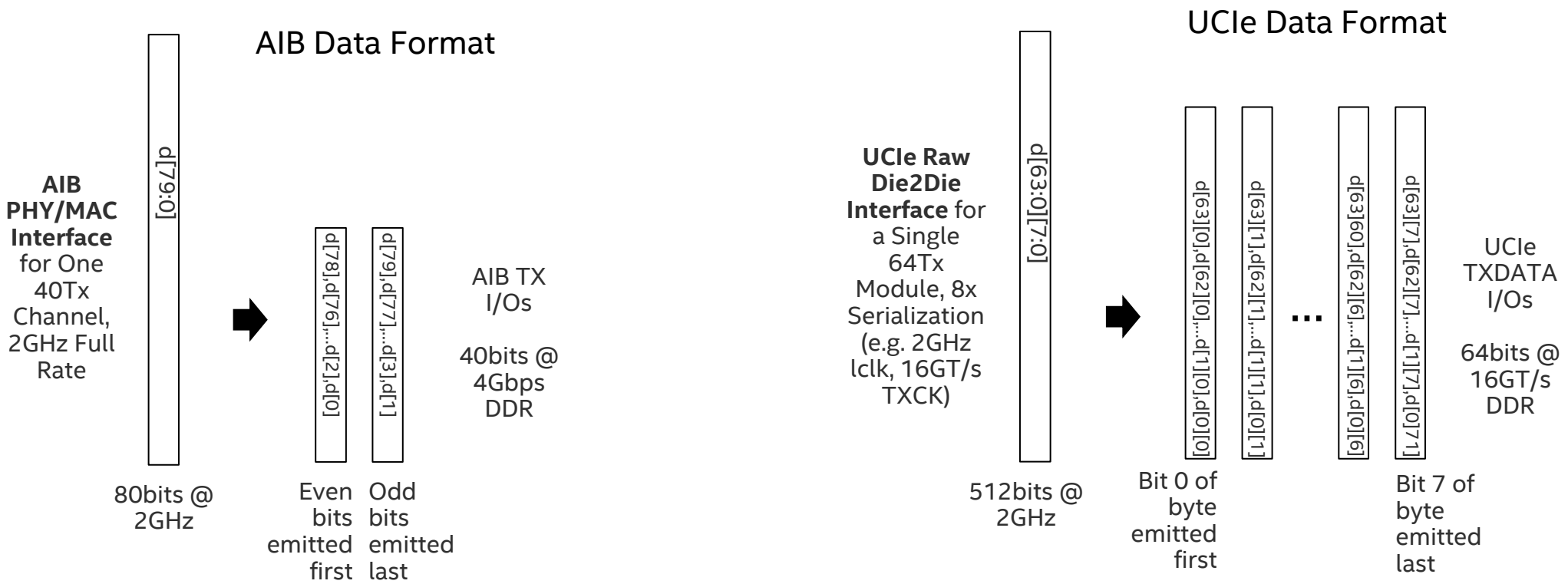
- ComboPHY shall support an additional clock phase pair beyond UCIe requirements to interoperate with AIB: 180/0
- ComboPHY supports 180/0 on both Tx and Rx
- ComboPHY needs to know if it is in UCIe mode or AIB mode to produce the correct clock phases. One way to select the mode is through a strap HI or LO through the package. A package strap is helpful when the mode needs to be known as soon as reset is released.

ComboPHY Clocking



- Clock phase circuits on Tx and Rx need UCIe and AIB superset functionality to produce the correct clock/data relationship (Tx) and to correctly capture the data (Rx)

Data Formatting

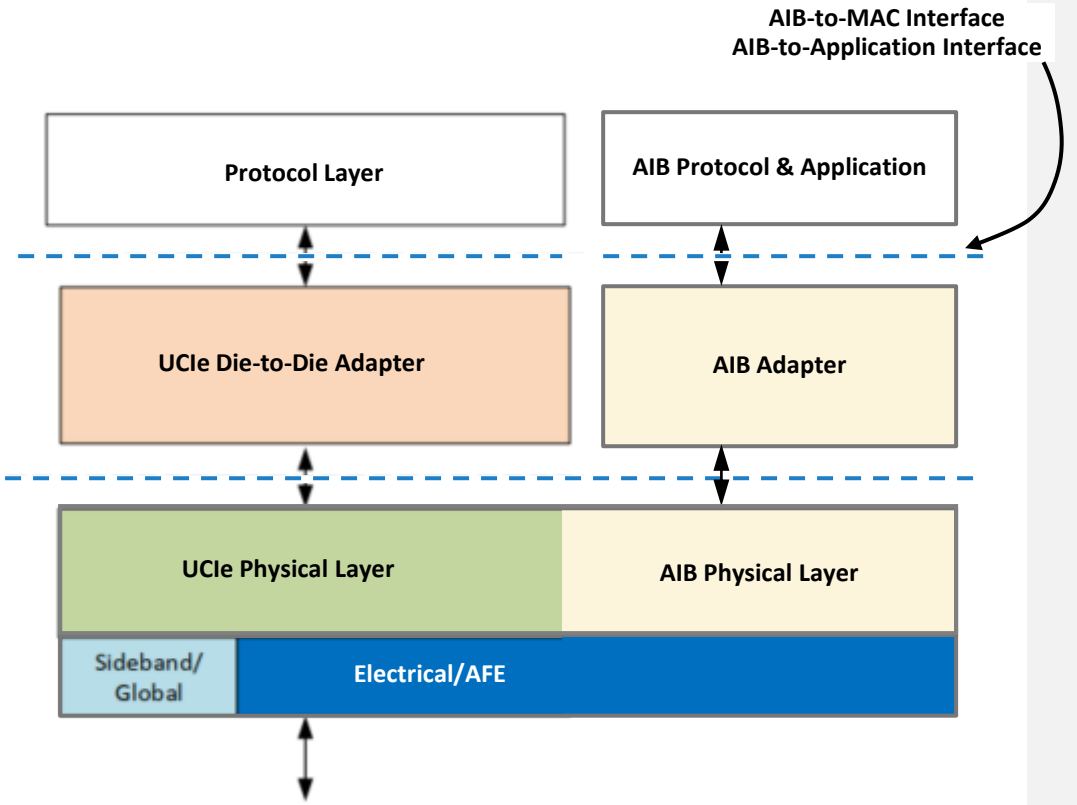


- AIB Data Format: MAC/PHY word is split into even & odd bit words. Even bit word emitted first onto the channel wires.
- UCIe Data Format: Raw Die-to-Die (RDI) or FLIT Aware Interface (FDI) word is split into bytes. Bit0 of bytes emitted first onto the channel wires.
- ComboPHY shall present an AIB PHY/MAC interface (PHY to ASIC/SOC core interface) to support AIB applications, AND shall present RDI and FDI to support UCIe applications
- ComboPHY shall use AIB data formatting to/from its AIB PHY/MAC interface when paired with an AIB chiplet. ComboPHY shall use UCIe data formatting to/from RDI and FDI when paired with a UCIe chiplet.
- Only one of AIB or UCIe format is ever active at any time.

AIB Adapter

ComboPHY AIB Adapter

- The ComboPHY AIB Adapter block performs the shift register data transfer, initialization and calibration functions according to the AIB specification
- The AIB Adapter presents an AIB spec compliant “AIB-to-MAC Interface” and “AIB-to-Application Interface” to higher level code
- It is expected that only one of the UCIe path or the AIB path is ever active on a given multi-chip package (MCP), since the ComboPHY’s companion chiplet type is established at MCP design time



AIB Adapter and AIB Sideband

- The AIB Sideband includes all signals other than mainband data and clocks
- In the ComboPHY, these shall be be passed through asynchronously from the I/Os to an AIB Adapter block
- Note that ns_sr_clk and fs_sr_clk may operate up to 1GHz. The paths from the ComboPHY pin to the ComboPHY AIB adapter for these clocks and the associated data must meet timing for successful data capture (ns_sr_clk, ns_sr_data, ns_sr_load) and output electrical specification and skew (fs_sr_clk, fs_sr_data, fs_sr_load)
- Note that in AIB2.0 Gen2 mode ns_sr_clkb from chiplet is unused and fs_sr_clkb from ComboPHY is unused

AIB Sideband Signals			
Chiplet AIB Name	**Connects to SoC UCIe Name**	**In to ComboPHY or Out**	**Notes**
fs_sr_clk	TXDATA[40]	Out	Asynchronous at ComboPHY I/O, used as clock at ComboPHY AIB adapter
fs_sr_clkb	TXDATA[41]	Out	Asynchronous at ComboPHY I/O, used as clock at ComboPHY AIB adapter
fs_sr_data	TXDATA[42]	Out	Asynchronous at ComboPHY I/O, clocked by fs_sr_clk/b at ComboPHY AIB adapter
fs_sr_load	TXDATA[43]	Out	Asynchronous at ComboPHY I/O, clocked by fs_sr_clk/b at ComboPHY AIB adapter
fs_mac_rdy	TXDATA[44]	Out	Asynchronous at ComboPHY I/O
fs_adapter_rstn	TXDATA[45]	Out	Asynchronous at ComboPHY I/O
ns_sr_clk	RXDATA[40]	In	Asynchronous at ComboPHY I/O, sourced as clock from ComboPHY AIB adapter
ns_sr_clkb	RXDATA[41]	In	Asynchronous at ComboPHY I/O, sourced as clock from ComboPHY AIB adapter
ns_sr_data	RXDATA[42]	In	Asynchronous at ComboPHY I/O, clocked by ns_sr_clk in ComboPHY AIB adapter
ns_sr_load	RXDATA[43]	In	Asynchronous at ComboPHY I/O, clocked by ns_sr_clk in ComboPHY AIB adapter
ns_mac_rdy	RXDATA[44]	In	Asynchronous at ComboPHY I/O

AIB Adapter and AIB Sideband

- Refer to *Advanced Interface Bus (AIB) Specification*, June 17, 2022, Revision 2.0.3
- The ComboPHY's AIB Adapter performs the functions of section 2.2, AIB Adapter and section 3, Reset and Initialization

Other AIB Requirements

Other AIB Requirements

- A ComboPHY should replace the AIB spec DFT requirements with requirements consistent with the overall ComboPHY
  - Near side and far side loopback capability is recommended
  - The test pattern extension is recommended
- Redundancy repair of microbump signals is not supported with a ComboPHY / AIB chiplet pair