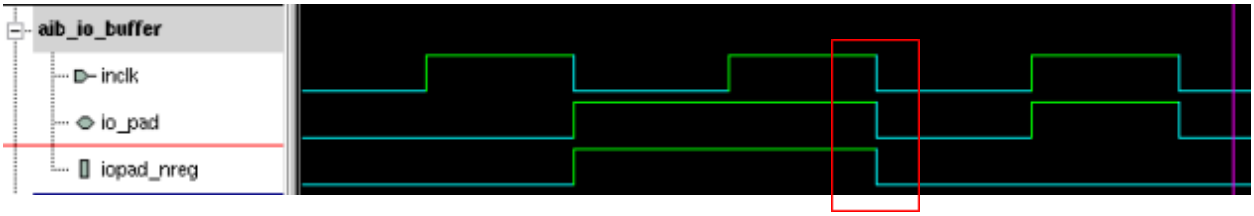
SCENARIO – Two simulations involving AIB to AIB traffic. One simulation behaving correctly according to spec. One simulation broken due to half cycle data misalignment.

Code Block in Question -- **aib_ioring.sv**

```
// Rx data sampled on negative edge of clock
always @(negedge inclk)
 if (rxen)
  begin
    iopad_nreg <= io_pad;
  end
```

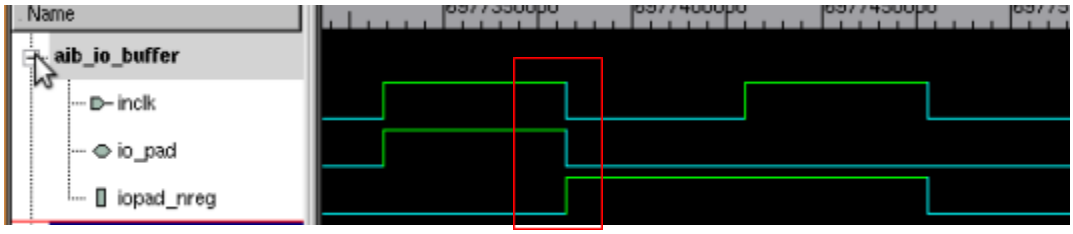
WORKING SIMULATION

- INCLK transitions to 0 (falling edge)
- IO_PAD transitions to 0 on the falling edge
- As a result, iopad_nreg transitions to 0



BROKEN SIMULATION

- INCLK transitions to 0 (falling edge)
- IO_PAD transitions to 0 on the falling edge
- iopad_nreg transitions to 1 **(race condition!)**



SOLUTION – Adding the following modification to aib_io_buffer.sv fixed the race condition presenting itself within iopad_nreg on the receive clock. However, one of our architects noted that the receive-side DLL in the AIB block should delay fs_fwd_clk by 90 degrees before using it to sample io_pad. Can you please investigate this and provide a more permanent solution?

```
assign #1 rx_strbclk = rxfcki;
```