RISC-V DV Workgroup update

3-23-2021

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Google

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Agenda

- Workgroup Overview
  - Attendance, topics, and etc. (3mins)
  - CI platform (3mins)
  - Python based tool (5mins)
  - Upcoming features (4mins)
    - ePMP Extension

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What are we doing?

Create a forum for discussing CHIPS Alliance contributions that will provide or enhance verification platforms. The WG should strive to accept/support platforms that demonstrate compliance, functionality and perhaps eventually performance.

What's been happening in the riscv-dv Workgroup?

- We've had 13 meetings!
- ~10 - 25 attendees/meeting. Participants include: Imperas, Google, Western Digital, Andes, Metrics and PerfectVIPs.
- Presenters from Edalize/Fuse-SOC
- Established riscv-dv Continuous Integration Platform
- Significant progress on Python based - riscv-dv-pyflow

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Evolution

2019 H2

+ ISA: F/D/A extensions
+ Debug mode support
+ Functional coverage model
+ Hint/illegal instruction testing
+ Handshake mechanism
+ Simulator: Questa, Metrics
+ ISS: ovpsim, whisper, sail-riscv
+ YAML based end-to-end flow
+ 10X speed improvement

2020

+ **Formed CHIPS ALLIANCE WG**
+ Bit manipulation extension
+ Vector extension
+ Physical memory protection
+ Multi-harts simulation
+ Enhance functional coverage
+ Python based generator

2021

+ **Continue CHIPS ALLIANCE WG**
+ Vector extension to 1.0
+ ePMP

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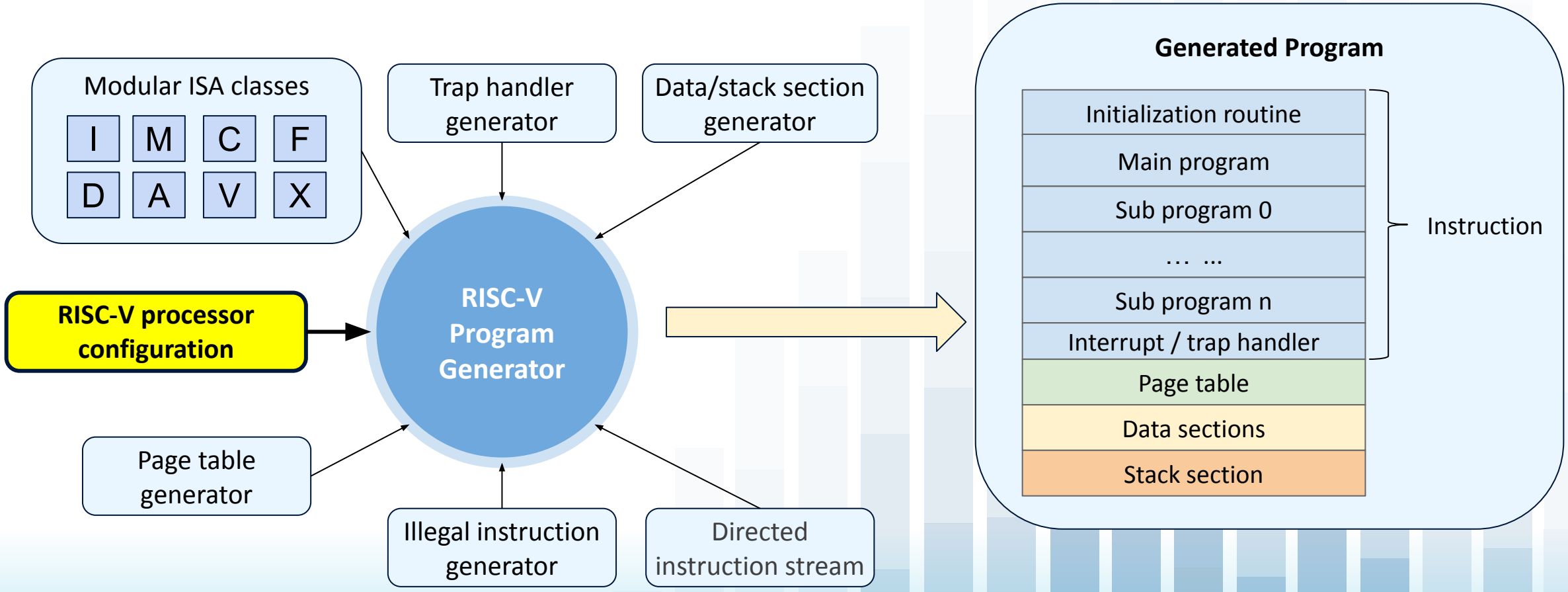
SV/UVM based random test generator



Continuous Integration Platform

- Collaboration between Google Cloud and Metrics
- Maintain functionality across contributions.
- Checks operation against latest version of toolchain

RISCV-DV Python based instruction generator

- Motivation
  - Provide a complete open and free instruction generator for RISC-V processor verification.
- Approach
  - Use PyVSC as the randomization and functional coverage framework
    - pyvsc (Verification Stimulus and Coverage) is a open source Python package for generating randomized stimulus and defining and collecting functional coverage.
    - It provides SV-like constraint and functional coverage syntax.
  - Use the same randomization flow as SV/UVM based approach.
    - Same class structure
  - Seamlessly integrate with the existing end-to-end verification flow

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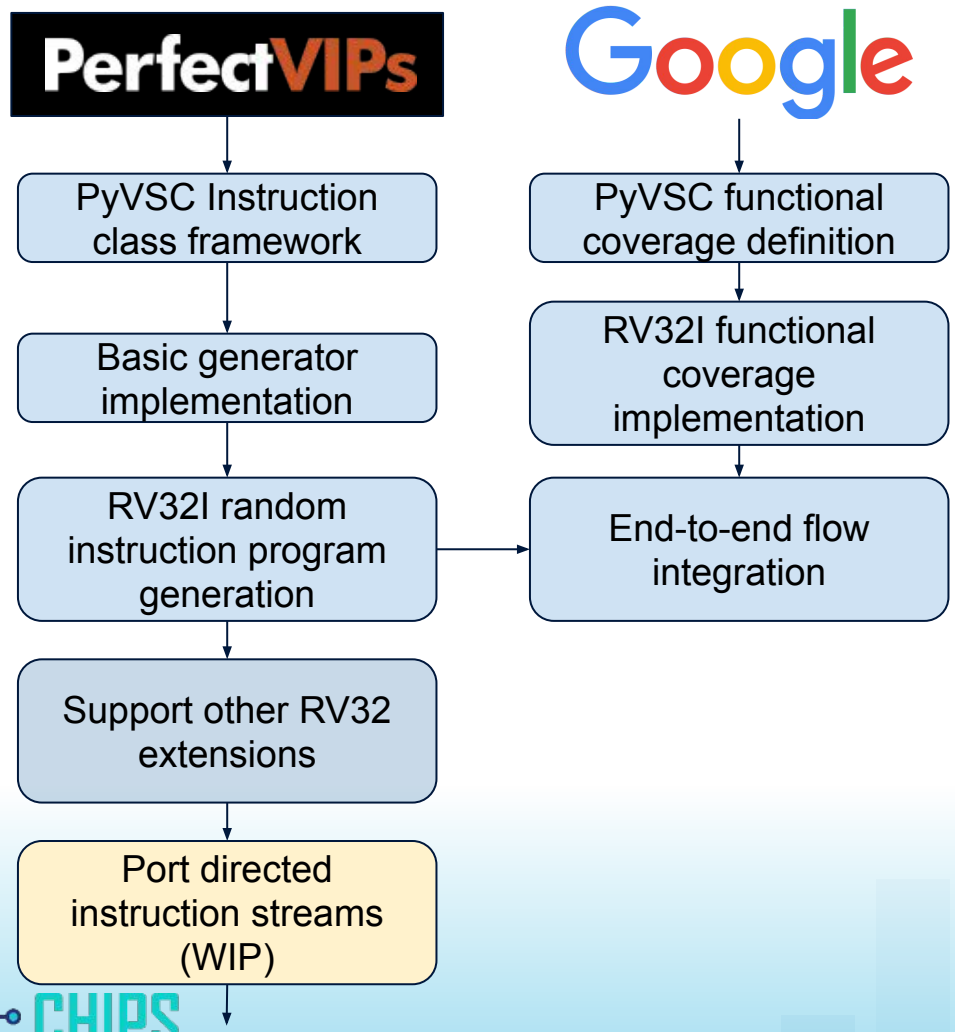
riscv-dv-pyflow Update



- Current status
  - Implemented Instruction class and generator framework
  - Completed random program generation with mixed random and directed instruction stream
    - Support RV32IMCBFDA extensions
    - Support multi-hart program generation
    - Most directed streams supported
  - Implemented RV32I functional coverage model
  - Integrated with upstream end-to-end flow

```
python3 run.py --simulator pyflow --target rv32i
python3 cov.py --simulator pyflow --target rv32i
```

- Future work
  - RV64 support
  - Functional coverage support for all extensions
  - Supervisor/User mode support
  - Feature compatible with SV based generator

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PMP Enhancements (ePMP)

- Original PMP meant to enforce internal memory range protections
- ePMP proposal adds a new CSR that can bypass/update/enforce existing PMP rules
- Plan to implement ePMP support in riscv-dv modularly, such that it remains backwards compatible with "original" PMP specifications
- Immediate use-case: Ibex core used in OpenTitan root-of-trust

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Conclusion

- Continued efforts to add features and enhance riscv-dv-pygen in 2021

- Grow the workgroup - please join if interested
  - Mailing Group: https://lists.chipsalliance.org/g/riscv-dv-wg
  - Google Meets Link here, next meeting 4/2/2021.

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