April 19, 2022

Chiplet Protocol IP

David Kehlet, Intel

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How can we make it easier to build chiplets and multi-chip package devices?

How can we advance the state of the art in chiplet design?

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Outline

- Die-to-Die Interfaces: AIB 2.0, UCIe
- New Chiplet SPI Open Source Hardware IP
- New Chiplet AXI Open Source Hardware IP

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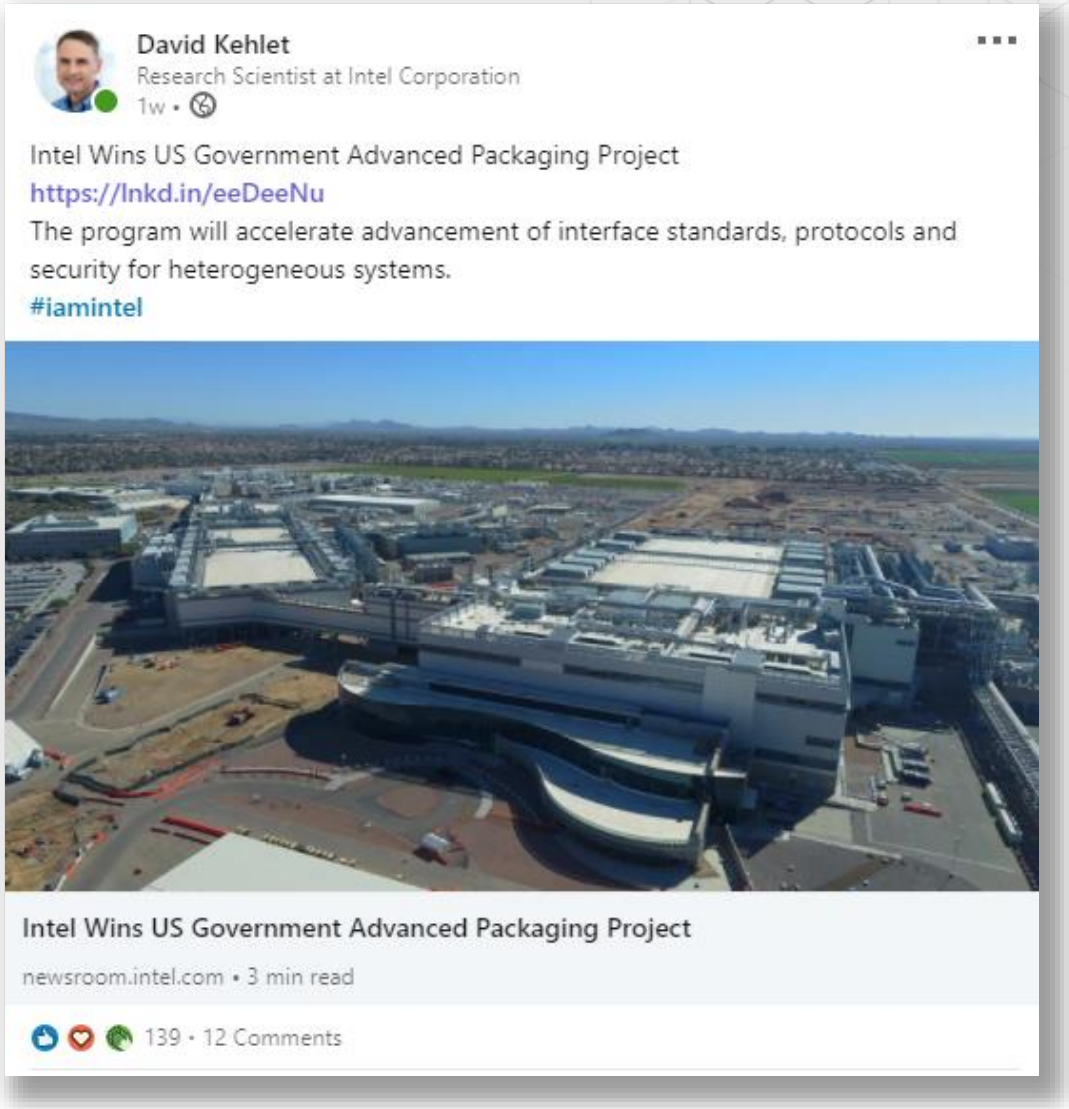
US Government SHIP Program

intel newsroom

October 2, 2020

The News: The U.S. Department of Defense has awarded Intel Federal LLC the second phase of its State-of-the-Art Heterogeneous Integration Prototype (SHIP) program. The SHIP program enables the U.S. government to access Intel's state-of-the-art semiconductor packaging capabilities.



SHIP includes developing chiplet interface standards and protocols

Chiplet AXI and SPI IP are being used in a SHIP Proof of Concept chiplet and Multi-Chip Package

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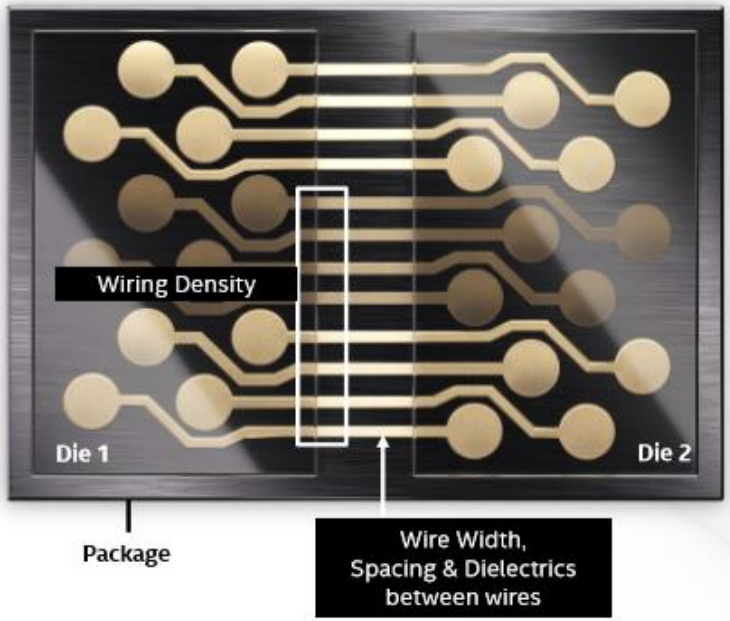
AIB 2.0: A Second Generation Die-to-Die Interface

Enabling an Ecosystem

High density die-to-die interconnects



Feature	AIB 1.0	AIB 2.0
Bandwidth/wire (Gbps)	2	Up to 6.4
Bump density (um)	55	55/45/36
Bandwidth/mm shoreline (Gbps/mm)	256	1638
IO Voltage (V)	0.90	0.90/0.40
Energy/bit (pJ/bit)	0.85	0.50
Backward Compatibility	n/a	1.0

AIB Generator available at:
github.com/chipsalliance

Image: Intel

AIB 2.0: A Second Generation Die-to-Die Interface

2.0 Spec at https://github.com/chipsalliance/AIB-specification

2.0 RTL at https://github.com/chipsalliance/aib-phy-hardware/v2.0

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Advanced Interface Bus (AIB) Specification

Feature	AIB 1.0	AIB 2.0
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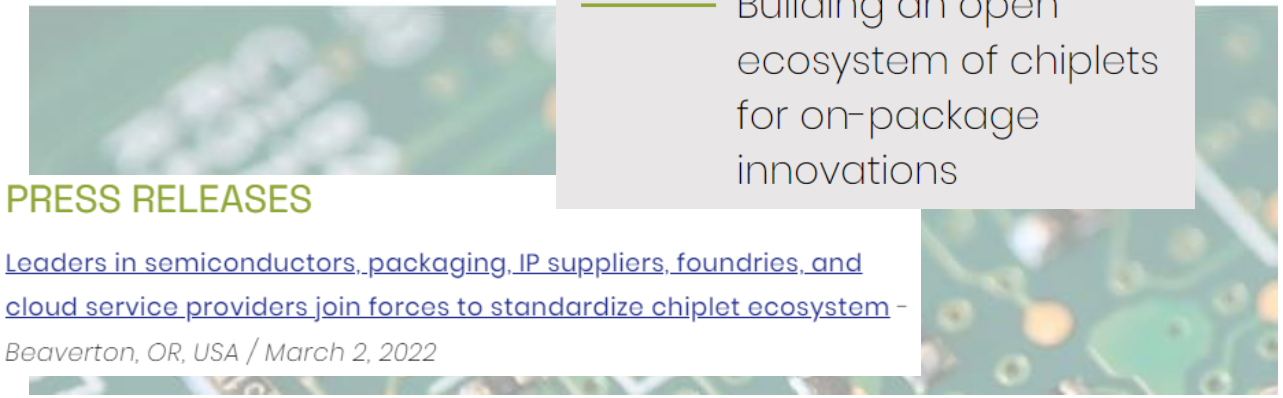
AIB Generator available at: **github.com/chipsalliance**

Image: Intel

Universal Chiplet Interconnect Express (UCIe)

UCIe
Universal Chiplet Interconnect Express

Building an open ecosystem of chiplets for on-package innovations



PRESS RELEASES

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers join forces to standardize chiplet ecosystem - *Beaverton, OR, USA / March 2, 2022*

- UCIe KPIs include per-wire rates up to 32Gbps
- UCIe specification will include details on interoperation with AIB-based chiplets
- Each UCIe participant determines their own product roadmap and availability
- Request the specification from the UCIe Consortium: https://www.uciexpress.org/specification

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Intel & UCIe

- Q: Will Intel continue to develop products using the current AIB specification?
- A: Yes, new products will use today's AIB interface, along with several being developed in concert with the US Government State-of-the-Art Heterogeneous Integration Prototype (SHIP) program.

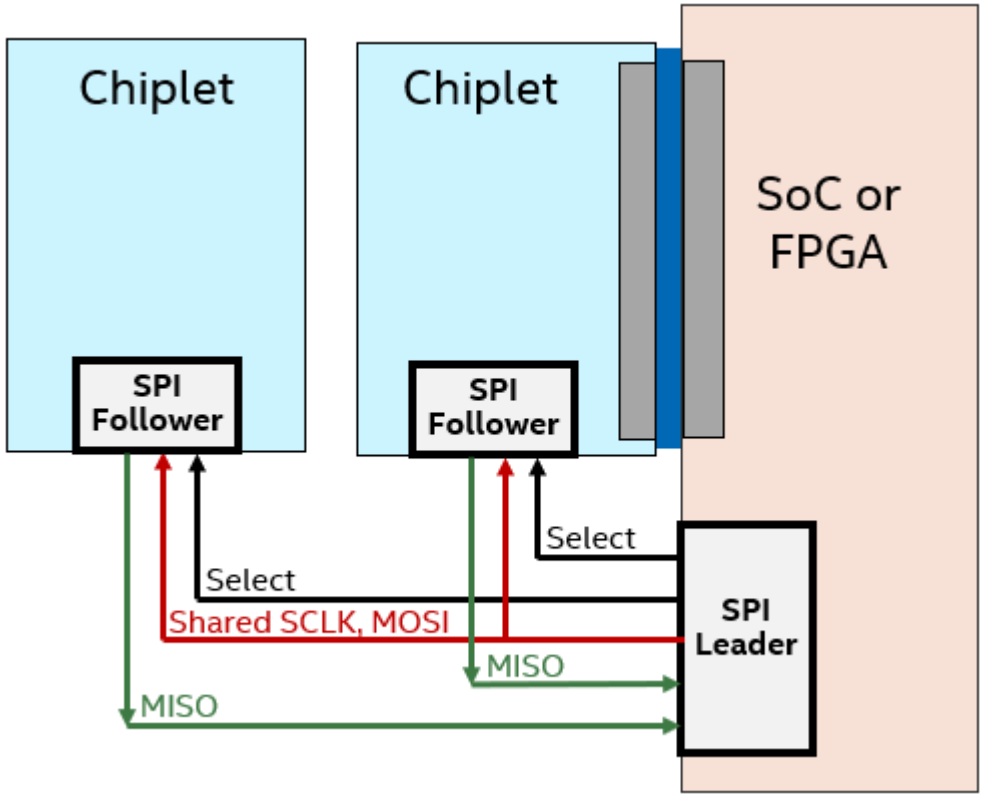
- Q: Will UCIe support AIB?
- A: Yes, the UCIe specification will include details on how UCIe implementations can interoperate with AIB-based chiplets, enabling AIB-based chiplets to join and contribute value to the UCIe chiplet ecosystem.

- Q: What are Intel's plans for AIB going forward?
- A: Intel is committed to UCIe and we will migrate AIB applications to UCIe eventually. The latest AIB 2.0 specification is being used now by developers for new chiplets. We do not expect any new spec development beyond AIB 2.0 given the UCIe path. We expect that many AIB developers will benefit from and seek to transition to UCIe to take full advantage of the improved KPIs. Developers using UCIe will be able to take advantage of UCIe/AIB super-set PHY to access the AIB chiplet ecosystem.

Chiplet SPI IP

Chiplet SPI IP

- Chiplet SPI IP is a simple protocol on top of SPI signaling
  - SPI is widely used for ADC/DACs, peripherals
- Chiplet SPI IP fills a general need for chiplet control, configuration and status
- Providing both SPI Leader (FPGA, ASIC or SoC) and SPI Follower (Chiplet) IP modules
  - Chiplet SPI Follower plugs in to AIB Hard Macro for AIB configuration, *and*
  - Chiplet SPI Follower plugs in to chiplet control and status register application



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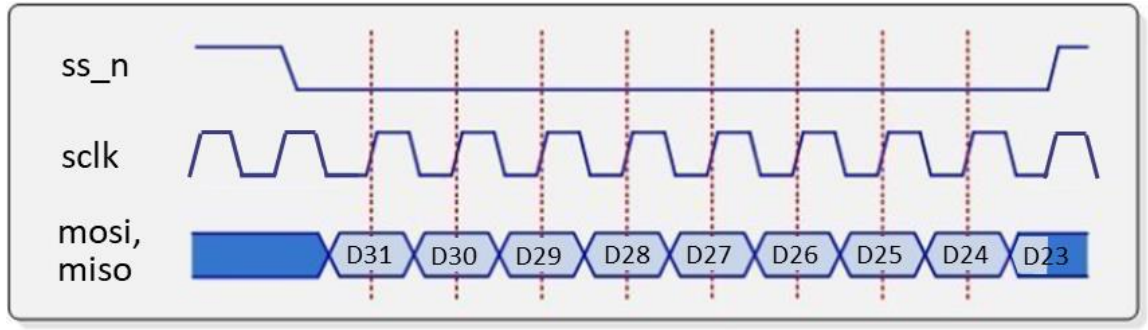
Chiplet SPI Die-to-Die Signals

- Leader supports up to 4 Followers
  - 4 select lines ss_n[3:0]
  - Separate miso[3:0] lines for ease of debugging
- mosi and miso are in 32b DWORD quantities
- Simple, right?
- The trick with SPI is framing of commands and data

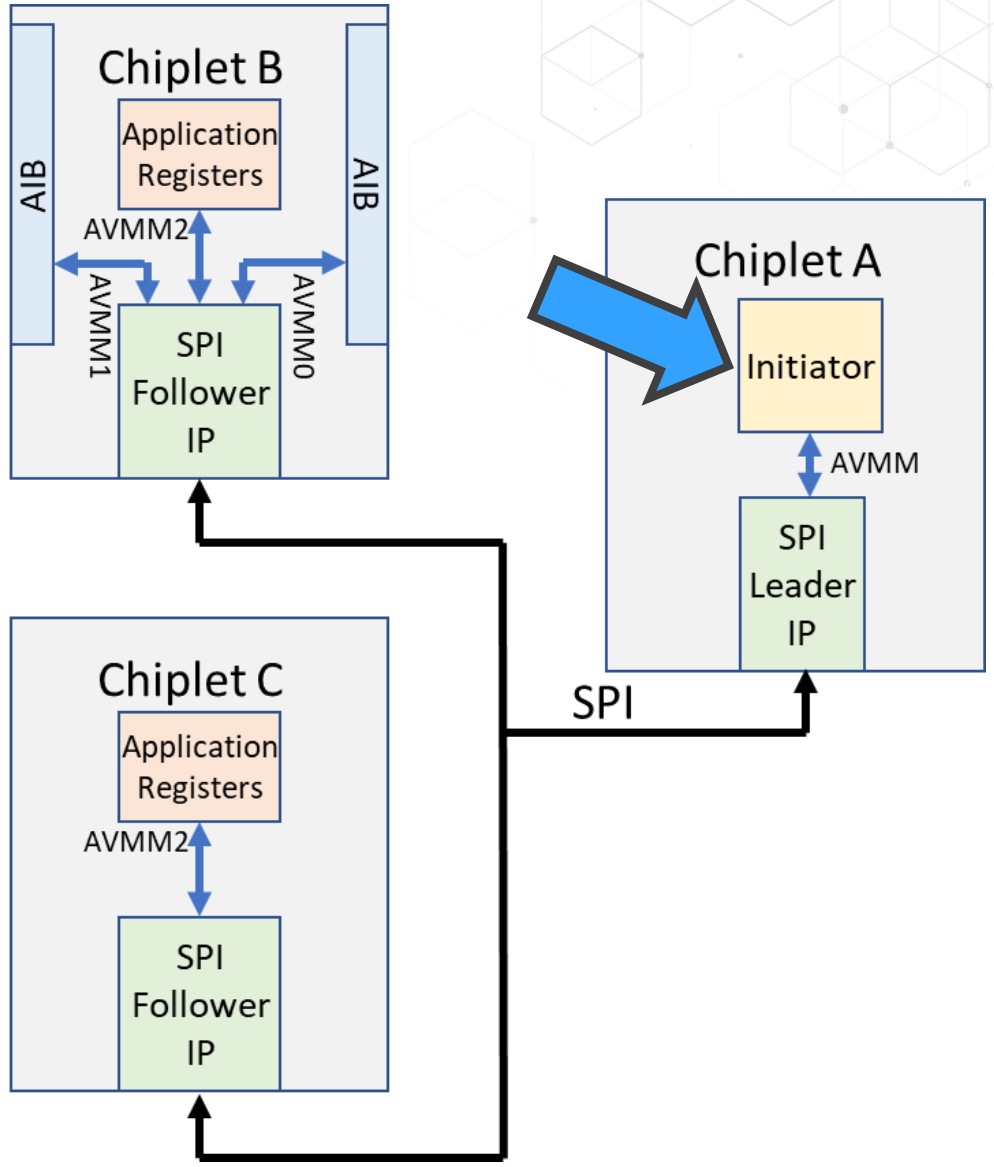
Leader SPI IO Ports	In/ Out	Width	Description
sclk	out	1	SPI serial clock from SPI leader. The SPI IP operates with a continuous sclk.
ss_n[3:0]	out	4	Follower select. Active low means the follower access is enabled. High means the follower is not enabled. The SPI Leader can support up to four SPI Followers.
mosi	out	1	Leader out, follower in
miso[3:0]	in	4	Leader in, follower out. The SPI Leader accepts separate miso lines for up to four SPI Followers.



Chiplet SPI IP Supports SPI Mode0

Chiplet SPI IP Interfaces

- Roles:
  - Initiator (RTL or microcontroller) starts all actions
  - SPI Leader IP (“Leader”)
  - SPI Follower IP (“Follower”)
  - Targets (AIB, Application Registers, other)
- Initiator drives the SPI Leader
  - Simple addressed read/write interface with 32b wdata, rdata



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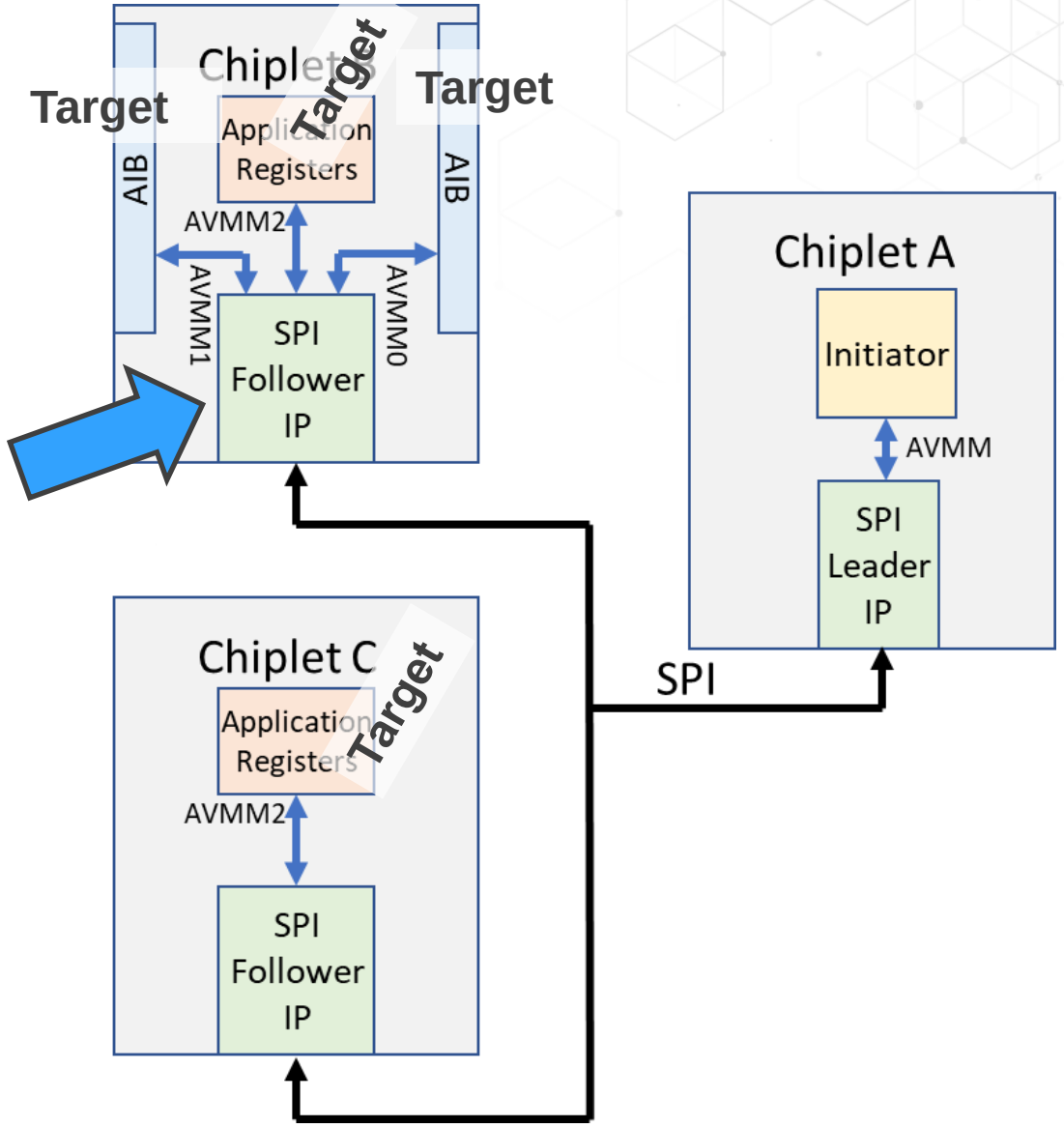
Chiplet SPI IP Interfaces

- **Objective: Writes and reads to Follower Targets**
- Follower has three interfaces to Targets
- Typical targets:
  - AIB PHY control and status registers (see https://github.com/chipsalliance/aib-phy-hardware)
  - General purpose chiplet control and status register block (see https://github.com/chipsalliance/aib-protocols/blob/main/spi-aib/rtl/app_avmm_csr.sv)



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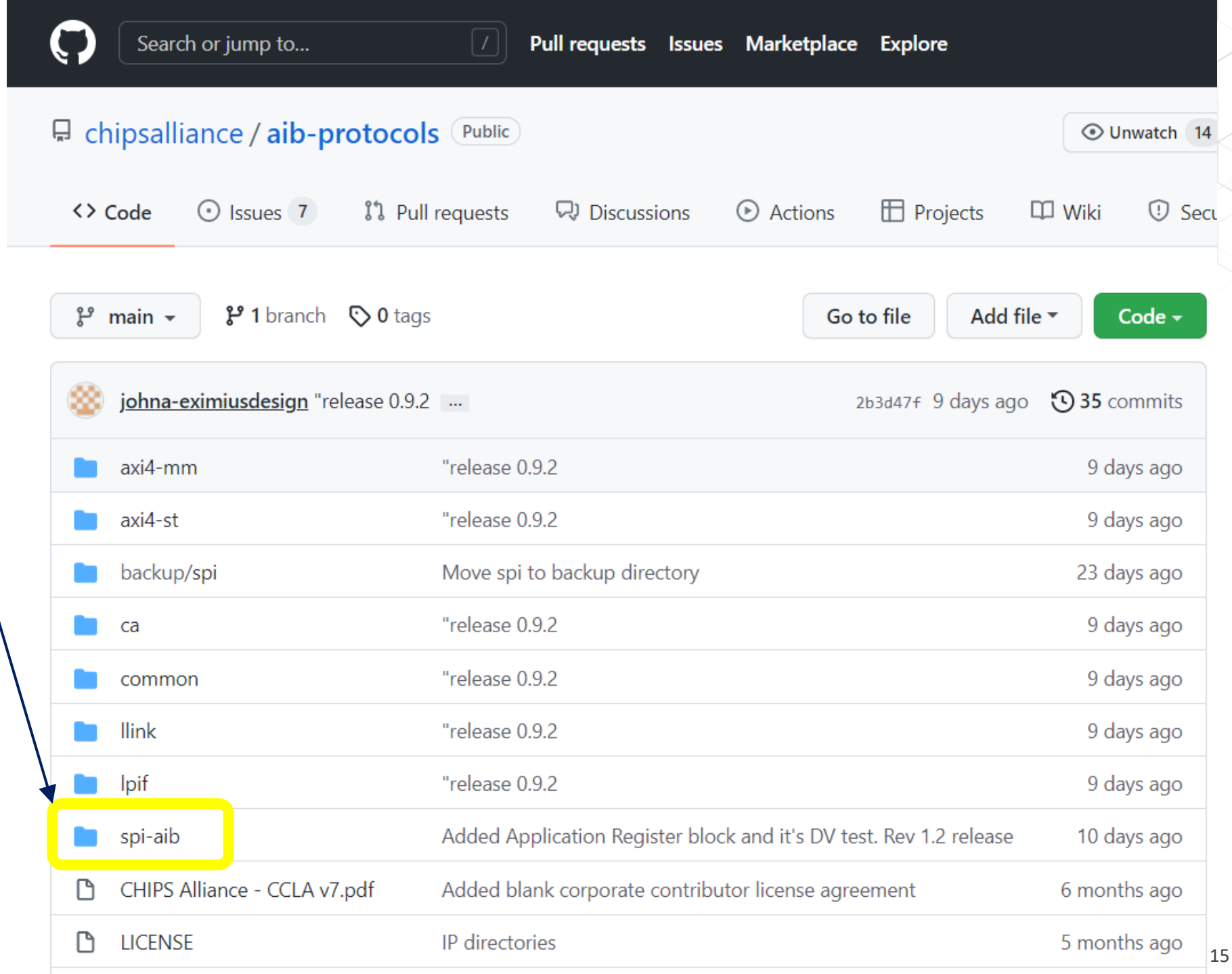
Chiplet SPI IP on GitHub

- Chiplet SPI User Guide:
- https://github.com/chipsalliance/aib-protocols/blob/main/spi-aib/doc/Chiplet_SPI_User_Guide_v1_0.pdf



AXI4 Protocol IP

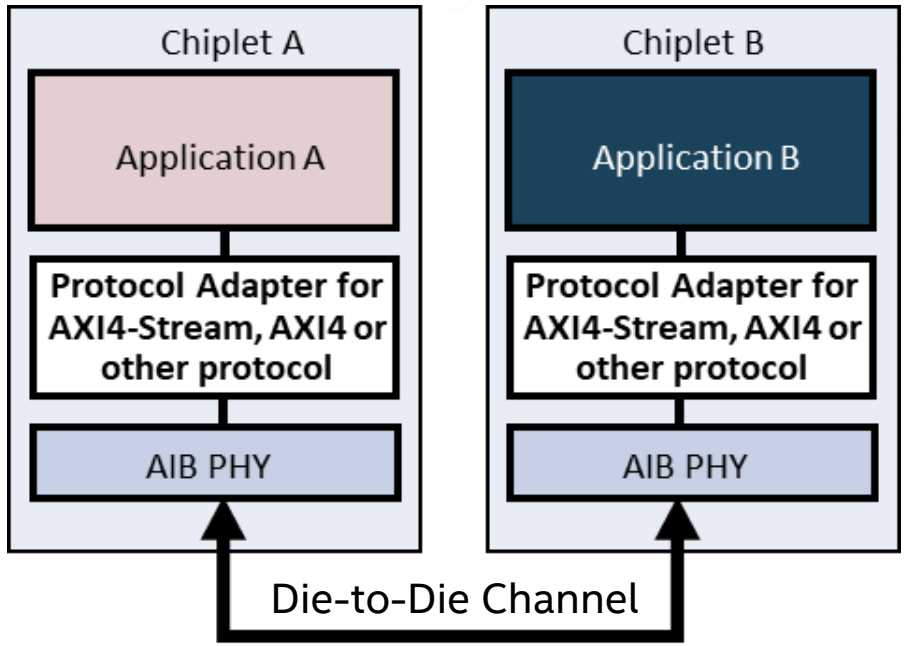
AXI4 Protocols for Chiplet Interoperability

Protocols are the next area of interoperability after the PHY

- The “Data Link” layer in the OSI reference model

Protocol adapters on each side convert the protocol interface to the AIB PHY data wires

- Both chiplets need to know how a protocol is mapped to the wires
- Providing adapter IP for both sides makes sure the mapping is understood



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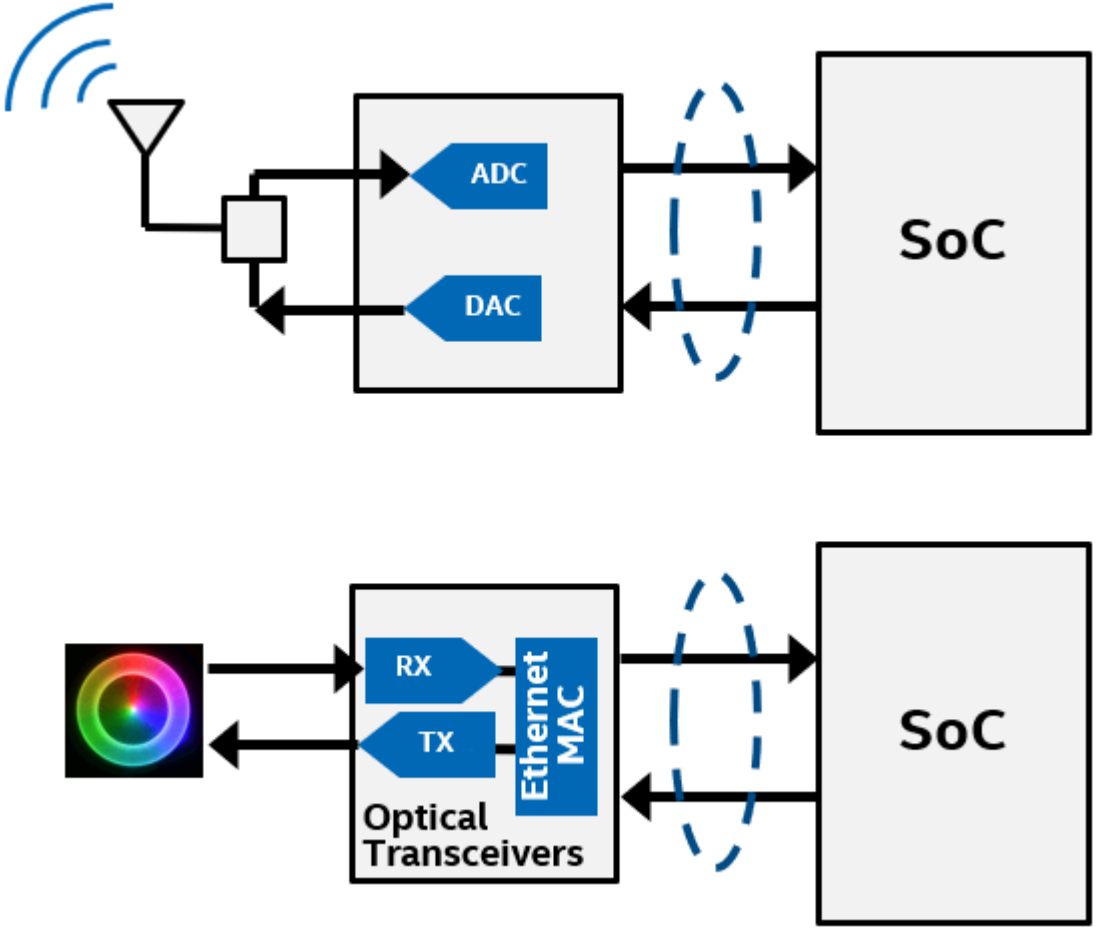
Chiplet Protocols: AXI4-Stream

- Streaming Applications
  - Parallel data width varies by application
  - High utilization/efficiency and Low latency
  - Data usually arrives every clock

  → Looks like AXI4 Stream!



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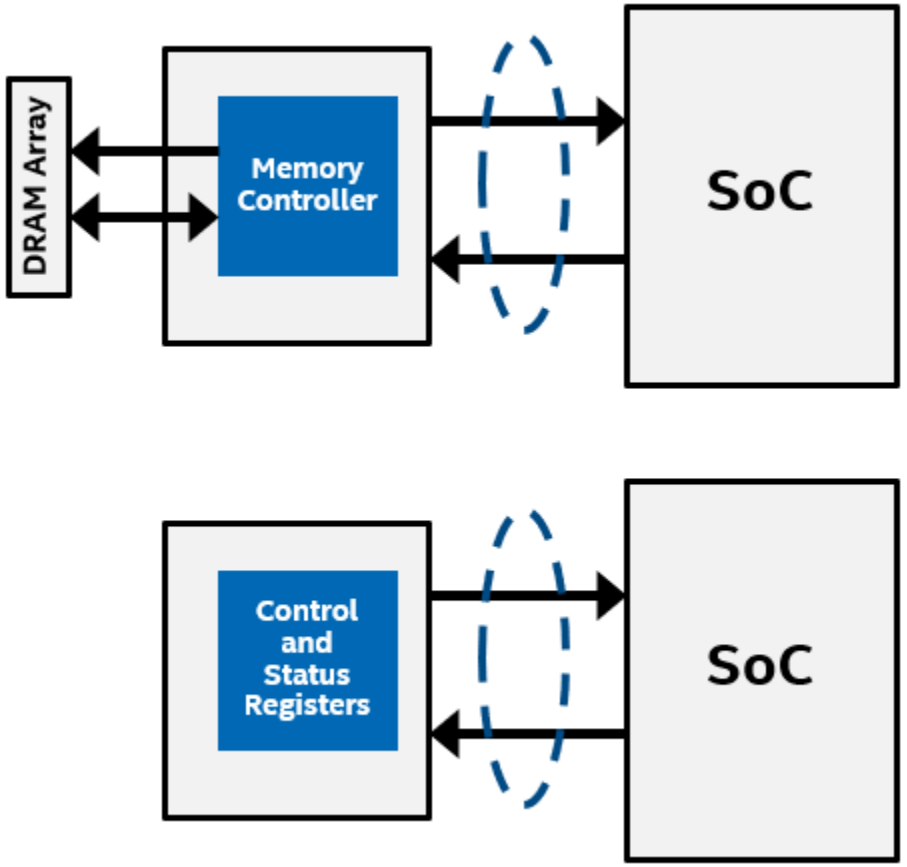
Chiplet Protocols: AXI4, AXI4-Lite

- Memory applications
  - Read and write transactions
  - High utilization/efficiency and Low latency

  → Looks like AXI4!
- Control and Status Registers applications
  - Moderate performance requirements

  → Looks like AXI4-lite!



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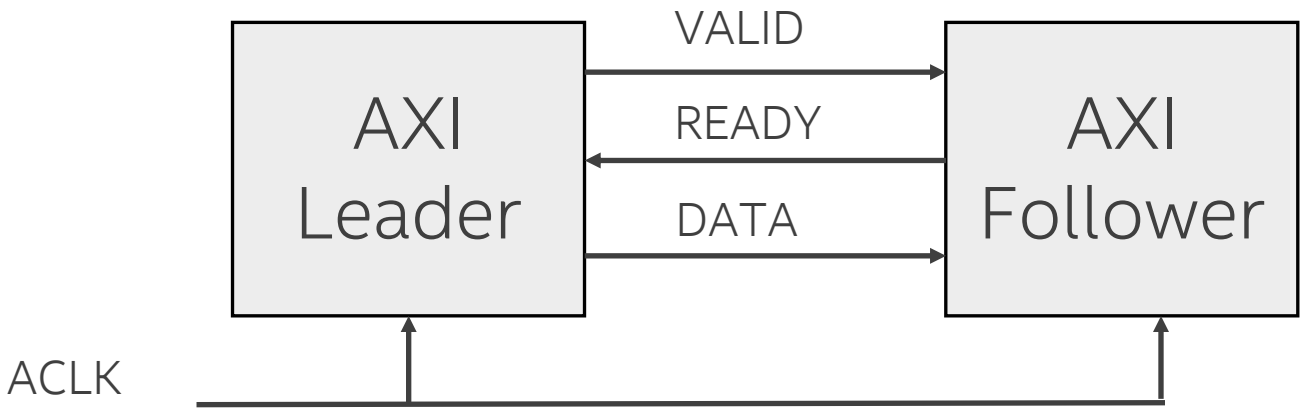
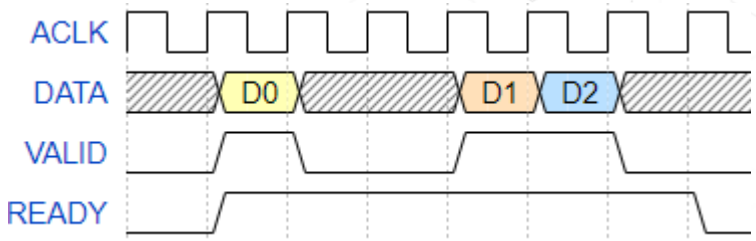
AXI4 Valid/Ready Flow Control Basics





- Leader asserts and holds VALID when data is available
- Follower asserts READY if able to accept data

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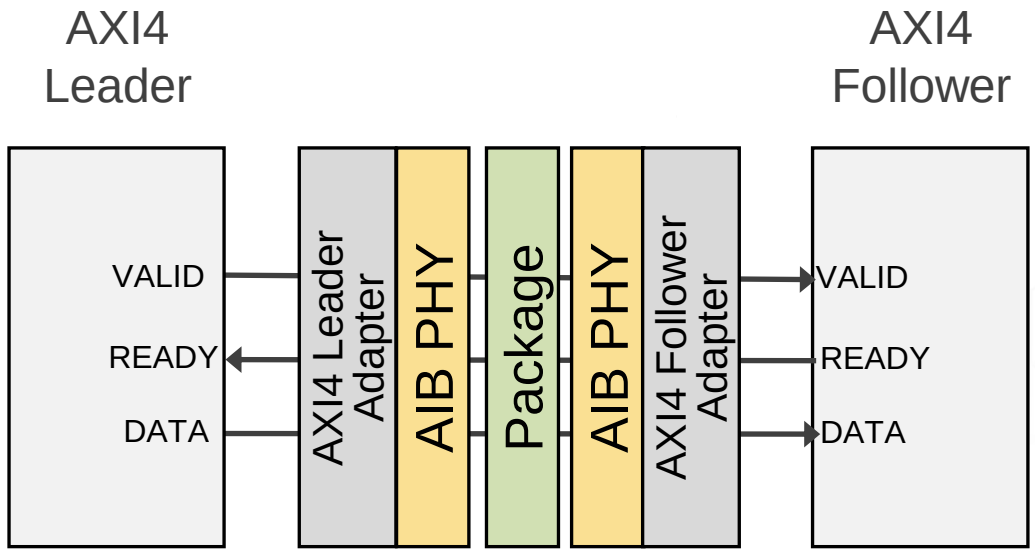
AXI4 over AIB



Leader must react to the follower's READY within the same cycle that READY is asserted.

Straight AXI4 does not work for die-to-die:

- Clock phase difference between leader and follower
- Pipeline delays crossing between leader and follower

Need adapters for AXI4 die-to-die operation, to allow for phase delays & pipeline delays

- Adapters implement a credit scheme: Leader can send when a credit is available, Follower returns a credit when a follower entry is vacated

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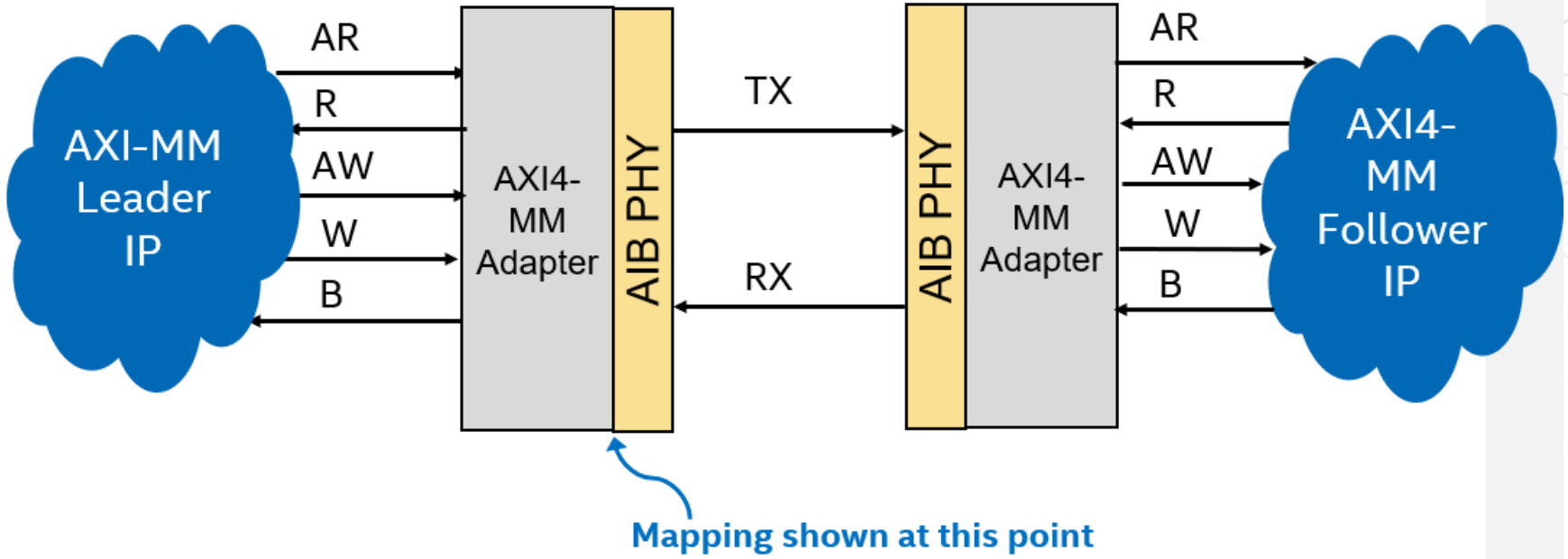
AXI4 Mapping Over AIB



	79	78	77	76	73	72	71	68	65	17	16	14	13	7	6	5	4	3	2	1	0
aw	header=1		r	b	awpush=1	Rsvd	Rsvd	Rsvd	Rsvd	awaddr[47:0]	awsize[2:0]=011		awlen[7:0]=0			awburst[1:0]=1		awid[3:0]			
w_0	header=2		r	b	wpush=1	Rsvd	Rsvd	wl=1	wdata[63:0]									wid[3:0]			

Simple example: 64b data bus over a AIB2.0 Gen2 channel at full rate

- awpush and wpush are “valid” indicators and use up credits in the adapter
- Write response comes back the other way with credit bits

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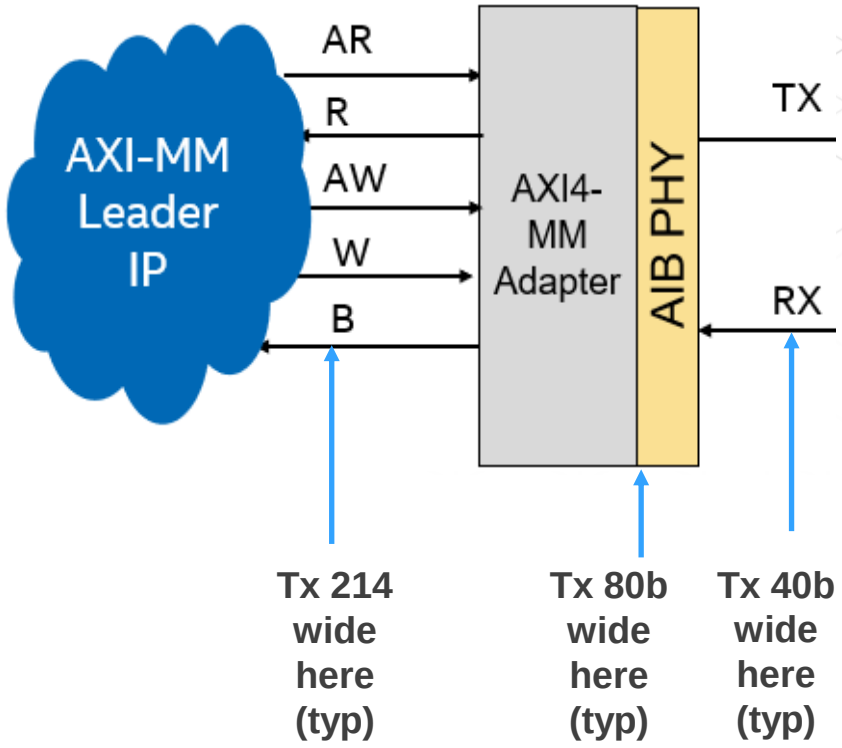
Benefit of Packetizing AXI4

- The AXI4 Adapter packetizes the AXI4 transmit channels AR, AW, W to share the AIB's Tx wires
- Alternatively, one could just fold the AXI4 wires onto Tx
- Compare the results for Packetizing vs. Folding

Case	Packetizing: Full Rate Cycles at Input to AIB PHY	Folding: Full Rate Cycles at Input to AIB PHY
64b Write Single	2	3
64b Write Burst of 4	5	12
64b Write Burst of 64	65	192



- Packetizing is much more efficient!
- When AXI4 is between two modules on the same die, the low utilization of wires is not significant since on-die wire width is up to 20x smaller than advanced packaging (e.g. 100nm on-die vs. 2um advanced packaging)
- Asymptotically achieves 80% efficiency for a 64bit AXI4 interface (80% = 64b AXI / 80b AIB)

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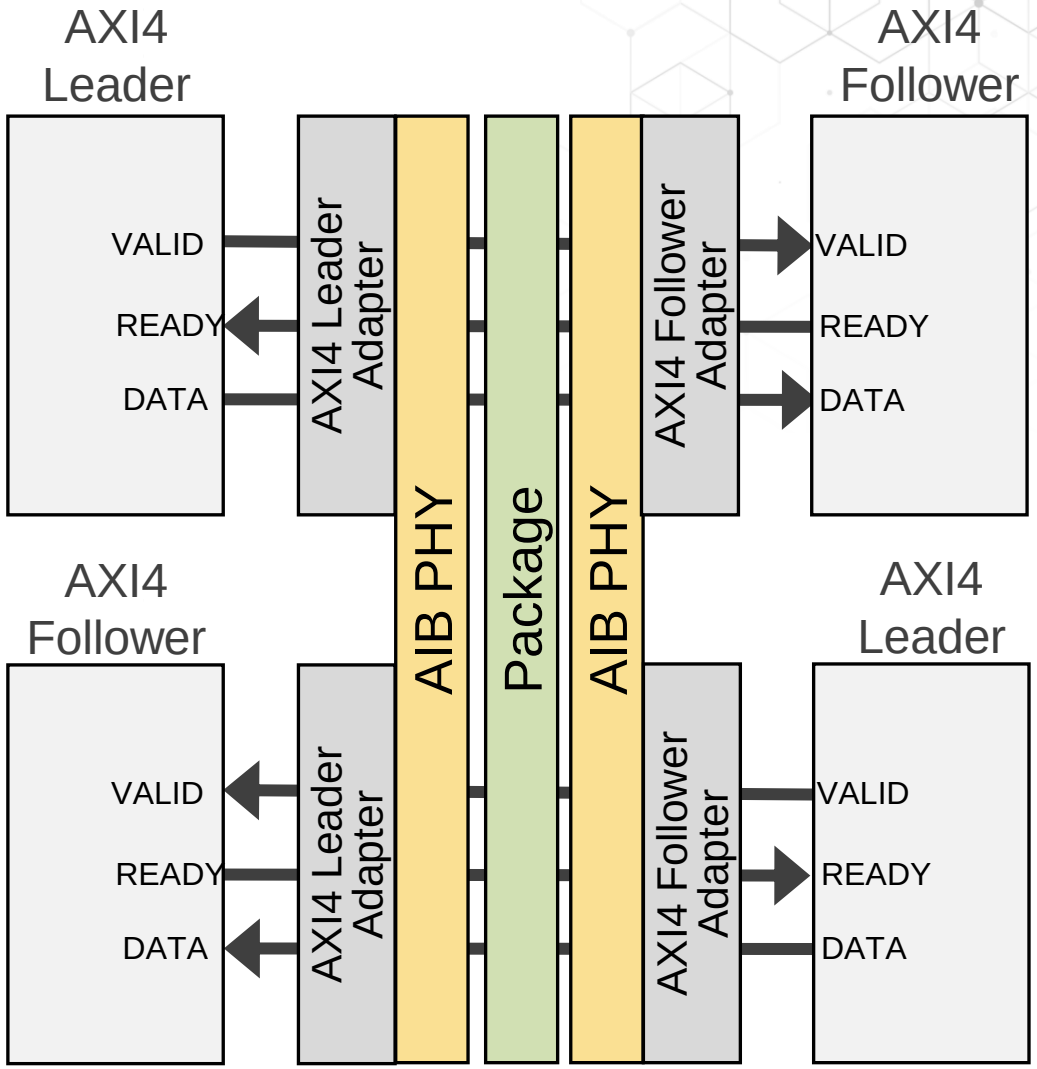
Chiplet Protocols: AXI4-Stream Interface Packing

- Our AXI4-Stream IP will pack an AXI4-Stream leader/follower pair **in each direction** to maximize AIB channel utilization



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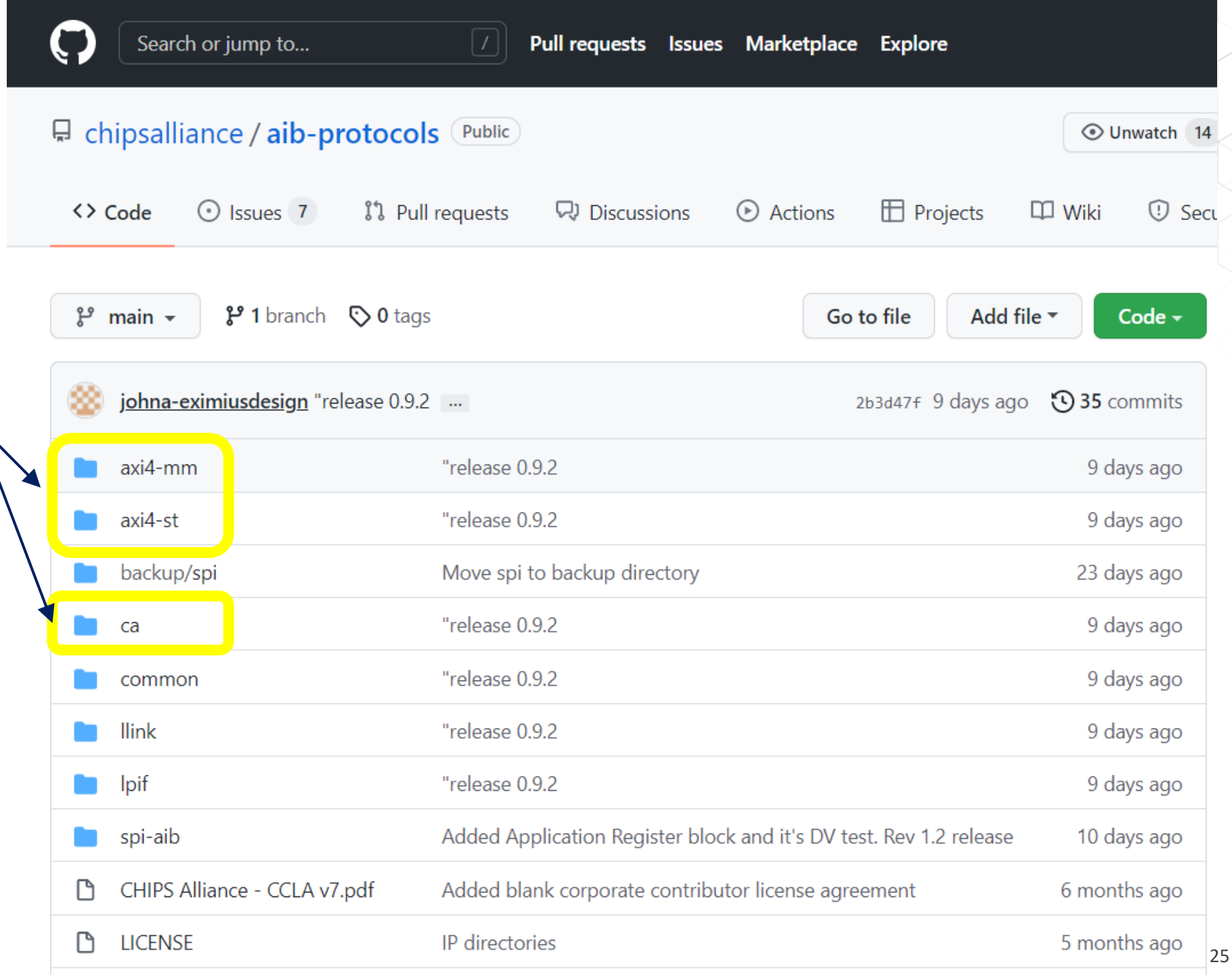
AXI4 IP on GitHub



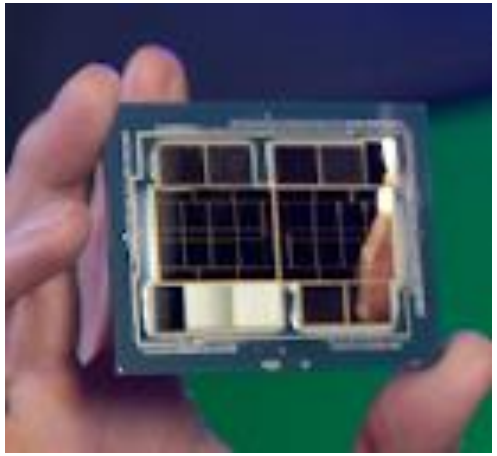
Conclusion

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

-Gordon E. Moore

1: 3rd Page of Moore's 1965 paper, "Cramming More Components onto Integrated Circuits"

- Chiplets are being used to build larger systems – *just as Gordon Moore predicted!*
- Advancing chiplet interoperability with open source hardware protocol RTL



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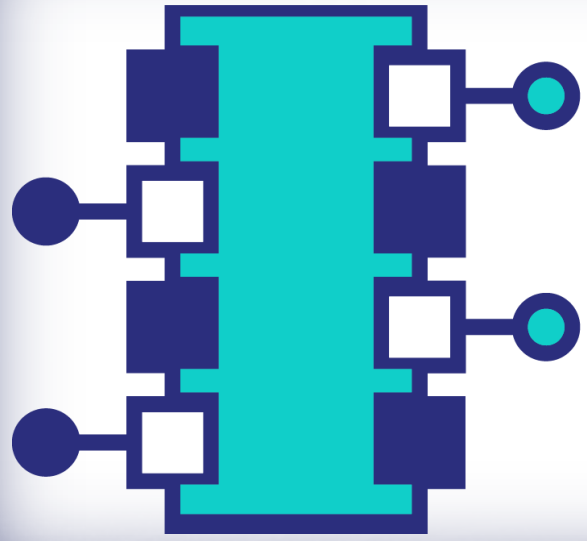

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Backup

Channel Alignment IP

Data distributed over multiple AIB channels will arrive at different times due to skew

Using a “Strobe” bit per channel, a Channel Alignment function can deskew the data

Included with the AXI4 and AXI4-Stream open source hardware IP