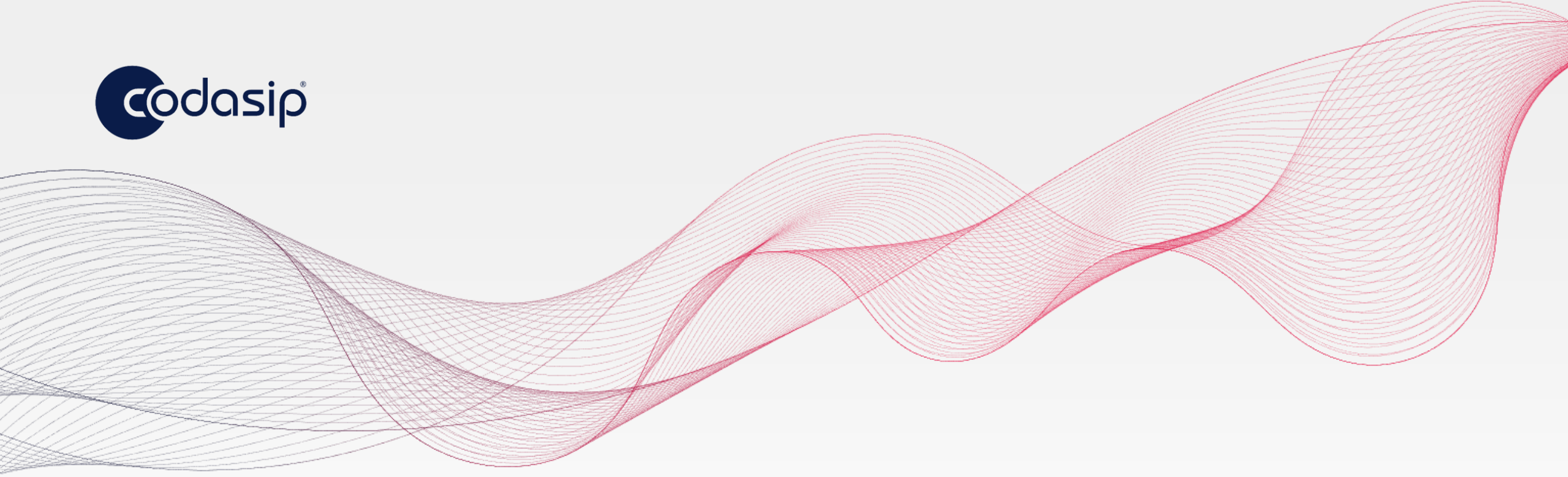


SweRV Core™ Support Package

In A Nutshell

30/03/2021

Zdeněk Přikryl

Codasip®

Solving Your On-Chip Processing Challenges

Who is Codasip?

Leading provider of **RISC-V processor IP** and processor **design automation tools**

Company founded in 2014 in Brno, Czech Republic (EU)

- Based on 10 years of university research on processor design automation
- Founding member of the RISC-V Foundation, www.riscv.org
- Introduced world's first licensable RISC-V processor IP in November 2015

Company headquarters and R&D centers located in the EU

- 90+ employees
- Branch office in Shenzhen, China
- Sales offices worldwide

Codasip Solutions

codasip
RISC-V PROCESSORS

- Selection of processors for any application
- Low power, small size, high performance
- RISC-V-compliant and customizable

codasip
STUDIO

- Create or modify processors using a high level description
- Fine-tune the design for performance, area and power
- Automatically generate dev tools SDK and HDK

codasip
SweRV CORE
SUPPORT PACKAGE

- Comprehensive package of tools
- EDA flows, examples, docs and support
- Available exclusively from Codasip

What Is SweRV?

Open-Source RISC-V Cores

The Family Of SweRV RISC-V Cores

Targeting high performance embedded applications

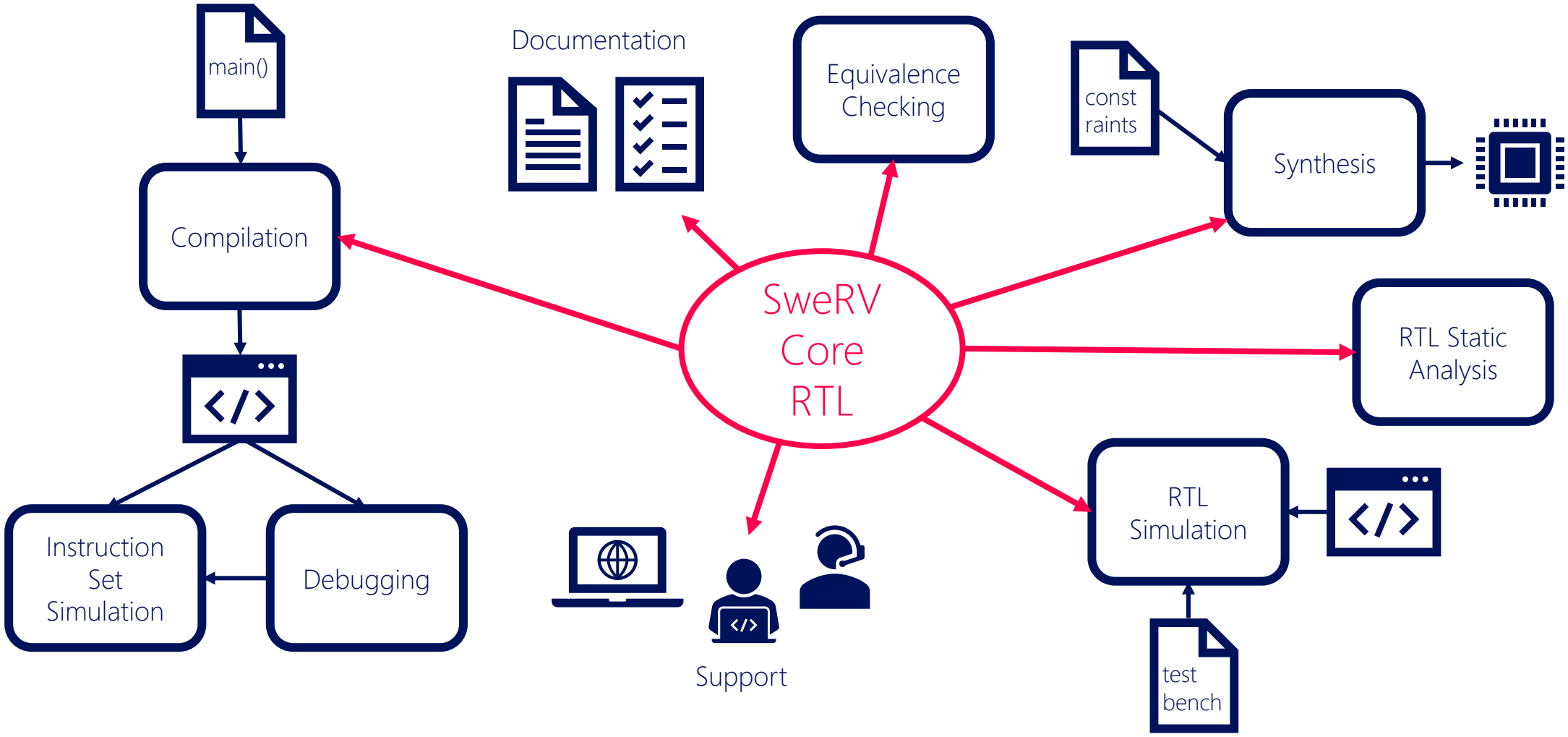
Developed by **Western Digital**

Open-sourced via **CHIPS Alliance**

The RTL provided **free of charge**

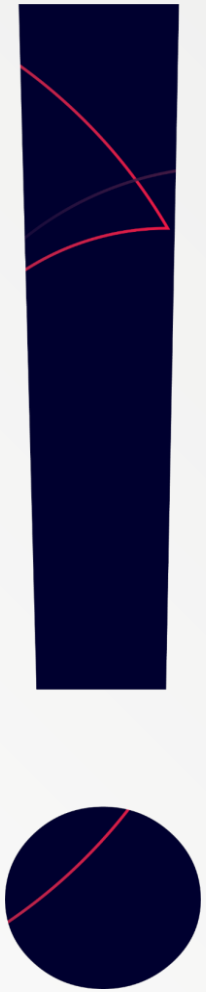
SweRV EH1	1	thread
	2	issue
	9	stage
SweRV EH2	2	thread
	2	issue
	9	stage
SweRV EL2	1	thread
	1	issue
	4	stage

RTL is free! But is it enough?



SweRV Core™ Support Package

Everything You Need To Deploy The Core

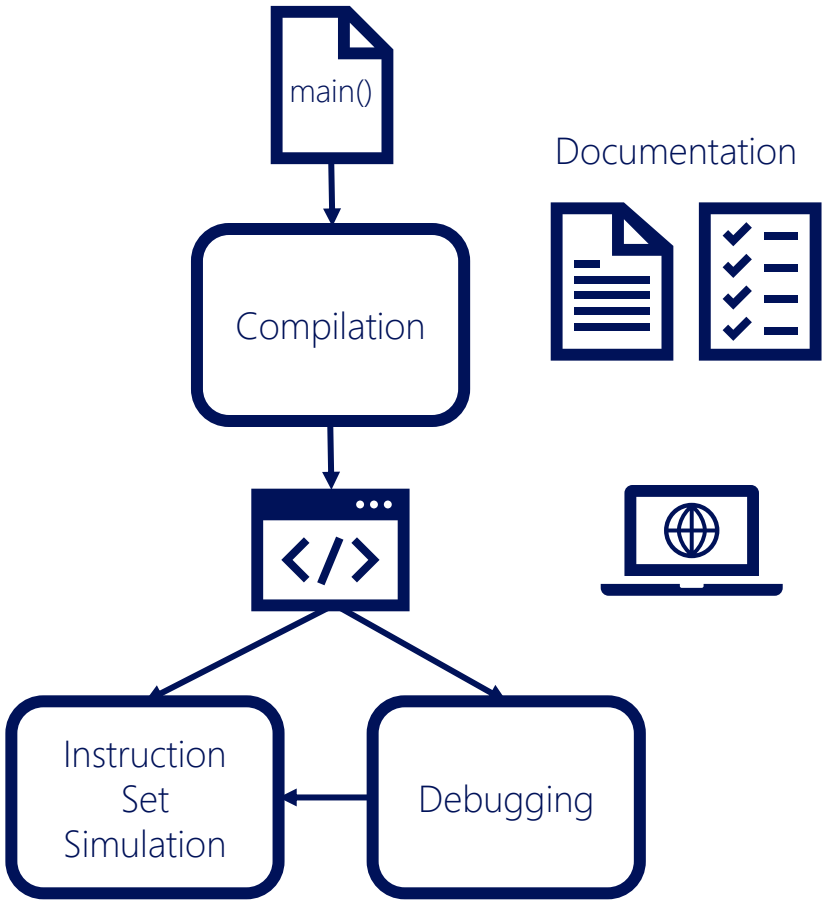


The Free Version

Free student/educational version

The **open-source** contents will stay free

Support may be reached via **GitHub**

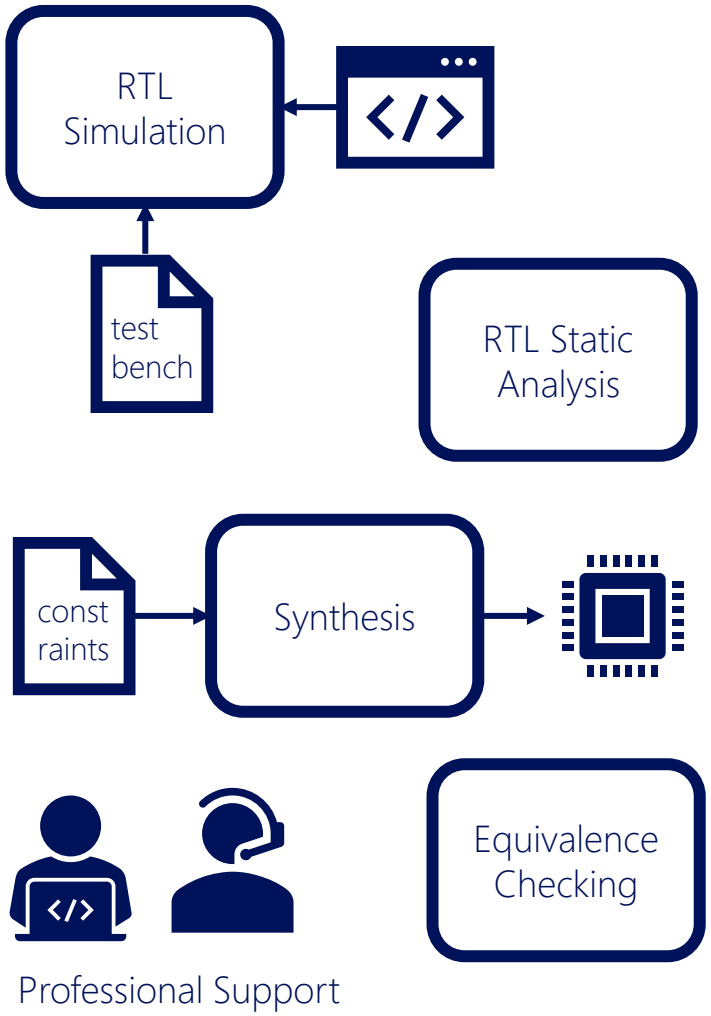


The Pro Version

Adds additional contents on top of the Free version

Integration of **commercial EDA tools** into the design flow

Professional support for the customers



Add-Ons To SweRV Core EH1

Commercially licensed add-ons to the open source SweRV core EH1

Floating point unit

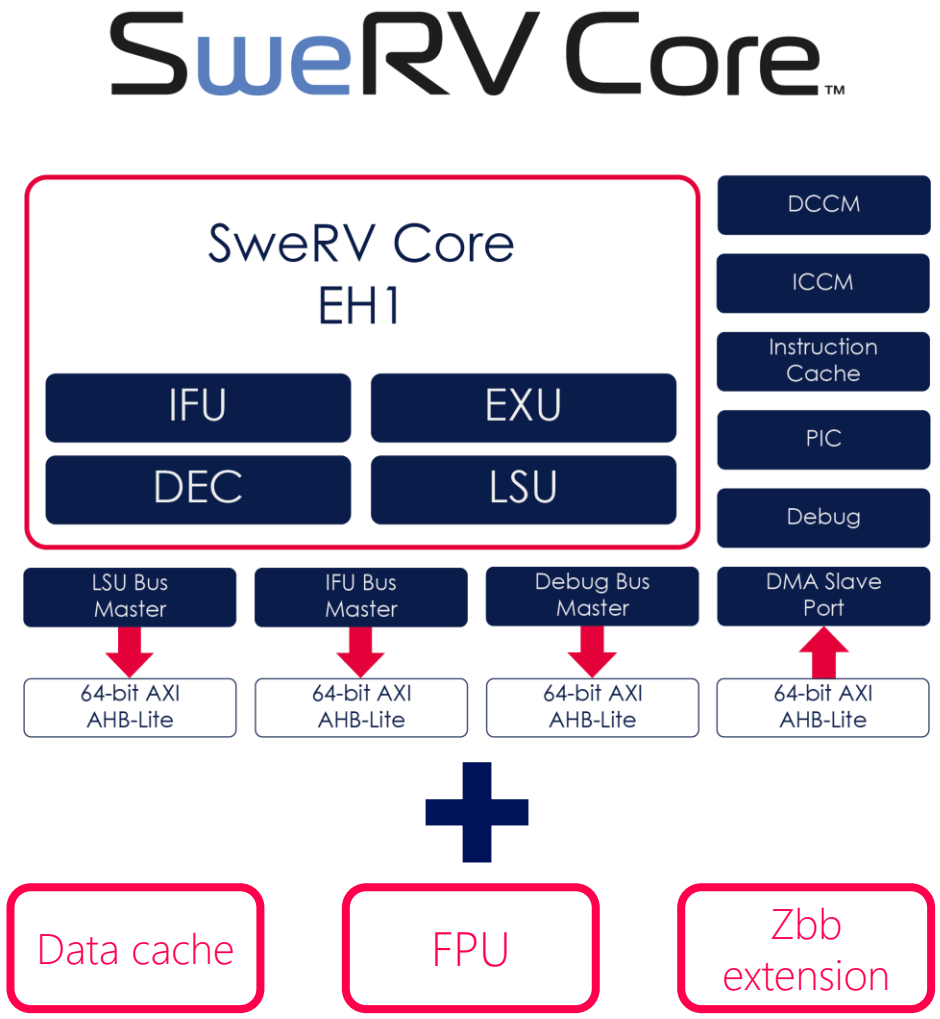
- Single or double precision
- RISC-V F & D extensions

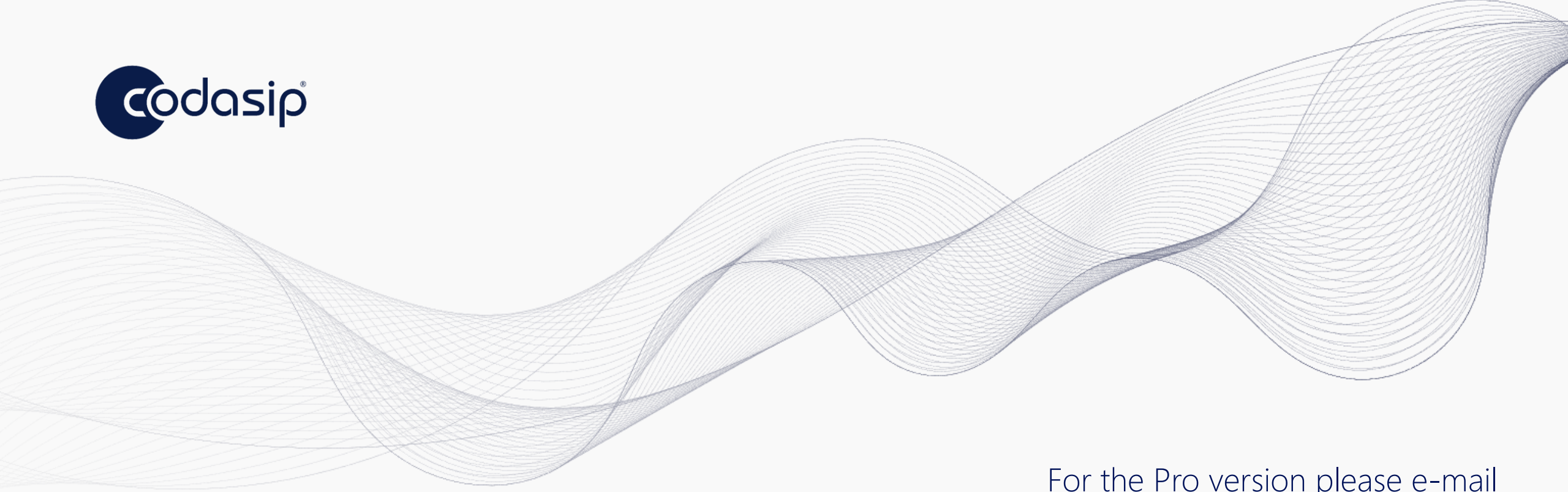
Data cache

- AXI or AHB Lite interface
- Size, associativity, cache-line is configurable

Zbb extension

- Endianness instructions only





Now, it's your turn!

For the Pro version please e-mail
contact@codasip.com
For the Free version please visit
https://github.com/chipsalliance/Cores-SweRV-Support-Package

prikryl@codasip.com