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Workshop

March 30, 2021

8:55am PDT: **Open Source AIB Chiplet Ecosystem**

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Chiplet Origins

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

-Gordon E. Moore

Image: Intel

1: 3rd Page of Moore's 1965 paper, "Cramming More Components onto Integrated Circuits"

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Outline: Open Source AIB Chiplet Ecosystem

- Chiplets are being used to build heterogeneously integrated solutions
  - *As Gordon Moore predicted!*
- SHIP Chiplet Design Technologies Project & Open Source
  - AIB 2.0 & AIB-O
  - Protocols
- Conclusion

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Chiplets in the Industry

- First Generation Chiplet Accomplishments
  - Chiplets are extending Moore's Law
  - Chiplets are commercially viable from multiple silicon suppliers
  - Standardization with the AIB interface is enabling an emerging ecosystem
- Starting on Second Generation Chiplets
  - Flow down SoC concepts like security to chiplets
  - Scale up to die-to-die bandwidth requirements of new wireless and optical systems with AIB 2.0
  - Provide protocol IP to chiplet developers to ease chiplet interoperability

Open Chiplet Interface Standard

Image: Intel

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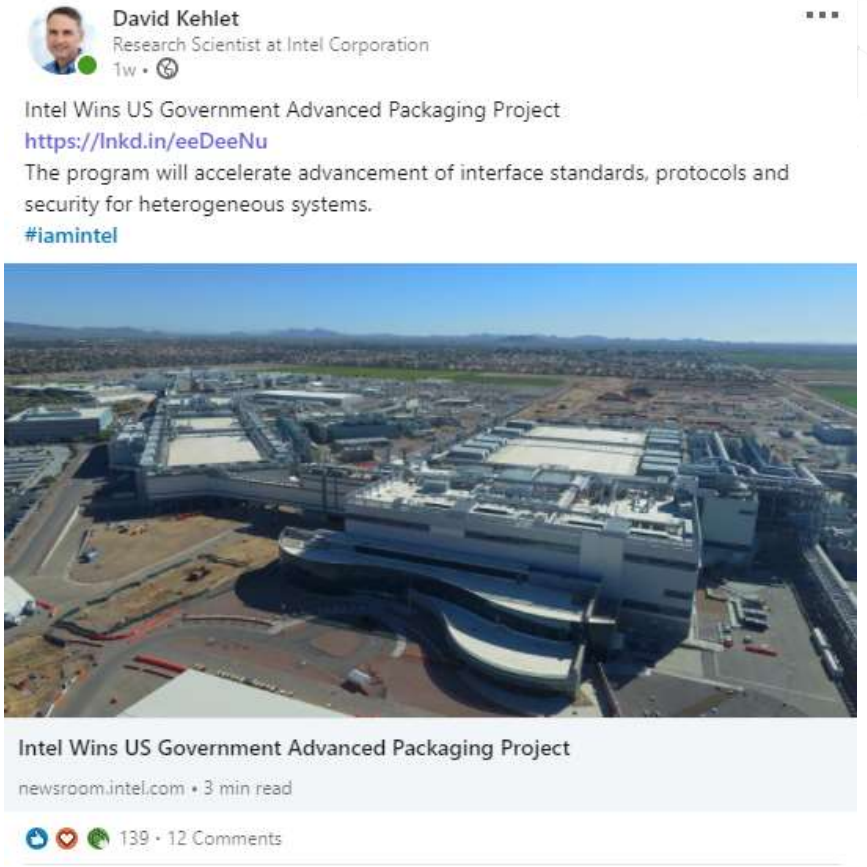
US Government SHIP Program

intel newsroom October 2, 2020

The News: The U.S. Department of Defense has awarded Intel Federal LLC the second phase of its State-of-the-Art Heterogeneous Integration Prototype (SHIP) program. The SHIP program enables the U.S. government to access Intel's state-of-the-art semiconductor packaging capabilities.

- SHIP includes chiplet packaging, manufacturing, security, interface standards and protocols



Images: Intel

USG RAMP Project

STRATEGIC & SPECTRUM MISSIONS ADVANCED RESILIENT TRUSTED SYSTEMS
(S^2MARTS)
REQUEST FOR DESIGNS (RFD)

in support of the

Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP) Phase 2

PROTOTYPE PROJECT REQUEST FOR DESIGNS

Project No. 20-06

The United States Navy and Air Force, in support of the Office of the Secretary of Defense (OSD), is developing integrated circuit (IC) hardware and workflow prototypes…

The Government is interested in selecting one Chiplet design that uses the packaging and interface technology developed in the State-of-the-Art Heterogeneous Integration Prototype (SHIP) program.

Chiplet:

1. > 5M gates w/o memory
2. **Uses AIB (Advanced Interface Bus) and/or AIB-2** interface protocols for IOs
3. **Coordinated with the SHIP program** for packaging and test
4. Must incorporate full production test capability, including DFT, ATPG, designer will provide test vectors, test coverage.

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Growing AIB Chiplet Portfolio

Device with AIB	Process	Status
Intel® Stratix® 10 FPGA	Intel 14	Production
L-tile 17G SERDES	TSMC 20	Production
H-tile 28G SERDES	TSMC 20	Production
E-tile 56G SERDES	TSMC 16	Production
Intel® Agilex™ FPGA	Intel 10	Sampling
P-tile PCIe Gen4/UPI	TSMC 16	Production
University of Michigan offload ASIC	TSMC 16	Powered up
Jariet EW class ADC/DAC	GF 14	Powered up
Ayar Labs Photonics I	GF 45RFSOI	Powered up
University & IP Test Chip (UMich, Blue Cheetah)	Intel 22	Powered up
Intel® High Performance Computing	TSMC x	In progress
Customer I	Intel 22	In progress
Ayar Labs Photonics II	GF x	In progress
Ayar Labs Photonics III	GF x	In progress
Customer II	Intel 22	In progress
Customer III	Intel 22	In progress
R-tile PCIe Gen5/CXL	Intel x	In progress
F-tile 116G SERDES	Intel x	In progress
Commercial	TSMC x	In progress
University	Intel 22	In progress
Intel® next generation FPGA and eASIC™ devices	Intel x	In progress

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9/2020

Technology & Foundry Agnostic

- 3 FPGA families
- 6 SERDES chiplets
- 3 Data Converter chiplets
- 3 Optical chiplets
- 2 ASIC compute chiplets
- 3 University research chiplets
- 3 Customer research chiplets
- 1 Intel® eASIC™ chiplet

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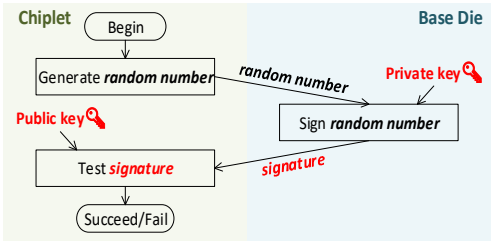
3/2021

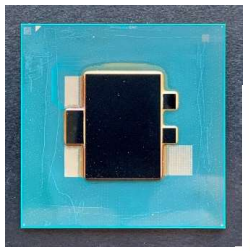
More AIB Chiplets Coming

- **SHIP Design Technologies Chiplet with Defense Industrial Base partner**
- **RAMP Chiplets**

SHIP Chiplet Design Technologies

- Goal of the SHIP Chiplet Design Project
  - Standards, protocol and security IP to enable Defense Industrial Base partners to develop and use chiplets (“Ecosystem Development”)
  - Builds on chiplet ecosystem development and heterogeneous integration experience from Altera, Intel, DARPA Research Projects
- Technology Development within SHIP Chiplet includes:
  - Chiplet interface standards and protocols
  - Security IP for Chiplets
  - Hardware Proof of Concept chiplet & board for proof in silicon



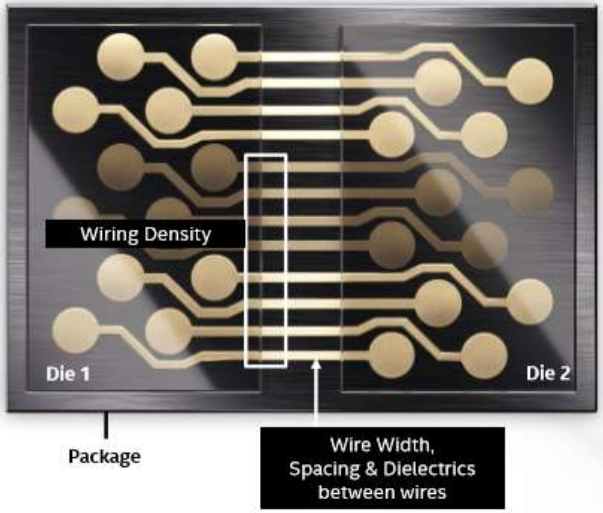


Images: Intel

AIB 2.0: A Second Generation Die-to-Die Interface

Enabling an Ecosystem

High density die-to-die interconnects



AIB 2.0: At 4 Gbps/wire, 7.68 Tbps (Rx+Tx) bandwidth per interface

Feature	AIB 1.0	AIB 2.0
Bandwidth/wire (Gbps)	2	Up to 6.4
Bump density (um)	55	55/45/36
Bandwidth/mm shoreline (Gbps/mm)	256	1638
IO Voltage (V)	0.90	0.90/0.40
Energy/bit (pJ/bit)	0.85	0.50
Backward Compatibility	n/a	1.0

AIB Generator available at: **github.com/chipsalliance**

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Architecture Day 2020

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Image: Intel

AIB 2.0: A Second Generation Die-to-Die Interface

More Features

- Data Bus Inversion
- Loopback for testability
- Test Pattern Generation and Checking BIST extension
- Simplified signal list
- Flexible application clocking

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- **2.0**: Now a CHIPS Alliance Released Specification!
- https://github.com/chipsalliance/AIB-specification

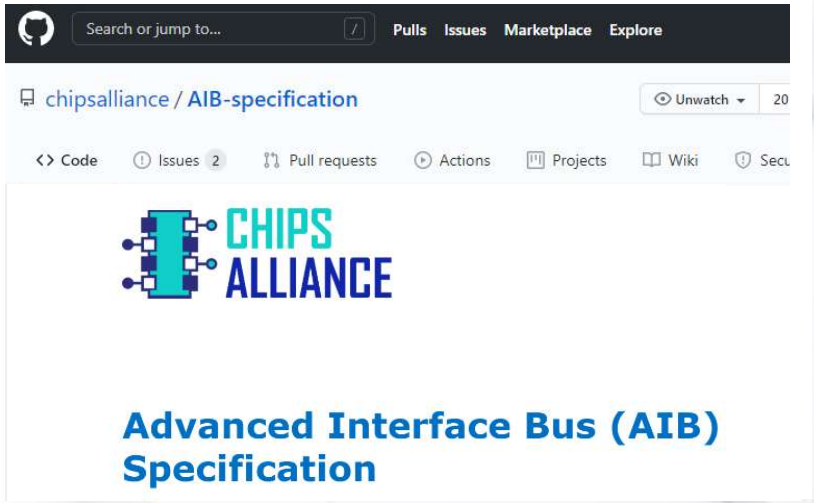

Image: Intel

AIB-O: AIB Optimized for Standard Packaging

- Provides a subset of AIB 2.0 capability with standard organic packaging bump spacing
  - Standard package substrates are more broadly available than advanced packaging
  - Can be assembled by many Outsourced Semiconductor Assembly and Test (OSATs)
- Wires on standard packaging are not unlimited; we must conserve!
  - Bandwidth is attractive for mid- to high-end applications

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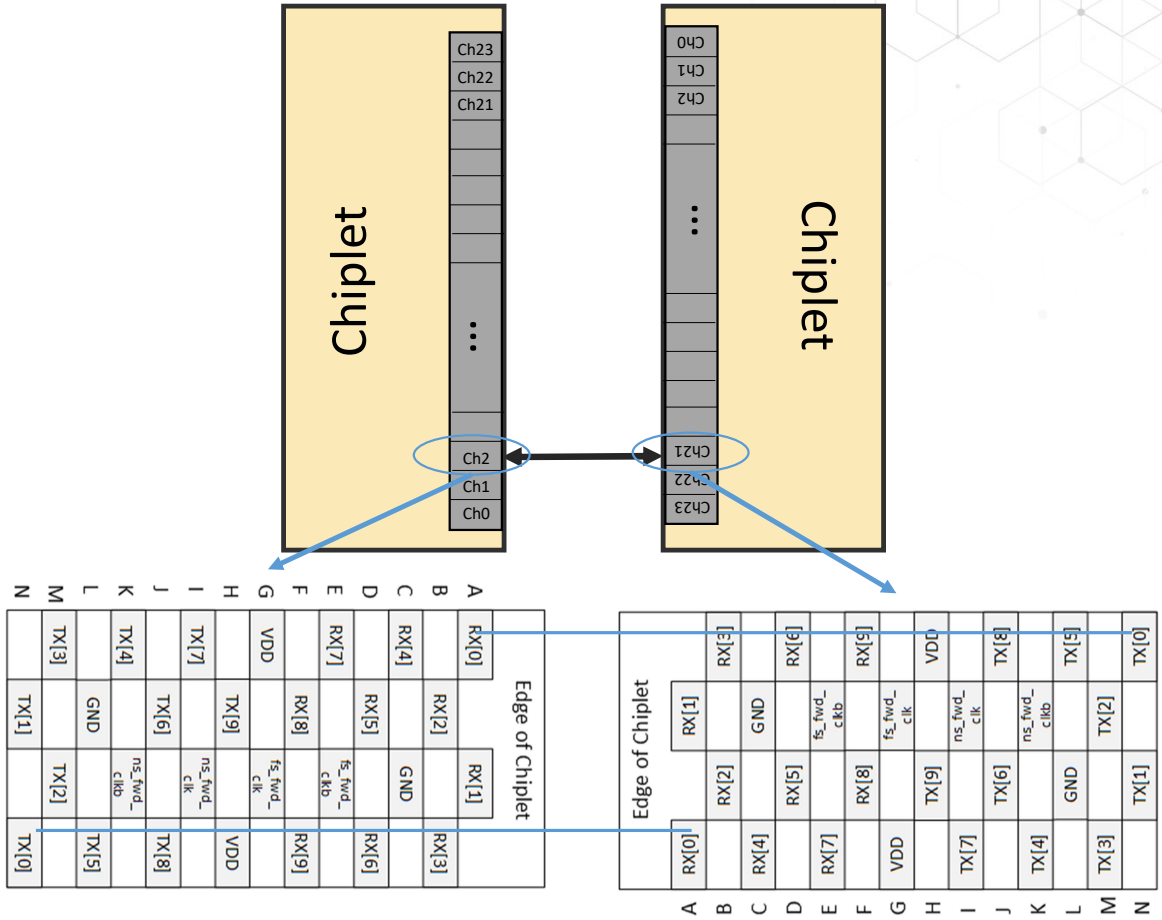
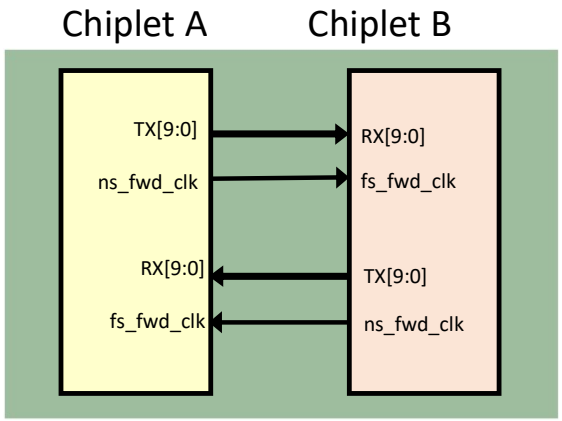
AIB-O Pair

- Common AIB-O configuration is 10 Tx, 10 Rx per channel, 24 channels, at the same AIB 312.48u channel height
  - (10Tx+10Rx)*4Gbps*24 channels = 1920Gbps
  - *Compare to AIB 2.0 (40Tx+40Rx)*4Gbps*24 channels = 7680Gbps*
- Bump map designed for matched trace length between the channel pair

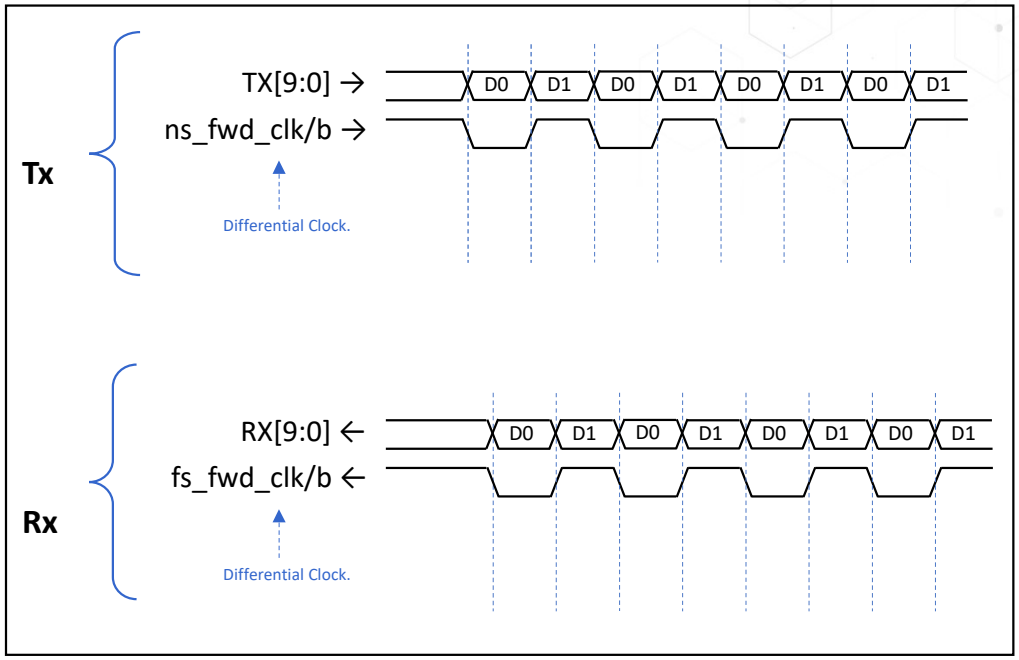


AIB-O Signaling



- AIB-O uses TX data, RX data, clocks
- DDR data transfer
- Full duplex

→ Same as AIB 1.0/2.0!



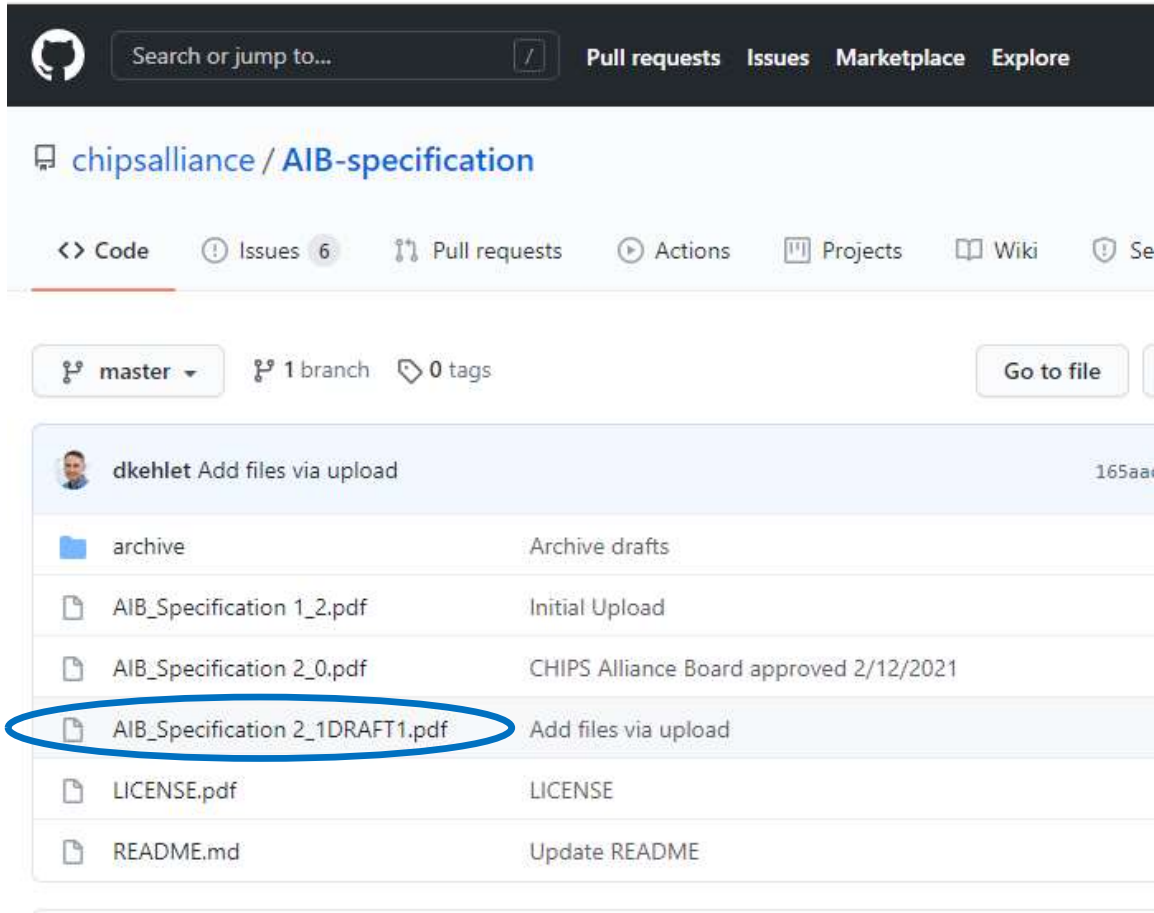
AIB-O Specification

- See the draft specification at:

  https://github.com/chipsalliance/AIB-specification

  AIB_Specification 2_1DRAFT1.pdf, Chapter 7

- Planning to complete by 9/2021



Protocols for Chiplet Interoperability

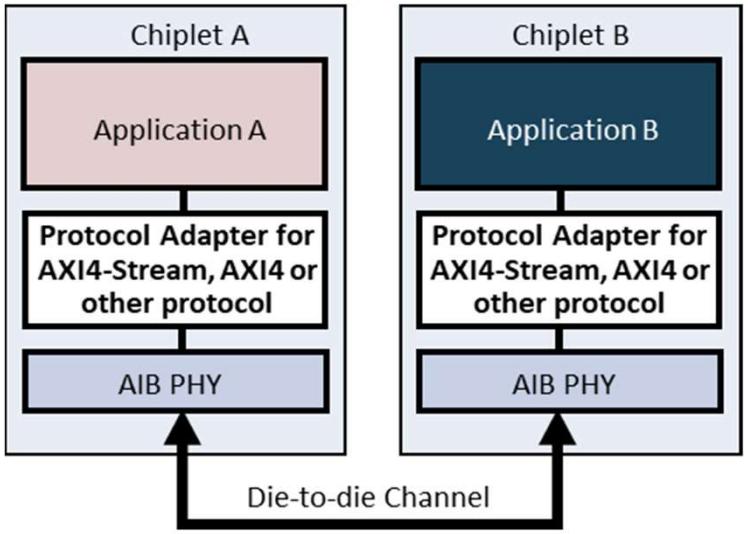
Protocols are the next area of interoperability after the PHY

- The “Data Link” layer in the OSI reference model

Protocol adapters on each side convert the protocol interface to the AIB PHY data wires

The SHIP Chiplet Design Technology project will provide open source hardware adapters

- AXI4-Stream
- AXI4 (Memory Mapped)
- Logical PHY Interface (LPIF) for CXL



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Conclusion

- Standardization with the AIB interface is growing an ecosystem of chiplets, IP, design tools and design services
- Open source enables other companies' silicon to interoperate with my silicon to meet an expanded set of customer requirements

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