



— Workshop —

March 30, 2021

# Workshop Program Agenda

Time (PT UTC-8)	Talk	Speaker	Affiliation
8:00	Welcome / Opening Remarks	Rob Mains	CHIPS Alliance
8:10	Chipyard	Bora Nikolic	UC Berkeley
8:40	RISC-V DV Workgroup Updates	Tao Liu / Matt Cockrell	Google
8:55	Open Source Flows in ASIC & FPGA Development	Michael Gielda	antmicro
9:10	Open-Source AIB Chiplet Ecosystem	David Kehlet	Intel
9:25	OmniXtend Milestone Updates	Dejan Vucinic	Western Digital
9:40	Chisel advances for next-gen SOC Designs	Jack Koenig	SiFive
9:55	Codasip SweRV Core Support Package in a Nutshell	Zdenek Prikyl	Codasip
10:10	An Introduction to the OpenROAD project	Andrew Kahng / Tom Spyrou	OpenROAD
10:40	Open Source FPGA Tooling	Brian Faith	Quicklogic
10:55	Fully Open Silicon Down to the Transistor	Tim Ansell	Google

# CHIPS Alliance

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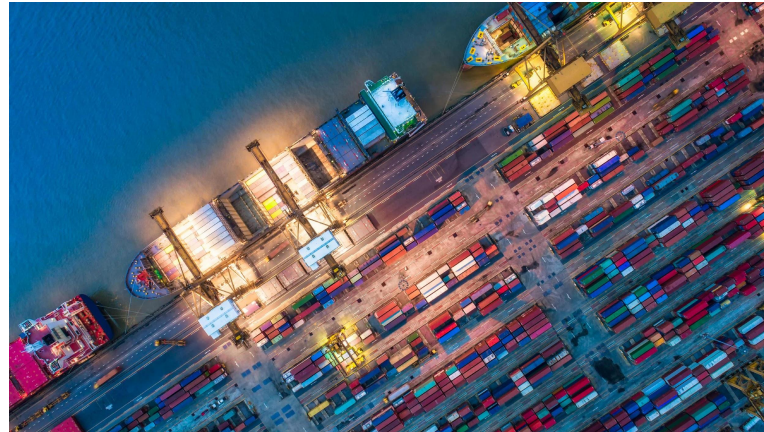




# Industrial Evolution: Siloed to Collaboration



Soup to Nuts Silo: In House



Supply Chain Management: Overseer

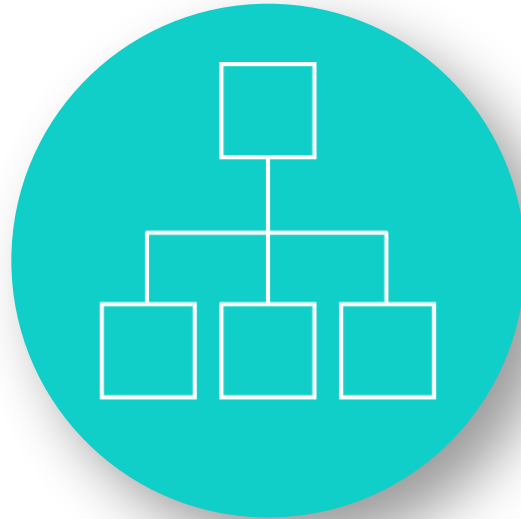


Open Collaboration

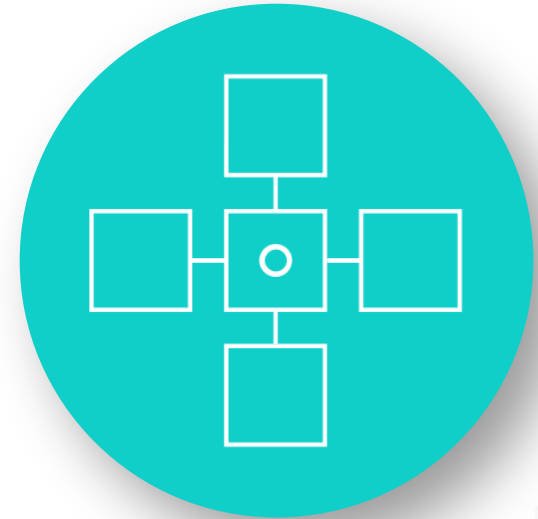
# Compute and Design Challenges



Costs of hardware  
increasing  
significantly

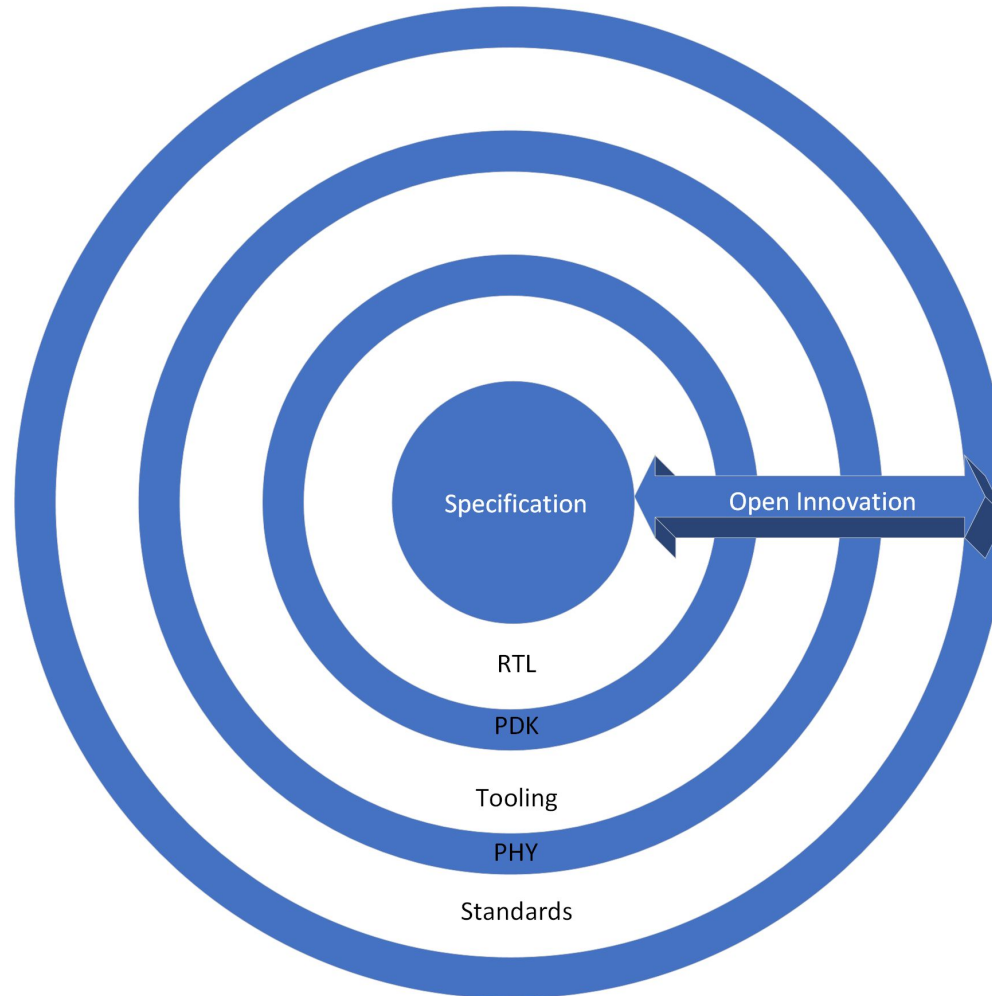


Innovation often stalled  
in corporate structures



Need more  
purpose-built  
architectures

# Concentric Collaborative Innovation: Open Design Ecosystem



Many Contributors

- Individuals
- Universities
- Foundations
- Companies

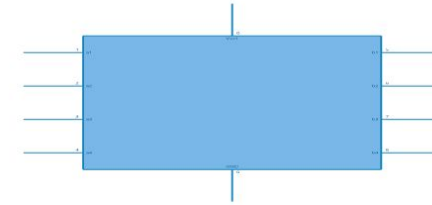
# Open Source Model: IP & Innovation -> Your Product



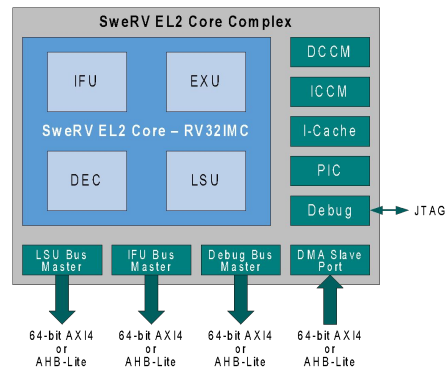
Open IP Catalog



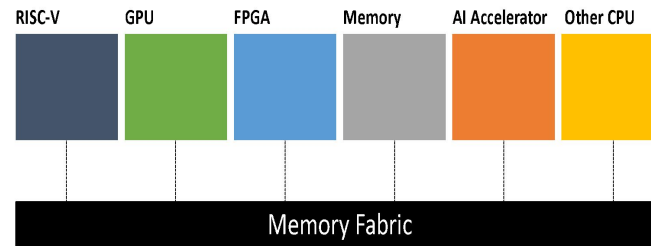
Your Innovation



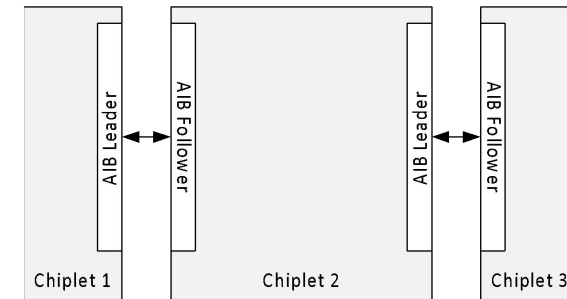
Your Product



SweRV: RISC-V ISA



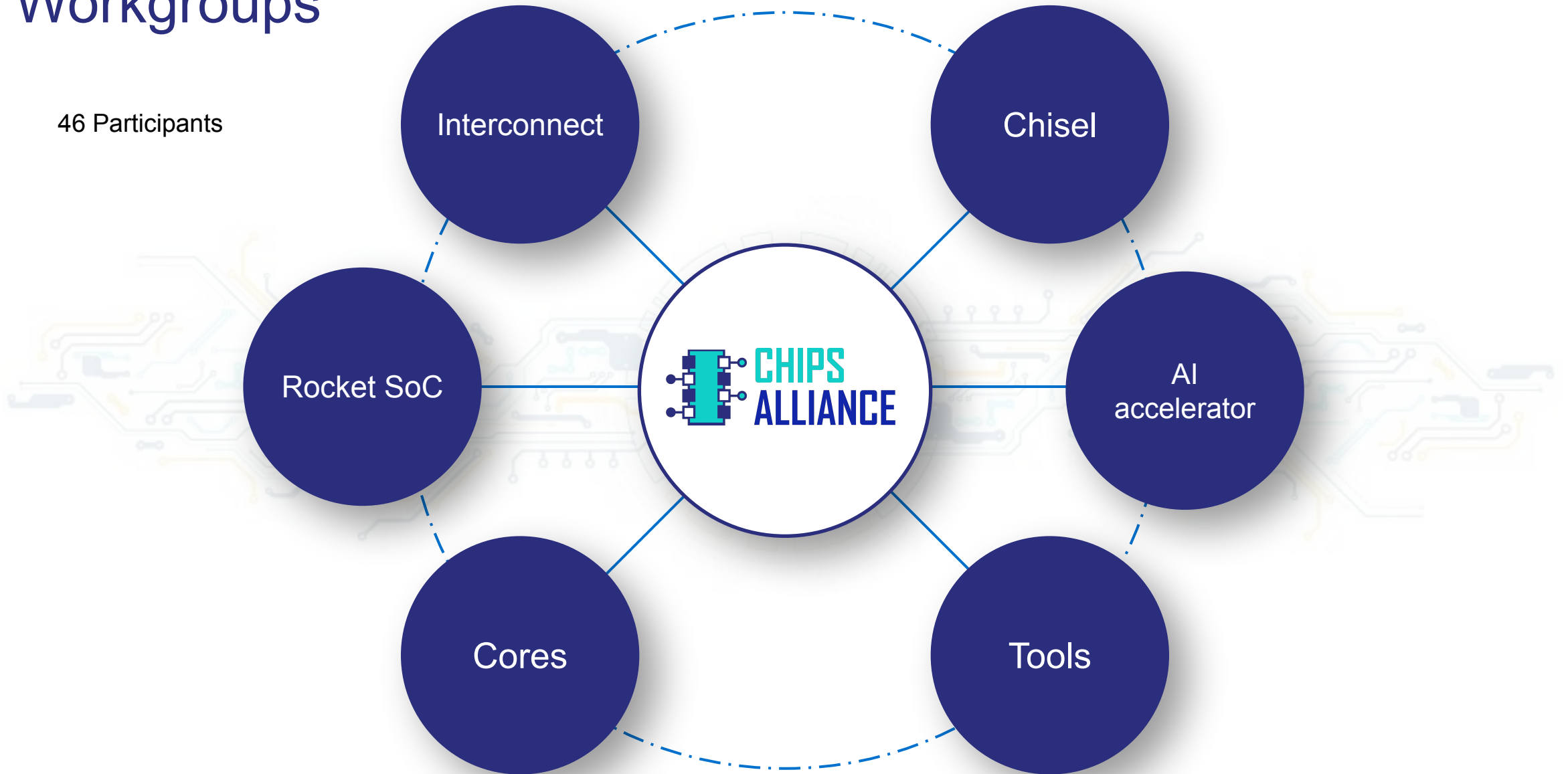
OmniXtend



AIB 2.0: Chiplets

# Workgroups

46 Participants





# Progress & Achievements so far in 2021

- Chiplets: AIB 2.0 Specification Release
  - › Enables system of collaborative PHY IP
  - › Standardized interface protocol
  - › Updated interface with higher performance
- OMNIXtend
  - › Cache coherency fabric
  - › Enables intelligent processor ecosystem
    - › RISC-V, GPU, DPU, ML Accelerators...
  - › CHIPS / RISC-V Collaboration
- Analog Tools Group Formation

# 2021 Goals

- Membership
- Increased Collaboration
  - AI / Automotive / 5G
- IP Contribution
- Menu of Choice for Innovation
- OpenEDA
  - › Architecture, RTL, Verification, Analog, Digital, FPGA
- University
  - › Contest
  - › Mentorship
- Moonshot

# Join the Alliance!

- Share resources to lower the cost of hardware development: digital and analog IP
- Collaborate in developing of open source design tools software, share good practices
- Receive high quality, open source CPU/SoC designs and complex IP blocks
- Grow your business in this forward thinking organization

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