
FrontEnd
OverView
also initiates request to BTB to obtain the takenality
request
response comes ba
BTB
main BTB
BHT
RAS
These 3 modules and interconnections among them are depicted in this post by me: https://github.com/chipsalliance/rocket-chip/issues/2993
decided by icacheParams.latency
request to icache at s0, resp at s1 or s2
ct no parity checking.
checking against the
he organization
ICache
errors
There are error signals sending to BEU through io.errors
Note that when refilling a cache block, there may be D channel error being asserted for some specific reason. There is one extra bit in the tag field of a cache block to stash this error state. When an access hits in that block, a hit is still reported to the initiator, but with ae field being asserted.