

access from the general interface that goes to ITIM(CTRL or MEM; See addrMaybelnScratchpad(io.s1\_paddr)) region always hit, but may return unspecified data





	io.imem.req.valid := take_pc io.imem.req.bits.speculative := !take_pc_wb io.imem.req.bits.pc := Mux(wb_xcpt    csr.io.eret, csr.io.evec, // exception or [m s]ret Mux(replay_wb, wb_reg_pc, // replay	csr.io.evec returns the right redirection addr for interrupt/exception and the ebreak/ecall/ eret case	a csr access op can be detected at ID, but only send this request to CSR module at WB stage. The CSR responds at the same cycle.	csr.io.rw.addr := wb_reg_inst(31,20) csr.io.rw.cmd := CSR.maskCmd(wb_reg_ valid, wb_ctrl.csr) csr.io.rw.wdata := wb_reg_wdata	the CSR module then docodes the op, and io. eret may therefore be asserted	io.eret := insn_call    insn_break    ins io.evec := tvec
-		for replay, just redirect to the pc of insn in WB stage				
	mem_npc)) // nosh or branch misprediction	mem_npcit's important to note that this s	also covers the			
se,m(s)tval are among io_dec.csr >= CSRs. rs will flush the pipeline.		flush case? why flush is needed	erstanding the d?			

