CBU5000 UWB SoC Family

V210 DATASHEET V1.0

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1 IC description

CBU5000V210 is a single-chip CMOS SoC with UWB(6~9GHz), BLE, and a 32-bit microprocessor (MCU) integrated.

The UWB system has a 1T3R architecture, which support ranging, 3D AOA, and radar function. The transmitter has a peak output power of 12dBm, and features a digital architecture to achieve low power consumption. A TRSW is integrated on chip for TX and RX0 to share one antenna. On chip matching are provided for all the transmitter and receiver channels so that they can be directly connected to 50Ω antennas and/or filters.

The BLE system supports BLE 5.0 with low power consumption, which enables the chip to support a battery life that is much longer than UWB only solutions.

The SOC integrates a high performance 32-bit MCU, hardware security platform and abundant function blocks such as timer, UART, SPI, I2C, making the chip ready for applications such as communication, ranging, IoT etc. It is possible to bypass the MCU to work in an UWB transceiver mode.

The whole chip shares one 32MHz crystal oscillator to reduce the BOM. On chip voltage and temperature monitoring are provided, and a 10-bit ADC is provided to support external sensors.

The high-level function diagram is shown as below.

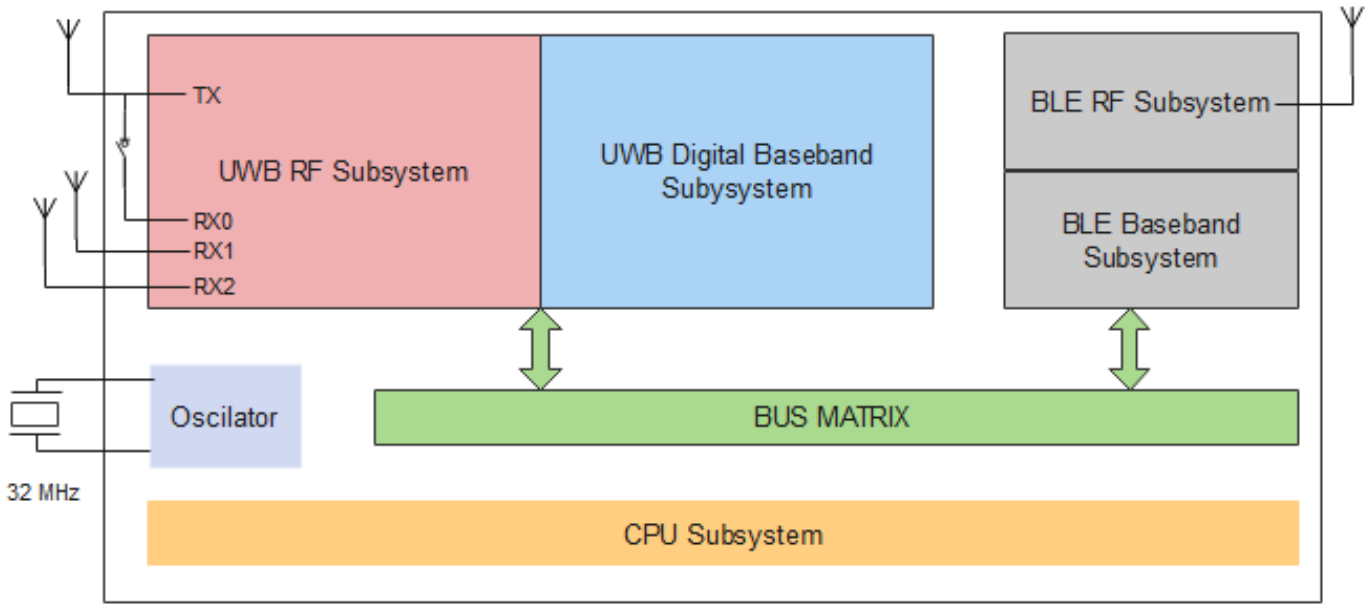


Figure 1-1 High Level Function Diagram of CBU5000V210

1.1 Key Features

1.1.1 General

- Compliant with IEEE 802.15.4z, IEEE 802.15.4-2015, and FiRa standards
- Support band group two from 6 to 9 GHz, i.e., channel 5, 6, 8, 9, 10
- Support packet length up to 4095 bytes
- Support various data rates from 850Kbps, 6.8Mbps, 7.8Mbps, 27.2Mbps, and 31.2Mbps
- Support STS packet configuration 0, 1 & 3, with integrated AES-128 for secure ranging.
- Support both SoC mode and transceiver mode
- Support two-way ranging (TWR), and time difference of arrival (TDOA)
- Support 3D angle of arrivals (AOA) with 1 TX and 3 RX
- Hardware based security architecture
- SPI command interface to the external host CPU with clock up to 32 MHz
- QSPI controller to support external flash up to 1Mbytes with speed of 64 MHz
- Low BOM cost due to the high integration of SoC

1.1.2 Special

- Fully integrated single-chip dual-transceivers SoC, i.e., IR-UWB and BLE
    - Integrated FiRa Framework API with both UWBS and OOB
- 32-Bit MCU at various rate, 16, 32, 64, and 128 MHz
    - Enable optimization between high performance & low power consumption
- Accurate estimation of crystal frequency offset
    - Enable accurate single-side two-way ranging (SS-TWR) to save time & power
- Configurable TX Pulse Shaping Module
    - Enable device to transmit at max regulatory power (-41dBm/MHz) for Channel 10 in China.
- RADAR mode to cater for the rising demand on various applications
    - Presence detection, fall detection, health monitoring
- Long range at max transmit power
    - The coverage for communication and ranging is able to reach 360 meters
- Short-frame Ranging Structure
    - 16-symbol preamble length to increase the ranging rate or reduce the power consumption

1.2 Application

1.2.1 Target Device

- Smartphone
- Anchor/Tag
- RADAR Device

1.2.2 Use cases

- Smart city & mobilities
  - Indoor navigation
  - Ticket validation
  - Parking Garage Access Control
  - Vehicle digital key
- Smart retail
  - Targeted Marketing
  - Tap-free mobile payment
  - Foot traffic and shopping behaviour analysis
- Smart home
  - Gesture-based control
  - Residential access control
  - Presence based device activation
- Smart Industrial
  - Social distancing
  - Patient tracking
  - Geo-fencing

2 Electrical Specification

2.1 Nominal Operating Conditions

Table 2-1: Nominal Operating Conditions

Parameter	Min	Typ.	Max	Units	Notes
Operating temperature	-40		85	°C	
Storage temperature	-65		150	°C	
Supply voltage VDD1a/b	1.62	3.3	3.6	V	Max current 20mA
Supply voltage VDD2a/b/c	1.42	1.5	3.6	V	Max current 500mA for 3RX

2.2 UWB Transmitter Characteristics

Table 2-2: UWB Transmitter AC Characteristics

Parameter	Min	Typ.	Max	Units	Notes
RF frequency	6489.6		8486.4	MHz	
Channel bandwidth		499.2		MHz	
Output power	-18		+12	dBm	Continuous Wave
	-61		-31	dBm/MHz	Mean PRF = 15.6 MHz
	-55		-25	dBm/MHz	Mean PRF = 62.4 MHz
	-52		-22	dBm/MHz	Mean PRF = 124.8 MHz
	-49		-19	dBm/MHz	Mean PRF = 249.6 MHz

2.3 UWB Receiver Characteristics

Table 2-3: UWB Receiver AC Characteristics (RX0)

Parameter	Min	Typ.	Max	Units	Notes
RF frequency	6489.6		8486.4	MHz	
Channel bandwidth		499.2		MHz	
Input P1dB		-12		dBm	
Sensitivity, 850Kbps		-101.5		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 6.8Mbps		-95.0		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 7.8Mbps		-95.5		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 27.2Mbps		-92.0		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 31.2Mbps		-92.5		dBm	Preamble length=64, SFD length=8, PER<=1%

Table 2-4: UWB Receiver AC Characteristics (RX1 & RX2)

Parameter	Min	Typ.	Max	Units	Notes
RF frequency	6489.6		8486.4	MHz	
Channel bandwidth		499.2		MHz	
Input P1dB		-13		dBm	
Sensitivity, 850Kbps		-102.5		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 6.8Mbps		-96.0		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 7.8Mbps		-96.5		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 27.2Mbps		-93.0		dBm	Preamble length=64, SFD length=8, PER<=1%
Sensitivity, 31.2Mbps		-93.5		dBm	Preamble length=64, SFD length=8, PER<=1%

Note 1: All the measurements above are collected by using a payload length of 20 bytes, CFO offset of +/-40ppm.

Note 2: RX1 and RX2 sensitivity is around 1.0dB better than RX0 because they do not have the loss of TRSW.

2.4 UWB Ranging & PDoA Characteristics

Table 2-5: Ranging & PDoA accuracy

Parameter	Standard Deviation	Condition	Notes
TWR ranging accuracy	1cm	Within 15 meter in a line-of-sight channel	Preamble length=64
TWR ranging accuracy	2cm	Within 50 meter in a line-of-sight channel	Preamble length=64
3D AOA accuracy	1°	Within ±30° (FOV) in a line-of-sight channel	Preamble length=64
3D AOA accuracy	2°	Within ±50° (FOV) in a line-of-sight channel	Preamble length=64

2.5 BLE Transmitter Characteristics

Table 2-6: BLE transmitter AC Characteristics

Parameter	Min	Typ.	Max	Units	Notes
RF frequency	2400		2484	MHz	
Channel bandwidth		1	2	MHz	
Output power	-20	0	3	dBm	

2.6 BLE Receiver Characteristics

Table 2-7: BLE Receiver AC Characteristics

Parameter	Min	Typ.	Max	Units	Notes
RF frequency	2400		2484	MHz	
Sensitivity, 1Mbps		-96		dBm	
Sensitivity, 2Mbps		-93		dBm	
Maximum receiving power		0		dBm	

2.7 Power Consumption Characteristics

The current consumption data for various mode is shown in the table below.

Table 2-8: Current Consumption Characteristics with Buck

(Condition: Temp = 25, Voltage = 3.3 V, TX Load Impedance = 50 ohm)

System	Mode	Current Consumption	Unit	Condition
UWB+CPU	UWB TX	42	mA	@ -19 dBm/MHz, MPRF = 249.6MHz
	UWB TX	31		@ -25 dBm/MHz, MPRF = 62.4MHz
	UWB TX	23		@ -41 dBm/MHz, MPRF = 62.4MHz
	UWB RX (1 RX)	80		
	UWB RX (3 RX)	189		
	UWB Standby	8.1		
BLE+CPU	BLE TX	13	mA	@ 3dBm
	BLE RX	8.9		
	BLE Standby	6.6		
CPU	Active	4.7	mA	@ 64MHz
	Sleep	1.2		
	Deep Sleep	3.8	uA	
	Power-Down	150	nA	

2.8 SPI Characteristics

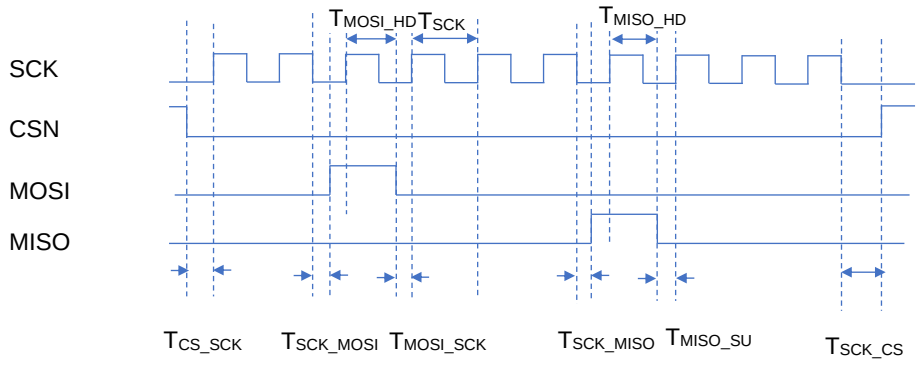


Figure 2-1: SPI Timing Diagram

Table 2-9: SPI Timing Characteristics in Master Mode

Parameter	Min	Typ.	Max	Units	Notes

T_{SCK}			32	MHz	SCK clock period
T_{CS_SCK}	16			ns	Delay from falling edge of CS to rising edge of SCK
T_{SCK_CS}	8			ns	Delay from falling edge of SCK to rising edge of CS
T_{SCK_MOSI}			1	ns	Delay from falling edge of SCK to valid MOSI
T_{MISO_SU}	0			ns	MISO setup requirement
T_{MISO_HD}	4			ns	MISO hold requirement

Table 2-10: SPI Timing Characteristics in Slave Mode

Parameter	Min	Typ.	Max	Units	Notes
T_{CS_SCK}	1			ns	CS setup requirement
T_{SCK_CS}	0			ns	CS hold requirement
T_{MOSI_HD}	1	-		ns	MOSI hold requirement
T_{MOSI_SCK}	1			ns	MOSI setup requirement
T_{SCK_MISO}			6	ns	MISO delay from falling edge of SCK

2.9 UART Characteristics

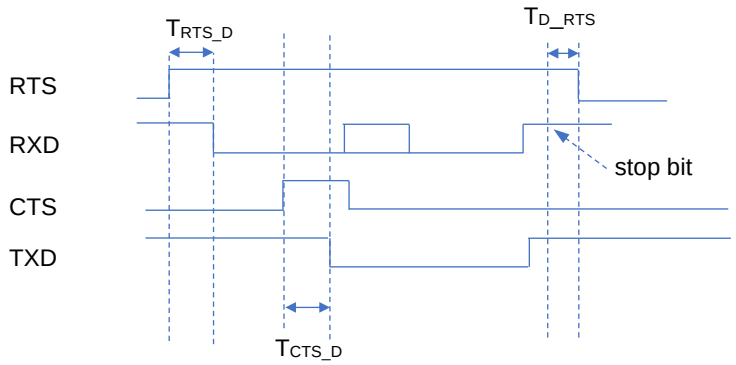


Figure 2-2: UART Timing Diagram

Table 2-11: UART Timing Characteristics

Parameter	Min	Typ.	Max	Units	Notes
T_{RTS_D}	0.5			symbol	
T_{D_RTS}			68	ns	
T_{CTS_D}	18		130	ns	

2.10 I2C Characteristics

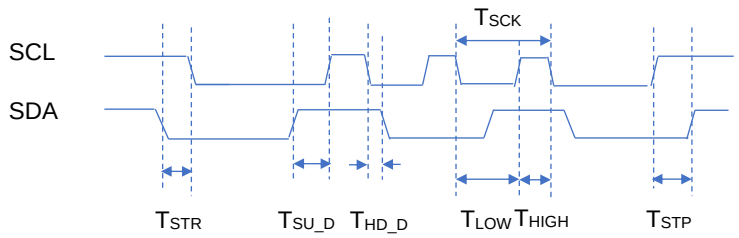


Figure 2-3: I2C Timing Diagram

Table 2-12: I2C Timing Characteristics

Parameter	Min	Typ.	Max	Units	Notes
T_{SCK}	64		65536	ns	
T_{STR}	16			ns	Hold time of START
T_{STP}	16			ns	Hold time of STOP
T_{SU_D}	5			ns	Setup time of SDA
T_{HD_D}	0			ns	Hold time of SDA
T_{HIGH}	16			ns	High period of SCL
T_{LOW}	16			ns	Low period of SCL

2.11 GPIO Characteristics

Table 2-13: GPIO DC Characteristics

Parameter	Min	Typ.	Max	Units	Notes
V_{IL}	-0.3		0.35*VDDIO	V	Input Low Voltage
V_{IH}	0.65*VDDIO		3.6	V	Input High Volrage
V_T	1.58	1.71	1.86	V	Threshold Point
V_{T+}	1.58	1.71	1.86	V	Schmitt Trigger Low to High Threshold Point
V_{T-}	1.11	1.23	1.37	V	Schmitt Trigger High to Low Threshold Point
V_{TPU}	1.57	1.7	1.85	V	Threshold Point with Pull-up Resistor Enabled
V_{TPD}	1.6	1.72	1.87	V	Threshold Point with Pull-down Resistor Enabled
V_{TPU+}	1.57	1.7	1.85	V	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled
V_{TPU-}	1.1	1.22	1.36	V	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled
V_{TPD+}	1.6	1.72	1.87	V	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled
V_{TPD-}	1.12	1.24	1.38	V	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled
I_I			±10	μA	Input Leakage Current @ V_I=3.3V or 0V
I_{OZ}			±10	μA	Tri-state Output Leakage Current @ V_O=3.3V or 0V
R_{SPU}	-	-	-	Ω	Strong Pull-up Resistor
R_{PU}	51k	75k	116k	Ω	Pull-up Resistor
R_{PD}	54k	84k	145k	Ω	Pull-down Resistor
V_{OL}			0.4	V	Output Low Voltage
V_{OH}	2.4			V	Output High Voltage
I_{OL}	4.4	7.1	10.1	mA	Low Level Output Current @ V_{OL} (max)
I_{OH}	5.8	11.5	19.5	mA	High Level Output Current @ V_{OH} (max)

2.12 Power on sequence

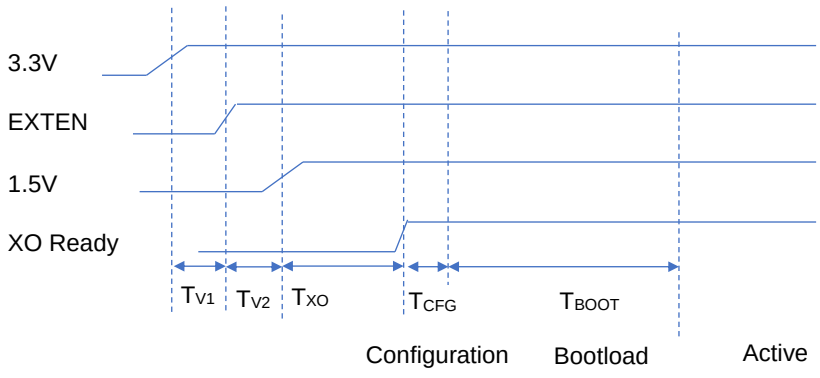


Figure 2-4: Power on Sequence

Table 2-14: Power on Sequence

Parameter	Min	Typ.	Max	Units	Notes
T_{V1}		400		us	Delay from 3.3V to EXTEN
T_{V2}		100		ns	DCDC power on time
T_{XO}		200		us	Delay from 1.5V to XO ready
T_{CFG}			6.938	us	Load efuse configuration
T_{BOOT}			8.197	ms	Load instructions to IBUF

2.13 Reference clock

Parameter	Min	Typ.	Max	Units	Notes
Frequency		32		MHz	
Frequency tolerance	-25		25	ppm	Including temperature variation
Load capacitance		12		pF	
Equivalent Series Resistance	40	-	100	Ω	

2.14 AuxADC Characteristics

Condition: VDD1a=3.3V, ambient temperature 25℃

Parameter	Min	Typ.	Max	Units	Notes
Resolution	-	10	-	bit	
Clock source	-	-	2M	Hz	From digital Support single/continuous sampling
Full-scale voltage	0.9	-	3.3	V	Configurable full-scale voltage of 0.9/1.2/1.5/1.8/2.5/3.3V
DC offset error			1	LSB	After internal calibration
DNL		1.2		LSB	
INL		1.5		LSB	
Input impedance	-	10	-	MΩ	Buffered input
Input capacitance	-	2	-	pF	IO capacitance

2.15 ESD Characteristics

Parameter	Min	Typ.	Max	Units	Notes
HBM		2000		V	All pins
CDM		500		V	All pins

3 Pin description

The chip has an eWLB package with 67 balls and a size of 3.6mm x 3.4mm. The pin names and signal names are illustrated as below.

Pin assignment, top view:

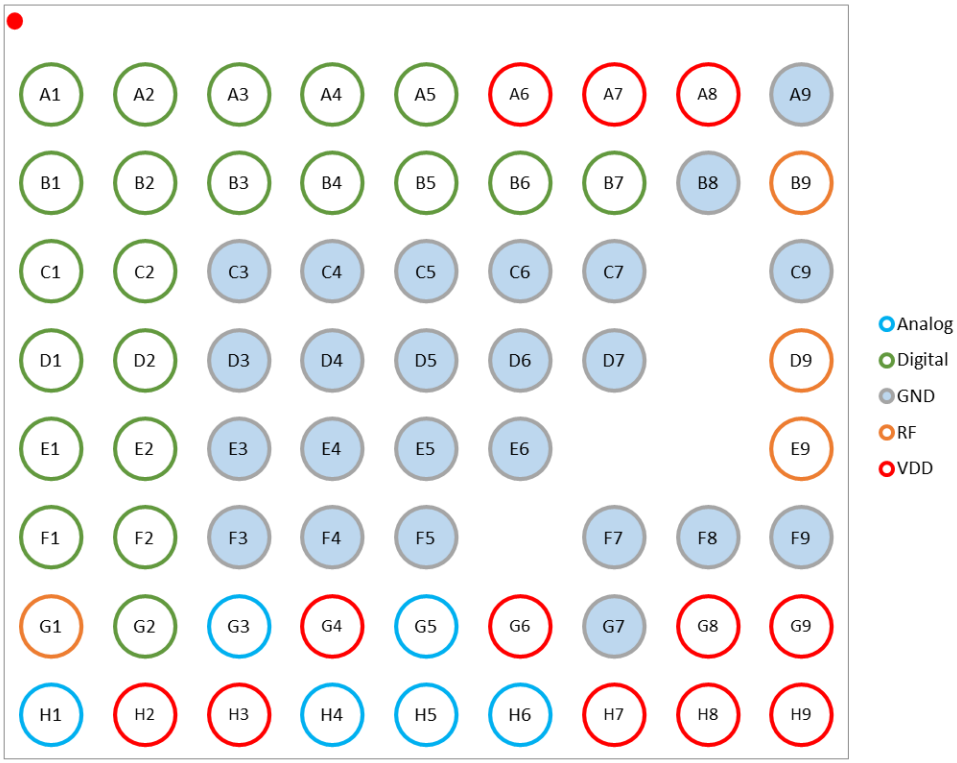


Figure 3-1: Top view of pin assignment

Signal names of pins, top view:

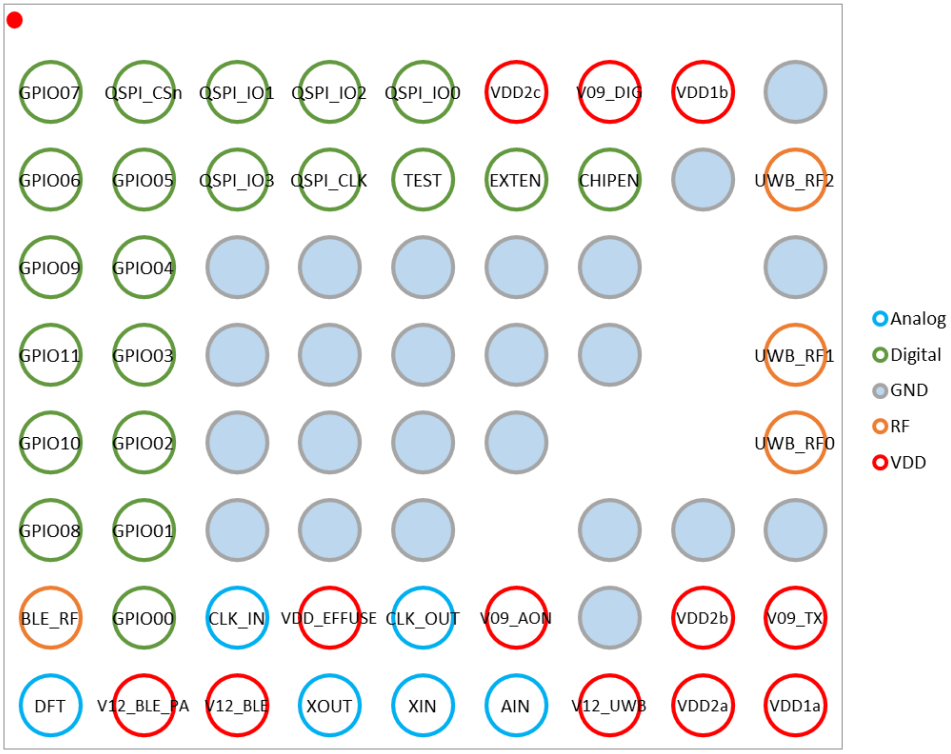


Figure 3-2: Top view of pin signal names

Description of the pins:

Table 3-1: Description of Pins

Pin #	Signal Name	Group	I/O	Voltage(V)			Description
				Min	Typ.	Max	
H6	AIN	Analog	I	0		VDD1a	AuxADC input pin. No connect if not used.
G3	CLK_IN	Analog	I	0		0.9	Test pin. Connect to GND for product.
G5	CLK_OUT	Analog	O	0		0.9	Test pin. Connect to GND for product.
H1	DFT	Analog	O	0		VDD1a	Test pin. No connect for product.
H5	XIN	Analog	I	0		0.9	32MHz XTAL input
H4	XOUT	Analog	O	0		0.9	32MHz XTAL output
B7	CHIPEN	Digital	I	0		VDD1b	Chip enable. 0: disable, 1: enable.
B6	EXTEN	Digital	O	0		VDD1b	DCDC enable for generating VDD2a/b/c
G2	GPIO00	Digital	I/O	0		VDD1b	GPIO
F2	GPIO01	Digital	I/O	0		VDD1b	GPIO
E2	GPIO02	Digital	I/O	0		VDD1b	GPIO
D2	GPIO03	Digital	I/O	0		VDD1b	GPIO
C2	GPIO04	Digital	I/O	0		VDD1b	GPIO
B2	GPIO05	Digital	I/O	0		VDD1b	GPIO
B1	GPIO06	Digital	I/O	0		VDD1b	GPIO
A1	GPIO07	Digital	I/O	0		VDD1b	GPIO
F1	GPIO08	Digital	I/O	0		VDD1b	GPIO
C1	GPIO09	Digital	I/O	0		VDD1b	GPIO
E1	GPIO10	Digital	I/O	0		VDD1b	GPIO
D1	GPIO11	Digital	I/O	0		VDD1b	GPIO
B4	QSPI_CLK	Digital	O	0		VDD1b	QSPI flash clock
A2	QSPI_CSn	Digital	O	0		VDD1b	QSPI flash chip select
A5	QSPI_IO0	Digital	I/O	0		VDD1b	QSPI flash IO
A3	QSPI_IO1	Digital	I/O	0		VDD1b	QSPI flash IO
A4	QSPI_IO2	Digital	I/O	0		VDD1b	QSPI flash IO
B3	QSPI_IO3	Digital	I/O	0		VDD1b	QSPI flash IO
B5	TEST	Digital	I	0		VDD1b	Test mode selection. 0: normal mode, 1: test mode Connect to GND for product.
A9	VSSA	Analog GND	GND		0		Analog GND
B8	VSSA	Analog GND	GND		0		Analog GND
C6	VSSA	Analog GND	GND		0		Analog GND
C7	VSSA	Analog GND	GND		0		Analog GND
C9	VSSA	Analog GND	GND		0		Analog GND
D6	VSSA	Analog GND	GND		0		Analog GND
D7	VSSA	Analog GND	GND		0		Analog GND
E3	VSSA	Analog GND	GND		0		Analog GND
E4	VSSA	Analog GND	GND		0		Analog GND

Pin #	Signal Name	Group	I/O	Voltage(V)			Description
				Min	Typ.	Max	
E6	VSSA	Analog GND	GND		0		Analog GND
F3	VSSA	Analog GND	GND		0		Analog GND
F4	VSSA	Analog GND	GND		0		Analog GND
F5	VSSA	Analog GND	GND		0		Analog GND
F7	VSSA	Analog GND	GND		0		Analog GND
F8	VSSA	Analog GND	GND		0		Analog GND
F9	VSSA	Analog GND	GND		0		Analog GND
G7	VSSA	Analog GND	GND		0		Analog GND
C3	VSSD	Digital GND	GND		0		Digital GND
C4	VSSD	Digital GND	GND		0		Digital GND
C5	VSSD	Digital GND	GND		0		Digital GND
D3	VSSD	Digital GND	GND		0		Digital GND
D4	VSSD	Digital GND	GND		0		Digital GND
D5	VSSD	Digital GND	GND		0		Digital GND
E5	VSSD	Digital GND	GND		0		Digital GND
G1	BLE_RF	RF	I/O		0		RF IO for BLE TX and RX
E9	UWB_RF0	RF	I/O		0		RF IO for UWB TX and RX channel 0
D9	UWB_RF1	RF	I		0		RF input for UWB RX channel 1
B9	UWB_RF2	RF	I		0		RF input for UWB RX channel 2
G4	VDD_EFFUSE	VDD	VDD	1.8	1.8	1.98	1.8V supply for EFFUSE programming. Connect to GND if programming is not required.
H9	VDD1a	VDD	VDD	1.71	3.3	3.6	Supply for analog circuit Connect 1uF+10nF to GND **near the pin**
A8	VDD1b	VDD	VDD	1.71	3.3	3.6	Supply for digital IO, RC32K, AON Connect 1uF+10nF to GND
H8	VDD2a	VDD	VDD	1.42	1.5	3.6	Supply for 1.2V BLE and UWB regulators Connect 1uF+10nF to GND
G8	VDD2b	VDD	VDD	1.42	1.5	3.6	Supply for 0.9V UWB TX regulator Connect 1uF+10nF to GND
A6	VDD2c	VDD	VDD	1.42	1.5	3.6	Supply for 0.9V digital regulator Connect 1uF+10nF to GND
G6	V09_AON	Regulator Cap	I/O	-	0.9	-	0.9V AON regulator output Connect 1uF to GND
A7	V09_DIG	Regulator Cap	I/O	-	0.9	-	0.9V Digital regulator output Connect 1uF+10nF to GND **near the pin**
G9	V09_TX	Regulator Cap	I/O	-	0.93	-	0.9V UWB TX regulator output Connect 1uF+10nF to GND **near the pin**
H3	V12_BLE	Regulator Cap	I/O	-	1.2	-	1.2V BLE regulator output Can share decoupling cap with H2
H2	V12_BLE_PA	Regulator Cap	I/O	-	1.2	-	1.2V BLE regulator output Connect 1uF+10nF to GND
H7	V12_UWB	Regulator Cap	I/O	-	1.2	-	1.2V UWB regulator output Connect 1uF+10nF to GND **near the pin**

4 Functional Description

4.1 Block Diagram

The functional block diagram of CBU5000V210 is shown in Figure 4-1. The chip integrates a 32-bit MCU with security feature, a UWB subsystem, a BLE subsystem and various peripherals such as UART, SPI, I2C.

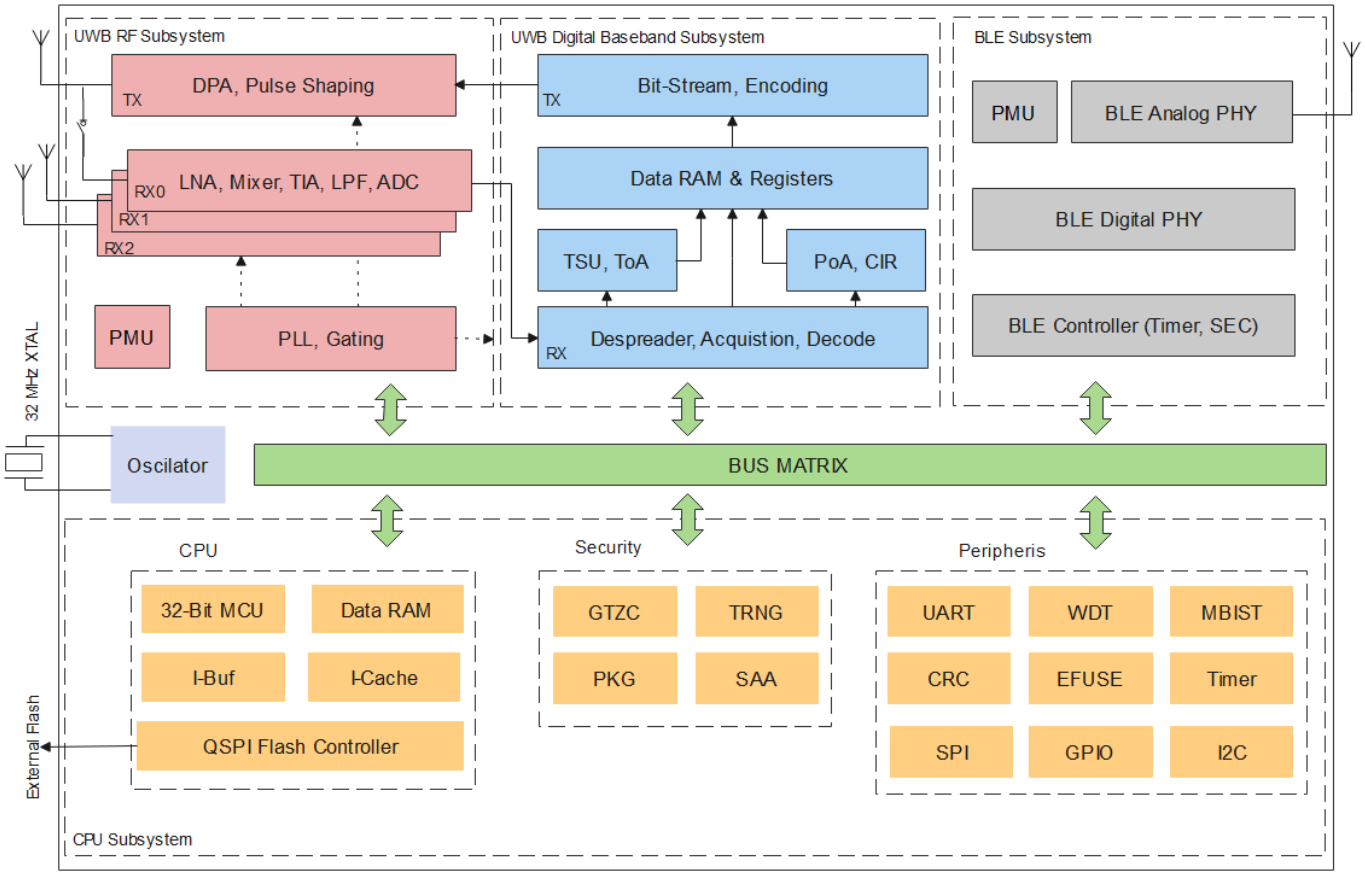


Figure 4-1: Functional Block Diagram of CBU5000V210

UWB subsystem consists of RF subsystem (Front-End) and Digital Baseband subsystem. In RF subsystem, there are three 3 RX chains and 1 TX chain, and an internal TRX switch (TRSW) allows TX and RX0 to share the same antenna. In Digital Baseband subsystem, it does also support 1 TX and 3 RX chains. In the TX chain, the data from upper layer are encoded and send to TX frond-end. In each RX chain, the data frame is captured and decoded based on the digitized samples from the RF chain. Thereafter, channel impulse response (CIR), phase of arrival (PoA), and time of arrival (ToA) are reported, and the information could be used to various applications, e.g., ranging, angle of arrival (AOA), and RADAR sensing.

BLE subsystem provides Bluetooth function for the chip with BLE PHY and BLE Controller integrated and makes the chip to support a battery life.

BUS MATRIX is used to connect UWB and BLE subsystems to the CPU subsystem.

CPU subsystem integrates abundant function blocks including a high performance 32-bit MCU, 2 UART ports, 1 configurable SPI interface, and 1 I2C for peripherals connections to make the chip ready for various applications.

The whole chip adopts single 32MHz crystal oscillator to reduce the BOM.

Please refer to the following subsections for details.

4.2 CPU subsystem

- 32-bit Microprocessor

    - 3-stages pipeline structure
    - Floating point unit
    - Hardware security platform, each device has its own secure settings
    - Little-Endian
    - Default frequency is 64MHz. Configurable operating frequency: 64, 128 MHz
    - SWD interface for debugging
- QSPI Flash controller
    - Support up to 1Mbytes flash memory
    - Working frequency is 64 MHz
- Data RAM
    - Up to 96 KB (4 16-KB and 1 32-KB SRAM)
- ICACHE
    - 16-KB Instruction cache
- IBUF
    - 256-KB Instruction buffer
- DMA
    - Four channel DMA for data transferring
- UART
    - Universal asynchronous receiver/transmitter
    - Communication baud rate can be set by software
    - Dedicated simple DMA to automatically write data to data RAM or read from data RAM
    - 2 UART
    - Each UART can be configured to any two GPIOs
- SPI
    - 1 general SPI, which can work as SPI master or slave
    - Clock frequency can be configured to: 32 MHz, 16MHz, 8MHz, 4MHz, 2MHz, 1MHz, 500KHz, 250KHz, 125KHz.
    - Dedicated simple DMA to automatically write data to data RAM or read from data RAM
    - Can be configured to any 4 GPIOs
- I2C
    - Standard I2C Master
    - Can be configured to any 2 GPIOs
- SAA
    - Security algorithm accelerator
    - Programmable AES 128/192/256 cryptographic function
- PKG
    - Public key generator
- TRNG
    - True Random number generator
- CRC
    - 8, 16, 32-bit CRC with configurable polynomial
    - A dedicated simple DMA is integrated to automatically read data from data memory
- EADC
    - 10bit ADC to sample external analog signal.
    - Sample frequency up to 8 MHz
    - Temperature sensor
- WDT

- Watch-dog timer
- TIMER
  - 4 general purpose timers
  - Able to output PWM signals
- SCR
  - System control register
- GPIO
  - 12 General purpose inputs/outputs
  - Shared with ports of SPI, I2C, UART
  - Shared with internal events
- BLE
  - BLE LL
  - BLE PHY 5.0
- UWB
  - UWB4Z

4.3 UWB subsystem

4.3.1 UWB RF Front-End

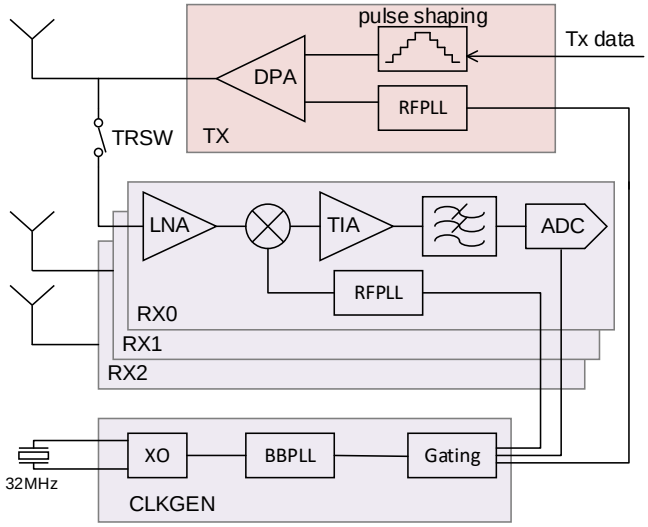


Figure 4-2: Block Diagram of UWB RF Front-End

The UWB PHY has a 1T3R architecture. The transmitter features a digital architecture which greatly reduces power consumption. TRSW and matching are integrated on chip so that the RF ports can be directly connected to 50Ω antennas and/or filters on board. The receiver channel 0 (RX0) shares antenna with TX using a TRSW, whereas RX1 and RX2 are directly connected to antennas with better sensitivity. The UWB subsystem shares XO with BLE and MCU, which reduces the BOM of the system.

4.3.2 UWB Digital Baseband

4.3.2.1 PPDU STS packet structure configurations

This chip support three PPDU STS packet structure configurations, i.e., SP0, SP1 and SP3.

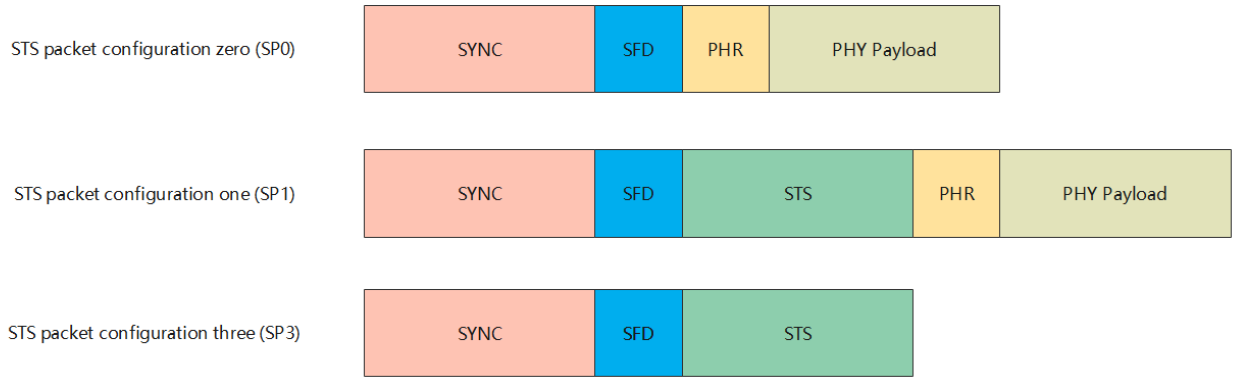


Figure 4-3: Supported STS packet configurations

4.3.2.2 SHR Format

The SHR contains SYNC and SFD. This chip support preamble code index 1 to 24 from IEEE 802.15.4-2020 (Legacy Mode) HRP UWB and 25-31 from IEEE 802.15.4z (4z Mode) HRP UWB standards.

Table 4-1: Supported Preamble Codes

Mode	Preamble Code Index	Code Length	Code Spreading Factor	Symbol Duration (ns)
Legacy	1 to 8	31	16	993.59
Legacy / 4z: BPRF	9 to 24	127	4	1017.63
4z: HPRF	25 to 32	91	4	729.17

This chip supports all the SFD sequences as shown in the table below. The SFD #0 is defined IEEE 802.15.4-2015, SFD #1, #2, #3 are defined in IEEE 802.15,4z. They are mandatory for HRP-ERDEV.

Table 4-2: Supported SFD Sequence

SFD #	SFD Length	SFD Sequence
0	8	[0 +1 0 -1 +1 0 0 -1]
1	4	[-1 -1 +1 -1]
2	8	[-1 -1 -1 +1 -1 -1 +1 -1]
3	16	[-1 -1 -1 -1 -1 +1 +1 -1 -1 +1 -1 +1 -1 -1 +1 -1]

4.3.2.3 PHR Rate

This chip supports the PHR coding rate of 850Kbps and 6.81Mbps for HRP UWB BPRF mode as defined in IEEE 802.15.4z standards.

4.3.2.4 Data Rate

This chip supports IEEE802.15.4-2015 HRP UWB standard with bit rates 850Kbps, 6.81Mbps and 27.2Mbps and Mean PRF values of 15.6MHz and 62.4MHz.

This chip supports IEEE802.15.4z HRP UWB standard BPRF mode with bit rates 6.81Mbps and Mean PRF values of 62.4Mbps.

This chip supports IEEE802.15.4z HRP UWB standard HPRF mode with bit rates 6.81Mbps, 7.8Mbps, 27.2Mbps and 31.2MBps and Mean PRF values of 124.8MHz and 249.6MHz.

Table 4-3: Supported Mean PRF & Data Rate

Mean PRF (MHz)	Data Rate (Mbps)
15.6	0.85, 6.81, 27.2
62.4	0.85, 6.81, 27.2
124.8	6.81, 7.8
249.6	27.2, 31.2

4.3.2.5 Data Length

This chip supports the maximum PSDU length of 127 Bytes as defined in IEEE802.15.4-2015 and IEEE 802.15.4z HRP UWB BPRF mode.

This chip supports the maximum PSDU length of 4095 Bytes as defined in IEEE 802.15.4z HRP UWB HPRF mode.

4.3.2.6 STS Format

This chip supports STS for both BPRF and HPRF mode for HRP-ERDEV.

Table 4-4: Supported STS Format

HRP-ERDEV	Delta Length	PRF (MHz)	Length of active segments in the unit of 512 chips	Number of segments
BPRF mode	8	62.4	64	1
HPRF mode	4	124.8	32, 64 ,128	1, 2

4.3.2.7 Ranging & 3D PDoA

The chip supports accurate ranging in multipath & non-line-of-sight (NLOS) environment through leading edge detection and interpolation. Its first-path dynamic range is more than 30dB.

With 1T3R architecture, this chip supports 3D PDoA by using single frame.

4.3.2.8 RADAR

The chip supports RADAR to detect surrounding reflection signals based on channel information, i.e., Channel Impulse Response. The dynamic range is 37dB and the sensitivity reaches -103dBm.

4.4 BLE subsystem

The BLE subsystem consists of BLE PHY and BLE controller.

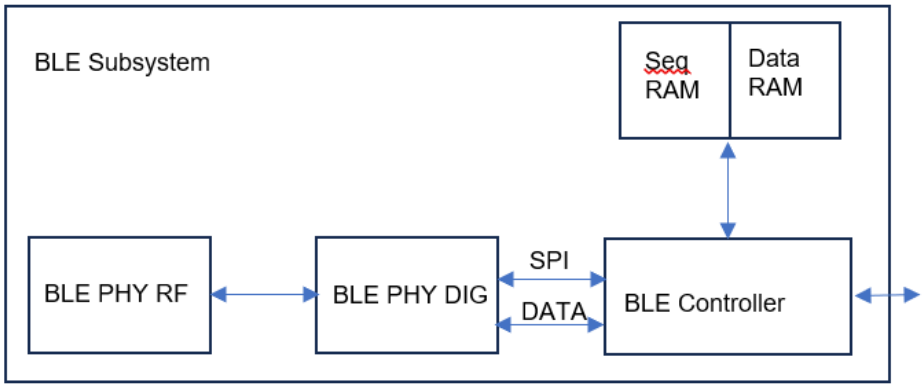


Figure 4-4: Block Diagram of BLE Subsystem

4.4.1 BLE PHY

The BLE PHY RF front-end includes a RF transceiver composed of a frequency synthesizer, PA and receiver. The frequency synthesizer shares reference clock with UWB. TRSW and matching for TX and RX of the BLE are also implemented on chip.

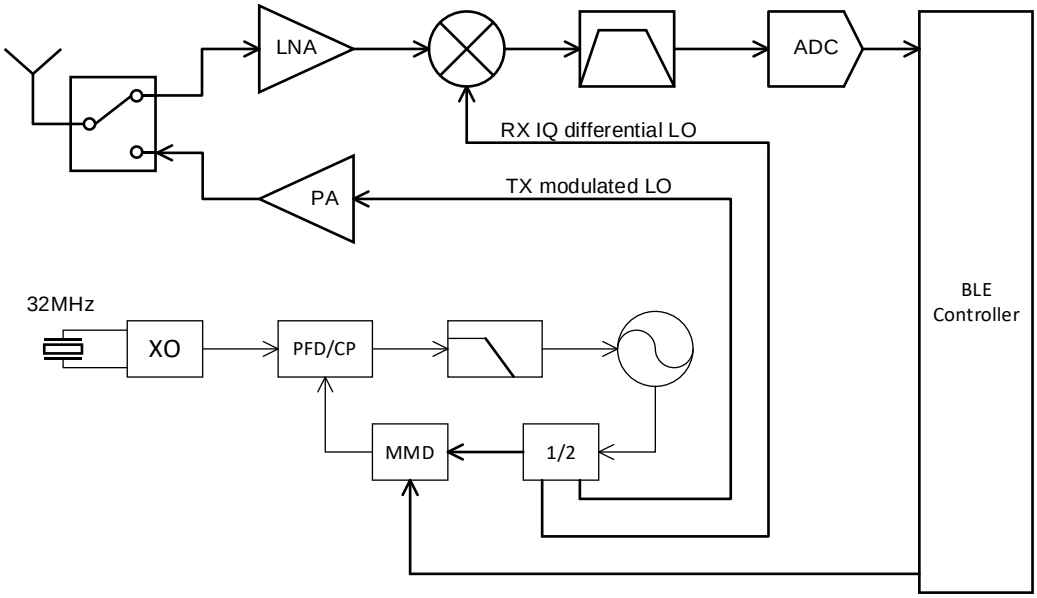


Figure 4-5: Block Diagram of BLE PHY

BLE PHY digital includes the MODEM and auto-calibration function. It is configurable via SPI interface by BLE controller.

4.4.2 BLE Controller

The BLE controller provides the Link Layer (LL) function that complies with the Bluetooth Core specification, version 5.0. It is designed to interface with the BLE PHY to provide a complete solution for a BLE subsystem. The following BLE packet format is supported.

Figure 4-6: BLE Packet Format

4.5 ADC_aux and voltage monitoring

The ADC_aux has a 10-bit resolution, and has an input amplifier with adjustable gain and voltage shifting. The capability to adjust gain and shift middle voltage enables the ADC to have both a wide input voltage range (0 to VDD1a), and also a fine resolution (0.2mV), making it ideal for detecting output voltage of various sensors.

The input of the ADC can be connected to the pin Ain or internal voltages. When internal voltages VDD1a and VDD2a are connected to the ADC, it functions as a voltage monitor for the system.

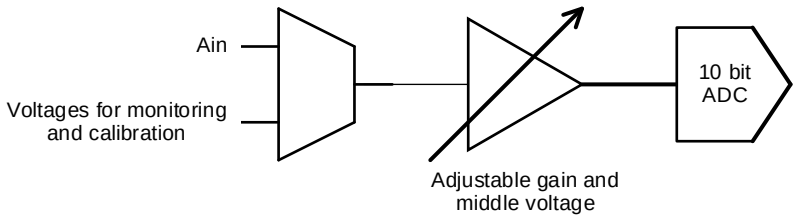


Figure 4-7: Block Diagram of ADC_aux and Voltage Monitoring

4.6 Temperature sensing

A temperature sensor with resolution better than 0.5°C is implemented on chip, and the offset of the temperature sensor can be calibrated.

5 Operation Mode

5.1 Overview

The chip has defined the following power states:

Table 5-1 Chip Power States

POWER STATES	DESCRIPTION
POWER-DOWN	The chip is power down, and can only be waked up by external chip enable pin.
DEEPSLEEP	The chip except AON is power down. Only AON is power on. The timer inside AON is used to wake up the chip to active state.
SLEEP	AON and basic CPU subsystem are power on. MCU core is power off, I-Buf, I-Cache and data ram can be in retention mode or power off based on the system register setting. The timer inside AON is used to wake up the chip to active state.
ACTIVE	The SOC is power on and in active mode. The chip is ready to enter various function modes. In transceiver mode, the MCU core is in power off state. In SOC mode, the MCU is power on.
BLE	Active state and BLE is power on.
UWB	Active state and UWB is power on

5.2 Operation state transition

Always-on module (AON) is responsible for the power management of the chip, which includes the sequence of power on, sleep and deep sleep. The chip will enter to ACTIVE state after power on.

In TRX mode, the chip is in ACTIVE state with MCU power off after wakeup from SLEEP, DEEPSLEEP or POWER-DOWN mode. BLE and UWB can be activated or power off by configuring registers in SCR via SPICMD interface.

In SOC mode, the chip enters ACTIVE state with MCU power on after wakeup from SLEEP, DEEPSLEEP or POWER-DOWN state. In this state, SOC automatically loads boot codes from flash and stores them in instruction buffer, then executes the codes from the instruction buffer. BLE and UWB can be activated or power off by firmware or software configuring registers in SCR.

In ACTIVE state, forcing the external chip enable pin to 0 is used to force the chip to POWER-DOWN state. Forcing this pin to 1 enable the chip back to ACTIVE state.

The chip can enter SLEEP or DEEPSLEEP state by configuring the corresponding SCR registers. The timer inside AON is used to wake up the chip to ACTIVE state.

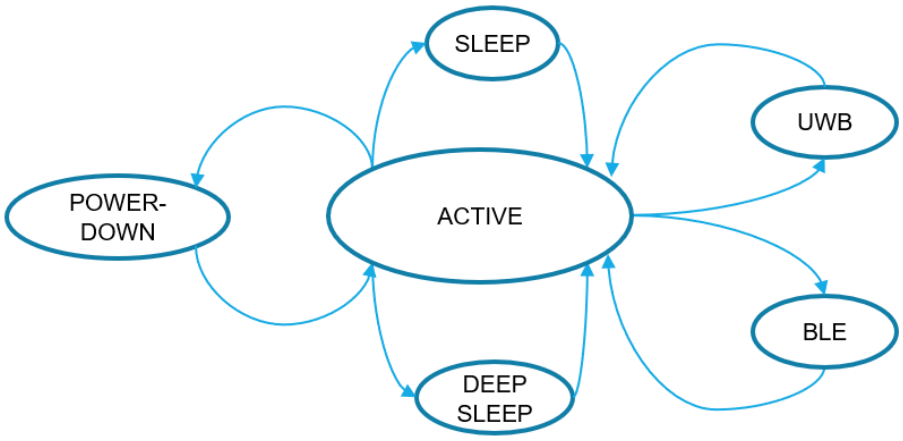


Figure 5-1: Block Diagram of State Transition

6 Powering CUB5000V210

6.1 Power options

This block diagram shows the internal power distribution within the CBU5000V210:

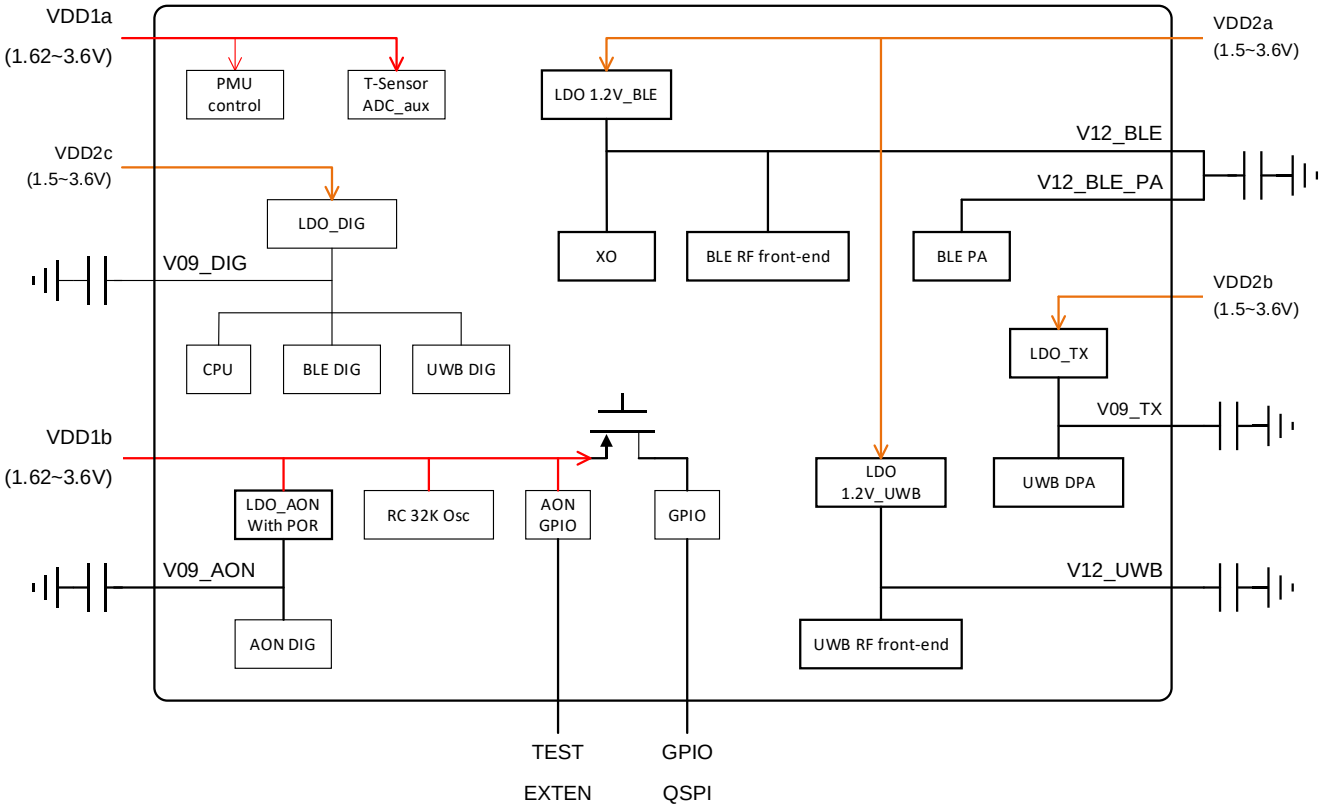


Figure 6-1: Block Diagram of Internal Power Distribution

Powering CBU5000V210 may choose the scheme of minimum BOM, in which only one supply of 1.62~3.6V are necessary, or choose the scheme of low power consumption, in which a Buck convertor with an output voltage of 1.5V is required for VDD2a/b/c. The pin VDD18_EFFUSE can be connected to GND as effuse is already programmed.

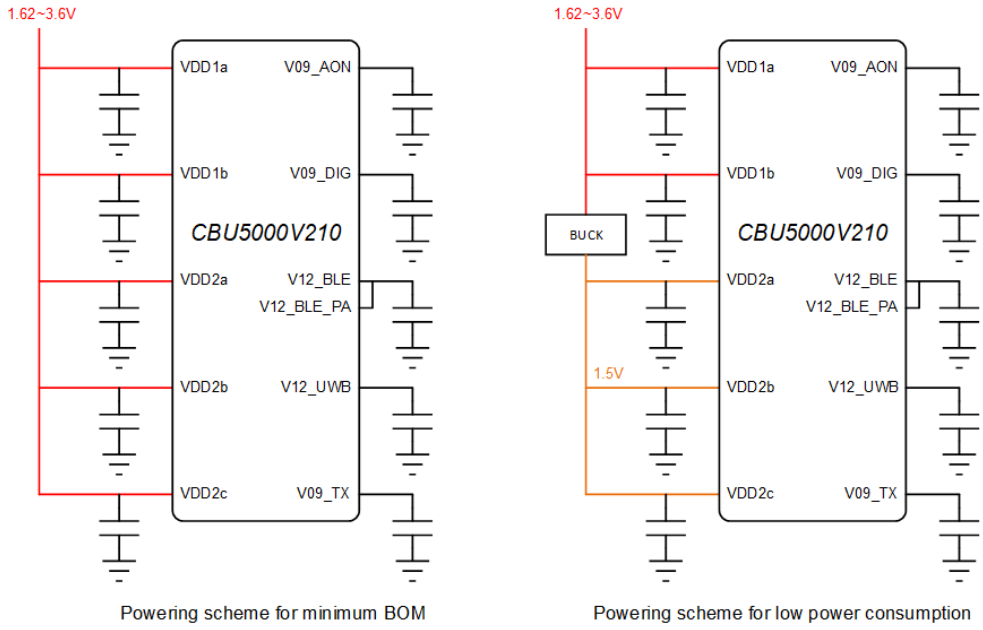


Figure 6-2: Powering Schemes of minimum BOM and Lower Power Consumption

6.2 Typical power mode switch

The chip can enter CPU-On mode from either DEEPSLEEP (DS) or SLEEP mode. Once in CPU-On mode, the chip can enter BLE-On, and/or UWB-On mode, depends on the use scenarios. The chip can enter SLEEP mode to save power if there is no activity for a short period, and wakeup quickly from SLEEP mode. The chip can enter DS mode to save power further if there is no activity for a long period, and wakeup relatively slowly from DS mode.

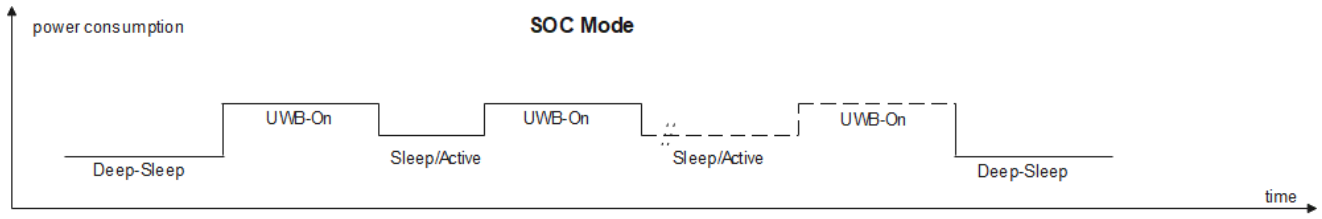


Figure 6-3: Examples of power mode switching

6.3 UWB typical power profiles

In the figure below, the power profile of the initiator for single side two-way ranging (SS-TWR) is presented. The chip is waked up from Deep-Sleep mode to Active mode. SS-TWR is conducted thereafter, and the peak current consumption is stated for each mode.

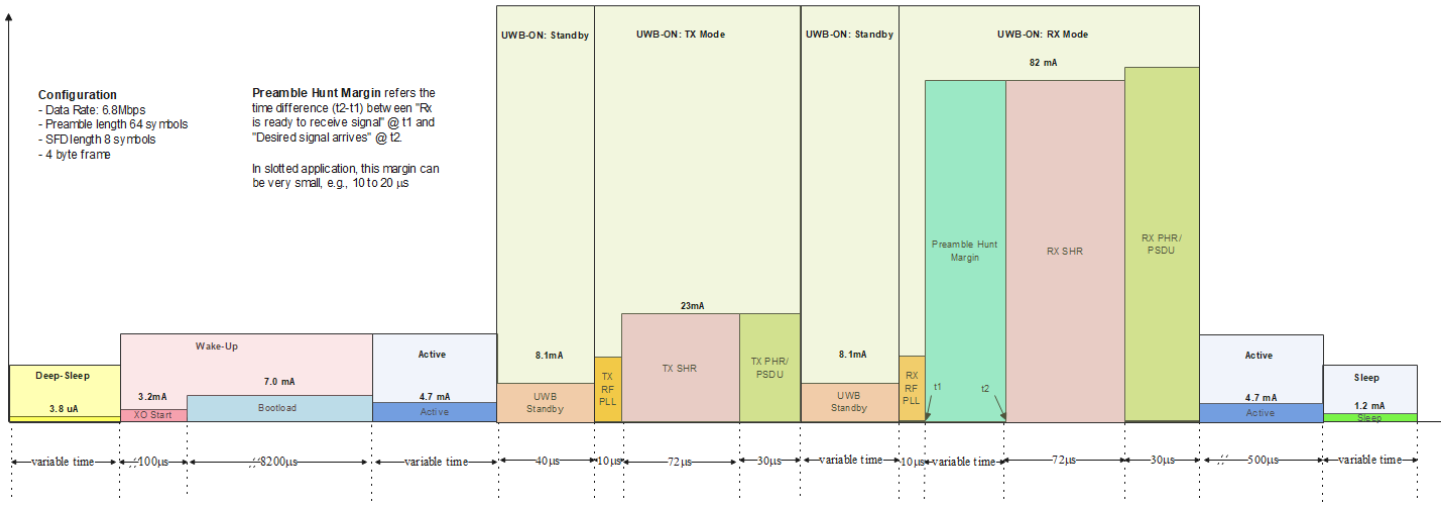


Figure 6-4: Typical Power Profile with Buck

7 Reference design

The following picture shows the reference design of CBU5000V210.

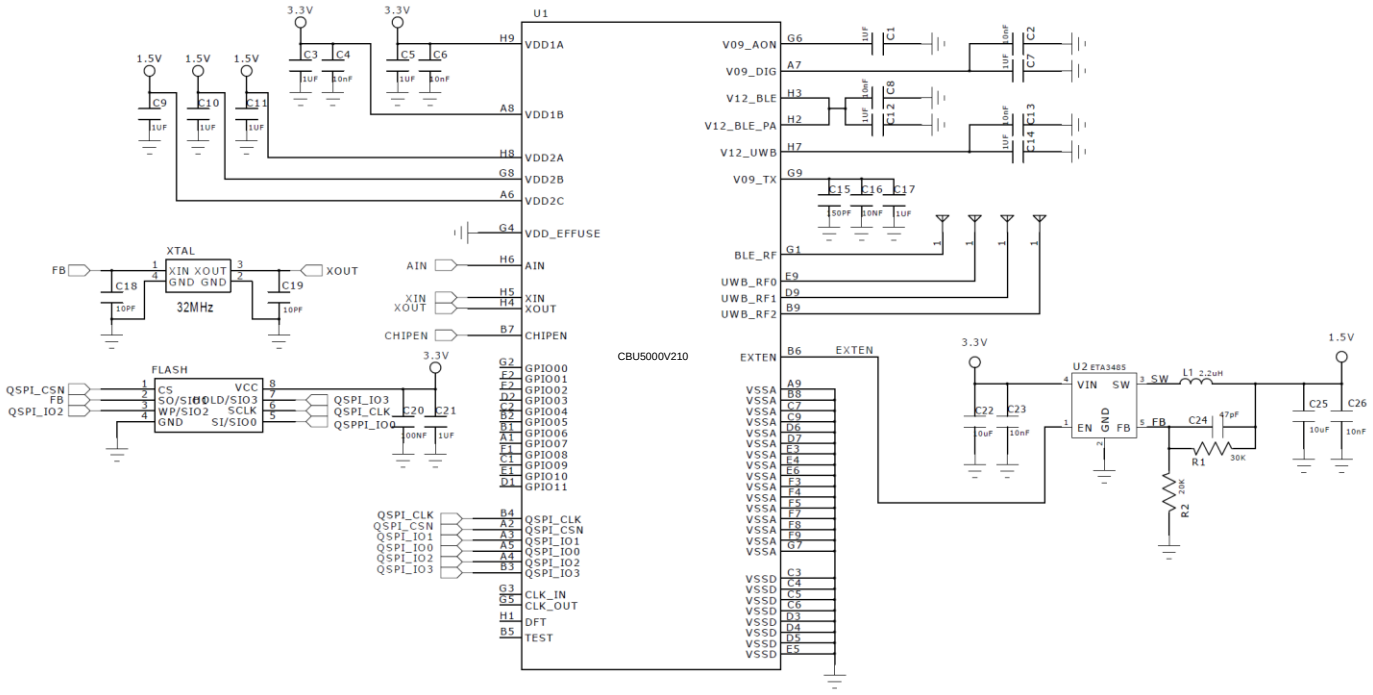
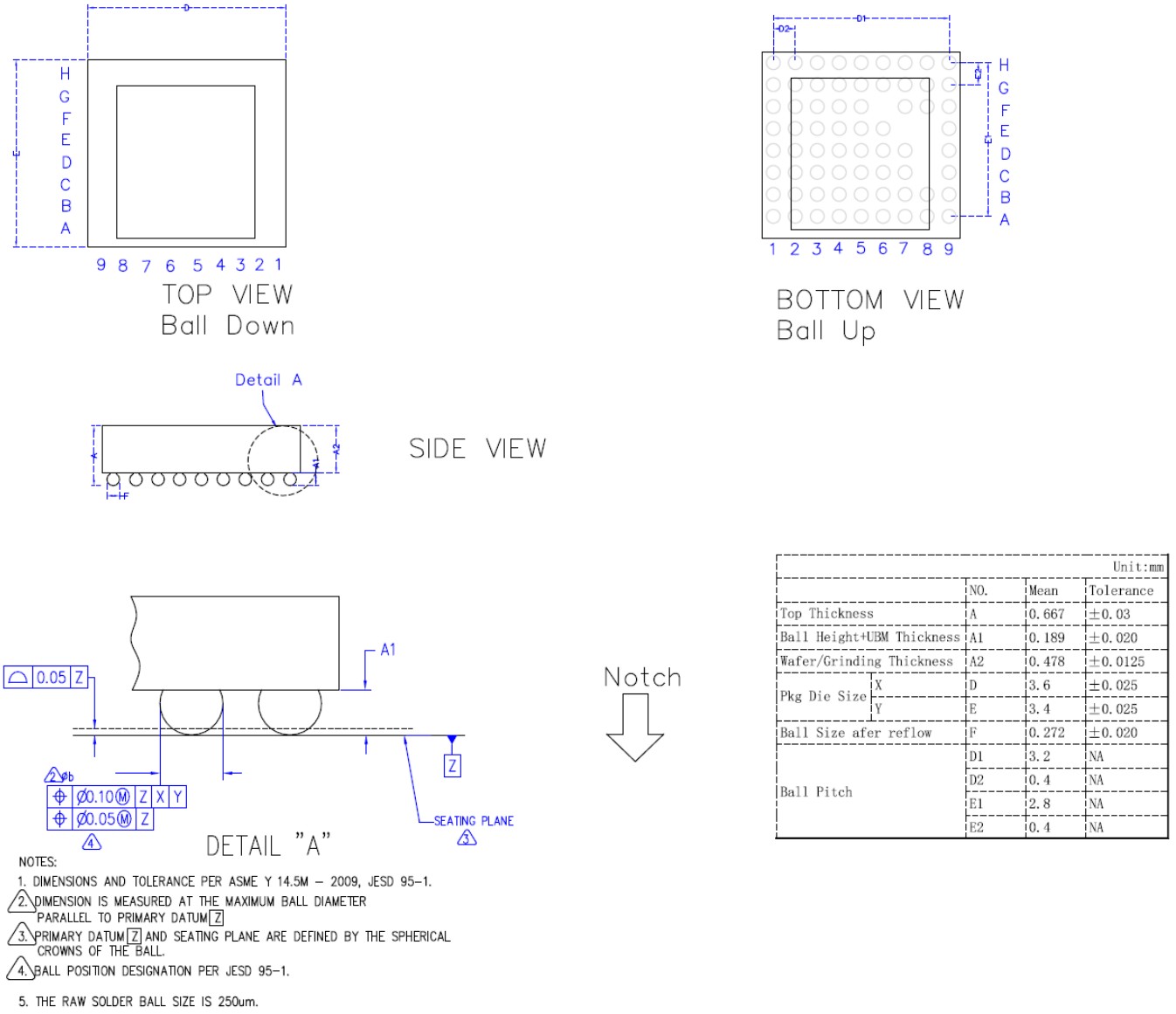


Figure 7-1: Reference Design of CBU5000V210

8 Packaging



Unit:mm			
	NO.	Mean	Tolerance
Top Thickness	A	0.667	±0.03
Ball Height+UBM Thickness	A1	0.189	±0.020
Wafer/Grinding Thickness	A2	0.478	±0.0125
Pkg Die Size X	D	3.6	±0.025
Pkg Die Size Y	E	3.4	±0.025
Ball Size afer reflow	F	0.272	±0.020
Ball Pitch	D1	3.2	NA
	D2	0.4	NA
	E1	2.8	NA
	E2	0.4	NA

NOTES:
1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M – 2009, JESD 95-1.
2. DIMENSION IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO PRIMARY DATUM Z
3. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BALL.
4. BALL POSITION DESIGNATION PER JESD 95-1.
5. THE RAW SOLDER BALL SIZE IS 250um.

Figure 8-1: Package Dimension

9 Glossary

Table 9-1: Glossary of Terms

Abbreviation	Full Title	Explanation
1T3R	One Transmitter and Three Receivers	UWB design mode.
ADC	Analog-to-Digital Converter	A system that converts an analog signal into a digital signal.
AES	Advanced Encryption Standard	A specification for the encryption of electronic data
AOA	angle of arrival	The angle of arrival of a signal is the direction from which the signal is received.
API	Application Programming Interface	A set of rules or protocols that let software applications communicate with each other to exchange data, features and functionality.
BLE	Bluetooth Low Energy	It is intended to provide considerably reduced power consumption and cost while maintaining a similar communication range.
BOM	Bill of Materials	A list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, parts, and the quantities of each needed to manufacture an end product.
CFO	Carrier Frequency Offset	The difference between the two carrier frequency.
CMOS	Complementary Metal-Oxide-Semiconductor	A type of technology used in the manufacturing of computer processors, memory chips, and other digital devices.
FOV	Field of View	The angular extent of the observable world that is seen at any given moment.
I2C	Inter-Integrated Circuit	A synchronous, multi-controller/multi-target (historically-termed as master/slave), single-ended, serial communication bus.
IEEE	Institute of Electrical and Electronic Engineers	The world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.
IoT	Internet of Things	It describes devices with sensors, processing ability, software and other technologies that connect and exchange data with other devices and systems over the Internet or other communications networks.
IR-UWB	Impulse-Radio Ultra-Wideband	The IR-UWB technology uses extremely wide bandwidth impulse signal to detect moving objects by transmitting and receiving impulse signal.
OOB	Out-of-Band signalling	The exchange of call control information in a separate band from the data or voice stream, or on an entirely separate, dedicated channel.
PDoA	Phase Difference of Arrival	Method of determining the direction of propagation of a radio-frequency wave incident on an antenna array using the phase difference between the signal received on each antenna array element.
QSPI	Quad Serial Peripheral Interface	A serial communication interface to involve a lot of memory-intensive data.
RF	Radio Frequency	The oscillation rate of an alternating electric current or voltage or of a magnetic, electric or electromagnetic field or mechanical system in the frequency range from around 20 kHz to around 300 GHz.
SFD	Start of Frame Delimiter	It marks the end of the packet preamble.
SoC	System on a Chip	An integrated circuit that compresses all of a system's required components onto one piece of silicon.
SPI	Serial Peripheral Interface	A de facto standard (with many variants) for synchronous serial communication, used primarily in embedded systems for short-distance wired communication between integrated circuits.
STS	Scrambled Timestamp Sequence	It is used to provide additional integrity as well as accuracy for ranging measurement.
TDoA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A number of such TDoA measurements at different locations can be used to uniquely determine the position of the transmitter.
TRSW	Transmitter and Receiver Switch	A switch to control the antenna for TX and RX0.
TWR	Two-Way Ranging	The two-way ranging method determines the time of flight of the UWB RF signal and then calculates the distance between the nodes by multiplying the time by the speed of light.
UART	Universal Asynchronous Receiver-Transmitter	A peripheral device for asynchronous serial communication in which the data format and transmission speeds are configurable.
UWBS	Ultra-Wideband Signalling	It refers to the transmission of data using ultra-wideband radio technology, which enables high-speed, short-range communication across a broad spectrum of frequencies.

10 Reference

[1] IEEE Std 802.15.4™-2020: IEEE Standard for Low-Rate Wireless Networks

[2] IEEE Std 802.15.4z™-2020: IEEE Standard for Low-Rate Wireless Networks. Amendment 1: Enhanced Ultra Wideband (UWB) Physical Layers (PHYs) and Associated Ranging Techniques

11 Version history

Data	Version	Description
2025	1.0	Initial version

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