CBU5000V210 UWB SoC

Hardware Design Guide V1.0

ShenZhen ChipsBank Technology Co., Ltd.

http://www.chipsbank.com/

7th Floor, Building 12, Phase II, Shenzhen Software Park,

Kejizhong 2nd Road, Nanshan District

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1 系统概述

1.1 概述

CBU5000V210 是一款集成了 UWB(6~9GHz)、BLE 5.0 和 32 位微处理器(Cortex-M33）的单芯片 SoC。该 SOC 同时集成硬件安全平台和丰富的功能模块，如定时器、UART、 SPI、 I2C 等，可应用于通信，测距，物联网等领域。

1.2 芯片框图

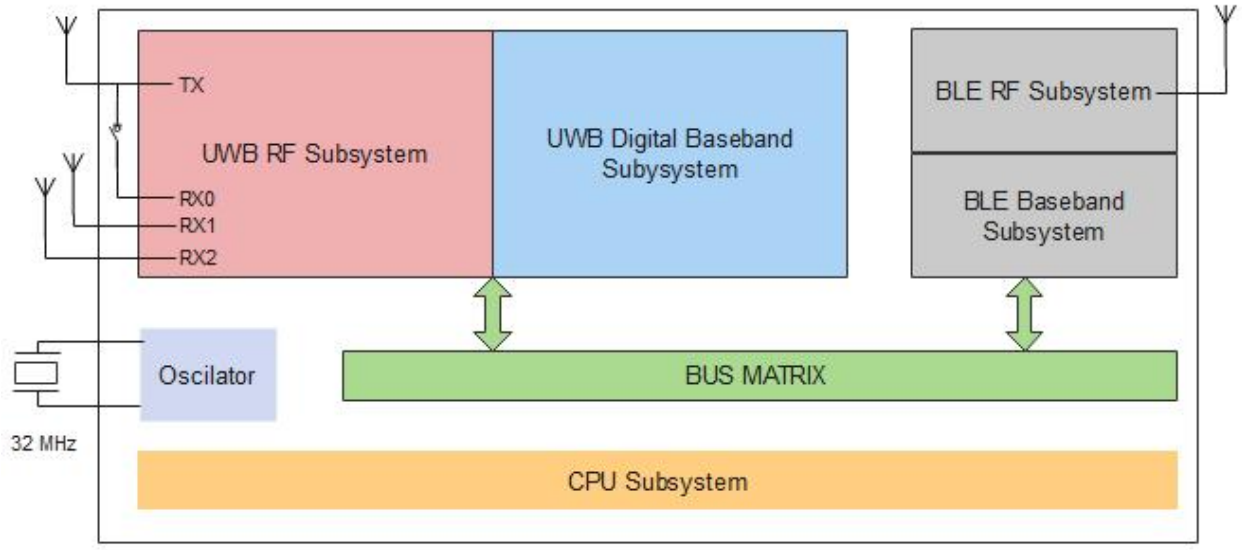
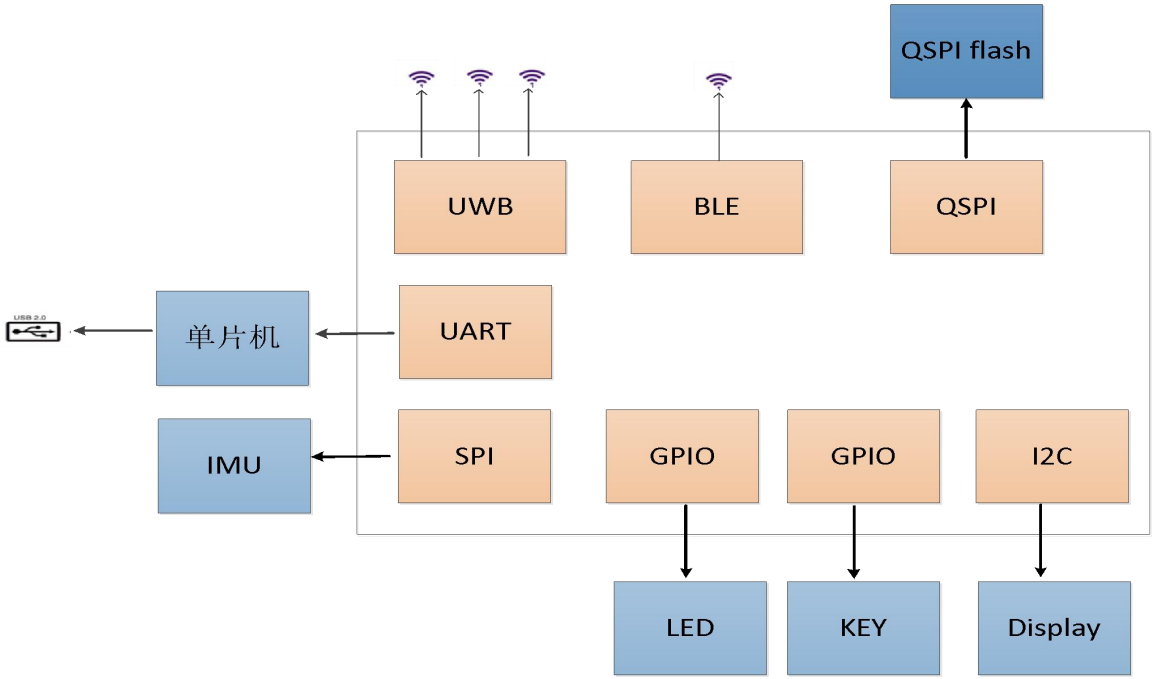


Figure 1-1 CBU5000V210 芯片框图

1.3 应用框图



以上框图是典型应用框图，具体使用请根据实际项目需求设计。

Figure 1-2 CBU5000V210 芯片应用框图

2 原理图设计建议

2.1 电源设计

CBU5000V210 芯片电源需求

Parameter	Min	Typ.	Max	Units	Notes
Supply voltage A8/H9（VDD1A/B）	1.62	3.3	3.6	V	
Supply voltage A6/G8/H8（VDD2A/B/C）	1.42	1.5	3.6	V	

Figure 2-1 CBU5000v210 芯片电源需求

Figure 2-1 表示 CBU5000V210 芯片电源需求。在满足供电电压情况下，同时要增加去耦电容，去耦电容有以下注意事项:

1. 去耦电容应靠近电源管脚放置，具体电容数量和容量参考原理图 Figure 2-2 和 Figure 2-3，请勿随意调整。
2. 推荐 2 个电容， 小电容 10nf，1UF。
3. 去耦电容摆放请参考 PCB 设计 3.6 章节。

如 Figure 2-2 和 Figure 2-3 是 CBU5000V210 A6/G8/H8、A6/G8/H8 电源管脚和电源接地管脚的参考原理图设计。

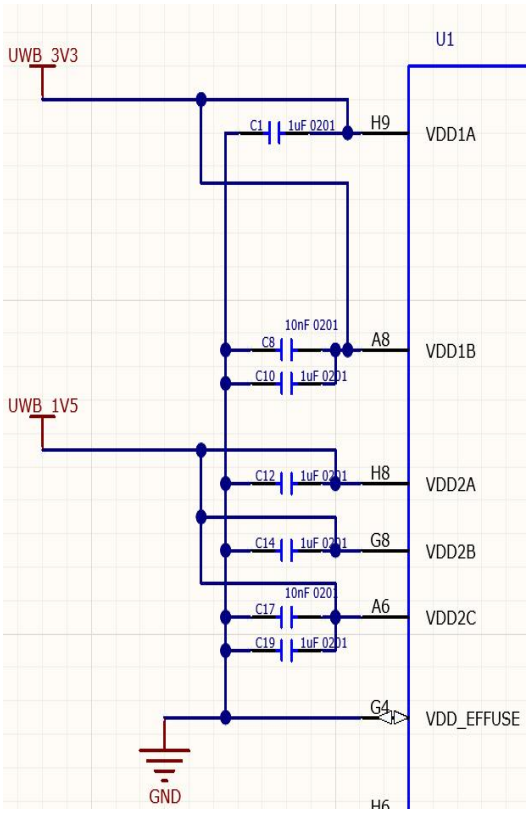


Figure 2-2 A8/H9、A6/G8/H8 电源管脚原理图

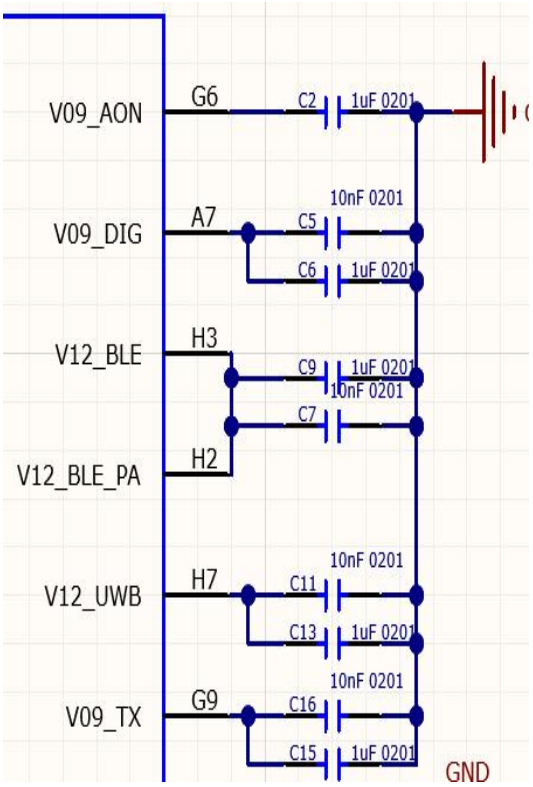


Figure 2-3 旁路电源管脚原理图

如 Figure 2-1 是 CBU5000V210 芯片电源需求，A6/G8/H8 电压大小 1.5V 为参考电压。Figure 2-4 为 3.3V 转 1.5V 电源电路参考原理图。

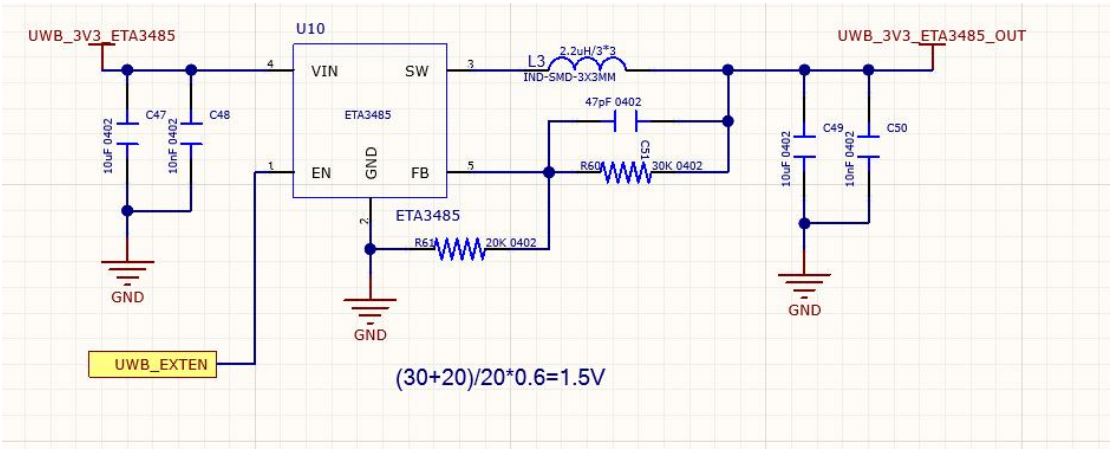


Figure 2-4 1.5V 电源电路参考原理图

3D PDOA 应用场景功耗情况:
1.5V 电源接口最大瞬间电流 250mA 左右。
3.3V 电源接口最大瞬间电流 50mA 左右。
单天线透传应用功耗情况:
1.5V 电源接口最大瞬间电流 200mA 左右。
3.3V 电源接口最大瞬间电流 50mA 左右。
以上电流可以作为电源 PCB 走线的电源设计参考。

注：以上电源引脚功耗情况，仅代表该应用场景以及瞬间电流。芯片的功耗情况和其他应用可另行研究。

2.2 外部晶振参考原理图设计

CBU5000V210 芯片内部的震荡电路与外置 32MHz 晶体一起构成时钟电路，如 Figure 2-5 所示。XIN 脚输入，XOUT 脚输出。推荐晶振型号 SX1B32.000F1210F30_SCTF(星通时频)-SX1B32.000F1210F30，匹配的滤波电容选择 12PF。支持有源晶振，从 H5 输入。

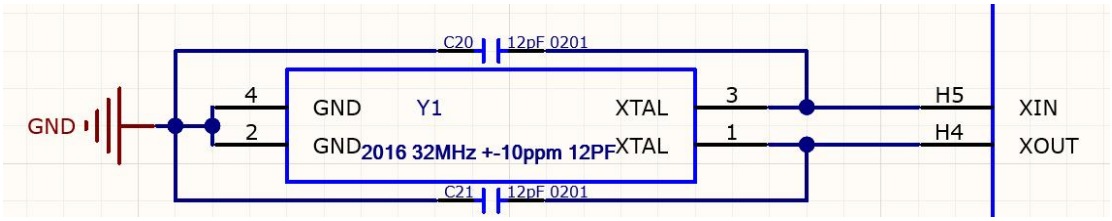


Figure 2-5 外部晶振参考原理图

2.3 Flash 电路设计

CBU5000V210 芯片集成 QSPI 控制器，可用于连接 QSPI flash。

2.3.1 QSPI FLASH 连接示意图

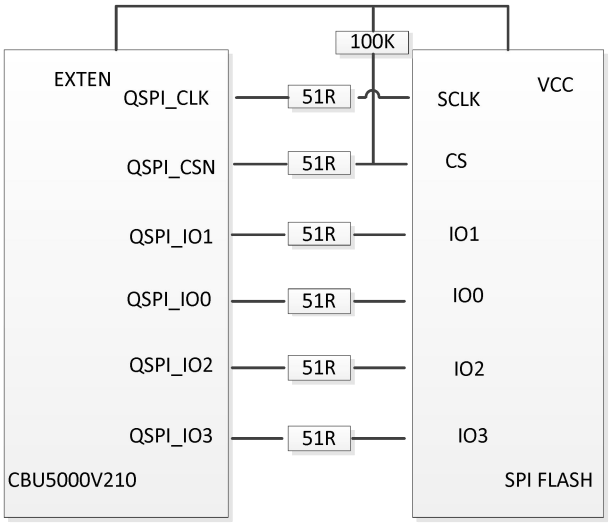


Figure 2-6 QSPI FLASH 连接示意图

在 CBU5000v210 芯片端串联 51ohm 电阻，串联电阻用于防止振铃， 如果 PCB 上的走线较长， 需要用这个补偿，否则速率高的时候 ， 容易出现误码。

2.3.2 SPI FLASH 支持型号列表

CBU5000V210 芯片外置的 FLASH 芯片可使用普冉 P25Q40SH-UXH-IR 型号。如 Figure 2-7 是 CBU5000V210 flash 参考原理图。Flash 电源连接到 CBU5000V210 芯片的 B6 （EXTEN）引脚,可实现 CBU5000V210 芯片在 deepsleep 状态下 FLASH 电源关断。

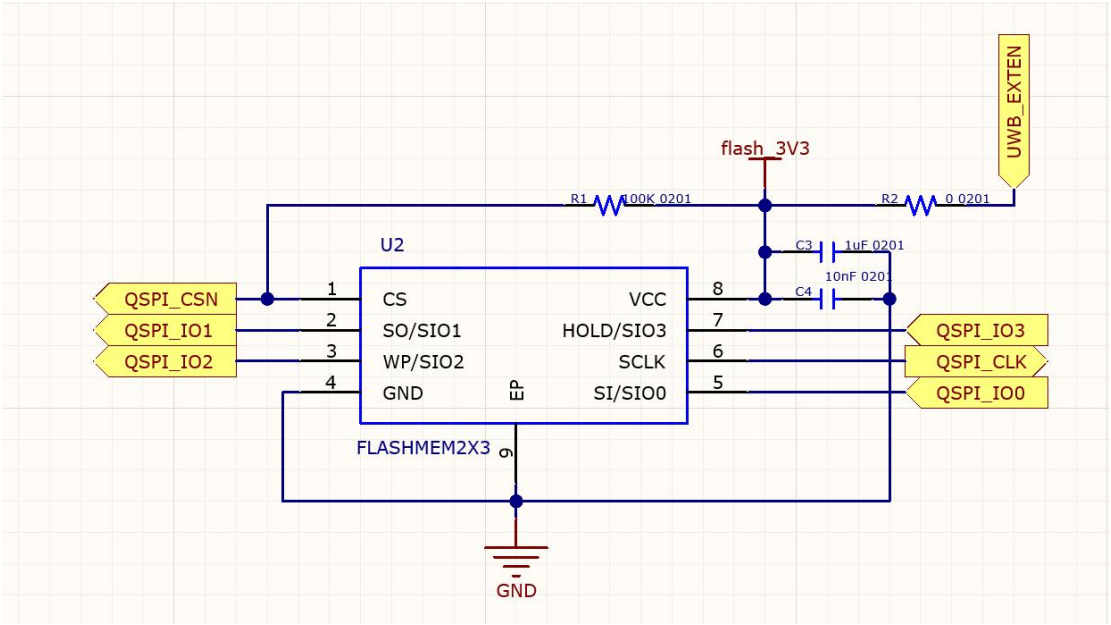


Figure 2-7 flash 参考原理图

2.4 使能电路参考原理图

CBU5000V210 芯片的硬件使能通过 pin B7（CHIPEN）管脚控制，高电平有效。pin B7（CHIPEN）管脚需要增加 10nf 电容，用来消除使能信号上的抖动，增强抗干扰能力，以防止误触发导致的系统异常。

如 Figure 2-8 是 chipen 参考原理图。

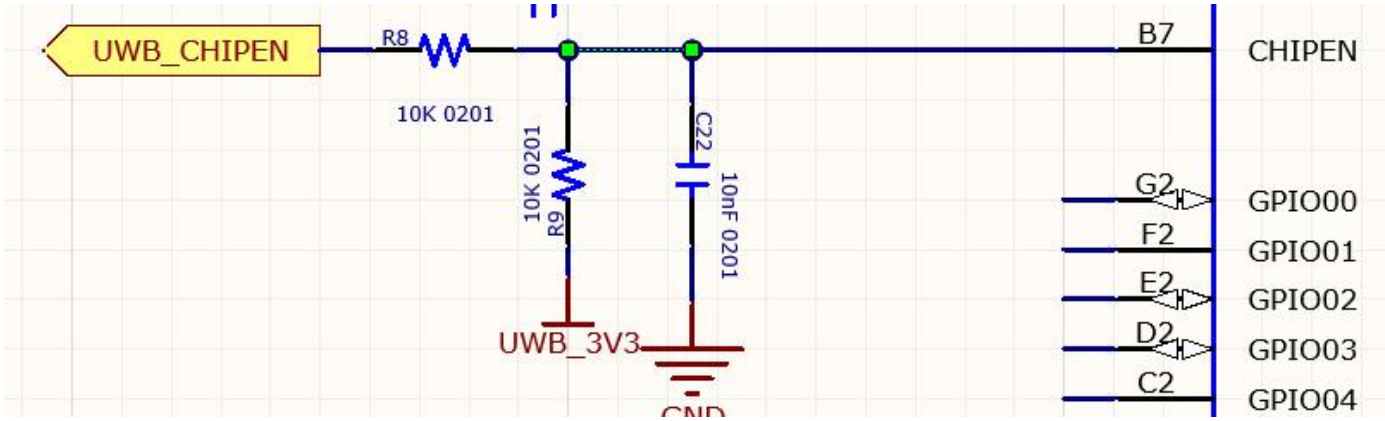


Figure 2-8 chipen 参考原理图

2.5 Test 电路

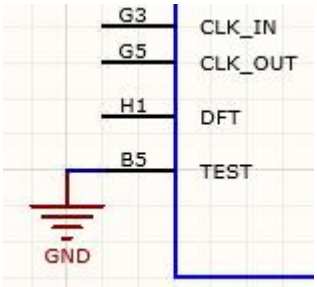


Figure 2-9 参考原理图

pin G3，pin G5，pin H1，pin B5 是一些芯片测试引脚。电路连接方式请参考 Figure 2-9，不要随意修改。

2.6 RF 管脚

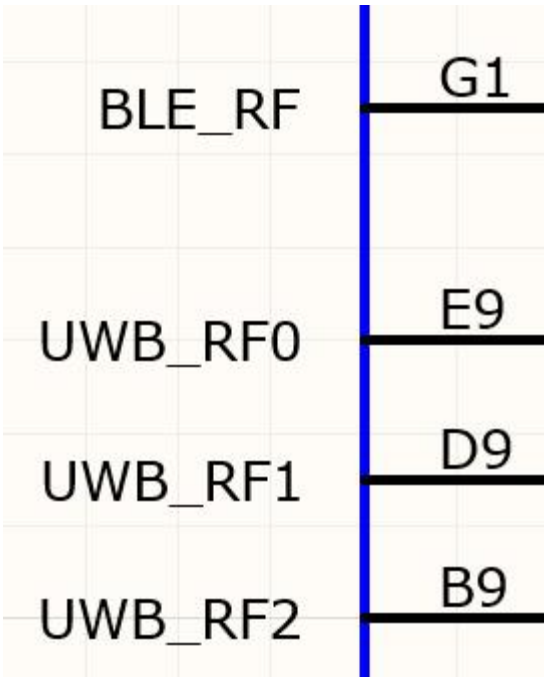


Figure 2-10 射频管脚图

G1 为蓝牙射频接口，集成 TX 和 RX 功能，E9，D9，B9 分别是 UWB 的射频接口，TX 对应 RF0，RX 对应 RF0，RF1，RF2。如图 Figure 2-10。

2.7 GPIO 管脚

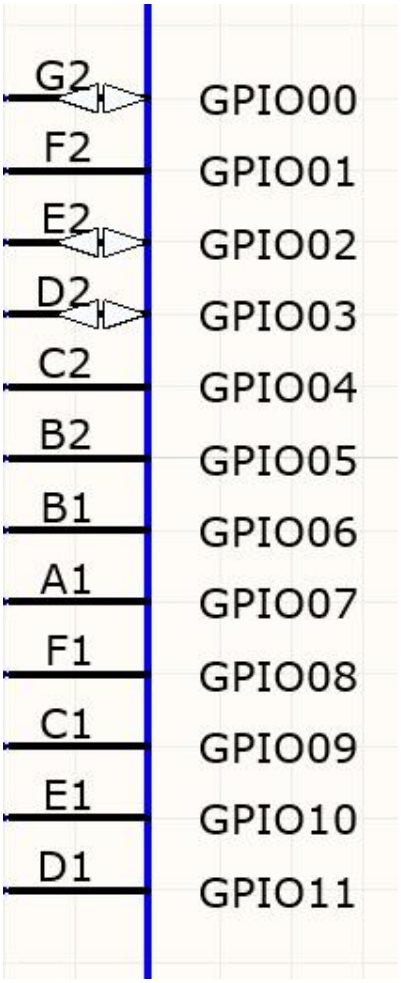


Figure 2-11 GPIO 管脚图

其中 C1（GPIO09）和 D1（GPIO11）可作为 SWD 管脚。前提是 G2（GPIO00），F2（GPIO01），E2（GPIO02）需要上拉到 3.3V，F1（GPIO08）需要下拉电阻接地。

注：在 SWD 模式下，F1（GPIO08)和 E1（GPIO10）只能作为输入。其他引脚可正常使用。

3 PCB 设计建议

3.1 PCB 叠层设计

UWB 应用中天线设计比较重要，推荐以下 4 层板叠层设计：

叠层信息

序号	叠构	物料名称	物料参数	残铜率(%)	物料厚(mm)	理论厚(mm)
L1			0.33_PT_1 OZ		0.012	0.039
		PP S1000H	3313(55%)*2		0.18	0.175
L2			0.5 OZ		0.018	0.018
		Core S1000H	1.5mm(含铜)		1.465	1.465
L3			0.5 OZ		0.018	0.018
		PP S1000H	3313(55%)*2		0.18	0.172
L4			0.33_PT_1 OZ		0.012	0.039

备注信息:	

阻抗信息：

序号	客户要求								调整计算				H1 (mil)	Er1	H2 (mil)	Er2	蚀刻值
	阻抗类型	控制层	上参考层	下参考层	线宽 (Mil)	线距 (Mil)	线铜 (Mil)	要求值 (Ω)	线宽 (Mil)	线距 (Mil)	线铜 (Mil)	计算值 (Ω)					
1	外层单端共面地	L1		L2	10.60		5.00	50±5	10.60		6.00	51.4	6.9	3.9			51.4

Figure 3-1 4 层板叠层

3.2 CBU5000V210 扇出设计

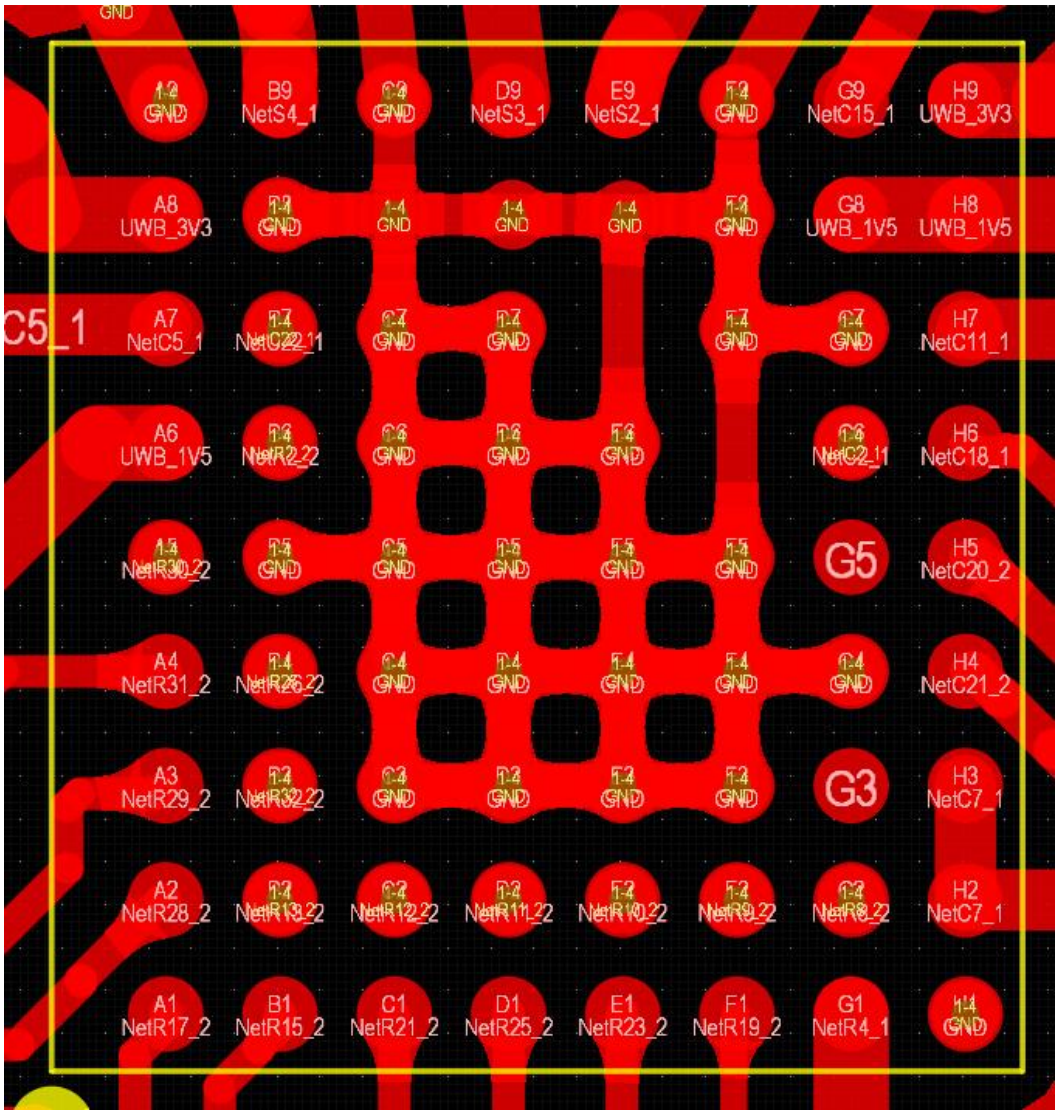


Figure 3-2 CBU5000V210 Ball 扇出

2.2.1 最外 Ball 扇出设计

靠最外圈 ball，GPIO 引脚可以从 top 层走 4mil 线宽。电源相关 ball 可以走 11mil 线宽。

2.2.2 内圈 Ball 扇出设计

内圈 ball，需要换层到内层，务必换层过孔规则放置。

内部地层可以通过网格状连接共地，有利于散热和焊接稳定。

3.3 RF 走线设计要求

1，为保证损耗最小，RF 走线尽量短，元件之间尽量排紧凑一些；RF 走线尽量走直 线，不要使用直角走线，走线宽度以及走线和外围 GND 的间距推荐 0.27mm/0.126mm。因 PCB 板材和介质会影响 RF 走线阻抗，为保证 RF 走线的阻抗为 50Ω，可以适当调整走线宽度以及走线和外围 GND 的间距。

2，RF 走线四周一定要 包地处理，上下层要通过 GND 过孔连接。

3，UWB RF0,RF1,RF2 3 个射频引脚保证隔离足够好。除了射频包地处理，RF0 和 RF1 尽量分开。

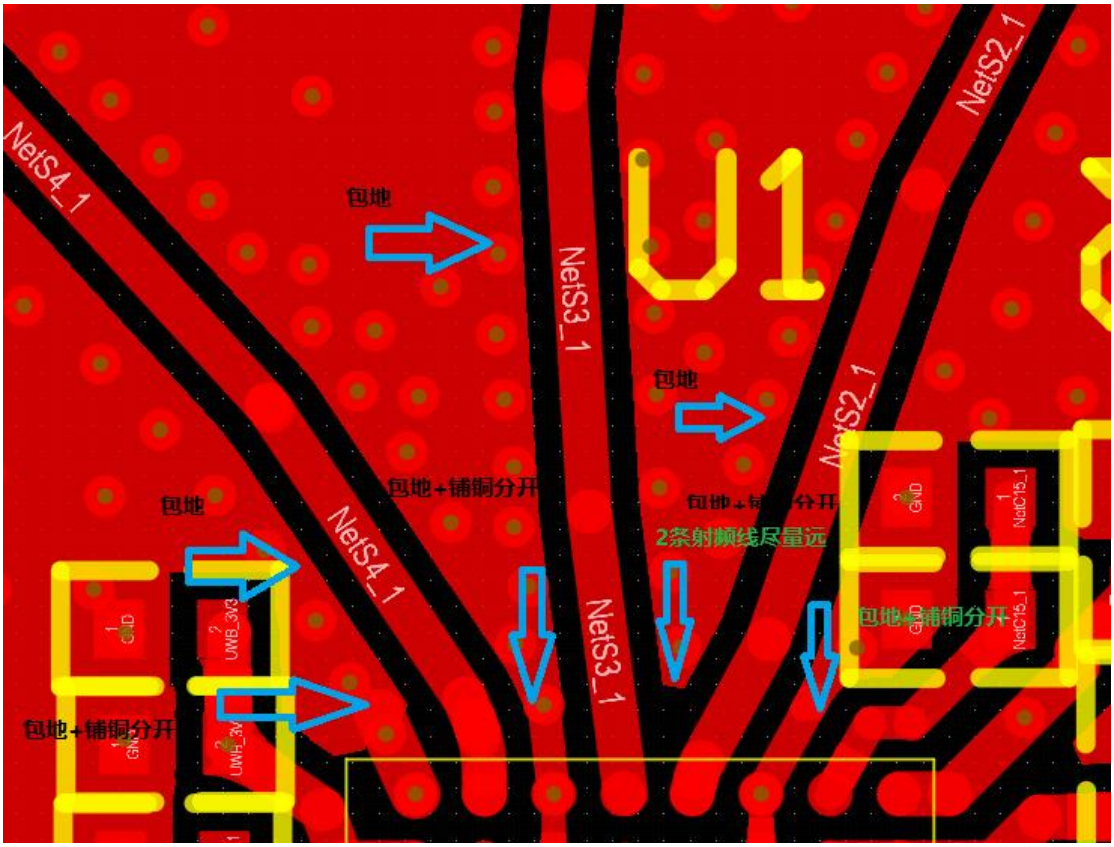


Figure 3-3 CBU5000V210 RF 走线

3.4 晶振走线设计要求

在时钟电路的 PCB 设计中，请注意：

晶体电路布局需要优先考虑，布局时应与芯片在同一层并尽量靠近放置以避免打过孔，晶体走线尽可能的短，远离干扰源，尽量远离板边缘；

1，晶体以及时钟信号需要全程包地处理，包地线每隔 200-300mil 至少添加一个 GND 过孔，并且必须保证邻层的地参考面完整；

2，晶体电路布局时如果与芯片不同层放置，晶体走线必须全程包地处理，避免被干扰；

3，时钟走线 Xin 和 Xout 以及晶体下方投影区域禁止任何走线，避免噪声耦合进入时钟电路；

4，晶体下方的顶层，可以围绕放置地环。地环通过过孔与相邻的接地层连接，以隔离噪声；

5，晶体下方的第二层保持完整的地参考平面，避免任何走线分割，有助于隔离噪声保持晶体输出。

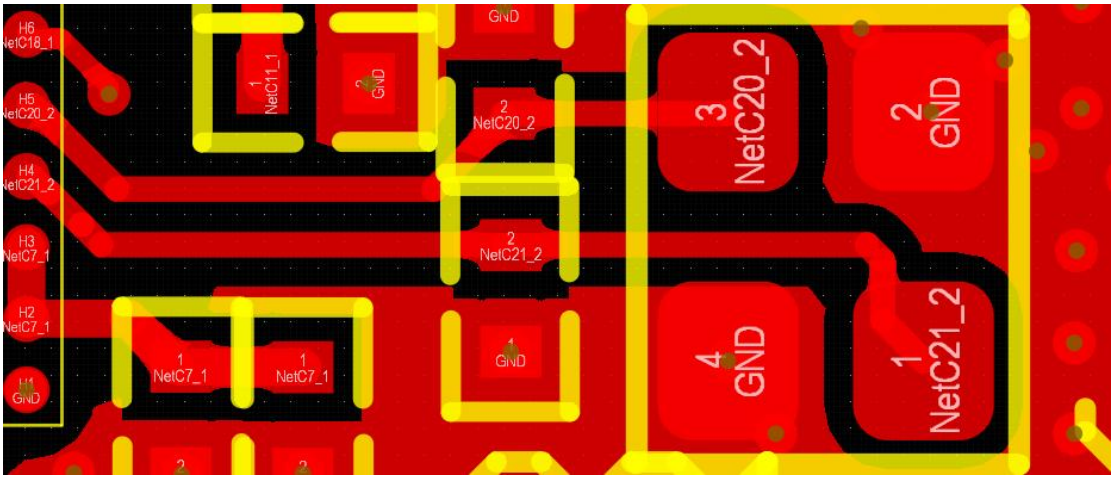


Figure 3-4 晶体布局和走线

3.5 电源走线

CBU5000V210 有 2 路电源：UWB_1V5 和 UWB_3V3。

为了保证电源的供流能力足够，UWB_1V5 和 UWB_3V3 线宽可从 1mm-0.5mm-0.27mm 的线宽变化，可参考 PCB 设计。优先考虑 UWB_1V5 走线，为了保证电源走线换层时有足够的过流能力，一般电源线需要通过 2 个电源过孔换层。

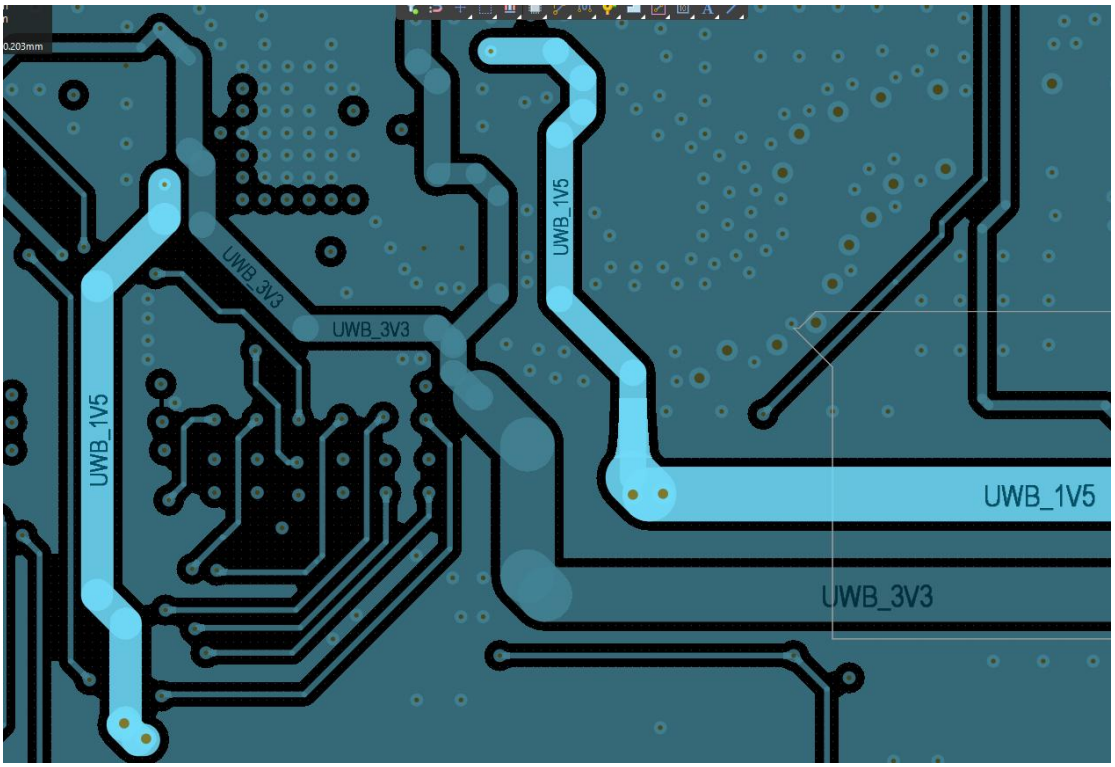


Figure 3-5 UWB_1V5 电源走线

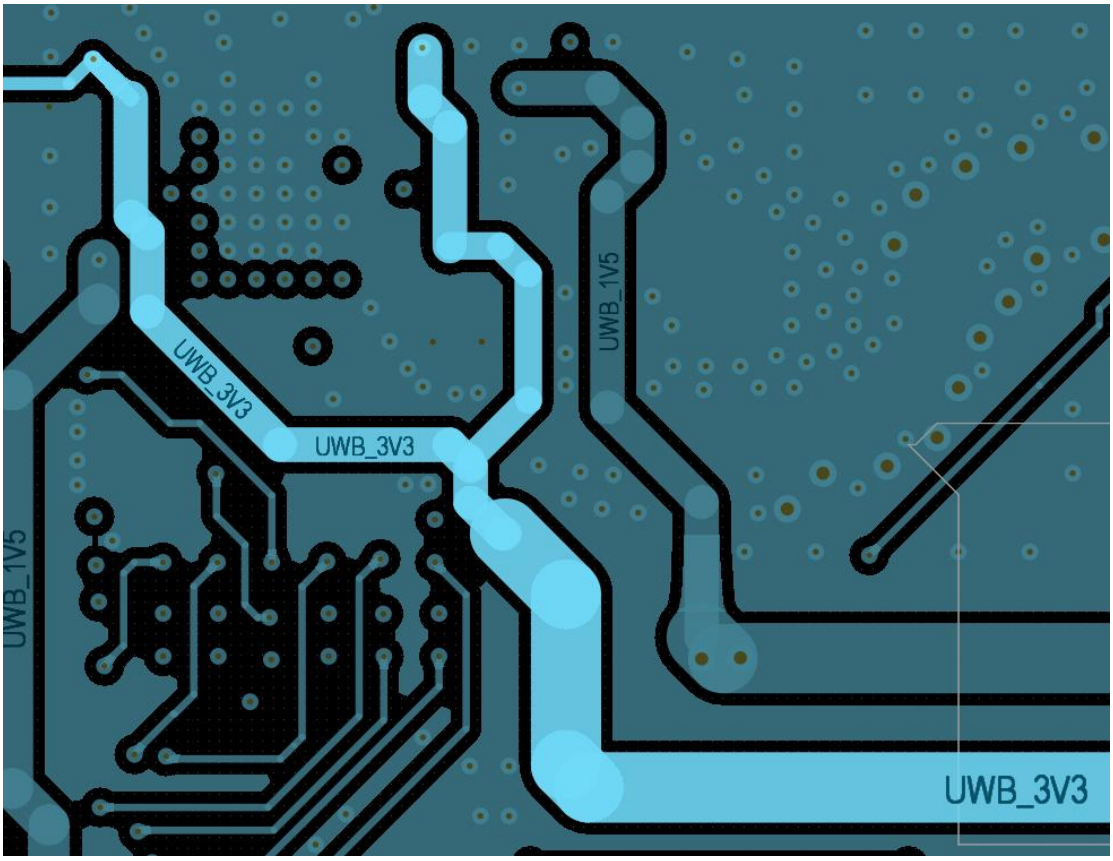


Figure 3-6 UWB_3V3 电源走线

3.6 滤波电容布局参考

滤波电容应靠近管脚摆放，请勿随意调整。如 Figure 3-7。

1，小电容 10nf 靠近芯片，1UF 随后。优先 考虑 VDD2A/B/C 管脚电容布局，其次 VDD1A/B 管脚电容布局。

2，对于旁路电源引脚，优先考虑 V09_TX ，V12_UWB 的滤波电容就近布局， 其次是 V12_BLE, V12_BLE_PA 旁路电源引脚。

3，滤波电容接地端，焊盘做盘中孔接地处理，保证接地。

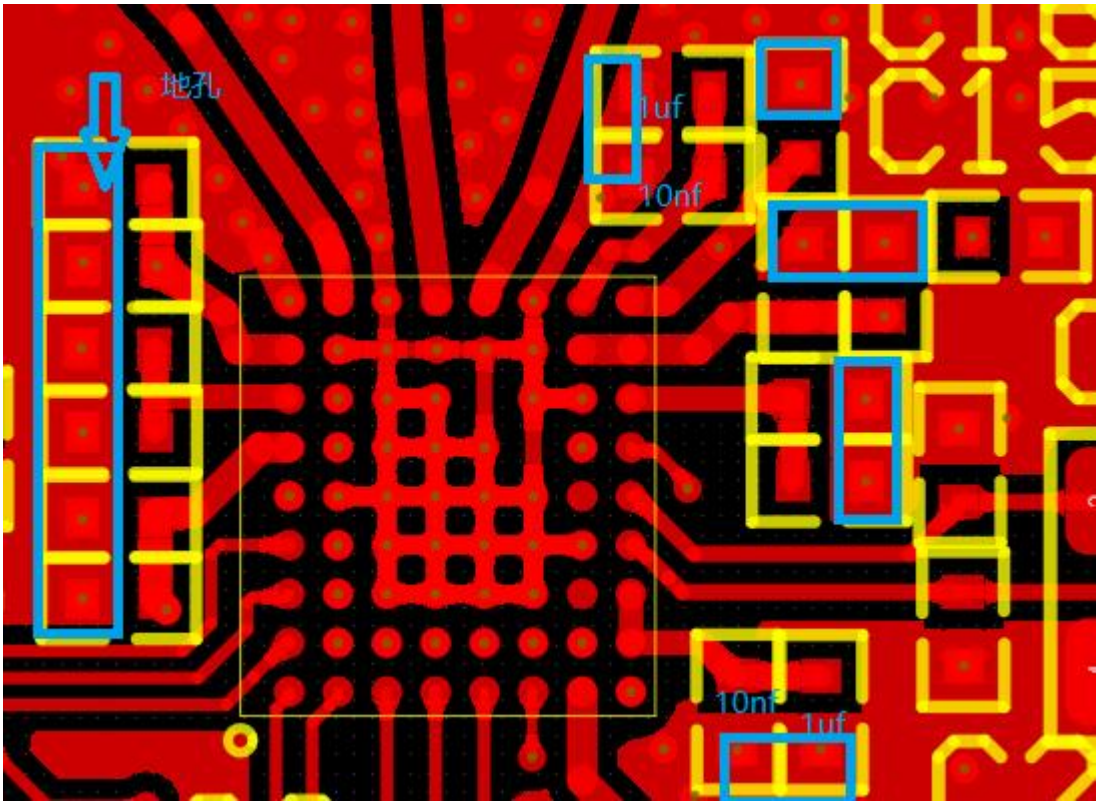


Figure 3-7 滤波电容布局

4 Version history

Data	Version	Description
2025-04-17	1.0	初始版本

5 Disclaimers

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