Birla Institute of Technology and Science

Ist Semester 2019-2020

Digital Design

CS/ EEE/ INSTR F215

Verilog Assignment

Instructions:

Following are a set of problems on Verilog programming. Write the verilog code for each of the problem as given below. Completed Problem sheet with solutions to be submitted on or before 11th November 2019 to the respective tutorial instructor of your tutorial section. The final solution sheet should be handwritten document by each student. Please write your name IDNO and Tutorial section number also in the sheet. Maximum marks for this assignment will be 10 marks.

Verilog Assignment Problems

Q1: Write a verilog behavioral code for a synchronous mod-8 counter which will count from 000 to 111. The counter also has asynchronous enable and reset pins. i.e., when reset is Logic 0 counter resets and when enable is Logic 1 counter enabled for counting.

Q2: Write the verilog code using gate level modelling for a 2×2 binary multiplier (unsigned numbers) . Also write a test bench.

Q3: A priority encoder can form an integral part of a programmable interrupt controller. Design a 8-input priority encoder using dataflow modeling. The order of Priority is D0 as Highest and D7 the lowest in the increasing order. If say 3 inputs D_0, D_3, D_7 are asserted, D_0 is given a priority.

Q4: Obtain the state diagram for the synchronous sequential machine that detects a sequence '110'. The output is made '1' whenever the sequence is detected and reset only with subsequent occurrence of '00'. Write a behavioral verilog HDL code to model this synchronous sequential machine. The output must change at positive edge of clock. Write a test bench to verify the code.

Q5: Write verilog code using any one of the models for BCD to 7-segment code generator with common cathode configuration, BCD to 7-segment code generator must accept input every positive clock edge and generates its output in next positive clock edge. Also write a test bench to display a stream '123456789', with one BCD digit in each clock cycle at a clock frequency of 1 Hz.