EE 238

Power Engineering – II

Power Electronics

Lecture 15

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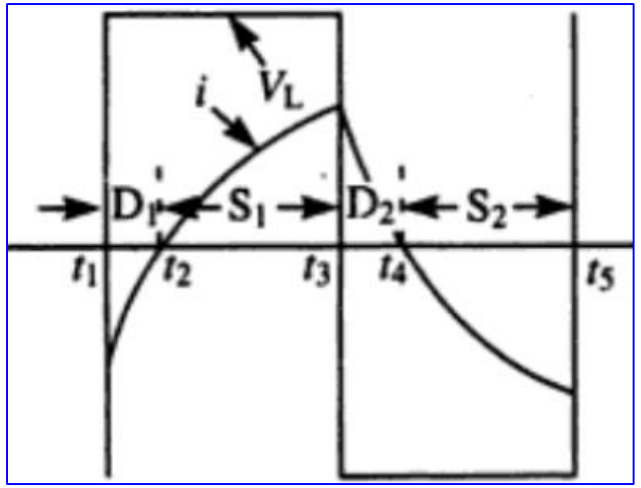
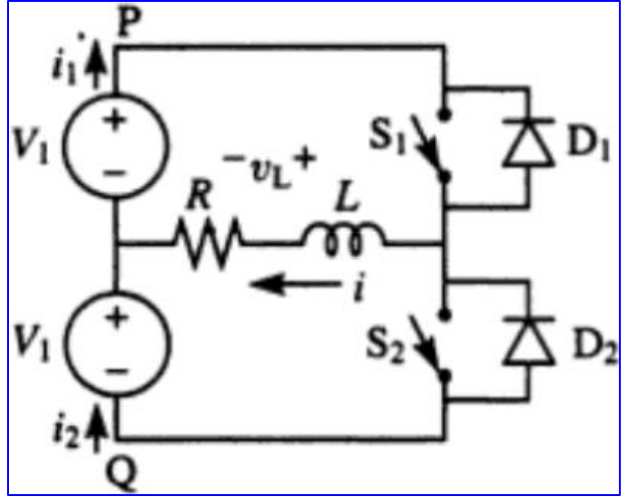
Commutation Sequence of Switching Elements

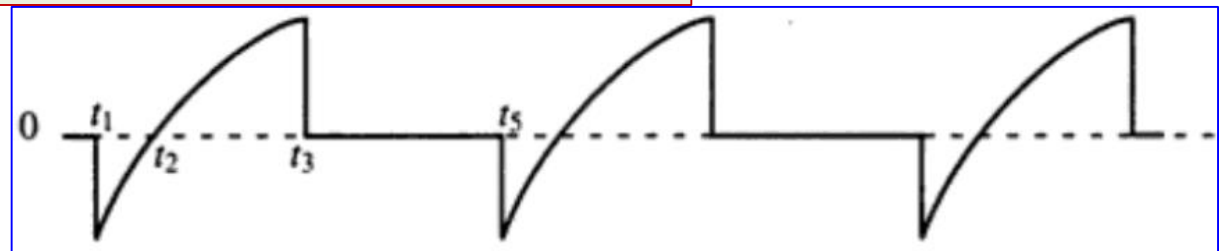




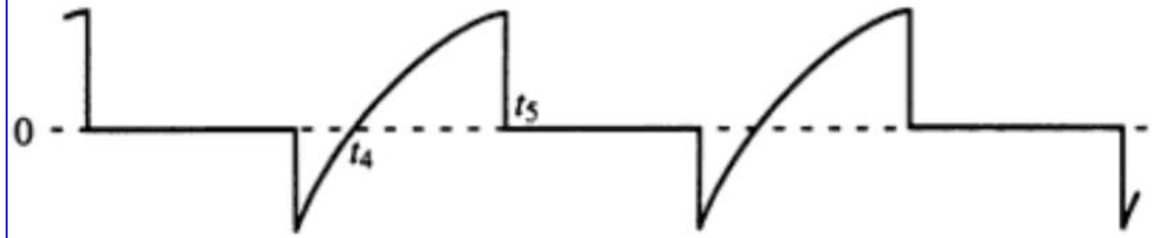
Current Waveform on the DC side

The input currents have a ripple component besides the DC component. An input filter will be necessary to reduce DC source current ripple to low values. A large enough filter will be able to limit the ripple current within acceptable limits and also eliminates the necessity for the DC source to handle reverse currents.

A DC bus supplied from a rectifier and not having a filter will not be able to handle a reverse current at any instant of time.

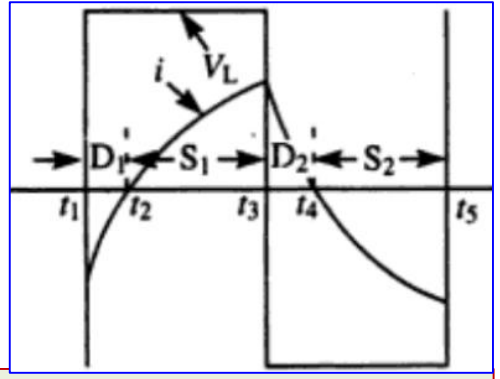


(a) Waveform of i_1



Adjustment of AC frequency and AC voltage

The half-bridge inverter topology does not lend itself to easy adjustment of voltage by PWM. For this, the full-bridge topology will be preferable.



Assume, t1 to t4 as one (positive) half-period and t4 to t7 as the negative half-period.

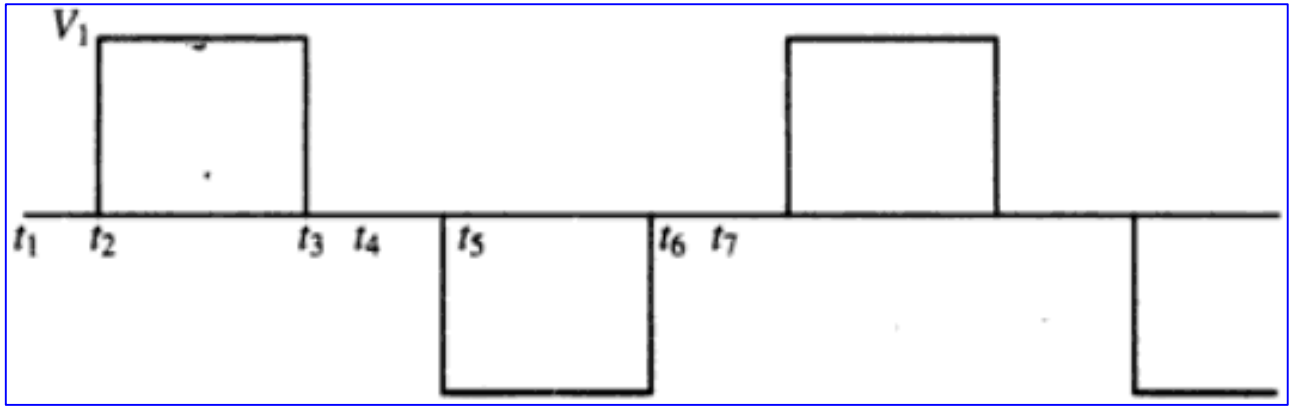
$$D = \frac{\text{actual duration of the pulse in a half-period } (t_2 \text{ to } t_3)}{\text{duration of one half-period } (t_1 \text{ to } t_4)}$$

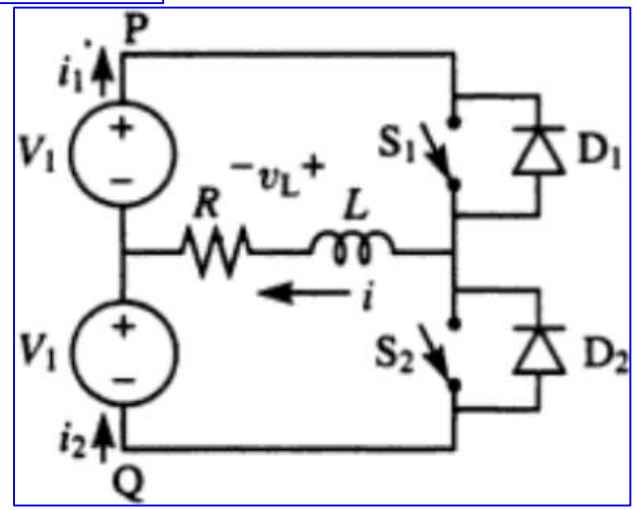
$$f_{\text{RMS}} = \sqrt{\frac{1}{T_2 - T_1}\int_{T_1}^{T_2} [f(t)]^2\, dt}$$

Therefore the mean square value of the AC output voltage will be given by

$$V_{ac}^2 = DV_1^2$$

Therefore we get the r.m.s. value of the AC output voltage as $V = \sqrt{D}V_1$



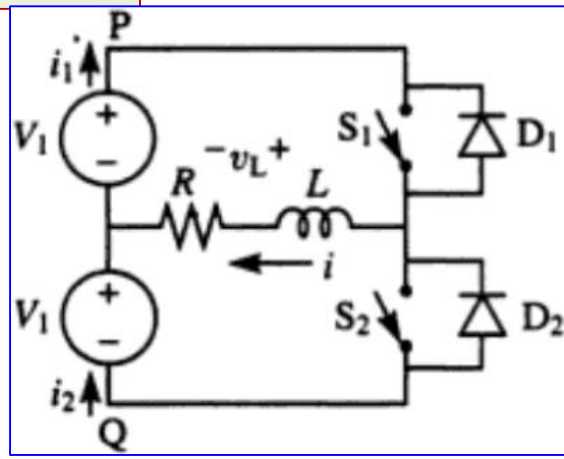


Implementation of PWM

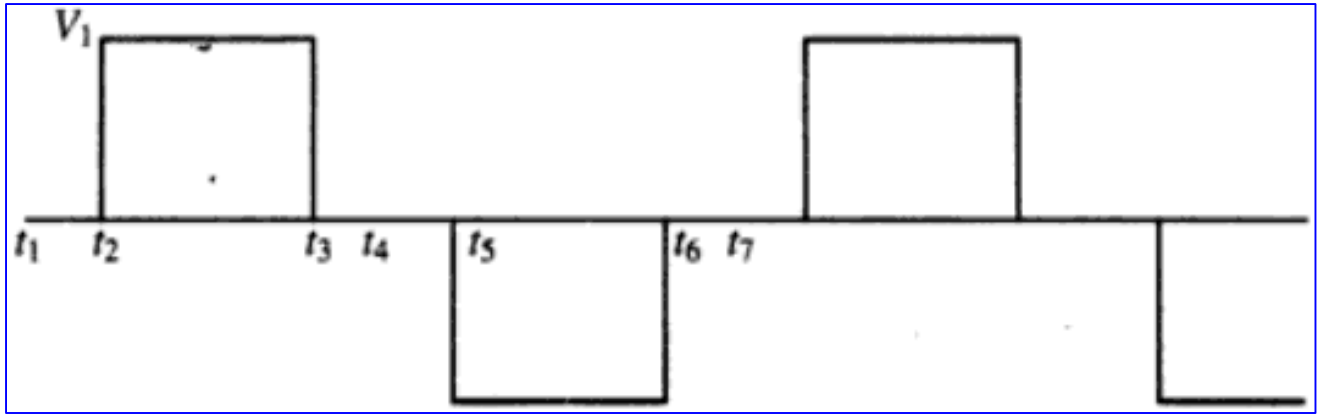
For PWM, during t1 to t2, the load voltage has to be maintained at zero. From t2 to t3, it has to be constant at V1. Then, from t3 to t4, it again has to be zero.

With the half-bridge topology, this voltage pattern is possible only if the load is a pure resistance. If the load is a pure resistance, the voltage across it can be made zero by keeping both the switching blocks OFF. The zero voltage condition is possible because the current will instantly fall to zero when both the switches S1 and S2 are turned OFF.

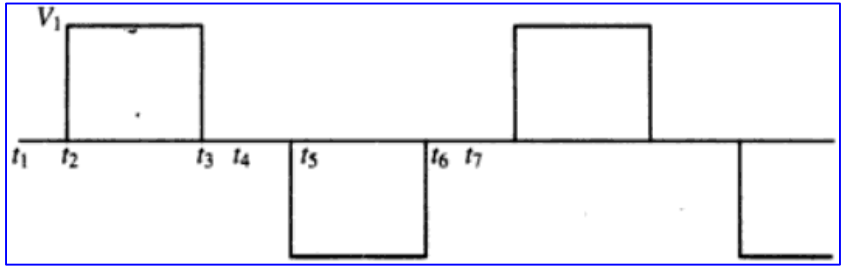
With an inductive load, the current will not instantly fall to zero when the associated controlled switching elements are turned OFF, but finds an alternative path through an uncontrolled switch (diode).



- We therefore conclude that, with the half-bridge topology, it is not always possible to implement PWM in the manner shown.
- With the full bridge topology, the difficulty can be overcome by a suitable choice of switching scheme.



Output Waveform Considerations



Rectangular waveform has, besides the fundamental comp., a significant content of harmonics.

It is possible to reduce the harmonic content and make the output closer to a sine wave, within acceptable limits, by using a **filter circuit** on the output side of the inverter. However, such a filter is also a power circuit and has to handle the voltage and current for which the inverter is designed, which are usually large, for PE applications. It'll **add to the size, weight and cost of the equipment and also cause added power loss**, thereby adversely affecting the overall efficiency.

Therefore, the output waveform should be shaped by switching in such a way that the filter requirement, if needed, is minimal.

There are basically two techniques used to shape the output voltage waveform:

- One is to shape the output voltage waveform by switching in such a way as to **selectively eliminate or minimize certain undesirable harmonics**.

- The second method is to shape the voltage waveform in such a way that the **spectrum of harmonic frequencies is totally shifted in the direction of high frequency**. In this case, the filter elements, if required, will be considerably smaller, because the harmonics to be eliminated will all be at high frequencies. The second method is more general and is often favored for many applications.

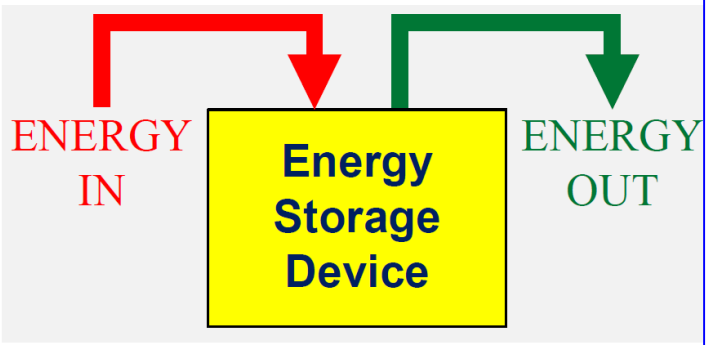
Why high frequency?

- Small size and light weight
- Inductors

$$P_L = E_L f_S = \frac{1}{2} L I_L^{\,2} f_S$$

- Capacitors

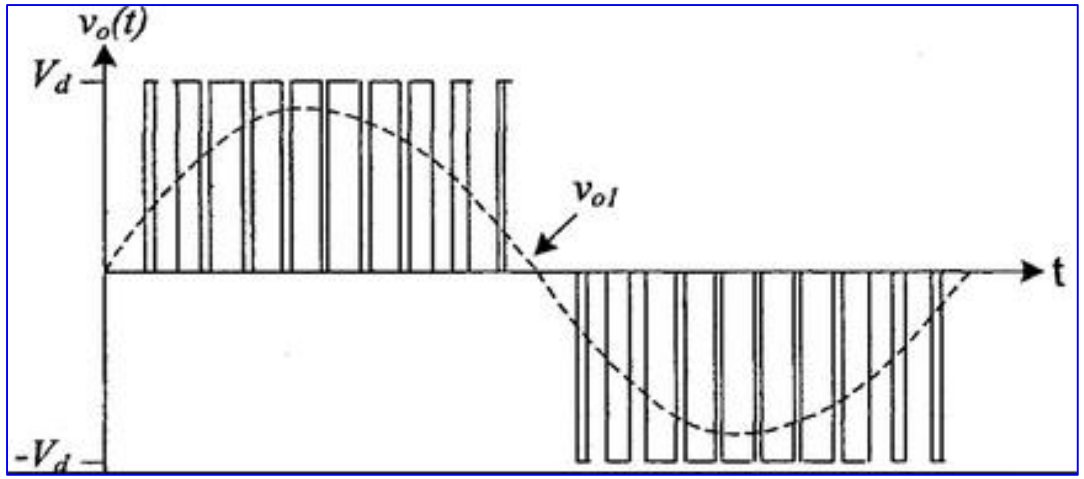
$$P_C = E_C f_S = \frac{1}{2} C V_C^{\,2} f_S$$



Sinusoidal Pulse Width Modulation (SPWM)

The shaping of the output voltage waveform is generally achieved by having multiple pulses in each half-period of the AC waveforms. SPWM is a particular type of multiple-pulse PWM.

In each half-period, the pulse width is maximum in the middle. *From the center, the pulse widths decrease as cosine function towards either side*. In the SPWM technique, voltage control is implemented by varying the widths of all the pulses, at the same time maintaining the cosine relationship.

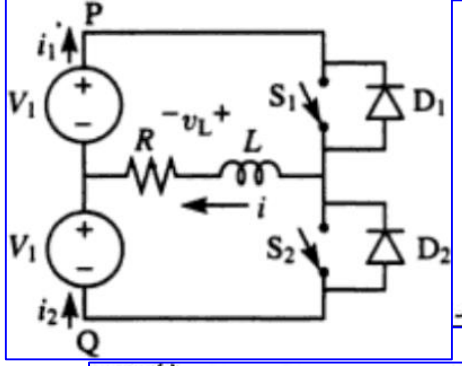


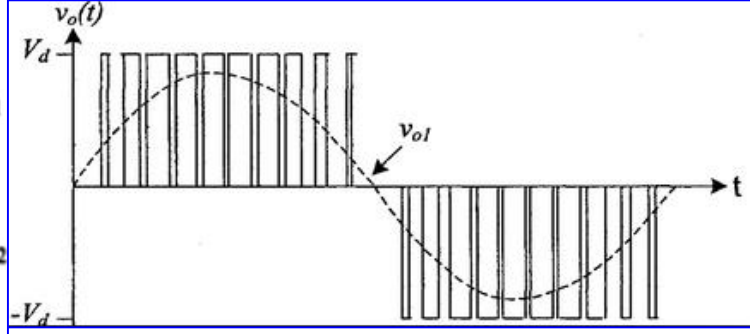
In an SPWM waveform, the total harmonic content is still very significant. But all the harmonic frequencies get shifted towards the high-frequency direction of the frequency spectrum. The order of the harmonics in the SPWM waveform depends on the number of pulses per half-cycle employed. If the pulse repetition frequency employed is made higher, the harmonic frequencies also become higher. The lower frequency harmonics become insignificant.

If the SPWM is implemented with a large number of pulses per half-cycle, the harmonic frequencies will be so large that for many applications, such as motor speed control, no separate filter may be needed on the output side. If a clean sine wave is required for the output voltage, this can be achieved by a filter consisting of only small values of L and C.

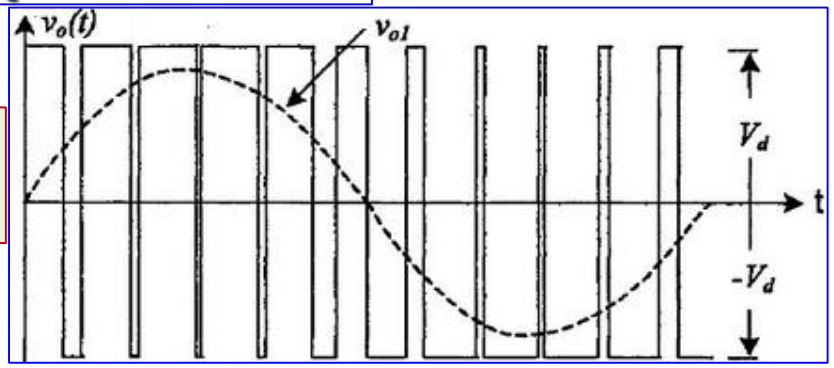
SPWM using the Half-bridge topology

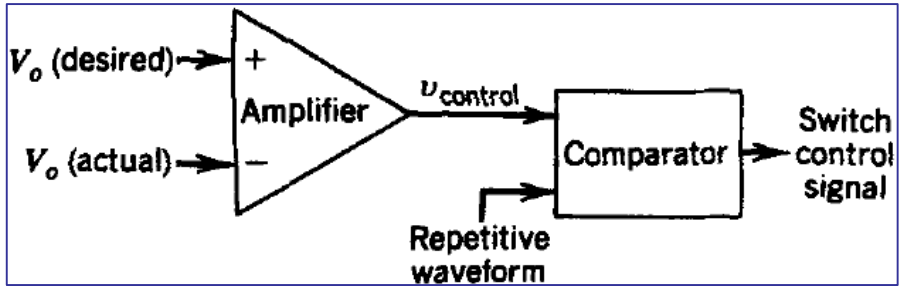
In half-bridge topology, with an inductive load, zero-volt. intervals between successive pulses are not possible.





SPWM can be implemented in the half-bridge also, but with negative voltage excursions.





In the PWM of full-bridge dc-dc converters , a control signal $v_{control}$ was compared with a repetitive switching frequency triangular waveform in order to generate the switching signals. Controlling the switch duty ratios in this way allowed the average dc voltage output to be controlled.

In inverter circuits, in order to produce a sinusoidal output voltage waveform at a desired frequency, a sinusoidal control signal at the desired frequency is compared with a triangular waveform. The frequency of the triangular waveform establishes the inverter switching frequency and is generally kept constant along with its amplitude $\widehat{V}_{tri}$.

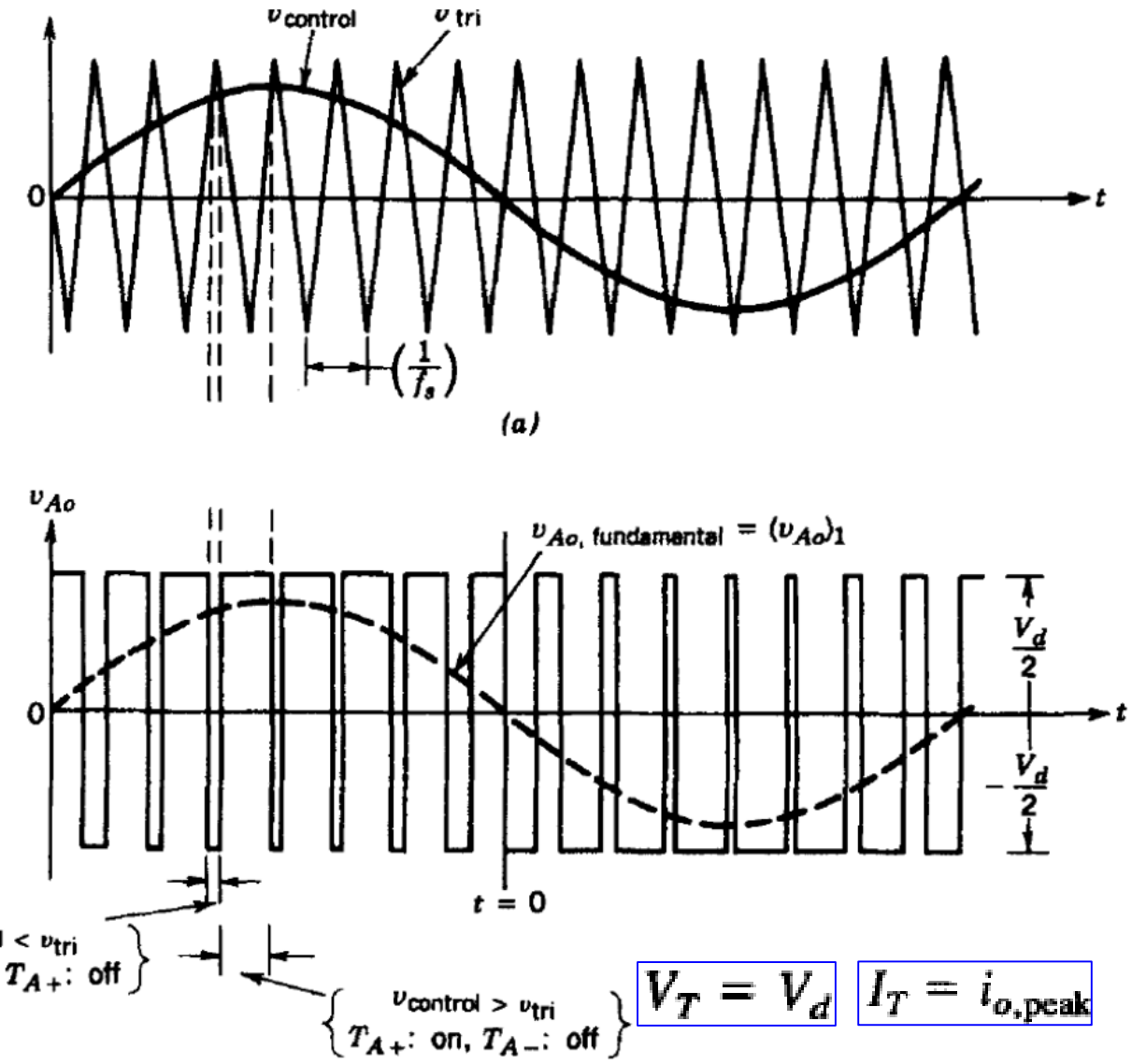
SPWM

$\hat{V}_{tri}$ is at a switching frequency f_s. (f_s is also called the carrier frequency), $v_{control}$ signal is used to modulate the switch duty ratio and has a frequency f_1.

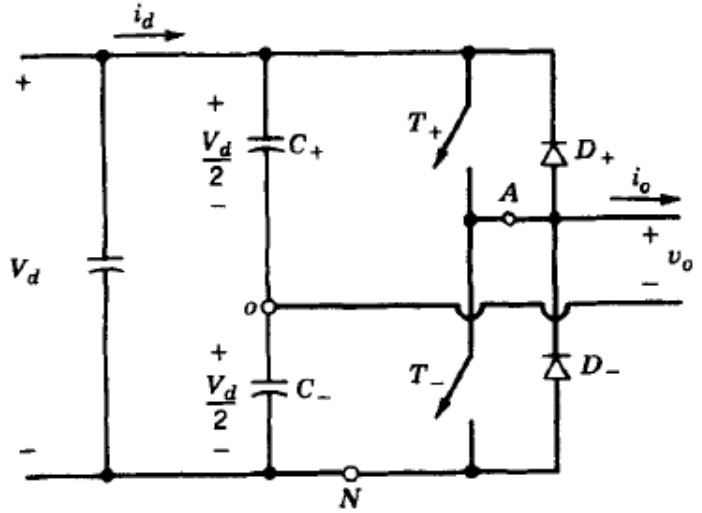
The amplitude modulation index m_a is $m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}}$

Where, $\hat{V}_{control}$ the peak amplitude of the control signal. The amplitude $\hat{V}_{tri}$ of the triangular signal is generally kept constant.

The frequency modulation ratio (index) *mf* : $m_f = \frac{f_s}{f_1}$



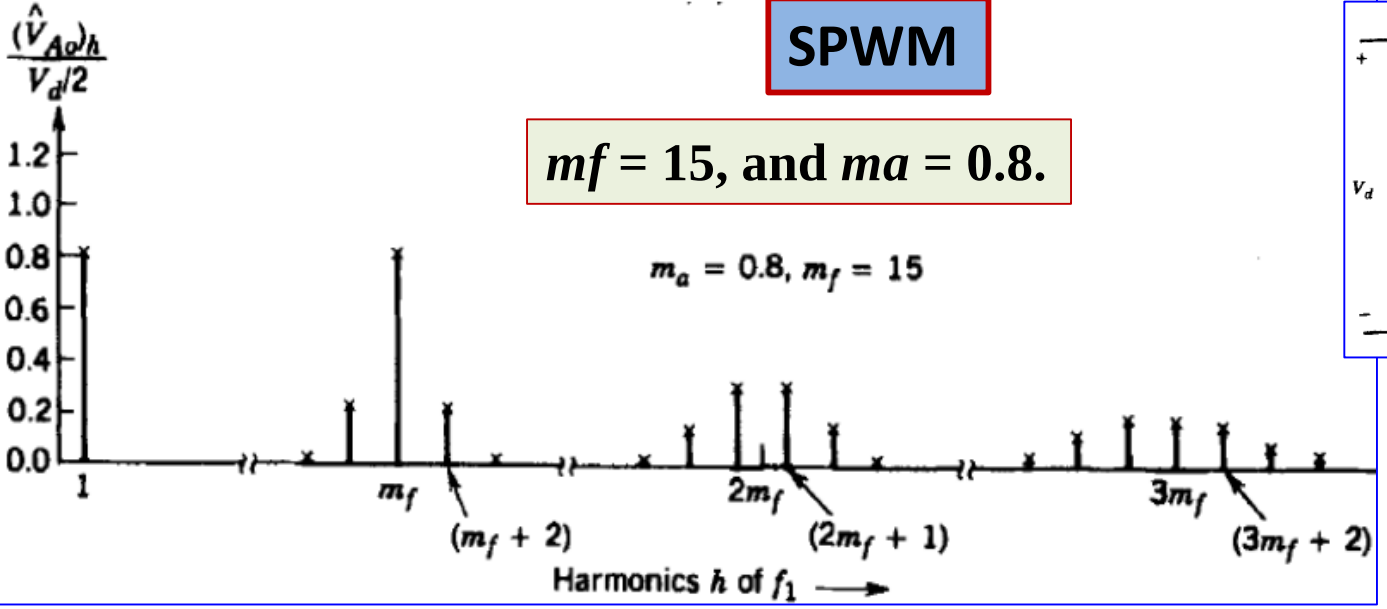
$V_T = V_d$ $I_T = i_{o,peak}$

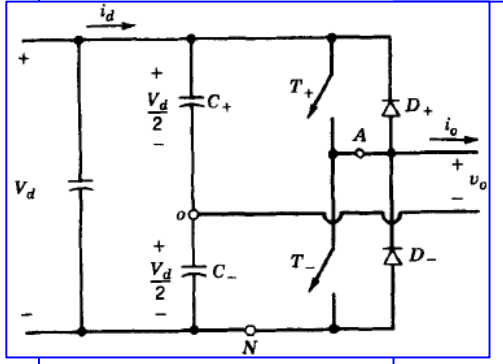


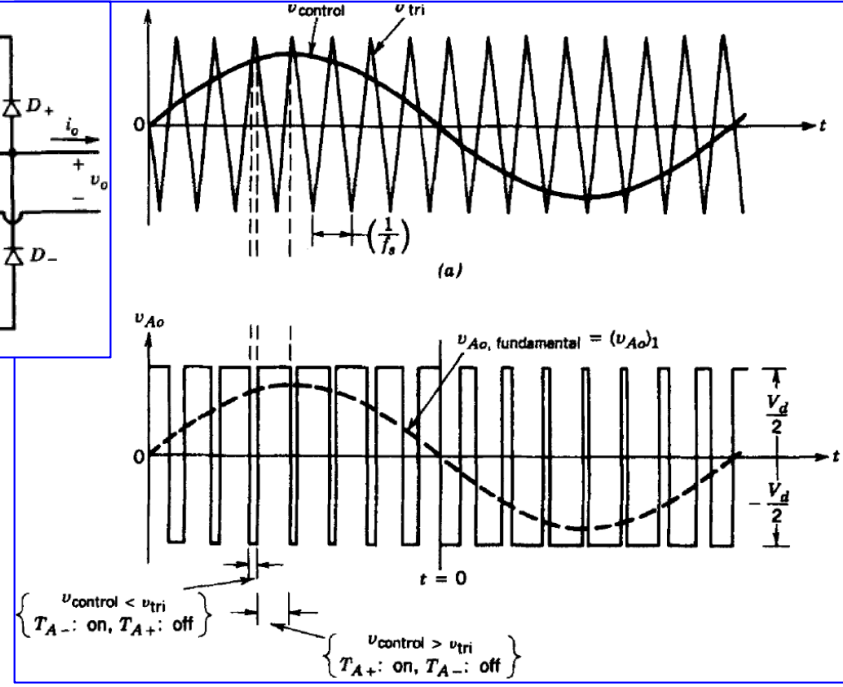
- $v_{control} > v_{tri}$, T_{A+} *is on*, $v_{Ao} = \frac{1}{2}V_d$
- $v_{control} < v_{tri}$, T_{A-} *is on*, $v_{Ao} = -\frac{1}{2}V_d$

SPWM

$mf = 15$, and $ma = 0.8$.

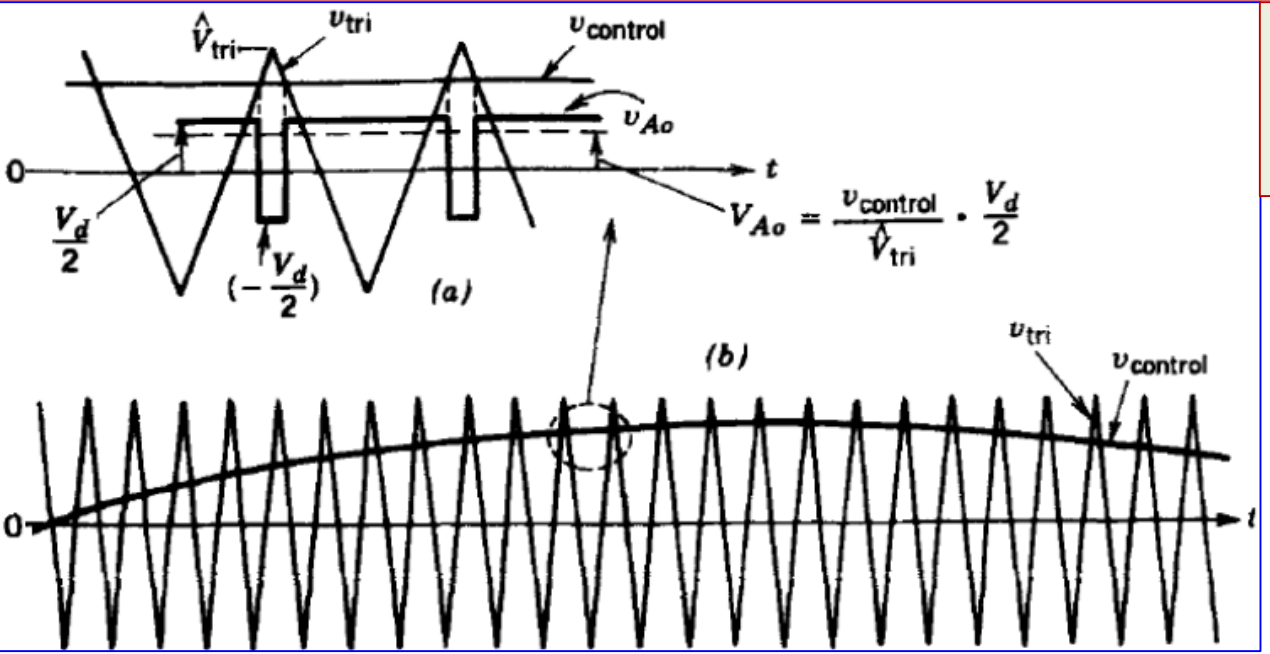






This plot (for *ma* < 1 .O) shows three items of importance:

- **The peak amplitude of the fundamental-frequency component $(\hat{V}_{Ao})_1$ is m_a times $V_d/2$.**



The average output voltage (the output voltage averaged over one switching time period *Ts* = 1/fs) VA0, depends on the ratio of vcontrol to *Vtri* for a given *Vd:*

$$V_{Ao} = \frac{v_{control}}{\hat{V}_{tri}} \frac{1}{2} V_d$$

$$v_{control} \leq \hat{V}_{tri}$$

SPWM

$$V_{Ao} = \frac{v_{control}}{\hat{V}_{tri}} \frac{1}{2} V_d$$

$$v_{control} \leq \hat{V}_{tri}$$

Assuming *vcontrol* to be constant over a switching time period, this eqn. indicates how the "instantaneous average" value of vA0 (averaged over one switching time period *Ts)* varies from one switching time period to the next. This "instantaneous average" is the same as the fundamental-frequency component of vA0.

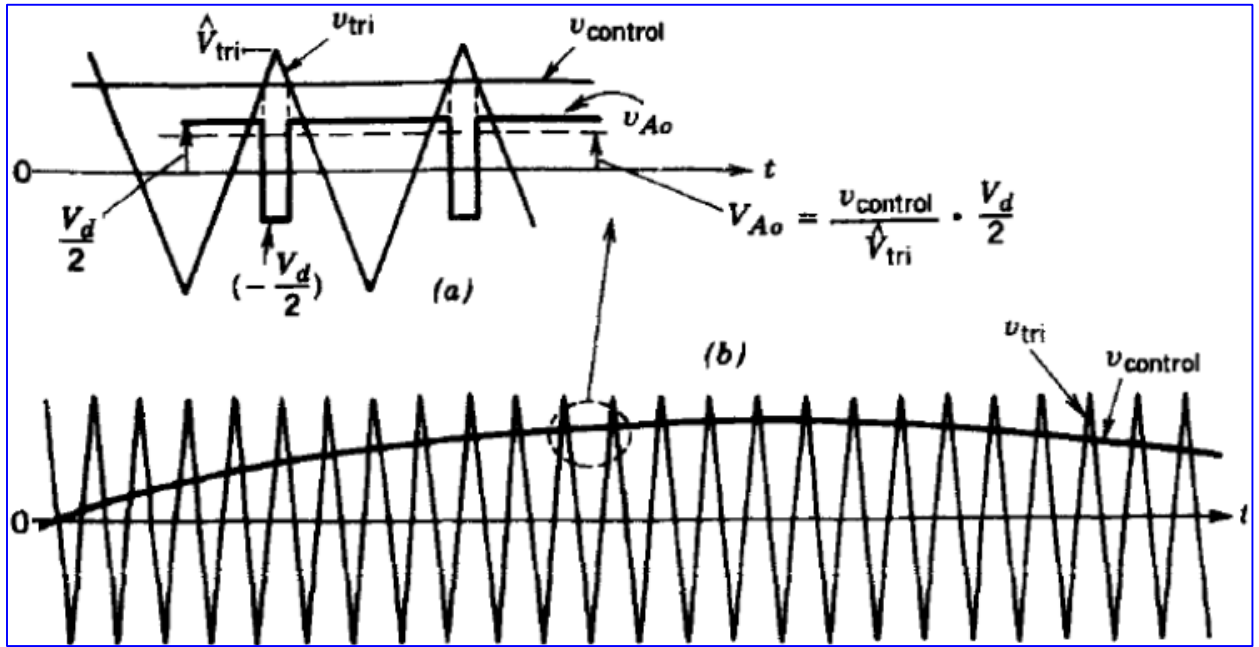
That's why vcontrol is chosen to be sinusoidal to provide a sinusoidal output voltage with fewer harmonics.

Let vcontrol vary sinusoidally at $f_1 = \omega_1/2\pi$, which is the fundamental freq. of inverter output:

$$v_{control} = \hat{V}_{control} \sin \omega_1 t, \qquad \text{where } \hat{V}_{control} \leq \hat{V}_{tri}$$

The fund. Freq. comp. $(v_{Ao})_1$ varies sinusoidally and in phase with *vcontrol* as a function of time.

$$(v_{Ao})_1 = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \sin \omega_1 t \frac{V_d}{2} \Rightarrow (v_{Ao})_1 = m_a \sin \omega_1 t \frac{V_d}{2} \text{ for } m_a \leq 1.0$$



$$Therefore, \ (\hat{V}_{Ao})_1 = m_a \frac{V_d}{2}$$
$$m_a \leq 1.0$$

It shows that in SPWM, the amplitude of the output voltage fundamental-frequency component varies linearly with m_a (provided $ma \leq 1.0$). Therefore, the range of m_a from 0 to 1 is referred to as the linear range.

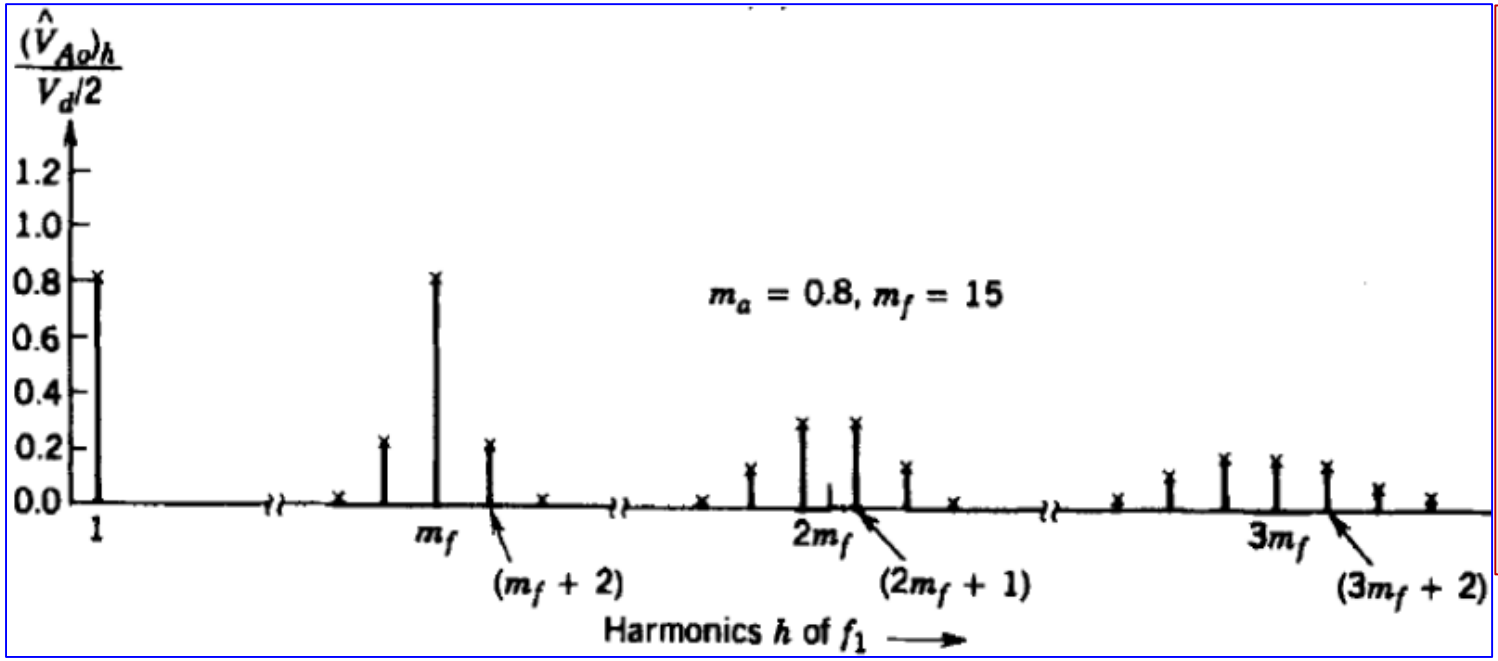
SPWM

2. The harmonics in the inverter output voltage waveform appear as sidebands, centered around the switching frequency and its multiples, that is, around harmonics *mf, 2mf, 3mf,* and so on. This general pattern holds true for all values of *ma* in the range 0 - 1.

For $m_f \geq 9$, the harmonic amplitudes are almost independent of m_f, though m_f defines the frequencies at which they occur.

The frequencies at which voltage harmonics occur can be indicated as $f_h = (jm_f \pm k)f_1$

that is, the harmonic order *h* corresponds to the kth sideband of *j* times the frequency modulation ratio m_f. $h = j(m_f) \pm k$, **where the fundamental frequency corresponds to *h* = 1 . For odd values of *j* , the harmonics exist only for even values of *k*. For even values of *j* , the harmonics exist only for odd values of *k*.**

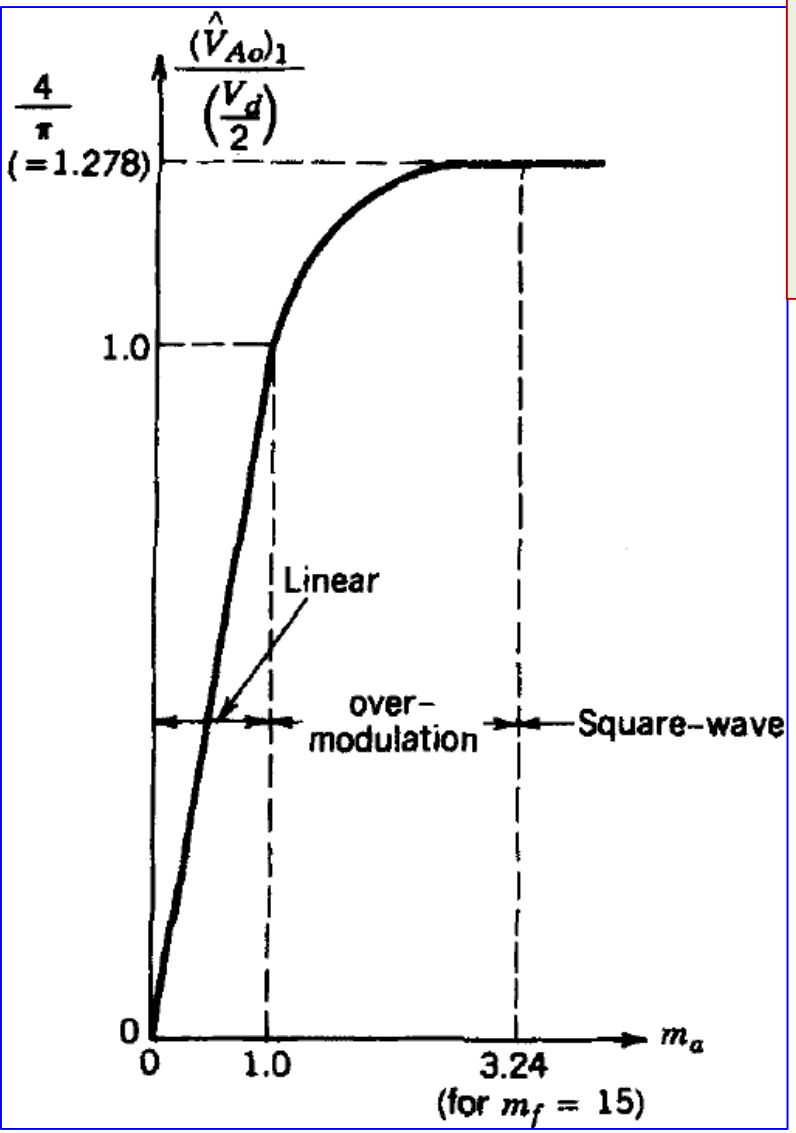


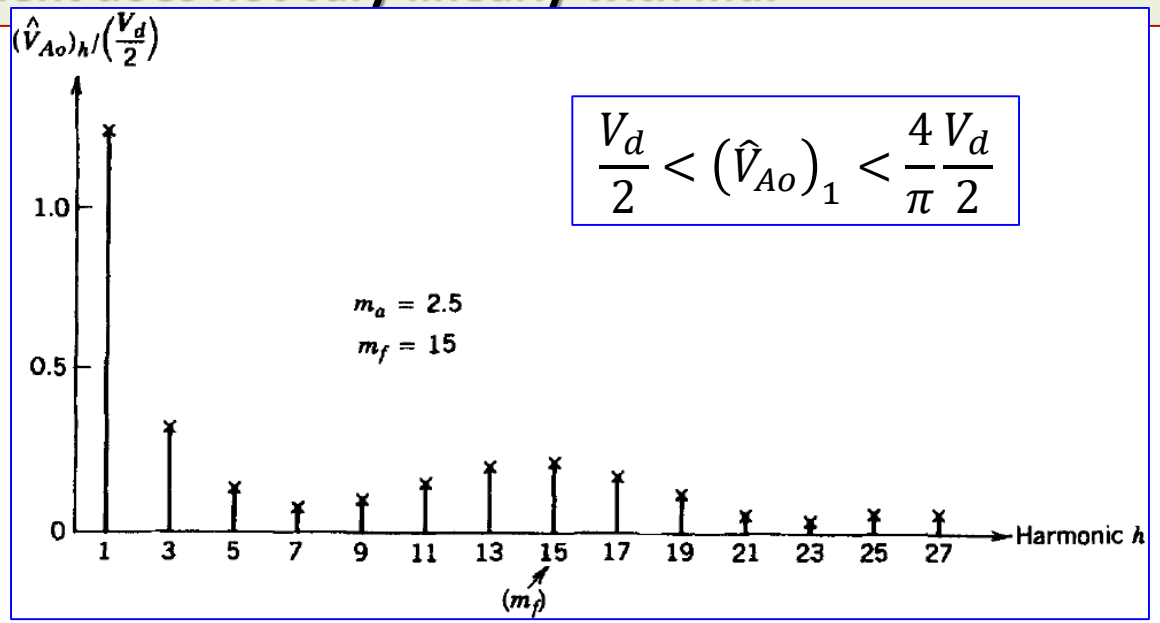
- **The harmonic *mf* should be an odd integer. Choosing *mf* as an odd integer results in an odd symmetry [*f (- t) = -f(t)*] as well as a half-wave symmetry [*f (t) = -f(t +T$_1$/2*]. Therefore, only odd harmonics are present and the even harmonics disappear from the waveform of v_{A0}. Moreover, only the coefficients of the sine series in the Fourier analysis are finite; those for the cosine series are zero.**

SPWM

To increase further the amplitude of the fundamental-frequency component in the output voltage, *ma* is increased beyond 1.0, resulting in what is called *overmodulation.*

Overmodulation causes the output voltage to contain many more harmonics in the sidebands as compared with the linear range (with ma ≤ 1.0). The harmonics with dominant amplitudes in the linear range may not be dominant during overmodulation. More significantly, with overmodulation, the amplitude of the fundamental-frequency component does not vary linearly with *ma*.





$$\frac{V_d}{2} < (\hat{V}_{Ao})_1 < \frac{4}{\pi}\frac{V_d}{2}$$

- The overmodulation region is avoided in uninterruptible power supplies because of a stringent requirement on minimizing the distortion in the output voltage.
- In induction motor drives, overmodulation is normally used.

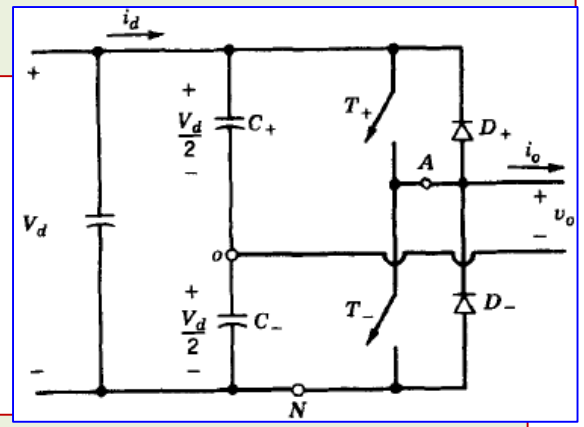
SQUARE-WAVE SWITCHING SCHEME

In the square-wave switching scheme, each switch of the inverter leg is on for one half-cycle (180^0) of the desired output frequency. From Fourier analysis, the peak values of the fundamental-frequency and harmonic components in the inverter output waveform can be obtained for a given input vd as

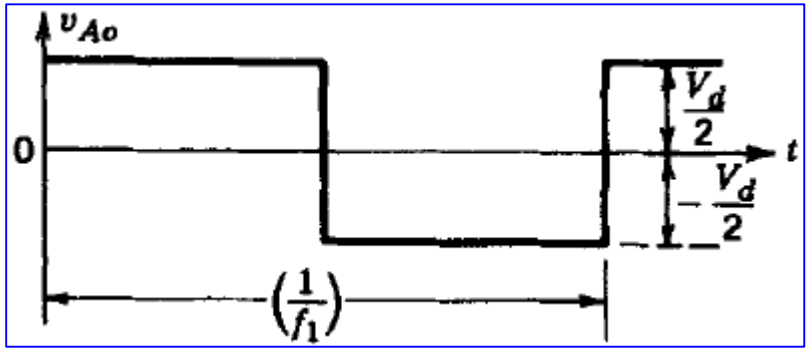
$$\left(\hat{V}_{Ao}\right)_1 = \frac{4}{\pi}\frac{V_d}{2} = 1.273\left(\frac{V_d}{2}\right)$$

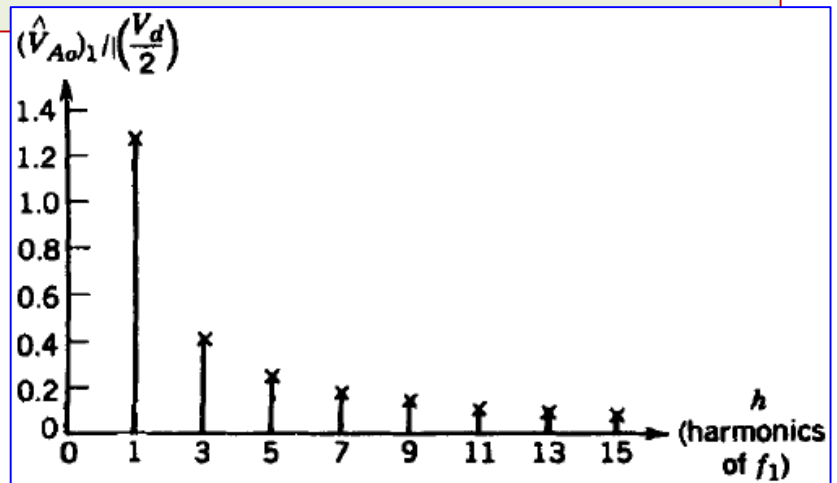
$$\left(\hat{V}_{Ao}\right)_h = \frac{\left(\hat{V}_{Ao}\right)_1}{h}$$

where the harmonic order h takes on only odd values.

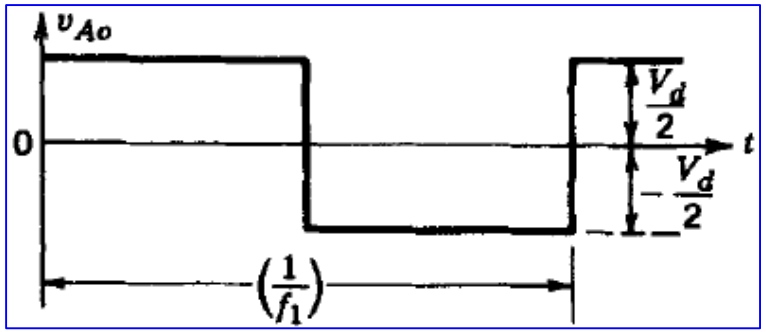


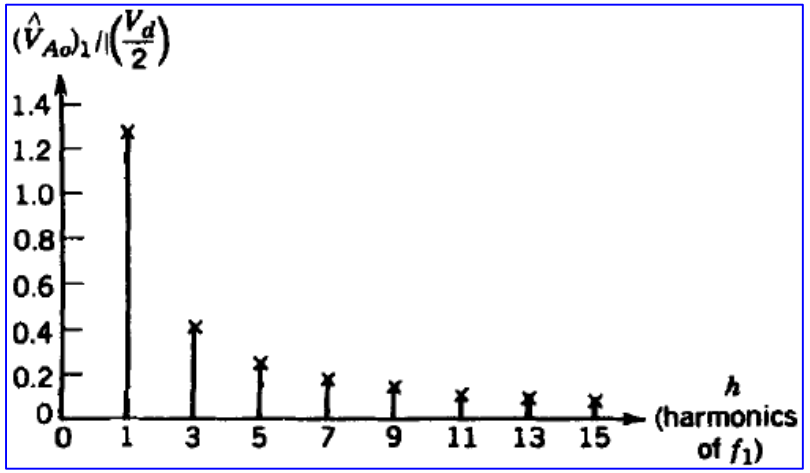
The square-wave switching is also a special case of SPWM switching when *ma* becomes so large that the control voltage waveform intersects with the triangular waveform only at the zero crossing of vcontrol. Therefore, the output voltage is independent of *ma* in the square-wave region.





SQUARE-WAVE SWITCHING SCHEME



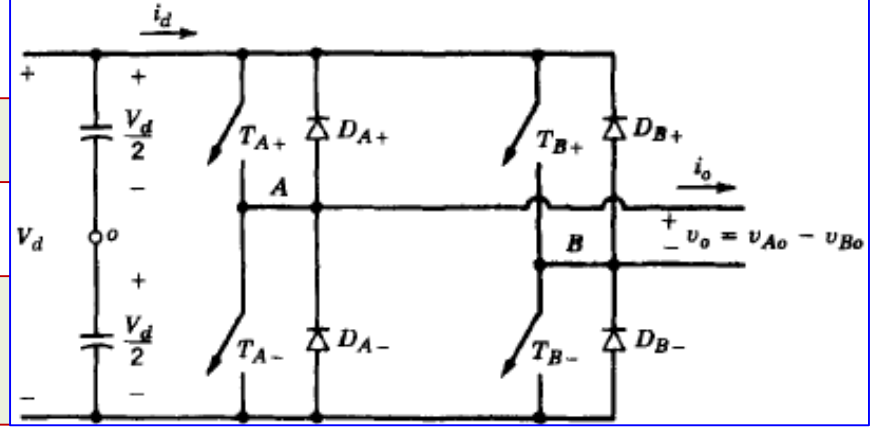


One of the advantages of the square-wave operation is that each inverter switch changes its state only twice per cycle, which is important at very high power levels where the solid-state switches generally have slower turn-on and turn-off speeds.

One of the serious disadvantages of square-wave switching is that the inverter is not capable of regulating the output voltage magnitude. Therefore, the dc input voltage Vd to the inverter must be adjusted in order to control the magnitude of the inverter output voltage.

THE FULL-BRIDGE INVERTER

The FB can be operated with or without PWM.



Operation without PWM with RL load

When S1 and S4 are ON and the other two are OFF, the loop equation will be: $L\frac{di}{dt} + Ri = V_1$

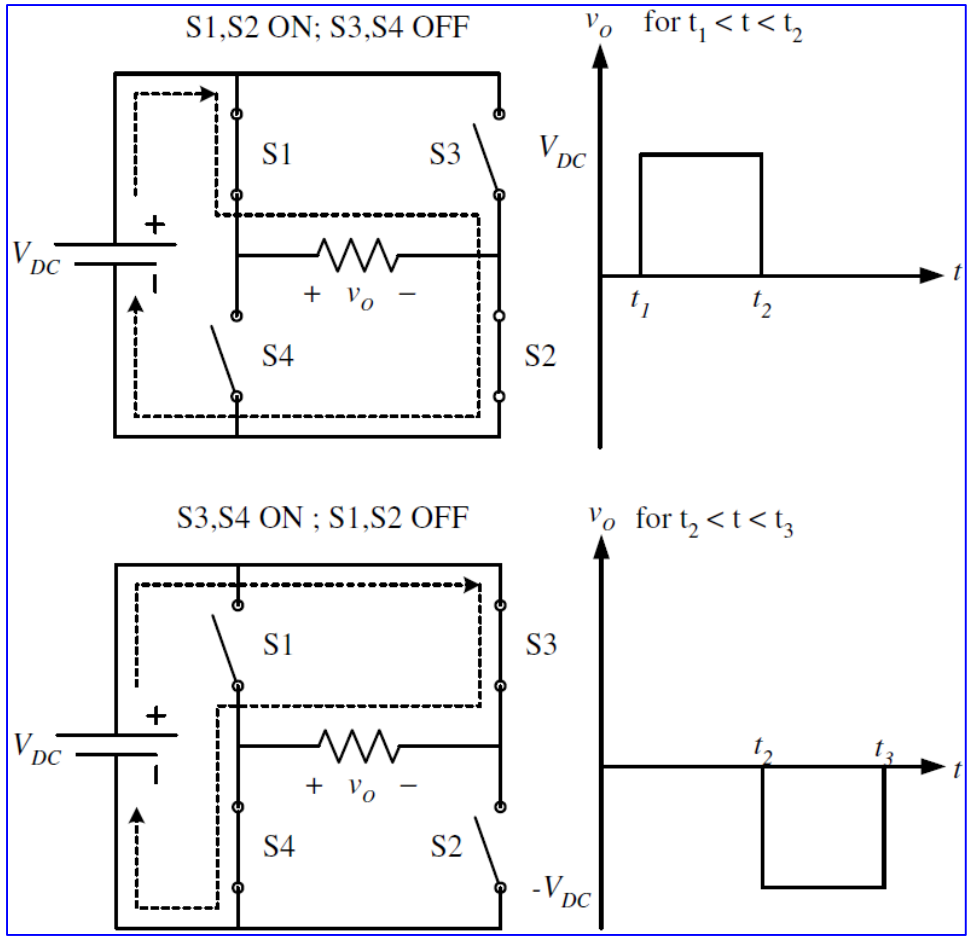
Similarly, when S2 and S3 are ON and the other two are OFF, $L\frac{di}{dt} + Ri = -V_1$

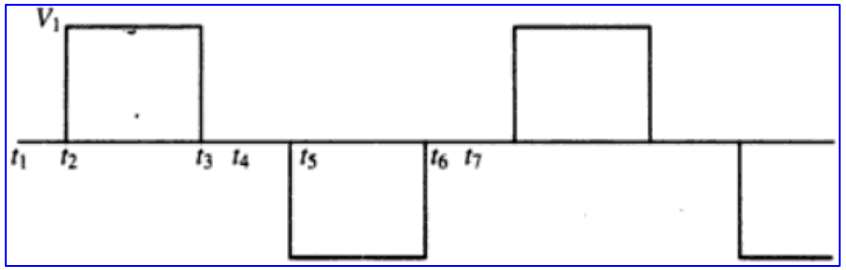
These equations are identical to those that we wrote earlier for the half-bridge inverter, except for the fact that for the latter we used the voltage V1, which is the voltage of one section of the split power supply. The full bridge does not need a split power supply, and in these equations, V1 is the full DC voltage supply to the bridge.

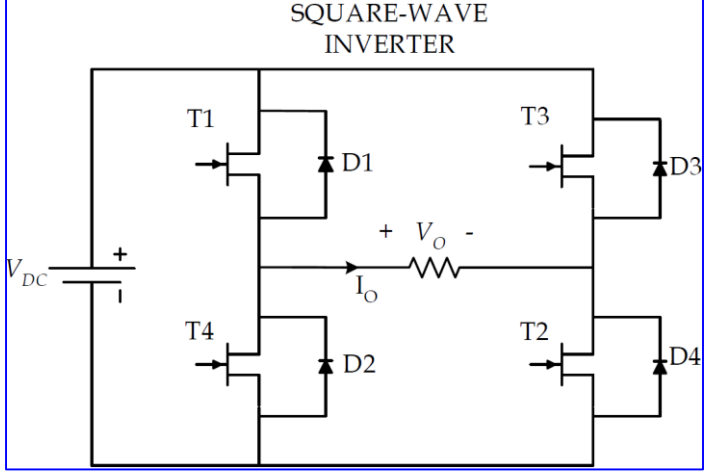
Just as we saw for the half-bridge, for the full-bridge also there will be an initial current build up period, after which we may assume repetitive conditions. The expressions for the current will be the same as we got earlier for the half-bridge, with V1 being the full DC voltage. Therefore, with repetitive conditions, the expression for the load current, *I* will be: $i = -\frac{V_1}{R}\frac{1-e^{-T/2\tau}}{1+e^{-T/2\tau}}e^{-t/\tau} + \frac{V_1}{R}(1-e^{-t/\tau})$ $\tau = L/R$

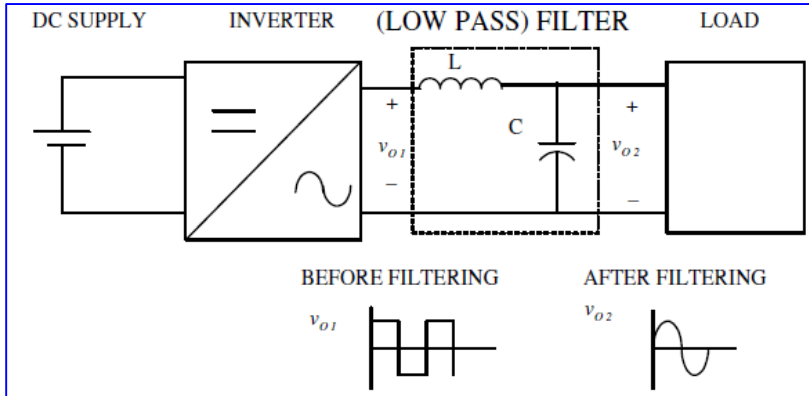
For the negative voltage half-period, the expression for i will be the same, with the sign reversed for V and the reference zero for t as the instant of commencement of this half-period.

THE FULL-BRIDGE INVERTER









- Output of the inverter is "chopped AC voltage with zero DC component". It contain **harmonics.**
- An **LC section low-pass filter** is normally fitted at the inverter output to reduce the high frequency harmonics.
- In some applications such as UPS, "*high purity*" sine wave output is required. Good filtering is a must.
- In some applications such as AC motor drive, filtering is not required.

THE FULL-BRIDGE INVERTER

PWM with Bipolar Voltage Switching

(TA+, TB-) **and** ***(TA-, TB+)*** **from the two legs are switched as switch pairs 1 and 2.**

The output voltage waveform of leg A is identical to the output of the basic one-leg inverter, which is determined in the same manner by comparison of *vcontrol* and *vtri*.

The output of inverter leg B is negative of the leg A output; for example, when *TA+* is on and *vA0* is equal to *+1/2 Vd* , *TB-* is also on and *vB0 = - 1/2 Vd.*

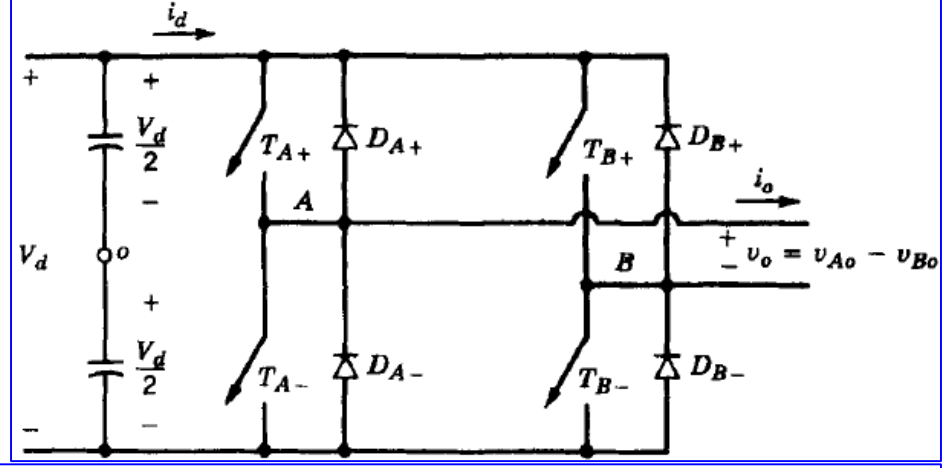
Therefore,

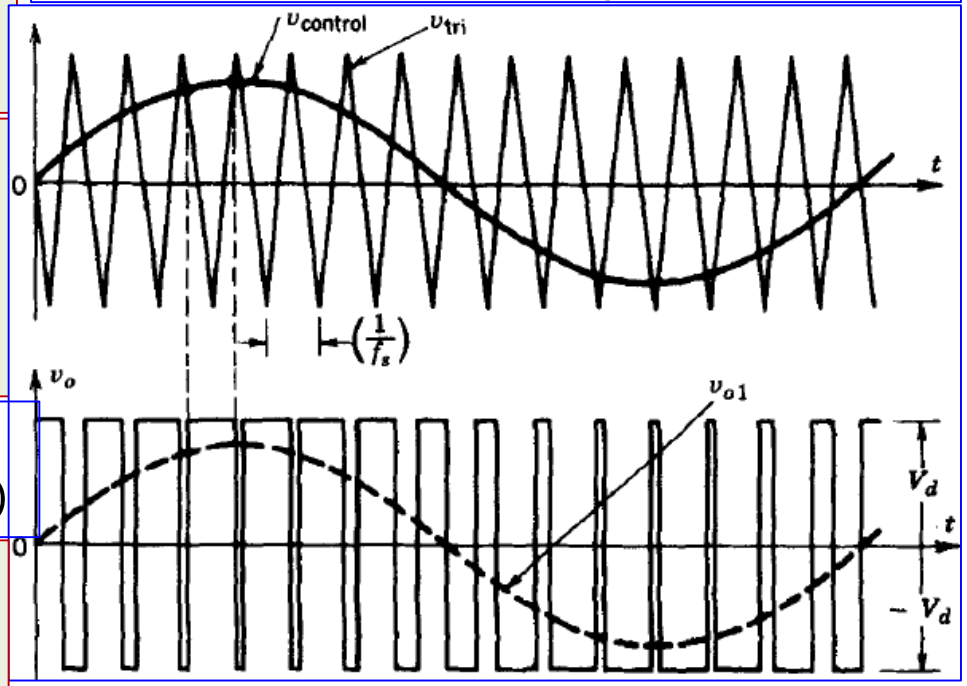
$$v_{Bo}(t) = -v_{Ao}(t)$$
$$v_o(t) = v_{Ao}(t) - v_{Bo}(t) = 2v_{Ao}(t)$$

The analysis carried out for the basic one-leg inverter completely applies to this type of PWM switching.

Therefore,

$$\hat{V}_{o1} = m_a V_d \qquad (m_a \le 1.0)$$
$$V_d < (\hat{V}_{Ao})_1 < \frac{4}{\pi} V_d \qquad (m_a > 1.0)$$

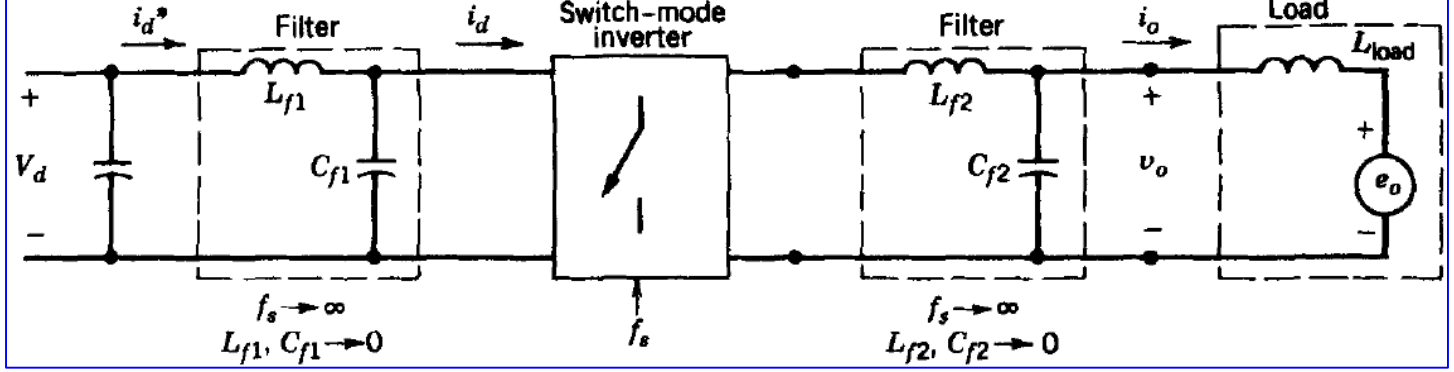




dc-Side Current i_d

With assumptions,

$$v_{o1} = v_o$$
$$= \sqrt{2}V_o \sin \omega_1 t$$



If e0 is a sine wave at frequency w1, then the output current would also be sinusoidal and would lag *v0* for an inductive load such as an ac motor:

$i_o = \sqrt{2}I_o \sin(\omega_1 t - \phi)$; where ϕ is the angle by which i_o lags v_o.

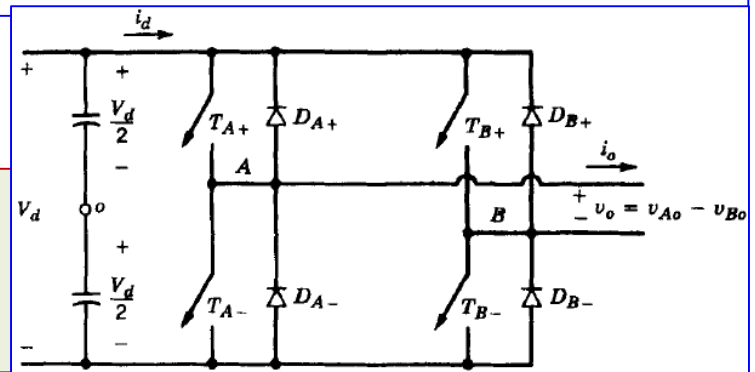
On the dc side, the *L-C* filter will filter the high-switching-frequency components in i_d, and i_d^* would only consist of the low-frequency and dc components.

Assuming that no energy is stored in the filters,

$$v_d i_d^*(t) = v_o(t) i_o(t) = \sqrt{2}V_o \sin \omega_1 t \sqrt{2} I_o \sin(\omega_1 t - \phi)$$

$$i_d^*(t) = \frac{V_o I_o}{V_d} \cos \phi - \frac{V_o I_o}{V_d} \cos(2\omega_1 t - \phi) = I_d + i_{d2} = I_d - \sqrt{2} I_{d2} \cos(2\omega_1 t - \phi)$$

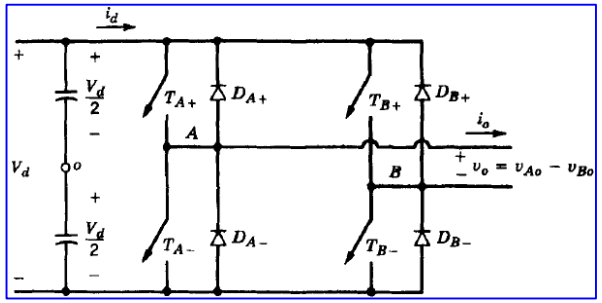
$$I_d = \frac{V_o I_o}{V_d} \cos \phi \qquad I_{d2} = \frac{1}{\sqrt{2}} \frac{V_o I_o}{V_d}$$

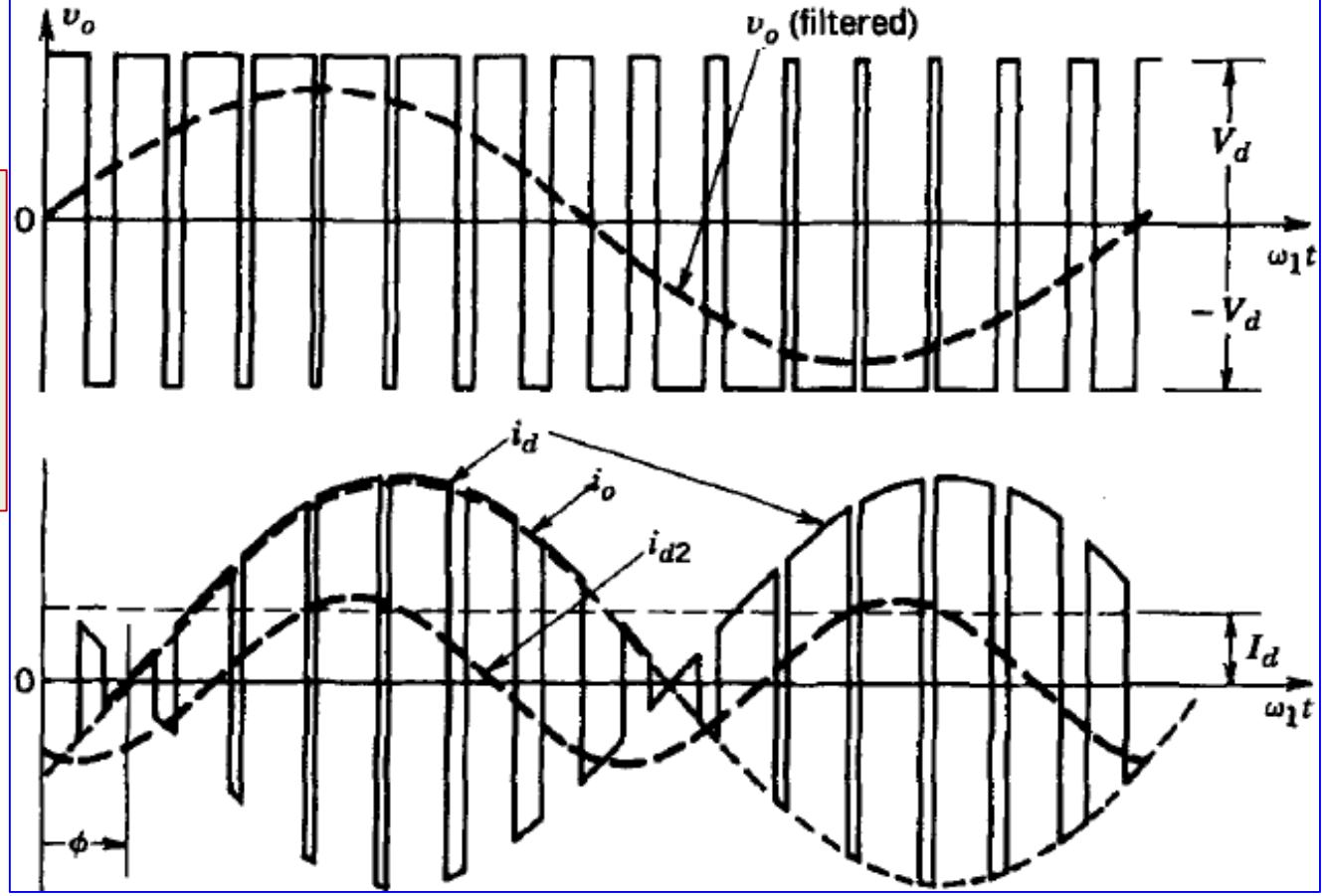


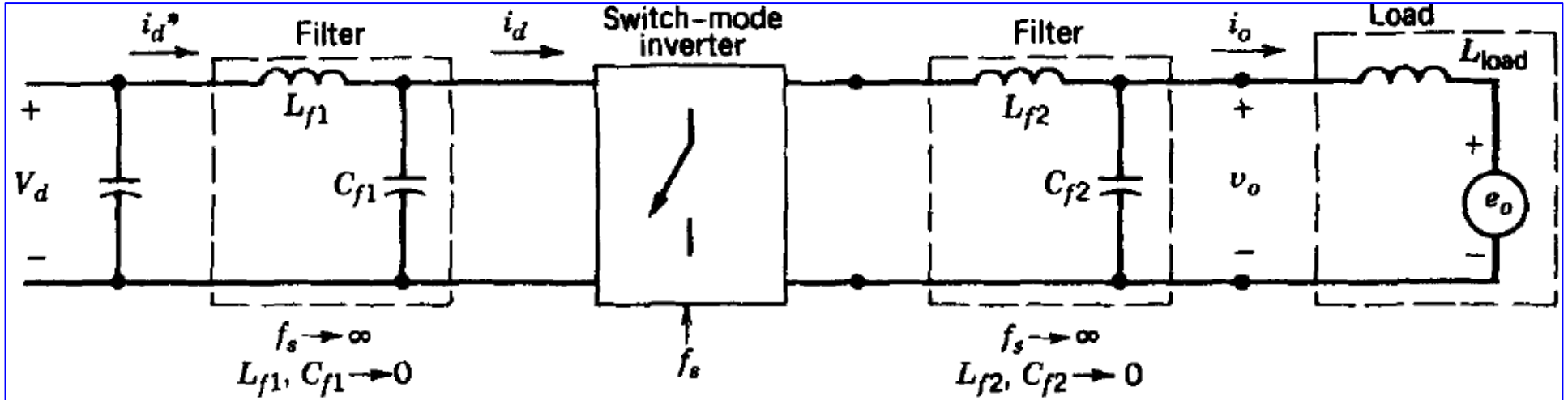
i_d^* consists of a dc component i_d (responsible for power transfer), and a sinusoidal component at twice the fundamental frequency.

dc-Side Current i_d

The inverter input current i_d consists of i_d* and the high-frequency components due to inverter switching.





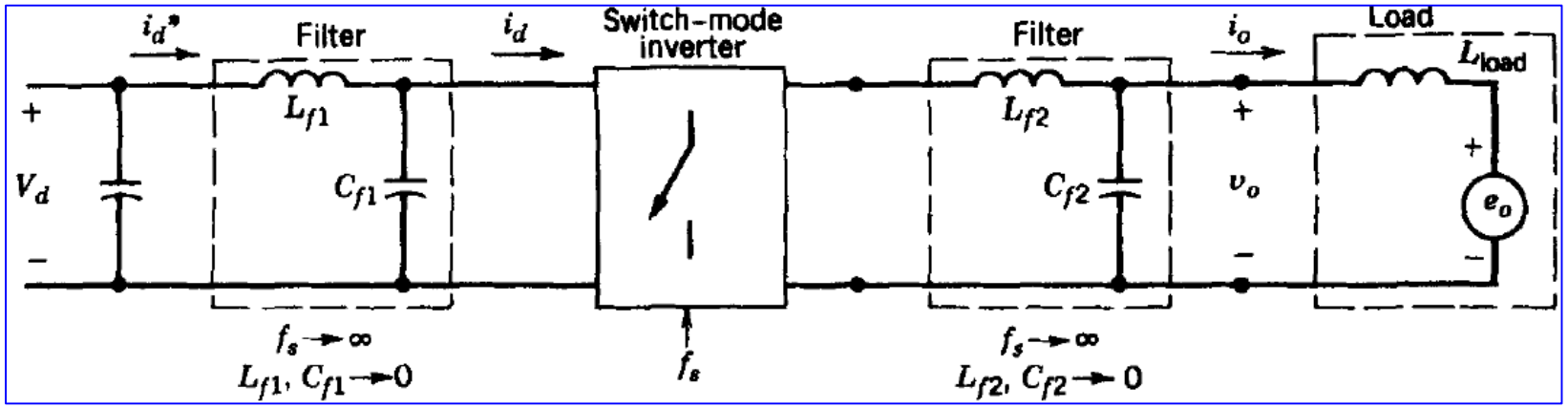


dc-Side Current i_d

- In practical systems, the previous assumption of a constant dc voltage as the input to the inverter is not entirely valid. Normally, this dc voltage is obtained by rectifying the ac utility line voltage.
- A large capacitor is used across the rectifier output terminals to filter the dc voltage. The ripple in the capacitor voltage, which is also the dc input voltage to the inverter, is due to *two* reasons:

  (1) The rectification of the line voltage to produce dc does not result in a pure dc, dealing with the line-frequency rectifiers.

  (2) As shown earlier, the current drawn by a single-phase inverter from the dc side is not a constant dc but has a second harmonic component (of the fundamental frequency at the inverter output) in addition to the high switching- frequency components.
- The second harmonic current component results in a ripple in the capacitor voltage, although the voltage ripple due to the high switching frequencies is essentially negligible.



PWM with Unipolar Voltage Switching

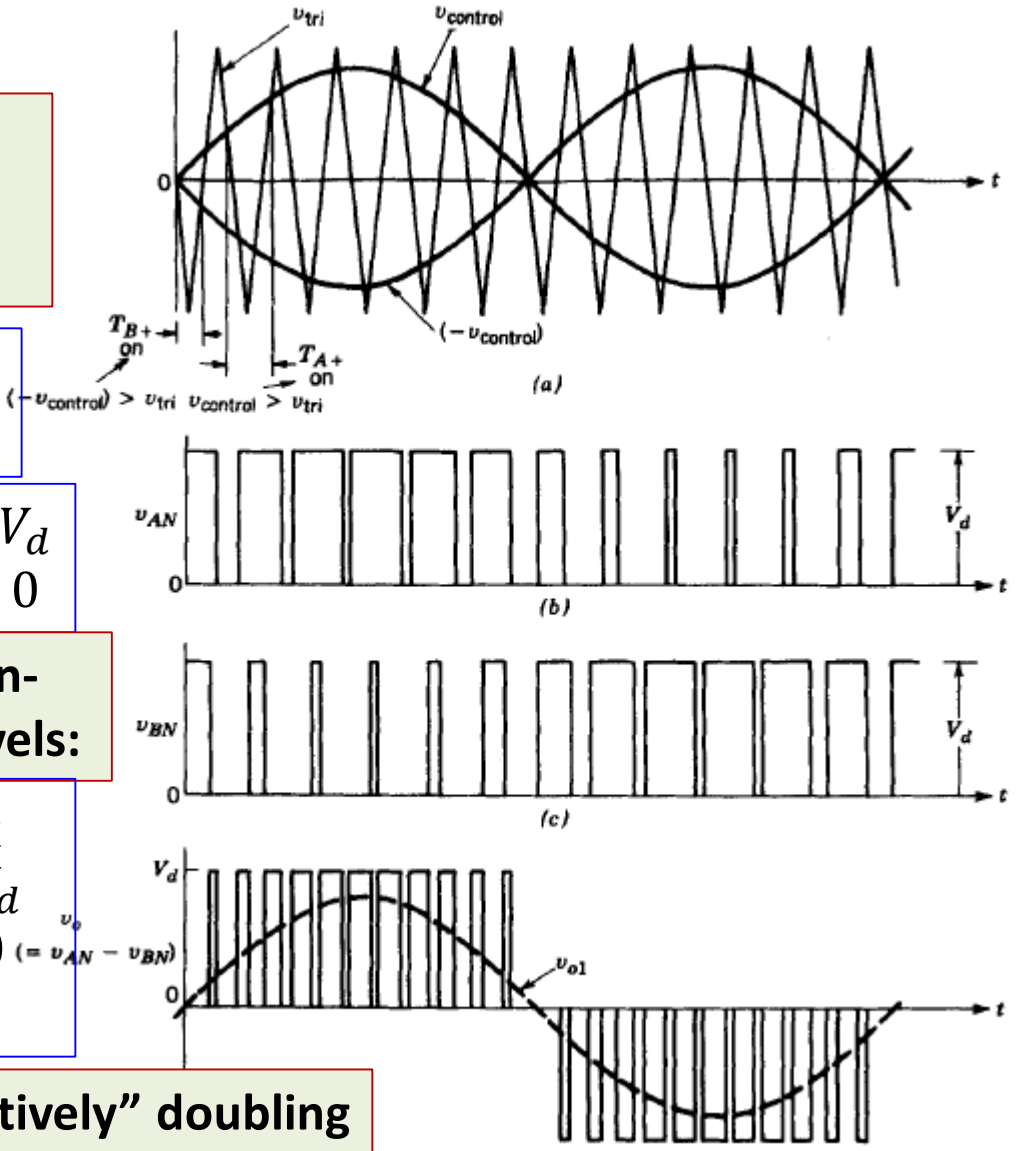
Legs A and B of the full-bridge inverter are controlled separately by comparing v_{tri} with $v_{control}$ and $-v_{control}$, respectively.

$$v_{control} > v_{tri}; T_{A+}\ on\ \ and\ \ V_{AN} = V_d$$
$$v_{control} < v_{tri}; T_{A-}\ on\ \ and\ \ V_{AN} = 0$$

$$(-v_{control}) > v_{tri}; T_{B+}\ on\ \ and\ \ V_{BN} = V_d$$
$$(-v_{control}) < v_{tri}; T_{B-}\ on\ \ and\ \ V_{BN} = 0$$

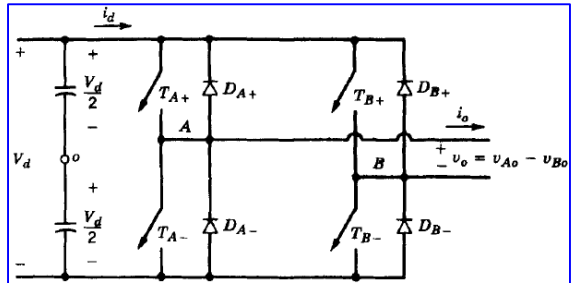
There are four combinations of switch on-states and the corresponding voltage levels:

$$T_{A+}, T_{B-}\ on: v_{AN} = V_d, v_{BN} = 0; v_o = V_d$$
$$T_{A-}, T_{B+}\ on: v_{AN} = 0, v_{BN} = V_d; v_o = -V_d$$
$$T_{A+}, T_{B+}\ on: v_{AN} = V_d, v_{BN} = V_d; v_o = 0$$
$$T_{A-}, T_{B-}\ on: v_{AN} = 0, v_{BN} = 0; v_o = 0$$

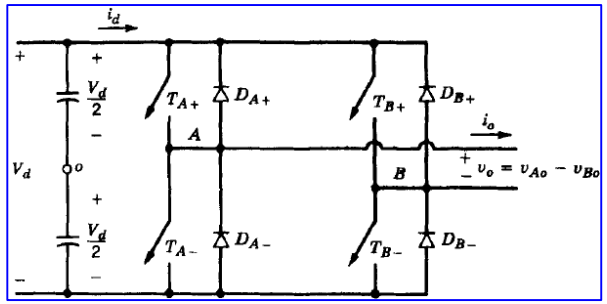


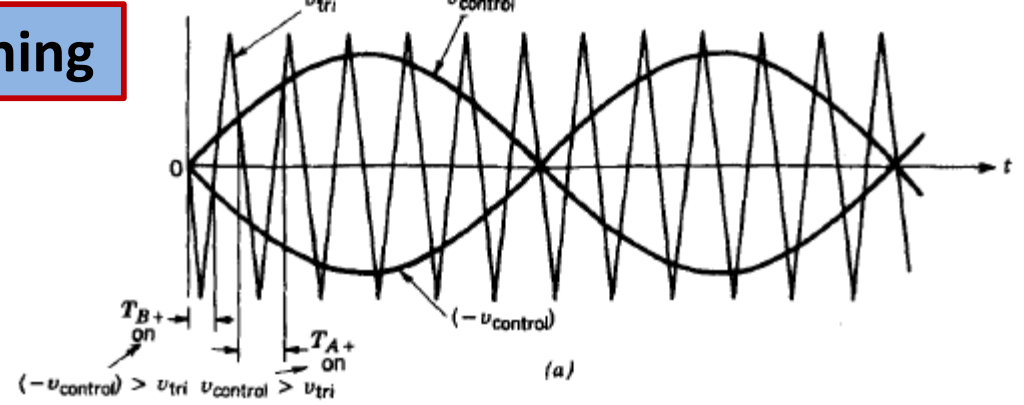
This scheme has the advantage of "effectively" doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar scheme.

The output voltage jumps at each switching are reduced to v_d, as compared to $2V_d$ in the bipolar scheme.



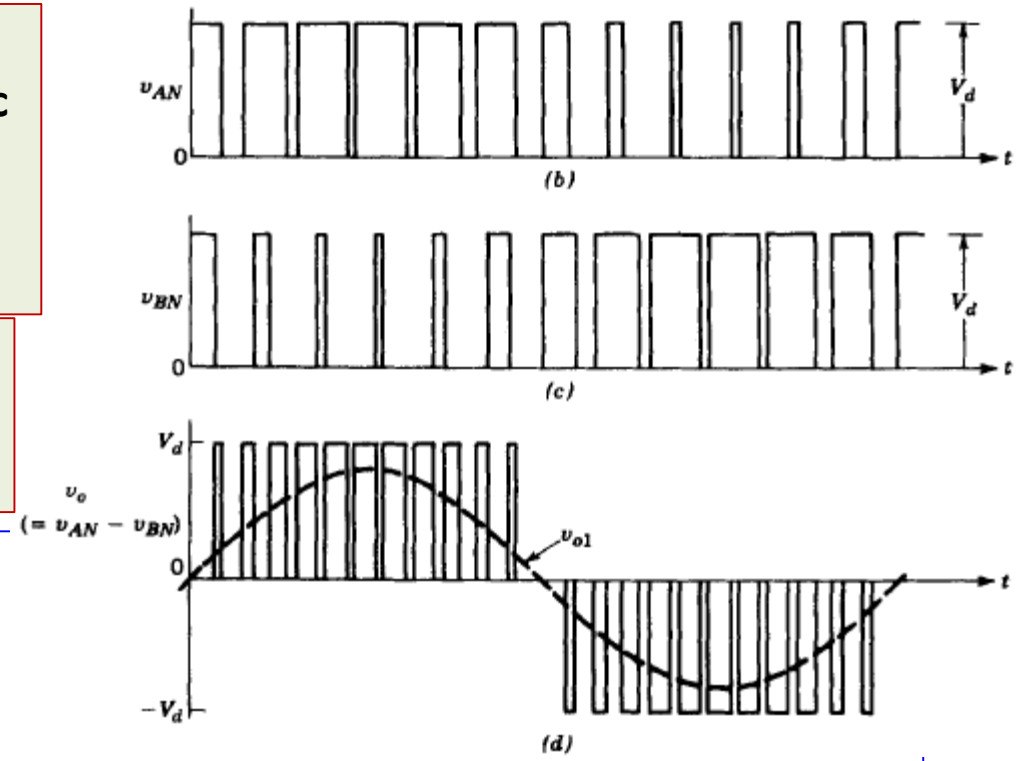
PWM with Unipolar Voltage Switching

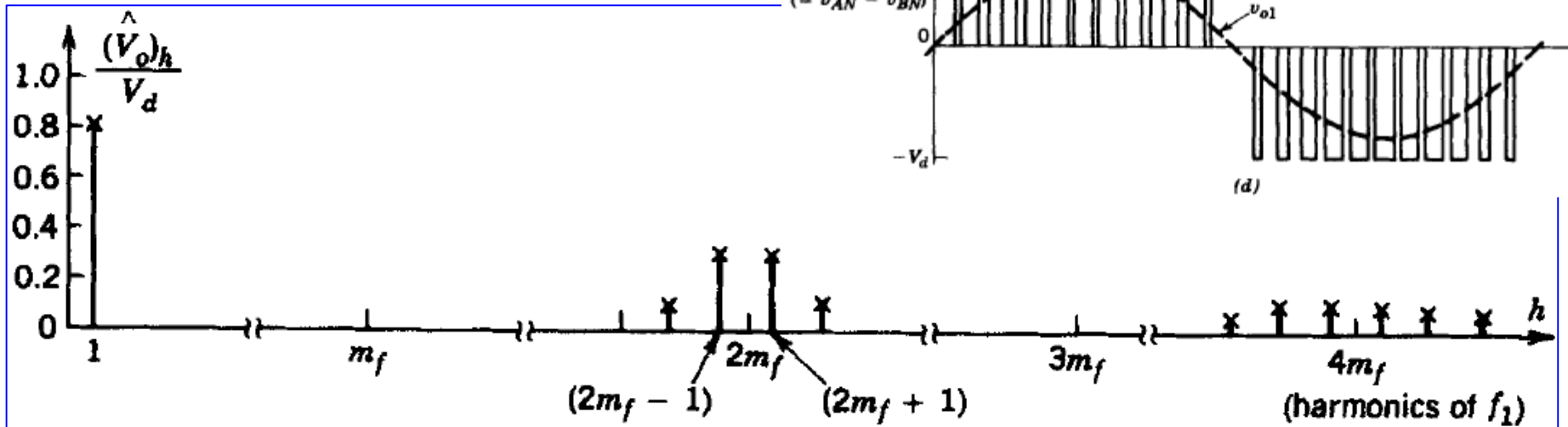




The advantage of "effectively" doubling the switching frequency appears in the harmonic spectrum of the output voltage waveform, where the lowest harmonics appear as sidebands of twice the switching frequency.

Let's choose *mf* to be even *(mf* should be odd for PWM with bipolar voltage switching) in a single-phase inverter.



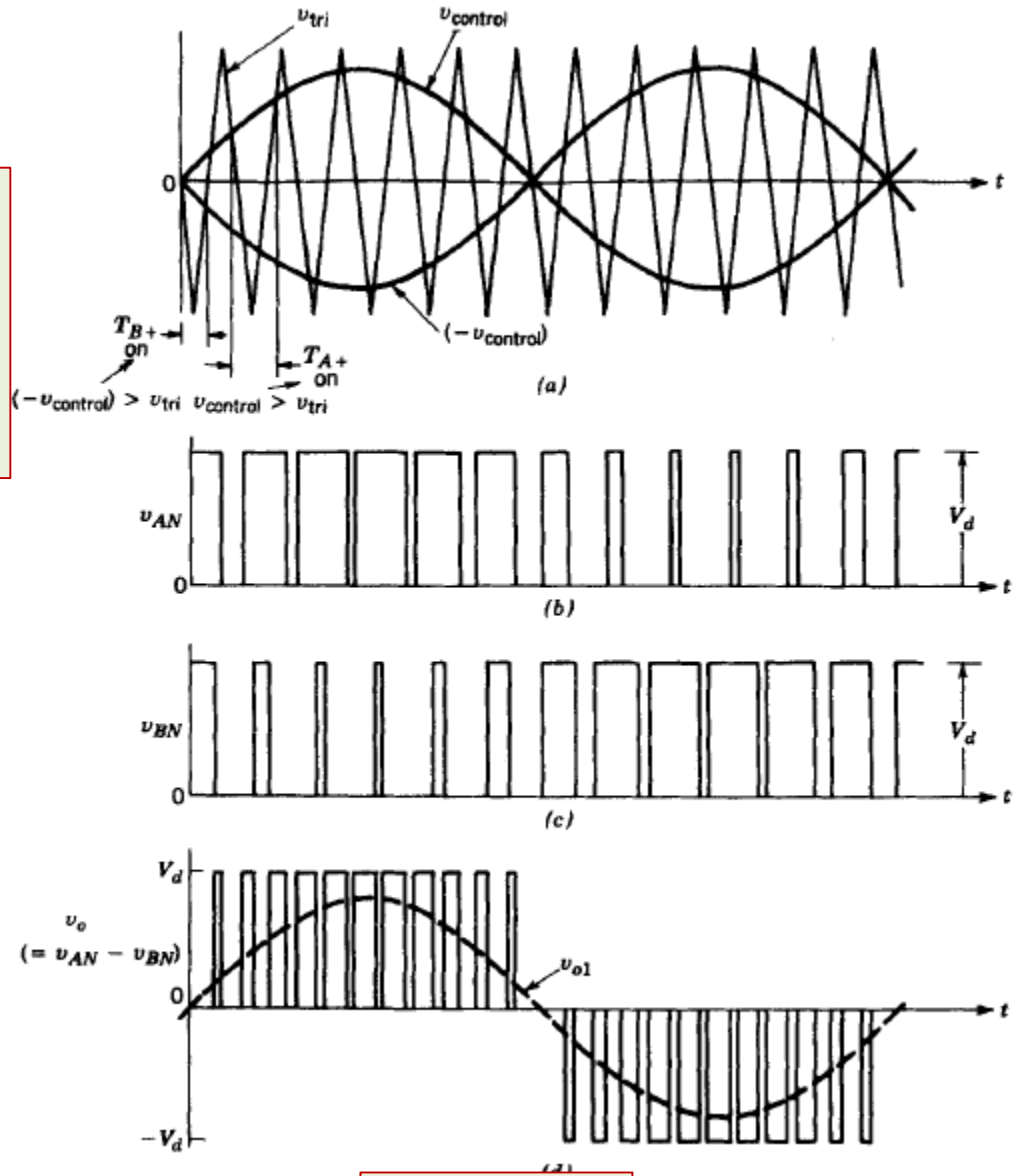


PWM with Unipolar Voltage Switching

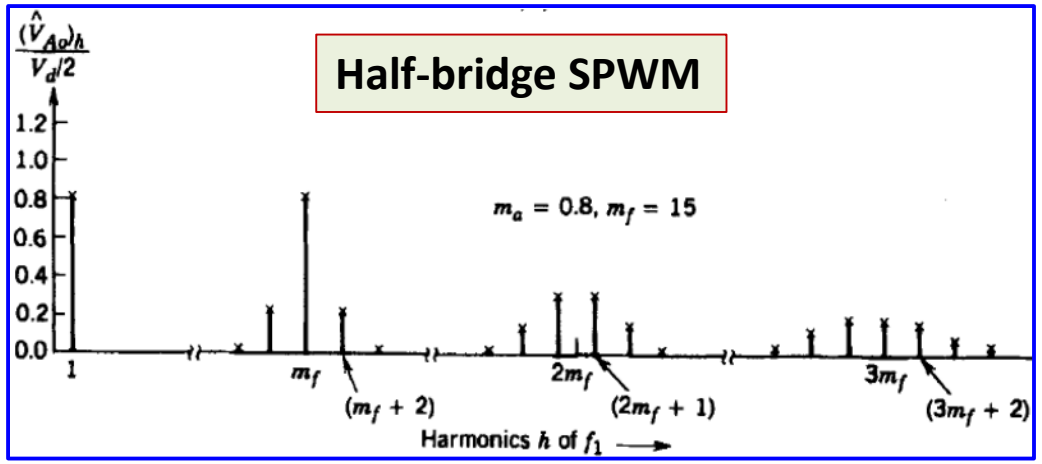
vAN and *vBN* are displaced by 180°.

Therefore, the harmonic components at the switching frequency in vAN and *vBN* have the same phase ($\phi_{AN} - \phi_{BN} = 180^0 . m_f = 0^0$, since the waveforms are 180^0 displaced and m_f is assumed to be even). This results in the cancellation of the harmonic component at the switching frequency in the output voltage $V_o = V_{AN} - V_{BN}$.

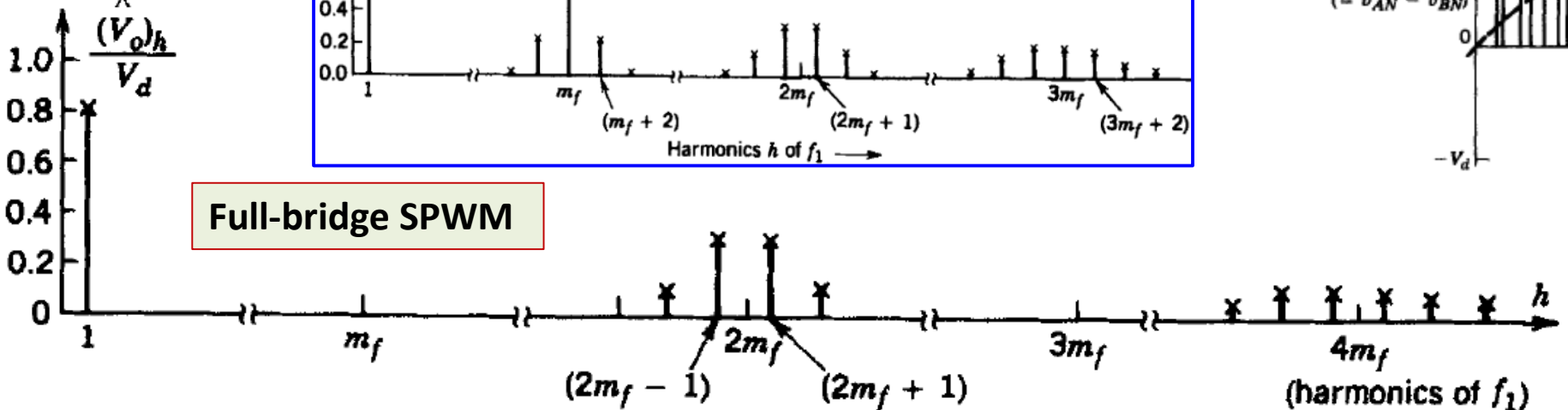
In addition, the sidebands of the switching-frequency harmonics disappear. In a similar manner, the other dominant harmonic at twice the switching frequency cancels out, while its sidebands do not.



Half-bridge SPWM



Full-bridge SPWM



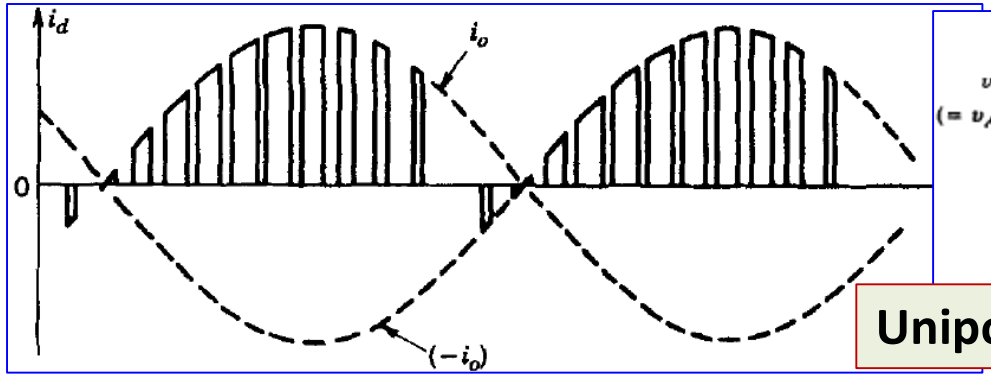
Here also,

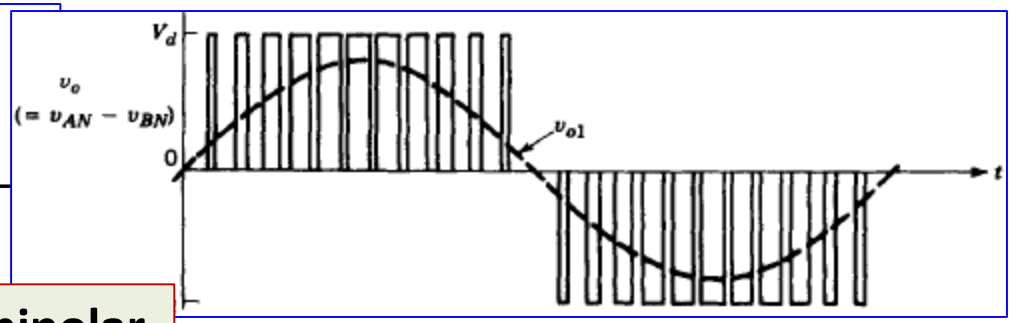
$$\hat{V}_{o1} = m_a V_d \ (m_a \leq 1.0)$$

$$V_d < \hat{V}_{o1} < \frac{4}{\pi} V_d \ (m_a > 1.0)$$

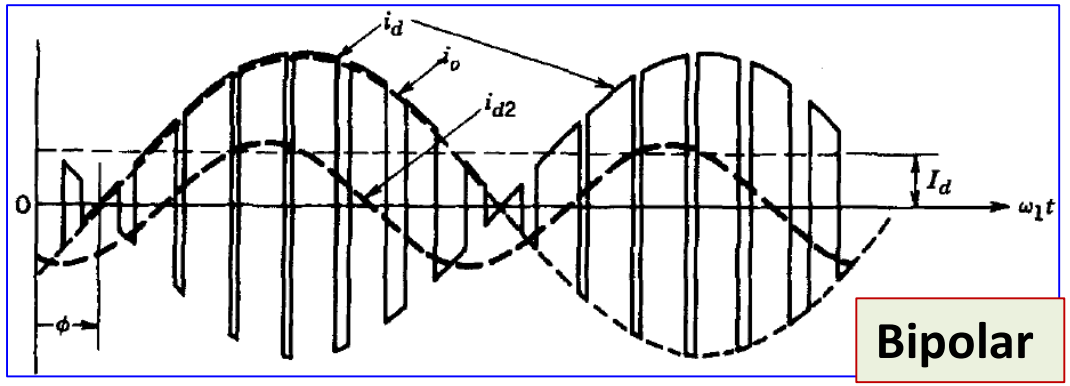
DC Side Current *id*

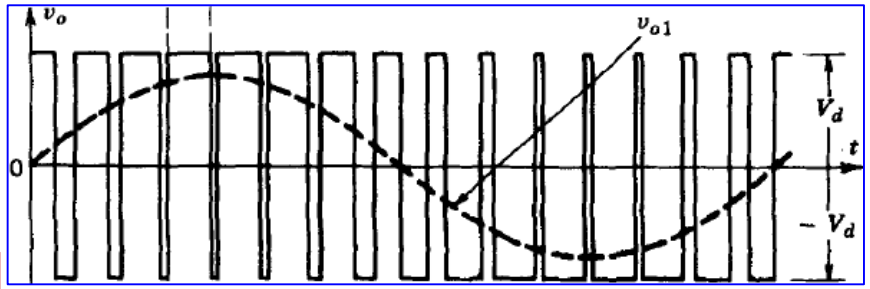
It is clear that using PWM with unipolar voltage switching results in a smaller ripple in the current on the dc side of the inverter.





Unipolar





Bipolar