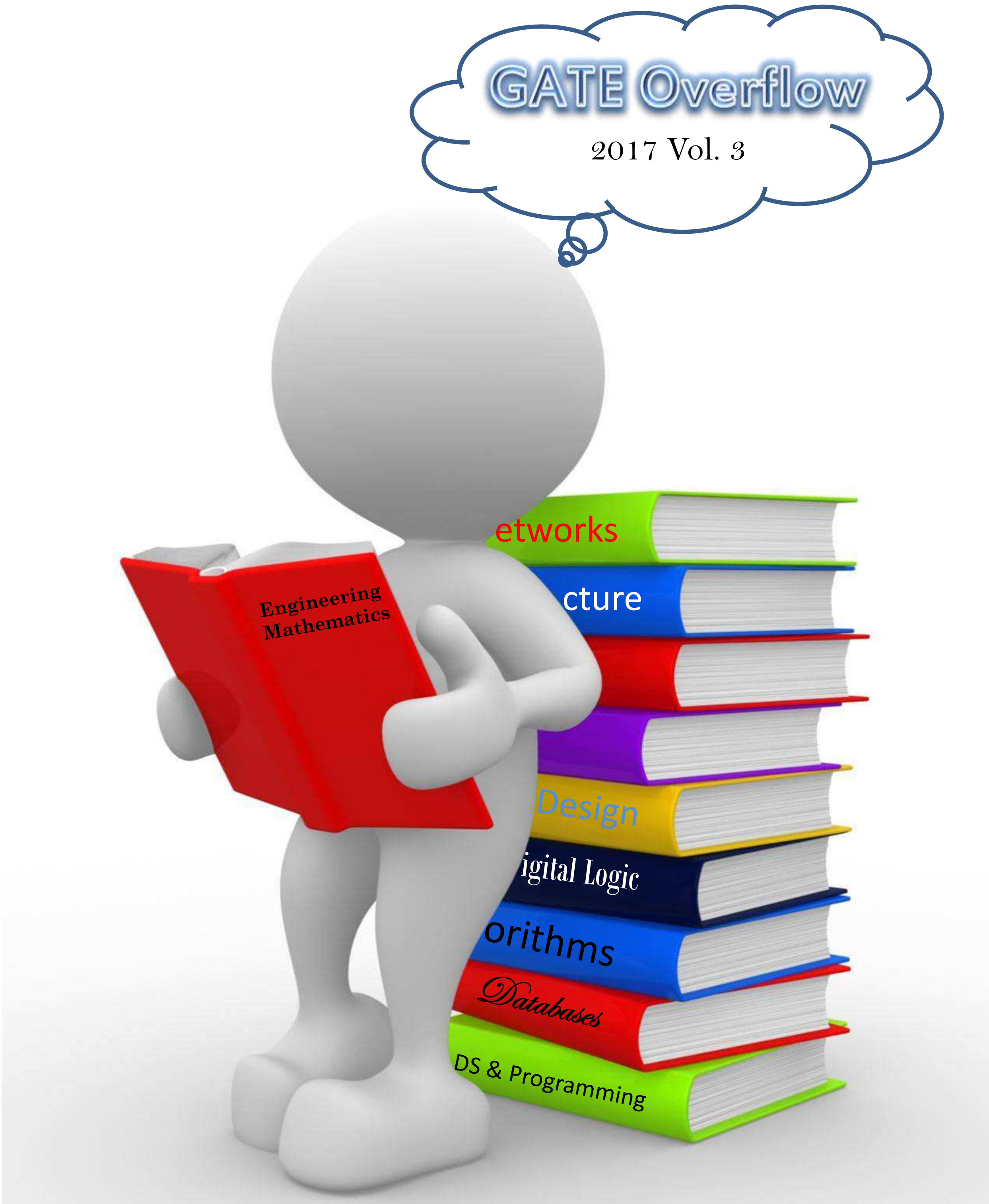

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This book was created programmatically by GATE Overflow on Sep 21, 2017. If you feel any doubt regarding the answer, click on the question link and give a comment on the site. Studying all these questions might get you 60 marks in GATE but that might not be enough for an IIT. So, read standard books, solve exercise questions and use these questions for cementing the concepts and aim 85+. At least if you are not getting the solution to a given problem first refer standard book. If any error is found on any question it shall be updated at **http://gateoverflow.in/corrections**.
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This book consists of only previous year GATE, TIFR, ISI and CMI questions (CS from 1987 and all 5 years of IT) all of which are relevant for GATE. Out of syllabus subjects as of GATE 2017 are removed from this book except in rare cases.

Since **GATE Overflow** started in August 2014, a lot of people have dedicated their time and effort in bringing this book now. Initiated by **Omesh Pandita** and **Arjun Suresh** as a Q/A platform for CSE students, **Kathleen Bankson** was instrumental in getting all previous year GATE questions here. Then experts like **Praven Saini**, **Happy Mittal**, **Sankaranarayanan P.N.**, **Suraj Kumar** etc. have contributed a lot to the answers here. **Pragy Agarwal** even after topping GATE has continuously contributed here with his knowledge as well as in making the contents beautiful with fine latex skills. We also have to thank the work by **Jothee**, **Misbah**, **Ishrat** and **Nataliyah** who are continuously adding and keeping the contents here neat and clean. There are also many toppers of GATE 2015, 2016, 2017 and probably 2018 who are contributing a lot here. The list of all the contributors can be found **here** but even that does not include the contributions of some like Arif Ali Anapparakkal in helping design this book, **Arvind Devaraj** and others who have provided guidance and help etc. Last but not the least, we thank all the users of GATE Overflow.

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1 CO & Architecture (175) top

1.1 Addressing Modes(17) top

1.1.1 Addressing Modes: GATE1987-1-V top http://gateoverflow.in/80194

The most relevant addressing mode to write position-independent codes is:

A. Direct mode
B. Indirect mode
C. Relative mode
D. Indexed mode

gate1987 co&architecture addressing-modes

Answer

1.1.2 Addressing Modes: GATE1989-2-ii top http://gateoverflow.in/87078

Match the pairs in the following questions:

(A) Base addressing	(p) Reentranecy
(B) Indexed addressing	(q) Accumulator
(C) Stack addressing	(r) Array
(D) Implied addressing	(s) Position independent

gate1989 match-the-following co&architecture addressing-modes easy

Answer

1.1.3 Addressing Modes: GATE1993_10 top http://gateoverflow.in/2307

The instruction format of a CPU is:

OP CODE	MODE	RegR

_____one memory word___

Mode and RegR together specify the operand. RegR specifies a CPU register and Mode specifies an addressing mode. In particular, Mode = 2 specifies that 'the register RegR contains the address of the operand, after fetching the operand, the contents of R RegR are incremented by 1'.

An instruction at memory location 2000 specifies Mode = 2 and the RegR refers to program counter (PC).

a. What is the address of the operand?

b. Assuming that is a non-jump instruction, what are the contents of PC after the execution of this instruction?

gate1993 co&architecture addressing-modes normal

Answer

1.1.4 Addressing Modes: GATE1996-1.16, ISRO2016-42 top http://gateoverflow.in/2720

Relative mode of addressing is most relevant to writing

A. Co-routines

B. Position – independent code

C. Shareable code

D. Interrupt Handlers

gate1996 co&architecture addressing-modes easy isro2016

Answer

1.1.5 Addressing Modes: GATE1998_1.19 top http://gateoverflow.in/1656

Which of the following addressing modes permits relocation without any change whatsoever in the code?

A. Indirect addressing

B. Indexed addressing

C. Base register addressing

D. PC relative addressing

gate1998 co&architecture addressing-modes easy

Answer

1.1.6 Addressing Modes: GATE1999_2.23 top http://gateoverflow.in/1500

A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?

A. Pointers
B. Arrays
C. Records
D. Recursive procedures with local variable

gate1999 co&architecture addressing-modes normal

Answer

1.1.7 Addressing Modes: GATE2000-1.10 top http://gateoverflow.in/633

The most appropriate matching for the following pairs

```
    X: Indirect addressing          1: Loops
    Y: Immediate addressing         2: Pointers
    Z: Auto decrement addressing    3: Constants
```

is

A. X - 3 Y - 2 Z - 1
B. X - 1 Y - 3 Z - 2
C. X - 2 Y - 3 Z - 1
D. X - 3 Y - 1 Z - 2

gate2000 co&architecture normal addressing-modes

Answer

1.1.8 Addressing Modes: GATE2001-2.9 top http://gateoverflow.in/727

Which is the most appropriate match for the items in the first column with the items in the second column

X. Indirect Addressing	I. Array implementation
Y. Indexed addressing	II. Writing relocatable code
Z. Base Register	III. Passing array as

Addressing	parameter

A. (X, III) (Y, I) (Z, II)
B. (X, II) (Y, III) (Z, I)
C. (X, III) (Y, II) (Z, I)
D. (X, I) (Y, III) (Z, II)

gate2001 co&architecture addressing-modes normal

Answer

1.1.9 Addressing Modes: GATE2002-1.24 top http://gateoverflow.in/829

In the absolute addressing mode

A. the operand is inside the instruction
B. the address of the operand in inside the instruction
C. the register containing the address of the operand is specified inside the instruction
D. the location of the operand is implicit

gate2002 co&architecture addressing-modes easy

Answer

1.1.10 Addressing Modes: GATE2004-20 top http://gateoverflow.in/1017

Which of the following addressing modes are suitable for program relocation at run time?

I. Absolute addressing

II. Based addressing

III. Relative addressing

IV. Indirect addressing

A. I and IV
B. I and II
C. II and III
D. I, II and IV

gate2004 co&architecture addressing-modes easy

Answer

1.1.11 Addressing Modes: GATE2005-65 top http://gateoverflow.in/1388

Consider a three word machine instruction

ADD A[R0], @B

The first operand (destination) “A[R0]” uses indexed addressing mode with R0 as the index register. The second operand (source) “@B” uses indirect addressing mode. A and B are memory addresses residing at the second and third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is:

A. 3
B. 4
C. 5
D. 6

gate2005 co&architecture addressing-modes normal

Answer

1.1.12 Addressing Modes: GATE2005-66 top http://gateoverflow.in/1389

Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

(1) A[I] = B[J]	(a) Indirect addressing
(2) while (*A++);	(b) Indexed addressing
(3) int temp = *x	(c) Auto increment

A. (1, c), (2, b) (3, a)
B. (1, c), (2, c) (3, b)
C. (1, b), (2, c) (3, a)
D. (1, a), (2, b) (3, c)

gate2005 co&architecture addressing-modes easy

Answer

1.1.13 Addressing Modes: GATE2006-IT-39, ISRO2009-42 top http://gateoverflow.in/3578

Which of the following statements about relative addressing mode is FALSE?

A. It enables reduced instruction size
B. It allows indexing of array element with same instruction
C. It enables easy relocation of data
D. It enables faster address calculation than absolute addressing

gate2006-it co&architecture addressing-modes normal isro2009

Answer

1.1.14 Addressing Modes: GATE2006-IT-40 top http://gateoverflow.in/3581

The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

MOVI	$R_s, 1$	; Move immediate
LOAD	$R_d, 1000(R_s)$	; Load from memory
ADDI	$R_d, 1000$	; Add immediate
STOREI	$0(R_d), 20$	; Store immediate

Which of the statements below is TRUE after the program is executed ?

A. Memory location 1000 has value 20
B. Memory location 1020 has value 20
C. Memory location 1021 has value 20
D. Memory location 1001 has value 20

gate2006-it co&architecture addressing-modes normal

Answer

1.1.15 Addressing Modes: GATE2008-33, ISRO2009-80 top http://gateoverflow.in/444

Which of the following is/are true of the auto-increment addressing mode?

I. It is useful in creating self-relocating code

II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation

III. The amount of increment depends on the size of the data item accessed

A. I only
B. II only
C. III only
D. II and III only

gate2008 addressing-modes co&architecture normal isro2009

Answer

1.1.16 Addressing Modes: GATE2011_21 top http://gateoverflow.in/2123

Consider a hypothetical processor with an instruction of type $\text{LW } \text{R1}, 20(\text{R2})$, which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

(A) Immediate addressing

(B) Register addressing

(C) Register Indirect Scaled Addressing

(D) Base Indexed Addressing

gate2011 co&architecture addressing-modes easy

Answer

1.1.17 Addressing Modes: GATE2017-1-11 top http://gateoverflow.in/118291

Consider the C struct defined below:

```
struct data {
    int marks [100];
    char grade;
    int cnumber;
};
struct data student;
```

The base address of student is available in register R1. The field student.grade can be accessed efficiently using

(A) Post-increment addressing mode, (R1)+

(B) Pre-decrement addressing mode, -(R1)

(C) Register direct addressing mode, R1

(D) Index addressing mode, X(R1), where X is an offset represented in 2's complement 16-bit representation.

gate2017-1 co&architecture addressing-modes

Answer

Answers: Addressing Modes

1.1.1 Addressing Modes: GATE1987-1-V top http://gateoverflow.in/80194

C) Relative Mode since we can just change the content of base register if we wish to relocate.

4 votes -- srestha (58.4k points)

1.1.2 Addressing Modes: GATE1989-2-ii top http://gateoverflow.in/87078

Selected Answer

(A) Base addressing	Position independent (By changing value in Base register location of address can be changed)
(B) Indexed addressing	Array
(C) Stack addressing	Reentranecy (Whenever code happens to be used again, address need not be the same)
(D) Implied addressing	Accumulator (If an address is not specified, it is assumed/implied to be the Accumulator)

6 votes -- Prashant Singh (49.2k points)

1.1.3 Addressing Modes: GATE1993_10 top http://gateoverflow.in/2307

Selected Answer

a) Address of the operand = content of PC = 2001 as PC holds the address of the next instruction to be executed and instruction size is 1 word as given in the diagram.

b) After execution of the current instruction PC will be automatically incremented by 1 when the next instruction is fetched. Also one extra increment will be done by operand fetch. So, PC = 2003 supposing next instruction is fetched. If we assume next instruction fetch is not done (this should be the default here), it should be **2002.**

5 votes -- Arjun Suresh (294k points)

1.1.4 Addressing Modes: GATE1996-1.16, ISRO2016-42 top

http://gateoverflow.in/2720

Selected Answer

Answer: B

Relative mode addressing is most relevant to writing a position-independent code.

Ref: http://en.wikipedia.org/wiki/Addressing_mode#PC-relative

13 votes -- Rajarshi Sarkar (35k points)

1.1.5 Addressing Modes: GATE1998_1.19 top

http://gateoverflow.in/1656

Selected Answer

PC relative addressing is the best option. For Base register addressing, we have to change the address in the base register while in PC relative there is absolutely no change in code needed.

7 votes -- Arjun Suresh (294k points)

1.1.6 Addressing Modes: GATE1999_2.23 top

http://gateoverflow.in/1500

Selected Answer

Pointer access requires indirect addressing which can be simulated with indexed addressing or register indirect addressing but not with direct and immediate addressing. An array and record access needs a pointer access. So, options A, B and C cannot be implemented on such a processor.

Now, to handle recursive procedures we need to use stack. A local variable inside the stack will be accessed as *(SP+offset) which is nothing but a pointer access and requires indirect addressing. Usually this is done by moving the SP value to Base register and then using Base Relative addressing to avoid unnecessary memory accesses for indirect addressing- but not possible with just direct and immediate addressing.

So, options A, B, C and D are correct.

21 votes -- Arjun Suresh (294k points)

1.1.7 Addressing Modes: GATE2000-1.10 top

http://gateoverflow.in/633

Selected Answer

C is the most appropriate one

9 votes -- Bhagirathi Nayak (13.3k points)

1.1.8 Addressing Modes: GATE2001-2.9 top

http://gateoverflow.in/727

Selected Answer

(A) is the answer.

Array implementation can use Indexed addressing

While passing array as parameter we can make use of a pointer (as in C) and hence can use Indirect addressing

Base Register addressing can be used to write relocatable code by changing the content of Base Register.

18 votes -- Arjun Suresh (294k points)

1.1.9 Addressing Modes: GATE2002-1.24 top

http://gateoverflow.in/829

Selected Answer

(b) is the answer. Absolute addressing mode means address of operand is given in the instruction.

(a) operand is inside the instruction -> immediate addressing
(c) register containing the address in specified in operand-> register Indirect addressing
(d) the location of operand is implicit-> implicit addressing

25 votes -- gatecse (13.4k points)

1.1.10 Addressing Modes: GATE2004-20 top

http://gateoverflow.in/1017

Selected Answer

Answer: C

A displacement type addressing should be preferred. So, I is not the answer.

Indirect Addressing leads to extra memory reference which is not preferable at run time. So, IV is not the answer.

10 votes -- Rajarshi Sarkar (35k points)

1.1.11 Addressing Modes: GATE2005-65 top

http://gateoverflow.in/1388

Selected Answer

1 memory read - get first operand from memory address A+R0 (A is given as part of instruction)
1 memory read - get address of second operand (since second uses indirect addressing)

1 memory read - to get second operand from the address given by the previous memory read

1 memory write - to store to first operand (which is the destination)

So, totally 4 memory cycles once the instruction is fetched.

The second and third words of the instruction are loaded as part of the Instruction fetch and not during the execute stage:
Ref: http://www.cs.iit.edu/~cs561/cs350/fetch/fetch.html

42 votes -- Arjun Suresh (294k points)

1.1.12 Addressing Modes: GATE2005-66 top

http://gateoverflow.in/1389

Selected Answer

(c) is the answer.
A[i] = B[j]; Indexed addressing

while(*A++); Auto increment

temp = *x; Indirect addressing

10 votes -- Arjun Suresh (294k points)

1.1.13 Addressing Modes: GATE2006-IT-39, ISRO2009-42 top http://gateoverflow.in/3578

Selected Answer

(D) is false. Relative addressing cannot be faster than absolute addressing as absolute address must be calculated from relative address. With specialized hardware unit, this can perform equally as good as absolute addressing but not faster.

(A) is true as instead of absolute address we can use a much smaller relative address in instructions which results in smaller instruction size.

(B) By using the base address of array we can index array elements using relative addressing.

(C) is true as we only need to change the base address in case of relocation- instructions remain the same.

23 votes -- Arjun Suresh (294k points)

1.1.14 Addressing Modes: GATE2006-IT-40 top http://gateoverflow.in/3581

Selected Answer

D) Memory location 1001 has value 20.
$R_s \leftarrow 1$ (Immediate Addressing)
$R_d \leftarrow 1$ (Indexed Addressing, value at memory location 1+1000 = 1001 is loaded to R_d which is 1)
$R_d \leftarrow 1001$ (R_d becomes 1+1000)
store in address $1001 \leftarrow 20$

18 votes -- Abhinav Rana (707 points)

1.1.15 Addressing Modes: GATE2008-33, ISRO2009-80 top http://gateoverflow.in/444

Selected Answer

In auto increment addressing mode, the base address is incremented after operand fetch. This is useful in fetching elements from an array. But this has no effect in self-relocating code (where code can be loaded to any address) as this works on the basis of an initial base address.

An additional ALU is desirable for better execution especially with pipelining, but never a necessity.

Amount of increment depends on the size of the data item accessed as there is no need to fetch a part of a data.

So, answer must be C only.

24 votes -- Arjun Suresh (294k points)

1.1.16 Addressing Modes: GATE2011_21 top http://gateoverflow.in/2123

Selected Answer

Answer: D

Base Index Addressing, as the content of register R2 will serve as the index and 20 will be the Base address.

14 votes -- Rajarshi Sarkar (35k points)

1.1.17 Addressing Modes: GATE2017-1-11 top http://gateoverflow.in/118291

Selected Answer

Option (D)

Displacement Mode :-

Similar to index mode, except instead of a index register a base register will be used. Base register contains a pointer to a memory location. An integer (constant) is also referred to as a displacement. The address of the operand is obtained by adding the contents of the base register plus the constant. The difference between index mode and displacement mode is in the number of bits used to represent the constant. When the constant is represented a number of bits to access the memory, then we have index mode. Index mode is more appropriate for array accessing; displacement mode is more appropriate for structure (records) accessing.

reference

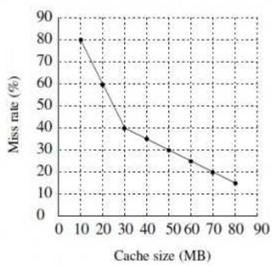
http://www.cs.iit.edu/~cs561/cs350/addressing/addsclm.html

5 votes -- Niraj Raghuvanshi (209 points)

1.2 Cache Memory(53) top

1.2.1 Cache Memory: GATE 2016-2-50 top http://gateoverflow.in/39592

A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



The smallest cache size required to ensure an average read latency of less than 6 ms is __________ MB.

gate2016-2 co&architecture cache-memory normal numerical-answers

Answer

1.2.2 Cache Memory: GATE1990-7a top http://gateoverflow.in/85403

A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of $16,384$ blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET and WORD fields?

gate1990 descriptive co&architecture cache-memory

Answer

1.2.3 Cache Memory: GATE1992-5,a top http://gateoverflow.in/584

The access times of the main memory and the Cache memory, in a computer system, are 500 n sec and 50 n sec, respectively. It is estimated that 80% of the main memory request are for read the rest for write. The hit ratio for the read access only is 0.9 and a write-through policy (where both main and cache memories are updated simultaneously) is used. Determine the average time of the main memory.

gate1992 co&architecture cache-memory normal

Answer

1.2.4 Cache Memory: GATE1993_11 top http://gateoverflow.in/2308

In the three-level memory hierarchy shown in the following table, p_i denotes the probability that an access request will refer to M_i.

Hierarchy Level (M_i)	Access Time (t_i)	Probability of access (p_i)	Page Transfer Time (T_i)
M_1	10^{-6}	0.99000	0.001 sec
M_2	10^{-5}	0.00998	0.1 sec
M_3	10^{-4}	0.00002	--

If a miss occurs at level M_i, a page transfer occurs from M_{i+1} to M_i and the average time required for such a page swap is T_i. Calculate the average time t_A required for a processor to read one word from this memory system.

gate1993 co&architecture cache-memory normal

Answer

1.2.5 Cache Memory: GATE1995_1.6 top http://gateoverflow.in/2593

The principle of locality justifies the use of

(a) Interrupts
(b) DMA
(c) Polling
(d) Cache Memory

gate1995 co&architecture cache-memory easy

Answer

1.2.6 Cache Memory: GATE1995_2.25 top http://gateoverflow.in/2638

A computer system has a 4 K word cache organized in block-set-associative manner with 4 blocks per set, 64 words per block. The number of bits in the SET and WORD fields of the main memory address format is:

(A) 15, 40
(B) 6, 4
(C) 7, 2
(D) 4, 6

gate1995 co&architecture cache-memory normal

Answer

1.2.7 Cache Memory: GATE1996_26 top http://gateoverflow.in/2778

A computer system has a three level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory) Access time = 50 nsec/byte	
Size	Hit Ratio
8 M byte	0.80
16 M byte	0.90
64 M byte	0.95

Level 2 (main memory) Access time = 200 nsec/byte	
Size	Hit ratio
4M byte	0.98
16 M byte	0.99
64 M byte	0.995

Level 3	
Size	Hit ratio
260 Mbyte	1.0

A. What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than 100 nsec

B. What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

26. A computer system has a three level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory) Access time = 50 nsec/byte		Level 2 (main memory) Access time = 200 nsec/byte		Level 3 Access time = 5 μsec/byte	
Size	Hit ratio	Size	Hit ratio	Size	Hit ratio
8 M byte	0.80	4M byte	0.98	260 Mbyte	1.0
16 M byte	0.90	16 M byte	0.99		
64 M byte	0.95	64 M byte	0.995		

(a) What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than 100 nsec?

(b) What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

gate1996 co&architecture cache-memory normal

Answer

1.2.8 Cache Memory: GATE1998_18 top

http://gateoverflow.in/1732

For a set-associative Cache organization, the parameters are as follows:

t_c	Cache access time
t_m	Main memory access time
l	number of sets
b	block size
$k \times b$	set size

Calculate the hit ratio for a loop executed 100 times where the size of the loop is $n \times b$, and $n = k \times m$ is a non-zero integer and $1 < m \leq l$.

Give the value of the hit ratio for $l = 1$.

gate1998 co&architecture cache-memory descriptive

Answer

1.2.9 Cache Memory: GATE1999_1.22 top

http://gateoverflow.in/1475

The main memory of a computer has 2 cm blocks while the cache has 2c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set

A. (k mod m) of the cache
B. (k mod c) of the cache

C. (k mod 2c) of the cache
D. (k mod 2 cm) of the cache

gate1999 co&architecture cache-memory normal

Answer

1.2.10 Cache Memory: GATE2001-1.7, ISRO2008-18 top

http://gateoverflow.in/700

More than one word are put in one cache block to

A. exploit the temporal locality of reference in a program
B. exploit the spatial locality of reference in a program
C. reduce the miss penalty
D. none of the above

gate2001 co&architecture easy cache-memory isro2008

Answer

1.2.11 Cache Memory: GATE2001-9 top

http://gateoverflow.in/750

A CPU has 32-bit memory address and a 256 KB cache memory. The cache is organized as a 4-way set associative cache with cache block size of 16 bytes.

a. What is the number of sets in the cache?
b. What is the size (in bits) of the tag field per cache block?
c. What is the number and size of comparators required for tag matching?
d. How many address bits are required to find the byte offset within a cache block?
e. What is the total amount of extra memory (in bytes) required for the tag bits?

gate2001 co&architecture cache-memory normal descriptive

Answer

1.2.12 Cache Memory: GATE2002-10 top

http://gateoverflow.in/863

In a C program, an array is declared as float A[2048]. Each array element is 4 Bytes in size, and the starting address of the array is 0x00000000. This program is run on a computer that has a direct mapped data cache of size 8 Kbytes, with block (line) size of 16 Bytes.

a. Which elements of the array conflict with element A[0] in the data cache? Justify your answer briefly.
b. If the program accesses the elements of this array one by one in reverse order i.e., starting with the last element and ending with the first element, how many data cache misses would occur? Justify your answer briefly. Assume that the data cache is initially empty and that no other data or instruction accesses are to be considered.

gate2002 co&architecture cache-memory normal descriptive

Answer

1.2.13 Cache Memory: GATE2004-65 top

http://gateoverflow.in/1059

Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is

8, 12, 0, 12, 8

A. 2
B. 3
C. 4
D. 5

gate2004 co&architecture cache-memory normal

Answer

1.2.14 Cache Memory: GATE2004-IT-12, ISRO2016-77 top

http://gateoverflow.in/3653

Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10 ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

A. 13.0
B. 12.8
C. 12.6
D. 12.4

gate2004-it co&architecture cache-memory normal isro2016

Answer

1.2.15 Cache Memory: GATE2004-IT-48 top http://gateoverflow.in/3691

Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7
If LRU replacement policy is used, which cache block will have memory block 7?

A. 4
B. 5
C. 6
D. 7

gate2004-it co&architecture cache-memory normal

Answer

1.2.16 Cache Memory: GATE2005-67 top http://gateoverflow.in/1390

Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively,

A. 10, 17
B. 10, 22
C. 15, 17
D. 5, 17

gate2005 co&architecture cache-memory easy

Answer

1.2.17 Cache Memory: GATE2005-IT-61 top http://gateoverflow.in/3822

Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks (0-7) and a main memory with 128 blocks (0-127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current job?
0 5 3 9 7 0 16 55

A. 0 3 5 7 16 55
B. 0 3 5 7 9 16 55
C. 0 5 7 9 16 55
D. 3 5 7 9 16 55

gate2005-it co&architecture cache-memory normal

Answer

1.2.18 Cache Memory: GATE2006-74 top http://gateoverflow.in/1851

Consider two cache organizations. First one is 32 kb 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases . A 2-to-1 multiplexer has latency of
$0.6ns$ while a
$k-$bit comparator has latency of

$\frac{k}{10} ns$. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2.

The value of h_1 is:

A. 2.4 ns
B. 2.3 ns
C. 1.8 ns
D. 1.7 ns

gate2006 co&architecture cache-memory normal

Answer

1.2.19 Cache Memory: GATE2006-75 top

http://gateoverflow.in/43565

Consider two cache organizations. First one is 32 kb 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases . A 2-to-1 multiplexer has latency of $0.6 ns$ while a $k-$bit comparator has latency of $\frac{k}{10} ns$. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2. The value of h_2 is:

A. 2.4 ns
B. 2.3 ns
C. 1.8 ns
D. 1.7 ns

gate2006 co&architecture cache-memory normal

Answer

1.2.20 Cache Memory: GATE2006-80 top

http://gateoverflow.in/1854

A CPU has a 32 KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2.

P1:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[i] [j];
    }
}
```

P2:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[j] [i];
    }
}
```

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and *i, j, x* are in registers. Let the number of cache misses experienced by P1 be M_1 and that for P2 be M_2.

The value of M_1 is:

A. 0
B. 2048
C. 16384
D. 262144

gate2006 co&architecture cache-memory normal

Answer

1.2.21 Cache Memory: GATE2006-81 top

http://gateoverflow.in/43517

A CPU has a 32 KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2.

P1:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[i] [j];
    }
}
```

P2:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[j] [i];
    }
}
```

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P1 be M1 and that for P2 be M2.

The value of the ratio $\frac{M_1}{M_2}$

A. 0
B. $\frac{1}{16}$
C. $\frac{1}{8}$
D. 16

co&architecture cache-memory normal gate2006

Answer

1.2.22 Cache Memory: GATE2006-IT-42 top

http://gateoverflow.in/3585

A cache line is 64 bytes. The main memory has latency 32ns and bandwidth 1G.Bytes/s. The time required to fetch the entire cache line from the main memory is

A. 32 ns
B. 64 ns
C. 96 ns
D. 128 ns

gate2006-it co&architecture cache-memory normal

Answer

1.2.23 Cache Memory: GATE2006-IT-43 top

http://gateoverflow.in/3586

A computer system has a level-1 instruction cache (1-cache), a level-1 data cache (D-cache) and a level-2 cache (L2-cache) with the following specifications:

	Capacity	Mapping Method	Block size
I-cache	4K words	Direct mapping	4 Words
D-cache	4K words	2-way set associative mapping	4 Words
L2-cache	64K words	4-way set associative mapping	16 Words

The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the I-cache, D-cache and L2-cache is, respectively,

A. 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit
B. 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit

C. 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
D. 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

gate2006-it co&architecture cache-memory normal

Answer

1.2.24 Cache Memory: GATE2007-10 top

http://gateoverflow.in/1208

Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

A. 9, 6, 5
B. 7, 7, 6
C. 7, 5, 8
D. 9, 5, 6

gate2007 co&architecture cache-memory normal

Answer

1.2.25 Cache Memory: GATE2007-80 top

http://gateoverflow.in/1273

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 x 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data misses will occur in total?

A. 48
B. 50
C. 56
D. 59

gate2007 co&architecture cache-memory normal

Answer

1.2.26 Cache Memory: GATE2007-81 top

http://gateoverflow.in/43511

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 x 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

A. line 4 to line 11
B. line 4 to line 12
C. line 0 to line 7
D. line 0 to line 8

gate2007 co&architecture cache-memory normal

Answer

1.2.27 Cache Memory: GATE2007-IT-37 top

http://gateoverflow.in/3470

Consider a Direct Mapped Cache with 8 cache blocks (numbered 0-7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9,16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82,17, 24.

Which of the following memory blocks will not be in the cache at the end of the sequence ?

A. 3
B. 18
C. 20

D. 30

gate2007-it co&architecture cache-memory normal

Answer

1.2.28 Cache Memory: GATE2008-35 top

http://gateoverflow.in/446

For inclusion to hold between two cache levels L1 and L2 in a multi-level cache hierarchy, which of the following are necessary?

I. L1 must be write-through cache

II. L2 must be a write-through cache

III. The associativity of L2 must be greater than that of L1

IV. The L2 cache must be at least as large as the L1 cache

A. IV only
B. I and IV only
C. I, II and IV only
D. I, II, III and IV

gate2008 co&architecture cache-memory normal

Answer

1.2.29 Cache Memory: GATE2008-71 top

http://gateoverflow.in/494

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The total size of the tags in the cache directory is

A. 32 Kbits
B. 34 Kbits
C. 64 Kbits
D. 68 Kbits

gate2008 co&architecture cache-memory normal

Answer

1.2.30 Cache Memory: GATE2008-72 top

http://gateoverflow.in/43490

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

Which of the following array elements have the same cache index as ARR[0][0]?

A. ARR[0][4]
B. ARR[4][0]
C. ARR[0][5]
D. ARR[5][0]

gate2008 co&architecture cache-memory normal

Answer

1.2.31 Cache Memory: GATE2008-73 top

http://gateoverflow.in/43491

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The cache hit ratio for this initialization loop is

A. 0%
B. 25%
C. 50%
D. 75%

gate2008 co&architecture cache-memory normal

Answer

1.2.32 Cache Memory: GATE2008-IT-80 top

http://gateoverflow.in/3403

Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are:

A. 7, 6, 7
B. 8, 5, 7
C. 8, 6, 6
D. 9, 4, 7

gate2008-it co&architecture cache-memory normal

Answer

1.2.33 Cache Memory: GATE2008-IT-81 top

http://gateoverflow.in/3405

Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

While accessing the memory location 0C795H by the CPU, the contents of the TAG field of the corresponding cache line is

A. 000011000
B. 110001111
C. 00011000
D. 110010101

gate2008-it co&architecture cache-memory normal

Answer

1.2.34 Cache Memory: GATE2009-29 top http://gateoverflow.in/1315

Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks are in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

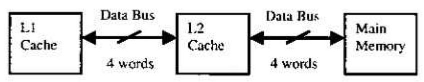
A. 3
B. 8
C. 129
D. 216

gate2009 co&architecture cache-memory normal

Answer

1.2.35 Cache Memory: GATE2010-48 top http://gateoverflow.in/2352

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and the main memory unit respectively.



When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?

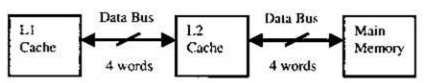
A. 2 nanoseconds
B. 20 nanoseconds
C. 22 nanoseconds
D. 88 nanoseconds

gate2010 co&architecture cache-memory normal barc2017

Answer

1.2.36 Cache Memory: GATE2010-49 top http://gateoverflow.in/43329

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and the main memory unit respectively.



When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?

A. 222 nanoseconds
B. 888 nanoseconds
C. 902 nanoseconds
D. 968 nanoseconds

gate2010 co&architecture cache-memory normal

Answer

1.2.37 Cache Memory: GATE2011_43 top http://gateoverflow.in/2145

An 8KB direct-mapped write-back cache is organized as multiple blocks, each size of 32-bytes. The processor generates 32-

bit addresses. The cache controller contains the tag information for each cache block comprising of the following.

- 1 valid bit
- 1 modified bit
- As many bits as the minimum needed to identify the memory block mapped in the cache.

What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

(A) 4864 bits

(B) 6144 bits

(C) 6656 bits

(D) 5376 bits

gate2011 co&architecture cache-memory normal

Answer

1.2.38 Cache Memory: GATE2012-54 top

http://gateoverflow.in/2192

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

A. 11
B. 14
C. 16
D. 27

gate2012 co&architecture cache-memory normal

Answer

1.2.39 Cache Memory: GATE2012-55 top

http://gateoverflow.in/43311

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is

A. 160 Kbits
B. 136 Kbits
C. 40 Kbits
D. 32 Kbits

normal gate2012 co&architecture cache-memory

Answer

1.2.40 Cache Memory: GATE2013_20 top

http://gateoverflow.in/1442

In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set $(s+1)$. The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from

(A) $(j \text{ mod } v) * k \text{ to } (j \text{ mod } v) * k + (k-1)$

(B) $(j \bmod v)$ to $(j \bmod v)+(k-1)$

(C) $(j \bmod k)$ to $(j \bmod k)+(v-1)$

(D) $(j \bmod k) * v$ to $(j \bmod k) * v+(v-1)$

gate2013 co&architecture cache-memory normal

Answer

1.2.41 Cache Memory: GATE2014-1-44 top http://gateoverflow.in/1922

An access sequence of cache block addresses is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k. What is the miss ratio if the access sequence is passed through a cache of associativity $A \geq k$ exercising least-recently-used replacement policy?

A. n/N
B. $1/N$
C. $1/A$
D. k/n

gate2014-1 co&architecture cache-memory normal

Answer

1.2.42 Cache Memory: GATE2014-2-43 top http://gateoverflow.in/2009

In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

A. A smaller block size implies better spatial locality
B. A smaller block size implies a smaller cache tag and hence lower cache tag overhead
C. A smaller block size implies a larger cache tag and hence lower cache hit time
D. A smaller block size incurs a lower cache miss penalty

gate2014-2 co&architecture cache-memory normal

Answer

1.2.43 Cache Memory: GATE2014-2-44 top http://gateoverflow.in/2010

If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

A. Width of tag comparator
B. Width of set index decoder
C. Width of way selection multiplexer
D. Width of processor to main memory data bus

gate2014-2 co&architecture cache-memory normal

Answer

1.2.44 Cache Memory: GATE2014-2-9 top http://gateoverflow.in/1963

A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____

gate2014-2 co&architecture cache-memory numerical-answers normal

Answer

1.2.45 Cache Memory: GATE2014-3-44 top http://gateoverflow.in/2078

The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _______.

gate2014-3 co&architecture cache-memory numerical-answers normal

Answer

1.2.46 Cache Memory: GATE2015-2_24 top http://gateoverflow.in/8119

Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is ______.

gate2015-2 co&architecture cache-memory easy numerical-answers

Answer

1.2.47 Cache Memory: GATE2015-3_14 top http://gateoverflow.in/8410

Consider a machine with a byte addressable main memory of 2^{20} bytes, block size of 16 bytes and a direct mapped cache having 2^{12} cache lines. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$. What are the tag and cache line addresses (in hex) for main memory address $(E201F)_{16}$?

A. E, 201
B. F, 201
C. E, E20
D. 2, 01F

gate2015-3 co&architecture cache-memory normal

Answer

1.2.48 Cache Memory: GATE2016-2-32 top http://gateoverflow.in/39622

The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _________ bits.

gate2016-2 co&architecture cache-memory normal numerical-answers

Answer

1.2.49 Cache Memory: GATE2017-1-25 top http://gateoverflow.in/118305

Consider a two-level cache hierarchy with $L1$ and $L2$ caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of $L1$ cache is 0.1; the $L2$ cache experiences, on average, 7 misses per 1000 instructions. The miss rate of $L2$ expressed correct to two decimal places is _________.

gate2017-1 co&architecture cache-memory

Answer

1.2.50 Cache Memory: GATE2017-1-54 top http://gateoverflow.in/118748

A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____________ bits.

gate2017-1 co&architecture cache-memory normal numerical-answers

Answer

1.2.51 Cache Memory: GATE2017-2-29 top http://gateoverflow.in/118371

In a two-level cache system, the access times of L_1 and L_2 caches are 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2. The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are

A. 0.111 and 0.056
B. 0.056 and 0.111
C. 0.0892 and 0.1784
D. 0.1784 and 0.0892

gate2017-2 cache-memory co&architecture normal

Answer

1.2.52 Cache Memory: GATE2017-2-45 top

http://gateoverflow.in/118597

The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	Read access time (in nanoseconds)	Hit ratio
I-cache	2	0.8
D-cache	2	0.9
L2-cache	8	0.9

The read access time of main memory in 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the writeback policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% od memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is __________

gate2017-2 co&architecture cache-memory numerical-answers

Answer

1.2.53 Cache Memory: GATE2017-2-53 top

http://gateoverflow.in/118613

Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is ________

gate2017-2 co&architecture cache-memory numerical-answers

Answer

Answers: Cache Memory

1.2.1 Cache Memory: GATE 2016-2-50 top

http://gateoverflow.in/39592

Selected Answer

Look aside Cache Latency = 1ms

Main Memory Latency = 10ms

- Lets try with 20 MB

  Miss rate = 60% , Hit rate = 40%

  Avg =0.4 (1) +0.6 (10)

  = 0.4 +6 = 6.4 ms > 6 ms

- Next Take 30 MB

  Miss rate = 40% , Hit rate = 60%

  Avg = 0.6 (1) + 0.4 (10)

  = 0.6 + 4 = 4.6 ms < 6ms

So answer is 30 MB

20 votes -- Akash (43.8k points)

1.2.2 Cache Memory: GATE1990-7a top

http://gateoverflow.in/85403

Selected Answer

For main memory, there are 2^14 blocks and each block size is 2^8 byte (byte can be considered as eight-bit words)

1.So size of main memory = 2^14*2^8=4MB(22 bits required for addressing the main memory).

2. For Word field , we require 8 bits,

As number of blocks is 2^7

As 4 block in 1 set, then 32 sets will be needed for 128 blocks so, For SET, we require 5bits.

As now tag bits= 22-(5+8)= 9 bits

9 bits (for tag)	5 bits(for set)	8bits (for word)

8 votes -- kirti singh (3.4k points)

1.2.3 Cache Memory: GATE1992-5,a top

http://gateoverflow.in/584

Selected Answer

Average memory access time = Time spend for read + Time spend for write

= Read time when cache hit + Read time when cache miss
+Write time when cache hit + Write time when cache miss

= 0.8 × 0.9 × 50 + 0.8 × 0.1 × (500+50) (assuming hierarchical read from memory and cache as only simultaneous write is mentioned in question)
+ 0.2 × 0.9 × 500 + 0.2 × 0.1 × 500 (simultaneous write mentioned in question)

= 36 + 44 + 90 + 10 = 180 ns

http://www.howardhuang.us/teaching/cs232/24-Cache-writes-and-examples.pdf

11 votes -- Arjun Suresh (294k points)

1.2.4 Cache Memory: GATE1993_11 top

http://gateoverflow.in/2308

Selected Answer

We are given the probabiliy of access being a hit in each level (clear since their sum adds to 1). So, we can get the average access time as:

$$t_A = 0.99 \times 10^{-6} + 0.00998 \times (10^{-6} + 10^{-5} + 0.001) + 0.00002 \times (10^{-6} + 10^{-5} + 10^{-4} + 0.1 + 0.001)] \approx (0.99 + 1$$

We can also use the following formula- for 100% of accesses M_1 is accessed, whenever M_1 is a miss, M_2 is accessed and when both misses only M_3 is accessed. So, average memory access time,

$$t_A = 10^{-6} + (1 - 0.99) \times (10^{-5} + 0.001) + 0.00002 \times (10^{-4} + 0.1) = 1 + 1.01 + 2 = 4.01 \mu s.$$

5 votes -- Arjun Suresh (294k points)

1.2.5 Cache Memory: GATE1995_1.6 top

http://gateoverflow.in/2593

Selected Answer

It is D.

Locality of reference is actually the frequent accessing of any storage location or some value. We can say in simple language that whatever things are used more frequently, they are stored in the locality of reference. So we have cache memory for the purpose.

10 votes -- Gate Keeda (19.1k points)

1.2.6 Cache Memory: GATE1995_2.25 top

http://gateoverflow.in/2638

Selected Answer

Number of sets = 4K /(64*4) = 16. So, we need 4 bits to identify a set => SET = 4 bits.

64 words per block means WORD is 6 bits.

So, (D)

8 votes -- Arjun Suresh (294k points)

1.2.7 Cache Memory: GATE1996_26 top

http://gateoverflow.in/2778

Selected Answer

The equation for access time can be written as follows (assuming a, b are the hit ratios of level1 and level2 respectively).

$T = T_1 + (1-a)T_2 + (1-a) \times (1-b)T_3$

Here $T \leq 100, T_1 = 50ns, T_2 = 200ns$ and $T_3 = 5000ns$. On substituting the a, b for the first case we get

T = 95ns for a = 0.8 and b = 0.995. i.e., L1 = 8M and L2 = 64M.
T = 75ns for a = 0.9 and b = 0.99. i.e., L1 = 16M and L2 = 4M

b.

1. $L_1 = 8M, a = 0.8, L_2 = 4M, b = 0.98$. So,
   $T = 50 + 0.2 \times 200 + 0.2 \times 0.02 \times 5000 = 50 + 40 + 20 = 110ns$
2. $L_1 = 16M, a = 0.9, L_2 = 16M, b = 0.99$. So,
   $T = 50 + 0.1 \times 200 + 0.1 \times 0.01 \times 5000 = 50 + 20 + 5 = 75ns$
3. $L_1 = 64M, a = 0.95, L_2 = 64M, b = 0.995$. So,
   $T = 50 + 0.05 \times 200 + 0.05 \times 0.005 \times 5000 = 50 + 10 + 1.25 = 61.25ns$

3 votes -- kireeti (1.1k points)

1.2.8 Cache Memory: GATE1998_18 top

http://gateoverflow.in/1732

Selected Answer

$\text{Size of the loop} = n \times b = k \times m \times b$

$\text{Size of a set} = k \times b \, (k - way$ associative)

Here, size of the loop is smaller than size of a set as $m \leq l$. Now, however be the mapping (whether all be mapped to the same set or not), we are guaranteed that the entire loop is in cache without any replacement.

For the first iteration:

$\text{No. of accesses} = n \times b$
$\text{No. of misses} = n$ as each new block access is a miss and loop body has n blocks each of size b for a total size of $n \times b$.

For, the remaining 99 iterations:

$\text{No. of accesses} = n \times b$
$\text{No. of misses} = 0$

So, $\text{total no. of accesses} = 100nb$

$\text{Total no. of hits} = \text{Total no. of accesses} - \text{Total no. of misses}$

$= 100nb - n$

So, $\text{hit ratio} = \frac{100nb-n}{100nb} = 1 - \frac{1}{100b}$

The hit ratio is independent if l, so for $l = 1$ also we have $\text{hit ratio} = 1 - \frac{1}{100b}$

8 votes -- Arjun Suresh (294k points)

1.2.9 Cache Memory: GATE1999_1.22 top

http://gateoverflow.in/1475

Selected Answer

Number of cache blocks = 2c

Number of sets in cache = 2c/2 = c since each set has 2 blocks. Now, a block of main memory gets mapped to a set (associativity of 2 just means there are space for 2 memory blocks in a cache set), and we have 2cm blocks being mapped to c sets. So, in each set 2m different main memory blocks can come and block k of main memory will be mapped to k mod c.

10 votes -- Arjun Suresh (294k points)

1.2.10 Cache Memory: GATE2001-1.7, ISRO2008-18 top

http://gateoverflow.in/700

Selected Answer

exploit the spatial locality of reference in a program as, if the next locality is addressed immediately, it will already be in the cache.

Consider the scenario similar to cooking, where when an ingredient is taken from cupboard, you also take the near by ingredients along with it- hoping that they will be needed in near future.

26 votes -- Arjun Suresh (294k points)

1.2.11 Cache Memory: GATE2001-9 top

http://gateoverflow.in/750

Selected Answer

What is the number of sets in the cache?

Number of sets = Cache memory/(set associativity * cache block size)

= 256KB/(4*16 B)

= 4096

What is the size (in bits) of the tag field per cache block?

Memory address size = 32-bit

Number of bits required to identify a particular set = 12 (Number of sets = 4096)

Number of bits required to identify a paticular location in cache line = 4 (cache block size = 16)

size of tag field = 32 -12 -4 = 16-bit

What is the number and size of comparators required for tag matching?

We use 4-way set associate cache. So, we need 4 comparators each of size 16 bits

http://ecee.colorado.edu/~ecen2120/Manual/caches/cache.html

How many address bits are required to find the byte offset within a cache block?

Cache block size is 16 byte. so 4 bits are required to find the byte offset within a cache block.

What is the total amount of extra memory (in bytes) required for the tag bits?

size of tag = 16 bits

Number of sets = 4096

Set associativity = 4

Extramemory required to store the tag bits = 16 * 4096 * 4 bits = 2^{18} bytes

15 votes -- suraj (5.1k points)

1.2.12 Cache Memory: GATE2002-10 top

http://gateoverflow.in/863

Selected Answer

(a)

Data cache size = 8KB.

Block line size = 16B.

Since each array element occupies 4B, four consecutive array elements occupy a block line (elements are aligned as starting address is 0)

Number of cache blocks = 8KB/16B = 512. Number of cache blocks needed for the array = 2048/4 = 512. So, all the array elements has its own cache block and there is no collision.

We can also explain this with respect to array address. Starting address is 0x00000000 = 0b0000..0 (32 0's). Ending address is 0x00001FFF = 0b0000..0111111111111 (4*2048 = 8192 location).

Here, the last 4 bits are used as OFFSET bits and the next 9 bits are used as SET bits. So, since the ending address is not extending beyond these 9 bits, all cache accesses are to diff sets.

(b) If the last element is accessed first, its cache block is fetched. (which should contain the previous 3 elements of the array also since each cache block hold 4 elements of array and 2048 is and exact multiple of 4). Thus, for every 4 accesses, we will have a cache miss => for 2048 accesses we will have 512 cache misses. (This would be same even if we access array in forward order).

15 votes -- Arjun Suresh (294k points)

1.2.13 Cache Memory: GATE2004-65 top

http://gateoverflow.in/1059

Selected Answer

We have 4 blocks and 2 blocks in a set

=> there are 2 sets. So blocks will go

to sets as follows:

Set Number	Block Number
0	0, 8, 12
1	

since the lowest bit of block address is used for indexing into the set.

So, 8, 12 and 0 first miss in cache with 0 replacing 8 (there are two slots in each set due to 2-way set) and then 12 hits in cache and 8 again misses. So totally 4 misses.

8 votes -- Arjun Suresh (294k points)

1.2.14 Cache Memory: GATE2004-IT-12, ISRO2016-77 top http://gateoverflow.in/3653

Selected Answer

By default we consider hierarchical access - because that is the common implementation and simultaneous access cache has great practical difficulty. But here the question is a bit ambiguous -- it says to ignore search time within the cache - usually search is applicable for an associative cache but here no such information given. So, may be they are telling to ignore the search time for L1 and just consider the time for L2 for an L1 miss and similarly just consider memory access time for L2 miss. This is nothing but simultaneous access.

Access time for hierarchical access $= t_1 + (1 - h_1) \times t_2 + (1 - h_1)(1 - h_2)t_m = 1 + 0.2 \times 10 + 0.2 \times 0.1 \times 500 = 13ns.$

Access time for simultaneous access $= h_1 \times t_1 + (1 - h_1)h_2 \times t_2 + (1 - h_1)(1 - h_2)t_m = 0.8 + 0.2 \times 0.9 \times 10 + 0.2 \times 0.1 \times 500 = 12.6ns.$

Both options in choice - :O

21 votes -- Arjun Suresh (294k points)

option C

t1 * h1 + (1- h1) h2 t2 + (1-h1) (1-h2) tm

tm- main memory access time

10 votes -- rajsh3kar (1.3k points)

1.2.15 Cache Memory: GATE2004-IT-48 top http://gateoverflow.in/3691

Selected Answer

When 45 comes, the cache contents are
4 3 25 8 19 6 16 35

LRU array (first element being least recently used)

[4 3 19 6 25 8 16 35]

So, 45 replaces 4

45 3 25 8 19 6 16 35 [3 19 6 25 8 16 35 45]

Similarly 22 replaces 3 to give

45 22 25 8 19 6 16 35 [19 6 25 8 16 35 45 22]

8 hits in cache

45 22 25 8 19 6 16 35 [19 6 25 16 35 45 22 8]

3 replaces 19

45 22 25 8 3 6 16 35 [6 25 16 35 45 22 8 3]

16 and 25 hits in cache

45 22 25 8 3 6 16 35 [6 35 45 22 8 16 25 3]

Finally 7 replaces 6, which is in block 5.

So, answer is (B)

10 votes -- Arjun Suresh (294k points)

1.2.16 Cache Memory: GATE2005-67 top

http://gateoverflow.in/1390

Selected Answer

Number of blocks = cache size/block size = 32KB/32 = 1024 bytes. So, indexing requires 10 bits. Number of OFFSET bits required to access 32 bit block = 5. So, number of TAG bits = 32 - 10 - 5 = 17. So, answer is (A).

11 votes -- Arjun Suresh (294k points)

1.2.17 Cache Memory: GATE2005-IT-61 top

http://gateoverflow.in/3822

Selected Answer

128 main memory blocks are mapped to 4 sets in cache. So, each set maps 32 blocks each. And in each set there is place for two blocks (2-way set).

Now, we have 4 sets meaning 2 index bits. Also, 32 blocks going to one set means 5 tag bits.

Now, these 7 bits identify a memory block and tag bits are placed before index bits. (otherwise adjacent memory references- spatial locality- will hamper cache performance)

So, based on the two index bits (lower 2 bits) blocks will be going to sets as follows:

Set Number	Block Numbers
0	0,16
1	5, 9
2	
3	~~3,~~ 7, 55

Since, each set has only 2 places, 3 will be throw out as its the least recently used block. So, final content of cache will be

0 5 7 9 16 55

(C) choice.

22 votes -- Arjun Suresh (294k points)

1.2.18 Cache Memory: GATE2006-74 top

http://gateoverflow.in/1851

Selected Answer

Cache size is 32 KB and cache block size is 32 B. So,

$$\text{number of sets} = \frac{\text{cache size}}{\text{no. of blocks in a set} \times \text{block size}}$$

$$= \frac{32KB}{2 \times 32B} = 512$$

So, number of index bits needed = 9 (since 2^9 = 512). Number of offset bits = 5 (since 2^5 = 32 B is the block size and assuming byte addressing). So, number of tag bits = 32 - 9 - 5 = 18 (as memory address is of 32 bits).

So, time for comparing the data = Time to compare the data + Time to select the block in set = 0.6 + 18/10 ns = 2.4 ns. (Two comparisons of tag bits need to be done for each block in a set, but they can be carried out in parallel and the succeeding one multiplexed as the output).

Ref: https://courses.cs.washington.edu/courses/cse378/09au/lectures/cse378au09-19.pdf

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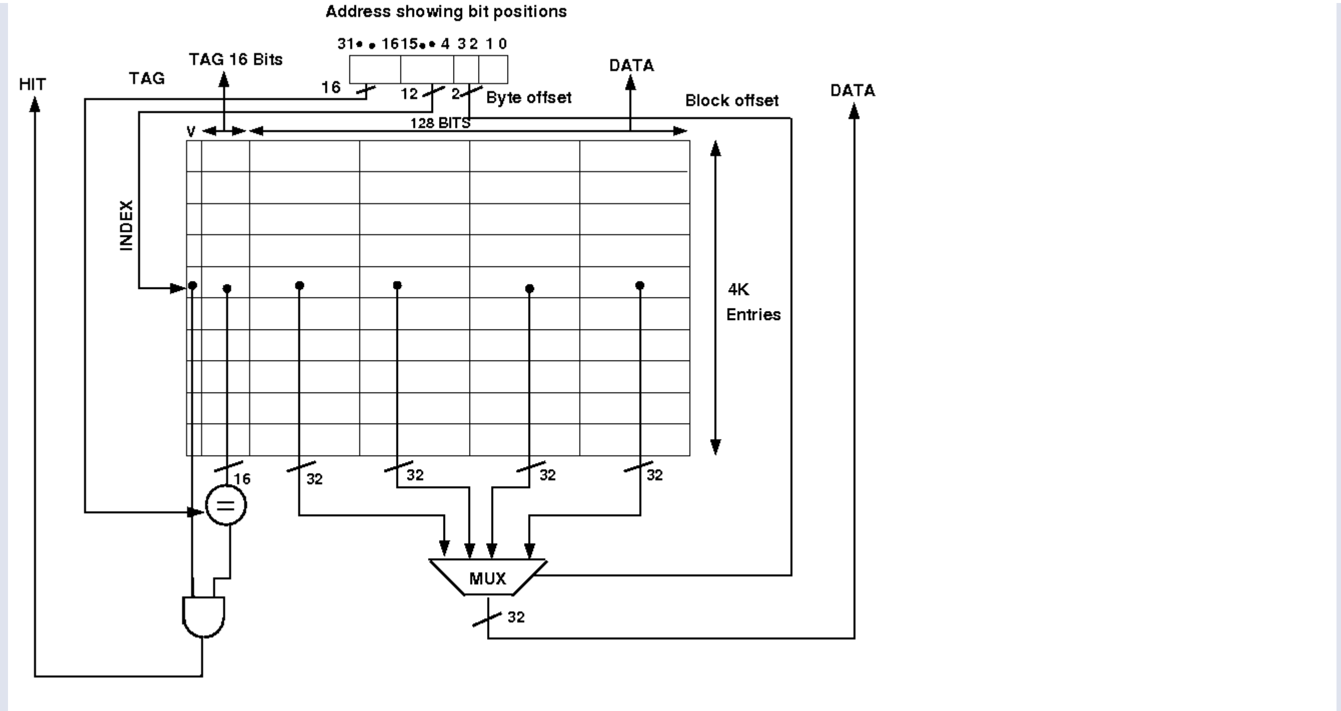


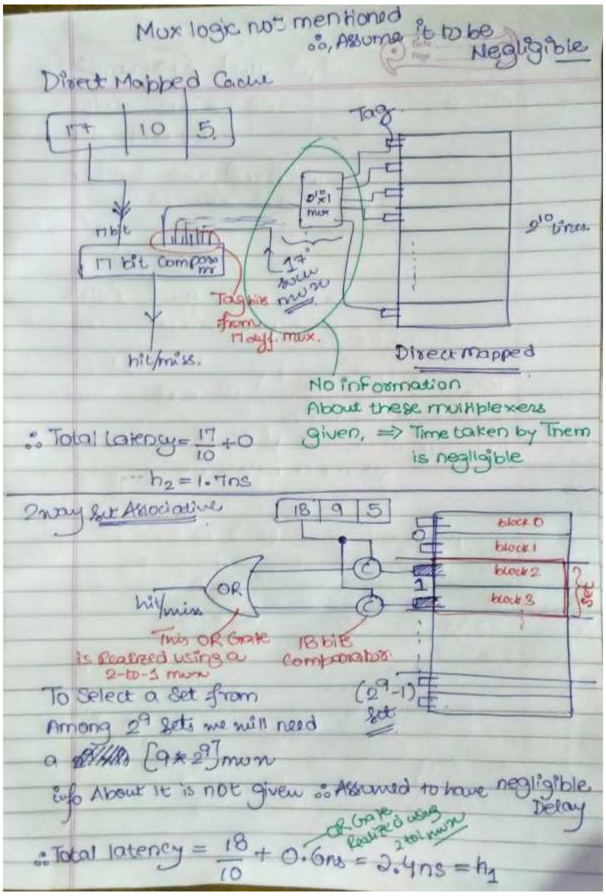
👍 22 votes -- Arjun Suresh (294k points)

2-Way Set Associative

tag	set	block offset
18	9	5

Direct Mapped

tag	line	block offset
17	10	5



gives a better insight.

20 votes -- Amar Vashishth (28.7k points)

1.2.19 Cache Memory: GATE2006-75 top http://gateoverflow.in/43565

word offset=5bit

block offset=32kb/32=10bit

so tag bit=32-10-5=17bit

hit latency=mux delay+comparator delay

1. mux is not required in direct mapped cache coz we have only one comprator(IF IT IS 2 WAY SET ASSOCITATIVE THEN COMPRATOR WILL BE 2 AND WE NEED A MUX OF 2-TO-1 TO DECIDE HIT/MISS) so mux delay=0..

2 comp. delay=k/10=17/10=1.7.

so h2 =1.7

5 votes -- asutosh kumar Biswal (10.2k points)

1.2.20 Cache Memory: GATE2006-80 top http://gateoverflow.in/1854

Selected Answer

Code being C implies array layout is row-major.

http://en.wikipedia.org/wiki/Row-major_order

When A[0][0] is fetched, 128 consecutive bytes are moved to cache. So, for the next 128/8 -1= 15 memory references there won't be a cache miss. For the next iteration of i loop also the same thing happens as there is no temporal locality in the code. So, number of cache misses for P1

$= \frac{512}{16} \times 512$

$= 32 \times 512$

$= 2^{14} = 16384$

14 votes -- Arjun Suresh (294k points)

$$\text{Number of Cache Lines} = \frac{2^{15}B}{128B} = 256$$

$$\text{In 1 Cache Line} = \frac{128B}{8B} = 16 \; elements$$

$$P_1 = \frac{\text{total elements in array}}{\text{elements in a cache line}} = \frac{512 \times 512}{16} = 2^{14} = 16384$$

It is so because for
P_1 for every line there is a miss, and once a miss is processed we get 16 elements in memory. So another miss happens after 16 elements.

Hence, answer = option C

11 votes -- Amar Vashishth (28.7k points)

1.2.21 Cache Memory: GATE2006-81 top http://gateoverflow.in/43517

Selected Answer

$$\begin{aligned}
\text{Number of Cache Lines} &= \frac{2^{15}B}{128B} \\
&= 256 \\
\text{In 1 Cache Line} &= \frac{128B}{8B} = 16 \; elements \\
P_1 &= \frac{\text{total elements in array}}{\text{elements in a cache line}} \\
&= \frac{512 \times 512}{16} \\
&= 2^{14} \\
&= 16384 \\
P_2 &= 512 \times 512 \\
&= 2^{18} \\
\frac{P_1}{P_2} &= \frac{16384}{512 \times 512} \\
&= 2^{14-18} \\
&= 2^{-4} \\
&= \frac{1}{16}
\end{aligned}$$

It is so because for
P_1 for every line there is a miss, and once a miss is processed we get 16 elements in memory. So another miss happens after 16 elements.
for
P_2 for every element there is a miss coz storage is row major order(by default) and we are accessing column wise.

Hence,
answer = option B

10 votes -- Amar Vashishth (28.7k points)

Code being C implies array layout is row-major.

http://en.wikipedia.org/wiki/Row-major_order

When A[0][0] is fetched, 128 consecutive bytes are moved to cache. So, for the next 128/8 -1= 15 memory references there won't be a cache miss. For the next iteration of i loop also the same thing happens as there is no temporal locality in the code. So, number of cache misses for P1

$= \frac{512}{16} \times 512$

$= 32 \times 512$

$= 2^{14} = 16384$

In the case of P2, the memory references are not consecutive. After A[0][0], the next access is A[1][0] which is after 512 * 8 memory locations. Since our cache block can hold only 128 contiguous memory locations, A[1][0] won't be in cache after a[0][0] is accessed. Now, the next location after A[0][0] is A[0][1] which will be accessed only after 512 iterations of the inner loop- after 512 distinct memory block accesses. In our cache we have only space for 32 KB/128 B = 256 memory blocks. So, by the time A[0][1] is accessed, its cache block would be replaced. So, each of the memory access in P2 results in a cache miss. Total number of cache miss

$= 512 \times 512$

So, $\frac{M_1}{M_2} = \frac{32 \times 512}{512 \times 512} = \frac{1}{16}$

15 votes -- Arjun Suresh (294k points)

1.2.22 Cache Memory: GATE2006-IT-42 top http://gateoverflow.in/3585

Selected Answer

ans : c

for 1 sec it is 10^9 bytes

so for 64 bytes?

it is 64 * 1 /10^9 so it is 64 ns but mm latency is 32 so total time required to place cache line is

64+32 = 96 ns

15 votes -- rajsh3kar (1.3k points)

1.2.23 Cache Memory: GATE2006-IT-43 top http://gateoverflow.in/3586

Selected Answer

1. **I-cache**

- Number of blocks in cache = 4K/4 = 2^{10} blocks
- Bits to represent blocks = 10
- Number of words in a block = 4 = 2^2 words
- Bits to represent words = 2
- tag bits = 30 - (10+2) = 18
- Each block will have it's own tag bits. So total tag bits = 1K x 18 bits.

2. **D-cache**

- Number of blocks in cache = 4K/4 = 2^{10} blocks
- Number of sets in cache = 2^{10}/2 = 2^9 sets
- Bits to represent sets = 9
- Number of words in a block = 4 = 2^2 words
- Bits to represent words = 2
- tag bits = 30 - (+2) = 19
- Each block will have it's own tag bits. So total tag bits = 1K x 19 bits.

3. **L2 cache**

- Number of blocks in cache = 64K/16 = 2^{12} blocks
- Number of sets in cache = 2^{12}/4 = 2^{10} sets
- Bits to represent sets = 10
- Number of words in cache = 16 = 2^4 words
- Bits to represent words = 4
- tag bits = 30 - (10+4) = 16
- Each block will have it's own tag bits. So total tag bits = 2^{12} x 16 bits = 4K x 16 bits

Option A.

13 votes -- Viral Kapoor (2k points)

1.2.24 Cache Memory: GATE2007-10 top

http://gateoverflow.in/1208

Selected Answer

Number of sets = cache size/(size of a block * No. of blocks in a set)

= 128 * 64 / (64 * 4) (4 way set associative means 4 blocks in a set)

= 32.

So, number of index (LINE) bits = 5 and number of WORD bits = 6 size cache block (line) size is 64. So, number of TAG bits = 20 - 6 - 5 = 9.

Answer is (D) choice

10 votes -- Arjun Suresh (294k points)

1.2.25 Cache Memory: GATE2007-80 top

http://gateoverflow.in/1273

Selected Answer

bits used to represent the address = $\log_2 2^{16} = 16$

each cache line size = 64 bytes; means offset requires 6 bits

total number of lines in cache = 32; means line# requires 5 bits

so, tag bits $= 16 - 6 - 5 = 5$

we have a 2D array each of its element is of size = 1 Byte;
total size of this array = $50 \times 50 \times 1Byte = 2500Bytes$

so, total number of lines it will require to get contain in cache = $\frac{2500B}{64B} = 39.0625 \approx 40$

starting address of array = 1100H = $00010\ 00100\ 000000$
the group of bits in middle represents Cache Line number $\implies$ array starts from cache line number 4,
we require 40 cache lines to hold all array elements, but we have only 32 cache lines

Lets group/partition our 2500 array elements in those 40 array lines, we call this first array line as A_0 which will have 64 of its elements. this line(group of 64 elements) of array will be mapped to cache line number 4 as found by analysis of starting address of array above.

This all means that among those 40 array lines some array lines will be mapped to same cache line, coz there are just 32 cache lines but 40 of array lines.

this is how mapping is :

0	A_{28}	
1	A_{29}	
2	A_{30}	
3	A_{31}	
4	A_0	A_{32}
5	A_1	A_{33}
6	A_2	A_{34}
7	A_3	A_{35}
8	A_4	A_{36}
9	A_5	A_{37}
10	A_6	A_{38}
11	A_7	A_{39}
12	A_8	
$\vdots$		
30	A_{26}	
31	A_{27}	

so, if we access complete array twice we get $= 32 + 8 + 8 + 8 = 56$ miss
coz only 8 lines from cache line number 4 to 11 are miss operation, rest are Hits(not counted) or Compulsory misses(first 32).

Hence, Q.80 answer = **option C**

54 votes -- Amar Vashishth (28.7k points)

$2^{16} = 64$ KB main memory is mapped to 32 lines of 64 bytes. So, number of offset bits = 6 (to identify a byte in a line) and number of indexing bits = 5 (to identify the line).

Size of array = 50* 50 = 2500 B. If array is stored in row-major order (first row, second-row..), and if elements are also accessed in row-major order (or stored and accessed in column-major order), for the first 64 accesses, there will be only 1 cache miss, and for 2500 accesses, there will be 2500/64 = 40 cache misses during the first iteration.

We have 5 index bits and 6 offset bits. So, for 2^{11} (5 + 6 = 11) continuous memory addresses there wont be any cache conflicts as the least significant bits are offset bits followed by index bits.

So, number of array elements that can be accessed without cache conflict = 2048 (as element size is a byte). The next 452 elements conflict with the first 452 elements. This means 452/64 = 8 cache blocks are replaced. (We used ceil, as even if one element from a new block is accessed, the whole block must be fetched).

So, during second iteration we incur misses for the first 8 cache blocks as well as for the last 8 cache blocks. So, total data cache misses across 2 iterations = 40 + 8 + 8 = 56.

16 votes -- Arjun Suresh (294k points)

1.2.26 Cache Memory: GATE2007-81 top

http://gateoverflow.in/43511

Selected Answer

Cache Organization:

Staring Address=1100H = 16^3+16^2+0+0 =4352B is the starting address.

We need to find Starting block = 4352B/64B = 68^{th} block in main memory from where array start storing elements.

50*50B =array size = 50*50B/64B =39.0625 blocks needed =approx = 40 blocks

68,69,70....107 block we need = 40 blocks starting block is 68 mod 32 = 4^{th} cache block and after that in sequence they will be accessed.

as shown in below table line no 4 to 11 has been replaced by array in second time

Cache block No.	First Cycle	Second Cycle
0	96	
1	97	
2	98	
3	99	
4	68 //100	68
5	69 //101	69
6	70 //102	70
7	71 //103	71
8	72 //104	72
9	73 // 105	73
10	74 //106	74
11	75 // 107	75
12	76	
13	77	
14	78	
15	79	
16	80	
17	81	
18	82	
19	83	
20	84	
21	85	
22	86	
23	87	
24	88	
25	89	
26	90	
27	91	
28	92	
29	93	
30	94	
31	95	

13 votes -- papesh (24.1k points)

1.2.27 Cache Memory: GATE2007-IT-37 top

http://gateoverflow.in/3470

Selected Answer

ans is B

cache location (memory block) = block req mod number of cache blocks. Since each block has only one location (associativity is 1) the last mod 8 request will be in cache (no need of any replacement policy as mapping is direct).

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24

Block 0- 8, 0, 16, 24, 24. At end contains 24.

1- 9, 17, 25, 17.
2- 2, 18, 2, 82.
3- 3.
4- 20.
5- 5, 5.
6- 30.
7- 63 63.

So, memory block 18 is not in cache while 3, 20 and 30 are in cache.

10 votes -- rajsh3kar (1.3k points)

1.2.28 Cache Memory: GATE2008-35 top

http://gateoverflow.in/446

Selected Answer

1st is not correct as data need not to be exactly same at the same point of time and so write back policy can be used in this.

2nd is not needed when talking only about L1 and L2.

For 3rd, associativity can be equal.

So only 4th statement is Necessarily true - A choice.

11 votes -- Shaun Patel (6.9k points)

1.2.29 Cache Memory: GATE2008-71 top

http://gateoverflow.in/494

Selected Answer

Number of sets = cache size/ size of a set
= 64 KB / (16 B * 2) (two blocks per set)
= 2 K = 2^{11}
So, we need 11 bits for set indexing.

Number of WORD bits required = 4 as a cache block consists of 16 bytes and we need 4 bits to address each of them.

So, number of tag bits = 32 - 11 - 4 = 17

Total size of the tag = 17 * Number of cache blocks
= 17 * 2^{11} * 2 (since each set has 2 blocks)

= 68 Kbits

answer = option D) 68 Kbits

We use the top 17 bits for tag and the next 11 bits for indexing and next 4 for offset. So, for two addresses to have the same cache index, their 11 address bits after the 4 offset bits from right must be same.

ARR[0][0] is located at virtual address 0x FF000 000. (FF000 is page address and 000 is page offset). So, index bits are 00000000000

Address of ARR[0][4] = 0xFF000 + 4 * sizeof (double) = 0xFF000 000 + 4*8 = 0xFF000 020 (32 = 20 in hex) (index bits differ)

Address of ARR[4][0] = 0xFF000 + 4 * 1024 * sizeof (double) [since we use row major storage] = 0xFF000 000 + 4096*8 = 0xFF000 000 + 0x8000 = 0xFF008 000 (index bits matches that of ARR [0][0] as both read 000 0000 0000)

Address of ARR[0][5] = 0xFF000 + 5 * sizeof (double) = 0xFF000 000+ 5*8 = 0xFF000 028 (40 = 28 in hex) (index bits differ)

Address of ARR[5][0] = 0xFF000 + 5 * 1024 * sizeof (double) [since we use row major storage] = 0xFF000 000 + 5120*8 = 0xFF000 000 + 0xA000 = 0xFF00A 000 (index bits differ)

So, only ARR[4][0] and ARR[0][0] have the same cache index.

The inner loop is iterating from 0 to 1023, so consecutive memory locations are accessed in sequence. Since cache block size is only 16 bytes and our element being double is of size 8 bytes, during a memory access only the next element gets filled in the cache. i.e.; every alternative memory access is a cache miss giving a hit ratio of 50%. (If loops i and j are reversed, all accesses will be misses and hit ratio will become 0).

25 votes -- Arjun Suresh (294k points)

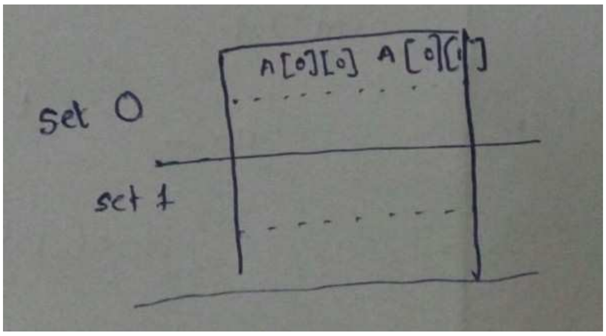
1.2.30 Cache Memory: GATE2008-72 top

http://gateoverflow.in/43490

Selected Answer

[Need @arjun sir to verify this solution]
Every element = 8B
Total Size Required By the Array = 1024 *1024 * 8 = 2 ^{23} B
Every Block = 16 B
Number of blocks for Array = $\frac{2^{23}}{2^4}$ = 2 ^{19}
Elements in one block = $\frac{16}{8}$ = 2
Number of blocks in cache = $\frac{2^{16}}{2^4}$ = 2 ^{12}
Number of Sets = $\frac{2^{12}}{2^1}$ = 2^{11}

$\Rightarrow$ 2 elements in one block



MM block 0 ε 0 mod 2^{11} = set 0
MM block 1 ε 1 mod 2^{11} = set 1
..
..
MM block 2048 ε 2048 mod 2^{11} = set 0 // **sharing same set**

Each Row of array has 1024 elements $\Rightarrow$ 512 blocks required

Row 0 : 0-511 blocks
Row1 : 511-1024
..
..
..
Row 'x' : 2048-2560

We need to find 'x'

x= $\frac{2048}{512}$ = 4
$\Rightarrow$ A[4][0] shares same set that of A[0][0]

11 votes -- pC (21.4k points)

Number of sets = cache size/ size of a set
= 64 KB / (16 B * 2) (two blocks per set)
= 2 K = 211
So, we need 11 bits for set indexing.

Number of WORD bits required = 4 as a cache block consists of 16 bytes and we need 4 bits to address each of them.

So, number of tag bits = 32 - 11 - 4 = 17

Total size of the tag = 17 * Number of cache blocks
= 17 * 211 * 2 (since each set has 2 blocks)

= 68 KB

We use the top 17 bits for tag and the next 11 bits for indexing and next 4 for offset. So, for two addresses to have the same cache index, their 11 address bits after the 4 offset bits from right must be same.

ARR[0][0] is located at virtual address 0x FF000 000. (FF000 is page address and 000 is page offset). So, index bits are 00000000000

Address of ARR[0][4] = 0xFF000 + 4 * sizeof (double) = 0xFF000 000 + 4*8 = 0xFF000 020 (32 = 20 in hex) (index bits differ)

Address of ARR[4][0] = 0xFF000 + 4 * 1024 * sizeof (double) [since we use row major storage] = 0xFF000 000 + 4096*8 = 0xFF000 000 + 0x8000 = 0xFF008 000 (index bits matches that of ARR [0][0] as both read 000 0000 0000)

Address of ARR[0][5] = 0xFF000 + 5 * sizeof (double) = 0xFF000 000+ 5*8 = 0xFF000 028 (40 = 28 in hex) (index bits differ)

Address of ARR[5][0] = 0xFF000 + 5 * 1024 * sizeof (double) [since we use row major storage] = 0xFF000 000 + 5120*8 = 0xFF000 000 + 0xA000 = 0xFF00A 000 (index bits differ)

So, only ARR[4][0] and ARR[0][0] have the same cache index.

The inner loop is iterating from 0 to 1023, so consecutive memory locations are accessed in sequence. Since cache block size is only 16 bytes and our element being double is of size 8 bytes, during a memory access only the next element gets filled in the cache. i.e.; every alternative memory access is a cache miss giving a hit ratio of 50%. (If loops i and j are reversed, all accesses will be misses and hit ratio will become 0).

12 votes -- Arjun Suresh (294k points)

1.2.31 Cache Memory: GATE2008-73 top

http://gateoverflow.in/43491

Selected Answer

block size=16B and one element=8B.so in one block 2 element will be stored.

for 1024*1024 element num of block required=1024*1024/2 =2^19 blocks required.

in one block first element will be a miss and second one is hit(since we are transferring two unit at a time)

=>hit ratio=total hit/total reference

=2^19/2^20

=1/2=0.5

=0.5*100=50%

9 votes -- asutosh kumar Biswal (10.2k points)

1.2.32 Cache Memory: GATE2008-IT-80 top

http://gateoverflow.in/3403

Selected Answer

Number of cache blocks = 8KB/(128*1) = 64

Number of sets in cache = Number of cache blocks/ 4 (4-way set)
= 64 / 4 = 16

So, number of SET bits required = 4 (as 2^4 = 16, and with 4 bits we can get 16 possible outputs)

We can now straight away choose (D) as answer but for confirmation can proceed further.

Since, only physical memory information is given we can assume cache is physically tagged (which is anyway the common case even in case of virtual memory). So, we can divide the physical memory into 16 regions so that, each set maps into only its assigned region. So, size of a region a set can address = 1MB/16 = 2^{16} Bytes = 2^{16} /128 = 2^9 cache blocks (as cache block size is 128 words = 128 bytes). So, when an access comes to an cache entry, it must be able to determine which out of the 2^9 possible physical block it is. In short it needs 9 bits for TAG.

Now, cache block size is 128 words and so to identify a word we need 7 bits for WORD.

12 votes -- Arjun Suresh (294k points)

1.2.33 Cache Memory: GATE2008-IT-81 top

http://gateoverflow.in/3405

Selected Answer

As shown in https://gateoverflow.in/3403/gate2008-it_80 we have 16 sets in cache and correspondingly 16 regions in physical memory to which each set is mapped. Now, WORD bit size is 7 as we need 7 bits to address 128 possible words in a cache block. So, the lowest 7 bits of 0C795H will be used for this giving us the remaining bits as
0000 1100 0111 1

Of these bits, the lower 4 are used for addressing the 16 possible sets, giving us the tag bits: 0000 1100 0 in (A) choice.

9 votes -- Arjun Suresh (294k points)

1.2.34 Cache Memory: GATE2009-29 top

http://gateoverflow.in/1315

Selected Answer

16 blocks and sets with 4 blocks each means there are 4 sets. So, the lower 2 bits are used for getting a set. And 4 way associative means in a set only the last 4 cache accesses can be stored.

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155

Mod 4 gives

0, 3, 1, 0, 3, 0, 1, 3, 0, 1, 3, 0, 0, 0, 1, 0, 3

Now for each of 0..3, the last 4 accesses will be in cache. So, {92, 32, 48, 8}, {155, 63, 159, 3}, {73, 129, 133, 1} and {} will be in cache. So, the missing element from choice is 216.

20 votes -- Arjun Suresh (294k points)

1.2.35 Cache Memory: GATE2010-48 top

http://gateoverflow.in/2352

Selected Answer

Ideally the answer should be 20 ns as it is the time to transfer a block from L2 to L1 and this time only is asked in question. But there is confusion regarding access time of L2 as this means the time to read data from L2 till CPU but here we need the time till L1 only. So, I assume the following is what is meant by the question.

A block is transferred from L2 to L1. And L1 block size being 4 words (since L1 is requesting we need to consider L1 block size and not L2 block size) and data width being 4 bytes, it requires one L2 access (for read) and one L1 access (for store). So, time = 20+2 = 22 ns.

39 votes -- Arjun Suresh (294k points)

1.2.36 Cache Memory: GATE2010-49 top

http://gateoverflow.in/43329

Selected Answer

The transfer time should be 4*200 + 20 = 820 ns. But this is not in option. So, I assume the following is what is meant by the question.

L2 block size being 16 words and data width between memory and L2 being 4 words, we require 4 memory accesses(for read) and 4 L2 accesses (for store). Now, we need to send the requested block to L1 which would require one more L2 access (for read) and one L1 access (for store). So, total time

= 4 * (200 + 20) + (20 + 2)

= 880 + 22

= 902 ns

18 votes -- Arjun Suresh (294k points)

1.2.37 Cache Memory: GATE2011_43 top

http://gateoverflow.in/2145

Selected Answer

Number of cache blocks = cache size / size of a block
=8 KB/32 B
=256

So, we need 8 bits for indexing the 256 blocks of the cache. And since a block is 32 bytes we need 5 WORD bits to address each byte. So, out of the remaining 19 bits (32 - 8 - 5) should be tag bits.

So, a tag entry size = 19 + 1(valid bit) + 1(modified bit) = 21 bits.
Total size of metadata = 21 * Number of cache blocks
= 21 * 256
= 5376 bits

14 votes -- Arjun Suresh (294k points)

1.2.38 Cache Memory: GATE2012-54 top

http://gateoverflow.in/2192

Selected Answer

Total cache size = 256 KB
Cache block size = 32 Bytes
So, number of cache entries = 256 K / 32 = 8 K

Number of sets in cache = 8 K/4 = 2 K as cache is 4-way associative.

So, log(2048) = 11 bits are needed for accessing a set. Inside a set we need to identify the cache entry.

No. of memory block possible = Memory size/Cache block size

$= \frac{2^{32}}{32} = 2^{27}$.

So, no. of memory block that can go to a single cache set

$= \frac{2^{27}}{2^{11}} = 2^{16}$.

So, we need 16 tag bits along with each cache entry to identify which of the possible 2^{16} blocks is being mapped there.

13 votes -- Arjun Suresh (294k points)

1.2.39 Cache Memory: GATE2012-55 top

http://gateoverflow.in/43311

Selected Answer

Total cache size = 256 KB
Cache block size = 32 Bytes

So, number of cache entries = 256 K / 32 = 8 K

Number of sets in cache = 8 K/4 = 2 K as cache is 4-way associative.

So, log(2048) = 11 bits are needed for accessing a set. Inside a set we need to identify the cache entry.
Total number of distinct cache entries = 2^{32}/cache entry size = $2^{32}/32 = 2^{27}$
Out of this 2^{27}, each set will be getting only $2^{27}/2^{11} = 2^{16}$ possible distinct cache entries as we use the first 11 bits to identify a set. So, we need 16 bits to identify a cache entry in a set, which is the number of bits in the tag field.

Size of cache tag directory = Size of tag entry * Number of tag entries
= 16 +(2+1+1) bits (2 valid, 1 modified, 1 replacement as given in question) * 8 K
= 20 * 8 = 160 Kbits

Not needed for this question, still:

Valid bit: Tells if the memory referenced by the cache entry is valid. Initially, when a process is loaded all entries are invalid. Only when a page is loaded, its entry becomes valid.

Modified bit: When processor writes to a cache location its modified bit is made 1. This information is used when a cache entry is replaced- entry 0 means no update to main memory needed. Entry 1 means an update is needed.

Replacement bit: This is needed for the cache replacement policy. Explained in the below link:
https://www.seas.upenn.edu/~cit595/cit595s10/handouts/LRUreplacementpolicy.pdf

8 votes -- Arjun Suresh (294k points)

1.2.40 Cache Memory: GATE2013_20 top http://gateoverflow.in/1442

Selected Answer

Number of sets in cache = v. The question gives a sequencing for the cache lines. For set 0, the cache lines are numbered 0, 1, .., k-1. Now for set 1, the cache lines are numbered k, k+1,... k+k-1 and so on. So, main memory block j will be mapped to set (j mod v), which will be any one of the cache lines from (j mod v) * k to (j mod v) * k + (k-1). (Associativity plays no role in mapping- k-way associativity means there are k spaces for a block and hence reduces the chances of replacement.)

26 votes -- Arjun Suresh (294k points)

1.2.41 Cache Memory: GATE2014-1-44 top http://gateoverflow.in/1922

Selected Answer

There are N accesses to cache.
Out of these n are unique block addresses.
Now, we need to find the number of misses. (min. n misses are guaranteed whatever be the access sequence due to n unique block addresses)

We are given that between two consecutive accesses to the same block, there can be only k unique block addresses. So, for a block to get replaced we can assume that all the next k block addresses goes to the same set (given cache is set-associative) which will be the worst case scenario (they may also go to a different set but then there is lesser chance of a replacement). Now, if associativity size is >= k, and if we use LRU (Least Recently Used) replacement policy, we can guarantee that these k accesses won't throw out our previously accessed cache entry (for that we need at least k accesses). So, this means we are at the best-cache scenario for cache replacement -- out of N accesses we miss only n (which are unique and can not be helped from getting missed and there is no block replacement in cache). So, miss ratio is n/N.

PS: In question it is given "bounded above by k", which should mean k unique block accesses as k is an integer, but to ensure no replacement this must be 'k-1'. Guess, a mistake in question.

47 votes -- Arjun Suresh (294k points)

1.2.42 Cache Memory: GATE2014-2-43 top http://gateoverflow.in/2009

Selected Answer

(A) A smaller block size means during a memory access only a smaller part of near by addresses are brought to cache- meaning spatial locality is reduced.

(B) A smaller block size means more number of blocks (assuming cache size constant)and hence we need more cache tag bits to identify the correct block. So, cache tag becomes bigger.

(C) A smaller block size implying larger cache tag is true, but this can't lower cache hit time in any way.

(D) A smaller block size incurs a lower cache miss penalty. This is because during a cache miss, an entire cache block is fetched from next lower level of memory. So, a smaller block size means only a smaller amount of data needs to be fetched and hence reduces the miss penalty (Cache block size can go til the size of data bus to the next level of memory, and beyond this only increasing the cache block size increases the cache miss penalty).

25 votes -- Arjun Suresh (294k points)

1.2.43 Cache Memory: GATE2014-2-44 top

http://gateoverflow.in/2010

Selected Answer

If associativity is doubled, keeping the capacity and block size constant, then the number of sets gets halved. So, width of set index decoder can surely decrease - (B) is false.
Width of way-selection multiplexer must be increased as we have to double the ways to choose from- (C) is false

As the number of sets gets decreased, the number of possible cache block entries that a set maps to gets increased. So, we need more tag bits to identify the correct entry. So, (A) is also false.

(D) is the correct answer- main memory data bus has nothing to do with cache associativity- this can be answered without even looking at other options.

17 votes -- Arjun Suresh (294k points)

1.2.44 Cache Memory: GATE2014-2-9 top

http://gateoverflow.in/1963

Selected Answer

Number of sets = cache size / sizeof a set

Size of a set = blocksize * no. of blocks in a set
= 8 words * 4 (4-way set-associative)
= 8*4*4 (since a word is 32 bits = 4 bytes)
= 128 bytes.

So, number of sets = 16 KB / (128 B) = 128

Now, we can divide the physical address space equally between these 128 sets. So, the number of bytes each set can access
= 4 GB / 128
= 32 MB
= 32/4 = 8 M words = 1 M blocks. (2^{20} blocks)

So, we need 20 tag bits to identify these 2^{20} blocks.

21 votes -- Arjun Suresh (294k points)

1.2.45 Cache Memory: GATE2014-3-44 top

http://gateoverflow.in/2078

Selected Answer

```
The question is to find the time taken for,
"100 fetch operation and 60 operand red operations and 40 memory
operand write operations"/"total number of instructions".
```

```
Total number of instructions= 100+60+40 =200

Time taken for 100 fetch operations(fetch =read)
= 100*((0.9*1)+(0.1*5)) // 1 corresponds to time taken for read
                        // when there is cache hit

= 140 ns //0.9 is cache hit rate

Time taken for 60 read operations = 60*((0.9*1)+(0.1*5))
                                  = 84ns

Time taken for 40 write operations = 40*((0.9*2)+(0.1*10))
                                   = 112 ns

// Here 2 and 10 the time taken for write when there is cache
// hit and no cahce hit respectively

So,the total time taken for 200 operations is = 140+84+112
                                              = 336ns

Average time taken = time taken per operation = 336/200
                                              = 1.68 ns
```

4 votes -- Divya Bharti (4k points)

Fetch is also a memory read operation.

Avg access time $= \frac{160(0.9\times1+0.1\times5)+40(0.9\times2+0.1\times10)}{200} = \frac{160\times1.4+40\times2.8}{200} = \frac{336}{200} = 1.68$

22 votes -- aravind90 (589 points)

1.2.46 Cache Memory: GATE2015-2_24 top

http://gateoverflow.in/8119

Selected Answer

Ans 14 ns = 0.8(5) + 0.2(50)

18 votes -- Vikrant Singh (13.4k points)

1.2.47 Cache Memory: GATE2015-3_14 top

http://gateoverflow.in/8410

Selected Answer

Block size of 16 bytes means we need 4 offset bits. (The lowest 4 digits of memory address are offset bits)

Number of sets in cache (cache lines) = 2^{12} so the next lower 12 bits are used for set indexing.

The top 4 bits (out of 20) are tag bits.

So, Answer A.

13 votes -- Arjun Suresh (294k points)

1.2.48 Cache Memory: GATE2016-2-32 top

http://gateoverflow.in/39622

Selected Answer

Physical Address = 40

Tag + Set + Block Offset = 40

T + S + B = 40 ----------- (1)

We have , Cache Size = number of sets $\times$ blocks per set $\times$ Block size

512 KB = number of sets$\times$ 8 $\times$ Block size

Number of sets$\times$ Block size = 512/8 KB = 64 KB

$S + B = 16$ ---------(2)

from (1) & (2)

T = **24 bits (Ans)**

Second way :

Cache Size = 2^{19}
MM size = 2^{40}
This means, We need to map 2^{40} / 2^{19}=2^{21} Blocks to one line. And a set contain 2^3 lines.
Therefore 2^{24} blocks are mapped to one set.
Using Tag field, I need to identify which one block out of 2^{24} blocks are present in this set.
Hence 24 bits are needed in Tag field.

25 votes -- Himanshu Agarwal (16.2k points)

In question block size has not been given,so we can assume block size 2^x Byte.

Number of Blocks:- $512 \text{ X } 2^{10} / 2^x = 2^{19-x}$

Number of sets:- $2^{19-x} / 8 = 2^{16-x}$

So number of bits for sets=16-x

Let number of bits for Tag=T

And we have already assumed block size 2^x Byte,therefore number of bits for block size is x

And finally, $T + (16-x) + x = 40$

$T+16 = 40$

$T = 24$

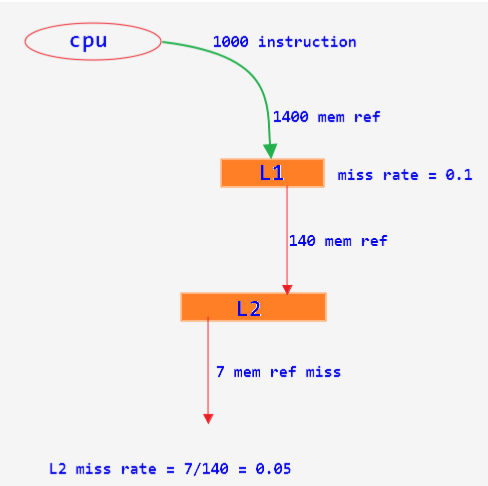
13 votes -- ajit (3.4k points)

1.2.49 Cache Memory: GATE2017-1-25 top

http://gateoverflow.in/118305

Selected Answer

Answer = 0.05.

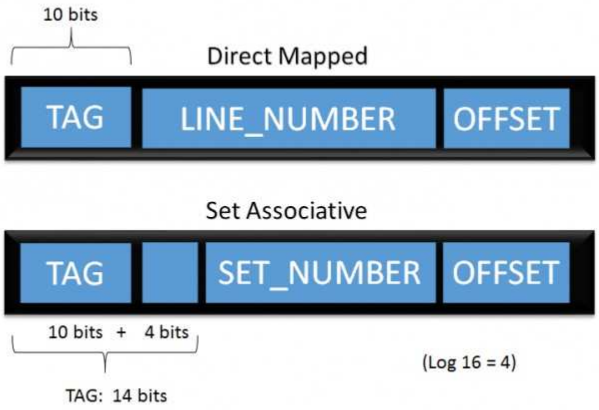


17 votes -- Debashish Deka (51.4k points)

1.2.50 Cache Memory: GATE2017-1-54 top

http://gateoverflow.in/118748

Selected Answer



In set-associative 1 set = 16 lines. So the number of index bits will be 4 less than the direct mapped case.

So, **Tag bits** increased to 14 bits.

13 votes -- Ahwan Mishra (5.3k points)

1.2.51 Cache Memory: GATE2017-2-29 top

http://gateoverflow.in/118371

Selected Answer

In two-level memory system (hierarchical), it is clear that the second level is accessed only when first level access is a miss. So, we must include the first level access time in all the memory access calculations. Continuing this way for any level, we must include that level access time (without worrying about the hit rate in that level), to all memory accesses coming to that level (i.e., by just considering the miss rate in the previous level). So, for the given question, we can get the following equation:

$$\text{AMAT} = \text{L1 access time} + \text{L1 miss rate} \times \text{L2 access time} + \text{L1 miss rate} \times \text{L2 miss rate} \times \text{Main memory access ti}$$

$$2 = 1 + x \times 8 + 0.5x^2 \times 18$$
$$\implies 9x^2 + 8x - 1 = 0$$

$$\implies x = \frac{-8 \pm \sqrt{64+36}}{18} = \frac{2}{18} = 0.111\,.$$

So, A.

10 votes -- Arjun Suresh (294k points)

1.2.52 Cache Memory: GATE2017-2-45 top

http://gateoverflow.in/118597

Selected Answer

L2 cache is shared between Instruction and Data (is it always?, see below)

So, average read time

= Fraction of Instruction Fetch * Average Instruction fetch time + Fraction of Data Fetch * Average Data Fetch Time

Average Instruction fetch Time = L1 access time + L1 miss rate * L2 access time + L1 miss rate * L2 miss rate * Memory access time

= 2 + 0.2 * 8 + 0.2 * 0.1 * 90
= 5.4 ns

Average Data fetch Time = L1 access time + L1 miss rate * L2 access time + L1 miss rate * L2 miss rate * Memory access time

= 2 + 0.1 * 8 + 0.1 * 0.1 * 90
= 3.7 ns

So, average memory access time

$$= 0.6 \times 5.4 + 0.4 \times 3.7 = 4.72ns$$

Now, why L2 must be shared? Because we can otherwise use it for either Instruction or Data and it is not logical to use it for only 1. Ideally this should have been mentioned in question, but this can be safely assumed also (not enough merit for Marks to All). Some more points in the question:

> Assume that the caches use the referred-word-first read policy and the writeback policy

Irrelevant for solving the given question as we do not care for writes

> Assume that all the caches are direct mapped caches.

Again irrelevant as average access times are given

> Assume that the dirty bit is always 0 for all the blocks in the caches

Again irrelevant as dirty bits are for cache replacement- which is not asked in the given question

12 votes -- Arjun Suresh (294k points)

1.2.53 Cache Memory: GATE2017-2-53 top http://gateoverflow.in/118613

Selected Answer

No. of blocks of main Memory $= \frac{2^{32}}{2^5} = 2^{27}$

And there are $512 = 2^9$ lines in Cache Memory.

Tag bits tell us to how many blocks does 1 line in Cache memory points to

1 cache line points to $\frac{2^{27}}{2^9} = 2^{18}$ lines

So, 18 bits are required as TAG bits.

11 votes -- Manish Joshi (25.2k points)

1.3 Cisc Risc Architecture(1) top

1.3.1 Cisc Risc Architecture: GATE1999-2.22 top http://gateoverflow.in/1499

The main difference(s) between a CISC and a RISC processor is/are that a RISC processor typically

(a) has fewer instructions

(b) has fewer addressing modes

(c) has more registers

(d) is easier to implement using hard-wired logic

gate1999 co&architecture normal cisc-risc-architecture

Answer

Answers: Cisc Risc Architecture

1.3.1 Cisc Risc Architecture: GATE1999-2.22 top http://gateoverflow.in/1499

Selected Answer

All are properties of RISC processor..

http://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/whatis/index.html

http://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/risccisc/index.html

http://homepage3.nifty.com/alpha-1/computer/Control_E.html

5 votes -- Digvijay (47k points)

1.4 Clock Frequency(2) top

1.4.1 Clock Frequency: GATE1992_01,iii top http://gateoverflow.in/547

(iii) Many microprocessors have a specified lower limit on clock frequency (apart from the maximum clock frequency limit) because ______

gate1992 normal co&architecture clock-frequency

Answer

1.4.2 Clock Frequency: GATE2007-IT-36 top http://gateoverflow.in/3469

The floating point unit of a processor using a design D takes $2t$ cycles compared to t cycles taken by the fixed point unit. There are two more design suggestions D_1 and D_2. D_1 uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design D. D_2 uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design D. For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative performances of three designs?
($D_i > D_j$ denotes that D_i is faster than D_j)

A. $D_1 > D > D_2$
B. $D_2 > D > D_1$
C. $D > D_2 > D_1$
D. $D > D_1 > D_2$

gate2007-it co&architecture normal clock-frequency

Answer

Answers: Clock Frequency

1.4.1 Clock Frequency: GATE1992_01,iii top http://gateoverflow.in/547

Selected Answer

Clock frequency becomes low means time period of clock becomes high. When this time period increases beyond the time period in which the non-volatile memory contents must be refreshed, we loose those contents. So, clock frequency can't go below this value.

Ref: http://gateoverflow.in/261/microprocessors-specified-frequency-frequency-___________

3 votes -- Rajarshi Sarkar (35k points)

1.4.2 Clock Frequency: GATE2007-IT-36 top http://gateoverflow.in/3469

Selected Answer

(B)

$$T = 0.8 \times \text{time taken in fixed point} + 0.2 \times \text{time taken in floating point}$$
$$D = 0.8 \times t + 0.2 \times 2t = 1.2t$$

$$D_1 = 0.8 \times 1.3t + 0.2 \times 0.7 \times 2t = 1.04t + .28t = 1.32t$$

$$D_2 = 0.8 \times 0.6t + 0.2 \times 1.1 \times 2t = 0.48t + .44t = 0.92t$$

So, D_2 is the best design for this given program followed by D and then D_1. Option B.

14 votes -- Vicky Bajoria (4.9k points)

1.5 Conflict Misses(1) top

1.5.1 Conflict Misses: GATE2017-1-51 top http://gateoverflow.in/118745

Consider a $2-$way set associative cache with 256 blocks and uses LRU replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

$$\{0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129\}$$

is repeated 10 times. The number of *conflict misses* experienced by the cache is __________ .

gate2017-1 co&architecture cache-memory conflict-misses normal numerical-answers

Answer

Answers: Conflict Misses

1.5.1 Conflict Misses: GATE2017-1-51 top http://gateoverflow.in/118745

Selected Answer

I am reiterating the same thing what Arjun already explained.

{0,128,256,128,0,128,256,128,1,129,257,129,1,129,257,129}

1st Iteration:

for {0,128,256,128,0,128,256,128}

Block Id	Type	Set0 content
0	Compulsory Miss	0
128	Compulsory Miss	0 128
256	Compulsory Miss	128 256
128	hit	256 128
0	Conflict Miss	128 0
128	hit	0 128
256	Conflict Miss	128 256
128	hit	256 128

Total number of conflict misses =2;

Similarly for {1,129,257,129,1,129,257,129}, total number of conflict misses in set1 = 2

Total number of conflict misses in 1st iteration = 2+2=4

2nd iteration:

for {0,128,256,128,0,128,256,128}

Block Id	Type	Set0 content
0	Conflict Miss	128 0

128	hit	0 128
256	Conflict Miss	128 256
128	hit	256 128
0	Conflict Miss	128 0
128	hit	0 128
256	Conflict Miss	128 256
128	hit	256 128

Total number of conflict misses = 4

Similarly for {1,129,257,129,1,129,257,129}, total number of conflict misses in set1 = 4

Total Number of conflict misses in 2nd iteration = 4+4=8

Note that content of each set is same, before and after 2nd iteration. Therefore each of the remaining iterations will also have 8 conflict misses.

Therefore, overall conflict misses = 4+8*9 = 76

10 votes -- suraj (5.1k points)

1.6 Control Unit(1) top

1.6.1 Control Unit: Gate1987-1-vi top http://gateoverflow.in/166

Microprogrammed control unit:

a)is faster than a hardwired control unit

b)facilitates easy implementation of new instructions

c)is useful when very small programs are to be run

d)usually refers to control unit of a microprocessor

gate1987 microprogramming control-unit easy co&architecture

Answer

Answers: Control Unit

1.6.1 Control Unit: Gate1987-1-vi top http://gateoverflow.in/166

Selected Answer

(a) is wrong. Microprogrammed CU can never be faster than hardwired CU. Microprogrammed CU it has an extra layer on top of hardwired CU and hence can only be slower than hardwired CU.

(b) is a suitable answer as we can add new instruction by changing the content of control memory.

(c) is not correct as when only small programs are there, hardwired control makes more sense.

(d) control unit can also be hardwired, so this is also not correct.

Reference: http://www2.mta.ac.il/~carmi/Teaching/Architecture/SlidesOriginal/ch07%20-%20Microprogrammed%20Control.pdf

5 votes -- Arjun Suresh (294k points)

1.7 Data Dependences(2) top

1.7.1 Data Dependences: GATE2007-IT-39 top http://gateoverflow.in/3472

Data forwarding techniques can be used to speed up the operation in presence of data dependencies. Consider the following replacements of LHS with RHS.

i. R1→ Loc, Loc→ R2 ≡ R1→ R2, R1 → Loc
ii. R1→ Loc, Loc→ R2 ≡ R1→ R2
iii. R1→ Loc, R2 → Loc ≡ R1→ Loc
iv. R1→ Loc, R2 → Loc ≡ R2→ Loc

In which of the following options, will the result of executing the RHS be the same as executing the LHS irrespective of the instructions that follow ?

A. i and iii
B. i and iv
C. ii and iii
D. ii and iv

gate2007-it data-dependences co&architecture

Answer

1.7.2 Data Dependences: GATE2015-3_47 top

http://gateoverflow.in/8556

Consider the following code sequence having five instructions from I_1 to I_5. Each of these instructions has the following format.

OP Ri, Rj, Rk

Where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.

I_1: ADD R1, R2, R3

I_2: MUL R7, R1, R3

I_3: SUB R4, R1, R5

I_4: ADD R3, R2, R4

I_5: MUL R7, R8, R9

Consider the following three statements.

S1: There is an anti-dependence between instructions I_2 and I_5

S2: There is an anti-dependence between instructions I_2 and I_4

S3: Within an instruction pipeline an anti-dependence always creates one or more stalls

Which one of the above statements is/are correct?

A. Only S1 is true
B. Only S2 is true
C. Only S1 and S3 are true
D. Only S2 and S3 are true

gate2015-3 co&architecture pipelining data-dependences normal

Answer

Answers: Data Dependences

1.7.1 Data Dependences: GATE2007-IT-39 top

http://gateoverflow.in/3472

Selected Answer

(i) is true. Both LOC and R2 are getting the value of R1 in LHS and RHS.

(ii) false, because R2 gets the correct data in both LHS and RHS, but LOC is not updated in RHS.

(iii) is wrong because R2 is writing last, not R1 in LHS, but not in RHS.

(iv) is true. The first write to Loc in LHS is useless as it is overwritten by the next write.

So, answer is B.

11 votes -- Vicky Bajoria (4.9k points)

1.7.2 Data Dependences: GATE2015-3_47 top

http://gateoverflow.in/8556

Selected Answer

Answer should be B.

Anti-dependence can be overcome in pipeline using register renaming. So, "always" in S3 makes it false. Also, if I2 is completed before I4 (execution stage of MUL), then also there won't be any stall.

18 votes -- ppm (627 points)

1.8 Data Path(4) top

1.8.1 Data Path: GATE 2016-2-30 top

http://gateoverflow.in/39627

Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G, respectively. Given two instances of U_F and two instances of U_G, it is required to implement the computation $F(G(X_i))$ for $1 \leq i \leq 10$. Ignoring all other delays, the minimum time required to complete this computation is ____________ nanoseconds.

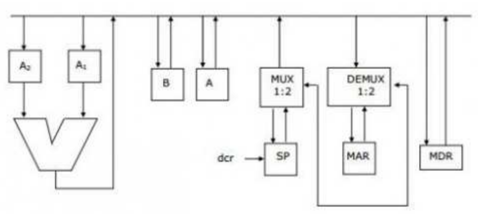
gate2016-2 co&architecture data-path normal numerical-answers

Answer

1.8.2 Data Path: GATE2001-2.13 top

http://gateoverflow.in/731

Consider the following data path of a simple non-pipelined CPU. The registers A, B, A_1, A_2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size $8 \times (2:1)$ and the DEMUX is of size $8 \times (1:2)$. Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.



The CPU instruction "push r" where, r = A or B has the specification

M[SP] ← r

SP ← SP - 1

How many CPU clock cycles are required to execute the "push r" instruction?

A. 2
B. 3
C. 4
D. 5

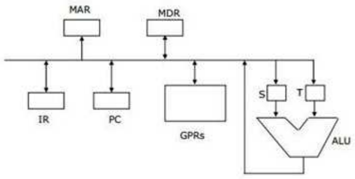
gate2001 co&architecture data-path machine-instructions normal

Answer

1.8.3 Data Path: GATE2005-79 top

http://gateoverflow.in/1402

Consider the following data path of a CPU.



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction “add R0, R1” has the register transfer interpretation R0 <= R0 + R1. The minimum number of clock cycles needed for execution cycle of this instruction is:

A. 2
B. 3
C. 4
D. 5

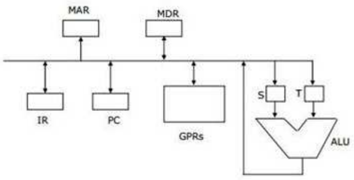
gate2005 co&architecture machine-instructions data-path normal

Answer

1.8.4 Data Path: GATE2005-80 top

http://gateoverflow.in/43568

The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.



The instruction "call Rn, sub” is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

Rn <= PC + 1;

PC <= M[PC];

The minimum number of CPU clock cycles needed during the execution cycle of this instruction is:

A. 2
B. 3
C. 4
D. 5

co&architecture normal gate2005 data-path machine-instructions

Answer

Answers: Data Path

1.8.1 Data Path: GATE 2016-2-30 top

http://gateoverflow.in/39627

Selected Answer

The same concept is used in pipelining. Bottleneck here is U_F as it takes 5 ns while U_G takes 3ns only. We have to do 10 such calculations and we have 2 instances of U_F and U_G respectively. So, U_F can be done in $50/2 = 25$ nano seconds. For the start U_F needs to wait for U_G output for 3 ns and rest all are pipelined and hence no more wait. So, answer is

$$3 + 25 = 28ns.$$

33 votes -- Arjun Suresh (294k points)

if somebody is trying to understand through a pipeline diagram,

18 votes -- Motamarri Anusha (11.6k points)

1.8.2 Data Path: GATE2001-2.13 top

http://gateoverflow.in/731

Selected Answer

A microinstruction can't be further broken down into two or more. It can take more than a cycle if it involves a memory access. The first instruction given here isn't a microinstruction. It is an assembly lang instruction.

It can be broken down as:

T1 , T2: MAR<--SP

T3.   : MDR<-- r , SP<-- SP-1 (it is not mandatory to decrement it in this cycle. Anyway, it can be decremented locally)

T4, T5   : M [MAR] <-- MDR

The problem says, 8-bit MDR, 8-bit data bus, 8 bit registers.Can't you see that the given CPU is 8-bit? 8 multiplexers transfer 8 bits when selection input is 0 and 1 respectively. During cycle 1, bits in even positions are moved to MAR. During cycle 2, bits in odd positions are transferred to MAR. We certainly need to move 16-bit SP to 16-bit MAR via a 8-bit bus. So, 2 cycles to get SP to MAR.

The given data path has a single bus, which requires r to be carried in a separate cycle. For the contents of r to be moved to MDR during the cycles T1 or T2, address and data bus should be separate. Here, it ain't the case.

Memory read takes 2 more cycles. In total, we need 5 of them clock cycles to execute a push.

https://www.cise.ufl.edu/~mssz/CompOrg/CDA-proc.html

Computer organization pal chaudari page 334-335

Computer architecture by behrooz parahmi exercise 7.6
Thank me later.

4 votes -- Rajaneesh Polavarapu (241 points)

1.8.3 Data Path: GATE2005-79 top

http://gateoverflow.in/1402

Selected Answer

instruction fetch require two cycles but question asks how many clock cycles require for execution part only !

now for execution

1) R1 out,Sin   S <- R0 ...... 1st cycle

2) R2 out,Tin,   T <- R1 ...... 2nd cycle

3)S out Tout Add R0 in , R0 <- R0 + R1 ..... 3rd cycle

so 3 cycles for execution

as it is asked for only execution cycles no of cycles=3

If it has been asked for instruction cycles then ans will be 5

hence option B is correct.

12 votes -- Pooja Palod (32.4k points)

1.8.4 Data Path: GATE2005-80 top

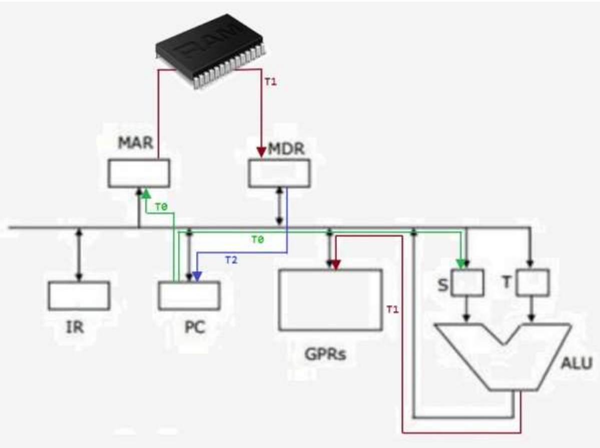
http://gateoverflow.in/43568

Selected Answer

$MAR \leftarrow PC$ ..... 1 cycle
$S \leftarrow PC$ (Since these two actions are independent they can be done in same cycle)
$MDR \leftarrow M[MAR]$ ..... 2nd cycle **(System BUS)**
$RN \leftarrow S+1$ (ALU Is free and the two actions are independent.) (**Internal BUS)**
$PC \leftarrow MDR$ ----- 3rd cycle

Therefore 3 cycles needed.

A rough sketch:



18 votes -- Riya Roy(Arayana) (7.1k points)

1.9 Dma(2) top

1.9.1 Dma: GATE 2016-1-31 top

http://gateoverflow.in/39698

The size of the data count register of a DMA controller is 16bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _________-.

gate2016-1 co&architecture dma normal numerical-answers

Answer

1.9.2 Dma: GATE2011_28 top

http://gateoverflow.in/2130

On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

```
        Initialize the address register
```

```
       Initialize the count to 500
LOOP:  Load a byte from device
       Store in memory at address given by address register
       Increment the address register
       Decrement the count
       If count !=0 go to LOOP
```

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

(A) 3.4

(B) 4.4

(C) 5.1

(D) 6.7

gate2011 co&architecture dma normal

Answer

Answers: Dma

1.9.1 Dma: GATE 2016-1-31 top

http://gateoverflow.in/39698

Selected Answer

Data count register gives the number of words the DMA can transfer in a single cycle..

Here it is 16 bits.. so max 2^{16} words can be transferred in one cycle..

Since memory is byte addressable.. 1 word = 1 byte
so 2^{16} bytes in 1 cycle..

Now for the given file..

File size = 29154 KB= 29154 * 2^{10} B

1 cylce $\rightarrow$ DMA transfers 2^{16} B

i.e

1 B transfered by DMA $\rightarrow$ $1/2^{16}$ cycles.

Now for full file of size 29154 KB, minimum number of cylces = (29154 * 2^{10} B) / 2^{16} = 455.53
But number of cylces is asked so 455.53$\rightarrow$ 456..

17 votes

-- Abhilash Panicker (8.8k points)

1.9.2 Dma: GATE2011_28 top

http://gateoverflow.in/2130

Selected Answer

```
                STATEMENT                                   CLOCK CYCLE(S) NEEDED
       Initialize the address register                               1
       Initialize the count to 500                                   1
LOOP:  Load a byte from device                                       2
       Store in memory at address given by address register          2
       Increment the address register                                1
       Decrement the count                                           1
       If count != 0 go to LOOP                                      1

Interrupt driven transfer time = 1+1+500×(2+2+1+1+1) = 3502
DMA based transfer time = 20+500*2 = 1020
Speedup = 3502/1020 = 3.4
```

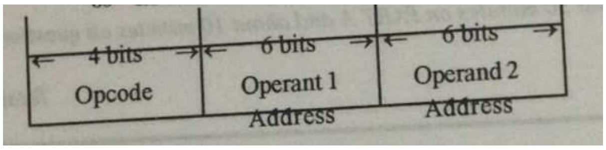
31 votes -- Manu Thakur (6k points)

1.10 Expanding Opcode(1) top

1.10.1 Expanding Opcode: GATE1988-2ii top http://gateoverflow.in/91676

Using an expanding opcode encoding for instructions, is it possible to encode all of the following in an instruction format shown in the below figure. Justify your answer.

14 double address instructions
127 single address instructions
60 no address (zero address) instructions



gate1988 normal co&architecture expanding-opcode descriptive

Answer

Answers: Expanding Opcode

1.10.1 Expanding Opcode: GATE1988-2ii top http://gateoverflow.in/91676

Selected Answer

4 bits are for the opcode so number of 2 address instructions will be 2^4 =16 ---so 14 double instructions are possible

But out of 16 only 14 are used so 2 are still left which can be used for 1 address instruction

For 1 address instruction we can use not only the 2 left over but also the 6 bits of operand1(to make it one address)--- so 6 bits that is 64 so they are laready 2 which each contains 64 so total 128 single address instructions -----so 127 single instructions are possible

But out of 128 ,127 are used so 1 left which can be used for zero address instruction to make number of zero address we can use the operand2 address 6 bits so total possible are 64 so total 1*64 = 64 zero address instructions are possible

So all encoding are possible

1 votes -- Pavan Kumar Munnam (10k points)

1.11 Instruction Execution(4) top

1.11.1 Instruction Execution: GATE1995-1.2 top http://gateoverflow.in/2589

Which of the following statements is true?

A. ROM is a Read/Write memory

B. PC points to the last instruction that was executed

C. Stack works on the principle of LIFO

D. All instructions affect the flags

gate1995 co&architecture normal instruction-execution

Answer

1.11.2 Instruction Execution: GATE2002-1.13 top

http://gateoverflow.in/817

Which of the following is not a form of memory

A. instruction cache
B. instruction register
C. instruction opcode
D. translation look-a-side buffer

gate2002 co&architecture easy instruction-execution

Answer

1.11.3 Instruction Execution: GATE2006-43 top

http://gateoverflow.in/1819

Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction “bbs reg, pos, label” jumps to label if bit in position pos of register operand reg is one. A register is 32 bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

$temp \leftarrow reg \& mask$

Branch to label if temp is non-zero. The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

A. $mask \leftarrow 0\text{x}1 << pos$
B. $mask \leftarrow 0\text{xffffffff} << pos$
C. $mask \leftarrow pos$
D. $mask \leftarrow 0\text{xf}$

gate2006 co&architecture normal instruction-execution

Answer

1.11.4 Instruction Execution: GATE2017-1-49 top

http://gateoverflow.in/118332

Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr. No.	Instruction
i :	add R2, R3, R4
i + 1 :	sub R5, R6, R7
i + 2 :	cmp R1, R9, R10
i + 3 :	beq R1, Offset

If the target of the branch instruction is i, then the decimal value of the Offset is ____________ .

gate2017-1 co&architecture normal numerical-answers instruction-execution

Answer

Answers: Instruction Execution

1.11.1 Instruction Execution: GATE1995-1.2 top

http://gateoverflow.in/2589

Selected Answer

It is C.

Only the top of the stack can be accessed at any time. You can imagine a stack to be opened from only one side data structure. So that if we put one thing over the other, we are able to access the last thing we inserted first. That is Last in

First Out (LIFO).

ROM is Read Only Memory.

PC points to the next instruction to be executed.

Not all instructions affect the flags.

8 votes -- Gate Keeda (19.1k points)

1.11.2 Instruction Execution: GATE2002-1.13 top http://gateoverflow.in/817

Selected Answer

The instruction opcode is a part of the instruction which tells the processor what operation is to be performed so it is not a form of memory while the others are

10 votes -- Bhagirathi Nayak (13.3k points)

1.11.3 Instruction Execution: GATE2006-43 top http://gateoverflow.in/1819

Selected Answer

a. $mask \leftarrow 0\text{x}1 << pos$

We want to check for a particular bit position say 2 (third from right). Let the number be 0xA2A7 (last 4 bits being 0111). Here, the bit at position 2 from right is 1. So, we have to AND this with 0x0004 as any other flag would give wrong value (may count other bits or discard the bit at position "pos"). And 0x0004 is obtained by 0x1 << 2 (by shifting 1 "pos" times to the left we get a flag with 1 being set only for the "pos" bit position).

10 votes -- Arjun Suresh (294k points)

1.11.4 Instruction Execution: GATE2017-1-49 top http://gateoverflow.in/118332

Selected Answer

Ans:(-16)

assume addresses start with 2000 for first instruction.

2000---add R2,R3,R4

2004--sub r5,r6,r7

2008---r1,r9,r10

2012--beq r1,offset //pc after instruction fetch of this instruction will be 2016,and branch target is 2000 ,offset will be (2016-16
)=2000

2016------next instruction

6 votes -- jatin saini (2.1k points)

1.12 Instruction Format(4) top

1.12.1 Instruction Format: GATE 2016-2-31 top http://gateoverflow.in/39601

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is __________.

gate2016-2 instruction-format machine-instructions co&architecture normal numerical-answers

Answer

1.12.2 Instruction Format: GATE1992_01,vi top http://gateoverflow.in/551

In an 11-bit computer instruction format, the size of address field is 4-bits. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero-address instructions it can support is ________

gate1992 co&architecture machine-instructions instruction-format normal

Answer

1.12.3 Instruction Format: GATE1994_3.2 top http://gateoverflow.in/2479

State True or False with one line explanation

Expanding opcode instruction formats are commonly employed in RISC. (Reduced Instruction Set Computers) machines.

gate1994 co&architecture machine-instructions instruction-format normal

Answer

1.12.4 Instruction Format: GATE2014-1-9 top http://gateoverflow.in/1767

A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is ____________

gate2014-1 co&architecture machine-instructions instruction-format numerical-answers normal

Answer

Answers: Instruction Format

1.12.1 Instruction Format: GATE 2016-2-31 top http://gateoverflow.in/39601

Selected Answer

Answer => 500 bytes

Number of register = 64

Number of bits to address register = $\lceil log_2 64 \rceil$ = 6 bits

Number of Instruction = 12

Opcode size = $\lceil log_2 12 \rceil$ = 4

Opcode**(4)**	reg1**(6)**	reg2**(6)**	reg2**(6)**	Immediate**(12)**

Total bits per instruction = 34

Total bytes per instruction= 4.25

Due to byte alignment we cannot store 4.25 bytes, without wasting 0.75 bytes ,

So Total bytes per instruction = 5

Total instruction = 100

Total size = Number of instruction $\times$ Size of instruction

100$\times$ 5= 500 Byes

23 votes -- Akash (43.8k points)

1.12.2 Instruction Format: GATE1992_01,vi top http://gateoverflow.in/551

Selected Answer

No. of possible instruction encoding = $2^{11} = 2048$

No. of encoding taken by two-address instructions = $5 \times 2^4 \times 2^4 = 1280$

No. of encoding taken by one-address instructions = $32 \times 2^4 = 512$

So, no. of possible zero-address instructions = $2048 - (1280 + 512) = 256$

21 votes -- Arjun Suresh (294k points)

1.12.3 Instruction Format: GATE1994_3.2 top http://gateoverflow.in/2479

Selected Answer

I think the answer is **TRUE**.

RISC systems use fixed length instruction to simplify pipeline.

eg: MIPS, PowerPC: Instructions are 4 bytes long.

CISC systems use Variable-length instructions.

eg: Intel 80x86: Instructions vary from 1 to 17 bytes long.

Now the challenge is: How to fit multiple sets of instruction types into same (limited) number of bits (Fixed size instruction)?

Here comes Expanding opcode into the picture.

RISC systems commonly uses Expanding opcode technique to have fixed size instructions.

6 votes -- Sachin Mittal (7.1k points)

1.12.4 Instruction Format: GATE2014-1-9 top http://gateoverflow.in/1767

Selected Answer

64 registers means 6 bits $\left(\lceil \log_2 64 \rceil = 6\right)$ for a register operand. So, 2 register operand requires 12 bits. Now, 45 instructions require another 6 bits for opcode $\left(\lceil \log_2 45 \rceil = 6\right)$. So, totally 18 bits. So, we have 32 - 18 = 14 bits left for the immediate operand. So, the max value will be $2^{14} - 1 = 16383$ (as the operand is unsigned we do not need a sign bit and with 14 bits we can represent from 0 to $2^{14} - 1$)

30 votes -- Arjun Suresh (294k points)

1.13 Instruction Prefetch(1) top

1.13.1 Instruction Prefetch: GATE1992-01,iv top http://gateoverflow.in/548

Many of the advanced microprocessors prefetch instructions and store it in an instruction buffer to speed up processing. This speed up is achieved because ________

gate1992 co&architecture easy instruction-prefetch

Answer

Answers: Instruction Prefetch

1.13.1 Instruction Prefetch: GATE1992-01,iv top http://gateoverflow.in/548

Selected Answer

Because CPU is faster than memory. Fetching instructions from memory would require considerable amount of time while CPU is much faster. So, prefetching the instructions to be executed can save considerable amount of waiting time.

2 votes -- Arjun Suresh (294k points)

1.14 Interrupts(6) top

1.14.1 Interrupts: GATE1987-1-viii top http://gateoverflow.in/80274

On receiving an interrupt from a I/O device the CPU:

A. Halts for a predetermined time.
B. Hands over control of address bus and data bus to the interrupting device.
C. Branches off to the interrupt service routine immediately.
D. Branches off to the interrupt service routine after completion of the current instruction.

gate1987 co&architecture interrupts

Answer

1.14.2 Interrupts: GATE1995_1.3 top http://gateoverflow.in/2590

In a vectored interrupt

A. The branch address is assigned to a fixed location in memory
B. The interrupting source supplies the branch information to the processor through an interrupt vector
C. The branch address is obtained from a register in the processor
D. None of the above

gate1995 co&architecture interrupts normal

Answer

1.14.3 Interrupts: GATE1998_1.20 top http://gateoverflow.in/1657

Which of the following is true?

A. Unless enabled, a CPU will not be able to process interrupts.
B. Loop instructions cannot be interrupted till they complete.
C. A processor checks for interrupts before executing a new instruction.
D. Only level triggered interrupts are possible on microprocessors.

gate1998 co&architecture interrupts normal

Answer

1.14.4 Interrupts: GATE2002-1.9 top http://gateoverflow.in/813

A device employing INTR line for device interrupt puts the CALL instruction on the data bus while

A. $\overline{INTA}$ is active
B. HOLD is active
C. READY is inactive
D. None of the above

gate2002 co&architecture interrupts normal

Answer

1.14.5 Interrupts: GATE2005-69 top

http://gateoverflow.in/1392

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4μsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

A. 15
B. 25
C. 35
D. 45

gate2005 co&architecture interrupts

Answer

1.14.6 Interrupts: GATE2009-8, UGCNET-June2012-III-58 top

http://gateoverflow.in/1300

A CPU generally handles an interrupt by executing an interrupt service routine

A. As soon as an interrupt is raised.

B. By checking the interrupt register at the end of fetch cycle.

C. By checking the interrupt register after finishing the execution of the current instruction.

D. By checking the interrupt register at fixed time intervals.

gate2009 co&architecture interrupts normal ugcnetjune2012iii

Answer

Answers: Interrupts

1.14.1 Interrupts: GATE1987-1-viii top

http://gateoverflow.in/80274

Selected Answer

Answer should be D i.e branches off to ISR after completing current instruction.

CPU checks the status bit of interrupt at the completion of each current instruction running when there is a interrupt it service the interrupt using ISR.

http://gateoverflow.in/18581/isro2009-78

1 votes -- Gate Mission (3.7k points)

1.14.2 Interrupts: GATE1995_1.3 top

http://gateoverflow.in/2590

Selected Answer

Answer: B

A vectored interrupt is a processing technique in which the interrupting device directs the processor to the appropriate interrupt service routine. This is in contrast to a polled interrupt system, in which a single interrupt service routine must determine the source of the interrupt by checking all potential interrupt sources, a slow and relatively laborious process.

5 votes -- Rajarshi Sarkar (35k points)

1.14.3 Interrupts: GATE1998_1.20 top

http://gateoverflow.in/1657

Selected Answer

Ans is A.

Options B and D is obviously false.

A processor checks for the interrupt before FETCHING an instruction, So Option C is also false.

7 votes -- Hardi Shah (329 points)

1.14.4 Interrupts: GATE2002-1.9 top http://gateoverflow.in/813

Selected Answer

INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INR signal & activates INTA signal, so another request can't be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option.

6 votes -- Tejas Jaiswal (661 points)

1.14.5 Interrupts: GATE2005-69 top http://gateoverflow.in/1392

Selected Answer

In Programmed I/O, the CPU issues a command and waits for I/O operations to complete.

So here, CPU will wait for 1sec to transfer 10KB of data.

overhead in programmed I/O = 1 sec

In Interrupt mode , data is transferred word by word (here word size is 1 byte as mentioned in question "Data is transferred byte-wise").
So to transfer 1 byte of data overhead is 4×10^{-6} sec
Thus to transfer 10 KB of data overhead is= $4 \times 10^{-6} \times 10^{4}$ sec

Performance gain $= \frac{1}{4 \times 10^{-6} \times 10^{4}} = \frac{1}{4x10^{-2}} = 25$

Thus, (b) is correct answer.

25 votes -- ashwini anand (319 points)

1.14.6 Interrupts: GATE2009-8, UGCNET-June2012-III-58 top http://gateoverflow.in/1300

Selected Answer

It will be C.

After finishing the execution of each instruction the CPU reads the interrupt pins to recognize the interrupts.

INTR = 1 = Interrupt is present.(Service the Interrupt)

= 0 = Interrupt is not present.(Goto next Instruction fetch from user program)

7 votes -- Gate Keeda (19.1k points)

1.15 Io Handling(4) top

1.15.1 Io Handling: GATE1996_1.24 top http://gateoverflow.in/2728

For the daisy chain scheme of connecting I/O devices, which of the following statements is true?

A. It gives non-uniform priority to various devices
B. It gives uniform priority to all devices
C. It is only useful for connecting slow devices to a processor device

D. It requires a separate interrupt pin on the processor for each device

gate1996 co&architecture io-handling normal

Answer

1.15.2 Io Handling: GATE1996_25 top

http://gateoverflow.in/2777

A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

25. A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 lock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block size transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

Level 1 (Cache memory)		Level 1 (Cache memory)	
Access time = 50 nsec/byte		Access time = 200 nsec/byte	
Size	Hit ratio	Size	Hit ratio
8 Kbytes	0.80	4 Kbytes	0.98
16 Kbytes	0.90	16 Kbytes	0.99
64 Kbytes	0.95	64 Kbytes	0.995

Size	Hit ratio
250 M bytes	1.0

gate1996 co&architecture io-handling dma normal

Answer

1.15.3 Io Handling: GATE1997_2.4 top

http://gateoverflow.in/2230

The correct matching for the following pairs is:

(A) DMA I/O	(1) High speed RAM
(B) Cache	(2) Disk
(C) Interrupt I/O	(3) Printer
(D) Condition Code Register	(4) ALU

A. A-4 B-3 C-1 D-2

B. A-2 B-1 C-3 D-4

C. A-4 B-3 C-2 D-1

D. A-2 B-3 C-4 D-1

gate1997 co&architecture normal io-handling

Answer

1.15.4 Io Handling: GATE2008-64, ISRO2009-13 top

http://gateoverflow.in/487

Which of the following statements about synchronous and asynchronous I/O is NOT true?

A. An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O

B. In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O

C. A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O

D. In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

gate2008 operating-system io-handling normal isro2009

Answer

Answers: Io Handling

1.15.1 Io Handling: GATE1996_1.24 top http://gateoverflow.in/2728

Selected Answer

daisy chaining approach tell the processor i which order the interrupt should be handled by providing priority to the devices .

In daisy chaining method all the devices are connected in serial. The device with the highest priority is placed in the first position, followed by lower priority devices . interrupt pin is common to all

so answer is a

17 votes -- No Need (14.1k points)

1.15.2 Io Handling: GATE1996_25 top http://gateoverflow.in/2777

Selected Answer

30 us for initialisation and termination and 2 ms for data transfer

Cpu time is consumed only for initialisation and termination

% of cpu time consumed =30us/(30us+2ms)*100=1.5%

10 votes -- Pooja Palod (32.4k points)

1.15.3 Io Handling: GATE1997_2.4 top http://gateoverflow.in/2230

Selected Answer

Answer: B

7 votes -- Rajarshi Sarkar (35k points)

1.15.4 Io Handling: GATE2008-64, ISRO2009-13 top http://gateoverflow.in/487

Selected Answer

Answer is (B).

In synchronous I/O process performing I/O operation will be placed in blocked state till the I/O operation is completed. An ISR will be invoked after the completion of I/O operation and it will place process from block state to ready state.

In asynchronous I/O, Handler function will be registered while performing the I/O operation. The process will not be placed in the block state and process continues to execute the remaining instructions. when the I/O operation completed signal mechanism is used to notify the process that data is available.

24 votes -- gate_asp (755 points)

1.16 Machine Instructions(18) top

1.16.1 Machine Instructions: GATE 2016-2-10 top http://gateoverflow.in/39547

A processor has 40 distinct instruction and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is________.

gate2016-2 machine-instructions co&architecture easy numerical-answers

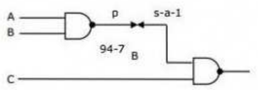
Answer

1.16.2 Machine Instructions: GATE1994_12 top http://gateoverflow.in/2508

a. Assume that a CPU has only two registers R_1 and R_2 and that only the following instruction is available $XOR\,R_i, R_j; \{R_j \leftarrow R_i \oplus R_j, \text{ for } i,j = 1,2\}$

   Using this XOR instruction, find an instruction sequence in order to exchange the contents of the registers R_1 and R_2

b. The line p of the circuit shown in figure has stuck at 1 fault. Determine an input test to detect the fault.



gate1994 co&architecture machine-instructions normal

Answer

1.16.3 Machine Instructions: GATE1999_17 top http://gateoverflow.in/1516

Consider the following program fragment in the assembly language of a certain hypothetical processor. The processor has three general purpose registers R1, R2 and R3. The meanings of the instructions are shown by comments (starting with ;) after the instructions.

```
X:  CMP R1, 0;  Compare R1 and 0, set flags appropriately in status register
    JZ  Z;   Jump if zero to target Z
    MOV R2, R1; Copy contents of R1 to R2
    SHR R1; Shift right R1 by 1 bit
    SHL R1; Shift left R1 by 1 bit
    CMP R2, R1; Compare R2 and R1 and set flag in status register
    JZ  Y;    Jump if zero to target Y
    INC R3; Increment R3 by 1;
Y:  SHR R1; Shift right R1 by 1 bit
    JMP X;  Jump to target X
Z:...
```

a. Initially R1, R2 and R3 contain the values 5, 0 and 0 respectively, what are the final values of R1 and R3 when control reaches Z?

b. In general, if R1, R2 and R3 initially contain the values n, 0, and 0 respectively. What is the final value of R3 when control reaches Z?

gate1999 co&architecture machine-instructions normal

Answer

1.16.4 Machine Instructions: GATE2003-48 top http://gateoverflow.in/938

Consider the following assembly language program for a hypothetical processor A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

	MOV B, #0	; $B \leftarrow 0$
	MOV C, #8	; $C \leftarrow 8$
Z:	CMP C, #0	; compare C with 0
	JZ X	; jump to X if zero flag is set
	SUB C, #1	; $C \leftarrow C - 1$
	RRC A, #1	; right rotate A through carry by one bit. Thus:
		; If the initial values of A and the carry flag are $a_7..a_0$ and
		; c_0 respectively, their values after the execution of this
		; instruction will be $c_0 a_7..a_1$ and a_0 respectively.
	JC Y	; jump to Y if carry flag is set
	JMP Z	; jump to Z
Y:	ADD B, #1	; $B \leftarrow B + 1$
	JMP Z	; jump to Z

X:

If the initial value of register A is A0 the value of register B after the program execution will be

A. the number of 0 bits in A_0
B. the number of 1 bits in A_0
C. A_0
D. 8

gate2003 co&architecture machine-instructions normal

Answer

1.16.5 Machine Instructions: GATE2003-49 top http://gateoverflow.in/43577

Consider the following assembly language program for a hypothetical processor A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

	MOV B, #0	;	$B \leftarrow 0$
	MOV C, #8	;	$C \leftarrow 8$
Z:	CMP C, #0	;	compare C with 0
	JZ X	;	jump to X if zero flag is set
	SUB C, #1	;	$C \leftarrow C - 1$
	RRC A, #1	;	right rotate A through carry by one bit. Thus:
		;	If the initial values of A and the carry flag are $a_7..a_0$ and
		;	c_0 respectively, their values after the execution of this
		;	instruction will be $c_0a_7..a_1$ and a_0 respectively.
	JC Y	;	jump to Y if carry flag is set
	JMP Z	;	jump to Z
Y:	ADD B, #1	;	$B \leftarrow B + 1$
	JMP Z	;	jump to Z
X:			

Which of the following instructions when inserted at location X will ensure that the value of the register A after program execution is as same as its initial value?

A. RRC A, #1
B. NOP ; no operation
C. LRC A, #1; left rotate A through carry flag by one bit
D. ADD A, #1

gate2003 co&architecture machine-instructions normal

Answer

1.16.6 Machine Instructions: GATE2004-63 top http://gateoverflow.in/1058

Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size (in words)
MOV R1, 5000	R1 ← Memory[5000]	2
MOV R2(R1)	R2 ← Memory[(R1)]	1
ADD R2, R3	R2 ← R2 + R3	1
MOV 6000, R2	Memory[6000] ← R2	2
HALT	Machine halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

A. 1007
B. 1020
C. 1024
D. 1028

gate2004 co&architecture machine-instructions normal

Answer

1.16.7 Machine Instructions: GATE2004-64 top http://gateoverflow.in/43570

Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size (in words)
MOV R1, 5000	R1 ← Memory[5000]	2
MOV R2(R1)	R2 ← Memory[(R1)]	1
ADD R2, R3	R2 ← R2 + R3	1
MOV 6000, R2	Memory[6000] ← R2	2
HALT	Machine halts	1

Let the clock cycles required for various operations be as follows:

Register to/from memory transfer	:	3 clock cycles
ADD with both operands in register	:	1 clock cycle
Instruction fetch and		2 clock cycles per

decode	:	word

The total number of clock cycles required to execute the program is

A. 29
B. 24
C. 23
D. 20

gate2004 co&architecture machine-instructions normal

Answer

1.16.8 Machine Instructions: GATE2004-IT-46 top http://gateoverflow.in/3689

If we use internal data forwarding to speed up the performance of a CPU (R1, R2 and R3 are registers and M[100] is a memory reference), then the sequence of operations

R1 → M[100]
M[100] → R2
M[100] → R3

can be replaced by

A. R1 → R3
R2 → M[100]
B. M[100] → R2
R1 → R2
R1 → R3
C. R1 → M[100]
R2 → R3
D. R1 → R2
R1 → R3
R1 → M[100]

gate2004-it co&architecture machine-instructions easy

Answer

1.16.9 Machine Instructions: GATE2006-09, ISRO2009-35 top http://gateoverflow.in/888

A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

A. 400
B. 500
C. 600
D. 700

gate2006 co&architecture machine-instructions easy isro2009

Answer

1.16.10 Machine Instructions: GATE2007-54 top http://gateoverflow.in/1252

In a simplified computer the instructions are:

OP R_j, R_i	-Performs R_j OP R_i and stores the result in register R_j.
OP m, R_i	-Performs val OP R_i and stores the result in register R_i. val denotes the content of the memory location m.
MOV m, R_i	-Moves the content of memory location m to

	register R_i
MOV R_i, m	-Moves the content of register R_i to memory location m

The computer has only two registers, and OP is either ADD or SUB. Consider the following basic block:

$t_1 = a + b$

$t_2 = c + d$

$t_3 = e - t_2$

$t_4 = t_1 - t_3$

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

A. 2
B. 3
C. 5
D. 6

gate2007 co&architecture machine-instructions normal

Answer

1.16.11 Machine Instructions: GATE2007-71 top http://gateoverflow.in/1269

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction size (no. of words)
	MOV R1,(3000)	R1 ← m[3000]	2
LOOP:	MOV R2,(R3)	R2 ← M[R3]	1
	ADD R2, R1	R2 ← R1 + R2	1
	MOV (R3), R2	M[R3] ← R2	1
	INC R3	R3 ← R3 +1	1
	DEC R1	R1 ← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

A. 10
B. 11
C. 20
D. 21

gate2007 co&architecture machine-instructions interrupts normal

Answer

1.16.12 Machine Instructions: GATE2007-72 top http://gateoverflow.in/43515

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction size (no. of words)

	MOV R1, (3000)	R1 ⟵ m[3000]	2
LOOP:	MOV R2, (R3)	R2 ⟵ M[R3]	1
	ADD R2, R1	R2 ⟵ R1 + R2	1
	MOV (R3), R2	M[R3] ⟵ R2	1
	INC R3	R3 ⟵ R3 +1	1
	DEC R1	R1 ⟵ R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

A. 100
B. 101
C. 102
D. 110

gate2007 co&architecture machine-instructions interrupts normal

Answer

1.16.13 Machine Instructions: GATE2007-73 top http://gateoverflow.in/43516

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction size (no. of words)
	MOV R1, (3000)	R1 ⟵ m[3000]	2
LOOP:	MOV R2, (R3)	R2 ⟵ M[R3]	1
	ADD R2, R1	R2 ⟵ R1 + R2	1
	MOV (R3), R2	M[R3] ⟵ R2	1
	INC R3	R3 ⟵ R3 +1	1
	DEC R1	R1 ⟵ R1 - 1	1
	BNZ LOOP	Branch on not zero	2

	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

A. 1005
B. 1020
C. 1024
D. 1040

gate2007 co&architecture machine-instructions interrupts normal

Answer

1.16.14 Machine Instructions: GATE2007-IT-41 top http://gateoverflow.in/3476

Following table indicates the latencies of operations between the instruction producing the result and instruction using the result.

Instruction producing the result	Instruction using the result	Latency
ALU Operation	ALU operation	2
ALU Operation	Store	2
Load	ALU Operation	1
Load	Store	0

Consider the following code segment.

```
Load R1, Loc 1;  Load R1 from memory location Loc1
Load R2, Loc 2;  Load R2 from memory location Loc 2
Add R1, R2, R1;  Add R1 and R2 and save result in R1
Dec R2;  Decrement R2
Dec R1;  Decrement R1
Mpy R1, R2, R3;  Multiply R1 and R2 and save result in R3
Store R3, Loc 3;  Store R3 in memory location Loc 3
```

What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

A. 7
B. 10
C. 13
D. 14

gate2007-it co&architecture machine-instructions normal

Answer

1.16.15 Machine Instructions: GATE2008-34 top http://gateoverflow.in/445

Which of the following must be true for the RFE (Return From Exception) instruction on a general purpose processor?

I. It must be a trap instruction

II. It must be a privileged instruction

III. An exception cannot be allowed to occur during execution of an RFE instruction

A. I only
B. II only
C. I and II only
D. I, II and III only

gate2008 co&architecture machine-instructions normal

Answer

1.16.16 Machine Instructions: GATE2008-IT-38 top http://gateoverflow.in/3348

Assume that EA = (X)+ is the effective address equal to the contents of location X, with X incremented by one word length after the effective address is calculated; EA = −(X) is the effective address equal to the contents of location X, with X decremented by one word length before the effective address is calculated; EA = (X)− is the effective address equal to the contents of location X, with X decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination ← source op destination). Using X as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

A. ADD (X)−, (X)
B. ADD (X), (X)−
C. ADD −(X), (X)+
D. ADD −(X), (X)

gate2008-it co&architecture machine-instructions normal

Answer

1.16.17 Machine Instructions: GATE2015-2_42 top http://gateoverflow.in/8215

Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the statring address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is $(5FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is

A. $(016A)_{16}$
B. $(016C)_{16}$
C. $(0170)_{16}$
D. $(0172)_{16}$

gate2015-2 co&architecture machine-instructions easy

Answer

1.16.18 Machine Instructions: ISI2011-CS-6a top http://gateoverflow.in/48179

Assume a machine has 4 registers (one of which is the accumulator A) and the following instruction set.

- $LOAD$ and $STORE$ are indirect memory operations that load and store, using the address stored in the given register operand. Thus, $LOAD\ R$ loads the contents of $memory[R]$ into A, and $STORE\ R$ stores the contents of A in $memory[R]$.
- MOV copies any register into any other register.
- ADD and SUB operate on the accumulator and one other register, such that $A = A\ op\ R$.
- LDC stores a given 7-bit constant in the accumulator.
- BRA, BZ, and BNE are branch instructions, each taking a 5-bit offset.

Design an instruction encoding scheme that allows each of the above instructions (along with operands) to be encoded in 8 bits.

co&architecture descriptive isi2011 machine-instructions

Answer

Answers: Machine Instructions

1.16.1 Machine Instructions: GATE 2016-2-10 top http://gateoverflow.in/39547

Selected Answer

Instruction Opcode Size => $\log_2 40$ => 6

Register operand size = $\log_2 24$ =>5

Total bits available => 32

Bits required for opcode + two register operands => 6 + 2 * 5 => 16

Bits available for immediate operand => 32 - 16 = 16 !

16 votes -- Akash (43.8k points)

1.16.2 Machine Instructions: GATE1994_12 top http://gateoverflow.in/2508

Selected Answer

(a)
$R2 \Longleftarrow R1 \oplus R2$
$R1 \Longleftarrow R2 \oplus R1$
$R2 \Longleftarrow R1 \oplus R2$

(b) A=1, B=1, C=1 should give output as 1 but as p is struck at 1 fault the output comes out to be 0.

6 votes -- Rajarshi Sarkar (35k points)

1.16.3 Machine Instructions: GATE1999_17 top http://gateoverflow.in/1516

Selected Answer

SHR R1 (Lower bit is lost and upper bit becomes 0 and all other bits shift right by 1)
SHL R1 (Upper bit is lost and lower bit becomes 0 and all other bits shift left by 1)

These two operations change the value of R1 if its lower bit is 1. So, the given program checks the lowest bit of R1 in each iteration and if its 1 then only increment R3 and loop terminates when R1 becomes 0. Thus at end, R3 will have the count of the number of bits set to 1 in R1.

a. R1 = 0, R3 = 2 as 101 has two 1's

b. R3 = #1 in R1.

7 votes -- Arjun Suresh (294k points)

1.16.4 Machine Instructions: GATE2003-48 top http://gateoverflow.in/938

Selected Answer

B. The code is counting the number of 1 bits in A0. When a 1 is moved to carry, B is incremented.

10 votes -- Arjun Suresh (294k points)

1.16.5 Machine Instructions: GATE2003-49 top http://gateoverflow.in/43577

Selected Answer

49. A. RRC a, #1. As the 8 bit register is rotated via carry 8 times.

a7a6a5a4a3a2a1a0
c0a7a6a5a4a3a2a1, now a0 is the new carry. So, after next rotation,
a0c0a7a6a5a4a3a2

So, after 8 rotations,

a6a5a4a3a2a1a0c0 and carry is a7.

Now, one more rotation will restore the original value of A0.

10 votes -- Arjun Suresh (294k points)

1.16.6 Machine Instructions: GATE2004-63 top http://gateoverflow.in/1058

Selected Answer

option **D**

Word size is 32 bits (4 bytes). Interrupt occurs **after execution of HALT** instruction NOT **during**, So address of next instruction will be saved on to the stack which is 1028.

(We have 5 instructions starting from address 1000, each of size 2, 1, 1, 2, 1 totaling 7 words = 7 *4 =28 bytes).

1000+ 28 = 1028 ,

1028 is the starting address of NEXT Instruction .

After HALT instruction CPU enters a HALT state and if an interrupt happens the return address will be **that of the instruction after the HALT.**

References :

1. http://x86.renejeschke.de/html/file_module_x86_id_134.html [X86 Instructors Manual]
2. http://electronics.stackexchange.com/questions/277735/what-happens-if-the-interrupt-occurs-during-the-execution-of-halt-instruction

23 votes -- Vikrant Singh (13.4k points)

1.16.7 Machine Instructions: GATE2004-64 top http://gateoverflow.in/43570

Selected Answer

64. **B.** 24 cycles

Instruction	Size	Fetch and Decode + Execute
mov	2	2*2 + 3 = 7
mov	1	2*1 + 3 = 5
add	1	2*1 + 1 = 3
mov	2	2*2 + 3 = 7
halt	1	2*1 + 0 = 2
	Total	24 cycles

21 votes -- Vikrant Singh (13.4k points)

1.16.8 Machine Instructions: GATE2004-IT-46 top http://gateoverflow.in/3689

Selected Answer

Data forwarding means if CPU writes to a memory location and subsequently reads from the same memory location, the second instruction can fetch the value directly from the register used to do the write than waiting for the memory. So, this increases the performance.

Here, choices A, B and C doesn't really make any sense as the data was in R1 and it must be moved to R2, R3 and M[100]. So, (D) is the answer.

13 votes -- Arjun Suresh (294k points)

1.16.9 Machine Instructions: GATE2006-09, ISRO2009-35 top http://gateoverflow.in/888

Selected Answer

Option c. 24 bit = 3 bytes instructions. So PC will have multiples of 3 in it.

14 votes -- anshu (3.2k points)

1.16.10 Machine Instructions: GATE2007-54 top http://gateoverflow.in/1252

Selected Answer

MOV a, R_1

ADD b, R_1

MOV c, R_2

ADD d, R_2

SUB e, R_2

SUB R_1, R_2

MOV R_2, m

Total no. of MOV Instruction = 3

21 votes -- Gate Keeda (19.1k points)

1.16.11 Machine Instructions: GATE2007-71 top http://gateoverflow.in/1269

Selected Answer

Loop is executed 10 times and there are two memory reference in the loop (each MOV is loading 1 word, so 1 memory reference for each MOV inside the loop). So number of memory reference inside loop is 2 (MOV) * 10 (times iteration) * 1 (1 word access/ MOV) = 20 memory accesses.

One memory access is outside the loop for the first instruction

```
MOV R1, (3000)
```

So, totally $20 + 1 = 21$

14 votes -- Vicky Bajoria (4.9k points)

1.16.12 Machine Instructions: GATE2007-72 top http://gateoverflow.in/43515

Selected Answer

The loop is executed 10 times and it modifies the contents from memory location 2000-2009. Memory location 2010 is untouched - contains 100 as before.

14 votes -- Vicky Bajoria (4.9k points)

The loop runs 10 times.

When R1=10 , Memory[2000] = 110,

When R1=9 , Memory[2001] = 109,

When R1=8 , Memory[2002] = 108,

When R1=7 , Memory[2003] = 107,

When R1=6 , Memory[2004] = 106,

When R1=5 , Memory[2005] = 105,

When R1=4 , Memory[2006] = 104,

When R1=3 , Memory[2007] = 103,

When R1=2 , Memory[2008] = 102,

When R1=1 , Memory[2009] = 101,

When R1=0 break the loop, Memory[2010]= 100

10 votes -- Arnab Bhadra (5.3k points)

1.16.13 Machine Instructions: GATE2007-73 top http://gateoverflow.in/43516

Selected Answer

An interrupt is checked for after the execution of the current instruction and the contents of PC (address of next instruction to be executed) is pushed on to stack. Here, address of INC, R3 $= 1000 + (2 + 1 + 1 + 1) \times 32/8 = 1020$ and next instruction address $= 1020 + 4 = 1024$ which is pushed on to stack.
Ref: http://www.ece.utep.edu/courses/web3376/Notes_files/ee3376-interrupts_stack.pdf

11 votes -- Vicky Bajoria (4.9k points)

1.16.14 Machine Instructions: GATE2007-IT-41 top http://gateoverflow.in/3476

Selected Answer

In the given question there are 7 instructions each of which takes 1 clock cycle to complete. (Pipelining may be used)
If an instruction is in execution phase and any other instructions can't be in the execution phase. So, atleast 7 clock cycles will be taken.
Now, it is given that between two instructions latency or delay should be there based on their operation. Ex- 1st line of the table says that between two operations in which first is producing the result of an ALU operation and the 2nd is using the result there should be a delay of 2 clock cyles.

clock cycle :

Clock cycle	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
	I1	I2		I3	I4		I5			I6			I7

1) Load R1, Loc 1; Load R1 from memory location Loc1
Takes 1 clock cycle, simply loading R1 on loc1.

2) Load R2, Loc 2; Load R2 from memory location Loc2
Takes 1 clock cycle, simply loading r2 on loc2.

3) Add R1, R2, R1; Add R1 and R2 and save result in R1
R1=R1+R2;

Hence, this instruction is using the result of R1 and R2, i.e. result of Instruction 1 and Instruction 2.

As instruction 1 is load operation and instruction 3 is ALU operation. So, there should be a delay of 1 clock cycle between instruction 1 and instruction 3.Which is already there due to I2.
As instruction 2 is load operation and instruction 3 is ALU operation. So, there should be a delay of 1 clock cycle between instruction 2 and instruction 3.

4) Dec R2; Decrement R2
This instruction is dependent on instruction 2 and there should be a delay of one clock cycle between Instruction 2 and Instruction 4. As instruction 2 is load and 4 is ALU . Which is already there due to Instruction 3.

5) Dec R1 Decrement R1
This instruction is dependent on Instruction 3
As Instruction I3 is ALU and I5 is also ALU so a delay of 2 clock cycles should be there between them of which 1 clock cycle delay is already there due to I4 so one clock cycle delay between I4 and I5.

6) MPY R1, R2, R3; Multiply R1 and R2 and save result in R3
R3=R1*R2;
This instruction uses the result of Instruction 5, as both instruction 5 and 6 are ALU so there should be a delay of 2 clock cycles.

7) Store R3, Loc 3 Store R3 in memory location Loc3
This instruction is dependent on instruction 6 which is ALU and instruction 7 is store so there should be a delay of 2 clock cycles between them.

Hence, a total of 13 clock cycles will be there.

15 votes -- Madhab Paul Choudhury (5.1k points)

Answer is (C)

Here each instruction takes 1 cycle but apart from that we have to consider latencies b/w instruction: If there are two ALU operations by I1 and I2 such that I2 uses the value produced by I1 in some register then I2 will be executed ONLY after waiting TWO more cycles after I1 has executed because latency b/w two ALU operations is 2

See here:

Clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Inst.	I1	I2	-	I3	I4	-	I5	-	-	I6	-	-	I7	

I3 is ALU operation which uses result of LOAD in I2 , so latency is of 1 cycle.

I5 is ALU operation using result of ALU in I3 therefore has to wait for 2 cycles after I3

I6 is ALU and uses result of ALU in I5 ,therefore waits 2 cycles

10 votes -- Sandeep_Uniyal (7.3k points)

1.16.15 Machine Instructions: GATE2008-34 top

http://gateoverflow.in/445

Selected Answer

RFE (Return From Exception) is a privileged trap instruction that is executed when exception occurs, so an exception is not allowed to execute. (D) is the correct option.

Ref: http://www.cs.rochester.edu/courses/252/spring2014/notes/08_exceptions

5 votes -- Vikrant Singh (13.4k points)

1.16.16 Machine Instructions: GATE2008-IT-38 top

http://gateoverflow.in/3348

Selected Answer

I think it should be A as 998<-1000+998.(i am writing only memory locations for sake of brevity). Lets say sp is 1000 initially then after it calculates the EA of source(which is 1000 as it decrements after the EA) the destination becomes 998 and that is where we want to store the result as stack is decrementing...in case of C and D it becomes 998<-998+998

12 votes -- Shaun Patel (6.9k points)

1.16.17 Machine Instructions: GATE2015-2_42 top

http://gateoverflow.in/8215

Selected Answer

first we have to consider here memory is byte-addressable

The CALL instruction is implemented as follows:

- Store the current value of PC in the stack

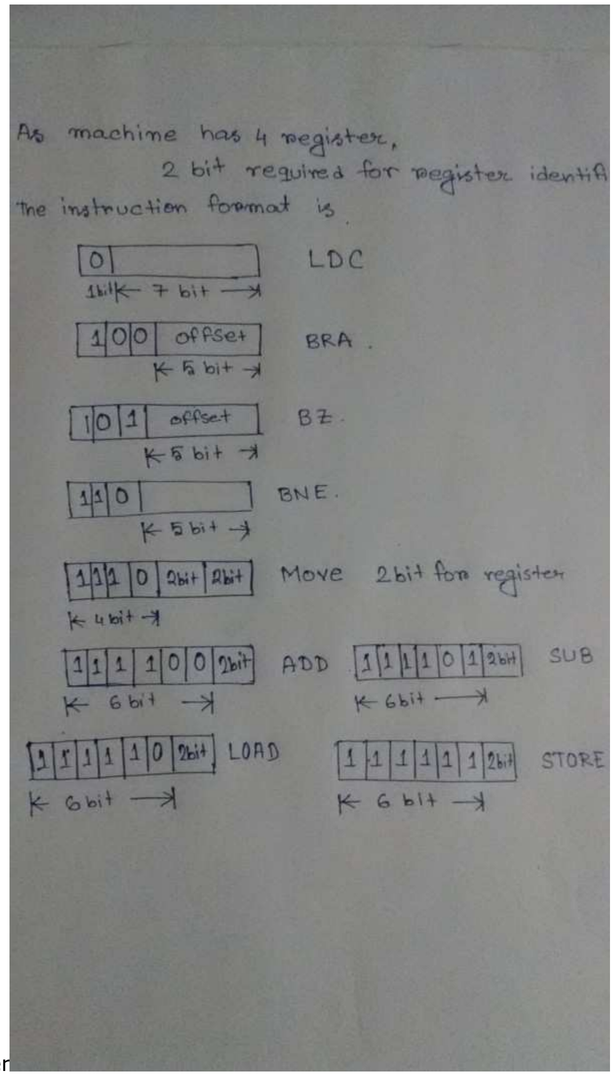
  pc is 2 byte it means when we store pc in stack it will increase by 2
  so current value of SP is $(016E)16 + 2$

- Store the value of PSW register in the stack
  psw is 2 byte it means when we store psw in stack it will increase by 2
  so current value of SP is $(016E)16 + 2 + 2 = (0172)_{16}$

32 votes -- Anoop Sonkar (4.9k points)

1.16.18 Machine Instructions: ISI2011-CS-6a top

http://gateoverflow.in/48179



This is answer

2 votes -- Arnab Bhadra (5.3k points)

1.17 Memory Interfacing(1) top

1.17.1 Memory Interfacing: GATE2016-1-09 top http://gateoverflow.in/39632

A processor can support a maximum memory of $4GB$, where the memory is word-addressable (a word consists of two bytes). The size of address bus of the processor is at least __________bits.

gate2016-1 co&architecture easy numerical-answers memory-interfacing

Answer

Answers: Memory Interfacing

1.17.1 Memory Interfacing: GATE2016-1-09 top http://gateoverflow.in/39632

Selected Answer

Size of Memory = No of words (Addresses) $\times$ No of bits per word

$2^{32}B =$ No of words (Addresses) $\times 2B$

No of words (Addresses) $= 2^{31}$

Number of Address lines = 31

25 votes -- Praveen Saini (53.6k points)

Max memory = 4 GB = 2^{32} Bytes since 1 word=2B.. total number of words=$2^{32}/2=2^{31}$ .. so to address these words we need minimum 31 bit address bus

12 votes -- Abhilash Panicker (8.8k points)

1.18 Microprogramming(11) top

1.18.1 Microprogramming: GATE1996_2.25 top http://gateoverflow.in/2754

A micro program control unit is required to generate a total of 25 control signals. Assume that during any microinstruction, at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be

A. 2
B. 2.5
C. 10
D. 12

gate1996 co&architecture microprogramming normal

Answer

1.18.2 Microprogramming: GATE1997_5.3 top http://gateoverflow.in/2254

A micro instruction is to be designed to specify

a. none or one of the three micro operations of one kind and

b. none or upto six micro operations of another kind

The minimum number of bits in the micro-instruction is

A. 9
B. 5
C. 8
D. None of the above

gate1997 co&architecture microprogramming normal

Answer

1.18.3 Microprogramming: GATE1999_2.19 top http://gateoverflow.in/1497

Arrange the following configuration for CPU in decreasing order of operating speeds:

Hard wired control, Vertical microprogramming, Horizontal microprogramming.

A. Hard wired control, Vertical microprogramming, Horizontal microprogramming.

B. Hard wired control, Horizontal microprogramming, Vertical microprogramming.

C. Horizontal microprogramming, Vertical microprogramming, Hard wired control.

D. Vertical microprogramming, Horizontal microprogramming, Hard wired control.

gate1999 co&architecture microprogramming normal

Answer

1.18.4 Microprogramming: GATE2002-2.7 top http://gateoverflow.in/837

Horizontal microprogramming

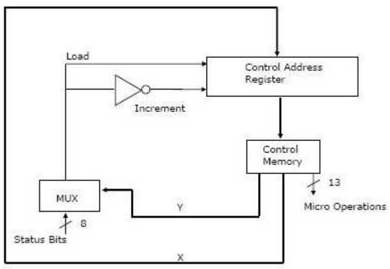
A. does not require use of signal decoders
B. results in larger sized microinstructions than vertical microprogramming
C. uses one bit for each control signal
D. all of the above

gate2002 co&architecture microprogramming

Answer

1.18.5 Microprogramming: GATE2004-67 top http://gateoverflow.in/1061

The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the input of the MUX.



How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

A. 10, 3, 1024
B. 8, 5, 256
C. 5, 8, 2048
D. 10, 3, 512

gate2004 co&architecture microprogramming normal

Answer

1.18.6 Microprogramming: GATE2004-IT-49 top http://gateoverflow.in/3692

A CPU has only three instructions I1, I2 and I3, which use the following signals in time steps T1-T5:

I1 : T1 : Ain, Bout, Cin
T2 : PCout, Bin
T3 : Zout, Ain
T4 : Bin, Cout
T5 : End

I2 : T1 : Cin, Bout, Din
T2 : Aout, Bin
T3 : Zout, Ain
T4 : Bin, Cout
T5 : End

I3 : T1 : Din, Aout
T2 : Ain, Bout
T3 : Zout, Ain
T4 : Dout, Ain
T5 : End

Which of the following logic functions will generate the hardwired control for the signal Ain ?

A. T1.I1 + T2.I3 + T4.I3 + T3
B. (T1 + T2 + T3).I3 + T1.I1

C. (T1 + T2).I1 + (T2 + T4).I3 + T3
D. (T1 + T2).I2 + (T1 + T3).I1 + T3

gate2004-it co&architecture microprogramming normal

Answer

1.18.7 Microprogramming: GATE2005-IT-45 top

http://gateoverflow.in/3806

A hardwired CPU uses 10 control signals S_1 to S_{10}, in various time steps T_1 to T_5, to implement 4 instructions I_1 to I_4 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S_5 and S_{10} respectively?

($(I_j + I_k)T_n$ indicates that the control signal should be generated in time step T_n if the instruction being executed is I_j or l_k)

A. $S_5 = T_1 + I_2 \cdot T_3$ and

$S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

B. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and

$S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

C. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and

$S_{10} = (I_2 + I_3 + I_4) \cdot T_2 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

D. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and

$S_{10} = (I_2 + I_3) \cdot T_2 + I_4 \cdot T_3 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

gate2005-it co&architecture microprogramming normal

Answer

1.18.8 Microprogramming: GATE2005-IT-49 top

http://gateoverflow.in/3810

An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

A. 0
B. 103
C. 22
D. 55

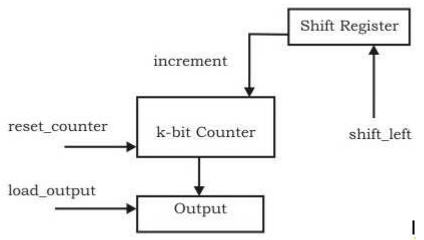
gate2005-it co&architecture microprogramming normal

Answer

1.18.9 Microprogramming: GATE2006-IT-41 top

http://gateoverflow.in/3584

The data path shown in the figure computes the number of 1s in the 32-bit input word corresponding to an unsigned even integer stored in the shift register.
The unsigned counter, initially zero, is incremented if the most significant bit of the shift register is 1.



The microprogram for the control is shown in the table below with missing control words for microinstructions $I_1, I_2, \ldots\ldots I_n$.

Microinstruction	reset_counter	shift_left	load_output
BEGIN	1	0	0
I_1	?	?	?
:	:		:
I_n	?	?	?
END	0	0	1

The counter width (k), the number of missing microinstructions (n), and the control word for microinstructions $I_1, I_2, \ldots\ldots I_n$ are, respectively,

A. 32, 5, 010
B. 5, 32, 010
C. 5, 31, 011
D. 5, 31, 010

gate2006-it co&architecture microprogramming normal

Answer

1.18.10 Microprogramming: GATE2008-IT-39 top http://gateoverflow.in/3349

Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

A. 125, 7
B. 125, 10
C. 135, 9
D. 135, 10

gate2008-it co&architecture microprogramming normal

Answer

1.18.11 Microprogramming: GATE2013_28 top http://gateoverflow.in/1539

Consider the following sequence of micro-operations.

```
MBR ← PC  MAR ← X  PC ← Y  Memory ← MBR
```

Which one of the following is a possible operation performed by this sequence?

(A) Instruction fetch

(B) Operand fetch

(C) Conditional branch

(D) Initiation of interrupt service

gate2013 co&architecture microprogramming normal

Answer

Answers: Microprogramming

1.18.1 Microprogramming: GATE1996_2.25 top http://gateoverflow.in/2754

Selected Answer

To generate 25 different control signals 5 bits are required....at any time atmost 2 signals are active..so control word length=5+5=10 bits

8 votes -- aravind90 (589 points)

1.18.2 Microprogramming: GATE1997_5.3 top http://gateoverflow.in/2254

Selected Answer

Actually the given question incorporates the concept of horizontal µprogramming (also known as decoded form of control signals) and vertical µprogramming(also known as encoded form of control signals)..

The a) part says :

none or one of the three micro operations of one kind

This is referred to encoding form of vertical one since at most one signal can be active in vertical microprogramming since it involves use of external decoder to select one control signal out of the given control signals..

As we know no of bits required for vertical microprogramming given n number of control signals = ceil ($\log_2 n$)

Here n = 3

So no of bits required for a) part = ceil($\log_2 3$)

= 2

Now coming to b) part , it says :

none or upto six micro operations of another kind

So it says at maximum we can have at most 6 microoperations of another kind at a time..To accomodate that we need decoded form of control signals which is horizontal signals..

So no of bits required for b) part = No of control signals of b) kind = 6

Therefore ,

Overall bits required to accomodate both a) and b) = 2 + 6

= 8 bits

Besides this , address field , flags etc are also there in a control word..That is why it is asked in the question :

minimum number of bits in the micro-instruction required

Hence minimum no of bits required = 8 bits

Hence C) is the correct answer..

14 votes -- HABIB MOHAMMAD KHAN (76.8k points)

1.18.3 Microprogramming: GATE1999_2.19 top http://gateoverflow.in/1497

Selected Answer

Hard wired control involves only hardware, whereas microprogramming is software approach. So, hardwire control should be faster than both microprogramming approaches.

Between vertical and horizontal microprogramming. Horizontal is faster because in this control signals are not encoded whereas in vertical microprogramming to save memory signals are encoded. So, it takes less time in horizontal microprogramming because decoding of signals is not required. Therefore, final order is :

hard wired control > horizontal microprogramming > vertical microprogramming

9 votes -- Shikhar Vashishth (5.7k points)

1.18.4 Microprogramming: GATE2002-2.7 top http://gateoverflow.in/837

Selected Answer

option (d). All statements are true.

Ref: http://www.cs.virginia.edu/~cs333/notes/microprogramming.pdf

15 votes -- Suvojit Mondal (431 points)

1.18.5 Microprogramming: GATE2004-67 top http://gateoverflow.in/1061

Selected Answer

$x + y + 13 = 26 \rightarrow (1)$
$y = 3$ // y is no of bits used to represent 8 different states of multiplexer$\rightarrow (2)$
x is no of bits required represent size of control memory
$x = 10$ from (1) and (2)

size of control memory $= 2^x = 2^{10} = 1024$

17 votes -- Digvijay (47k points)

1.18.6 Microprogramming: GATE2004-IT-49 top http://gateoverflow.in/3692

Selected Answer

We just have to see which all options give 1 whenever A_{in} is 1 and 0 otherwise.

So, Ain is 1 in T3 of I1, I2 and I3. Also during T1 of I1, and T2 and T4 of I3. So, answer will be

T1.I1 + T2.I3 + T4.I3 + T3.I1 + T3.I2 + T3.I3

Since CPU is having only 3 instructions, T3.I1 + T3.I2 + T3.I3 can be replaced with T3 (we don't need to see which instruction and A_{in} will be activated in time step 3 of all the instructions).

So, T1.I1 + T2.I3 + T4.I3 + T3

is the answer. Option A.

14 votes -- Arjun Suresh (294k points)

1.18.7 Microprogramming: GATE2005-IT-45 top http://gateoverflow.in/3806

Selected Answer

4. is the option for this question.
If we look at the table, we need to find those time-stamps and instructions which are using these control signals.

For example, $S_5 = T_1$ has used control signal S_5 for all the instructions, or we can say irrespective of the instructions. Also, S_5 is used by instructions I_2 and I_4 for the time stamp T_3 so that comes to:

$$S_5 = T_1 + I_2 \cdot T_3 + I_4 \cdot T_3 = T_1 + (I_2 + I_3) \cdot T_3$$

In the same way, we'll calculate for S_{10}.
It's an example of Hardwired CU Programming used in RISC processors. It gives accurate result, but isn't good for

debugging since minor change will cause to restructure the control unit.

14 votes -- Manu Thakur (6k points)

1.18.8 Microprogramming: GATE2005-IT-49 top http://gateoverflow.in/3810

Selected Answer

In horizontal microprogramming we need 1 bit for every control word, therefore total bits in

Horizontal Microprogramming=20+70+2+10+23=125

Now lets consider vertical microprogramming, In vertical microprogramming we use Decoder (n to 2^n) and output lines are equal to number of control words . A input is given according to what control word we have to select.

Now in this question these 5 groups contains mutually exclusive signals, i.e, they can be activated one at a time for a given group, we can safely use decoder.

group 1= $\lceil \log_2 20 \rceil$=5 (Number of input bits for decoder, given output is number of control word in given group)

group 2= $\lceil \log_2 70 \rceil$ =7

group 3= $\lceil \log_2 2 \rceil$ =1

group 4= $\lceil \log_2 10 \rceil$ =4

group 5= $\lceil og_2 23 \rceil$=5

Total bits required in vertical microprogramming= 5+7+1+4+5=22

So number of control words saved= 125-22=103 hence (B) is answer

23 votes -- Prateeksha Keshari (2.1k points)

1.18.9 Microprogramming: GATE2006-IT-41 top http://gateoverflow.in/3584

Selected Answer

Answer should be **D.**

Here **i1 to in** are microinstructions and reset_counter, shift_left and load_output are control singals to activate corresponding hardware(eg. Shift register or load output).

Counter width (k) is 5 bits as shift regiter uses 32 bit data Only.

Number of missing microinstructions (n) should be 31 as shift register contain Only unsigned EVEN integer. LSB Will be always 0 so no need to shift for LSB.

Control word contains:-

1 for active/enable. 0 for inactive or disable.

Reset counter is to reset the counter so it must be 0 for all microins.

Shift_left CS should be 1 to shift the given data in shift reg.

And load output has no meaning to make **output** active for all micro instructions as it will be used in the END only so it should be 0.

5 votes -- khush tak (6.8k points)

1.18.10 Microprogramming: GATE2008-IT-39 top http://gateoverflow.in/3349

Selected Answer

Its ans shuld be D becoz 140 instruction each requiring 7 cycles means...980 cycles which will take 10 bits since its horizontal so for control word = 125 control signals + 10 bits =135 bits will be required

8 votes -- nagendra2016 (171 points)

1.18.11 Microprogramming: GATE2013_28 top http://gateoverflow.in/1539

Selected Answer

Here PC value is being stored in memory. which is done when either CALL RETURN involved or there is Interrupt. As, we will have to come back to execute current instruction.

so, option (A), (B) are clearly incorrect

option (C) is incorrect coz conditional branch does not require to save PC contents.

option (D) is correct as it matches the generic Interrupt Cycle :

Interrupt Cycle:

t1: MBR ← (PC)
t2: MAR ← save-address
PC ← routine-address
t3: memory ← (MBR)

11 votes -- Himanshu Agarwal (16.2k points)

1.19 Page Fault(1) top

1.19.1 Page Fault: GATE1998-2.18, UGCNET-June2012-III-48 top http://gateoverflow.in/1691

If an instruction takes i microseconds and a page fault takes an additional j microseconds, the effective instruction time if on the average a page fault occurs every k instruction is:

A. $i + \frac{j}{k}$

B. $i + j^* k$

C. $\frac{i+j}{k}$

D. $(i + j)^* k$

gate1998 co&architecture page-fault easy ugcnetjune2012iii

Answer

Answers: Page Fault

1.19.1 Page Fault: GATE1998-2.18, UGCNET-June2012-III-48 top http://gateoverflow.in/1691

Selected Answer

page fault rate=1/k

page hit rate=1-1/k

service time=i

page fault service time=i+j

now effective memory access time=1/k*(i+j)+(1-1/k)*i=(i+j)/k+i-i/k=i/k+j/k+i-i/k=i+j/k

so option A is correct..

11 votes -- shashi shekhar (515 points)

1.20 Pipelining(34) top

1.20.1 Pipelining: GATE 2016-1-32 top

http://gateoverflow.in/39691

The stage delays in a 4-stage pipeline are $800, 500, 400$ and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionality equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is ____________ percent.

gate2016-1 co&architecture pipelining normal numerical-answers

Answer

1.20.2 Pipelining: GATE 2016-2-33 top

http://gateoverflow.in/39580

Consider a 3 GHz (gigahertz) processor with a three stage pipeline and stage latencies τ_1, τ_2 and τ_3 such that $\tau_1 = \frac{3\tau_2}{4} = 2\tau_3$. If the longest pipeline stage is split into two pipeline stages of equal latency , the new frequency is ___________ GHz, ignoring delays in the pipeline registers.

gate2016-2 co&architecture pipelining normal numerical-answers

Answer

1.20.3 Pipelining: GATE1999_13 top

http://gateoverflow.in/1512

An instruction pipeline consists of 4 stages – Fetch (F), Decode field (D), Execute (E) and Result Write (W). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below

	No. of cycles needed for			
Instruction	**F**	**D**	**E**	**W**
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Find the number of clock cycles needed to perform the 5 instructions.

gate1999 co&architecture pipelining normal

Answer

1.20.4 Pipelining: GATE2000-1.8 top

http://gateoverflow.in/631

Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on a non-pipelined but identical CPU, we can say that

A. T1 ≤ T2
B. T1 ≥ T2
C. T1 < T2
D. T1 and T2 plus the time taken for one instruction fetch cycle

gate2000 pipelining co&architecture easy

Answer

1.20.5 Pipelining: GATE2000-12 top http://gateoverflow.in/683

An instruction pipeline has five stages where each stage take 2 nanoseconds and all instruction use all five stages. Branch instructions are not overlapped. i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,

a. Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instruction. Ignore the fact that some branch instructions may be conditional.
b. If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.

gate2000 co&architecture pipelining normal descriptive

Answer

1.20.6 Pipelining: GATE2001-12 top http://gateoverflow.in/753

Consider a 5-stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence:

I1: sub r2, r3, r4; /* $r2 \leftarrow r3 - r4$ */
I2: sub r4, r2, r3; /* $r4 \leftarrow r2 - r3$ */
I3: sw r2, 100(r1) /* $M[r1 + 100] \leftarrow r2$ */
I4: sub r3, r4, r2 /* $r3 \leftarrow r4 - r2$ */

a. Show all data dependencies between the four instructions.
b. Identify the data hazards.
c. Can all hazards be avoided by forwarding in this case.

gate2001 co&architecture pipelining normal descriptive

Answer

1.20.7 Pipelining: GATE2002-2.6, ISRO2008-19 top http://gateoverflow.in/836

The performance of a pipelined processor suffers if

A. the pipeline stages have different delays
B. consecutive instructions are dependent on each other
C. the pipeline stages share hardware resources
D. All of the above

gate2002 co&architecture pipelining easy isro2008

Answer

1.20.8 Pipelining: GATE2003-10 top http://gateoverflow.in/901

For a pipelined CPU with a single ALU, consider the following situations

I. The j+1 –st instruction uses the result of the j-th instruction as an operand
II. The execution of a conditional jump instruction
III. The j-th and j+1st instructions require the ALU at the same time.

Which of the above can cause a hazard

A. I and II only
B. II and III only
C. III only
D. All the three

gate2003 co&architecture pipelining normal

Answer

1.20.9 Pipelining: GATE2004-69 top

http://gateoverflow.in/1063

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

A. 120.4 microseconds

B. 160.5 microseconds

C. 165.5 microseconds

D. 590.0 microseconds

gate2004 co&architecture pipelining normal

Answer

1.20.10 Pipelining: GATE2004-IT-47 top

http://gateoverflow.in/3690

Consider a pipeline processor with 4 stages S1 to S4. We want to execute the following loop:

```
for (i = 1; i < = 1000; i++)
    {I1, I2, I3, I4}
```

where the time taken (in ns) by instructions I1 to I4 for stages S1 to S4 are given below:

	S1	S2	S3	S4
I1:	1	2	1	2
I2:	2	1	2	1
I3:	1	1	2	1
I4:	2	1	2	1

The output of I1 for i = 2 will be available after

A. 11 ns
B. 12 ns
C. 13 ns
D. 28 ns

gate2004-it co&architecture pipelining normal

Answer

1.20.11 Pipelining: GATE2005-68 top

http://gateoverflow.in/1391

A 5 stage pipelined CPU has the following sequence of stages:

- IF – instruction fetch from instruction memory
- RD – Instruction decode and register read
- EX – Execute: ALU operation for data and address computation
- MA – Data memory access – for write access, the register read at RD state is used.
- WB – Register write back

Consider the following sequence of instructions:

- I_1: L R0, loc 1; R0 <= M[loc1]
- I_2: A R0, R0; R0 <= R0 +R0
- I_3: S R2, R0; R2 <= R2-R0

Let each stage take one clock cycle

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I_1?

A. 8
B. 10
C. 12
D. 15

gate2005 co&architecture pipelining normal

Answer

1.20.12 Pipelining: GATE2005-IT-44 top http://gateoverflow.in/3805

We have two designs D1 and D2 for a synchronous pipeline processor. D1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D2 has 8 pipeline stages each with 2 nsec execution time How much time can be saved using design D2 over design D1 for executing 100 instructions?

A. 214 nsec
B. 202 nsec
C. 86 nsec
D. -200 nsec

gate2005-it co&architecture pipelining normal

Answer

1.20.13 Pipelining: GATE2006-42 top http://gateoverflow.in/1818

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

A. 1.0 second
B. 1.2 seconds
C. 1.4 seconds
D. 1.6 seconds

gate2006 co&architecture pipelining normal

Answer

1.20.14 Pipelining: GATE2006-IT-78 top http://gateoverflow.in/3622

A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement X = (S - R * (P + Q))/T is given below. The values of variables P, Q, R, S and T are available in the registers R0, R1, R2, R3 and R4 respectively, before the execution of the instruction sequence.

```
ADD   R5, R0, R1  ; R5 ← R0 + R1
MUL   R6, R2, R5  ; R6 ← R2 * R5
SUB   R5, R3, R6  ; R5 ← R3 - R6
DIV   R6, R5, R4  ; R6 ← R5/R4
STORE R6, X       ; X  ← R6
```

The number of Read-After-Write (RAW) dependencies, Write-After-Read(WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,

A. 2, 2, 4
B. 3, 2, 3
C. 4, 2, 2
D. 3, 3, 2

gate2006-it co&architecture pipelining normal

Answer

1.20.15 Pipelining: GATE2006-IT-79 top http://gateoverflow.in/3623

A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement X = (S - R * (P + Q))/T is given below. The values of variables P, Q, R, S and T are available in the registers R0, R1, R2, R3 and R4 respectively, before the execution of the instruction sequence.

```
ADD    R5, R0, R1  ; R5 → R0 + R1
MUL    R6, R2, R5  ; R6 → R2 * R5
SUB    R5, R3, R6  ; R5 → R3 - R6
DIV    R6, R5, R4  ; R6 → R5/R4
STORE  R6, X       ; X  ← R6
```

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. The number of clock cycles required to complete the sequence of instructions is

A. 10
B. 12
C. 14
D. 16

gate2006-it co&architecture pipelining normal

Answer

1.20.16 Pipelining: GATE2007-37, ISRO2009-37 top http://gateoverflow.in/1235

Consider a pipelined processor with the following four stages:

- IF: Instruction Fetch
- ID: Instruction Decode and Operand Fetch
- EX: Execute
- WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2, R1, R0	R2 ⟵ R1 + R0
MUL	R4, R3, R2	R4 ⟵ R3 * R2
SUB	R6, R5, R4	R6 ⟵ R5 - R4

A. 7
B. 8
C. 10
D. 14

gate2007 co&architecture pipelining normal isro2009

Answer

1.20.17 Pipelining: GATE2007-IT-6, ISRO2011-25 top http://gateoverflow.in/3437

A processor takes 12 cycles to complete an instruction I. The corresponding pipelined processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

A. 1.83
B. 2
C. 3
D. 6

gate2007-it co&architecture pipelining normal isro2011

Answer

1.20.18 Pipelining: GATE2008-36 top

http://gateoverflow.in/447

Which of the following are NOT true in a pipelined processor?

I. Bypassing can handle all RAW hazards
II. Register renaming can eliminate all register carried WAR hazards
III. Control hazard penalties can be eliminated by dynamic branch prediction

A. I and II only
B. I and III only
C. II and III only
D. I, II and III

gate2008 pipelining co&architecture normal

Answer

1.20.19 Pipelining: GATE2008-76 top

http://gateoverflow.in/496

Delayed branching can help in the handling of control hazards

For all delayed conditional branch instructions, irrespective of whether the condition evaluates to true or false,

A. The instruction following the conditional branch instruction in memory is executed

B. The first instruction in the fall through path is executed

C. The first instruction in the taken path is executed

D. The branch takes longer to execute than any other instruction

gate2008 co&architecture pipelining normal

Answer

1.20.20 Pipelining: GATE2008-77 top

http://gateoverflow.in/43487

Delayed branching can help in the handling of control hazards

The following code is to run on a pipelined processor with one branch delay slot:

I1: ADD $R2 \leftarrow R7 + R8$

I2: Sub $R4 \leftarrow R5 – R6$

I3: ADD $R1 \leftarrow R2 + R3$

I4: STORE Memory $[R4] \leftarrow R1$

BRANCH to Label if $R1 == 0$

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any program modification?

A. I1
B. I2
C. I3
D. I4

gate2008 co&architecture pipelining normal

Answer

1.20.21 Pipelining: GATE2008-IT-40 top

http://gateoverflow.in/3350

A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is

A. 4.5
B. 4.0
C. 3.33
D. 3.0

gate2008-it co&architecture pipelining normal

Answer

1.20.22 Pipelining: GATE2009-28 top

http://gateoverflow.in/1314

Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?

For (i=1 to 2) {I1; I2; I3; I4;}

A. 16
B. 23
C. 28
D. 30

gate2009 co&architecture pipelining normal

Answer

1.20.23 Pipelining: GATE2010-33 top

http://gateoverflow.in/2207

A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Opearnd Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	**Meaning of instruction**
$t_0 : \mathrm{MUL}\ \mathrm{R}_2, \mathrm{R}_0, \mathrm{R}_1$	$\mathrm{R}_2 \leftarrow \mathrm{R}_0 * \mathrm{R}_1$
$t_1 : \mathrm{DIV}\ \mathrm{R}_5, \mathrm{R}_3, \mathrm{R}_4$	$\mathrm{R}_5 \leftarrow \mathrm{R}_3 / \mathrm{R}_4$
$t_2 : \mathrm{ADD}\ \mathrm{R}_2, \mathrm{R}_5, \mathrm{R}_2$	$\mathrm{R}_2 \leftarrow \mathrm{R}_5 + \mathrm{R}_2$
$t_3 : \mathrm{SUB}\ \mathrm{R}_5, \mathrm{R}_2, \mathrm{R}_6$	$\mathrm{R}_5 \leftarrow \mathrm{R}_2 - \mathrm{R}_6$

A. 13
B. 15
C. 17
D. 19

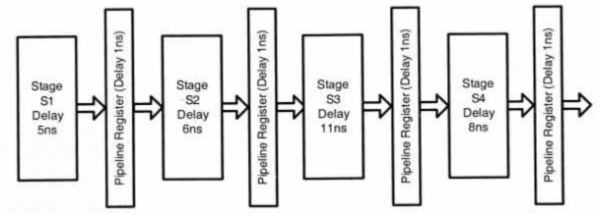
gate2010 co&architecture pipelining normal

Answer

1.20.24 Pipelining: GATE2011_41 top

http://gateoverflow.in/2143

Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure.



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

(A) 4.0

(B) 2.5

(C) 1.1

(D) 3.0

gate2011 co&architecture pipelining normal

Answer

1.20.25 Pipelining: GATE2012-20, ISRO2016-23 top http://gateoverflow.in/52

Register renaming is done in pipelined processors

A. as an alternative to register allocation at compile time
B. for efficient access to function parameters and local variables
C. to handle certain kinds of hazards
D. as part of address translation

gate2012 co&architecture pipelining easy isro2016

Answer

1.20.26 Pipelining: GATE2013_45 top http://gateoverflow.in/330

Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, …, I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

(A) 132 (B) 165 (C) 176 (D) 328

gate2013 normal co&architecture pipelining

Answer

1.20.27 Pipelining: GATE2014-1-43 top http://gateoverflow.in/1921

Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is ______________

gate2014-1 co&architecture pipelining numerical-answers normal

Answer

1.20.28 Pipelining: GATE2014-3-43 top http://gateoverflow.in/2077

An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the

ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is __________.

gate2014-3 co&architecture pipelining numerical-answers normal

Answer

1.20.29 Pipelining: GATE2014-3-9 top http://gateoverflow.in/2043

Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.

P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.

P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.

P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

A. P1
B. P2
C. P3
D. P4

gate2014-3 co&architecture pipelining normal

Answer

1.20.30 Pipelining: GATE2015-1-38 top http://gateoverflow.in/8288

Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is_______________.

gate2015-1 co&architecture pipelining normal numerical-answers

Answer

1.20.31 Pipelining: GATE2015-2_44 top http://gateoverflow.in/8218

Consider the sequence of machine instruction given below:

MUL	R5, R0, R1
DIV	R6, R2, R3
ADD	R7, R5, R6
SUB	R8, R7, R4

In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register shows the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instruction is _________.

gate2015-2 co&architecture pipelining normal numerical-answers

Answer

1.20.32 Pipelining: GATE2015-3_51 top http://gateoverflow.in/8560

Consider the following reservation table for a pipeline having three stages S_1, S_2 and S_3.

$Time \rightarrow$	1	2	3	4	5
S_1	X				X
S_2		X		X	
S_3			X		

The minimum average latency (MAL) is _______

gate2015-3 co&architecture pipelining difficult numerical-answers

Answer

1.20.33 Pipelining: GATE2017-1-50 top

http://gateoverflow.in/118719

Instruction execution in a processor is divided into 5 stages, *Instruction Fetch* (IF), *Instruction Decode* (ID), *Operand fetch* (OF), *Execute* (EX), and *Write Back* (WB). These stages take **5, 4, 20, 10** and **3 nanoseconds (ns)** respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of **2 ns**. Two pipelined implementation of the processor are contemplated:

(i) a naive pipeline implementation (NP) with 5 stages and

(ii) an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of**12 ns** and **8 ns** respectively.

The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is _________ .

gate2017-1 co&architecture pipelining normal numerical-answers

Answer

1.20.34 Pipelining: ISI2012-CS-2a top

http://gateoverflow.in/47848

A machine $\mathcal{M}$ has the following five pipeline stages; their respective time requirements in nanoseconds (ns) are given within parentheses:

- F-stage — instruction fetch (9 ns),
- D-stage — instruction decode and register fetch (3 ns),
- X-stage — execute/address calculation (7 ns),
- M-stage — memory access (9 ns),
- W-stage — write back to a register (2 ns).

Assume that for each stage, the pipeline overhead is 1 ns. A program P having 100 machine instructions runs on $\mathcal{M}$, where every 3rd instruction needs a 1-cycle stall before the X-stage. Calculate the CPU time in seconds for completing P.

descriptive isi2012 co&architecture pipelining

Answer

Answers: Pipelining

1.20.1 Pipelining: GATE 2016-1-32 top

http://gateoverflow.in/39691

Selected Answer

In pipeline ideally $CPI = 1$
So in 1 cycle 1 instruction gets completed
Throughout is instructions in unit time
In pipeline 1, cycle time=max stage delay $= 800psec$
In $800 * psec,$ we expect to finish 1 instuction
So, in 1s, $\frac{1}{800}$ instructions are expected to be completed, which is also the throughput for pipeline 1.

Similarly pipeline 2, throughput$= \frac{1}{600}$
Throughput increase in percentage
$= \frac{new-old}{old} * 100$
$= \frac{\frac{1}{600} - \frac{1}{800}}{\frac{1}{800}} * 100$

$= \frac{200}{600} * 100$
$= 33.33\%$

44 votes -- Anurag Semwal (8k points)

Maximum throughput of a Pipeline i.e in best case without any stalls is equal to Clock Frequency of the pipeline

In first case Clock cycle time = Max Stage Delay = Max(800,500,400 and 300) = 800. So clock Frequency = 1/800 (Ignore the units as we have to calculate percentage only)

In Second Case Clock cycle time = Max(600,350,500,400 and 300) = 600. So clock Frequency = 1/600.

Percentage increase in throughput of pipeline = percentage in Clock Frequency = (1/600 - 1/800)/1/800 = 33.33%

11 votes -- Mehak Sharma (1.5k points)

1.20.2 Pipelining: GATE 2016-2-33 top

http://gateoverflow.in/39580

Selected Answer

Answer is 4 GHz.

Given 3 stage pipeline , with 3 GHz processor.

Given , $e_1 = 3e_2 / 4 = 2e_3$

Put $e_1 = 6x$

we get, $e_2 = 8x$, $e_3 = 3x$

Now largest stage time is 8x.

So, frequency is
$\frac{1}{8x}$

=>
$\frac{1}{8x}$ = 3 GHz

=>
$\frac{1}{x}$ = 24 GHz ---------(1)

Now, we divide e_2 into two stages of 4x & 4x.

New processor has 4 stages -

6x , 4x, 4x, 3x.

Now largest stage time is 6x.

So, new frequency is

$\frac{1}{6x}$ =
$\frac{24}{6}$ = **4 GHz (Ans)**

------- from (1)

43 votes -- Himanshu Agarwal (16.2k points)

1.20.3 Pipelining: GATE1999_13 top

http://gateoverflow.in/1512

Selected Answer

answer = 15 cycles are required.

```
1|F D D E W
2|  F - D D E E W
3|      F F D - E E E W W
4|          F - D D D E E W
5|              F - - D D E W W
```

6 votes -- Amar Vashishth (28.7k points)

1.20.4 Pipelining: GATE2000-1.8 top

http://gateoverflow.in/631

Selected Answer

Here we are comparing the execution time of only a single instruction. Pipelining in no way increases the execution time of a single instruction (the time from its start to end). It increases the overall performance by splitting the execution to multiple pipeline stages so that the following instructions can use the finished stages of the previous instructions. But in doing so pipelining causes some problems also as given in the below link, which might slow some instructions. So, (B) is the answer.

http://www.cs.wvu.edu/~jdm/classes/cs455/notes/tech/instrpipe.html

22 votes -- Arjun Suresh (294k points)

1.20.5 Pipelining: GATE2000-12 top

http://gateoverflow.in/683

Selected Answer

Each stage is 2ns. So, after 5 time units each of 2ns, the first instruction finishes (i.e., after 10ns), in every 2ns after that a new instruction gets finished. This is assuming no branch instructions. Now, once the pipeline is full, we can assume that the initial fill time doesn't matter our calculations and average execution time for each instruction is 2ns assuming no branch instructions.

(a) Now, we are given that 20% of instructions are branch (like JMP) and when a branch instruction is executed, no further instruction enters the pipeline. So, we can assume every 5th instruction is a branch instruction. So, with this assumption, total time to finish 5 instruction will be 5 * 2 + 8 = 18 ns (as when a branch instruction enters the pipeline and before it finishes, 4 pipeline stages will be empty totaling 4 * 2 = 8 ns, as it is mentioned in question that the next instruction fetch starts only when branch instruction completes). And this is the same for every set of 5 instructions, and hence the average instruction execution time = 18/5 = 3.6 ns

(b) This is just a complex statement. But what we need is to identify the % of branch instructions which cause a branch to be taken as others will have no effect on the pipeline flow.
20% of branch instructions are branch instructions. 80% of branch instructions are conditional.
That means .2*.8 = 16% of instructions are conditional branch instructions and it is given that 50% of those result in a branch being taken.
So, 8% of instructions are conditional branches being taken and we also have 20% of 20% = 4% of unconditional branch instructions which are always taken.

So, percentage of instructions where a branch is taken is 8+4 = 12% instead of 20% in (a) part.

So, in 100 instructions there will be 12 branch instructions. We can do a different calculation here as compared to (a) as 12 is not a divisor of 100. Each branch instruction causes a pipeline delay of 4*2 = 8 ns. So, 12 instructions will cause a delay of 12 * 8 = 96 ns. For 100 instructions, we need 100 * 2 = 200 ns without any delay and with delay we require 200 + 96 = 296 ns for 100 instructions.

So, average instruction execution time = 296/100 = 2.96 ns

(We can also use this method for part (a) which will give 100 * 2 + 20*8 = 360 ns for 100 instructions)

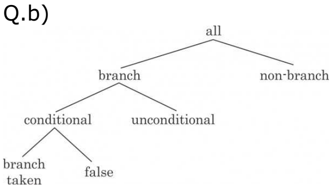
21 votes -- Arjun Suresh (294k points)

if an instruction branches then it takes $2ns \times 5 = 10ns$, coz if branch is taken then the instruction after that branch instruction is not fetched until entire current branch instruction is completed, this means it will go through all stages.

if an instruction is non-branch or branching does not happen then, it takes $2ns$ to get completed.

Q.a) $\text{average time taken} = 0.8 \times 2ns + 0.2 \times 10ns = 3.6ns$

Q.b)



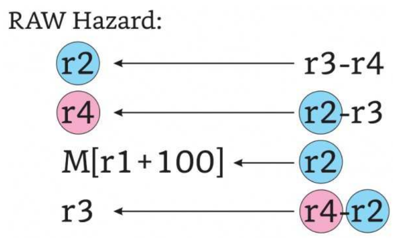
$\text{Average time taken} = 0.8 \times 2ns + 0.2$ $\Big($

17 votes -- Amar Vashishth (28.7k points)

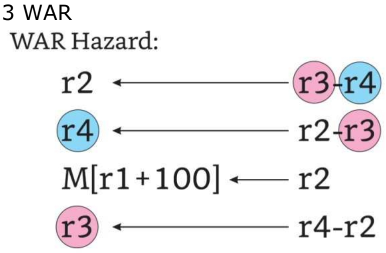
1.20.6 Pipelining: GATE2001-12 top http://gateoverflow.in/753

Selected Answer

4 RAW



3 WAR



With operand forwarding:

I_1	IF	ID	$^{3}_{4}$EX^{2}	M	WB			
I_2		IF	ID	$^{2}_{3}$EX^{4}	M	WB		
I_3			IF	ID	EX	^{2}M	WB	
I_4				IF	ID	$^{2}_{4}$EX^{3}	M	WB

R2 is forwarded R4 is forwarded

Without it:
(both tables represent the same pipeline)

for r2

①	IF	ID	EX	M	WB						
②		IF	IF	IF	ID	EX	M	WB			
③					IF	ID	EX	M	WB		
④						IF	IF	ID	EX	M	WB

for r4

WB					①			②	③		④
M				①			②	③		④	
EX			①			②	③		④		
ID		①			②	③		④			
IF	①	②	②	②	③	④	④				

13 votes -- Amar Vashishth (28.7k points)

1.20.7 Pipelining: GATE2002-2.6, ISRO2008-19 top http://gateoverflow.in/836

Selected Answer

Answer: D

A: Yes. Total delay = Max (All delays) + Register Delay.

B: Yes, if data forwarding is not there.

C: Yes, like ID and EX shares ID/EX register.

14 votes -- Rajarshi Sarkar (35k points)

1.20.8 Pipelining: GATE2003-10 top http://gateoverflow.in/901

Selected Answer

1. Data hazard
2. Control hazard
3. Structural hazard as only one ALU is there

So, D all of these.

http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/hazards.html

16 votes -- Arjun Suresh (294k points)

1.20.9 Pipelining: GATE2004-69 top http://gateoverflow.in/1063

Selected Answer

Pipelining requires all stages to be synchronized meaning, we have to make the delay of all stages equal to the maximum pipeline stage delay which here is 160.

Time for execution of the first instruction = (160+5) * 3 + 160 = 655 ns (5 ns for intermediate registers which is not needed for the final stage).

Now, in every 165 ns, an instruction can be completed. So, Total time for 1000 instructions = 655 + 999*165 = 165.49 microseconds

18 votes -- Arjun Suresh (294k points)

1.20.10 Pipelining: GATE2004-IT-47 top

http://gateoverflow.in/3690

Selected Answer

time	1	2	3	4	5	6	7	8	9	10	11	12	13
I1	s1	s2	s2	s3	s4	s4							
I2		s1	s1	s2	s3	s3	s4						
I3				s1	s2	-	s3	s3	s4				
I4					s1	s1	s2	-	s3	s3	s4		
I1							s1	-	s2	s2	s3	s4	s4

so total time would be=13 ns

so option (c).

correct me if i am wrong...

17 votes -- Suvojit Mondal (431 points)

1.20.11 Pipelining: GATE2005-68 top

http://gateoverflow.in/1391

Selected Answer

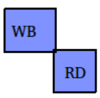
Answer here is option A

Without data forwarding:

13 clock - WB and RD state non overlapping .

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
IF	RD	EX	MA	WB								
	IF				RD	EX	MA	WB				
					IF				RD	EX	MA	WB

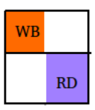
Here , WB and RD stage operate in Non- Overlaping mode .



11 clock - WB and RD state overlapping .

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11
IF	RD	EX	MA	WB						
	IF			RD	EX	MA	WB			
				IF			RD	EX	MA	WB

Split Phase access between WB and RD means :



WB stage produce the output during the rising edge of the clock and RD stage fetch the output during the falling edge.

In Question it is mentioned

for write access, the register read at RD state is used.

This means that for writing operands back to memory, register read at RD state is used (no operand forward for STORE instructions).

Note

- As in any question in any subject unless otherwise stated we always consider the best case. So, do overlap - unless otherwise stated. But this is for only WB/RD

1. **Why there is stall for I_2 in T_3 and T_4 ?**
 RD is instruction decode and register read . IF we execute RD of I2 in T3 . data from memory will not get stored to R0 hence proper operands are not available at T3 . Perhaps I2 has to wait untill I1 write values to memory
2. **WB of I1 and RD of I2 are operating in same clock why it is so ?**
If nothing has mentioned in question . This senario is taken into consideration by default . It is because after MA operands will be available in register so RD and WB could overlap .

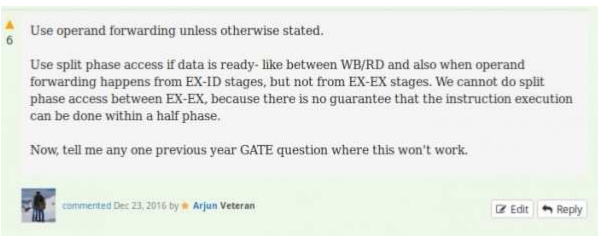
With data forwarding

(Should be the case here as question says no operand forwarding for memory register for STORE instructions)

8 clock cycles

1	2	3	4	5	6	7	8	9
IF	RD	EX	MA	WB				
	IF	RD		EX	MA	WB		
		IF		RD	EX	MM	WB	

1. **Why there is a stall I2 in T4 ?**
Data is being forwarded from MA of I1 EX of I2 .MA operation of I1 must complete so that correct data will be available in register .
2. **Why RD of I2 in T3 ? Will it not fetch incorrect information if executed before Operand are forwarded from MA of I1 ?**
 Yes. RD of I2 will definetly fetch INCORRECT data at T3 . But don't worry about it Operand Forwarding technique will take care of it .
3. **Why can't RD of I2 be placed in T4 ?**
Yes . We can place RD of I2 in T4 as well. But what is the fun in that ? pipeline is a technique used to reduce the execution time of instrcutions . Why do we need to make an extra stall ? Moreover there is one more problem which is discussed just below .After reading the below point Just think if we had created a stall at T3 !
4. **Why can't RD of I3 be placed at T4 ?**
This cannot be done . I3 cannot use RD because Previous instrction I2 should start next stage (EX) before current (I3) could utilise that(RD) stage . It is because data will be residing in buffers.
5. **Can an operand being forwarded from one clock cycle to same clock cycle ?**
 No . the previous clock cycle must complete before data being forwarded . Unless split phase technique is used
6. **Cant there be a forwarding from EX stage(T3) of I1 to EX stage(T4) of I2 ?**
This is not possible . See what is happening in I1 . It is Memory Read .So data will be available in register after memory read only .So data cannot be forwarded from EX of I1 .
7. **In some case data is forwarded from MA and some case data is forwarded from EX Why it is so ?**
Data is forwarded when it is ready . It solely depends on the type of instruction .
8. **When to use Split-Phase ?**


6

Use operand forwarding unless otherwise stated.

Use split phase access if data is ready- like between WB/RD and also when operand forwarding happens from EX-ID stages, but not from EX-EX stages. We cannot do split phase access between EX-EX, because there is no guarantee that the instruction execution can be done within a half phase.

Now, tell me any one previous year GATE question where this won't work.

commented Dec 23, 2016 by Arjun Veteran

Edit Reply

 [mostly when it is given in question that there is operand forwarding from A stage to B stage eg:http://gateoverflow.in/8218/gate2015-2_44]

Split-Phase can be used even when no Operand Forwarding beacause they aren't releated

References

- http://web.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html

Similar Question

- http://gateoverflow.in/8218/gate2015-2_44
- http://gateoverflow.in/2207/gate2010-33
- http://gateoverflow.in/34735/pipelining-without-operand-forwarding

Discussions

- http://gateoverflow.in/102565/operand-forwarding-in-pipeline
- http://gateoverflow.in/113244/doubts-in-pipelining

32 votes -- pC (21.4k points)

answer = **option A**

8 cycles required with operand forwarding.

With operand forwarding

```
I1 | IF RD EX MA WB
I2 |    IF RD -- EX MA WB
I3 |       IF -- RD EX MA WB
```

Without it

```
I1 | IF RD EX MA WB
I2 |    IF -- -- -- RD EX MA WB
I3 |                IF -- -- -- RD EX MA WB
```

it is not given that RD and WB stage could overlap.

Without it, but RD and WB overlaps.

```
I1 | IF RD EX MA WB
I2 |    IF -- -- RD EX MA WB
I3 |             IF -- -- RD EX MA WB
```

18 votes -- Amar Vashishth (28.7k points)

1.20.12 Pipelining: GATE2005-IT-44 top

http://gateoverflow.in/3805

Selected Answer

(B) is the correct option for this question.

Execution time for Pipeline = (K+n-1)*execution_time where k = no of stages in pipeline n = no of instructions
execution time = Max(all stages execution time)

D1 = (5+100-1)*4 = 416

D2 = (8+100-1)*2 = 214

Time saved using D2 = 416-214 =202

12 votes -- Manu Thakur (6k points)

1.20.13 Pipelining: GATE2006-42 top

http://gateoverflow.in/1818

Selected Answer

Delay slots in pipeline caused due to a branch instruction is 2 as after the 3rd stage of current instruction (during 4th stage) IF of next begins. Ideally this should be during 2nd stage.

So, for total no. of instructions = 10^9 and 20% branch, we have $0.2 \times 2 \times 10^9 = 4 \times 10^8$ cycle penalty.

Since, clock speed is 1GHz and each instruction on average takes 1 cycle, total execution time in seconds will be

$10^9/10^9 + 4 \times 10^8/10^9 = 1.4$

18 votes -- Arjun Suresh (294k points)

1.20.14 Pipelining: GATE2006-IT-78 top

http://gateoverflow.in/3622

Selected Answer

(C) is the correct option for this question:

RAW

1. I1 - I2 (R5)
2. I2 - I3 (R6)
3. I3 - I4 (R5)
4. I4 - I5 (R6)

WAR

1. I2 - I3 (R5)
2. I3 - I4 (R6)

WAW

1. I1 - I3 (R5)
2. I2 - I4 (R6)

16 votes -- Manu Thakur (6k points)

1.20.15 Pipelining: GATE2006-IT-79 top

http://gateoverflow.in/3623

Selected Answer

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
IF	ID	EX	WB								
	IF	ID	EX	EX	EX	WB					
		IF			ID	EX	WB				
					IF	ID	EX	EX	EX	WB	
						IF			ID	EX	WB

Stalls

EX
ID
Data is forwarded from Ex to ID state

This is what i have solved. so answer is 12

28 votes -- Manu Thakur (6k points)

answer = **option D** = 16 cycles are required

With Operand Forwarding:

ADD	IF	ID	EX	WB												
MUL		IF	—	ID	EX	EX	EX	WB								
SUB				IF	—	—	—	ID	EX	WB						
DIV								IF	—	ID	EX	EX	EX	WB		
STORE										IF	—	—	—	ID	EX	WB

14 votes -- Amar Vashishth (28.7k points)

1.20.16 Pipelining: GATE2007-37, ISRO2009-37 top http://gateoverflow.in/1235

Selected Answer

Answer: **option B**
considering EX to EX data forwarding.

	1	2	3	4	5	6	7	8
I1	IF	ID	EX	WB				
I2		IF	ID	EX	EX	EX	WB	
I3			IF	ID			EX	WB

18 votes -- Rajarshi Sarkar (35k points)

1.20.17 Pipelining: GATE2007-IT-6, ISRO2011-25 top http://gateoverflow.in/3437

Selected Answer

For non pipeline processor we have n instruction and each instruction take 12 cycle so total 12n instruction.

For pipeline processor we have each stage strict to 6ns so time to complete the n instruction is 6*6+ (n-1)*6

Lim $_{n\to\infty}$ 12n / 36 + (n-1)*6 = 12 / 6 =2

23 votes -- Arpit Dhuriya (3k points)

1.20.18 Pipelining: GATE2008-36 top http://gateoverflow.in/447

Selected Answer

(B) I and III

I - False Bypassing can't handle all RAW hazard, consider when any instruction depends on the result of LOAD instruction, now LOAD updates register value at Memory Access Stage (MA), so data will not be available directly on Execute stage.

II - True, register renaming can eliminate all WAR Hazard.

III- False, It cannot completely eliminate, though it can reduce Control Hazard Penalties

28 votes -- Prateeksha Keshari (2.1k points)

1.20.19 Pipelining: GATE2008-76 top http://gateoverflow.in/496

Selected Answer

76. Answer is A. In order to avoid the pipeline delay due to conditional branch instruction, a suitable instruction is placed below the conditional branch instruction such that the instruction will be executed irrespective of whether branch is taken or not and won't affect the program behaviour.

77. Answer is D) I4. The STORE instruction can be moved below the conditional branch instruction. Whether the branch is taken or not, STORE will be executed as the next instruction after conditional branch instruction, due to delayed branching.

Here, I3 is not the answer because the branch conditional variable R1 is dependent on it. Same for I1. Similarly, I4 has a dependency on I2 and hence I2 must be executed before I4.

23 votes -- Arjun Suresh (294k points)

1.20.20 Pipelining: GATE2008-77 top

http://gateoverflow.in/43487

Selected Answer

What is Delayed Branching ?
One way to maximize the use of the pipeline, is to find an instruction that can be safely exeucted whether the branch is taken or not, and execute that instruction. So, when a branch instruction is encountered, the hardware puts the instruction following the branch into the pipe and begins executing it, just as in predict-not-taken. However, unlike in predict-not-taken, we do not need to worry about whether the branch is taken or not, we do not need to clear the pipe because no matter whether the branch is taken or not, we know the instruction is safe to execute.
More Read : https://www.cs.umd.edu/class/fall2001/cmsc411/projects/branches/delay.html

Moving I_1 after branch

- I1 is updating the value of R2
- R2 which is used to determine branch condition R1
- Value of R2 is available after branch
  $\Rightarrow$ **Cannot be moved**

Moving I_3 after branch

- value of R1 is computed in this instruction
- R1 is the branch condition
  $\Rightarrow$ **Cannot be moved**

Moving I_4 after branch

- I4 is simple store instruction used to store R1 in memory
- program execution will have no effect if this is placed after conditional branch
  $\Rightarrow$ **Can be moved**

Moving I_2 after branch

- It update the memory location to place the storing of conditional branch instruction R1
- If moved after branch , when compiler reaches I4 program execution will stop
  $\Rightarrow$ **Canot be moved**
- However I_2 I_4 both can be moved after the branch instruction

Apt choice will be I_4

Hence **Option D**

13 votes -- pC (21.4k points)

1.20.21 Pipelining: GATE2008-IT-40 top

http://gateoverflow.in/3350

Selected Answer

Here we have to keep in mind the phrase :

> a non pipelined single cycle processor

This signifies that instruction in a non pipelined scenario is incurring only a single cycle to execute entire instruction..Hence no conept of stage comes in case of single cycle non pipelined system..

The cycle time can be calculated from clock frequency given in non pipelined system = 100 MHz

Therefore clock cycle time in non pipelined system = $1 / (100 * 10^6)$ s

= 10 ns

Now cycle time in pipelined system = max(stage delay + interface delay)

= 2.5 + 0.5

= 3 ns

Therefore ,

Speedup = $CPI_{non\ pipeline}$ * Cycle $time_{non\ pipeline}$ / ($CPI_{pipeline}$ * Cycle $time_{pipeline}$)

= 1 * 10 / (1 * 3)

= 3.33

[Since in case of non pipeline we have single cycle processor , so $CPI_{non\ pipeline}$ = 1 and $CPI_{pipeline}$ by default = 1]

Hence C) is the correct answer..

16 votes -- HABIB MOHAMMAD KHAN (76.8k points)

answer is C..

explanation:

for non pipeline system time required = 2.5 + 1.5 + 2.0 + 1.5 + 2.5 = 10

for pipelined system = max(stage delay) + max(latch delay) = 2.5 + 0.5 = 3

speedup = time in non pipelie / time in pipeline = 10/3 = 3.33

17 votes -- jayendra (8.1k points)

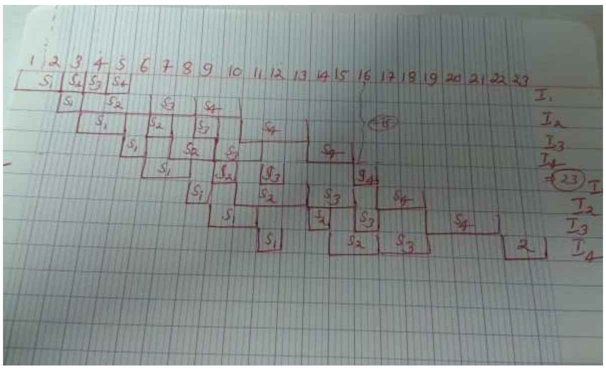
1.20.22 Pipelining: GATE2009-28 top

http://gateoverflow.in/1314

Selected Answer

Here bound of the loop are constants, therefore compiler will do the loop unrolling(If compiler won't then prefetcher will do) to increase the instruction level parallelism. And after loop unrolling 23 cycles are required for execution. Therefore correct answer would be (B).

PS: We assume the buffers between the pipeline stages can store multiple results in the form of a queue.



14 votes -- suraj (5.1k points)

this is the loop level level paralellism question but when we apply the loop level parallelism then we get 25 cycles so dis is not in option so we have to do it without loop level parallelism and the frst time loop output the result at 15 cc so total 30 cc for 2 iterations

13 votes -- Shreyans Dhankhar (2.6k points)

1.20.23 Pipelining: GATE2010-33 top

http://gateoverflow.in/2207

Selected Answer

t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15
IF	ID	OF	PO	PO	PO	WO								
	IF	ID	OF			PO	PO	PO	PO	PO	PO	WO		
		IF	ID			OF						PO	WO	
			IF			ID						OF	PO	WO

Operand forwarding allows an output to be passed for the next instruction. Here from the output of PO stage of DIV instruction operand is forwarded to the PO stage of ADD instruction and similarly between ADD and SUB instructions. Hence, 15cycles required.

http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html

22 votes -- Arjun Suresh (294k points)

1.20.24 Pipelining: GATE2011_41 top

http://gateoverflow.in/2143

Selected Answer

Answer is (**B) 2.5**

In pipeline system Time taken is determined by the max delay at any stage i.e., 11ns plus the delay incurred by pipeline stages i.e., 1ns = 12ns. In non-pipeline system Delay = 5ns + 6ns + 11ns + 8ns = 30ns.

$\therefore$ The speedup is $\frac{30}{12} = 2.5$ ns.

26 votes -- Sona Praneeth Akula (4k points)

1.20.25 Pipelining: GATE2012-20, ISRO2016-23 top

http://gateoverflow.in/52

Selected Answer

Register renaming is done to eliminate WAR (Write after Read) and WAW (Write after Write) dependency between instructions which could have caused pipieline stalls. Hence (C) is the answer.

Example:

I1: Read A to B
I2: Write C to A

Here, there is a WAR dependency and pipeline would need stalls. In order to avoid it register renaming is done and

Write C to A
will be
Write C to A'

WAR dependency is actually called anti-dependency and there is no real dependency except the fact that both uses same memory location. Register renaming can avoid this. Similarly WAW also.

http://people.ee.duke.edu/~sorin/ece252/lectures/4.2-tomasulo.pdf

21 votes -- Arjun Suresh (294k points)

1.20.26 Pipelining: GATE2013_45 top

http://gateoverflow.in/330

Selected Answer

After pipelining we have to adjust the stage delays such that no stage will be waiting for another to ensure smooth pipelining (continuous flow). Since we can not easily decrease the stage delay, we can increase all the stage delays to the maximum delay possible. So, here maximum delay is 10ns. Buffer delay given is 1ns. So, each stage takes 11ns in total.

FI of I9 can start only after the EI of I4. So, the total execution time will be

$$15 \times 11 = 165$$

	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
I1	FI	DI	FO	EI	WO										
I2		FI	DI	FO	EI	WO									
I3			FI	DI	FO	EI	WO								
I4				FI	DI	FO	EI	WO							
					stall										
						stall									
							stall								
I9								FI	DI	FO	EI	WO			
I10									FI	DI	FO	EI	WO		
I11										FI	DI	FO	EI	WO	
I12											FI	DI	FO	EI	WO

👍 40 votes -- gatecse (13.4k points)

answer = **option B**

WO					1	2	3	4	5	6	7	9	10	11	12
EI				1	2	3	4	5	6	7	9	10	11	12	
FO			1	2	3	4	5	6	7	9	10	11	12		
DI		1	2	3	4	5	6	7	9	10	11	12			
FI	1	2	3	4	5	6	7	9	10	11	12				

cycles in pink are stall cycles, at EI-4 it was notified to the system that instruction 9 has to be loaded next.
We have completed execution in a total of 15 cycles where each cycle was (10+1)ns long,

Hence, answer =
$15 \times 11 = 165$ ns

👍 13 votes -- Amar Vashishth (28.7k points)

1.20.27 Pipelining: GATE2014-1-43 top

http://gateoverflow.in/1921

Selected Answer

Time without pipeline = 6 stages=6 cycles

Time with pipeline =1+stall freqency*stall cycle

=1+.25*2

=1.5

Speed up = 6/1.5

=4

👍 23 votes -- aravind90 (589 points)

1.20.28 Pipelining: GATE2014-3-43 top

http://gateoverflow.in/2077

Selected Answer

five stages:

(IF), instruction decode and register fetch (ID/RF),

instruction execution (EX),

memory access (MEM), and register writeback (WB)

P old design:

with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns

MAX(1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns) = 2.2nsec

AVG instruction execution time is

T_{avg}*=(1+no of stalls*branch penality)*cycle time*

*=(1+0.20*2)2.2* *{ branch peanlity is 2 because the next instruction pointer at the end of the EX stage in the old design.}*

=3.08 nsec

Q :new DESIGN:

the designers decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages.

time of stages in new design ={1 ns, 0.73ns, 0.73ns, 0.73ns , 1ns,1ns, 1 ns, and 0.75 ns}

(IF), instruction decode

register fetch (ID/RF) ----> further divided into 3 ie with latency 0.73 of each

instruction execution (EX)--->further divided int 1 nsec of each)

memory access (MEM)

register writeback (WB)

MAX(1 ns, 0.73ns, 0.73ns, 0.73ns , 1ns,1ns, 1 ns, and 0.75 ns) =1nsec

AVG instruction execution time is

T_{avg}*=(1+no of stalls*branch penality)*cycle time*

*=(1+0.20*5)1* *{ branch peanlity is 5 because the next instruction pointer at the end of the EX2 stage in the new design.}*

=2 nsec

---

final result

P/Q=3.08/2 =1.54

18 votes -- kunal (20.8k points)

cpi for first case = 2.2(1+2*.2) as the stall required is 2 and 2.2 is the maximum stage delay.

cpi for second state = 1*(1+5*.2) as now stall increase to 5 as there are five stages before the address is calculated and the maximum stage delay now is 1.

cpu_time1/cpu_time2 = 3.08/2 = 1.54

18 votes -- Arpit Dhuriya (3k points)

1.20.29 Pipelining: GATE2014-3-9 top

http://gateoverflow.in/2043

Selected Answer

frequency = 1 / max(time in stages)
for P3 it is 1/1 GHz

for P1 it is 1/2 = 0.5 GHz
for P2, it is 1/1.5 = 0.67 GHz
for P4, it is 1/1.1 GHz

18 votes -- Arpit Dhuriya (3k points)

1.20.30 Pipelining: GATE2015-1-38 top

http://gateoverflow.in/8288

Selected Answer

Speed up = Old execution time/New execution time

Old execution time = CPI/2.5 = 4/2.5 = 1.6 ns

With pipelining, each instruction needs old execution time * old frequency/new frequency (without pipelining) = 1.6 * 2.5 / 2 = 2 ns

There are 5 stages and when there is no pipeline stall, this can give a speed up of up to 5 (happens when all stages take same number of cycles). In our case this time will be 2/5 = 0.4 ns. But clock frequency being 2 GHz, clock cycle is 1/2 GHz = 0.5 ns and a pipeline stage cannot be faster than this.

So, average instruction execution time after pipelining = max (0.4, 0.5) = 0.5 ns.

So, speed up compared to non-pipelined version = 1.6 / 0.5 = 3.2.

25 votes -- Arjun Suresh (294k points)

answer = **3.2**

To compute cycle time, we know that a 2.5GHz processor means it completes 2.5G cycles in a second. so, for an instruction which on an average takes 4 cycles to get completed will take
$4/2.5G$ seconds.

On successful piplelining(i.e one which has no stalls)
$CPI = 1$ as during it an instruction takes just one cycle time to get completed. So,

$$\begin{aligned}\text{Speed Up} &= \frac{\text{Old Execution Time of an Instruction}}{\text{New Execution Time of an Instruction}}\\ &= \frac{CPI_{old}/CF_{old}}{CPI_{new}/CF_{new}}\\ &= \frac{4/2.5G}{1/2G}\\ &= 3.2\end{aligned}$$

44 votes -- naresh1845 (1.4k points)

1.20.31 Pipelining: GATE2015-2_44 top

http://gateoverflow.in/8218

Selected Answer

	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15
I1	IF	OF	PO	PO	PO	WB									
I2		IF	OF	-	-	PO	PO	PO	PO	PO	WB				
I3			IF	-	-	-	-	-	-	-	OF	PO	WB		

I4	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15
											IF		OF	PO	WB

It is mentioned in the question that operand forwarding takes place from PO stage to OF stage and not to PO stage. So, 15 clock cycles.

But since operand forwarding is from PO-OF, we can do like make the PO stage produce the output during the rising edge of the clock and OF stage fetch the output during the falling edge. This would mean the final PO stage and OF stage can be done in one clock cycle making the total number of cycles = 13. And 13 is the answer given in GATE key.

	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13
I1	IF	OF	PO	PO	PO	WB							
I2		IF	OF	-	-	PO	PO	PO	PO	PO	WB		
I3			IF	-	-	-	-	-	-	OF	PO	WB	
I4				-	-	-	-	-	-	IF	OF	PO	WB

Ref: http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html

35 votes -- Arjun Suresh (294k points)

1.20.32 Pipelining: GATE2015-3_51 top

http://gateoverflow.in/8560

Selected Answer

Ref: Page 24 http://www2.cs.siu.edu/~cs401/Textbook/ch3.pdf

S1 is needed at time 1 and 5, so its forbidden latency is 5-1 = 4.

S2 is needed at time 2 and 4, so its forbidden latency is 4-2 = 2.

So, forbidden latency = (2,4,0) (0 by default is forbidden)

Allowed latency = (1,3,5) (any value more than 5 also).

Collision vector (4,3,2,1,0) = 10101 which is the initial state as well.

From initial state we can have a transition after "1" or "3" cycles and we reach new states with collision vectors (10101 >> 1 + 10101 = 11111) and (10101 >> 3 + 10101 = 10111) respectively. These 2 becomes states 2 and 3 respectively. For "5" cycles we come back to state 1 itself.

From state 2 (11111), the new collision vector is 11111. We can have a transition only when we see first 0 from right. So, here it happens on 5th cycle only which goes to initial state. (Any transition after 5 or more cycles goes to initial state as we have 5 time slices).

From state 3 (10111), the new collision vector is 10111. So, we can have a transition on 3, which will give (10111 >> 3 + 10101 = 10111) third state itself. For 5, we get the initial state. Thus all the transitions are complete.

State\Time	1	3	5
1 (10101)	2	3	1
2 (11111)	-	-	1
3 (10111)	-	3	1

So, minimum length cycle is of **length 3** either from 3-3 or from 1-3, 3-1.

Not asked in question, still.

Pipeline throughput is the number of instructions initiated per unit time. So, with MAL = 3, we have 2 initiations in 1+3 = 4 units of time (one at time unit 1 and another at time unit 4). So, throughput = 2/4 = 0.5.

Pipeline efficiency is the % of time every stage of pipeline is being used. For the given question we can extend the reservation table and taking MAL = 3, we can initiate new tasks after every 3 cycles. So, we can consider the time interval from 4-6 in below figure. (The red color shows a stage not being used- affects efficiency).

Time→											
	1	2	3	**4**	**5**	**6**	7	8	9	10	11
S1	X			Y	X	\	Z	Y		A	Z

S2		X		X	Y	\	Y	Z		Z	A
S3			X	\	\	Y			Z		

Here (during cycles 4-6), stage 1 is used 2/3, stage 2 is used 2/3 and stage 3 is used 1/3. So, total stage utilization = (2+2+1)/9 = 5/9 and efficiency = 500/9% = 55.55%.

For simulation, Ref: http://www.ecs.umass.edu/ece/koren/architecture/ResTable/SimpRes/

Similar Question

- http://gateoverflow.in/77125/advanced-computer-architecture-collision-vector-pipeline

11 votes -- Arjun Suresh (294k points)

1.20.33 Pipelining: GATE2017-1-50 top http://gateoverflow.in/118719

Selected Answer

CASE 1

stages 5, max delay= 22(after adding buffer delay), number of instructions= 20

CASE 2

stages 6(since OF is split), max delay=14, number of instructions=20

so execution time is (K+N-1)*Max delay

speedup =528/350=1.508 (Execution time case 1/Execution time case 2)

so answer is 1.508

8 votes -- sriv_shubham (2.7k points)

1.20.34 Pipelining: ISI2012-CS-2a top http://gateoverflow.in/47848

Selected Answer

As there are 5 stages so 1 istruction will take 5 clock cycles, now all subsequent instructions will take 1-1 cycle each so Now without any stall cycle total cycles are - 5+(100-1) =104

now each 3rd instruction is taking one stall cycle so total stall cycles in 100 instructions are 100/3=33

total cycle to complete the 100 instructions are - 104+33=137cycles.

Max time taken from all the stages are 9ns and 1 ns is overhead then 10ns can be given as clock cycle time so total time taken is: 137*10=1370ns ...:)

2 votes -- shayal chhabra (821 points)

1.21 Runtime Environments(2) top

1.21.1 Runtime Environments: GATE2001-1.10, UGCNET-Dec2012-III-36 top

Suppose a processor does not have any stack pointer registers, which of the following statements is true?

A. It cannot have subroutine call instruction
B. It cannot have nested subroutines call
C. Interrupts are not possible
D. All subroutine calls and interrupts are possible

gate2001 co&architecture normal ugcnetdec2012iii runtime-environments

Answer

1.21.2 Runtime Environments: GATE2008-37, ISRO2009-38 top

http://gateoverflow.in/448

The use of multiple register windows with overlap causes a reduction in the number of memory accesses for

I. Function locals and parameters

II. Register saves and restores

III. Instruction fetches

A. I only
B. II only
C. III only
D. I, II and III

gate2008 co&architecture normal isro2009 runtime-environments

Answer

Answers: Runtime Environments

1.21.1 Runtime Environments: GATE2001-1.10, UGCNET-Dec2012-III-36 top

http://gateoverflow.in/703

Selected Answer

i think ans is B.

because in nested subroutine calls we used to push old subroutines into stack and pointing most recent call with stack pointer.

14 votes -- jayendra (8.1k points)

1.21.2 Runtime Environments: GATE2008-37, ISRO2009-38 top

http://gateoverflow.in/448

Selected Answer

I. Functions locals and parameters
this is true because overlapped registers eliminates the need for memory accesses. we here got to use registers instead.

II. Register saves and restores
this is false bc we need to see where memory accesses are reduced here before also we were using register as it says Register saves... later also (i.e. after using multiple register windows) registers will are refered. So NO memory accesses are reduced here.

III. Instruction fetches
it has nothing to do with reduction in memory accesses.

Hence, **option A** is correct.

11 votes -- Amar Vashishth (28.7k points)

1.22 Speedup(2) top

1.22.1 Speedup: GATE2004-IT-50 top

http://gateoverflow.in/790

In an enhancement of a design of a CPU, the speed of a floating point until has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is 2:3 and the floating point operation used to take twice the time taken by the fixed point operation in the original design?

A. 1.155
B. 1.185

C. 1.255
D. 1.285

gate2004-it normal co&architecture speedup

Answer

1.22.2 Speedup: GATE2014-1-55 top

http://gateoverflow.in/1935

Consider two processors P_1 and P_2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1. If the clock frequency of P_1 is 1GHZ, then the clock frequency of P_2 (in GHz) is _______.

gate2014-1 co&architecture numerical-answers normal speedup

Answer

Answers: Speedup

1.22.1 Speedup: GATE2004-IT-50 top

http://gateoverflow.in/790

Selected Answer

```
Speed up = Original time taken/ new time taken
Let x be the time for a fixed point operation
Original time taken = (3x + 2*2x)/5 = 7x/5
New time taken = ((3x/1.1) + (4x/1.2))/5 = 8x/1.32*5
So, speed up = 7*1.32/8 = 1.155
```

22 votes -- gatecse (13.4k points)

1.22.2 Speedup: GATE2014-1-55 top

http://gateoverflow.in/1935

Selected Answer

CPU TIME (T) = No. of Instructions(I) x No. of Cycles Per Instruction (c) x Cycle Time (t)

OR

CPU TIME (T) = $\frac{No. of Instructions(I) \times No. of Cycles Per Instruction(c)}{Clock frequency(f)}$

$\rightarrow T = I_c \times CPI \times F^{-1}$

$\rightarrow \frac{T \times F}{CPI} = I_c$

P_1 & P_2 executing same instruction set **So**, No. of Instructions same for both = I_1 = I_2 = I

If P_1 takes T_1 time $\rightarrow$ T_2 = 0.75 x T1 $\rightarrow$ $\frac{T_2}{T_1}$ = 0.75

If P_1 incurs C_1 clock cycles per instruction $\rightarrow$ C_2 = 1.2 x C_1 $\rightarrow$ $\frac{C_2}{C_1}$ = 1.2

Since I is same for both $\rightarrow \frac{(f_1 \times T_1)}{c1} = \frac{(f_2 \times T_2)}{c2}$ and f1 = 1 GHz

$\rightarrow$ F_2 = $(\frac{C_2}{C_1}) \times (\frac{T_1}{T_2}) \times F_1$ = $\frac{1.2 \times 1GHz}{0.75}$ = 1.6 GHz

Hence,the clock frequency of P_2 is = 1.6 GHz.

28 votes -- Suraj Kaushal (361 points)

Execution time (T) = CPI * #instructions * time for a clock
= CPI * #instructions / clock frequency (F)

Given P1 and P2 execute the same set of instructions and

$T_2 = 0.75\ T_1$,
$CPI_2 = 1.2\ CPI_1$ and
$F_1 = 1GHz$.

So,

$\frac{T_1}{CPI_1} \times F_1 = \frac{T_2}{CPI_2} \times F_2$

$\frac{T_1}{CPI_1} \times 1GHz = \frac{0.75T_1}{1.2CPI_1} \times F_2$

$\implies F_2 = \frac{1.2}{0.75} GHz$

$= 1.6GHz$

10 votes -- Arjun Suresh (294k points)

1.23 Virtual Memory(3) top

1.23.1 Virtual Memory: GATE1991_03,iii top http://gateoverflow.in/517

03. Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

(iii) The total size of address space in a virtual memory system is limited by

a. the length of MAR
b. the available secondary storage
c. the available main memory
d. all of the above
e. none of the above

gate1991 co&architecture virtual-memory normal

Answer

1.23.2 Virtual Memory: GATE2004-47 top http://gateoverflow.in/318

Consider a system with a two-level paging scheme in which a regular memory access takes 150 nanoseconds, and servicing a page fault takes 8 milliseconds. An average instruction takes 100 nanoseconds of CPU time, and two memory accesses. The TLB hit ratio is 90%, and the page fault rate is one in every 10,000 instructions. What is the effective average instruction execution time?

A. 645 nanoseconds
B. 1050 nanoseconds
C. 1215 nanoseconds
D. 1230 nanoseconds

gate2004 co&architecture virtual-memory normal

Answer

1.23.3 Virtual Memory: GATE2008-38 top http://gateoverflow.in/449

In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is

A. before effective address calculation has started

B. during effective address calculation

C. after effective address calculation has completed

D. after data cache lookup has completed

gate2008 co&architecture virtual-memory normal

Answer

Answers: Virtual Memory

1.23.1 Virtual Memory: GATE1991_03,iii top http://gateoverflow.in/517

Selected Answer

Answer is (a) and (b)

Virtual memory concept is independent of size of main memory and depends only on the availability of the secondary storage.

MAR holds the address generated by CPU and this obviously limits the total virtual memory address space.

14 votes -- Kalpna Bhargav (3.2k points)

1.23.2 Virtual Memory: GATE2004-47 top http://gateoverflow.in/318

Selected Answer

```
Average Instruction execution time

 = Average CPU execution time + Average time for getting data(instruction operands from memory for each instruction)

 =   Average CPU execution time
   + Average address translation time for each instruction
   + Average memory fetch time for each instruction
   + Average page fault time for each instruction
```

=

$$100 + 2\Big(0.9(0) + 0.1(2 \times 150)\Big) + 2 \times 150 + \frac{1}{10000} \times 8 \times 10^6$$

(Page Fault Rate per 10,000 instruction is directly given in question.Two memory accesses per instruction and hence we need 2 $\times$ address translation time for average instruction execution time)

[TLB access time assumed as 0 and 2 page tables need to be accessed in case of TLB miss as the system uses two-level paging]

=

$$100 + 60 + 300 + 800$$

=

$$1260ns$$

56 votes -- Arjun Suresh (294k points)

(gate 2004 qus)

EAIET=[CPU execution time]+(TLB Hit*2*Memory access time +TLB miss ratio(page table access time+2*memory access time))+{page fault probability*page fault service time}
That is 100ns+(0.9*2*150+0.1(150+150+2*150))+800ns.....[800ns herecomes from 0.0001*8*10^6]

=100ns+2*(135+30)ns+800ns
=100ns+2*165ns+800ns
=1230ns

12 votes -- Rohan Ghosh (1.9k points)

1.23.3 Virtual Memory: GATE2008-38 top http://gateoverflow.in/449

Selected Answer

C as only after the calculation of Virtual address you can look up in the TLB

13 votes -- Shaun Patel (6.9k points)

2 Computer Networks (189) top

2.1 Application Layer Protocols(8) top

2.1.1 Application Layer Protocols: GATE 2016-1-25 top http://gateoverflow.in/39628

Which of the following is/are example(s) of stateful application layer protocol?

i. HTTP
ii. FTP
iii. TCP
iv. POP3

A. (i) and (ii) only
B. (ii) and (iii) only
C. (ii) and (iv) only
D. (iv) only

gate2016-1 computer-networks application-layer-protocols normal

Answer

2.1.2 Application Layer Protocols: GATE2005-IT-25 top http://gateoverflow.in/3770

Consider the three commands : PROMPT, HEAD and RCPT.
Which of the following options indicate a correct association of these commands with protocols where these are used?

A. HTTP, SMTP, FTP
B. FTP, HTTP, SMTP
C. HTTP, FTP, SMTP
D. SMTP, HTTP, FTP

gate2005-it computer-networks application-layer-protocols normal

Answer

2.1.3 Application Layer Protocols: GATE2006-IT-18 top http://gateoverflow.in/3557

HELO and PORT, respectively, are commands from the protocols

A. FTP and HTTP
B. TELNET and POP3
C. HTTP and TELNET
D. SMTP and FTP

gate2006-it computer-networks application-layer-protocols normal

Answer

2.1.4 Application Layer Protocols: GATE2007-20 top http://gateoverflow.in/1218

Which one of the following uses UDP as the transport protocol?

A. HTTP
B. Telnet
C. DNS
D. SMTP

gate2007 computer-networks network-protocols application-layer-protocols easy

Answer

2.1.5 Application Layer Protocols: GATE2008-14, ISRO2016-74 top http://gateoverflow.in/412

What is the maximum size of data that the application layer can pass on to the TCP layer below?

A. Any size
B. 2^{16} bytes - size of TCP header
C. 2^{16} bytes
D. 1500 bytes

gate2008 easy computer-networks application-layer-protocols isro2016

Answer

2.1.6 Application Layer Protocols: GATE2008-IT-20 top http://gateoverflow.in/3280

Provide the best matching between the entries in the two columns given in the table below:

I.	Proxy Server	a.	Firewall
II.	Kazaa, DC++	b.	Caching
III.	Slip	c.	P2P
IV.	DNS	d.	PPP

A. I-a, II-d, III-c, IV-b
B. I-b, II-d, III-c, IV-a
C. I-a, II-c, III-d, IV-b
D. I-b, II-c, III-d, IV-a

gate2008-it computer-networks normal application-layer-protocols

Answer

2.1.7 Application Layer Protocols: GATE2011_4 top http://gateoverflow.in/2106

Consider the different activities related to email.

- m1: Send an email from mail client to mail server
- m2: Download an email from mailbox server to a mail client
- m3: Checking email in a web browser

Which is the application level protocol used in each activity?

A. m1: HTTP m2: SMTP m3: POP
B. m1: SMTP m2: FTP m3: HTTP
C. m1: SMTP m2: POP m3: HTTP
D. m1: POP m2: SMTP m3: IMAP

gate2011 computer-networks application-layer-protocols easy

Answer

2.1.8 Application Layer Protocols: GATE2012_10 top http://gateoverflow.in/42

The protocol data unit (PDU) for the application layer in the Internet stack is

(A) Segment
(B) Datagram
(C) Message
(D) Frame

gate2012 computer-networks application-layer-protocols easy

Answer

Answers: Application Layer Protocols

2.1.1 Application Layer Protocols: GATE 2016-1-25 top http://gateoverflow.in/39628

Selected Answer

HTTP - stateless

FTP - stateful

TCP - not application layer protocol

POP3 - Stateful

And according to options answer would be C)

29 votes -- Abhilash Panicker (8.8k points)

2.1.2 Application Layer Protocols: GATE2005-IT-25 top http://gateoverflow.in/3770

Selected Answer

RCPT->Recipient to,As the name suggest it is used in SMTP(Simple Mail Transfer protocol)

HEAD->this is used in HTTP to get the meta-information,to decide the category of packet.

Prompt->turns off prompting for individual files when using the mget or mput commands

14 votes -- nagalla pruthvi (883 points)

2.1.3 Application Layer Protocols: GATE2006-IT-18 top http://gateoverflow.in/3557

Selected Answer

Answer: D

Ref:

http://en.wikipedia.org/wiki/Simple_Mail_Transfer_Protocol#SMTP_transport_example

http://en.wikipedia.org/wiki/File_Transfer_Protocol#Protocol_overview

6 votes -- Rajarshi Sarkar (35k points)

2.1.4 Application Layer Protocols: GATE2007-20 top http://gateoverflow.in/1218

Selected Answer

The answer is C.

Where quick response is needed, there UDP is preferred.

15 votes -- Gate Keeda (19.1k points)

2.1.5 Application Layer Protocols: GATE2008-14, ISRO2016-74 top http://gateoverflow.in/412

Selected Answer

OPTION A

Its transport layers responsibility to divide data in to fragments/ packets. Application layer need not worry about it.

14 votes -- Desert_Warrior (9.6k points)

2.1.6 Application Layer Protocols: GATE2008-IT-20 top http://gateoverflow.in/3280

Selected Answer

Ans is C) I-a, II-c, III-d, IV-b

I. Proxy Server ==> Proxy Server and Firewall can be combined => a. Firewall

II. Kazaa, DC++ => These are P2P application. c. P2P

III. Slip => . P2P Slip is predecessor of PPP. => d. PPP

IV. DNS => DNS responses are often catedh = > b. Caching

7 votes -- Akash (43.8k points)

2.1.7 Application Layer Protocols: GATE2011_4 top http://gateoverflow.in/2106

Selected Answer

Sender/Client send mail from client mailbox to server mail box with the help of SMTP protocol whereas Receiver or Server retreive the mail from its mail box to reading using POP3 protocal.

When we want to take the help process to see email in browser in that case we HTTP.Because It create buetiful page of mailbox with the help of process.

10 votes -- Paras Singh (5.5k points)

2.1.8 Application Layer Protocols: GATE2012_10 top http://gateoverflow.in/42

Selected Answer

(C) Message is answer.

For Application, Presentation and Session layers, the PDU is message

For Transport layer, PDU is segment for TCP and datagram for UDP

For Network layer, PDU is packet

For Datalink layer, PDU is frames

For physical layer, PDU is stream of bits

29 votes -- gatecse (13.4k points)

2.2 Bit Stuffing(1) top

2.2.1 Bit Stuffing: GATE2014-3-24 top http://gateoverflow.in/2058

A bit-stuffing based framing protocol uses an 8-bit delimiter pattern of 01111110. If the output bit-string after stuffing is 01111100101, then the input bit-string is

A. 0111110100
B. 0111110101
C. 0111111101
D. 0111111111

gate2014-3 computer-networks bit-stuffing

Answer

Answers: Bit Stuffing

2.2.1 Bit Stuffing: GATE2014-3-24 top

http://gateoverflow.in/2058

Selected Answer

011111 *one zero emitted here* 0101

14 votes -- abhishek1317 (299 points)

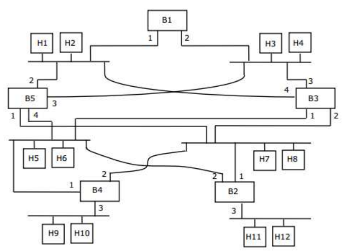
2.3 Bridges(2) top

2.3.1 Bridges: GATE2006-82 top

http://gateoverflow.in/1855

Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



For the given connection of LANs by bridges, which one of the following choices represents the depth first traversal of the spanning tree of bridges?

A. B1, B5, B3, B4, B2
B. B1, B3, B5, B2, B4
C. B1, B5, B2, B3, B4
D. B1, B3, B4, B5, B2

gate2006 computer-networks bridges normal

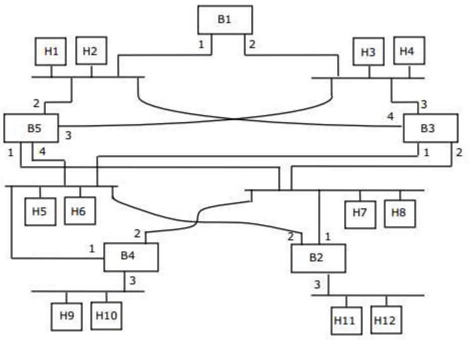
Answer

2.3.2 Bridges: GATE2006-83 top

http://gateoverflow.in/79790

Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



Consider the spanning tree B1, B5, B3, B4, B2 for the given connection of LANs by bridges, that represents the depth first traversal of the spanning tree of bridges. Let host H1 send out a broadcast ping packet. Which of the following options represents the correct forwarding table on B3?

A.

Hosts	Port
H1, H2, H3, H4	3
H5, H6, H9, H10	1
H7, H8, H11, H12	2

B.

Hosts	Port
H1, H2	4
H3, H4	3
H5, H6	1
H7, H8, H9, H10,H11,H12	2

C.

Hosts	Port
H3, H4	3
H5, H6, H9, H10	1
H1, H2	4
H7, H8, H11, H12	2

D.

Hosts	Port
H1, H2, H3, H4	3
H5, H7, H9, H10	1
H7, H8, H11, H12	4

gate2006 computer-networks bridges normal

Answer

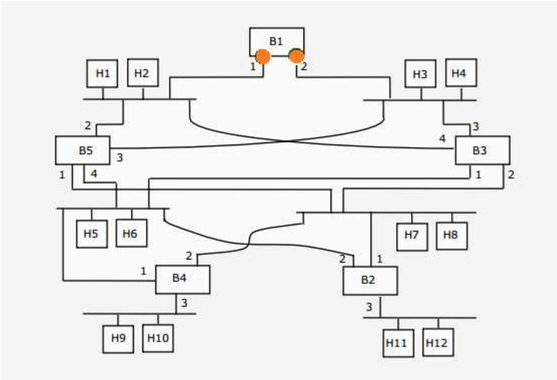
Answers: Bridges

2.3.1 Bridges: GATE2006-82 top

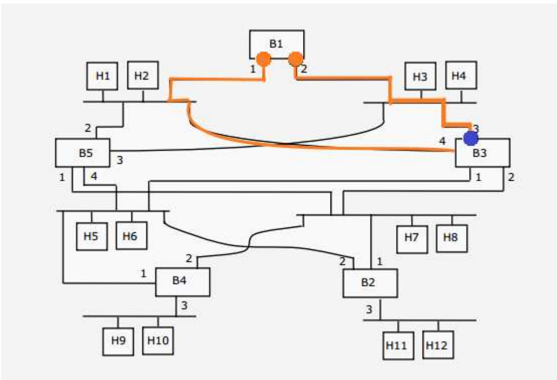
http://gateoverflow.in/1855

Selected Answer

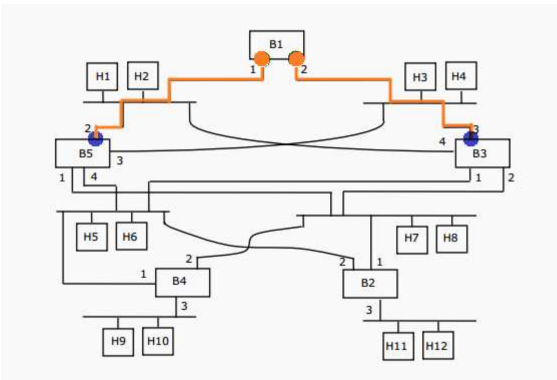
- First select B1 as the root bridge. This selection is based on lower serial ID as given in the question.
- All ports of root bridge are designated ports and they are in forwarding state.



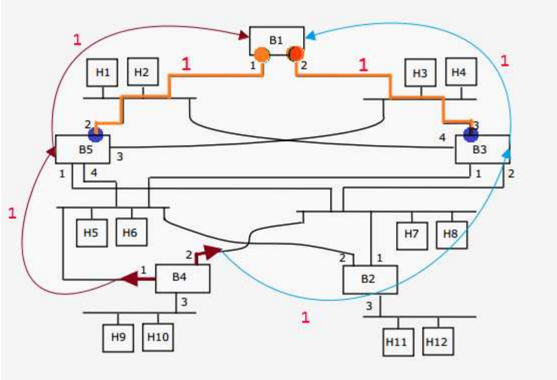
- Every non-root bridge must have a root port. All root ports are placed in forwarding state.
- Root port is the port that is closest to the root bridge
- For example, we observe bridge $B3$.
- It has two ports leading to the root bridge. If we assume bridge-to-bridge cost as 1 unit, both these paths have the same cost. Then we will select the lower port index as given in the question as the root port for the bridge $B3$.
- port 3 of $B3$ becomes the root port.



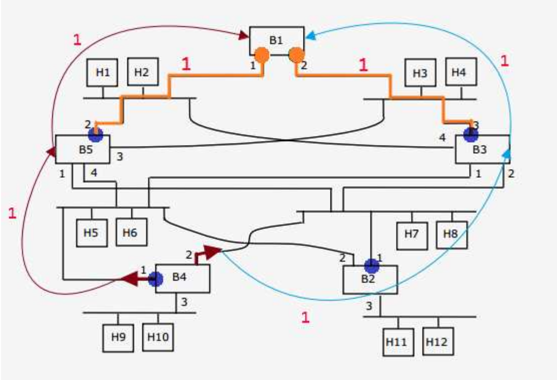
- Using the same logic we will find out the root ports for $B5$ also.



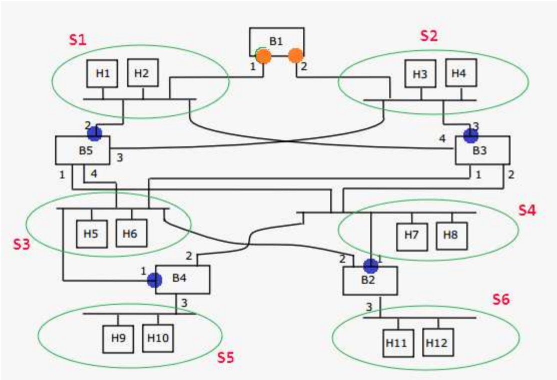
- Coming to $B4$ for root port selection.



- We have again two different paths with the same cost. We will select port 1 as the root port for $B4$
- Using the same logic port 1 is selected as root port for $B2$ as well.

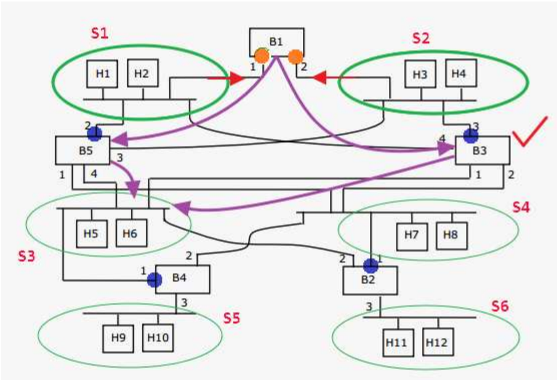


- Now we have to consider the designated ports
- The designated ports are the ports responsible for forwarding traffic onto a network segment
- We have total 6 network segments or LAN's. Each segment will have one designated ports.

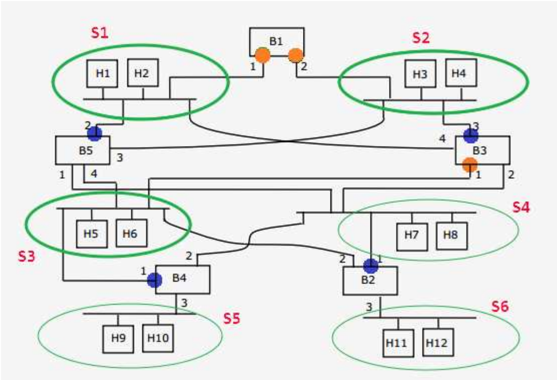


- $S1$ and $S2$ are connected to the root bridge itself via two designated ports. So no issue with segments $S1$ and $S2$ traffic.
- Let's consider other segments.

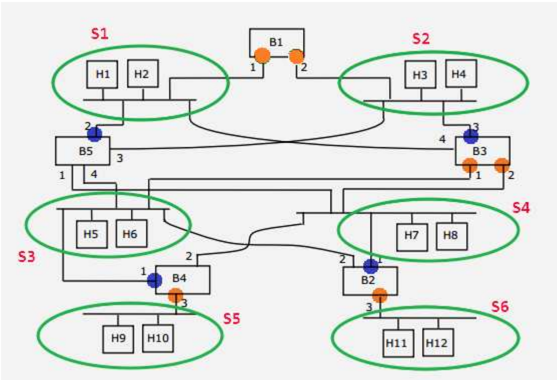
- For example $S3$.



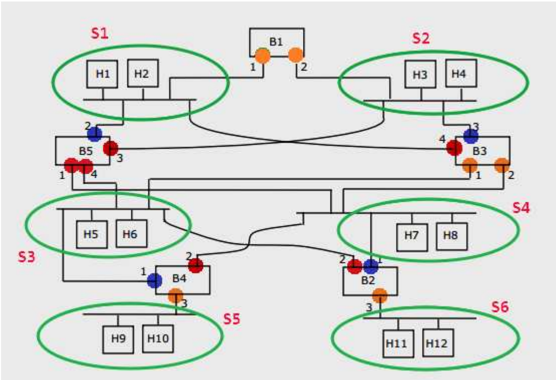
- $B2$,$B3$,$B4$,$B5$ all can forward traffic to this segment $S3$
- According to the question in this situation, we will consider only those bridges which arenearer to the root bridge $B1$.
- $B5$ and $B3$ are both nearer to the root bridge.
- Then we will break this tie by selecting the lower bridge serial ID i.e. $B3$ is selected and designated port is port 1 of $B3$ for the segment $S3$



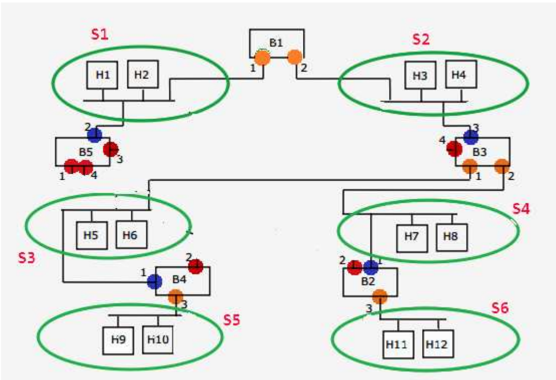
- Similarly, we can choose designated ports for $S4$, $S5$ and $S6$



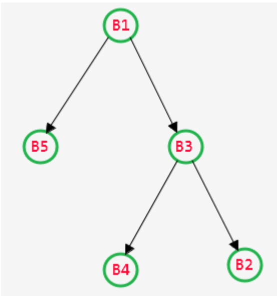
- Remaining all ports are blocked ports.



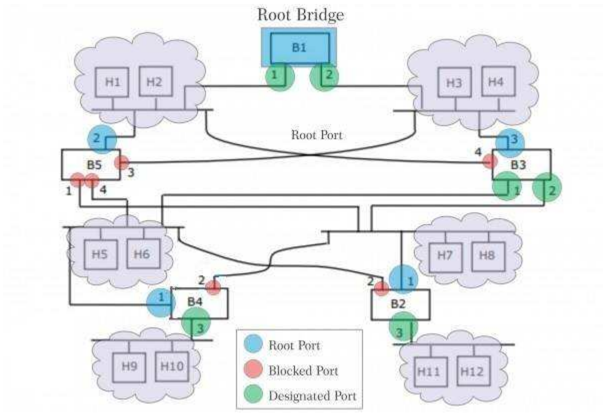
- This the final spanning Tree



- DFS traversal will give answer as A



28 votes -- Debashish Deka (51.4k points)



This makes it clear that:
Q.82 answer = **option A**
Q.83 answer = **option A**

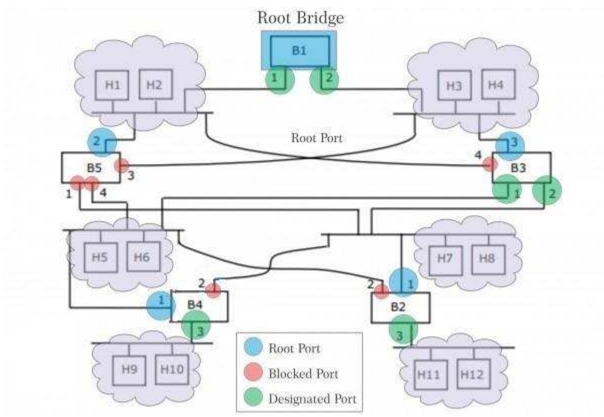
13 votes -- Amar Vashishth (28.7k points)

2.3.2 Bridges: GATE2006-83 top

http://gateoverflow.in/79790

Selected Answer

Option is A see this as we go with options , option A match only with this picture.



4 votes -- Bikram (44.7k points)

2.4 Communication(9) top

2.4.1 Communication: GATE1987-2-i top

http://gateoverflow.in/87074

Match the pairs in the following questions:

(A) Cyclic redundancy code	(p) Error correction
(B) Serial communication	(q) Wired-OR
(C) Open collector	(r) Error detection
(D) Hamming code	(s) RS-232-C

gate1989 descriptive computer-networks communication

Answer

2.4.2 Communication: GATE1993-6.4, ISRO2008-14 top http://gateoverflow.in/2287

Assume that each character code consists of 8 bits. The number of characters that can be transmitted per second through an asynchronous serial line at 2400 baud rate, and with two stop bits is

A. 109
B. 216
C. 218
D. 219

gate1993 computer-networks communication normal isro2008

Answer

2.4.3 Communication: GATE1997_2.3 top http://gateoverflow.in/2229

Purpose of a start bit in RS 232 serial communication protocol is

A. to synchronize receiver for receiving every byte
B. to synchronize receiver for receiving a sequence of bytes
C. a parity bit
D. to synchronize receiver for receiving the last byte

gate1997 computer-networks communication normal

Answer

2.4.4 Communication: GATE2002-1.11 top http://gateoverflow.in/815

In serial data transmission, every byte of data is padded with a '0' in the beginning and one or two '1's at the end of byte because

A. receiver is to be synchronized for byte reception
B. receiver recovers lost '0's and '1's from these padded bits
C. padded bits are useful in parity computation
D. none of the above

gate2002 computer-networks communication easy

Answer

2.4.5 Communication: GATE2004-22 top http://gateoverflow.in/1019

How many 8-bit characters can be transmitted per second over a 9600 baud serial communication link using asynchronous mode of transmission with one start bit, eight data bits, two stop bits and one parity bit?

A. 600
B. 800
C. 876
D. 1200

gate2004 computer-networks communication normal

Answer

2.4.6 Communication: GATE2004-IT-45 top http://gateoverflow.in/3688

A serial transmission T1 uses 8 information bits, 2 start bits, 1 stop bit and 1 parity bit for each character. A synchronous transmission T2 uses 3 eight-bit sync characters followed by 30 eight-bit information characters. If the bit rate is 1200 bits/second in both cases, what are the transfer rates of T1 and T2?

A. 100 characters/sec, 153 characters/sec
B. 80 characters/sec, 136 characters/sec
C. 100 characters/sec, 136 characters/sec
D. 80 characters/sec, 153 characters/sec

gate2004-it computer-networks communication normal

Answer

2.4.7 Communication: GATE2007-IT-62 top http://gateoverflow.in/3506

Let us consider a statistical time division multiplexing of packets. The number of sources is 10. In a time unit, a source transmits a packet of 1000 bits. The number of sources sending data for the first 20 time units is 6, 9, 3, 7, 2, 2, 2, 3, 4, 6, 1, 10, 7, 5, 8, 3, 6, 2, 9, 5 respectively. The output capacity of multiplexer is 5000 bits per time unit. Then the average number of backlogged of packets per time unit during the given period is

A. 5
B. 4.45
C. 3.45
D. 0

gate2007-it computer-networks communication normal

Answer

2.4.8 Communication: GATE2007-IT-64 top http://gateoverflow.in/3509

A broadcast channel has 10 nodes and total capacity of 10 Mbps. It uses polling for medium access. Once a node finishes transmission, there is a polling delay of 80 μs to poll the next node. Whenever a node is polled, it is allowed to transmit a maximum of 1000 bytes. The maximum throughput of the broadcast channel is

A. 1 Mbps
B. 100/11 Mbps
C. 10 Mbps
D. 100 Mbps

gate2007-it computer-networks communication normal

Answer

2.4.9 Communication: GATE2012_44 top http://gateoverflow.in/2153

Consider a source computer (S) transmitting a file of size 10^6 bits to a destination computer (D) over a network of two routers $(R_1 \text{ and } R_2)$ and three links $(L_1, L_2, \text{ and } L_3)$. L_1 connects S to R_1; L_2 connects R_1 to R_2; and L_3 connects R_2 to D. Let each link be of length 100 km. Assume signals travel over each link at a speed of10^8 meters per second. Assume that the link bandwidth on each link is 1 Mbps. Let the file be broken down into 1000 packets each of size 1000 bits. Find the total sum of transmission and propagation delays in transmitting the file from S to D?

(A) 1005 ms
(B) 1010 ms
(C) 3000 ms
(D) 3003 ms

gate2012 computer-networks communication normal

Answer

Answers: Communication

2.4.1 Communication: GATE1987-2-i top http://gateoverflow.in/87074

Selected Answer

(A) Cyclic redundancy code	(r) Redundancy checking technique (error detection)
(B) Serial communication	(s) RS-232-C

(C) Open collector (q) wired OR
(D) Hamming code (p) error correction method

Explainations
A) A **cyclic redundancy check** (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data

B) RS-232C is the physical interface that your computer uses to talk to and exchange data with your modem and other serial devices

C) ref: http://www.ni.com/white-paper/3544/en/

D) The Hamming code is an error correction method using redundant bits. By rearranging the order of bit transmission of the data units, the Hamming code can correct burst errors.

1 votes -- Lokesh . (9.8k points)

2.4.2 Communication: GATE1993-6.4, ISRO2008-14 top

http://gateoverflow.in/2287

Selected Answer

Total bit per character = 8 bit data + 2 stop bit +1 start bit (#) = 11 bits
no of characters = 2400/11 = 218.18

Since it is asked for transmitted characters we take floor and answer is 218.

13 votes -- Digvijay (47k points)

2.4.3 Communication: GATE1997_2.3 top

http://gateoverflow.in/2229

A) Because RS 232 requires a start before each byte transmission for synchronization..

2 votes -- Hunaif (485 points)

2.4.4 Communication: GATE2002-1.11 top

http://gateoverflow.in/815

Selected Answer

In serial communication in beginning '0' is padded as start bit and one or two '1's are padded as stop bit.

and those bits are for synchronize receiver

http://www.powerbasic.com/support/help/pbcc/start_and_stop_bits.htm

http://esd.cs.ucr.edu/labs/serial/serial.html

6 votes -- srestha (58.4k points)

2.4.5 Communication: GATE2004-22 top

http://gateoverflow.in/1019

Selected Answer

The baud rate is the rate at which information is transferred in a communication channel. Serial ports use two-level (binary) signaling, so the data rate in bits per second is equal to the symbol rate in bauds. Ref: https://en.wikipedia.org/wiki/Serial_port#Speed.

"9600 baud" means that the serial port is capable of transferring a maximum of 9600 bits per second."

So, transmission rate here = 9600 bps

An eight bit data (which is a char) requires 1 start bit, 2 stop bits and 1 parity bit = 12 bits.

So, number of characters transmitted per second = 9600 / 12 = 800

15 votes -- Arjun Suresh (294k points)

2.4.6 Communication: GATE2004-IT-45 top

http://gateoverflow.in/3688

Selected Answer

1. T_1: 1 char. = (8 + 2 + 1 + 1) = 12 bit

Transfer Rate = 1200/12 = 100 char/sec.

T_2: Transfer character in bits = 24 + 240 = 264 bits

In 264 = 30 character

Then 1200 = ?

264/30 = 1200/X

X = 136.3 character / sec.

so correct option is (C)

14 votes -- Shreyans Dhankhar (2.6k points)

2.4.7 Communication: GATE2007-IT-62 top

http://gateoverflow.in/3506

Selected Answer

Answer is B

Here we can spent at max 5 packets per Time unit 5000 /1000.

So Whatever which is not sent is backlog.

So

First Time Unit => 6 ,

Backlog in First time unit => 6-5 => 1 This one gets added to next Time units load

Second time unit => 9 + 1 (One from Previous Time Unit)

Backlog in Second time Unit = 10-5 => 5 (This one gets added to next Time Units load.)

Total Backlog this way = 1+5+3+5+2+0+0+0+0+1+0+5+7+7+10+8+9+6+10+10=89

Avg Backlog=89/20=4.45

The average number of backlogged of packets per time unit during the given period is 4.45 , (Option B) .

19 votes -- Akash (43.8k points)

2.4.8 Communication: GATE2007-IT-64 top

http://gateoverflow.in/3509

Selected Answer

Propagation time is not given so that's negligible here.
efficiency = transmission time/(transmission time + polling time)
Tx=1000 bytes/10Mbps =800μs.
Delay because of polling is = 80 μs
Efficiency of channel , e =transmission delay/ (total delay) =800/(800+80)= 10/11
Maximum throughput is =(10/11) * 10 Mbps= 100/11 Mbps

23 votes -- Manu Thakur (6k points)

2.4.9 Communication: GATE2012_44 top

http://gateoverflow.in/2153

Selected Answer

routers are store and forward devices.
Propagation time = 100km/10^8m/s = 1 milli second
Transmission time for a pocket = 1000/10^6 = 1 milli second

Packets will be forwarded in pipelined manner, after the first packet reaches the receiver, in every 1 ms a new one arrives.

now Time taken by packet no 1 to reach destination is :
1 ms (TT at sender) + 1 ms (PT from sender to R1) + 1ms (TT at R1) + 1ms(PT from R1 to R2) + 1ms (TT at R2) + 1ms (PT from R2 to destination)
= 6ms

So, time for packet 1000 = 6ms + 999ms
= 1005ms

31 votes -- Digvijay (47k points)

2.5 Congestion Control(4) top

2.5.1 Congestion Control: GATE2005-IT-73 top

http://gateoverflow.in/3836

On a TCP connection, current congestion window size is Congestion Window = 4 KB. The window size advertised by the receiver is Advertise Window = 6 KB. The last byte sent by the sender is LastByteSent = 10240 and the last byte acknowledged by the receiver is LastByteAcked = 8192. The current window size at the sender is

A. 2048 bytes
B. 4096 bytes
C. 6144 bytes
D. 8192 bytes

gate2005-it computer-networks congestion-control normal

Answer

2.5.2 Congestion Control: GATE2008-56 top

http://gateoverflow.in/479

In the slow start phase of the TCP congestion algorithm, the size of the congestion window

A. does not increase
B. increase linearly
C. increases quadratically
D. increases exponentially

gate2008 computer-networks congestion-control normal

Answer

2.5.3 Congestion Control: GATE2012_45 top

http://gateoverflow.in/2156

Consider an instance of TCP's Additive Increase Multiplicative Decrease (AIMD) algorithm where the window size at the start of the slow start phase is 2 MSS and the threshold at the start of the first transmission is 8 MSS. Assume that a timeout occurs during the fifth transmission. Find the congestion window size at the end of the tenth transmission.

(A) 8 MSS
(B) 14 MSS
(C) 7 MSS
(D) 12 MSS

gate2012 computer-networks congestion-control normal

Answer

2.5.4 Congestion Control: GATE2014-1-27 top

http://gateoverflow.in/1794

Let the size of congestion window of a TCP connection be 32 KB when a timeout occurs. The round trip time of the connection is 100 msec and the maximum segment size used is 2 KB. The time taken **(in msec)** by the TCP connection to get back to 32 KB congestion window is __________.

gate2014-1 computer-networks tcp congestion-control numerical-answers normal

Answer

Answers: Congestion Control

2.5.1 Congestion Control: GATE2005-IT-73 top

http://gateoverflow.in/3836

Selected Answer

Ans should be (B)

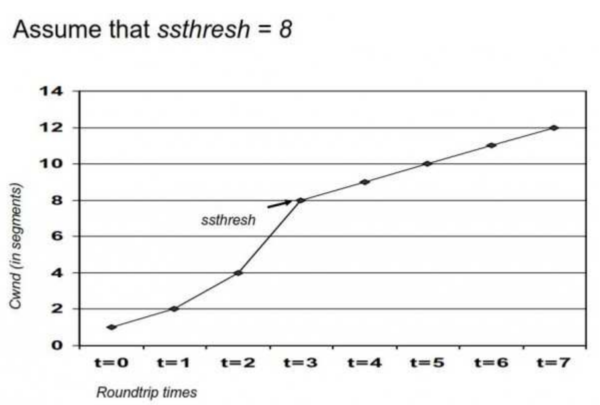
Current Sender window = min (Congestion Window, Advertised Window)= min(4KB, 6KB)= 4KB

29 votes -- srestha (58.4k points)

2.5.2 Congestion Control: GATE2008-56 top

http://gateoverflow.in/479

Selected Answer



increase is exponential in the Slow Start Phase.

answer = **option D**

9 votes -- Amar Vashishth (28.7k points)

2.5.3 Congestion Control: GATE2012_45 top

http://gateoverflow.in/2156

Selected Answer

The Answer is correct , but method of solving is wrong .

At

t=1, =>2mss

t=2, =>4mss

t=3, =>8mss

t=4, =>9mss (after threshold additive increase)

t=5, =>10mss (fails)

Threshold will be reduced by n/2 i.e. 10/2 = 5.

t=6, =>**1mss,**

(The window size is always = 1 mss after a time out irrespective of what value it started from, http://www.cs.ccsu.edu/~stan/classes/CS490/Slides/Networks4-Ch3-5.pdf **)**

t=7 =>2mss

t=8, =>4mss

t=9, =>5mss

t=10, =>6mss.

So **at the end of 10th sucessful transmission** ,the the congestion window size will be **(6+1) = 7mss.**

18 votes -- Harsh181996 (2.7k points)

At

t=1, =>2mss

t=2, =>4mss

t=3, =>8mss

t=4, =>9mss (after threshold additive increase)

t=5, =>10mss (fails)

Threshold will be reduced by n/2 i.e. 10/2 = 5.

t=6, =>2mss

t=7 =>4mss

t=8, =>5mss

t=9, =>6mss

t=10, =>7mss.

So at the end of 10th transmission congestion window size will be 8 mss.

24 votes -- Gate Keeda (19.1k points)

2.5.4 Congestion Control: GATE2014-1-27 top

http://gateoverflow.in/1794

Selected Answer

Ans: Given that at the time of **Time Out**, Congestion Window Size is $32KB$ and **RTT** = $100ms$,

When Time Out occurs, for the next round of Slow Start,

Threshold = $\frac{size\ of\ congestion\ window}{2}$,

Threshold = 16KB

Suppose we have a **slow start** ==>> $2KB \mid 4KB \mid 8KB \mid 16KB$ (As the threshold is reached, Additive increase starts) $\mid 18KB \mid 20KB \mid 22KB \mid 24KB \mid 26KB \mid 28KB \mid 30KB \mid 32KB$

Here | (vertical line) is representing **RTT** so the total number of vertical lines is $11 * 100ms$ ==>> $1100msec$ and so this is the answer...

👍 50 votes -- Jay (1.2k points)

2.6 Crc Polynomial(3) top

2.6.1 Crc Polynomial: GATE2005-IT-78 top http://gateoverflow.in/3842

Consider the following message M = 1010001101. The cyclic redundancy check (CRC) for this message using the divisor polynomial $x^5 + x^4 + x^2 + 1$ is :

A. 01110
B. 01011
C. 10101
D. 10110

gate2005-it computer-networks crc-polynomial normal

Answer

2.6.2 Crc Polynomial: GATE2007-68, ISRO2016-73 top http://gateoverflow.in/1266

The message 11001001 is to be transmitted using the CRC polynomial $x^3 + 1$ to protect it from errors. The message that should be transmitted is:

A. 11001001000

B. 11001001011

C. 11001010

D. 110010010011

gate2007 computer-networks error-detection crc-polynomial normal isro2016

Answer

2.6.3 Crc Polynomial: GATE2017-1-32 top http://gateoverflow.in/118313

A computer network uses polynomials over $GF(2)$ for error checking with 8 bits as information bits and uses $x^3 + x + 1$ as the generator polynomial to generate the check bits. In this network, the message 01011011 is transmitted as

(A) 01011011010

(B) 01011011011

(C) 01011011101

(D) 01011011100

gate2017-1 computer-networks crc-polynomial normal

Answer

Answers: Crc Polynomial

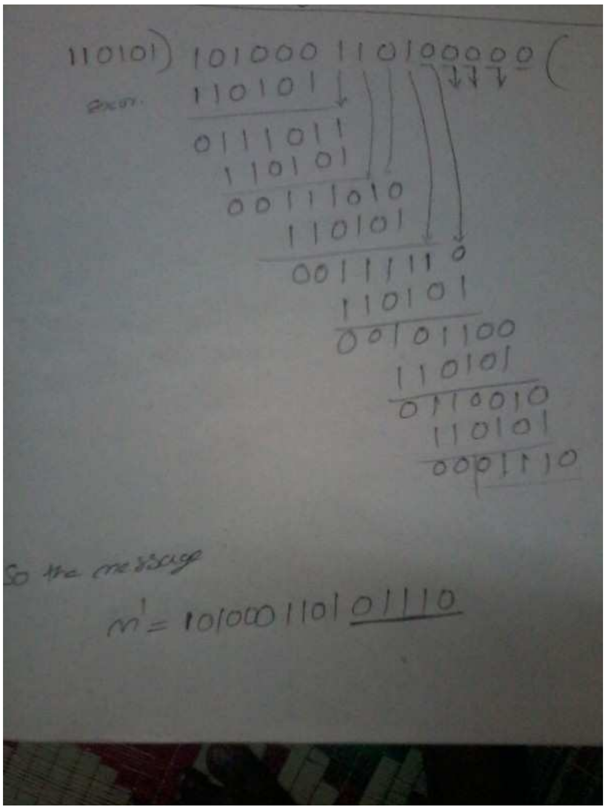
2.6.1 Crc Polynomial: GATE2005-IT-78 top http://gateoverflow.in/3842

Selected Answer

Answer: A

Divide 101000110100000 by 110101 to get 01110 as remainder. And as we know, remainder is the CRC.

👍 11 votes -- Rajarshi Sarkar (35k points)



crc calculation is

ans is a

👍 11 votes -- kvkumar (4.1k points)

2.6.2 Crc Polynomial: GATE2007-68, ISRO2016-73 top http://gateoverflow.in/1266

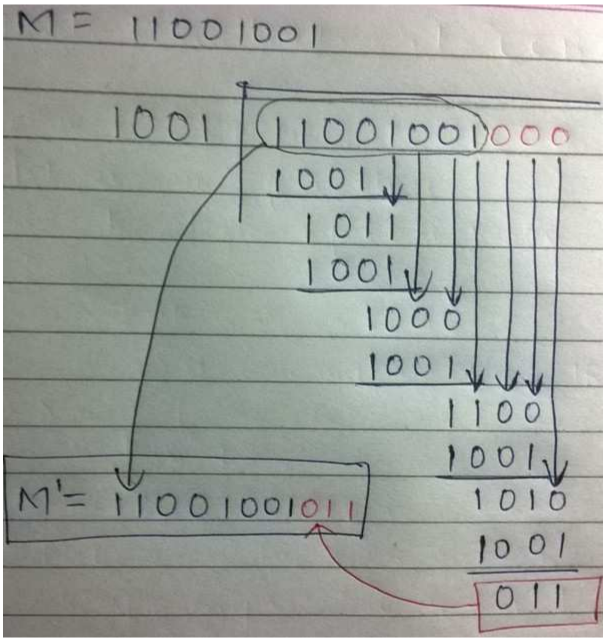
Selected Answer

answer - B

degree of generator polynomial is 3 hence 3 bits are appended before performing division

after performing division using 2's complement arithmetic remainder is 011

the remainder is appended to original data bits



By **Anurag Pandey**

14 votes -- ankitrokdeonsns (9.1k points)

2.6.3 Crc Polynomial: GATE2017-1-32 top

http://gateoverflow.in/118313

Selected Answer

Solution:

```
Message : 0 1 0 1 1 0 1 1
GF:   x^3 + x + 1 = 1 0 1 1

              0 1 0 0 0 0 1 1
           -----------------------
1 0  1 1 / 0 1 0 1 1 0 1 1 0 0 0
           0 0 0 0 | | | | | | |
           -------- | | | | | |
             1 0 1 1 | | | | | |
             1 0 1 1 | | | | | |
             -------- | | | | |
               0 0 0 0 1 1 0 0 |
                       1 0 1 1 |
                       --------
                         1 1 1 0
                         1 0 1 1
                         ------|
                           1 0 1 (remainder )
```

Answer: Message transmitted :0 1 0 1 1 0 1 1 **1 0 1** (OPTION C)

6 votes -- Smriti012 (3.1k points)

2.7 Cryptography(1) top

2.7.1 Cryptography: GATE 2016-2-23 top

http://gateoverflow.in/39555

Anarkali digitally signs a message and sends it to Salim. Verification of the signature by Salim requires.

A. Anarkali's public key.
B. Salim's public key.
C. Salim's private key.

D. Anarkali's private key.

gate2016-2 computer-networks network-security cryptography easy

Answer

Answers: Cryptography

2.7.1 Cryptography: GATE 2016-2-23 top

http://gateoverflow.in/39555

Selected Answer

In digital signature,
Alice/Anarkali/sender :P
First encrypts with **own private key** then again encrypts with Receivers/Bob/Salim's **Public key.**

Thus to decrypt, receiver will need **sender's/Anarkali's public key** after decrypting it with own/receiver's private key.

So answer is A !

23 votes -- Shashank Chavan (3.4k points)

2.8 Csma Cd(5) top

2.8.1 Csma Cd: GATE 2016-2-53 top

http://gateoverflow.in/39589

A network has a data transmission bandwidth of 20×10^6 bits per second. It uses **CSMA/CD** in the **MAC** layer. The maximum signal propagation time from one node to another node is 40 microseconds. The minimum size of a frame in the network is ___________ bytes.

gate2016-2 computer-networks csma-cd numerical-answers normal

Answer

2.8.2 Csma Cd: GATE2005-IT-27 top

http://gateoverflow.in/3773

Which of the following statements is TRUE about CSMA/CD

A. IEEE 802.11 wireless LAN runs CSMA/CD protocol
B. Ethernet is not based on CSMA/CD protocol
C. CSMA/CD is not suitable for a high propagation delay network like satellite network
D. There is no contention in a CSMA/CD network

gate2005-it computer-networks congestion-control csma-cd normal

Answer

2.8.3 Csma Cd: GATE2005-IT-71 top

http://gateoverflow.in/3834

A network with CSMA/CD protocol in the MAC layer is running at 1 Gbps over a 1 km cable with no repeaters. The signal speed in the cable is 2 x 10^8 m/sec. The minimum frame size for this network should be

A. 10000 bits
B. 10000 bytes
C. 5000 bits
D. 5000 bytes

gate2005-it computer-networks congestion-control csma-cd normal

Answer

2.8.4 Csma Cd: GATE2008-IT-65 top

http://gateoverflow.in/3376

The minimum frame size required for a CSMA/CD based computer network running at 1 Gbps on a 200m cable with a link speed of 2×10^8m/s is

A. 125 bytes
B. 250 bytes
C. 500 bytes
D. None of the above

gate2008-it computer-networks csma-cd normal

Answer

2.8.5 Csma Cd: GATE2015-3_6 top

http://gateoverflow.in/8400

Consider a CSMA/CD network that transmits data at a rate of 100 Mbps (10^8 bits per second) over a 1 km (kilometer) cable with no repeaters. If the minimum frame size required for this network is 1250 bytes, what is the signal speed (km/sec) in the cable?

A. 8000
B. 10000
C. 16000
D. 20000

gate2015-3 computer-networks congestion-control csma-cd normal

Answer

Answers: Csma Cd

2.8.1 Csma Cd: GATE 2016-2-53 top

http://gateoverflow.in/39589

Selected Answer

Since CSMA/CD
Transmission Delay = RTT
hence,
L=B $\times$RTT
L=B $\times 2 \times$ Tpropagation delay
L=$(20 \times 10^6) \times 2 \times 40 \times 10^{-6}$
=$20 \times 2 \times 40$
=1600bits
=200bytes
Hence 200Bytes is the answer.

16 votes -- Shashank Chavan (3.4k points)

2.8.2 Csma Cd: GATE2005-IT-27 top

http://gateoverflow.in/3773

Selected Answer

Answer->C

CSMA/CD was used in early days,802.3 not in 802.11

There will be contention in this protocol.

Ethernet is based on csma/cd early in 1980s,

👍 12 votes -- nagalla pruthvi (883 points)

2.8.3 Csma Cd: GATE2005-IT-71 top http://gateoverflow.in/3834

Selected Answer

Minimum frame size is needed to ensure that collisions are detected properly. The minimum frame size ensures that before a frame is completely send, it would be notified of any possible collision and hence collision detection works perfectly.

In CSMA/CD a sender won't send a packet if it senses that another sender is using it. So, assume a sender A and a receiver B. When sender sends a packet, receiver might use the cable until it is notified that a packet is being send to it. The receiver will be notified as soon as the first bit arrives that a packet is coming and it won't send any packet after this until that packet is finished. So, in the worst case for collision, receiver will transmit a packet back to the sender just before the first bit of the packet reaches it. (If t_d is the propagation delay of the channel, this time would be justt_d). In this case, surely there will be collision. But for the sender to detect it, it should be notified of B's packet before the sending of the first packet finishes. i.e., when B's packet arrives at A (takes another t_d time), A shouldn't have finished transmission of the first packet for it to detect a collision. i.e., A should be still continuing the sending of the packet in this time interval of $2 \times t_d$. Thus,

The amount of bits that can be transmitted by A in $2 \times t_d$ time should be less than the frame size (S) (sending of the frame shouldn't finish in this time)

Amount of bits transmitted in time t is $\text{bandwidth} \times t$ and propagation delay- t_d is $\frac{\text{distance}}{\text{link speed}}$

So, $S \geq 2 \times \text{bandwidth} \times t_d$

$\geq 2 \times 10^9 \times \frac{1000}{2 \times 10^8}$

≥ 10000 bits

👍 17 votes -- Arjun Suresh (294k points)

2.8.4 Csma Cd: GATE2008-IT-65 top http://gateoverflow.in/3376

Selected Answer

Minimum frame size is needed to ensure that collisions are detected properly. The minimum frame size ensures that before a frame is completely send, it would be notified of any possible collision and hence collision detection works perfectly.

In CSMA/CD a sender won't send a packet if it senses that another sender is using it. So, assume a sender A and a receiver B. When sender sends a packet, receiver might use the cable until it is notified that a packet is being send to it. The receiver will be notified as soon as the first bit arrives that a packet is coming and it won't send any packet after this until that packet is finished. So, in the worst case for collision, receiver will transmit a packet back to the sender just before the first bit of the packet reaches it. (If t_d is the propagation delay of the channel, this time would be justt_d). In this case, surely there will be collision. But for the sender to detect it, it should be notified of B's packet before the sending of the first packet finishes. i.e., when B's packet arrives at A (takes another t_d time), A shouldn't have finished transmission of the first packet for it to detect a collision. i.e., A should be still continuing the sending of the packet in this time interval of $2 \times t_d$. Thus,

The amount of bits that can be transmitted by A in $2 \times t_d$ time should be less than the frame size (S) (sending of the frame shouldn't finish in this time)

Amount of bits transmitted in time t is $\text{bandwidth} \times t$ and propagation delay- t_d is $\frac{\text{distance}}{\text{link speed}}$

So, $S \geq 2 \times \text{bandwidth} \times t_d$

$\geq 2 \times 10^9 \times \frac{200}{2 \times 10^8}$

≥ 2000 bits

≥ 250 bytes

👍 17 votes -- Arjun Suresh (294k points)

2.8.5 Csma Cd: GATE2015-3_6 top http://gateoverflow.in/8400

Selected Answer

For collision to be detected, the frame size should be such that the transmission time of the frame should be greater than twice the propagation delay (So, before the frame is completely sent, any possible collision will be discovered).

So, $1250 * 8 /(10^8) >= 2 * 1 / x$

$x = 2 * 10^4 = 20000$

18 votes -- Arjun Suresh (294k points)

2.9 Distance Vector Routing(6) top

2.9.1 Distance Vector Routing: GATE2005-IT-29 top http://gateoverflow.in/3775

Count to infinity is a problem associated with

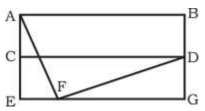
A. link state routing protocol.
B. distance vector routing protocol
C. DNS while resolving host name
D. TCP for congestion control

gate2005-it computer-networks routing distance-vector-routing normal

Answer

2.9.2 Distance Vector Routing: GATE2007-IT-60 top http://gateoverflow.in/3504

For the network given in the figure below, the routing tables of the four nodes A, E, D and G are shown. Suppose that F has estimated its delay to its neighbors, A, E, D and G as 8, 10, 12 and 6 msecs respectively and updates its routing table using distance vector routing technique.



Routing Table of A	
A	0
B	40
C	14
D	17
E	21
F	9
G	24

Routing Table of D	
A	20
B	8
C	30
D	0
E	14
F	7
G	22

Routing Table of E	
A	24
B	27
C	7
D	20
E	0
F	11
G	22

Routing Table of G	
A	21
B	24
C	22
D	19
E	22
F	10
G	0

A.

A	8
B	20
C	17
D	12

E	10
F	0
G	6

B.

A	21
B	8
C	7
D	19
E	14
F	0
G	22

C.

A	8
B	20
C	17
D	12
E	10
F	16
G	6

D.

A	8
B	8
C	7
D	12
E	10
F	0
G	6

gate2007-it computer-networks distance-vector-routing normal

Answer

2.9.3 Distance Vector Routing: GATE2010-54 top http://gateoverflow.in/2362

Consider a network with 6 routers R1 to R6 connected with links having weights as shown in the following diagram.

All the routers use the distance vector based routing algorithm to update their routing tables. Each router starts with its routing table initialized to contain an entry for each neighbour with the weight of the respective connecting link. After all the routing tables stabilize, how many links in the network will never be used for carrying any data?

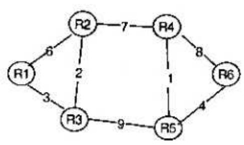
A. 4
B. 3
C. 2
D. 1

gate2010 computer-networks routing distance-vector-routing normal

Answer

2.9.4 Distance Vector Routing: GATE2010-55 top http://gateoverflow.in/43326

Consider a network with 6 routers R1 to R6 connected with links having weights as shown in the following diagram.



Suppose the weights of all unused links are changed to 2 and the distance vector algorithm is used again until all routing tables stabilize. How many links will now remain unused?

A. 0
B. 1

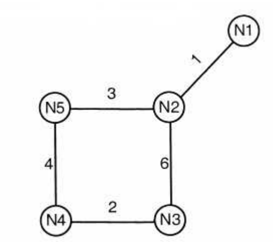
C. 2
D. 3

gate2010 computer-networks routing distance-vector-routing normal

Answer

2.9.5 Distance Vector Routing: GATE2011-52 top http://gateoverflow.in/2160

Consider a network with five nodes, N1 to N5, as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as following.

N1: (0, 1, 7, 8, 4)

N2: (1, 0, 6, 7, 3)

N3: (7, 6, 0, 2, 6)

N4: (8, 7, 2, 0, 4)

N5: (4, 3, 6, 4, 0)

Each distance vector is the distance of the best known path at that instance to nodes, N1 to N5, where the distance to itself is 0. Also all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link N2-N3 reduces to 2 (in both directions). After the next round of updates, what will be the new distance vector at node, N3?

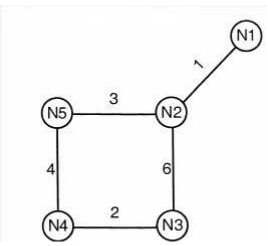
A. (3, 2, 0, 2, 5)
B. (3, 2, 0, 2, 6)
C. (7, 2, 0, 2, 5)
D. (7, 2, 0, 2, 6)

gate2011 computer-networks routing distance-vector-routing normal

Answer

2.9.6 Distance Vector Routing: GATE2011-53 top http://gateoverflow.in/43317

Consider a network with five nodes, N1 to N5, as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as following.

N1: (0, 1, 7, 8, 4)

N2: (1, 0, 6, 7, 3)

N3: (7, 6, 0, 2, 6)

N4: (8, 7, 2, 0, 4)

N5: (4, 3, 6, 4, 0)

Each distance vector is the distance of the best known path at that instance to nodes, N1 to N5, where the distance to itself is 0. Also all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link N2-N3 reduces to 2 (in both directions). After the next round of updates,the link N1-N2 goes down. N2 will reflect this change immediately in its distance vector as cost,
∞. After the **NEXT ROUND** of update, what will be the cost to N1 in the distance vector of N3?

A. 3
B. 9
C. 10
D. ∞

gate2011 computer-networks routing distance-vector-routing normal

Answer

Answers: Distance Vector Routing

2.9.1 Distance Vector Routing: GATE2005-IT-29 top http://gateoverflow.in/3775

Selected Answer

Answer->B

Distance vector routing

7 votes -- nagalla pruthvi (883 points)

2.9.2 Distance Vector Routing: GATE2007-IT-60 top http://gateoverflow.in/3504

Selected Answer

Answer: A

Distance from F to F is 0 which eliminates option C.

Using distance vector routing protocol, F -> D -> B yields distance as 20 which eliminates option B and D.

17 votes -- Rajarshi Sarkar (35k points)

2.9.3 Distance Vector Routing: GATE2010-54 top http://gateoverflow.in/2362

Selected Answer

Answer (C)

Following will be distance vectors of all nodes.

Shortest Distances from R1 to R2, R3, R4, R5 and R6
R1 (5, 3, 12, 12, 16)
Links used: R1-R3, R3-R2, R2-R4, R3-R5, R5-R6

Shortest Distances from R2 to R3, R4, R5 and R6
R2 (2, 7, 8, 12)
Links used: R2-R3, R2-R4, R4-R5, R5-R6

Shortest Distances from R3 to R4, R5 and R6
R3 (9, 9, 13)
Links used: R3-R2, R2-R4, R3-R5, R5-R6

Shortest Distances from R4 to R5 and R6
R4 (1, 5)
Links used: R4-R5, R5-R6

Shortest Distance from R5 to R6
R5 (4)
Links Used: R5-R6

If we mark, all the used links one by one, we can see that following links are never used.
R1-R2
R4-R6

11 votes -- pC (21.4k points)

C is the right answer.. The links R1-R2 and R4-R6 will never be used for data transfer because there are shorter paths available in any case.

16 votes -- Hunaif (485 points)

2.9.4 Distance Vector Routing: GATE2010-55 top http://gateoverflow.in/43326

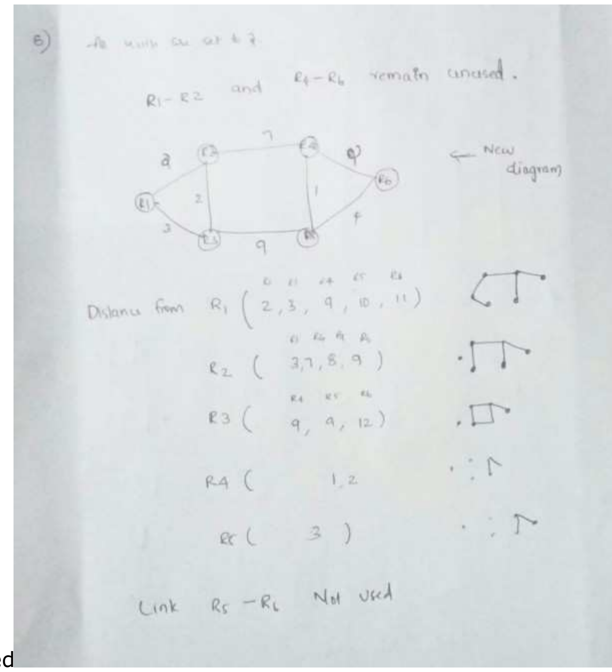
Selected Answer

First we need to find which are the unused links in the graph
For that we need not make distance vector tables,
We can do this by simply looking into the graph or else DVT can also give the answer.
So, R1-R2 and R4-R6 will remain unused.

Now If We changed the unused links to value 2.
R5-R6 will Now remain unused.

So the Correct answer is option B)

13 votes -- saif ahmed (3.8k points)



Only one link is not used

11 votes -- pC (21.4k points)

2.9.5 Distance Vector Routing: GATE2011-52 top http://gateoverflow.in/2160

Selected Answer

Q:52 Answer is (A)

1. As soon as N2-N3 reduces to 2,both N2 and N3 instantly updates their distance to N3 and N2 to 2 respectively. So N2: (1, 0, 2, 7, 3), N3: (7, 2, 0, 2, 6) becomes this.

After this starts first round of update in which each node shares its table with their respective neighbors ONLY. BUT KEEP IN MIND THAT ONLY OLD TABLES WILL BE SHARED.What I mean is tables that will be used for updation at this moment contain the values as N1: (0, 1, 7, 8, 4),N2: (1, 0, 2, 7, 3),N3: (7, 2, 0, 2, 6),N4: (8, 7, 2, 0, 4),N5: (4, 3, 6, 4, 0).

SEE at this time all the entries are old EXCEPT in N2 and N3 where value changes to 2 instead of 6.

Question asks for N3. So focus on that.

N3 receives tables from N2: (1, 0, 2, 7, 3) and N4: (8, 7, 2, 0, 4). Using THIS ONLY original N3: (7, 2, 0, 2, 6) updates to N3(3,2,0,2,5) .(For updation and forming the tables for this refer FOROUZAN.)

So answer is (A).

24 votes -- Sandeep_Uniyal (7.3k points)

2.9.6 Distance Vector Routing: GATE2011-53 top http://gateoverflow.in/43317

Selected Answer

First, as soon as N1-N2 goes down, N2 and N1 both update that entry in their tables as infinity.So N2 at this moment will be N2(inf,0,2,_,_). I have left blank coz that details are not important.

Now for N3 to get updated in the subsequent round it will get tables from N2 and N4 only. But first we need to find the N4 calculated in previous update. So in previous question N4 received updates from N3 and N5 which are N3: (7, 6, 0, 2, 6),N5: (4, 3, 6, 4, 0).

NOW THIS IS VERY IMPORTANT AS WHY N4 DID NOT GET UPDATED TABLES FROM N3. SO ANSWER IS THAT these tables were shared at the same moment and so in a particular round of update old values of all the tables are used and not the updated values.

N3 was updates AFTER IT PASSED ITS OLD table to its neighbors AS WHY WOULD N4 WAIT FOR N3 to GET UPDATED first !!! **So N4 will update its table (in prev question) to N4(8,7,2,0,4).**

See here path to N1 exists via N5 and not via N3 bcoz when table was shared by N3 it contained path to N1 as 7 and N1 via N3 sums to 7+2 =9 . Now when N3 receives tables from N2(inf,0,_,_,_) and N4(8,7,2,0,4).

At first it will see its distance to N1 as "Inf" and NOT 3 because "inf" is the new distance with the same Next hop N2**(If next hop is same, new entry is updated even though it is larger than previous entry for the same NEXT HOP).**

But at the same time it sees distance to N1 from N4 as 8 and so updates with the value (N3-N4 + N4-N1)= (2+8)=10. So N3-N1 distance in N3(10,_,0,_,_) is 10.

So answer is (C)

Ref: http://www.cs.princeton.edu/courses/archive/spr11/cos461/docs/lec14-distvector.pdf

12 votes -- Sandeep_Uniyal (7.3k points)

2.10 Dns(1) top

2.10.1 Dns: GATE2005-IT-77 top http://gateoverflow.in/3840

Assume that "host1.mydomain.dom" has an IP address of 145.128.16.8. Which of the following options would be most appropriate as a subsequence of steps in performing the reverse lookup of 145.128.16.8? In the following options "NS" is an abbreviation of "nameserver".

A. Query a NS for the root domain and then NS for the "dom" domains
B. Directly query a NS for "dom" and then a NS for "mydomain.dom" domains
C. Query a NS for in-addr.arpa and then a NS for 128.145.in-addr.arpa domains
D. Directly query a NS for 145.in-addr.arpa and then a NS for 128.145.in-addr.arpa domains

gate2005-it computer-networks normal dns

Answer

Answers: Dns

2.10.1 Dns: GATE2005-IT-77 top

http://gateoverflow.in/3840

Selected Answer

Answer is C)

A & B are clearly wrong as we are doing Reverse lookup.

C is most closest answer to process given in RFC 1033. We need to get NS for in-addr.arpa before doing query to 8.16.128.145.in-addr.arpa

D is not correct, it is not close to process.

Relevant stuff From https://tools.ietf.org/html/rfc1033 ==>

```
IN-ADDR.ARPA

   The structure of names in the domain system is set up in a
   hierarchical way such that the address of a name can be found by
   tracing down the domain tree contacting a server for each label of
   the name.  Because of this 'indexing' based on name, there is no easy
   way to translate a host address back into its host name.

   In order to do the reverse translation easily, a domain was created
   that uses hosts' addresses as part of a name that then points to the
   data for that host.  In this way, there is now an 'index' to hosts'
   RRs based on their address.  This address mapping domain is called
   IN-ADDR.ARPA.  Within that domain are subdomains for each network,
   based on network number.  Also, for consistency and natural
   groupings, the 4 octets of a host number are reversed.

   For example, the ARPANET is net 10.  That means there is a domain
   called 10.IN-ADDR.ARPA.  Within this domain there is a PTR RR at
   51.0.0.10.IN-ADDR that points to the RRs for the host SRI-NIC.ARPA
   (who's address is 10.0.0.51).  Since the NIC is also on the MILNET
   (Net 26, address 26.0.0.73), there is also a PTR RR at 73.0.0.26.IN-
   ADDR.ARPA that points to the same RR's for SRI-NIC.ARPA.  The format
   of these special pointers is defined below along with the examples
   for the NIC.

 The PTR record is used to let special names point to some other
   location in the domain tree.  They are mainly used in the IN-
   ADDR.ARPA records for translation of addresses to names.  PTR's
   should use official names and not aliases.

   For example, host SRI-NIC.ARPA with addresses 10.0.0.51 and 26.0.0.73
   would have the following records in the respective zone files for net
   10 and net 26:

           51.0.0.10.IN-ADDR.ARPA.  PTR   SRI-NIC.ARPA.
           73.0.0.26.IN-ADDR.ARPA.  PTR   SRI-NIC.ARPA.
```

8 votes

-- Akash (43.8k points)

2.11 Encoding(1) top

2.11.1 Encoding: GATE2006-IT-65 top

http://gateoverflow.in/3609

In the 4B/5B encoding scheme, every 4 bits of data are encoded in a 5-bit codeword. It is required that the codewords have at most 1 leading and at most 1 trailing zero. How many such codewords are possible?

A. 14
B. 16
C. 18
D. 20

gate2006-it computer-networks encoding permutations-and-combinations normal

Answer

Answers: Encoding

2.11.1 Encoding: GATE2006-IT-65 top

http://gateoverflow.in/3609

Selected Answer

Answer is (C)

It says we have 5 bit codeword such that "it can't have two consecutive zeros in first and second bit" and also" can't have two consecutive zeros in last two bits.

Code word with first two bits zero = 0|0|x|x|x| =8

Code word with last two bits zero = |x|x|x|0|0| =8

Code word with first and last two bits zero = 0|0|x|0|0| =2

Code word with first OR last two bits zero = 8+8-2=14

Therefore possible codewords =32-14 =18

15 votes -- Sandeep_Uniyal (7.3k points)

2.12 Error Detection(6) top

2.12.1 Error Detection: GATE1992_01,ii top

http://gateoverflow.in/546

Consider a 3-bit error detection and 1-bit error correction hamming code for 4-bit datq. The extra parity bits required would be ____ and the 3-bit error detection is possible because the code has a minimum distance of _____

gate1992 computer-networks error-detection normal

Answer

2.12.2 Error Detection: GATE1995_1.12 top

http://gateoverflow.in/2599

What is the distance of the following code 000000, 010101, 000111, 011001, 111111?

A. 2
B. 3
C. 4
D. 1

gate1995 computer-networks error-detection normal

Answer

2.12.3 Error Detection: GATE2005-IT-74 top

http://gateoverflow.in/3837

In a communication network, a packet of length L bits takes link L_1 with a probability of p_1 or link L_2 with a probability of p_2. Link L_1 and L_2 have bit error probability of b_1 and b_2 respectively. The probability that the packet will be received without error via either L_1 or L_2 is

A. $(1-b_1)^L p_1 + (1-b_2)^L p_2$
B. $[1-(b_1+b_2)^L] p_1 p_2$
C. $(1-b_1)^L (1-b_2)^L p_1 p_2$
D. $1-(b_1^L p_1 + b_2^L p_2)$

gate2005-it computer-networks error-detection probability normal

Answer

2.12.4 Error Detection: GATE2007-IT-43 top http://gateoverflow.in/3478

An error correcting code has the following code words: 00000000, 00001111, 01010101, 10101010, 11110000. What is the maximum number of bit errors that can be corrected?

A. 0
B. 1
C. 2
D. 3

gate2007-it computer-networks error-detection normal

Answer

2.12.5 Error Detection: GATE2008-IT-66 top http://gateoverflow.in/3380

Data transmitted on a link uses the following $2D$ parity scheme for error detection:
Each sequence of 28 bits is arranged in a 4×7 matrix (rows r_0 through r_3, and columns d_7 through d_1) and is padded with a column d_0 and row r_4 of parity bits computed using the Even parity scheme. Each bit of column d_0 (respectively, row r_4) gives the parity of the corresponding row (respectively, column). These 40 bits are transmitted over the data link.

	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
r_0	0	1	0	1	0	0	1	**1**
r_1	1	1	0	0	1	1	1	**0**
r_2	0	0	0	1	0	1	0	**0**
r_3	0	1	1	0	1	0	1	**0**
r_4	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**

(Ctrl)

The table shows data received by a receiver and has n corrupted bits. What is the minimum possible value of n?

A. 1
B. 2
C. 3
D. 4

gate2008-it computer-networks normal error-detection

Answer

2.12.6 Error Detection: GATE2009-48 top http://gateoverflow.in/1334

Let $G(x)$ be the generator polynomial used for CRC checking. What is the condition that should be satisfied by $G(x)$ to detect odd number of bits in error?

A. $G(x)$ contains more than two terms
B. $G(x)$ does not divide $1+x^k$, for any k not exceeding the frame length
C. $1+x$ is a factor of $G(x)$
D. $G(x)$ has an odd number of terms.

gate2009 computer-networks error-detection normal

Answer

Answers: Error Detection

2.12.1 Error Detection: GATE1992_01,ii top

http://gateoverflow.in/546

Selected Answer

The Hamming distance between two bit strings is the number of bits that would have to flip to make the strings identical.

To **detect d errors** requires a minimum Hamming distance of d + 1 .

Correcting d bit flips requires a minimum Hamming distance of 2 * d + 1 , where d is number of bit in errors .

For the first blank , each error detection we need 1 parity bit

for 3 bit error detection we need 3 parity bit ...... So, 3 parity bit requires here. answer is 3.

Also we can calculate this way, formula is d+p+1 <= 2^p where d=data bits , p = parity bits , d=4 bit given.

according to 1st question, d= 4 so 4+p+1<= 2^p

p+5 <= 2^p now if p=2 it becomes 7 <= 4 , Not satisfy . p = 3 it becomes 8 <= 8 , satisfy.

so p must be 3 .[Minimum value of p is 3]

The second blank the 3-bit error detection is possible because the code has a minimum distance of ____ answer is 3+1=4, where d=3. Formula used d+1.

Answer for 2 blanks are [3,4]

2 votes -- Bikram (44.7k points)

let minimum Hamming distance is t.
so with this hamming distance t-1 bit error detection as well as (t-1)/2 bit error correction is possible..

for 3 bit error detection minimum Hamming distance = 3+1 =4
for 1 bit error correction minimum Hamming distance = 2*1+1 = 3
no of parity bits = p
p + t + 1 <= 2^p
p + 4 +1 <= 2^p
p=3

12 votes -- Digvijay (47k points)

2.12.2 Error Detection: GATE1995_1.12 top

http://gateoverflow.in/2599

Selected Answer

Distance (also called min-distance) of a block code is the minimum number of positions in which any two distinct codes differ. Here, min-distance occurs for the codes 2 and 3 and they differ only in 2 positions. So, d = 2.

https://en.wikipedia.org/wiki/Block_code

16 votes -- Arjun Suresh (294k points)

2.12.3 Error Detection: GATE2005-IT-74 top

http://gateoverflow.in/3837

Selected Answer

Probability of choosing link $L_1 = p_1$

Probability for no bit error (for any single bit)= $(1 - b_1)$

Similarly for link L_2

Probability of no bit error $= (1 - b_2)$

Packet can go either through link L_1 or L_2 they are mutually exclusive events (means one event happens other won't be happening and so we can simply add their respective probabilities for the favorable case).

Probability packet will be received without any error = Probability of L_1 being chosen and no error in any of the L bits + Probability of L_2 being chosen and no error in any of the L bits

$= (1 - b_1)^L p_1 + (1 - b_2)^L p_2.$

Hence answer is option A .

Why option D is not correct choice here ?

Option D here is giving the probability of a frame being arrived with at least one bit correctly - i.., all the bits are not errors.

👍 24 votes -- Pooja Palod (32.4k points)

2.12.4 Error Detection: GATE2007-IT-43 top http://gateoverflow.in/3478

Selected Answer

Answer: B

For correction: Floor of [(Hamming Distance - 1)/2] = Floor of [1.5] = 1 bit error.

For detection: Hamming Distance - 1 = 3 bit error.

👍 18 votes -- Rajarshi Sarkar (35k points)

2.12.5 Error Detection: GATE2008-IT-66 top http://gateoverflow.in/3380

Selected Answer

	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
r_0	0	1	0	1	0	0	1	1
r_1	1	1	**1**	0	1	1	1	0
r_2	0	0	0	1	0	1	0	0
r_3	0	1	1	0	1	0	1	0
r_4	1	1	0	0	0	**0**	1	**1**

Here we need t o change minmum 3 bits, so by doing it correct we get correct parity column wise and row wise (Correction marked by dark number).

C is answer

👍 11 votes -- Prashant Singh (49.2k points)

2.12.6 Error Detection: GATE2009-48 top http://gateoverflow.in/1334

Selected Answer

Let me first explain building blocks to this problem. Before answering this, we should know the relationship between Sent codeword, Received codeword, CRC generator and error polynomial.

let's take an example:

Sent codeword = 10010 $(=x^4+x)$

Received codeword = 10**1**10 (error at 2nd bit) $(=x^4+x^2+x)$

Now, i can write **Sent codeword = Received codeword + error** (10010 = 10**1**10 + 00100, here we do modulo 2 arithmetic i.e 1+1 =0 without carry)

in polynomial also we can see x^4+x = x^4+x^2+x**+**x^2 = x^4+**2**x^2+x = **x^4+x (here multiplier with 2 means 0** bcoz it coressopnds to binary modulo 2 arithmetic **which is 1+1 = 0** (not 2) **)**

OR

We can also write **Received codeword = Sent codeword + error** (Check it using same mrthod as above)

Sent codeword C(x), Received codeword R(x) and error E(x).

Now we have R**(x) = C(x) + E(x)**. and let CRC polynomial be G**(x)**. G(x) always divides C(x), and if there is an error then G(x) should not divide R(x). Lets check -

R(x) mod G(x) =**(**C(x) + E(x)**)** mod G(x) (for simplicity i am writing mod as division)

$$\frac{R(x)}{G(x)} = \frac{C(x)}{G(x)} + \frac{E(x)}{G(x)} \quad G(x) \text{ always divides } C(x)$$

$$\Rightarrow \frac{R(x)}{G(x)} = 0 + \frac{E(x)}{G(x)}$$

If G(x) divides E(x) also this would mean G(x) divides R(x). We know that, If G(x) does not properly divide R(x) then there is an error but we are never sure if there is error or not when G(x) divides R(X).

As we saw, G(x) divides R(x) or not totally depends on G(x) divides E(x) or not. whole strength of G(x) lies if it does not divide any possible E(x).

Lets see again E(x). if there is an error in 3rd and 4th bit from left (LSb is 0th bit) then E(X) = x^4+x^3.(it does not matter error is from toggling 1 to 0 or 0 to 1) Check with above example.

Now come to question. it says G(x) should detect odd number of bits in error?. If number of bits are odd then terms in E(x) would be odd.

for instance if 1st, 2nd and 5th bit got corrupted then E(x) = x^5+x^2+x.

It is clear that if any function $f(x)$ has a factor of x-k, then at x=k, $f(x)$ would be zero. I.e. $f(x) = 0$ at x=k.

- We want to detect odd number of bits that means received message R(x) contains an odd number of inverted bits, then E(x) must contain an odd number of terms with coefficients equal to 1.
- As a result, E(1) must equal to 1 (remeber 1+1 = 0, 1+1+1 = 1. Any Odd number of times sum of one's is = 1). E(1) is not zero, this means x+1 is not a factor of E(x).
- Now I want G(x) not to be a factor of E(x), So that G(x) wont divide E(x) and i would happily detect odd number of bits.
- So, if we make sure that G(1) = 0, we can conclude that G(x) does not divide any E(x) corresponding to an odd number of error bits. In this case, a CRC based on G(x) will detect any odd number of errors.
- As long as $1 + x$ is a factor of G(x), G(x) can never divide E(x). Because we know E(x) dont have factor of $1 + x$.

Option **C**.

(Option B might confuse you, If G(x) has some factor of the form $x^k + 1$ then also G(x) would detect all odd number of errors, But in Option B, language is changed, and that too we should not have any upper bound on k.)

15 votes -- Sachin Mittal (7.1k points)

2.13 Ethernet(4) top

2.13.1 Ethernet: GATE 2016-2-24 top

http://gateoverflow.in/39543

In an Ethernet local area network, which one of the following statements is **TRUE**?

A. A station stops to sense the channel once it starts transmitting a frame.
B. The purpose of the jamming signal is to pad the frames that are smaller than the minimum frame size.
C. A station continues to transmit the packet even after the collision is detected.
D. The exponential back off mechanism reduces the probability of collision on retransmissions.

gate2016-2 computer-networks ethernet normal

Answer

2.13.2 Ethernet: GATE2004-54 top http://gateoverflow.in/1050

A and B are the only two stations on an Ethernet. Each has a steady queue of frames to send. Both A and B attempt to transmit a frame, collide, and A wins the first backoff race. At the end of this successful transmission by A, both A and B attempt to transmit and collide. The probability that A wins the second backoff race is

A. 0.5
B. 0.625
C. 0.75
D. 1.0

gate2004 computer-networks ethernet probability normal

Answer

2.13.3 Ethernet: GATE2006-IT-19 top http://gateoverflow.in/3558

Which of the following statements is TRUE?

A. Both Ethernet frame and IP packet include checksum fields
B. Ethernet frame includes a checksum field and IP packet includes a CRC field
C. Ethernet frame includes a CRC field and IP packet includes a checksum field
D. Both Ethernet frame and IP packet include CRC fields

gate2006-it computer-networks normal ethernet

Answer

2.13.4 Ethernet: GATE2013_36 top http://gateoverflow.in/1547

Determine the maximum length of the cable (in km) for transmitting data at a rate of 500 Mbps in an Ethernet LAN with frames of size 10,000 bits. Assume the signal speed in the cable to be 2,00,000 km/s.

(A) 1 (B) 2 (C) 2.5 (D) 5

gate2013 computer-networks ethernet normal

Answer

Answers: Ethernet

2.13.1 Ethernet: GATE 2016-2-24 top http://gateoverflow.in/39543

Selected Answer

On Ethernet

A) This is false because station need not stop to listen to stuff !

B) No, this is not purpose of jamming singlal.

C) No, stations sends jamming signal if collusion is detected. This is reason why B is false.

So answer is D)

12 votes -- Akash (43.8k points)

2.13.2 Ethernet: GATE2004-54 top http://gateoverflow.in/1050

Selected Answer

Find this solution.

In Ethernet networks, the Exponential back-off algorithm is commonly used to schedule re-transmissions after collisions. This algorithm gives waiting time for the stations that are involved in collision.
Waiting time for station = k x 51ms
K is randomly chosen from 0 to 2^n-1 where n= no of collisions a station is involved.
51ms is a generic RTT for a standard Ethernet.

Station A and Station both try to access a link at the same time. Since they detect a collision, A waits for a random time between 0 and 1 time units and so does B. It's given that A wins the first back-off race. Hence A has no need to wait and begins to use the link and B waits for 1 x 51ms (k=1 is the number selected by B according to the algorithm). At the end of this successful transmission by A, both A and B attempts to transmit, and collide. A will once again choose a random back-off time between 0 and 1, but B will choose a back-off time between 0 and 3 - because this is his second time colliding in a row.

Value of K selected by A	Value of K selected by B	Winner
0	0	X
0	1	A
0	2	A
0	3	A
1	0	B
1	1	X
1	2	A
1	3	A

Hence A has 5 chances to win out of 8 combinations.
Therefore that A wins the second backoff race = 5/8 = 0.625

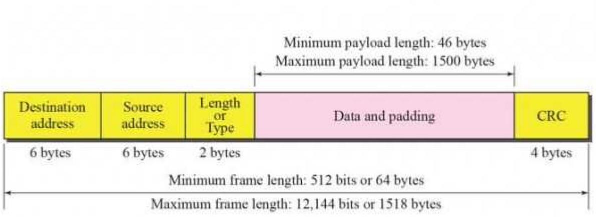
24 votes -- Bijendra Behera (171 points)

2.13.3 Ethernet: GATE2006-IT-19 top

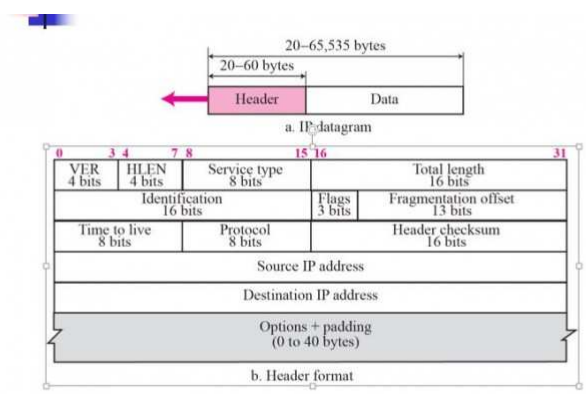
http://gateoverflow.in/3558

Selected Answer

Ethernet frame



IP packet



5 votes -- Prateek kumar (6k points)

2.13.4 Ethernet: GATE2013_36 top

http://gateoverflow.in/1547

Selected Answer

$$\begin{aligned}
\text{transmission time} &\geq \text{round trip time of 1 bit} \\
\text{transmission time} &\geq 2 \times \text{propagation time} \\
\frac{10,000\ bits}{500\ Mbps} &\geq 2 \times \frac{d}{2 \times 10^5 \text{ km per sec}} \\
2 \text{ km} &\geq d
\end{aligned}$$

option B is correct

15 votes -- Amar Vashishth (28.7k points)

2.14 Firewall(1) top

2.14.1 Firewall: GATE2011_2 top

http://gateoverflow.in/2104

A layer-4 firewall (a device that can look at all protocol headers up to the transport layer)**CANNOT**

A. block entire HTTP traffic during 9:00PM and 5:00AM
B. block all ICMP traffic
C. stop incoming traffic from specific IP address but allow outgoing traffic to the same IP address
D. block TCP traffic from a specific user on a multi-user system during 9:00PM to 5:00AM

gate2011 computer-networks network-security firewall normal

Answer

Answers: Firewall

2.14.1 Firewall: GATE2011_2 top

http://gateoverflow.in/2104

Selected Answer

Answer is (D).

(A) It is POSSIBLE to block "entire" HTTP traffic by blocking all the traffic on port number 80 Since here we DON'T need to check anything that is application layer specific. We only need to block port no 80 for required time span.

(B) & (C) are fairly possible to achieve.

(D) However (D) is not possible to achieve although the service uses TCP at transport layer. But see the question. We dont need to block entire TCP traffic so we cant block any specific PORT number. Also it is given that IT IS MULTI- USER System and so many user may be using same port for communication. Therefore blocking that port would block all the users WHILE we want a specific user. So how to do that. To do so we need Application layer specific information of the user like user_id type of things which cant be checked as it is 4-layer firewall.

So it is not possible to allow other users and block some specific at the same time using a 4-layer firewall (unless they all be using different port numbers which we actually cant predict).

32 votes -- Sandeep_Uniyal (7.3k points)

2.15 Hamming Code(1) top

2.15.1 Hamming Code: GATE1994_9 top

http://gateoverflow.in/2505

Following 7 bit single error correcting hamming coded message is received.

7	6	5	4	3	2	1	bit No.
1	0	0	0	1	1	0	

Determine if the message is correct (assuming that at most 1 bit could be corrupted). If the message contains an error find the bit which is erroneous and gives correct message.

gate1994 computer-networks error-detection hamming-code normal

Answer

Answers: Hamming Code

2.15.1 Hamming Code: GATE1994_9 top http://gateoverflow.in/2505

Selected Answer

Here Answer is yes. There is error in This message. Error is in bit 6.

How to calculate it ? First of all reverse given input to get it in correct position from 1 to 7.

0110001

Bit 1, Bit 2 & Bit 4 are partity bits.

Calculating position of error =>

c3 c2 c1

1 1 0

Here c1 = bit4⊕bit5⊕bit6⊕bit7=0⊕0⊕0⊕1=1 (Taking Even parity)

c2 = bit2⊕bit3⊕bit6⊕bit7=1⊕1⊕0⊕1=1

c3 = bit1⊕bit3⊕bit5⊕bit7=0⊕1⊕0⊕1=0

Ref -> https://en.wikipedia.org/wiki/Hamming%287,4%29

When you correct bit 6 .

You get message as 0110011.

IF you calculate C1,c2,c3 all will be 0 now !

6 votes -- Akash (43.8k points)

2.16 Huffman Code(1) top

2.16.1 Huffman Code: GATE2017-2-50 top http://gateoverflow.in/118395

A message is made up entirely of characters from the set $X = \{P, Q, R, S, T\}$. The table of probabilities for each of the characters is shown below:

Character	Probability
P	0.22
Q	0.34
R	0.17
S	0.19
T	0.08

Total	1.00

If a message of 100 characters over X is encoded using Huffman coding, then the expected length of the encoded message in bits is _______.

gate2017-2 huffman-code numerical-answers

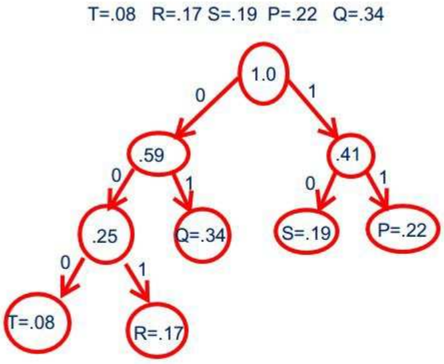
Answer

Answers: Huffman Code

2.16.1 Huffman Code: GATE2017-2-50 top

http://gateoverflow.in/118395

Selected Answer



no of bit required for each alphbet:
T=3bit, R=3bit, Q=2bit, S=2bit, P=2bit
agv length/char=no of bit* frequency of occurance of each alphabet
=3*.08+3*.17+2*.34+2*.19+2*.22=2.25bits
so for 100 char=2.25*100=225bits

so ans is 225

11 votes

-- 2018 (5.2k points)

2.17 Icmp(1) top

2.17.1 Icmp: GATE2005-IT-26 top

http://gateoverflow.in/3772

Traceroute reports a possible route that is taken by packets moving from some host A to some other host B. Which of the following options represents the technique used by traceroute to identify these hosts

A. By progressively querying routers about the next router on the path to B using ICMP packets, starting with the first router

B. By requiring each router to append the address to the ICMP packet as it is forwarded to B. The list of all routers en-route to B is returned by B in an ICMP reply packet

C. By ensuring that an ICMP reply packet is returned to A by each router en-route to B, in the ascending order of their hop distance from A

D. By locally computing the shortest path from A to B

gate2005-it computer-networks icmp application-layer-protocols normal

Answer

Answers: Icmp

2.17.1 Icmp: GATE2005-IT-26 top
http://gateoverflow.in/3772

Selected Answer

A) Traceroute works by sending packets with gradually increasing TTL value, starting with TTL value of 1. The first router receives the packet, decrements the TTL value and drops the packet because it then has TTL value zero. The router sends an ICMP Time Exceeded message back to the source. The next set of packets are given a TTL value of 2, so the first router forwards the packets, but the second router drops them and replies with ICMP Time Exceeded. Proceeding in this way, traceroute uses the returned ICMP Time Exceeded messages to build a list of routers that packets traverse, until the destination is reached and returns an ICMP Echo Reply message

16 votes -- Shaun Patel (6.9k points)

2.18 Ip Packet(7) top

2.18.1 Ip Packet: GATE 2016-1-53 top
http://gateoverflow.in/39712

An IP datagram of size 1000 bytes arrives at a router. The router has to forward this packet on a link whose MTU (maximum transmission unit) is 100 bytes. Assume that the size of the IP header is 20 bytes.

The number of fragments that the IP datagram will be divided into for transmission is_________.

gate2016-1 computer-networks ip-packet normal numerical-answers

Answer

2.18.2 Ip Packet: GATE2004-IT-86 top
http://gateoverflow.in/3730

In the TCP/IP protocol suite, which one of the following is NOT part of the IP header?

A. Fragment Offset
B. Source IP address
C. Destination IP address
D. Destination port number

gate2004-it computer-networks ip-packet normal

Answer

2.18.3 Ip Packet: GATE2010-15 top
http://gateoverflow.in/2188

One of the header fields in an IP datagram is the Time-to-Live (TTL) field. Which of the following statements best explains the need for this field?

A. It can be used to prioritize packets.
B. It can be used to reduce delays.
C. It can be used to optimize throughput.
D. It can be used to prevent packet looping.

gate2010 computer-networks ip-packet easy

Answer

2.18.4 Ip Packet: GATE2014-3-25 top
http://gateoverflow.in/2059

Host A (on TCP/IP v4 network A) sends an IP datagram D to host B (also on TCP/IP v4 network B). Assume that no error occurred during the transmission of D. When D reaches B, which of the following IP header field(s) may be different from that of the original datagram D?

i. TTL
ii. Checksum
iii. Fragment Offset

A. i only
B. i and ii only
C. ii and iii only
D. i, ii and iii

gate2014-3 computer-networks ip-packet normal

Answer

2.18.5 Ip Packet: GATE2014-3-28 top http://gateoverflow.in/2062

An IP router with a Maximum Transmission Unit (MTU) of 1500 bytes has received an IP packet of size 4404 bytes with an IP header of length 20 bytes. The values of the relevant fields in the header of the third IP fragment generated by the router for this packet are

A. MF bit: 0, Datagram Length: 1444; Offset: 370
B. MF bit: 1, Datagram Length: 1424; Offset: 185
C. MF bit: 1, Datagram Length: 1500; Offset: 370
D. MF bit: 0, Datagram Length: 1424; Offset: 2960

gate2014-3 computer-networks ip-packet normal

Answer

2.18.6 Ip Packet: GATE2015-1_22 top http://gateoverflow.in/8220

Which of the following fields of an IP header is NOT modified by a typical IP router?

A. Check sum
B. Source address
C. Time to Live (TTL)
D. Length

gate2015-1 computer-networks ip-packet easy

Answer

2.18.7 Ip Packet: GATE2015-2_52 top http://gateoverflow.in/8255

Host A sends a UDP datagram containing 8880 bytes of user data to host B over an Ethernet LAN. Ethernet frames may carry data up to 1500 bytes (i.e. MTU = 1500 bytes). Size of UDP header is 8 bytes and size of IP header is 20 bytes. There is no option field in IP header. How many total number of IP fragments will be transmitted and what will be the contents of offset field in the last fragment?

A. 6 and 925
B. 6 and 7400
C. 7 and 1110
D. 7 and 8880

gate2015-2 computer-networks ip-packet normal

Answer

Answers: Ip Packet

2.18.1 Ip Packet: GATE 2016-1-53 top http://gateoverflow.in/39712

Selected Answer

MTU (M) is 80 + 20bytes

Datagram size (DS) is 980 + 20

no. of fragments are DS / M = 980 / 80 = 12.25 So Answer is 13.

13 votes -- G VENKATESWARLU (619 points)

IP Datagram size = 1000B
MTU = 100B

IP header size = 20B
So, each packet will have 20B header + 80B payload.
Therefore, 80 * **12** = 960
now remaining 40B data could be sent in next fragment. So, total 12 + **1** = 13 fragments.

33 votes -- Monanshi Jain (8.5k points)

2.18.2 Ip Packet: GATE2004-IT-86 top http://gateoverflow.in/3730

Selected Answer

D.) Destination Port number.

Why? Because the IP header has nothing to do with the port number.

Port numbers are used by the transport layer to ensure process to process delivery.

15 votes -- Gate Keeda (19.1k points)

2.18.3 Ip Packet: GATE2010-15 top http://gateoverflow.in/2188

Selected Answer

It can be used to prevent packet looping.

17 votes -- Sankaranarayanan P.N (11.2k points)

2.18.4 Ip Packet: GATE2014-3-25 top http://gateoverflow.in/2059

Selected Answer

The Answer is OPTION D.

Whenever an IP packet is transmitted, the value in Time to Live (TTL) field will be decremented on every single hop. Hence, TTL is changed on every hop.

Now, since TTL changes, hence the Checksum of the packet will also change.

For the Fragmentation offset, A packet will be fragmented if the packet has a size greater than the Maximum Transmission Unit (MTU) of the network. Hence, Fragmentation offset can also be changed.

33 votes -- saurabhrk (1.5k points)

2.18.5 Ip Packet: GATE2014-3-28 top http://gateoverflow.in/2062

Selected Answer

ip packet length is given 4404 which includes ip header of length 20

so data is 4384

now router divide this data in 3 parts

1480 1480 1424

after adding ip header in last packet packet size is 1444 and since its the last packet therefore MF =0

and offset is 2960/8=370

20 votes -- anmolgate (315 points)

2.18.6 Ip Packet: GATE2015-1_22 top

http://gateoverflow.in/8220

Selected Answer

Source Address.

15 votes

-- Arjun Suresh (294k points)

2.18.7 Ip Packet: GATE2015-2_52 top

http://gateoverflow.in/8255

Selected Answer

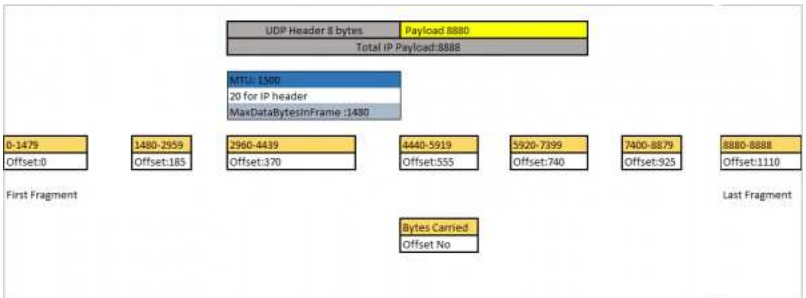
Ans C

number of fragments = ceil(8888/1480) = 7
offset of last fragment = (1500 - 20) * 6 / 8 = 1110 (scaling factor of 8 is used in offset field).

TCP or UDP header will be added to the DataUnit received from Transport Layer to Network Layer. And fragmentation happens at Network Layer. So no need to add TCP or UDP header into each fragment.

32 votes

-- Vikrant Singh (13.4k points)



Answer is : 7 fragments and last fragment offset is 1110

18 votes

-- bahirNaik (3.7k points)

2.19 Ipv4(8) top

2.19.1 Ipv4: GATE2003-27 top

http://gateoverflow.in/917

Which of the following assertions is FALSE about the Internet Protocol (IP)?

A. It is possible for a computer to have multiple IP addresses
B. IP packets from the same source to the same destination can take different routes in the network
C. IP ensures that a packet is discarded if it is unable to reach its destination within a given number of hops
D. The packet source cannot set the route of an outgoing packets; the route is determined only by the routing tables in the routers on the way

gate2003 computer-networks ipv4 normal

Answer

2.19.2 Ipv4: GATE2004-56 top

http://gateoverflow.in/1052

Consider three IP networks A, B and C. Host H_A in network A sends messages each containing 180 bytes of application data to a host H_C in network C. The TCP layer prefixes 20 byte header to the message. This passes through an intermediate network B. The maximum packet size, including 20 byte IP header, in each network is:

- A: 1000 bytes
- B: 100 bytes

- C: 1000 bytes

The network A and B are connected through a 1 Mbps link, while B and C are connected by a 512 Kbps link (bps = bits per second).

Assuming that the packets are correctly delivered, how many bytes, including headers, are delivered to the IP layer at the destination for one application message, in the best case? Consider only data packets.

A. 200
B. 220
C. 240
D. 260

gate2004 computer-networks ipv4 tcp normal

Answer

2.19.3 Ipv4: GATE2004-57 top

http://gateoverflow.in/43572

Consider three IP networks A, B and C. Host H_A in network A sends messages each containing 180 bytes of application data to a host H_C in network C. The TCP layer prefixes 20 byte header to the message. This passes through an intermediate network B. The maximum packet size, including 20 byte IP header, in each network is:

- A: 1000 bytes
- B: 100 bytes
- C: 1000 bytes

The network A and B are connected through a 1 Mbps link, while B and C are connected by a 512 Kbps link (bps = bits per second).

What is the rate at which application data is transferred to host H_C? Ignore errors, acknowledgements, and other overheads.

A. 325.5 Kbps
B. 354.5 Kbps
C. 409.6 Kbps
D. 512.0 Kbps

gate2004 computer-networks ipv4 tcp normal

Answer

2.19.4 Ipv4: GATE2006-5 top

http://gateoverflow.in/884

For which one of the following reasons does internet protocol(IP) use the time-to-live(TTL) field in IP datagram header?

A. Ensure packets reach destination within that time
B. Discard packets that reach later than that time
C. Prevent packets from looping indefinitely
D. Limit the time for which a packet gets queued in intermediate routers

gate2006 computer-networks ipv4 ip-packet easy

Answer

2.19.5 Ipv4: GATE2012_23 top

http://gateoverflow.in/1606

In the IPv4 addressing format, the number of networks allowed under Class C addresses is

(A) 2^{14}
(B) 2^{7}
(C) 2^{21}

(D) 2^{24}

gate2012 computer-networks ipv4 easy

Answer

2.19.6 Ipv4: GATE2013_37 top http://gateoverflow.in/1548

In an IPv4 datagram, the M bit is 0, the value of HLEN is 10, the value of total length is 400 and the fragment offset value is 300. The position of the datagram, the sequence numbers of the first and the last bytes of the payload, respectively are

(A) Last fragment, 2400 and 2789
(B) First fragment, 2400 and 2759
(C) Last fragment, 2400 and 2759
(D) Middle fragment, 300 and 689

gate2013 computer-networks ipv4 normal

Answer

2.19.7 Ipv4: GATE2014-3-27 top http://gateoverflow.in/2061

Every host in an IPv4 network has a 1-second resolution real-time clock with battery backup. Each host needs to generate up to 1000 unique identifiers per second. Assume that each host has a globally unique IPv4 address. Design a 50-bit globally unique ID for this purpose. After what period (in seconds) will the identifiers generated by a host wrap around?

gate2014-3 computer-networks ipv4 numerical-answers normal

Answer

2.19.8 Ipv4: GATE2017-2-20 top http://gateoverflow.in/118427

The maximum number of IPv4 router addresses that can be listed in the record route (RR) option field of an IPv4 header is______

gate2017-2 computer-networks ipv4 numerical-answers

Answer

Answers: Ipv4

2.19.1 Ipv4: GATE2003-27 top http://gateoverflow.in/917

Selected Answer

In computer networking, **source routing**, also called **path addressing**, allows a sender of a packet to partially or completely specify the route of the packet takes through the network. In contrast, in non-source routing protocols, routers in the network determine the path based on the packet's destination.

http://en.wikipedia.org/wiki/Source_routing

Answer-D

14 votes -- Priya_das (775 points)

2.19.2 Ipv4: GATE2004-56 top http://gateoverflow.in/1052

Selected Answer

Packet A sends an IP packet of 180 bytes of data + 20 bytes of TCP header + 20 bytes of IP header to B.

IP layer of B now removes 20 bytes of IP header and has 200 bytes of data. So, it makes 3 IP packets - [80 + 20, 80 + 20 + 40 + 20] and sends to C as the Ip packet size of B is 100. So, C receives 260 bytes of data which includes 60 bytes of IP headers and 20 bytes of TCP header.

For data rate, we need to consider only the slowest part of the network as data will be getting accumulated at that sender (data rate till that slowest part, we need to add time if a faster part follows a slower part).

So, here 180 bytes of application data are transferred from A to C and this causes 260 bytes to be transferred from B to

C.

26 votes -- Arjun Suresh (294k points)

2.19.3 Ipv4: GATE2004-57 top

http://gateoverflow.in/43572

Selected Answer

Packet A sends an IP packet of 180 bytes of data + 20 bytes of TCP header + 20 bytes of IP header to B.

IP layer of B now removes 20 bytes of IP header and has 200 bytes of data. So, it makes 3 IP packets - [80 + 20, 80 + 20 , 40 + 20] and sends to C as the Ip packet size of B is 100. So, C receives 260 bytes of data which includes 60 bytes of IP headers and 20 bytes of TCP header.

For data rate, we need to consider only the slowest part of the network as data will be getting accumulated at that sender (data rate till that slowest part, we need to add time if a faster part follows a slower part).

So, here 180 bytes of application data are transferred from A to C and this causes 260 bytes to be transferred from B to C.

Time to transfer 260 bytes from B-C = 260 * 8/(512 * 1000) = 65/16000 = 13/3200

So, data rate = 180 * 3200 / 13 = 44.3 kBps = 354.46 kbps

21 votes -- Arjun Suresh (294k points)

Over all bytes received by NETWORK C =260 bytes (this include tcp header and ip header).

EFFECTIVE DATA TRANSFERRED FROM NETWORK B TO NETWORK C=180 Byte.

HENCE EFFECTIVE EFFICIENCY = (180/260)*512 Kbps = 354.46 Kbps

19 votes -- Ankit Chourasiya (591 points)

2.19.4 Ipv4: GATE2006-5 top

http://gateoverflow.in/884

Selected Answer

ans c)

10 votes -- Aditi Dan (5.3k points)

2.19.5 Ipv4: GATE2012_23 top

http://gateoverflow.in/1606

Selected Answer

Answer is (c)

Class	Leading bits	Size of *network number* bit field	Size of *rest* bit field	Number of networks	Addresses per network	Total addresses in class	Start address	End address
Class A	0	8	24	128 (2^7)	16,777,216 (2^{24})	2,147,483,648 (2^{31})	0.0.0.0	127.255.255.255
Class B	10	16	16	16,384 (2^{14})	65,536 (2^{16})	1,073,741,824 (2^{30})	128.0.0.0	191.255.255.255
Class C	110	24	8	2,097,152 (2^{21})	256 (2^8)	536,870,912 (2^{29})	192.0.0.0	223.255.255.255
Class D (multicast)	1110	not defined	not defined	not defined	not defined	268,435,456 (2^{28})	224.0.0.0	239.255.255.255
Class E (reserved)	1111	not defined	not defined	not defined	not defined	268,435,456 (2^{28})	240.0.0.0	255.255.255.255

We have 32 bits in the IPV4 network

Class A = 8 network bits + 24 Host bits

Class B = 16 network bits + 16 Host bits

Class C = 24 network bits + 8 host bits.

Now for class C we have 3 bits reserved for the network id... Hence remaining bits are 21. Therefore total number of networks possible are 2^{21}.

Similarly in Class B we have 2 bits reserved... Hence total number of networks in class B are 2^{14}.

And we have 1 bit reserved in Class A, therefore there are 2^{7} networks.

And a better reasoning for the bit reservation is given here. have a look.

https://en.wikipedia.org/wiki/Classful_network

16 votes -- Gate Keeda (19.1k points)

2.19.6 Ipv4: GATE2013_37 top

http://gateoverflow.in/1548

Selected Answer

$M = 0$ meaning no more fragments after this. Hence, its the last fragment.

IHL = internet header length = $10 \times 4 = 40B$ coz 4 is the scaling factor for this field.
Total Length = $400B$
Payload size = Total length - Header length = $400 - 40 = 360B$

fragment offset = $300 \times 8 = 2400B$ = represents how many Bytes are before this. 8 is the scaling factor here.
$\therefore$ the first byte # $= 2400$

Last byte # = first byte # + total bytes in payload - 1 = $2400 + 360 - 1 = 2759$

option C is correct

21 votes -- Amar Vashishth (28.7k points)

payload =total length-header

=400-40

=360

M bit is 0 so it is last fragment

offset is 300

so packet's first bit 300*8=2400

last bit =2400+359=2759

so ans is c

16 votes -- Pooja Palod (32.4k points)

2.19.7 Ipv4: GATE2014-3-27 top

http://gateoverflow.in/2061

Worst case scenario can be that all 2^32 host are present on the network each generating 1000 packets simultaneously in 1 second

so total packet produced in 1 second = 2^32 * 2^10 (assuming 1024 = 1000) = 2^42

now we can distinguish 2^50 packets, after that wrap around (SO wrap around time will be when 2^50 identifiers are used)

2^42 takes 1 second

2^50 will take = (2^50/2^42)=2^8=256seconds

17 votes -- lgau0522 (329 points)

2.19.8 Ipv4: GATE2017-2-20 top

http://gateoverflow.in/118427

Selected Answer

A record-route (RR) option is used to record the Internet routers that handle the datagram. It is listed in OPTIONS of IPv4.

According to RFC 791, there are two cases for the format of an option:

Case 1: A single octet of option-type.

Case 2: An option-type octet, an option-length octet, and the actual option-data octets.

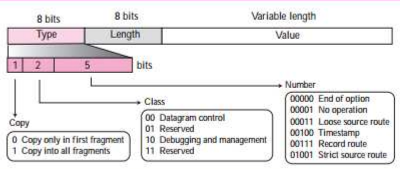
In both the cases, first 16 bits of OPTIONS field is used. Therefore, out off 40 Bytes only 38 Bytes are remaining for storing IPv4 addresses. In 38 Bytes we can store 9 IPv4 addresses as each IPv4 address is of 4 Bytes.

$\therefore$ 9 should be answer.

Ref : https://tools.ietf.org/html/rfc791

Diagram from Forouzan :

Figure 7.10 *Option format*



15 votes -- Kantikumar (3.5k points)

2.20 Lan Technologies(5) top

2.20.1 Lan Technologies: GATE2003-83 top

http://gateoverflow.in/966

A 2km long broadcast LAN has 10^7 bps bandwidth and uses CSMA/CD. The signal travels along the wire at 2×10^8 m/s. What is the minimum packet size that can be used on this network?

A. 50 bytes
B. 100 bytes
C. 200 bytes
D. None of the above

gate2003 computer-networks lan-technologies normal

Answer

2.20.2 Lan Technologies: GATE2004-IT-27 top

http://gateoverflow.in/3668

A host is connected to a Department network which is part of a University network. The University network, in turn, is part of the Internet. The largest network in which the Ethernet address of the host is unique is

A. the subnet to which the host belongs
B. the Department network
C. the University network
D. the Internet

gate2004-it computer-networks lan-technologies ethernet normal

Answer

2.20.3 Lan Technologies: GATE2005-IT-28 top

http://gateoverflow.in/3774

Which of the following statements is FALSE regarding a bridge?

A. Bridge is a layer 2 device
B. Bridge reduces collision domain
C. Bridge is used to connect two or more LAN segments
D. Bridge reduces broadcast domain

gate2005-it computer-networks lan-technologies normal

Answer

2.20.4 Lan Technologies: GATE2006-IT-66 top

http://gateoverflow.in/3610

A router has two full-duplex Ethernet interfaces each operating at 100 Mb/s. Ethernet frames are at least 84 bytes long (including the Preamble and the Inter-Packet-Gap). The maximum packet processing time at the router for wirespeed forwarding to be possible is (in microseconds)

A. 0.01
B. 3.36
C. 6.72
D. 8

gate2006-it computer-networks lan-technologies ethernet normal

Answer

2.20.5 Lan Technologies: GATE2007-65 top

http://gateoverflow.in/1263

There are n stations in slotted LAN. Each station attempts to transmit with a probability p in each time slot. What is the probability that **ONLY** one station transmits in a given time slot?

A. $np(1-p)^{n-1}$
B. $(1-p)^{n-1}$
C. $p(1-p)^{n-1}$
D. $1-(1-p)^{n-1}$

gate2007 computer-networks lan-technologies probability normal

Answer

Answers: Lan Technologies

2.20.1 Lan Technologies: GATE2003-83 top

http://gateoverflow.in/966

Selected Answer

In CSMA/CD, to detect a collision the transmission time (which depends on the packet size) must be greater than twice the propagation delay.

Propagation delay here = $\frac{2km}{2\times10^8 m/s}$
$= 10 \text{ microseconds}$

Now, transmission time for x bytes = $\frac{x\times8}{10^7} = 0.8x \text{ microseconds}$

So, $0.8x > 2\times10 \implies x > 25 \text{ bytes}$

So, None of these.

17 votes -- Arjun Suresh (294k points)

2.20.2 Lan Technologies: GATE2004-IT-27 top

http://gateoverflow.in/3668

Selected Answer

Ans is D, Ethernet address is nothing but MAC Address which is present on NIC and it is unique for every network device (a single system might have multiple network cards and each can have its own MAC address).

PS: We can never say Ethernet address is unique only in a network -- because it is independent of the network a device is connected to. That is, if we move a device from one network to another, MAC address remains same. Of course we can do spoofing, but this is not relevant to the asked question.

15 votes -- Pradyumna Paralikar (353 points)

2.20.3 Lan Technologies: GATE2005-IT-28 top

http://gateoverflow.in/3774

Selected Answer

Bridges are DataLink layer devices used to connect LANs.. Briges are collision domain separator but unable to separate Broadcast domain..

11 votes -- Digvijay (47k points)

2.20.4 Lan Technologies: GATE2006-IT-66 top

http://gateoverflow.in/3610

Selected Answer

Here we need at least enough speed that we are able to transmit packets in a speed we get them !

We have got 2 Full duplex ports, each operating at 100 Mb/s. So we require incoming packets with 200 Mbps so that we can sent out data at 200 Mbps over the two interfaces.

For each packet to come In router, you will need transmission TIme, in case of single 84 byte packet you will get it as 6.72 microsecond.

Now D is simply wrong. You take 8 Microsecond to process, soon you will have pile of packets waiting (Processing > Transmission), and we are getting 2 packets per 6.72 micro seconds as input.

C is wrong, here we can get 2 6.72 micro seconds packets & we are barely able to process 1 packet in that time. So every processing time our Queue will increase size by 1 & get full and overflow.

B & A are okay.

A is best though as we are asked to give Maximum, **B is answer !**

Assume that in B you got 2 packet at time 0, by time 3.36 you can start sending packet 1, by 6.72 packet 2. By 6.72 you got 2 more packet. By time you finish processing Packet no 3, first port where you started processing with 3.36 is free, so you can start sending Packet 3 and so on !

Ref: https://en.wikipedia.org/wiki/Wire_speed

21 votes -- Akash (43.8k points)

For maintaining the speed of forwarding of wire, i.e. 100 Mbps, processing time should be at most same as minimum transmission time. (Otherwise the packet will be delayed for transmission due to processing).

i.e. 84*8 bits / 100 Mbps = 6.72 micro seconds.

Ref: https://en.wikipedia.org/wiki/Wire_speed

PS: Wire speed doesn't imply a packet is sent without any waiting time. It just means receiving and sending rates are the maximum possible.

12 votes -- Shreyans Dhankhar (2.6k points)

2.20.5 Lan Technologies: GATE2007-65 top

http://gateoverflow.in/1263

Selected Answer

Probability that only one station transmits in a given slot = $\binom{n}{1}p^1(1-p)^{n-1}$

answer = **option A**

p for 1 transmitting and $(1-p)$ for $n-1$ non transmitting and n ways to choose 1 from n.

15 votes -- Aditi Dan (5.3k points)

2.21 Link State Routing(1) top

2.21.1 Link State Routing: GATE2014-1-23 top http://gateoverflow.in/1790

Consider the following three statements about link state and distance vector routing protocols, for a large network with 500 network nodes and 4000 links.

[S1]: The computational overhead in link state protocols is higher than in distance vector protocols.

[S2]: A distance vector protocol (with split horizon) avoids persistent routing loops, but not a link state protocol.

[S3]: After a topology change, a link state protocol will converge faster than a distance vector protocol.

Which one of the following is correct about S1, S2, and S3 ?

A. S1, S2, and S3 are all true.
B. S1, S2, and S3 are all false.
C. S1 and S2 are true, but S3 is false.
D. S1 and S3 are true, but S2 is false.

gate2014-1 computer-networks routing distance-vector-routing link-state-routing normal

Answer

Answers: Link State Routing

2.21.1 Link State Routing: GATE2014-1-23 top http://gateoverflow.in/1790

Selected Answer

The computational overhead in link state protocols is higher than in distance vector protocols. Bcz LSR is based upon global knowledge whereas DVR is based upon Local info .

Persistent looping can be avoid with the help of split horizon in DVR.But there is no concept of persisitent looping in LSR,In LSR only temporary loop exist and can automatically solved by system or router.S2 is false.

And After a topology change, a link state protocol will converge faster than a distance vector protocol.S3 is true.

Option-D

10 votes -- Paras Singh (5.5k points)

S1 : because of flooding at each router computational overhead in link state routing is more.
S2 : Persistent loop i.e. count to infinity problem takes place in Distance vector routing not in link state routing.
S3 : Link state routing protocol converges faster when topology changes.

14 votes -- Digvijay (47k points)

2.22 Longest Mask(1) top

2.22.1 Longest Mask: GATE2006-IT-63, ISRO2015-57 top http://gateoverflow.in/3607

A router uses the following routing table:

Destination	Mask	Interface
144.16.0.0	255.255.0.0	eth0
144.16.64.0	255.255.224.0	eth1
144.16.68.0	255.255.255.0	eth2
144.16.68.64	255.255.255.224	eth3

packet bearing a destination address 144.16.68.117 arrives at the router. On which interface will it be forwarded?

A. eth0
B. eth1
C. eth2
D. eth3

gate2006-it computer-networks subnetting normal isro2015 longest-mask

Answer

Answers: Longest Mask

2.22.1 Longest Mask: GATE2006-IT-63, ISRO2015-57 top

http://gateoverflow.in/3607

Selected Answer

Firstly start with **Longest mask**

144. 16 . 68 .117 = 144. 16. 68. 01110101 **AND**

255.255.255.224 = 255.255.255. 11100000

= 144.16.68.96 **(Not matching with Destination)**

Now, take 255. 255. 255. 0

144.16. 68.117 AND 255.255.255.0 = 144.16.68.0 (**matched**)

So,interface chosen is **eth2** **OPTION (C).**

24 votes

-- Himanshu Agarwal (16.2k points)

---

to get network id we perform bitwise AND operation of ip address with every subnet mask...after if the obtain value matches with the network id ..then we send the data through that..if more than one network id matches then we check for the longest mask.

ip address= 144.16.68.117 and with all mask one by one

first mask 255.255.0.0 ===> 11111111.11111111.00000000.00000000

144.16.68.117===> 10010000.00010000.01000100.01110101

bit wise and operation

---

we get 144.16.0.0===> 10010000.00010000.00000000.00000000

which is matching with network id 144.16.0.0 given opposite to mask 255.255.0.0

but we cannot stop here may some more network id matches..so check for every mask

similarly 255.255.224.0

144.16.68.117

144.16.64.0

which is matching with network id 144.16.64.0 given opposite to mask 255.255.224.0

now next

255.255.255.0

144.16.68.117

144.16.68.0

which is matching with network id 144.16.68.0 given opposite to mask 255.255.255.0

now last

255.255.255.224

144.16.68.117

144.16.68.96

which is NOT matching with network id 144.16.68.64 given opposite to mask 255.255.255.224

NOW 3 OF the networks are matching...now we check for longest mask..

i.e 255.255.0.0

255.255.224.0

255.255.255.0 so last one is the largest therefore eth2 will be chosen to send packet

10 votes -- Tauhin Gangwar (9.3k points)

2.23 Mac Protocol(4) top

2.23.1 Mac Protocol: GATE2004-IT-85 top http://gateoverflow.in/3729

onsider a simplified time slotted MAC protocol, where each host always has data to send and transmits with probability p = 0.2 in every slot. There is no backoff and one frame can be transmitted in one slot. If more than one host transmits in the same slot, then the transmissions are unsuccessful due to collision. What is the maximum number of hosts which this protocol can support, if each host has to be provided a minimum through put of 0.16 frames per time slot?

A. 1
B. 2
C. 3
D. 4

gate2004-it computer-networks congestion-control mac-protocol normal

Answer

2.23.2 Mac Protocol: GATE2005-74 top http://gateoverflow.in/1397

Suppose the round trip propagation delay for a 10 Mbps Ethernet having 48-bit jamming signal is 46.4 μs. The minimum frame size is:

A. 94
B. 416
C. 464
D. 512

gate2005 computer-networks mac-protocol normal debated

Answer

2.23.3 Mac Protocol: GATE2005-IT-75 top

http://gateoverflow.in/3838

In a TDM medium access control bus LAN, each station is assigned one time slot per cycle for transmission. Assume that the length of each time slot is the time to transmit 100 bits plus the end-to-end propagation delay. Assume a propagation speed of 2 x 10^8 m/sec. The length of the LAN is 1 km with a bandwidth of 10 Mbps. The maximum number of stations that can be allowed in the LAN so that the throughput of each station can be 2/3 Mbps is

A. 3
B. 5
C. 10
D. 20

gate2005-it computer-networks mac-protocol normal

Answer

2.23.4 Mac Protocol: GATE2015-2_8 top

http://gateoverflow.in/8056

A link has transmission speed of 10^6 bits/sec. It uses data packets of size 1000 bytes each. Assume that the acknowledgement has negligible transmission delay, and that its propagation delay is the same as the data propagation delay. Also assume that the processing delays at nodes are negligible. The efficiency of the stop-and-wait protocol in this setup is exactly 25%. The value of the one way propagation delay (in milliseconds) is______.

gate2015-2 computer-networks mac-protocol stop-and-wait normal numerical-answers

Answer

Answers: Mac Protocol

2.23.1 Mac Protocol: GATE2004-IT-85 top

http://gateoverflow.in/3729

Selected Answer

Let there be N such hosts.
Then when one host is transmitting then others must be silent for successful transmission.
So the throughput per host

$$0.16 = 0.2 \times 0.8^{N-1}$$

$$\implies 0.8 = 0.8^{N-1}$$

on comparing the exponents, since base are identical
$N - 1 = 1, N = 2.$

28 votes -- Shreyans Dhankhar (2.6k points)

2.23.2 Mac Protocol: GATE2005-74 top

http://gateoverflow.in/1397

Selected Answer

The sender must be able to detect a collision before completely sending a frame. So, the minimum frame length must be such that, before the frame completely leaves the sender any collision must be detected.

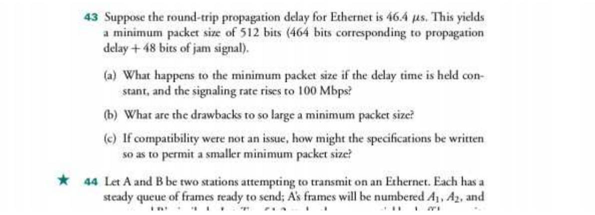
Now, the worst case for collision detection is when the start of the frame is about to reach the receiver and the receiver starts sending. Collision happens and a jam signal is produced and this signal must travel to the sender. So, the time for this will be the time for the start of the frame to reach near the receiver + time for the jam signal to reach the sender + transmission time for the jam signal. (We don't need to include transmission time for the frame as as soon as the first bit of the frame arrives, the receiver will have detected it). Time for the start of the frame to reach near the receiver + Time for the jam signal to reach the sender = Round trip propagation delay = 46.4 μs. So, 46.4 + 48/10 (48 bits at 10 Mbps takes 4.8 micro sec.) = 51.2 μs.

Now, the frame length must be such that its transmission time must be more than 51.2 μs. So, minimum frame length

= $51.2 * 10^{-6} * 10 * 10^6$ = 512 bits.

http://gatecse.in/w/images/3/32/3-MACSublayer.ppt

A reference question from Peterson Davie:


43 Suppose the round-trip propagation delay for Ethernet is 46.4 μs. This yields a minimum packet size of 512 bits (464 bits corresponding to propagation delay + 48 bits of jam signal).

(a) What happens to the minimum packet size if the delay time is held constant, and the signaling rate rises to 100 Mbps?

(b) What are the drawbacks to so large a minimum packet size?

(c) If compatibility were not an issue, how might the specifications be written so as to permit a smaller minimum packet size?

★ 44 Let A and B be two stations attempting to transmit on an Ethernet. Each has a steady queue of frames ready to send; A's frames will be numbered A_1, A_2, and

Another reference for requiring jam signal bits to be included for minimum frame size.

http://intronetworks.cs.luc.edu/current/html/ethernet.html

Can collision be detected by the source without getting the full jam signal (by change in current)?

Probably yes. But to be safe (from signal loss) the source waits for the entire jam signal. See below link

http://superuser.com/questions/264171/collisions-in-csma-cd-ethernet

37 votes -- Arjun Suresh (294k points)

2.23.3 Mac Protocol: GATE2005-IT-75 top

http://gateoverflow.in/3838

Selected Answer

Tt = 10 micro secs

Tp = 5 micro secs

Efficiency of the network = Tt / (Tt + Tp) = 10 / 15 = 2/3

Total throughput available for the entire network = Efficiency * Bandwidth = (2/3) * 10 Mbps = 20/3 Mbps

Let, No. of stations = N (each wants a Throughput of 2/3 Mbps),

N * (2/3 Mbps) = 20/3 Mbps => N = 10

=> 10 stations can be connected in the channel at max.

16 votes -- Ravi Ranjan (2.9k points)

2.23.4 Mac Protocol: GATE2015-2_8 top

http://gateoverflow.in/8056

Selected Answer

In stop and wait, a frame is sent and next frame will be sent only after ACK is received.

$$\text{Efficiency} = \frac{\text{Amount of data sent}}{\text{Amount of data that could be sent}}$$

$$= \frac{\text{Amount of data sent}}{RTT \times 10^6}$$

$$= \frac{\text{Amount of data sent}}{(\text{ Prop. delay for data} + \text{Prop. delay for ACK} + \text{Transmission time for data} + \text{Transmission time for ACK}) \times 10^6}$$

$$= \frac{1000 \times 8}{(p + p + 1000 \times 8/10^6 + 0) \times 10^6}$$

$$= \frac{8}{2p + 8ms} \text{ (where p is the prop. delay in milli seconds)}$$

$= \frac{4}{p+4} = 0.25 \text{ (given in question)}$

So, $p + 4 = 16, p = 12ms$.

19 votes -- Arjun Suresh (294k points)

2.24 Manchester Encoding(2) top

2.24.1 Manchester Encoding: GATE2007-19 top http://gateoverflow.in/1217

In Ethernet when Manchester encoding is used, the bit rate is:

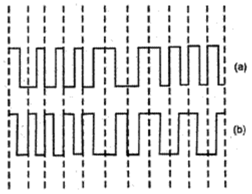
A. Half the baud rate
B. Twice the baud rate
C. Same as the baud rate
D. None of the above

gate2007 computer-networks ethernet manchester-encoding normal

Answer

2.24.2 Manchester Encoding: GATE2007-IT-61 top http://gateoverflow.in/3505

In the waveform (a) given below, a bit stream is encoded by Manchester encoding scheme. The same bit stream is encoded in a different coding scheme in wave form (b). The bit stream and the coding scheme are



A. 1000010111 and Differential Manchester respectively
B. 0111101000 and Differential Manchester respectively
C. 1000010111 and Integral Manchester respectively
D. 0111101000 and Integral Manchester respectively

gate2007-it computer-networks communication manchester-encoding normal

Answer

Answers: Manchester Encoding

2.24.1 Manchester Encoding: GATE2007-19 top http://gateoverflow.in/1217

Selected Answer

Bit rate is half the baud rate in Manchester encoding as bits are transferred only during a positive transition of the clock.

http://stackoverflow.com/questions/25834577/why-in-manchester-encoding-the-bit-rate-is-half-of-the-baud-rate

9 votes -- Arjun Suresh (294k points)

2.24.2 Manchester Encoding: GATE2007-IT-61 top http://gateoverflow.in/3505

Selected Answer

THE AMBIGUOUS QUESTION WITHOUT ANY STANDARD MENTION !!

BOTH A and B is correct , it is just the convention which determine the correct answer.

see this from IIT KGP, they follow IEEE standard - http://nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Computer%20networks/pdf/M2L4.pdf

and this one from IITB , they follow G E Thomas version --

https://www.cse.iitb.ac.in/synerg/lib/exe/fetch.php?media=public:courses:cs348-spring08:slides:topic03-phy-encoding.pdf

as per IEEE B is correct

as per G E Thomas A is correct.

as we ususally follow IEEE thus B is correct

10 votes -- Bikram (44.7k points)

2.25 Network Addressing(1) top

2.25.1 Network Addressing: GATE2005-24 top

http://gateoverflow.in/1360

The address resolution protocol (ARP) is used for:

A. Finding the IP address from the DNS
B. Finding the IP address of the default gateway
C. Finding the IP address that corresponds to a MAC address
D. Finding the MAC address that corresponds to an IP address

gate2005 computer-networks normal network-addressing

Answer

Answers: Network Addressing

2.25.1 Network Addressing: GATE2005-24 top

http://gateoverflow.in/1360

Selected Answer

ans d)

9 votes -- Aditi Dan (5.3k points)

2.26 Network Communication(1) top

2.26.1 Network Communication: GATE2017-2-35 top

http://gateoverflow.in/118537

Consider two hosts X and Y, connected by a single direct link of rate 10^6 bits/sec. The distance between the two hosts is $10,000$ km and the propagation speed along the link is 2×10^8 m/sec. Host X sends a file of $50,000$ bytes as one large message to host Y continuously. Let the transmission and propagation delays be p milliseconds and q milliseconds respectively. Then the value of p and q are

A. p=50 and q=100
B. p=50 and q=400
C. p=100 and q=50
D. p=400 and q=50

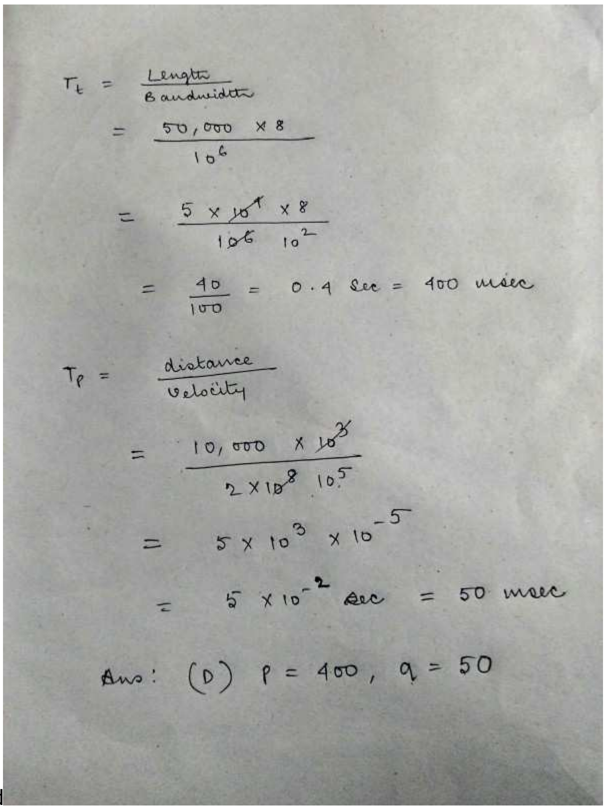
gate2017-2 computer-networks network-communication

Answer

Answers: Network Communication

2.26.1 Network Communication: GATE2017-2-35 top http://gateoverflow.in/118537

Selected Answer



$$T_t = \frac{\text{Length}}{\text{Bandwidth}} = \frac{50{,}000 \times 8}{10^6} = \frac{5 \times \cancel{10^4} \times 8}{\underset{10^2}{\cancel{10^6}}} = \frac{40}{100} = 0.4 \text{ sec} = 400 \text{ msec}$$

$$T_p = \frac{\text{distance}}{\text{velocity}} = \frac{10{,}000 \times \cancel{10^3}}{2 \times \underset{10^5}{\cancel{10^8}}} = 5 \times 10^3 \times 10^{-5} = 5 \times 10^{-2} \text{ sec} = 50 \text{ msec}$$

Ans: (D) $p = 400$, $q = 50$

Hence answer d

8 votes

-- Arnabi (6.4k points)

2.27 Network Flow(6) top

2.27.1 Network Flow: GATE1992_01,v top http://gateoverflow.in/550

(v) A simple and reliable data transfer can be accomplished by using the 'handshake protocol'. It accomplishes reliable data transfer because for every data item sent by the transmitter ______.

gate1992 computer-networks network-flow easy

Answer

2.27.2 Network Flow: GATE1992_02,v top http://gateoverflow.in/560

02. Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

(v). Start and stop bis don not contain an 'information' but are used in serial communication

(a). Error detection

(b). Error correction

(c). Synchronization

(d). Slowing down the communications

gate1992 easy computer-networks network-flow

Answer

2.27.3 Network Flow: GATE2004-IT-80 top http://gateoverflow.in/3724

In a data link protocol, the frame delimiter flag is given by 0111. Assuming that bit stuffing is employed, the transmitter sends the data sequence 01110110 as

A. 01101011
B. 011010110
C. 011101100
D. 0110101100

gate2004-it computer-networks network-flow normal

Answer

2.27.4 Network Flow: GATE2004-IT-87 top http://gateoverflow.in/3731

A TCP message consisting of 2100 bytes is passed to IP for delivery across two networks. The first network can carry a maximum payload of 1200 bytes per frame and the second network can carry a maximum payload of 400 bytes per frame, excluding network overhead. Assume that IP overhead per packet is 20 bytes. What is the total IP overhead in the second network for this transmission?

A. 40 bytes
B. 80 bytes
C. 120 bytes
D. 160 bytes

gate2004-it computer-networks network-flow normal

Answer

2.27.5 Network Flow: GATE2005-IT-72 top http://gateoverflow.in/3835

A channel has a bit rate of 4 kbps and one-way propagation delay of 20 ms. The channel uses stop and wait protocol. The transmission time of the acknowledgement frame is negligible. To get a channel efficiency of at least 50%, the minimum frame size should be

A. 80 bytes
B. 80 bits
C. 160 bytes
D. 160 bits

gate2005-it computer-networks network-flow stop-and-wait normal

Answer

2.27.6 Network Flow: GATE2006-IT-67 top http://gateoverflow.in/3611

A link of capacity 100 Mbps is carrying traffic from a number of sources. Each source generates an on-off traffic stream; when the source is on, the rate of traffic is 10 Mbps, and when the source is off, the rate of traffic is zero. The duty cycle, which is the ratio of on-time to off-time, is 1 : 2. When there is no buffer at the link, the minimum number of sources that can be multiplexed on the link so that link capacity is not wasted and no data loss occurs is S1. Assuming that all sources are synchronized and that the link is provided with a large buffer, the maximum number of sources that can be multiplexed so that no data loss occurs is S2. The values of S1 and S2 are, respectively,

A. 10 and 30
B. 12 and 25
C. 5 and 33
D. 15 and 22

gate2006-it computer-networks network-flow normal

Answer

Answers: Network Flow

2.27.1 Network Flow: GATE1992_01,v top

http://gateoverflow.in/550

Selected Answer

the receiver responds that it is ready to receive the data item.

Ref: http://www.sqa.org.uk/e-learning/NetInf101CD/page_28.htm

3 votes -- Rajarshi Sarkar (35k points)

2.27.2 Network Flow: GATE1992_02,v top

http://gateoverflow.in/560

Selected Answer

Answer: C

The start and stop bits are used to synchronize the serial receivers.

Ref: http://esd.cs.ucr.edu/labs/serial/serial.html

4 votes -- Rajarshi Sarkar (35k points)

2.27.3 Network Flow: GATE2004-IT-80 top

http://gateoverflow.in/3724

Selected Answer

Answer will be option D.)

The bit stuffing is done after every two '11' (as flag is 0111) to differentiate the data part from the flag- there must not be "111" in the data so after every 11 a '0' is added. The receiver also knows this and so it decodes every "110" as "11". Therefore option D. is the answer.

http://web.nchu.edu.tw/~pcwang/computer_networks/data_link_layer.pdf

https://en.wikipedia.org/wiki/High-Level_Data_Link_Control

18 votes -- Gate Keeda (19.1k points)

2.27.4 Network Flow: GATE2004-IT-87 top

http://gateoverflow.in/3731

Selected Answer

`At source` : TCP passes $2100B$ to IP layer. IP appends 20B header and sends it to DLL and so on. (We are interested in IP overhead, So lets consider DLL header to be negligible)

A router on the way has highest layer as Network Layer, So, complete TCP segment is fragmented. And in question 1200 and 400 are given as maximum payload without network overhead, means we are directly given the amount of data part of IP datagram a Frame can hold. [1200 doesn't contain IP header]

`Router-1`: 2120B reach $R_1's$ network layer. It removes original IP header, fragments data part at IP and then appends IP header to all fragments and forwards. So, it divides 2100 Bytes into two fragments of size 1200 and 900.And Both fragments are sent to R_2.

`Router-2`: Both fragments that reach R_2 exceed MTU at R_2. So, both are fragmented. First packet of 1200B is fragmented into 4 packets of 400, 400 and 400 Bytes respectively and Second packet of 900B is fragmented into three fragments of 400, 400 and 100 Bytes respectively.

Original data during fragmentation should not change. Only additional IP headers are added. So totally 6 $packets$ reach destination. And IP header is also an overhead because our main aim is to send data only.

Total IP Overhead $= 6 * 20 = 120$B

Hence, (C) is correct answer.

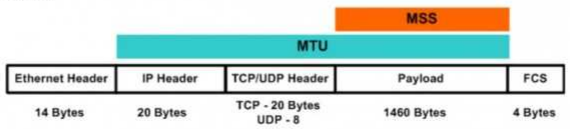
http://quiz.geeksforgeeks.org/gate-gate-it-2004-question-87/

11 votes -- Manish Joshi (25.2k points)

TRANSPORT LAYER

Maximum Segment Size (MSS)

The **maximum-segment-size option** defines the size of the biggest unit of data that can be received by the destination of the TCP segment. In spite of its name, it defines the maximum size of the data, not the maximum size of the segment. Since the field is 16 bits long, the value can be 0 to 65,535 bytes. Figure 15.44 shows the format of this option.



The MTU is defined as the maximum length of data that can be transmitted by a protocol in one instance. What makes this slightly confusing is that the MTU does NOT include the Ethernet headers required to transmit the packet on Ethernet, it only includes the IP packet information. That is, with regards to MTU, we always assume the Ethernet interface is already taking into account the 18 bytes of Ethernet headers (sometimes we don't even see the FCS so its 1514 not 1518). So this is pretty straight forward, nothing too exciting here. The majority of networks assume an MTU of 1500 bytes and everything works as expected.

MSS is slightly different because it is determined by each end of the TCP connection. During session setup a device can specify the MSS they want to use in their SYN packet. However, the devices technically do not need to agree on an MSS and each device can use a different MSS value. The only requirement is that the sending device must limit the size of the data it sends to the MSS it receives from it's peer. MSS is generally 40 bytes less than MTU to accommodate for a 20 byte IP header and a 20 byte TCP header.

> Maximum Payload of 1200 B per frame is given ,i.e , as the above picture says Payload = MSS, hence, it is different from packet size.

Answer is C).

Question says TCP message is of size = 2100 B, hence header is encapsulated with the frame and send to IP layer, and IP layer when receives this message thinks it as complete data to be send .

To be send across the first network, It is fragmented into 2 payloads of sizes 1200 and 900 .

> No need to add IP Header size with 2100B, as fragmentation acts on data/Payload and not the packet.

Now, since, IP thinks 2100B as the data so, it will directly fragment it and hence, no need to add any header.

Payload / Fragment 1: 1200 B {1200 / 8 = 150, Except last fragment all the fragments should be divisible by 8}

Payload 2: 900 B

At the second network, 1200 B is fragmented into 400 B,400 B and 400 B .

Similarly, 900 B is fragmented into 400, 400 and 100 B.

Since, 2100 B is fragmented into 6 data payloads and Header is attached to all the payloads when they will be forwared to DLL layer. **So, Total Overhead = 6 * 20 = 120 B**

Hence, DLL layer will receive total Data = 2100 + 120 = 2220 B and DLL will treat it as a complete data to be sent and DLL header will be encapsulated in DLL frame.

24 votes -- Shreyans Dhankhar (2.6k points)

2.27.5 Network Flow: GATE2005-IT-72 top

http://gateoverflow.in/3835

Selected Answer

for 50% utilization

tt/(tt+2tp)>=1/2

2tt>=tt+2tp

tt>=2tp

L/B>=2*tp

L>=2*tp*B

so here L=2*20*10^-3*4*10^3

=160 bits

so ans is d

13 votes -- Pooja Palod (32.4k points)

2.27.6 Network Flow: GATE2006-IT-67 top http://gateoverflow.in/3611

Selected Answer

Since there is no buffer.. and constraint given is there should not be any data lost, and no wastage of capacity as well..

Since data should not be lost, we calculate for the extreme case when all sources are on-time (that is transmitting)..

10 Mbps * n-station $\leqslant$ 100 Mbps

n-station = 10..

In the next part of the question it is given that the link is provided with large buffer and we are asked to find out large no. of stations..

for that we'll calculate expected value of bandwidth usage (if more data comes we store in buffer and due to expectation, the buffer will be emptied soon):

E = 1/3 * 10 + 1/3 * 10 +...n-station times $\leqslant$ 100 Mbps **[total time is (1+2) = 3 then on time is 1 so 1/3 of BW]**

=> 1/3 * 10 * n-station $\leqslant$ 100 Mbps

=> n-station = 30

so, option (A)

14 votes -- Vicky Bajoria (4.9k points)

2.28 Network Layering(3) top

2.28.1 Network Layering: GATE2003-28 top http://gateoverflow.in/918

Which of the following functionality *must* be implemented by a transport protocol over and above the network protocol?

A. Recovery from packet losses
B. Detection of duplicate packets
C. Packet delivery in the correct order
D. End to end connectivity

gate2003 computer-networks network-layering easy

Answer

2.28.2 Network Layering: GATE2004-15 top http://gateoverflow.in/1012

Choose the best matching between Group 1 and Group 2

Group - 1	**Group -2**
P. Data link layer	1. Ensures reliable transport of data over a physical point-to-point link

Group-1	Group-2
Q. Network layer	2. Encodes/decodes data for physical transmission
R. Transport layer	3. Allows end-to-end communication between two processes
	4. Routes data from one network node to the next

A. P-1, Q-4, R-3
B. P-2, Q-4, R-1
C. P-2, Q-3, R-1
D. P-1, Q-3, R-2

gate2004 computer-networks network-layering normal

Answer

2.28.3 Network Layering: GATE2013_14 top

http://gateoverflow.in/1436

Assume that source S and destination D are connected through two intermediate routers labeled R. Determine how many times each packet has to visit the network layer and the data link layer during a transmission from S to D.

(A) Network layer – 4 times and Data link layer – 4 times

(B) Network layer – 4 times and Data link layer – 3 times

(C) Network layer – 4 times and Data link layer – 6 times

(D) Network layer – 2 times and Data link layer – 6 times

gate2013 computer-networks network-layering normal

Answer

Answers: Network Layering

2.28.1 Network Layering: GATE2003-28 top

http://gateoverflow.in/918

Selected Answer

End to end connectivity is the required functionality provided by Trnasport protocol. UDP of transport layer protocol that doesn't implement other three functionalities, they are implemented only in TCP.

13 votes -- Anurag Semwal (8k points)

2.28.2 Network Layering: GATE2004-15 top

http://gateoverflow.in/1012

Selected Answer

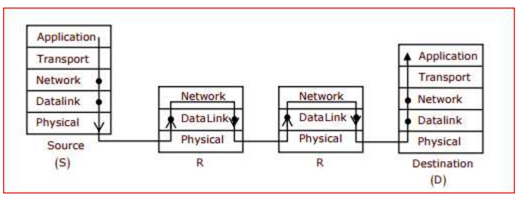
ans a)

11 votes -- Aditi Dan (5.3k points)

2.28.3 Network Layering: GATE2013_14 top

http://gateoverflow.in/1436

Selected Answer



C is the answer .

👍 16 votes -- Mithlesh Upadhyay (5.4k points)

in source it is 1 data link and 1 network .. now as routers are in network layer so

in router1:

at first it goes to network layer like physical->DLL->network (then again comes to physical like)->DLL->physical

Router2:Phhysical->DLL->network->Dll->physical

Destination:

Physical->DLL->NEtwork->TCP->Application

in both routers after computation in Network layer it is coming back to physical again ..the reason is signals can only be transmitted with physical layer

So Network Layer=4 Visit

DLL=6 Visit

👍 12 votes -- Aboveallplayer (18.5k points)

2.29 Network Protocols(5) top

2.29.1 Network Protocols: GATE 2016-1-24 top

http://gateoverflow.in/39639

Which one of the following protocols is **NOT** used to resolve one form of address to another one?

A. DNS
B. ARP
C. DHCP
D. RARP

gate2016-1 computer-networks network-protocols normal

Answer

2.29.2 Network Protocols: GATE2007-70 top

http://gateoverflow.in/1268

Match the following:

(P)	SMTP	(1)	Application layer
(Q)	BGP	(2)	Transport layer
(R)	TCP	(3)	Data link layer
(S)	PPP	(4)	Network layer
		(5)	Physical layer

A. P - 2, Q - 1, R - 3, S - 5
B. P - 1, Q - 4, R - 2, S - 3
C. P - 1, Q - 4, R - 2, S - 5
D. P - 2, Q - 4, R - 1, S - 3

gate2007 computer-networks network-layering network-protocols easy

Answer

2.29.3 Network Protocols: GATE2007-IT-69 top

http://gateoverflow.in/3514

Consider the following clauses:

i. Not inherently suitable for client authentication.
ii. Not a state sensitive protocol.
iii. Must be operated with more than one server.
iv. Suitable for structured message organization.
v. May need two ports on the serve side for proper operation.

The option that has the maximum number of correct matches is

A. IMAP-i; FTP-ii; HTTP-iii; DNS-iv; POP3-v
B. FTP-i; POP3-ii; SMTP-iii; HTTP-iv; IMAP-v
C. POP3-i; SMTP-ii; DNS-iii; IMAP-iv; HTTP-v
D. SMTP-i; HTTP-ii; IMAP-iii; DNS-iv; FTP-v

gate2007-it computer-networks network-protocols normal

Answer

2.29.4 Network Protocols: GATE2008-IT-68 top

http://gateoverflow.in/3382

Which of the following statements are TRUE?

- **S1:** TCP handles both congestion and flow control
- **S2:** UDP handles congestion but not flow control
- **S3:** Fast retransmit deals with congestion but not flow control
- **S4:** Slow start mechanism deals with both congestion and flow control

A. S1, S2 and S3 only
B. S1 and S3 only
C. S3 and S4 only
D. S1, S3 and S4 only

gate2008-it computer-networks network-protocols normal

Answer

2.29.5 Network Protocols: GATE2015-1_17 top

http://gateoverflow.in/8214

In one of the pairs of protocols given below , both the protocols can use multiple TCP connections between the same client and the server. Which one is that?

A. HTTP, FTP
B. HTTP, TELNET
C. FTP, SMTP
D. HTTP, SMTP

gate2015-1 computer-networks network-protocols normal

Answer

Answers: Network Protocols

2.29.1 Network Protocols: GATE 2016-1-24 top

http://gateoverflow.in/39639

Selected Answer

A) DNS - host name to IP address
B) ARP - IP to MAC
D) RARP - MAC to IP

So ANSWER C

12 votes -- Abhilash Panicker (8.8k points)

A) DNS - host name to IP address or vice versa
B) ARP - IP to MAC
c) DHCP-MAC to IP
D) RARP - MAC to IP
So answer will be A only because host name is not an adress as in other options.

14 votes -- Rajat Sharma (569 points)

2.29.2 Network Protocols: GATE2007-70 top

http://gateoverflow.in/1268

Selected Answer

Answer is B
SMTP is an application layer protocol used for e-mail transmission.
TCP is a core transport layer protocol.
BGP is a network layer protocol backing the core routing decisions on the Internet
PPP is a data link layer protocol commonly used in establishing a direct connection between two networking

10 votes -- naga praveen (3.6k points)

I guess answer is (b) here.PPP is a data link layer protocol

https://docs.oracle.com/cd/E18752_01/html/816-4554/ipov-6.html

11 votes -- Madhur Rawat (2.6k points)

2.29.3 Network Protocols: GATE2007-IT-69 top

http://gateoverflow.in/3514

Selected Answer

They are asking for maximum correct matches so

1.Should be HTTP thus we use HTTPS
2.HTTP as it does not depend on state of device or operating system.
3.IMAP or DNS *Not sure but they may involve multiple servers
4.POP3 is suitable for structuring or arranging the folders.
5.FTP needs two ports, 20 for data and 21 for control.

Thus, Option D, As it's matching with HTTP-2,IMAP-3,FTP-5

5 votes -- Shashank Chavan (3.4k points)

2.29.4 Network Protocols: GATE2008-IT-68 top

http://gateoverflow.in/3382

Selected Answer

(S1) TCP handles both congestion and flow control => True. IT uses congestion window for congestion control & Advertisement window for flow control
(S2) UDP handles congestion but not flow control => UDP does not handle congestion but also not handle flow control.
(S3) Fast retransmit deals with congestion but not flow control => Yes. Fast Retransmit is technique for detecting out of Order Datagram & Sending it. It is congestion control technique and has no relation with Flow control
(S4) Slow start mechanism deals with both congestion and flow control => False. It has nothing to do with Flow control. Flow control is taken care by Advertisement window. Slow start is way Sender tries to gauge network capacity !

Ans -> **S1** and **S3** only

21 votes -- Akash (43.8k points)

2.29.5 Network Protocols: GATE2015-1_17 top

http://gateoverflow.in/8214

Selected Answer

SMTP: only one TCP connection

Ref: https://tools.ietf.org/html/rfc821

Telnet: only one TCP connection

Ref: https://tools.ietf.org/html/rfc854

HTTP: Multiple connections can be used for each resource

Ref: http://www.w3.org/Protocols/rfc2616/rfc2616-sec1.html#sec1

FTP: FTP uses Telnet protocol for Control info on a TCP connection and another TCP connection for data exchange

Ref: https://tools.ietf.org/html/rfc959 (See page 8)

So, answer is A.

22 votes -- Arjun Suresh (294k points)

2.30 Network Security(14) top

2.30.1 Network Security: GATE 2016-1-52 top http://gateoverflow.in/39694

Consider that B wants to send a message m that is digitally signed to A. Let the pair of private and public keys for A and B be denoted by ${K_x}^-$ and ${K_x}^+$ for $x = A, B$, respectively. Let $K_x(m)$ represent the operation of encrypting m with a key K_x and $H(m)$ represent the message digest. Which one of the following indicates the **CORRECT** way of sending the message m along with the digital signature to A?

A. $\{m, {K_B}^+(H(m))\}$
B. $\{m, {K_B}^-(H(m))\}$
C. $\{m, {K_A}^-(H(m))\}$
D. $\{m, {K_A}^+(m)\}$

gate2016-1 computer-networks network-security easy

Answer

2.30.2 Network Security: GATE2004-IT-25 top http://gateoverflow.in/3666

A sender is employing public key cryptography to send a secret message to a receiver. Which one of the following statements is TRUE?

A. Sender encrypts using receiver's public key
B. Sender encrypts using his own public key
C. Receiver decrypts using sender's public key
D. Receiver decrypts using his own public key

gate2004-it computer-networks network-security normal

Answer

2.30.3 Network Security: GATE2004-IT-84 top http://gateoverflow.in/3728

Consider a parity check code with three data bits and four parity check bits. Three of the code words are 0101011, 1001101 and 1110001. Which of the following are also code words?

I. 0010111
II. 0110110
III. 1011010
IV. 0111010

A. I and III
B. I, II and III
C. II and IV
D. I, II, III and IV

gate2004-it computer-networks network-security normal

Answer

2.30.4 Network Security: GATE2005-IT-79 top http://gateoverflow.in/3843

Suppose that two parties A and B wish to setup a common secret key (D-H key) between themselves using the Diffie-Hellman key exchange technique. They agree on 7 as the modulus and 3 as the primitive root. Party A chooses 2 and party B chooses 5 as their respective secrets. Their D-H key is

A. 3
B. 4
C. 5
D. 6

gate2005-it computer-networks network-security normal

Answer

2.30.5 Network Security: GATE2007-IT-15 top http://gateoverflow.in/3448

Consider the following two statements:

i. A hash function (these are often used for computing digital signatures) is an injective function.
ii. A. encryption technique such as DES performs a permutation on the elements of its input alphabet.

Which one of the following options is valid for the above two statements?

A. Both are false
B. Statement (i) is true and the other is false
C. Statement (ii) is true and the other is false
D. Both are true

gate2007-it computer-networks network-security normal

Answer

2.30.6 Network Security: GATE2007-IT-18 top http://gateoverflow.in/3451

A firewall is to be configured to allow hosts in a private network to freely open TCP connections and send packets on open connections. However, it will only allow external hosts to send packets on existing open TCP connections or connections that are being opened (by internal hosts) but not allow them to open TCP connections to hosts in the private network. To achieve this the minimum capability of the firewall should be that of

A. A combinational circuit
B. A finite automaton
C. A pushdown automaton with one stack
D. A pushdown automaton with two stacks

gate2007-it computer-networks theory-of-computation normal network-security

Answer

2.30.7 Network Security: GATE2007-IT-70 top http://gateoverflow.in/3515

Your are given the following four bytes :

10100011	00110111	11101001	10101011

Which of the following are substrings of the base 64 encoding of the above four bytes ?

A. zdp
B. fpq
C. qwA
D. oze

gate2007-it computer-networks network-security normal

Answer

2.30.8 Network Security: GATE2008-IT-70 top http://gateoverflow.in/3384

The total number of keys required for a set of n individuals to be able to communicate with each other using secret key and public key cryptosystems, respectively are:

A. n(n-1) and 2n
B. 2n and ((n(n - 1))/2)
C. ((n(n - 1))/2) and 2n
D. ((n(n - 1))/2) and n

gate2008-it computer-networks network-security normal

Answer

2.30.9 Network Security: GATE2009-46 top

http://gateoverflow.in/1332

In the RSA public key cryptosystem, the private and public keys are (e,n) and (d,n) respectively, where $n = p \times q$ and p and q are large primes. Besides, n is public and p and q are private. Let M be an integer such that $0 < M < n$ and $\phi(n) = (p-1)(q-1)$. Now consider the following equations.

I. $M' = M^e \bmod n$
$M = (M')^d \bmod n$

II. $ed \equiv 1 \bmod n$

III. $ed \equiv 1 \bmod \phi(n)$

IV. $M' = M^e \bmod \phi(n)$
$M = (M')^d \bmod \phi(n)$

Which of the above equations correctly represents RSA cryptosystem?

A. I and II
B. I and III
C. II and IV
D. III and IV

gate2009 computer-networks network-security normal

Answer

2.30.10 Network Security: GATE2013_13 top

http://gateoverflow.in/1435

Using public key cryptography, X adds a digital signature σ to message M, encrypts $< M, \sigma >$, and sends it to Y, where it is decrypted. Which one of the following sequences of keys is used for the operations?

(A) Encryption: X's private key followed by Y's private key; Decryption: X's public key followed by Y's public key

(B) Encryption: X's private key followed by Y's public key; Decryption: X's public key followed by Y's private key

(C) Encryption: X's public key followed by Y's private key; Decryption: Y's public key followed by X's private key

(D) Encryption: X's private key followed by Y's public key; Decryption: Y's private key followed by X's public key

gate2013 computer-networks network-security normal

Answer

2.30.11 Network Security: GATE2014-1-24 top

http://gateoverflow.in/1791

Which of the following are used to generate a message digest by the network security protocols?

I. RSA
II. SHA-1
III. DES
IV. MD5

A. I and III only
B. II and III only
C. II and IV only
D. III and IV only

gate2014-1 computer-networks network-security normal

Answer

2.30.12 Network Security: GATE2014-2-27 top http://gateoverflow.in/1986

An IP machine Q has a path to another IP machine H via three IP routers R1, R2, and R3.

$Q - R1 - R2 - R3 - H$

H acts as an HTTP server, and Q connects to H via HTTP and downloads a file. Session layer encryption is used, with DES as the shared key encryption protocol. Consider the following four pieces of information:

$[I1]$ The URL of the file downloaded by Q

$[I2]$ The TCP port numbers at Q and H

$[I3]$ The IP addresses of Q and H

$[I4]$ The link layer addresses of Q and H

Which of I1, I2, I3, and I4 can an intruder learn through sniffing at R2 alone?

A. Only I1 and I2
B. Only I1
C. Only I2 and I3
D. Only I3 and I4

gate2014-2 computer-networks network-security normal

Answer

2.30.13 Network Security: GATE2015-1_21 top http://gateoverflow.in/8244

Suppose that everyone in a group on N people wants to communicate secretly with the N - 1 others using symmetric Key cryptographic system. The communication between any two person should not be decodable by the others in the group. The numbers of keys required in the system as a whole to satisfy the confidentiality requirement is

A. 2N
B. N(N - 1)
C. N(N - 1)/2
D. $(N - 1)^2$

gate2015-1 computer-networks network-security normal

Answer

2.30.14 Network Security: TIFR2011-B-36 top http://gateoverflow.in/20918

Consider malware programs. Which of the following is true?

a. A worm is a parasite.
b. A virus cannot affect a linux operating system.
c. A trojan can be in the payload of only a worm.
d. A worm and virus are self replicating programs.
e. There is no difference between a virus and a worm.

tifr2011 computer-networks network-security

Answer

Answers: Network Security

2.30.1 Network Security: GATE 2016-1-52 top http://gateoverflow.in/39694

Selected Answer

B wants to send message 'm' to A.
Private keys are denoted by $K^-(x)$ and public keys by $K^+(x)$.
In digital signature, the private key of sender is used to encrypt the message and its public key is used to decrypt.
So, {m, K^-(B)(H(m))} must be the correct way of sending the message.
Option B.

26 votes -- Monanshi Jain (8.5k points)

2.30.2 Network Security: GATE2004-IT-25 top

http://gateoverflow.in/3666

Selected Answer

A) Sender encrypts using receiver's public key

13 votes -- Omesh Pandita (2.7k points)

2.30.3 Network Security: GATE2004-IT-84 top

http://gateoverflow.in/3728

Selected Answer

Let x1, x2 and x3 are data bits, and c1, c2, c3 and c4 are parity check bits.

Given transmitted codewords are

x1	x2	x3	c1	c2	c3	c4
0	1	0	1	0	1	1
1	0	0	1	1	0	1
1	1	1	0	0	0	1

By inspection, we can find the rule for generating each of the parity bits –

x1	x2	x3	x1⊕x2	x1⊕x3	x2⊕x3	x1⊕x2⊕x3
0	1	0	1	0	1	1
1	0	0	1	1	0	1
1	1	1	0	0	0	1

Now we can not only eliminate options, we can also find the set of all eight code words using x1, x2 and x3.

x1	x2	x3	x1⊕x2	x1⊕x3	x2⊕x3	x1⊕x2⊕x3
0	0	0				
0	0	1				
0	1	0	1	0	1	1
0	1	1				
1	0	0	1	1	0	1
1	0	1				

1	1	0				
1	1	1	0	0	0	1

We can fill all remaining entries above :)

Now i am directly writing answer, Option **A** is correct choice !

26 votes -- Sachin Mittal (7.1k points)

The simplest way to solve this is to use XOR property of codewords which says that XOR of two codewords is itself a codeword.
Upon XORing 1st and 3rd codeword we get another codeword **1011010**, which is III .
And on XORing this new generated codeword with 2nd codeword given we get **0010111**, which is I.

Hence Answer = **A**

21 votes -- learncp (1.4k points)

2.30.4 Network Security: GATE2005-IT-79 top

http://gateoverflow.in/3843

Selected Answer

For Diffie-Hellman the secret is g^a^b mod p , where g is the prime root (or generator) and p is the modulus.

So the answer should be (3^10) mod 7 which is B) 4.

13 votes -- Omesh Pandita (2.7k points)

2.30.5 Network Security: GATE2007-IT-15 top

http://gateoverflow.in/3448

Selected Answer

Answer: C

i. Hash function is not one one or injective. It is many to one.

ii. True. Uses P-Box permutation.

13 votes -- Rajarshi Sarkar (35k points)

2.30.6 Network Security: GATE2007-IT-18 top

http://gateoverflow.in/3451

Selected Answer

A) A combinational circuit => Not possible, because we need memory in Firewall, Combinational ckt has none.
B) A finite automaton => We need infinite memory, there is no upper limit on Number of TCP ckt so Not this.
C) A pushdown automaton with one stack => Stack is infinite. Suppose we have 2 connections , we have pushed details of those on stack we can not access the details of connection which was pushed first, without popping it off. So Big NO.
D) A pushdown automaton with two stacks => This is TM. It can do everything our normal computer can do so Yes. Firewall can be created out of TM.

23 votes -- Akash (43.8k points)

2.30.7 Network Security: GATE2007-IT-70 top

http://gateoverflow.in/3515

Selected Answer

Your are given the following four bytes :

10100011 00110111 11101001 10101011 =32**+ ADD 4 0's** = 36
accoding to wikipedia, make pair of 6 should be made. https://en.wikipedia.org/wiki/Base64

101000 110011 011111 101001 101010 11**0000**
40 51 31 41 42 48

o z f p q w from base 64 table.
now the longest substring will be from option checking is '**fpq**'

7 votes -- Jayesh10 (175 points)

2.30.8 Network Security: GATE2008-IT-70 top

http://gateoverflow.in/3384

Selected Answer

For private key crypto for communication between each pair of individuals on secret key will be required, so if a individual wants to communicate with other n-1 individuals he should have n-1 secret keys, so the total number of secret keys for private encryption is n*(n-1) (If we include copies) or n*(n-1)/2 (distinct keys).

For public key encryption each individual needs to have a public and private key, so the total keys required in 2*n

From the tone of the question the answer seems to be C) n(n-1)/2 and 2n

21 votes -- Omesh Pandita (2.7k points)

2.30.9 Network Security: GATE2009-46 top

http://gateoverflow.in/1332

Selected Answer

The basic principle behind RSA is the observation that it is practical to find three very large positive integers e, d and n such that with modular exponentiation for all m:

$(m^e)^d \equiv m \pmod{n}$ and that even knowing e and n or even m it can be extremely difficult to find d.

Additionally, for some operations it is convenient that the order of the two exponentiations can be changed and that this relation also implies: $(m^d)^e \equiv m \pmod{n}$

The keys for the RSA algorithm are generated the following way:

- Choose two distinct prime numbers p and q.
- Compute $n = pq$.
- Compute $\varphi(n) = \varphi(p)\varphi(q) = (p-1)(q-1)$
- This is more clearly stated as: solve for d given $d{\cdot}e \equiv 1 \pmod{\varphi(n)}$

so B is answer

9 votes -- Prashant Singh (49.2k points)

2.30.10 Network Security: GATE2013_13 top

http://gateoverflow.in/1435

Selected Answer

X adds his digital signature: In order to identify the authentic user, X uses his**Private Key** to encrypt his signature.

X then encrypts the whole message with the digital signature: X uses Y's**Public Key** to encrypt the message so that Y can decipher it when it reaches to him using his private key.

Message then reaches Y.

Y then uses his **Private key** to decrypt the message, and extracts the message and along with the signature.

But as the signature has been encrypted using X's private key so:

Y uses X's **Public Key** to see the signature if it matches X's actual signature (this step ensures that no one can fake as X and sends a message to Y).

Nobody can tamer the message as in order to do that he/she has to first know Y's private key to decipher the message extract the signature and then change the signature and then recreate that using X's private key which is not with him.

So sequence of operations:

X's Private Key -> Y's public key -> Y's Private key -> X's public Key which is **(D).**

16 votes -- Santanu Naskar (209 points)

2.30.11 Network Security: GATE2014-1-24 top http://gateoverflow.in/1791

Selected Answer

- RSA – It is an algorithm used to **encrypt and decrypt** messages.
- SHA 1 – Secure Hash Algorithm 1, or SHA 1 is a **cryptographic hash function**. It produces a 160 bit (20 byte) hash value (message digest).
- DES – Data Encryption Standard, or DES is a **symmetric key algorithm for encryption** of electronic data.
- MD5 – Message Digest 5, or MD5 is a widely used **cryptographic hash function** that produces a 128 bit hash value (message digest).

II and IV i.e SHA 1 and MD5 are used to generate a message digest by the network security protocols. So, C is the correct choice.

3 votes -- Divya Bharti (4k points)

RSA and DES are used for Encryption where MD5 and SHA 1 are used to generate Message Digest.

15 votes -- Shiva Chaitanya Gajula (573 points)

2.30.12 Network Security: GATE2014-2-27 top http://gateoverflow.in/1986

Selected Answer

[I1] intruder cant see URL because it is well encrypted by DES at session layer..
[I2] TCP PORT number available to intruder because TCP header contains source as well as destination address.

[I3] Network layer header contains Source as Well as Destination IP.
[I4] Link address unavailable because on sniffing at R2 intruder can see link address of R1, R3 ,only not link address of Q and H

Answer is **C**

16 votes -- Digvijay (47k points)

2.30.13 Network Security: GATE2015-1_21 top http://gateoverflow.in/8244

Selected Answer

In symmetric key cryptographic system, both parties have access to key. So, the first person has N-1 keys with other N-1 people, second one has another N-2 with N-2 people (1 we already considered) and so on till 1. So, total number of keys required

= N-1 + N-2 + ... + 1

= N(N-1)/2

C choice.

Had we been using Public key cryptography we needed just 2N keys in the system.

Ref: https://en.wikipedia.org/wiki/Symmetric-key_algorithm

15 votes -- Arjun Suresh (294k points)

2.30.14 Network Security: TIFR2011-B-36 top http://gateoverflow.in/20918

- A worm is a parasite. **False**

ANS: worm is a standalone malware computer program that replicates itself in order to spread to other computers.

- A virus cannot affect a linux operating system. **False**

ANS: virus can affect any operating system.

- A trojan can be in the payload of only a worm. **False**
- A worm and virus are self replicating programs. **True**

ANS: worm and virus is self replicating programs But trojan are not.

- There is no difference between a virus and a worm. **False**

ANS: since worm are standalone software and do not require a host program or human help to propagate.

So D is choice

6 votes -- Prashant Singh (49.2k points)

2.31 Network Switching(4) top

2.31.1 Network Switching: GATE2004-IT-22 top http://gateoverflow.in/3663

Which one of the following statements is FALSE?

A. Packet switching leads to better utilization of bandwidth resources than circuit switching
B. Packet switching results in less variation in delay than circuit switching
C. Packet switching requires more per-packet processing than circuit switching
D. Packet switching can lead to reordering unlike in circuit switching

gate2004-it computer-networks network-switching normal

Answer

2.31.2 Network Switching: GATE2005-73 top http://gateoverflow.in/1396

In a packet switching network, packets are routed from source to destination along a single path having two intermediate nodes. If the message size is 24 bytes and each packet contains a header of 3 bytes, then the optimum packet size is:

A. 4
B. 6
C. 7
D. 9

gate2005 computer-networks network-switching normal

Answer

2.31.3 Network Switching: GATE2014-2-26 top http://gateoverflow.in/1985

Consider the store and forward packet switched network given below. Assume that the bandwidth of each link is 10^6 bytes / sec. A user on host A sends a file of size 10^3 bytes to host B through routers R1 and R2 in three different ways. In the first case a single packet containing the complete file is transmitted from A to B. In the second case, the file is split into 10 equal parts, and these packets are transmitted from A to B. In the third case, the file is split into 20 equal parts and these packets are sent from A to B. Each packet contains 100 bytes of header information along with the user data. Consider only transmission time and ignore processing, queuing and propagation delays. Also assume that there are no errors during transmission. Let T1, T2 and T3 be the times taken to transmit the file in the first, second and third case respectively. Which one of the following is CORRECT?

A. $T < T2 < T3$
B. $T1 > T2 > T3$
C. $T2 = T3, T3 < T1$
D. $T1 = T3, T3 > T2$

gate2014-2 computer-networks network-switching normal

Answer

2.31.4 Network Switching: GATE2015-3_36 top

http://gateoverflow.in/8495

Two hosts are connected via a packet switch with 10^7 bits per second links. Each link has a propagation delay of 20 microseconds. The switch begins forwarding a packet 35 microseconds after it receives the same. If 10000 bits of data are to be transmitted between the two hosts using a packet size of 5000 bits, the time elapsed between the transmission of the first bit of data and the reception of the last bit of the data in microseconds is _______.

gate2015-3 computer-networks normal numerical-answers network-switching

Answer

Answers: Network Switching

2.31.1 Network Switching: GATE2004-IT-22 top

http://gateoverflow.in/3663

Selected Answer

Answer B

In circuit switching, a fix bandwidth is allocated to each connection, e.g. 64 Kb/s allocated to each each phone call.

In circuit switching each connection has a dedicated circuit or channel all the way along the path and the circuit is not shared with anyone else.

Thus in circuit switching each call has its own private, guaranteed, isolated data rate from end to end.So we can say that every connection or flow is independent of others.

In the case of packet switching, all flows share the full channel capacity by statistical multiplexing.

So the bandwidth allocated to each flow depends upon the number of concurrent flows & network traffic.

In packet switching if we know the type of link we are using, the bandwidth allocated, the packet size for any flow then we can calculate the Propagation Delay & Transmission Delays.

But **Queueing Delay is a random variable that depends upon the number of packets arriving at the same time at any switch.**

It is the only random variable in our end to end delay expression.All other delays can be calculated precisely if we have enough information about the flows.

So queueing adds unpredictable & variable delays in the packet switching.

There are delays like propagation delay etc. in circuit switching but they have a very small variance because of independence, privacy & bandwidth guarantees.

19 votes -- Anurag Pandey (13.1k points)

2.31.2 Network Switching: GATE2005-73 top

http://gateoverflow.in/1396

Selected Answer

correct answer should be option (d)

As we know in packet switching .... dividing message into packets decrease the transmission time due to pipelined transmission.

but if there are many packets beyond some threshold then transmission time may increase .. so we can do by option checking

1. packet size =4 = packet data + header size = 1+3 ...so no of packets will be = message / packet data = 24B/1B = 24 packets ...

so time to reach at receiver for 1st packet will be = 3(source + two intermediate node)* transmission time

TT= L/BW... here L will be changed according to option and BW will remain same ..

so time to reach at receiver for 1st packet will be= 3*4/BW= 12/BW

and for remaining 23 packets will take time = 23 *TT= 23* 4/BW= 92/BW

TOTAL TIME = 104/BW

2. packet size = 6 = 3+3 (packet data + header size) so no of packets will be 8.

time to reach at receiver for 1st packet will be= 3*6/BW= 18/BW

and for remaining 7 packet will take time = 7*6/BW= 42/BW

total time = 60/BW

3. packet size = 7 = 4+3 ,so no of packets = 24/4=6 packets

for 1st packet time will be = 3*7/BW= 21/BW

for remaining 5 packet will take time= 5*7/BW= 35/BW

total time= 56/BW

4 . packet size =9. 6+3= so no of packet will be 4 .

for 1st packet time will be = 3*9/BW=27/BW

for remaining 3 packets will take time= 3*9/BW= 27/BW

TOTAL time= 54/BW

SO optimal packet size will be 9 byte due to less total transmission time.

Alternate method (thanks to sachin)

In that case we can do it using minimisation of a variable.

Let 24 byte data is divided into number of packets each have x byte of data.

Therefore packet size = x+3, and Number of packets (**k**) = $24/x$. (it is ceil, if 24 is not multiple of x)

total time = 3(x+3)+ (k-1)(x+3) (assumed BW =1, just to avoid writing "BW" again and again)

(ignoring propagation delay as it has nothing to do with packet size, if one wish he/she can add that too but later he will realize it will anyway become zero while differentiating.)

$\Longrightarrow$ total time = 2x+3k+kx+6 (k is equal to 24/x)

$\Longrightarrow$ total time = $2x+(3\times 24/x)+(24/x\times x)+6$

$\Longrightarrow$ total time = $2x+72/x+30$

to minimise this time, diffrentiation should be 0.

that gives, $2-72/x^2 = 0$

$\Longrightarrow x=6$

including 3 bytes of header, packet size = 9 Bytes.

Option **D**.

26 votes -- sonam vyas (13.2k points)

option D

packet size P = p+h where h is header size and p = √(hx / k-1) where x is message size and k is no of hopes.

so p= √(3*24 / 2) = √ (72 / 2) = √36 = 6

so optimum packet size is 6 + 3 = 9

16 votes -- skrahul (603 points)

2.31.3 Network Switching: GATE2014-2-26 top http://gateoverflow.in/1985

Selected Answer

In this question we have used the concept of pipelining.

In second and Third case, First packet will take $3*T_t$ time and all subsequent packets will be delivered in one T_t time.

$T1 = 3 * T_t = 3 * (1000+ 100) / B$

T_t = (data + header)/ Bandwidth

data = 1000 Bytes; header = 100 Bytes

$T1 = 3300/B$ seconds

$T2 = 3 * T_t' + 9 * T_t' = 12 * T_t'$

T_t' = (data + header)/ Bandwidth

$T2 = 12* (100 + 100) / B= 2400/ B$ seconds

$T3 = 3 * T_t'' + 19 * T_t'' = 22 * T_t''$

$T_t'' = (50 + 100) / B$

$T3 = 22 * 150 / B = 3300 / B$

So T1 = T3 and T3 > T2;

option D

45 votes -- Vikrant Singh (13.4k points)

2.31.4 Network Switching: GATE2015-3_36 top http://gateoverflow.in/8495

Selected Answer

No. of packets sent = 10000/5000 = 2.

Time for the first packet to reach switch = Transmission time + Propagation delay
= $(5000/10^7) *10^6$ μs + 20 μs

= 520 μs.

(Another 520 μs is required for the same packet to reach the destination from the switch and in between there is a forwarding delay of 35 μs. So, first packet is received at destination at 2 * 520 + 35 = 1075 μs.)

After 520 μs, the switch can start receiving the second packet and at 520 + 500 = 1020 μs, second frame is completely received by the switch (we don't need to add propagation time here as packet 2 can just follow packet 1). So, at 1055 μs from the start the switch starts sending the second packet and this will be received at destination after another 520 μs = 1575 μs. Since we added transmission time, this ensures that the last bit of data is received at the sender.

EDIT:-

(Alternate solution)

We can Think the same question in terms of last packet, argument here is: The moment last packet reaches to destination, all other packets are already reached.

Total time = Transmission time of all packets $+$ Propagation time for first link $+$ Switch Delay $+$ Transmission time of last packet for Switch $+$ propagation time for 2nd link.

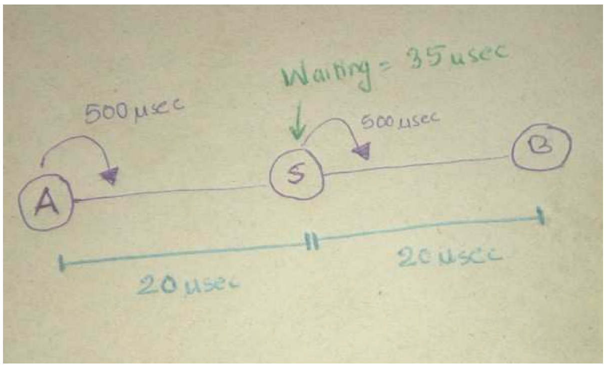
= $\left(\frac{10^4}{10^7} sec = 1ms = 1000\mu s\right)$ 1000 $+$ 20 $+$ 35 $+$ 500 $+$ 20 = 1575μs

31 votes -- Arjun Suresh (294k points)

$\text{number of packets send } = \frac{10000}{5000} = 2$

$\text{Transmission Time } = \frac{5000}{10^7} = 500$ micro seconds

$\text{Propogation Time } = 20$ micro seconds



packet 1

At t=0
packet starts from source
At t=500
packet 1 is fully transmitted by source. Now it is availble in the link

At t=520
packet 1 is availbe at swich

At t=555
packet transmission starts from switch after waiting for 35μs

At t= 1055
packet 1 is fully transmitted by switch . Now it is availble in the link

At t=1075
packet 1 reaches Receiver.

packet 2

At t=500
packet starts from source

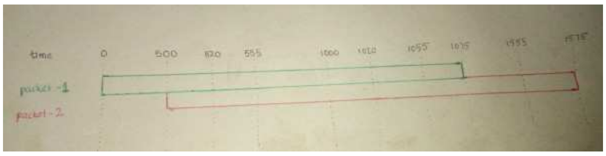
At t=1000
packet 2 is Now available in the Link. Fully transmitted from source .packet 2 Now, begins to propogate to Switch

At t=1020
packet 2 now reachs switch

At t= 1055
packet transmission starts from switch after waiting for 35μs

At t=1555
packet 2 is fully transmitted by switch . Now it is availble in the link

At t=1575
packet 2 Reaches destination



👍 47 votes -- pC (21.4k points)

2.32 Osi Protocol(1) top

2.32.1 Osi Protocol: GATE2014-3-23 top http://gateoverflow.in/2057

In the following pairs of OSI protocol layer/sub-layer and its functionality, the **INCORRECT** pair is

A. Network layer and Routing
B. Data Link Layer and Bit synchronization
C. Transport layer and End-to-end process communication
D. Medium Access Control sub-layer and Channel sharing

gate2014-3 computer-networks network-layering osi-protocol easy

Answer

Answers: Osi Protocol

2.32.1 Osi Protocol: GATE2014-3-23 top http://gateoverflow.in/2057

Selected Answer

Answer is B) Data Link Layer & Bit Synchronization.

Because, Data Link Layer is associated with Frame Synchronization, and not Bit Synchronization.

👍 18 votes -- saurabhrk (1.5k points)

2.33 Routers Bridge Hubs Switches(1) top

2.33.1 Routers Bridge Hubs Switches: GATE2004-16 top http://gateoverflow.in/1013

Which of the following is NOT true with respect to a transparent bridge and a router?

A. Both bridge and router selectively forward data packets
B. A bridge uses IP addresses while a router uses MAC addresses
C. A bridge builds up its routing table by inspecting incoming packets
D. A router can connect between a LAN and a WAN

gate2004 computer-networks routers-bridge-hubs-switches normal

Answer

Answers: Routers Bridge Hubs Switches

2.33.1 Routers Bridge Hubs Switches: GATE2004-16 top http://gateoverflow.in/1013

Selected Answer

A. Both bridge and router selectively forward data packets => True. Bridge can drop packets not meant for other side, so can router.

B. A bridge uses IP addresses while a router uses MAC addresses => False . A bridge operate at layer 2 (data link layer) so it uses MAC address, while router at layer 3 (network layer) so it using IP addresse

C. A bridge builds up its routing table by inspecting incoming packets => True. Self Learning Bridges

D. A router can connect between a LAN and a WAN => True. Router connecting home LAN To internet !

11 votes -- Akash (43.8k points)

2.34 Routing(8) top

2.34.1 Routing: GATE2005-26 top http://gateoverflow.in/1362

In a network of LANs connected by bridges, packets are sent from one LAN to another through intermediate bridges. Since more than one path may exist between two LANs, packets may have to be routed through multiple bridges. Why is the *spanning tree algorithm* used for bridge-routing?

A. For shortest path routing between LANs

B. For avoiding loops in the routing paths

C. For fault tolerance

D. For minimizing collisions

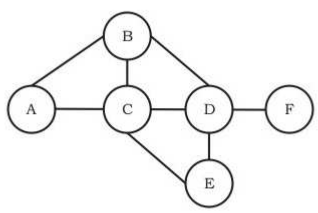
gate2005 computer-networks routing normal

Answer

2.34.2 Routing: GATE2005-IT-85a top http://gateoverflow.in/3858

Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updation interval, three tasks are performed.

i. A node determines whether its neighbours in the graph are accessible. If so, it sets the tentative cost to each accessible neighbour as 1. Otherwise, the cost is set to ∞.
ii. From each accessible neighbour, it gets the costs to relay to other nodes via that neighbour (as the next hop).
iii. Each node updates its routing table based on the information received in the previous two steps by choosing the minimum cost.



For the graph given above, possible routing tables for various nodes after they have stabilized, are shown in the following options. Identify the correct table.

A. Table for node A

A	-	-
B	B	1
C	C	1
D	B	3
E	C	3
F	C	4

B. Table for node C

A	A	1
B	B	1

C	-	-
D	D	1
E	E	1
F	E	3

C. Table for node B

A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

D. Table for node D

A	B	3
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

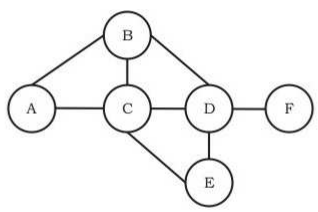
gate2005-it computer-networks routing normal

Answer

2.34.3 Routing: GATE2005-IT-85b top http://gateoverflow.in/3859

Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updation interval, three tasks are performed.

i. A node determines whether its neighbours in the graph are accessible. If so, it sets the tentative cost to each accessible neighbour as 1. Otherwise, the cost is set to ∞.
ii. From each accessible neighbour, it gets the costs to relay to other nodes via that neighbour (as the next hop).
iii. Each node updates its routing table based on the information received in the previous two steps by choosing the minimum cost.



Continuing from the earlier problem, suppose at some time t, when the costs have stabilized, node A goes down. The cost from node F to node A at time (t + 100) is :

A. > 100 but finite
B. ∞
C. 3
D. > 3 and ≤ 100

gate2005-it computer-networks routing normal

Answer

2.34.4 Routing: GATE2007-IT-63 top http://gateoverflow.in/3508

A group of 15 routers are interconnected in a centralized complete binary tree with a router at each tree node. Router i communicates with router j by sending a message to the root of the tree. The root then sends the message back down to router j. The mean number of hops per message, assuming all possible router pairs are equally likely is

A. 3
B. 4.26
C. 4.53
D. 5.26

gate2007-it computer-networks routing binary-tree normal

Answer

2.34.5 Routing: GATE2008-IT-67 top http://gateoverflow.in/3381

Two popular routing algorithms are Distance Vector(DV) and Link State (LS) routing. Which of the following are true?

(S1): Count to infinity is a problem only with DV and not LS routing
(S2): In LS, the shortest path algorithm is run only at one node
(S3): In DV, the shortest path algorithm is run only at one node
(S4): DV requires lesser number of network messages than LS

A. S1, S2 and S4 only
B. S1, S3 and S4 only
C. S2 and S3 only
D. S1 and S4 only

gate2008-it computer-networks routing normal

Answer

2.34.6 Routing: GATE2014-2-23 top http://gateoverflow.in/1981

Which of the following is TRUE about the interior gateway routing protocols — Routing Information Protocol (RIP) and Open Shortest Path First $(OSPF)$

A. RIP uses distance vector routing and OSPF uses link state routing
B. OSPF uses distance vector routing and RIP uses link state routing
C. Both RIP and OSPF use link state routing
D. Both RIP and OSPF use distance vector routing

gate2014-2 computer-networks routing normal

Answer

2.34.7 Routing: GATE2014-3-26 top http://gateoverflow.in/2060

An IP router implementing Classless Inter-domain Routing (CIDR) receives a packet with address 131.23.151.76. The router's routing table has the following entries:

Prefix	Output Interface Identifier
131.16.0.0/ 12	3
131.28.0.0/ 14	5
131.19.0.0/ 16	2
131.22.0.0/ 15	1

The identifier of the output interface on which this packet will be forwarded is _______.

gate2014-3 computer-networks routing normal numerical-answers

Answer

2.34.8 Routing: GATE2017-2-09 top http://gateoverflow.in/118338

Consider the following statements about the routing protocols. Routing Information Protocol (RIP) and Oprn Shortest Path First (OSPF) in an IPv4 network.

I. RIP uses distance vector routing
II. RIP packets are sent using UDP
III. OSPF packets are sent using TCP
IV. OSPF operation is based on link-state routing

Which of the above statements are CORRECT?

A. I and IV only
B. I, II and III only
C. I, II and IV only
D. II, III and IV only

gate2017-2 computer-networks routing

Answer

Answers: Routing

2.34.1 Routing: GATE2005-26 top http://gateoverflow.in/1362

Selected Answer

The answer is B.

Since, in a spanning tree, there is a unique path from a source to the destination, which avoids loops, since it is a tree, and contains all the nodes, since it is a spanning tree.

11 votes -- saurabhrk (1.5k points)

2.34.2 Routing: GATE2005-IT-85a top http://gateoverflow.in/3858

Selected Answer

Table for node A

A	-	-
B	B	1
C	C	1
D	B	2
E	C	2
F	C	3

Table for node D

A	B	2
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

Table for node C

A	A	1
B	B	1
C	-	-
D	D	1
E	E	1
F	D	2

Table for node B

A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

correct table are updated

only option C is matching here with given tables

6 votes -- Prashant Singh (49.2k points)

2.34.3 Routing: GATE2005-IT-85b top http://gateoverflow.in/3859

Selected Answer

We consider A B D F at t they are

The distance between A and the nodes B,D,F respectively are:
t: 1 2 3

t+1: 3 2 3

t+2 :3 4 3

t+3: 5 4 5

t+4: 5 6 5

t+5: 7 6 7

t+6: 7 8 7

t+7: 9 8 9

t+8: 9 10 9
and this continues

so in every two steps they get incremented by 2

so at t+99 F is 101

at t+100 F is 101

So count to infinity problem
so option A

10 votes -- Shreya Roy (3.7k points)

A)..the cost would be 102.

14 votes -- Shaun Patel (6.9k points)

2.34.4 Routing: GATE2007-IT-63 top http://gateoverflow.in/3508

Selected Answer

OPTION C

Here, we have to count average hops per message.

Steps -

1) Message goes up from sender to root

2) Message comes down from root to destination

---

1) Average hops message goes to root -
$\frac{(3*8)+(2*4)+(1*2)+(0*1)}{15}$ = 2.267

Here 3 * 8 represents 3 hops & 8 routers for Bottommost level & So on..

---

2) Similarly average hops when message comes down -
$\frac{(3*8)+(2*4)+(1*2)+(0*1)}{15}$ {Same as above}

So, Total Hops = 2 * 2.267 = **4.53 (Ans)**

43 votes -- Himanshu Agarwal (16.2k points)

The path length differs for nodes from each level. For a node in level 4, we have maximum no. of hops as follows

Level	Max. no. of hops
1	3 (3-2-1)
2	3+1 = 4 (3-2-1-2)
3	3 + 2 = 5 (3-2-1-2-3)
4	3 + 3 = 6 (3-2-1-2-3-4)

So, mean no. of hops for a node in level 4

$= \frac{1.3+2.4+4.5+7.6}{14} = \frac{73}{14}$, as we have 1, 2, 4 and 8 nodes respectively in levels 1, 2, 3 and 4 and we discard the source one in level 4.

Similarly, from a level 3 node we get mean no. of hops,

$$= \frac{1.2+2.3+3.4+8.5}{14} = \frac{60}{14}$$

From level 2, we get mean no. of hops

$$= \frac{1.1+1.2+4.3+8.4}{14} = \frac{47}{14}$$

And from level 1, we get, mean no. of hops

$$= \frac{0+2.1+4.2+8.3}{14} = \frac{34}{14}.$$

So, now we need to find the overall mean no. of hops which will be

$$= \frac{\text{Sum of mean no. of hops for each node}}{\text{No. of nodes}} = \frac{\frac{73}{14}\times8+\frac{60}{14}\times4+\frac{47}{14}\times2+\frac{34}{14}\times1}{15} = \frac{68}{15} = 4.53$$

13 votes -- Arjun Suresh (294k points)

2.34.5 Routing: GATE2008-IT-67 top

http://gateoverflow.in/3381

Selected Answer

S1 is true, S2 and S3 are false and S4 is true.

Link State: https://cseweb.ucsd.edu/classes/fa10/cse123/lectures/123-fa10-l12.pdf

Distance Vector: http://cseweb.ucsd.edu/classes/fa10/cse123/lectures/123-fa10-l13.pdf

14 votes -- Arjun Suresh (294k points)

2.34.6 Routing: GATE2014-2-23 top

http://gateoverflow.in/1981

Selected Answer

ans a)

11 votes -- Aditi Dan (5.3k points)

2.34.7 Routing: GATE2014-3-26 top

http://gateoverflow.in/2060

Selected Answer

Answer: (1)

Exp: Given address 131.23.151.76.coming to the first field of given routing table

$\Rightarrow$ 131.16.0.0/12

131.0001 0111.151.76

131.0001 0000.0.0 ($\because$ given mask bits = 12)

$\Rightarrow$ 131.16.0.0 Matched

Coming to the 2nd field of given Routing table

$\Rightarrow$ 131.28.0.0/14

131.0001 0111.151.76

131.0001 0100.0.0 ($\because$ given mask bits = 14)

$\Rightarrow$ 131.20.0.0 Not matched.

Coming to the 3rd field of given Routing table

Error! Not a valid link. 131.19.0.0/16

131.0001 0111.151.76

131.0001 0111.0.0 ($\because$ given mask bits = 16)

$\Rightarrow$ 131.23.0.0 Not matched

Coming to the 4th field of given Routing table

$\Rightarrow$ 131.22.0.0/15

131.0001 0111.151.76

131.0001 0110.0.0 ($\because$ given mask bits = 15)

$\Rightarrow$ 131.22.0.0 Matched

We are getting 1st and 4th entries are matched so among them we have to picked up the longest mask bit , so output interface identifier is 1.

Hence Answer is Interface **1**

👍 15 votes -- saurabhrk (1.5k points)

2.34.8 Routing: GATE2017-2-09 top http://gateoverflow.in/118338

Selected Answer

Statement 1 is **CORRECT** Bcoz RIP is one of the Oldest DVR(Distance Vector Routing) Protocols which employ the hop count as a routing metric.

Statement 2 is **CORRECT** Bcoz RIP uses the UDP as its transport protocol with port no 520.

Statement 3 is **INCORRECT** Bcoz OSPF doesnot use a transport protocol such as UDP or TCP but encapsulates its data directly into IP Packets.

Statement 4 is **CORRECT** Bcoz OSPF is a routing protocol which uses Link State Routing(LSR) and works within a single Autonomous System.

PS:

OSPF needs to perform reliable multicasting because it needs to talk to multiple possible neighbors on the same network segment. Now, TCP does not support multicast and UDP is not reliable Therefore, OSPF implements its own transport mechanism that allows both for reliability (acknowledgements and retransmissions of lost segments) and multicasting, bypassing both TCP and UDP.

Hence, Option C is CORRECT.

👍 9 votes -- G VENKATESWARLU (619 points)

2.35 Rsa Security Networks(1) top

2.35.1 Rsa Security Networks: GATE2017-1-44 top http://gateoverflow.in/118327

In a RSA cryptosystem, a participant A uses two prime numbers $p = 13$ and $q = 17$ to generate here public and private keys. If the public key of A is 35, then the private key of A is ___________ .

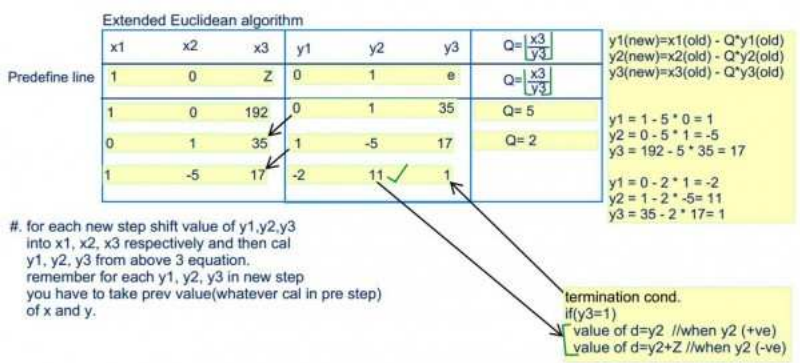
gate2017-1 network-security computer-networks rsa-security-networks numerical-answers normal

Answer

Answers: Rsa Security Networks

2.35.1 Rsa Security Networks: GATE2017-1-44 top http://gateoverflow.in/118327

Selected Answer



Efficient for bigger values

👍 4 votes -- 2018 (5.2k points)

2.36 Selective Repeat(1) top

2.36.1 Selective Repeat: GATE 2016-2-55 top http://gateoverflow.in/39577

Consider a 128×10^3 bits/second satellite communication link with one way propagation delay of 150 milliseconds. Selective retransmission (repeat) protocol is used on this link to send data with a frame size of 1 kilobyte. Neglect the transmission time of acknowledgement. The minimum number of bits required for the sequence number field to achieve 100% utilization is ________.

gate2016-2 computer-networks selective-repeat normal numerical-answers

Answer

Answers: Selective Repeat

2.36.1 Selective Repeat: GATE 2016-2-55 top http://gateoverflow.in/39577

Selected Answer

Answer is 4 bits.

As we want 100 percent efficiency, ws=1+2a

$$a = \frac{\text{propagation time}}{\text{transmission time}} = \frac{150}{1024{\times}8/128} = \frac{150}{64} = 2.34, \implies ws = 1 + 2a = 5.6875 \approx 6$$

Available seq numbers>= ws+wr

In Selective Repeat,

ws=wr(let it be n)

2*n=2*6=12

avail seq numbers>=12

so minimum seq numbers are 12

number of bits for that is ceil of $\lceil \log_2 12 \rceil = 4.$

28 votes

-- Sreyas S (1.7k points)

2.37 Serial Communication(3) top

2.37.1 Serial Communication: GATE1992_03,v top http://gateoverflow.in/582

Start and stop bits do not contain any "information" but are used in serial communication for

A. Error detection
B. Error correction
C. Synchronization
D. Slowing down the communications.

gate1992 computer-networks easy serial-communication

Answer

2.37.2 Serial Communication: GATE1998_1.16 top http://gateoverflow.in/1653

In serial communication employing 8 data bits, a parity bit and 2 stop bits, the minimum band rate required to sustain a transfer rate of 300 characters per second is

A. 2400 band
B. 19200 band
C. 4800 band
D. 1200 band

gate1998 computer-networks communication serial-communication normal

Answer

2.37.3 Serial Communication: GATE2008-IT-18 top http://gateoverflow.in/3278

How many bytes of data can be sent in 15 seconds over a serial link with baud rate of 9600 in asynchronous mode with odd parity and two stop bits in the frame?

A. 10,000 bytes
B. 12,000 bytes
C. 15,000 bytes
D. 27,000 bytes

gate2008-it computer-networks communication serial-communication normal

Answer

Answers: Serial Communication

2.37.1 Serial Communication: GATE1992_03,v top http://gateoverflow.in/582

Selected Answer

Answer is C

3 votes -- saurabhrk (1.5k points)

2.37.2 Serial Communication: GATE1998_1.16 top http://gateoverflow.in/1653

Selected Answer

Since stop bit is given it is asynchronous communication and 1 start bit is implied. So,

(8 + 2 + 1 + 1) * 300 = 3600 bps

Minimum band rate required would be 4800 here.

6 votes -- Arjun Suresh (294k points)

2.37.3 Serial Communication: GATE2008-IT-18 top http://gateoverflow.in/3278

Selected Answer

Answer: B

Given that it is asynchronous mode of transmission, then along with per byte, you have to send some extra bit like start, stop bit and party bits,etc (start and stop bit are compulsory).

1 bit for start bit, 8 bits for data, 1 bit for parity, 2 bits for stop bits.

9600*15/(1+8+1+2) Byte = 12000 Byte.

13 votes -- Rajarshi Sarkar (35k points)

2.38 Sliding Window(15) top

2.38.1 Sliding Window: GATE2003-84 top http://gateoverflow.in/967

Host A is sending data to host B over a full duplex link. A and B are using the sliding window protocol for flow control. The send and receive window sizes are 5 packets each. Data packets (sent only from A to B) are all 1000 bytes long and the transmission time for such a packet is 50 µs. Acknowledgement packets (sent only from B to A) are very small and require negligible transmission time. The propagation delay over the link is 200 μs. What is the maximum achievable throughput in this communication?

A. 7.69×10^6 Bps

B. 11.11×10^6 Bps

C. 12.33×10^6 Bps

D. 15.00×10^6 Bps

gate2003 computer-networks sliding-window normal

Answer

2.38.2 Sliding Window: GATE2004-IT-81 top http://gateoverflow.in/3725

In a sliding window ARQ scheme, the transmitter's window size is N and the receiver's window size is M. The minimum number of distinct sequence numbers required to ensure correct operation of the ARQ scheme is

A. min (M, N)
B. max (M, N)
C. M + N
D. MN

gate2004-it computer-networks sliding-window normal

Answer

2.38.3 Sliding Window: GATE2004-IT-83 top http://gateoverflow.in/3727

A 20 Kbps satellite link has a propagation delay of 400 ms. The transmitter employs the "go back n ARQ" scheme with n set to 10. Assuming that each frame is 100 bytes long, what is the maximum data rate possible?

A. 5 Kbps
B. 10 Kbps
C. 15 Kbps
D. 20 Kbps

gate2004-it computer-networks sliding-window normal

Answer

2.38.4 Sliding Window: GATE2004-IT-88 top http://gateoverflow.in/3732

Suppose that the maximum transmit window size for a TCP connection is 12000 bytes. Each packet consists of 2000 bytes. At some point of time, the connection is in slow-start phase with a current transmit window of 4000 bytes. Subsequently, the transmitter receives two acknowledgements. Assume that no packets are lost and there are no time-outs. What is the maximum possible value of the current transmit window?

A. 4000 bytes
B. 8000 bytes
C. 10000 bytes
D. 12000 bytes

gate2004-it computer-networks sliding-window normal

Answer

2.38.5 Sliding Window: GATE2005-25 top http://gateoverflow.in/1361

The maximum window size for data transmission using the selective reject protocol with $n-bit$ frame sequence numbers is:

A. 2^n
B. 2^{n-1}

C. $2^n - 1$
D. 2^{n-2}

gate2005 computer-networks sliding-window easy

Answer

2.38.6 Sliding Window: GATE2006-44 top

http://gateoverflow.in/1820

Station A uses 32 byte packets to transmit messages to Station B using a sliding window protocol. The round trip delay between A and B is 80 milliseconds and the bottleneck bandwidth on the path between A and B is 128 kbps. What is the optimal window size that A should use?

A. 20
B. 40
C. 160
D. 320

gate2006 computer-networks sliding-window normal

Answer

2.38.7 Sliding Window: GATE2006-46 top

http://gateoverflow.in/1822

Station A needs to send a message consisting of 9 packets to Station B using a sliding window (window size 3) and go-back-n error control strategy. All packets are ready and immediately available for transmission. If every 5^{th} packet that A transmits gets lost (but no acks from B ever get lost), then what is the number of packets that A will transmit for sending the message to B?

A. 12
B. 14
C. 16
D. 18

gate2006 computer-networks sliding-window normal

Answer

2.38.8 Sliding Window: GATE2006-IT-64 top

http://gateoverflow.in/3608

Suppose that it takes 1 unit of time to transmit a packet (of fixed size) on a communication link. The link layer uses a window flow control protocol with a window size of N packets. Each packet causes an ack or a nak to be generated by the receiver, and ack/nak transmission times are negligible. Further, the round trip time on the link is equal to N units. Consider time i > N. If only acks have been received till time i(no naks), then the goodput evaluated at the transmitter at time i(in packets per unit time) is

A. 1 - N/i
B. i/(N + i)
C. 1
D. 1 - $e^{(i/N)}$

gate2006-it computer-networks sliding-window normal

Answer

2.38.9 Sliding Window: GATE2007-69 top

http://gateoverflow.in/1267

The distance between two stations M and N is L kilometers. All frames are K bits long. The propagation delay per kilometer is t seconds. Let R bits/second be the channel capacity. Assuming that the processing delay is negligible, the minimum number of bits for the sequence number field in a frame for maximum utilization, when the $\text{sliding window protocol}$ is used, is:

A. $\lceil \log_2 \frac{2LtR+2K}{K} \rceil$

B. $\lceil \log_2 \frac{2LtR}{K} \rceil$

C. $\lceil \log_2 \frac{2LtR+K}{K} \rceil$

D. $\lceil \log_2 \frac{2LtR+2K}{2K} \rceil$

gate2007 computer-networks sliding-window normal

Answer

2.38.10 Sliding Window: GATE2008-IT-64 top http://gateoverflow.in/3375

A 1Mbps satellite link connects two ground stations. The altitude of the satellite is 36,504 km and speed of the signal is 3×10^8 m/s. What should be the packet size for a channel utilization of 25% for a satellite link using go-back-127 sliding window protocol? Assume that the acknowledgment packets are negligible in size and that there are no errors during communication.

A. 120 bytes
B. 60 bytes
C. 240 bytes
D. 90 bytes

gate2008-it computer-networks sliding-window normal

Answer

2.38.11 Sliding Window: GATE2009-57, ISRO2016-75 top http://gateoverflow.in/1340

Frames of 1000 bits are sent over a 10^6 bps duplex link between two hosts. The propagation time is 25ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

What is the minimum number of bits (I) that will be required to represent the sequence numbers distinctly? Assume that no time gap needs to be given between transmission of two frames.

A. I=2
B. I=3
C. I=4
D. I=5

gate2009 computer-networks sliding-window normal isro2016

Answer

2.38.12 Sliding Window: GATE2009-58 top http://gateoverflow.in/43470

Frames of 1000 bits are sent over a 10^6 bps duplex link between two hosts. The propagation time is 25ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

Let I be the minimum number of bits (I) that will be required to represent the sequence numbers distinctly assuming that no time gap needs to be given between transmission of two frames.

Suppose that the sliding window protocol is used with the sender window size of 2^l, where I is the numbers of bits as mentioned earlier and acknowledgements are always piggy backed. After sending 2^I frames, what is the minimum time the sender will have to wait before starting transmission of the next frame? (Identify the closest choice ignoring the frame processing time.)

A. 16ms
B. 18ms
C. 20ms
D. 22ms

gate2009 computer-networks sliding-window normal

Answer

2.38.13 Sliding Window: GATE2014-1-28 top http://gateoverflow.in/1795

Consider a selective repeat sliding window protocol that uses a frame size of 1 KB to send data on a 1.5 Mbps link with a one-way latency of 50 msec. To achieve a link utilization of 60%, the minimum number of bits required to represent the sequence number field is ________.

gate2014-1 computer-networks sliding-window numerical-answers normal

Answer

2.38.14 Sliding Window: GATE2015-3_28 top http://gateoverflow.in/8481

Consider a network connecting two systems located 8000 kilometers apart. The bandwidth of the network is 500×10^6 bits per second. The propagation speed of the media is 4×10^6 meters per second. It is need to design a Go-Back-N sliding window protocol for this network. The average packet size is 10^7 bits. The network is to be used to its full capacity. Assume that processing delays at nodes are negligible. Then, the minimum size in bits of the sequence number field has to be ______.

gate2015-3 computer-networks sliding-window normal numerical-answers

Answer

2.38.15 Sliding Window: ISI2015-CS-4b top http://gateoverflow.in/47326

Stations A and B are connected through a line of bandwidth 64 $kbps$. Station A uses 16 byte packets to transmit messages to B using a sliding window protocol. The round trip propagation delay between A and B is 50 milliseconds. Determine the window size A should use to maximize the line utilization. Assume that the ack frame is of negligible size and processing delay may be ignored. Justify your answer.

descriptive isi2015 computer-networks sliding-window

Answer

Answers: Sliding Window

2.38.1 Sliding Window: GATE2003-84 top http://gateoverflow.in/967

Selected Answer

We need the maximum throughput, and for that we need to send as much data as possible to fully utilize the bandwidth.

so, maximum packets that can be sent = 1 + 2a = 9(after calculation) for 100% efficiency.

But we have a window size of 5 only, so we can send only 5 packets at max.

Efficiency = 5/9

Now, A/Q, Bandwidth of the channel (BW) = L/Tt = 1000 / (50*10^-6) = 20*10^6 bytes/sec.

So, max. throughput achievable = Efficiency * BW = 5/9 * 20*10^6 = 11.11 * 10^6 bytes/sec. (B)

34 votes -- Ravi Ranjan (2.9k points)

I think options are given in bytes per sec instead of bits per sec.

Transmission time =50 micro sec
Propagation time =200 micro sec
RTT= 50+2*200=450 microsec (Receiver can send an ACK as soon as the first packet is received)

total number of bits transmitted before first ACK is received = 1000x5x8 bits =40000 bits

After first ACK is received, same cycle of action repeats. So,

Throughput = (40000/450) x10^6 bits = 88.88x10^6 bits ps=11.11x10^6 bytes per sec

31 votes -- Parul Agarwal (793 points)

2.38.2 Sliding Window: GATE2004-IT-81 top http://gateoverflow.in/3725

Selected Answer

C) M+N

Because Ws+Wr ≤ Sequence numbers (as the maximum number of unacknowledged packets at sender will be Ws and at the receiver it will be Wr, similar to the sequence numbering in Selective Repeat)

where Ws is size of sender window and Wr is receiver window's size.

17 votes -- Parul Agarwal (793 points)

2.38.3 Sliding Window: GATE2004-IT-83 top

http://gateoverflow.in/3727

Selected Answer

Answer: B
Transmission TIme = 100*8 bits/20 Kbps = 40 ms
Propagation Time = 400 ms
Efficiency = Window Size*Transmission Time/(Transmission Time + 2*Propagation Time) = 10*40/(40+2*400) = .476
Maximum Data Rate = .476*20 Kbps = 9.52 Kbps which is close to option B.

21 votes -- Rajarshi Sarkar (35k points)

2.38.4 Sliding Window: GATE2004-IT-88 top

http://gateoverflow.in/3732

Selected Answer

In slow-start phase, for each ACK, the sender increases the current transmit window by Maximum Segment Size (MSS). In the question it is given a packet consists of 2000 bytes and that can be taken as MSS. So, after two ACKs, current transmit window
= 4000 + 2000 + 2000
= 8000

http://www.ece.virginia.edu/~mv/edu/ee136/Lectures/congestion-control/tcp-congestion-control.pdf

21 votes -- Arjun Suresh (294k points)

2.38.5 Sliding Window: GATE2005-25 top

http://gateoverflow.in/1361

Selected Answer

ans b)

In selective reject protocol, the maximum window size must be half the sequence number space = $2^n/2 = 2^{n-1}$.

For Go-back n, the maximum window size can be 2^n-1.

http://webmuseum.mi.fh-offenburg.de/index.php?view=exh&src=73

17 votes -- Aditi Dan (5.3k points)

2.38.6 Sliding Window: GATE2006-44 top

http://gateoverflow.in/1820

Selected Answer

Round trip delay = 80 ms.

Quoting from Wikipedia

> the **round-trip delay** time (RTD) or **round-trip** time (RTT) is the length of time it takes for a signal to be sent plus the length of time it takes for an acknowledgment of that signal to be received.

Now, in many books including standard ones, they have used RTT to mean just the 2-waypropagation delay by considering the signal/packet as of the smallest possible quantity so that its transmission time is negligible. The given question is following the first definition as given by Wikipedia which is clear from the choice.

During this time the first ACK arrives and so sender can continue sending frames. So, for maximum utilization sender should have used the full bandwidth during this time. i.e., it should have sent 128 kbps * 80 ms amount of data and a packet being of size 32 byte we get no. of packets

$$= \frac{128 \times 80}{32 \times 8} = 40.$$

15 votes -- Arjun Suresh (294k points)

Answer: B

Round Trip Time = 80ms
Frame size = 32
$\times 8$ bits
Bandwidth = 128kbps
Transmission Time =
$\frac{32 \times 8}{128} ms = 2ms$
Let
n be the window size.
Utilization =
$\frac{n}{1+2a}$
where
$a = \frac{\text{Propagation Time}}{\text{Transmission Time}} = \frac{n}{1+\frac{2\times 40}{2}}$
For maximum utilization:
$n = 41$ which is **close to option (B)**.

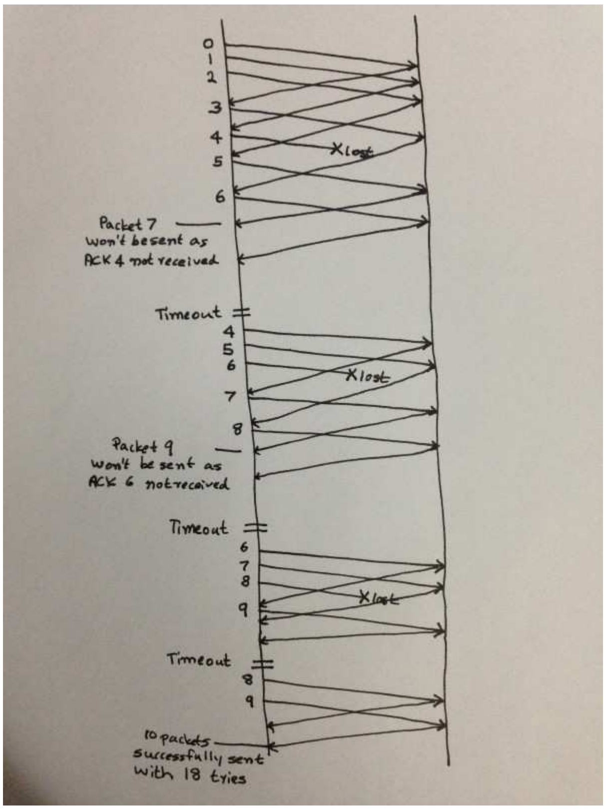
23 votes -- Rajarshi Sarkar (35k points)

2.38.7 Sliding Window: GATE2006-46 top

http://gateoverflow.in/1822

Selected Answer

Since all packets are ready initially itself, we can assume a timeout is detected after all possible packets are sent. So, the sending happens as shown in figure (I draw the figure assuming 10 packets. For 9 packets answer will be 16).



29 votes -- Arjun Suresh (294k points)

2.38.8 Sliding Window: GATE2006-IT-64 top

http://gateoverflow.in/3608

Selected Answer

In computer networks, **goodput** is the application level throughput, i.e. the number of useful information bits delivered by the network to a certain destination per unit of time. (From wikipedia).

So, successful delivery of packet can be assured if ACK has been received for it.

So till time 'i' we would have transmitted 'i' packets but only (i-N) can be acknowledged as minimum time for a packet to get Acknowledged is N (since RTT is N which is equal to the window size, there is no waiting time for the sender).

So successfully delivered packets = (i-N)

Time for transmission = i

Goodput = Successfully delivered data/ Time = (i-N)/i = 1- N/i

Therefore (A)

26 votes -- Sandeep_Uniyal (7.3k points)

2.38.9 Sliding Window: GATE2007-69 top

http://gateoverflow.in/1267

Selected Answer

Answer: C

We can send $\frac{\text{RTT}}{\text{Transmission Time}}$ number of packets for maximum utilisation of the channel, as in this time we get the first ACK back and till that time, we can continue sending packets.

So, $\frac{\text{Transmission Time} + 2^*\text{Propagation Time}}{\text{Transmission Time}}$ number of packets should be sent.

Therefore, bits required for the sequence number field:

$$\left\lceil \log_2\left(\frac{\frac{K}{R}+2Lt}{\frac{K}{R}}\right)\right\rceil = \left\lceil \log_2\left(\frac{K+2LtR}{K}\right)\right\rceil$$

Edit : here it is asked for general sliding window protocol not GBN nor SR .

In general sliding window protocol:

Sequence number bit = log(sender window size)

18 votes -- Rajarshi Sarkar (35k points)

for maximum utilization $\eta = 1$,

$$\eta = SWS \times \frac{\text{Transmission Time}}{\text{Transmission Time} + 2{*}\text{Propagation Time}}$$

$$1 = SWS \times \frac{\text{Transmission Time}}{\text{Transmission Time} + 2{*}\text{Propagation Time}}$$

so,

$$\frac{\text{Transmission Time} + 2{*}\text{Propagation Time}}{\text{Transmission Time}} = SWS$$

gives the number of packets that are sent. It means that it is the Sender's Window Size.

But we also know that

$$\substack{\text{sequence numbers}\\ \text{available}} \geq \text{SWS} + \text{RWS}$$

so, to get the minimum number of bits needed to represent the sequence numbers we should consider what protocols are in use.

if GBN ARQ:

$$\begin{aligned}\substack{\#\text{ bits required to rep.}\\ \text{sequence numbers}} &= \lceil \log_2(SWS + RWS)\rceil \\ &= \left\lceil \log_2\left(\frac{K/R+2Lt}{K/R}+1\right)\right\rceil \\ &= \left\lceil \log_2\left(\frac{2K+2LtR}{K}\right)\right\rceil\end{aligned}$$

if Selective Repeat ARQ :

$$\begin{aligned}\substack{\#\text{ bits required to rep.}\\ \text{sequence numbers}} &= \lceil \log_2(2 \times SWS)\rceil \\ &= \left\lceil \log_2\left(2 \times \frac{K/R+2Lt}{K/R}\right)\right\rceil \\ &= \left\lceil \log_2\left(\frac{2K+4LtR}{K}\right)\right\rceil\end{aligned}$$

37 votes -- Amar Vashishth (28.7k points)

2.38.10 Sliding Window: GATE2008-IT-64 top

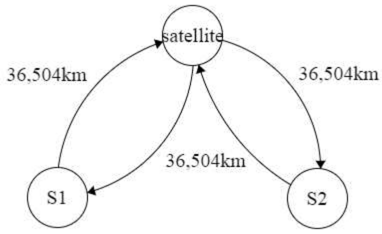
http://gateoverflow.in/3375

Selected Answer

Distance from Station A to Satellite $= 36504 \times 10^3$ m

Time to reach satellite $= \frac{36504000}{300000000} = 0.12168s$

RTT for a bit $= 4 \times$ Time to reach satellite$(S1 \rightarrow Satellite, Satellite \rightarrow S2, S2 \rightarrow Satellite, Satellite \rightarrow S1)$



Efficiency is the ratio of the amount of data sent to the maximum amount of data that could be sent. Let X be the packet size.

In Go-Back-N, within RTT we can sent n packets. So, useful data is $n \times X$, where X is the packet size. Now, before we can sent another packet ACK must reach back. Time for this is transmission time for a packet (other packets are pipelined and we care only for first ACK), and RTT for a bit (propagation times for the packet + propagation time for ACK + transmission time for ACK - neglected as per question)

$$\text{Efficiency} = \frac{\text{Transmitted Data Size}}{PacketSize + RTT_{bit} \times \text{Bandwidth}}$$

$$0.25 = \frac{127 \times X}{X + 4 \times 0.12168 \times B}$$

$$0.25X + 0.25 \times 4 \times 0.12168 \times B = 127X$$

$$0.25 \times X + 0.12168 \times 10^6 = 127X$$

$$121680 = 126.75X$$

$$X = 9.6 \times 10^{-4} \times 10^6 = 960$$

Packet Size = 960 bits = 120 Bytes

so option (A)

36 votes -- Danish (3.6k points)

2.38.11 Sliding Window: GATE2009-57, ISRO2016-75 top http://gateoverflow.in/1340

Selected Answer

Bandwidth won't be halved in full duplex. http://superuser.com/questions/335979/does-1-gbit-s-port-in-full-duplex-mean-1-gbit-s-send-and-1-gbit-s-receive

Propagation time is given as 25 ms.

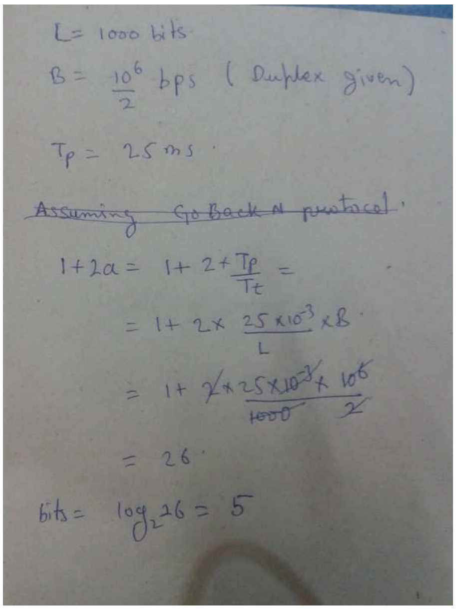
Bandwidth = 10^6 bps.

So, to fully utilize the channel, we must send 10^6 bits into the channel in a second, which will be 1000 frames per second as each frame is 1000 bits. Now, since the propagation time is 25 ms, to fully pack the link we need to send at least 1000 * 25 * 10^{-3} = 25 frames. So, we need $\lceil \log_2 25 \rceil$ = 5 bits.

45 votes -- Arjun Suresh (294k points)

When the link is duplex do we have to take Bandwidth = B/2 ?

My solution:



$L = 1000$ bits

$B = \frac{10^6}{2}$ bps (Duplex given)

$T_p = 25$ ms

~~Assuming Go Back N protocol~~

$1 + 2a = 1 + 2 * \frac{T_p}{T_t} =$

$= 1 + 2 \times \frac{25 \times 10^{-3}}{L} \times B$

$= 1 + \cancel{2} \times \frac{25 \times 10^{-3}}{\cancel{1000}} \times \frac{10^6}{\cancel{2}}$

$= 26$

bits $= \log_2 26 = 5$

11 votes -- Vikrant Singh (13.4k points)

2.38.12 Sliding Window: GATE2009-58 top

http://gateoverflow.in/43470

Selected Answer

Bandwidth won't be halved in full duplex. http://superuser.com/questions/335979/does-1-gbit-s-port-in-full-duplex-mean-1-gbit-s-send-and-1-gbit-s-receive

Propagation time is given as 25 ms.

Bandwidth = 10^6 bps.

So, to fully utilize the channel, we must send 10^6 bits into the channel in a second, which will be 1000 frames per second as each frame is 1000 bits. Now, since the propagation time is 25 ms, to fully pack the link we need to send at least 1000 * 25 * 10^{-3} = 25 frames. So, we need $\lceil \log_2 25 \rceil$ = 5 bits.

I = 5, so 2^I = 32 frames are sent.

Now, we need to get RTT (which is the time between which a frame is sent and its ACK is received), to determine the waiting time.

Transmission time (for a frame of size 1000 bits) = $1000/10^6$ = 1 ms.
So, transmission time for 32 frames = 32 ms.

RTT = Propagation time for frame + Transmission time for frame + Propagation time for ACK + Transmission time for ACK

= 25 ms + 1 ms + 25 ms + 1 ms (ACK is piggy backed and assuming frame size for piggy backing is also 1000 bits)
= 52 ms

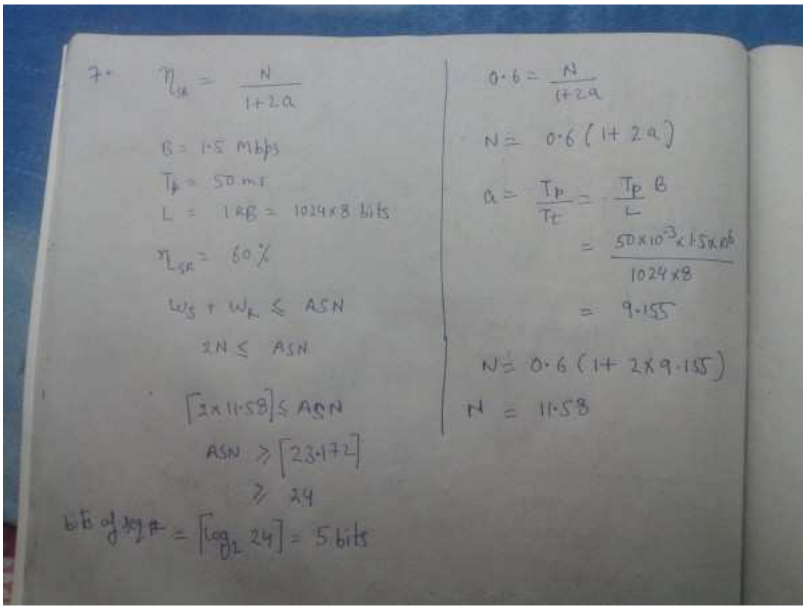
So, waiting time = 52 - 32 = 20 ms. (For the 32 ms, the sender was transmitting and not waiting)

31 votes -- Arjun Suresh (294k points)

2.38.13 Sliding Window: GATE2014-1-28 top

http://gateoverflow.in/1795

Selected Answer



Is it the correct solution for this problem?

41 votes -- Vikrant Singh (13.4k points)

A frame is 1 KB and takes 8 * $10^3/1.5*10^6$ s = 5.33 ms to reach the destination. (8 is used to convert byte to bits)

Adding the propagation delay of 50 ms, the total time will be 50 + 5.33 = 55.33 ms

Now, we need the ACK to reach back also, so the time between a packet is sent and an ACK is received = 55.33 + 50 (transmission time of ACK neglected)= 105.33 ms

The channel band width is 1.5 Mbps, so in 1 ms, 1.5 K bits can be transferred and so in 105.33 ms, 157.995 K bits can be transferred.

To, ensure 60% utilization, amount of bits to be transferred in 1 ms = 157.995 * 0.6 = 94.797 Kb = 94.797/(8 * 1000) frames = 11.849 frames ≈ 12 frames. (we bounded up to ensure at least 60% utilization)

So, we need a minimum window size of 12.

Now, in selective repeat protocol, the window size must be less than half the sequence number space. (http://stackoverflow.com/questions/3999065/why-is-window-size-less-than-or-equal-to-half-the-sequence-number-in-sr-protocol)

So, this means sequence number space must be larger than 2 * 12 = 24. To have a sequence number space of 24, sequence bits must be at least $\log_2 24$ = 5

16 votes -- Arjun Suresh (294k points)

2.38.14 Sliding Window: GATE2015-3_28 top

http://gateoverflow.in/8481

Selected Answer

Answer = 8 bits

In order to achieve full utilization, sender has to keep on sending frames till the acknowledgement arrives for the first frame.

Time taken for acknowledgement to arrive is 2 times propagation delay + transmission time for a frame.

One way propagation time = 8000x10^3 / (4x10^6)

= 2 secs

Time taken to transmit one frame = 10^7/(500x10^6)

=0.02 secs

So, RTT = 2 * 2 = 4

No of frames that can be transmitted in 4 secs = 4/0.02

=200

Hence minimum number of bits required for sequence numbers till 200 is 8 (as 2^8 = 256)

19 votes -- overtomanu (1.2k points)

Isn't the minimum sequence number >= SWS+RWS. So we are getting 201 for the sender window and since we are using GBN we should add 1 as the RWS. So total sequence number >= 201+1 =202. Answer will still remain 8 though

10 votes -- Shivam Gairola (115 points)

2.38.15 Sliding Window: ISI2015-CS-4b top

http://gateoverflow.in/47326

Bandwidth between Stations A and B = 64 kbps = 64000 bps

Size of data packet = 16 Byte = 128 bits

So, Transmission time (T_t)= $\frac{Size of data packet}{Bandwidth} = \frac{128}{64000} = .002sec$

Round trip Propagation delay ($2*T_p$)= 50 milisec= .05 sec

For maximum Utilization in sliding window protocol window size of sender= $1+2*\frac{Tp}{Tt}$

= $1+\frac{.05}{.002} = 26$

Hence,Window size of sender should be 26.

3 votes -- Leen Sharma (32.3k points)

2.39 Sockets(4) top

2.39.1 Sockets: GATE2008-17 top

http://gateoverflow.in/415

Which of the following system calls results in the sending of SYN packets?

A. socket
B. bind
C. listen
D. connect

gate2008 normal computer-networks sockets

Answer

2.39.2 Sockets: GATE2008-59 top

http://gateoverflow.in/482

A client process P needs to make a TCP connection to a server process S. Consider the following situation: the server process S executes a $\text{socket}()$, a $\text{bind}()$ and a $\text{listen}()$ system call in that order, following which it is preempted. Subsequently, the client process P executes a $\text{socket}()$ system call followed by $\text{connect}()$ system call to connect to the server process S. The server process has not executed any $\text{accept}()$ system call. Which one of the following events could take place?

A. $\text{connect}()$ system call returns successfully

B. $\text{connect}()$ system call blocks

C. $\text{connect}()$ system call returns an error

D. $\text{connect}()$ system call results in a core dump

gate2008 computer-networks sockets normal

Answer

2.39.3 Sockets: GATE2014-2-24 top http://gateoverflow.in/1982

Which of the following socket API functions converts an unconnected active TCP socket into a passive socket?

A. connect
B. bind
C. listen
D. accept

gate2014-2 computer-networks sockets easy

Answer

2.39.4 Sockets: GATE2015-2_20 top http://gateoverflow.in/8108

Identify the correct order in which a server process must invoke the function calls accept, bind, listen, and recv according to UNIX socket API.

A. listen, accept, bind, recv
B. bind, listen, accept, recv
C. bind, accept, listen, recv
D. accept, listen, bind, recv

gate2015-2 computer-networks sockets easy

Answer

Answers: Sockets

2.39.1 Sockets: GATE2008-17 top http://gateoverflow.in/415

Selected Answer

answer (D)

socket() creates a new socket of a certain socket type, identified by an integer number, and allocates system resources to it.

bind() is typically used on the server side, and associates a socket with a socket address structure, i.e. a specified local port number and IP address.

listen() is used on the server side, and causes a bound TCP socket to enter listening state.

connect() is used on the client side, and assigns a free local port number to a socket. In case of a TCP socket, it causes an attempt to establish a new TCP connection.

When **connect()** is called by client, following three way handshake happens to establish the connection in TCP.

1) The client requests a connection by sending a SYN (synchronize) message to the server.

2) The server acknowledges this request by sending SYN-ACK back to the client.

3) The client responds with an ACK, and the connection is established.

20 votes -- sonam vyas (13.2k points)

2.39.2 Sockets: GATE2008-59 top

http://gateoverflow.in/482

Selected Answer

First thing to note: All the sockets are by default in BLOCKING mode. What do we mean by blocking ??

Blocking mode means that when we make a system call, it blocks the caller for the time "when call() is made till the job is done OR an error returns ". We can set each socket to Non-blocking explicitly. Setting to Non-Blocking means we are telling the kernel that "If the system call cant be completed without putting process to sleep then DON'T put the process to sleep . Instead return with an ERROR immediately and continue the process" which can be checked for the completion by the caller in between the execution of other tasks.

Now coming to this question:

Suppose connect() is in default blocking mode then calling connect() sends SYN packet to the server. Since server has not executed any accept() call it can not acknowledge the SYN packet. Connect() in blocking mode keep sending SYN packets at fixed intervals(first after 6 sec, second after 24 sec typically until 75 sec latest). This is done until an error ETIMEDOUT is returned by the TCP.(in this case,else there are several other type of errors returned in case No port exists for that connection or server id not listening etc.)

here option (B) saying that connect() blocks is not entirely wrong but since we know that accept() call is not made by server, connect() WILL NOT WAIT FOREVER and SO IT CAN NOT BLOCK. It will **ultimately return** with an ERROR message.

So option (c) is CORRECT.

Core dump thing I don't know about !!

But once connect() returns error that socket can not be reused and must be CLOSED.

And a non-blocking connect() is never blocked and immediately returns with an error if connection is not successful although IT CONTINUES WITH TRYING TO CONNECT .Error here just means that it returns a message saying "I could not connect immediately BUT i am trying AND you can check it in between.

Hope it clears a bit.

35 votes -- Sandeep_Uniyal (7.3k points)

2.39.3 Sockets: GATE2014-2-24 top

http://gateoverflow.in/1982

Selected Answer

C is ans listen converts unconnected socket into passive coonect i.e it is waiting for request from client

15 votes -- Pooja Palod (32.4k points)

2.39.4 Sockets: GATE2015-2_20 top

http://gateoverflow.in/8108

Selected Answer

Answer: B

Bind: Binds the socket to an address

Listen: Waits for connections to the socket

Accept: Accepts a connection to the socket

Recv: Receives data from connection

From Man page of accept:

It extracts the first connection request on the queue of pending connections for the listening socket, creates a new connected socket, and returns a new file descriptor referring to that socket. The newly created socket is not in the listing state. The original socket is unaffected by this call

15 votes -- Rajarshi Sarkar (35k points)

2.40 Stop And Wait(4) top

2.40.1 Stop And Wait: GATE 2016-1-55 top

http://gateoverflow.in/39696

A sender uses the Stop-and-Wait ARQ protocol for reliable transmission of frames. Frames are of size 1000 bytes and the transmission rate at the sender is 80 Kbps (1 Kbps = 1000 bits/second). Size of an acknowledgement is 100 bytes and the transmission rate at the receiver is 8 Kbps. The one-way propagation delay is 100 milliseconds.

Assuming no frame is lost, the sender throughout is _________ bytes/ second.

gate2016-1 computer-networks stop-and-wait normal numerical-answers

Answer

2.40.2 Stop And Wait: GATE2006-IT-68 top

http://gateoverflow.in/3612

On a wireless link, the probability of packet error is 0.2. A stop-and-wait protocol is used to transfer data across the link. The channel condition is assumed to be independent from transmission to transmission. What is the average number of transmission attempts required to transfer 100 packets?

A. 100
B. 125
C. 150
D. 200

gate2006-it computer-networks sliding-window stop-and-wait normal

Answer

2.40.3 Stop And Wait: GATE2015-1_53 top

http://gateoverflow.in/8363

Suppose that the stop-and-wait protocol is used on a link with a bit rate of 64 kilobits per second and 20 milliseconds propagation delay. Assume that the transmission time for the acknowledgement and the processing time at nodes are negligible. Then the minimum frame size in bytes to achieve a link utilization of at least 50% is__________________.

gate2015-1 computer-networks stop-and-wait normal numerical-answers

Answer

2.40.4 Stop And Wait: GATE2017-1-45 top

http://gateoverflow.in/118328

The values of parameters for the Stop-and-Wait ARQ protocol are as given below:

Bit rate of the transmission channel = 1 Mbps.
Propagation delay from sender to receiver = 0.75 ms.
Time to process a frame = 0.25 ms.
Number of bytes in the information frame = 1980.
Number of bytes in the acknowledge frame = 20.
Number of overhead bytes in the information frame = 20.

Assume there are no transmission errors. Then, the transmission efficiency (expressed in percentage) of the Stop-and-Wait ARQ protocol for the above parameters is ______________ (correct to 2 decimal places).

gate2017-1 computer-networks stop-and-wait numerical-answers normal

Answer

Answers: Stop And Wait

2.40.1 Stop And Wait: GATE 2016-1-55 top

http://gateoverflow.in/39696

Selected Answer

Answer is 2500 bytes per second.

Throughput is number of bytes we are able to send per second.

Calculate the transmission time of sender Tt_Send , calculate one way propogation delay Tp , Calculate the transmission time of receiver Tt_Recv . We get Tt_Send here as 1/10 seconds , Tp as 1/10 seconds(given in qstn as 100 ms) , Tt_Recv as 1/10 seconds.

So , total time taken to send a frame from sender to destination = Tt_Send + 2*Tp + Tt_Recv

=4/10 seconds

So, we can send 1000 bytes (frame size) in 4/10 seconds. So in 1 second, we can send 2500 bytes. So throughput is 2500 bytes per second.

26 votes -- Sreyas S (1.7k points)

Answer is 2500.

Sender transmission time = 1000*8/(80*1000) = 0.1 sec = 100 ms

Receiver transmission time = 100*8/(8*1000) = 0.1 sec = 100ms RTT= 2*100 = 200 ms

So, total time = 400 ms

In 400 ms, we send only 1000 bytes so,

Throughput = 1000/(400*10^-3) = 2500 bytes / sec

13 votes -- Deepak Sharma (691 points)

2.40.2 Stop And Wait: GATE2006-IT-68 top

http://gateoverflow.in/3612

Selected Answer

total number of retransmissions for one frame in general is 1/(1-p) where p is the probablity of error
so here it would be
for one frame 1/(1-0.2)
so for 100 frames 100/(0.8)=125

12 votes -- Shreyans Dhankhar (2.6k points)

2.40.3 Stop And Wait: GATE2015-1_53 top

http://gateoverflow.in/8363

Selected Answer

Link Utilization = Amount of data sent/Max. amount of data that could be sent.

Let x be the frame size in bits.

In stop-and-wait protocol, once a frame is sent, next frame won't be sent until ACK is received. Time for this,
RTT = Propagation delay for frame + Transmission time for frame + Propagation delay for ACK + Transmission time for ACK
= 20 ms + x /64 ms + 20 ms + 0(as given in question)
= (40 + x/64) ms.

Amount of data sent during RTT = x

Max. amount of data that could be sent = (40 + x/64) * 64 = 2560 + x bits.

So, link utilization, 0.5 = x/(2560 + x)

x = 2560 bits = 320 bytes.

alternative approach ,
link utilization or efficiency of stop and wait protocol is ,

efficiency = Tx / (Tx + 2Tp) = 1 / (1 + 2(Tp / Tx)) = 1 / (1 +2a) ,

where , Transmission time = Tx = packet size / bandwidth = L / B

Propagation time = Tp = distance / speed = d / v ,
and , a = Propagation time / Transmission time = (Tp / Tx) ,
now for 50% efficiency ,
efficiency = 1 / (1 +2a)
50% = 1 / (1 +2a)

1 / 2 = 1 / (1 +2a) ,
2 = (1 +2a)
2 - 1 = 2a
1 = 2.(Tp / Tx)
Tx = 2.Tp
L / B = 2* 20 ms
L = 2 * 20 ms * B = 2* 20 * 10^{-3} * 64 k bits = 2* 20*10^{-3} * 64 10^3 bits
L = 40 * 64 bits = 40 * 64/8 bytes = 40* 8 bytes = 320 bytes (answer)

30 votes -- Arjun Suresh (294k points)

2.40.4 Stop And Wait: GATE2017-1-45 top

http://gateoverflow.in/118328

Selected Answer

Efficieny is usually calculated as $\frac{InfoFrameTransmitTime}{TotalTime}$

Efficiency = $\frac{InfoFrameTransmitTime}{InfoFrameTransmitTime+InfoFrameProcessTime+2*PropDelay+AckFrameTransmitTime+AckFrameProcessTime}$

Reference to calculate efficiency formula - http://nptel.ac.in/courses/106106091/pdf/Lecture13_StopAndWaitAnalysis.pdf

http://spinlab.wpi.edu/courses/ece230x/lec14-15.pdf

From the question it is not very clear wether frame processing time is mentioned about InfoFrame or AckFrame or Combined. It is also explicitly not mentioned wether to consider FrameProcessing time for ACK or not. Thus, following are the different inferences that could be made from the question -

1. As Size of InfoFrame (1980-2000 Bytes) is very large as compared to AckFrame (20 Bytes) one could assume the given processing time is for InfoFrame and processing time for AckFrame is neglible. The processing time does depend on size of frame for various parameters one of them is checksum calculation. Check the below reference for more details - http://rp-www.cs.usyd.edu.au/~suparerk/Research/Doc/Stop-and-Wait_Simulation.pdf
2. It is also mentioned in the question that there are no trasmission errors. One can also think as an hint that since frames are successfully transmitted there is no need for ACK processing at sender Side
3. Considering frame processing time given is combined both ACK+Info Frame
4. Considering frame processing time indvidually and which is the Ans in Official key (**86.5 - 87.5**)

The below answers could be due to case 1,2,3 -

No of Bytes in the Information frame = 1980 Bytes (Not very clear from question wether it implies total bytes or data bytes)

No of OverHead Bytes = 20 Bytes

Assuming they have explicity mentioned Overhead bytes -

Total Frame Size = No of Bytes in the Information frame + No of OverHead Bytes

= 2000 B

InfoTransmission Time = $\frac{InfoFrameSize}{Bandwidth}$

= $\frac{2000*8*10^3}{1*10^6}$

= 16 ms

AckTransmissionTime = $\frac{20*10^3}{1*10^6}$

= 0.16 ms

Efficiency = $\frac{16}{16+2*0.75+0.25+0.16}$

=**89.34 %** (After round-off)

Assuming bytes in information includes Overhead bytes -

InfoFrameTranmission Time = 15.84

Efficiency = 89.23 %

Range could be 87.5 - 89.34

Reference to the similar questions -

http://gateoverflow.in/43981/isro-2013-41

http://gateoverflow.in/39696/gate-2016-1-55

More Efficiency Concept Reference -

http://nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Computer%20networks/pdf/M3L3.pdf

11 votes -- yg92 (2.3k points)

2.41 Subnetting(14) top

2.41.1 Subnetting: GATE2003-82, ISRO2009-1 top http://gateoverflow.in/965

The subnet mask for a particular network is 255.255.31.0. Which of the following pairs of IP addresses could belong to this network?

A. 172.57.88.62 and 172.56.87.23

B. 10.35.28.2 and 10.35.29.4

C. 191.203.31.87 and 191.234.31.88

D. 128.8.129.43 and 128.8.161.55

gate2003 computer-networks subnetting normal isro2009

Answer

2.41.2 Subnetting: GATE2004-55 top http://gateoverflow.in/1051

The routing table of a router is shown below:

Destination	Subnet Mask	Interface
128.75.43.0	255.255.255.0	Eth0
128.75.43.0	255.255.255.128	Eth1
192.12.17.5	255.255.255.255	Eth3
Default		Eth2

On which interface will the router forward packets addressed to destinations 128.75.43.16 and 192.12.17.10 respectively?

A. Eth1 and Eth2
B. Eth0 and Eth2

C. Eth0 and Eth3
D. Eth1 and Eth3

gate2004 computer-networks subnetting normal

Answer

2.41.3 Subnetting: GATE2004-IT-26 top http://gateoverflow.in/3667

A subnet has been assigned a subnet mask of 255.255.255.192. What is the maximum number of hosts that can belong to this subnet?

A. 14
B. 30
C. 62
D. 126

gate2004-it computer-networks subnetting normal

Answer

2.41.4 Subnetting: GATE2005-27 top http://gateoverflow.in/1363

An organization has a class B network and wishes to form subnets for 64 departments. The subnet mask would be:

A. 255.255.0.0

B. 255.255.64.0

C. 255.255.128.0

D. 255.255.252.0

gate2005 computer-networks subnetting normal

Answer

2.41.5 Subnetting: GATE2005-IT-76 top http://gateoverflow.in/3839

A company has a class C network address of 204.204.204.0. It wishes to have three subnets, one with 100 hosts and two with 50 hosts each. Which one of the following options represents a feasible set of subnet address/subnet mask pairs?

A. 204.204.204.128/255.255.255.192
204.204.204.0/255.255.255.128
204.204.204.64/255.255.255.128
B. 204.204.204.0/255.255.255.192
204.204.204.192/255.255.255.128
204.204.204.64/255.255.255.128
C. 204.204.204.128/255.255.255.128
204.204.204.192/255.255.255.192
204.204.204.224/255.255.255.192
D. 204.204.204.128/255.255.255.128
204.204.204.64/255.255.255.192
204.204.204.0/255.255.255.192

gate2005-it computer-networks subnetting normal

Answer

2.41.6 Subnetting: GATE2006-45 top http://gateoverflow.in/1821

Two computers C1 and C2 are configured as follows. C1 has IP address 203.197.2.53 and netmask 255.255.128.0. C2 has IP address 203.197.75.201 and netmask 255.255.192.0. Which one of the following statements is true?

A. C1 and C2 both assume they are on the same network
B. C2 assumes C1 is on same network, but C1 assumes C2 is on a different network
C. C1 assumes C2 is on same network, but C2 assumes C1 is on a different network
D. C1 and C2 both assume they are on different networks.

gate2006 computer-networks subnetting normal

Answer

2.41.7 Subnetting: GATE2006-IT-70 top

http://gateoverflow.in/3614

A subnetted Class B network has the following broadcase address : 144.16.95.255. Its subnet mask

A. is necessarily 255.255.224.0
B. is necessarily 255.255.240.0
C. is necessarily 255.255.248.0
D. could be any one of 255.255.224.0, 255.255.240.0, 255.255.248.0

gate2006-it computer-networks subnetting normal

Answer

2.41.8 Subnetting: GATE2007-67, ISRO2016-72 top

http://gateoverflow.in/1265

The address of a class B host is to be split into subnets with a 6-bit subnet number. What is the maximum number of subnets and the maximum number of hosts in each subnet?

A. 62 subnets and 262142 hosts.

B. 64 subnets and 262142 hosts.

C. 62 subnets and 1022 hosts.

D. 64 subnets and 1024 hosts.

gate2007 computer-networks subnetting easy isro2016

Answer

2.41.9 Subnetting: GATE2008-57 top

http://gateoverflow.in/480

If a class B network on the Internet has a subnet mask of 255.255.248.0, what is the maximum number of hosts per subnet?

A. 1022
B. 1023
C. 2046
D. 2047

gate2008 computer-networks subnetting easy

Answer

2.41.10 Subnetting: GATE2008-IT-85 top

http://gateoverflow.in/3409

Host X has IP address 192.168.1.97 and is connected through two routers R1 and R2 to another host Y with IP address 192.168.1.80. Router R1 has IP addresses 192.168.1.135 and 192.168.1.110. R2 has IP addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Which IP address should X configure its gateway as?

A. 192.168.1.67
B. 192.168.1.110
C. 192.168.1.135
D. 192.168.1.155

gate2008-it computer-networks subnetting normal

Answer

2.41.11 Subnetting: GATE2010-47 top

http://gateoverflow.in/2349

Suppose computers A and B have IP addresses 10.105.1.113 and 10.105.1.91 respectively and they both use same netmask N. Which of the values of N given below should not be used if A and B should belong to the same network?

A. 255.255.255.0
B. 255.255.255.128
C. 255.255.255.192
D. 255.255.255.224

gate2010 computer-networks subnetting easy

Answer

2.41.12 Subnetting: GATE2012_34 top http://gateoverflow.in/1752

An Internet Service Provider (ISP) has the following chunk of CIDR-based IP addresses available with it: $245.248.128.0/20$. The ISP wants to give half of this chunk of addresses to Organization A, and a quarter to Organization B, while retaining the remaining with itself. Which of the following is a valid allocation of addresses to A and B?

(A) $245.248.136.0/21 \text{ and } 245.248.128.0/22$
(B) $245.248.128.0/21 \text{ and } 245.248.128.0/22$
(C) $245.248.132.0/22 \text{ and } 245.248.132.0/21$
(D) $245.248.136.0/24 \text{ and } 245.248.132.0/21$

gate2012 computer-networks subnetting normal

Answer

2.41.13 Subnetting: GATE2015-2_41 top http://gateoverflow.in/8213

Consider the following routing table at an IP router:

Network No	Net Mask	Next Hop
128.96.170.0	255.255.254.0	Interface 0
128.96.168.0	255.255.254.0	Interface 1
128.96.166.0	255.255.254.0	R2
128.96.164.0	255.255.252.0	R3
0.0.0.0	Default	R4

For each IP address in Group I Identify the correct choice of the next hop from Group II using the entries from the routing table above.

Group I	**Group II**
i) 128.96.171.92	a) Interface 0
ii) 128.96.167.151	b) Interface 1
iii) 128.96.163.151	c) R2
iv) 128.96.164.121	d) R3
	e) R4

A. i-a, ii-c, iii-e, iv-d
B. i-a, ii-d, iii-b, iv-e
C. i-b, ii-c, iii-d, iv-e
D. i-b, ii-c, iii-e, iv-d

gate2015-2 computer-networks subnetting easy

Answer

2.41.14 Subnetting: GATE2015-3_38 top http://gateoverflow.in/8497

In the network 200.10.11.144/27, the fourth octet (in decimal) of the last IP address of the network which can be assigned to a host is ______.

gate2015-3 computer-networks subnetting normal numerical-answers

Answer

Answers: Subnetting

2.41.1 Subnetting: GATE2003-82, ISRO2009-1 top http://gateoverflow.in/965

Selected Answer

A and C are not the answers as the second byte of IP differs and subnet mast has 255 for second byte.

Consider B, (& for bitwise AND)

10.35.28.2 & 255.255.31.0 = 10.35.28.0 ($28 = 11100_2$)
10.35.29.4 & 255.255.31.0 = 10.35.29.0 ($29 = 11111_2$)
So, we get different subnet numbers

Consider D.

128.8.129.43 & 255.255.31.0 = 128.8.1.0 ($129 = 10000001_2$)
128.8.161.55 & 255.255.31.0 = 128.8.1.0 ($161 = 10100001_2$)
The subnet number matches. So, D is the answer.

38 votes -- Arjun Suresh (294k points)

2.41.2 Subnetting: GATE2004-55 top http://gateoverflow.in/1051

Selected Answer

The Answer must be **A**.

For 1st packet,

(128.75.43.16) && (255.255.255.0) = (128.75.43.0) since {16 && 0 = 0}, as well as

(128.75.43.16) && (255.255.255.128) = (128.75.43.0) since {16 && 128 = 0}.

Now, since both these subnet masks are producing the same Network ID, hence The one with greater number of ones will be selected, and the packet will be forwarded there. Hence packet 1 will be forwarded to Eth1.

For 2nd packet,

(192.12.17.10) when anded with each of the subnet masks does not match with any of the network ID, since:

(192.12.17.10) && (255.255.255.0) = (192.12.17.0) {Does not match with any of the network addresses}

(192.12.17.10) && (255.255.255.128) = (192.12.17.0) {Does not match with any of the network addresses}

(192.12.17.10) && (255.255.255.255) = (192.12.17.10) {Does not match with any of the network addresses}

Hence, Default interface must be selected for packet 2, i.e Interface Eth2.

21 votes -- saurabhrk (1.5k points)

2.41.3 Subnetting: GATE2004-IT-26 top http://gateoverflow.in/3667

Selected Answer

C is answer since you have 6 zeroes so u can make 64-2 hosts

13 votes -- Shreyans Dhankhar (2.6k points)

2.41.4 Subnetting: GATE2005-27 top http://gateoverflow.in/1363

Selected Answer

D is correct answer.

to form subnet for 64 departments we need 6 continuous bit and the value of **11111100 = 252**.

organization has class B network so subnet mask would be **255.255.252.0**

11 votes -- R.B. Tiwari (357 points)

2.41.5 Subnetting: GATE2005-IT-76 top http://gateoverflow.in/3839

Selected Answer

Answer->D

MSB in last 8 bits helps us to get two subnets

10000000--->subnet1

00000000--->subnet2

subnet2 is divided into 2 more subnets using 7th bit

00000000--->subnet2(0)

01000000--->subnet2(1)

13 votes -- nagalla pruthvi (883 points)

2.41.6 Subnetting: GATE2006-45 top http://gateoverflow.in/1821

Selected Answer

Subnetmask for C1 is 255.255.128.0. So, it finds the network ID as

203.197.2.53 AND 255.255.128.0 = 203.197.0.0
203.197.75.201 AND 255.255.128.0 = 203.197.0.0

Both same.

Bow subnetmask for C2 is 255.255.192.0. So, the respective network IDs are

203.197.2.53 AND 255.255.192.0 = 203.197.0.0
203.197.75.201 AND 255.255.192.0 = 203.197.64.0

Both not same. So, option C.

17 votes -- Arjun Suresh (294k points)

2.41.7 Subnetting: GATE2006-IT-70 top http://gateoverflow.in/3614

Selected Answer

option (D) is correct. In the broadcast address for a subnet, all the host bits are set to 1. So as long as all the bits to the right are 1, bits left to it can be taken as possible subnet.

broadcast address for subnet is .95.255 .0101 1111. 1111 1111 (as in Class B, 16 bits each are used for network and host)

So we can take minimum 3 bits (from left) as subnet and make rest as host bits(as they are 1).

.224.0 1110 0000. 0000 0000 (leftmost 3 bits for subnet)

.240.0 1111 0000. 0000 0000 (leftmost 4 bits for subnet)

.248.0 1111 1000. 0000 0000 (... 5 bits for subnet)

13 votes -- Sandeep_Uniyal (7.3k points)

2.41.8 Subnetting: GATE2007-67, ISRO2016-72 top http://gateoverflow.in/1265

Selected Answer

this question is asking **maximum no of subnets and hosts/subnet**...NOT **how many hosts are configurable**...so no need to subtract 2 in either case...
subnet bits=6
means 2^6 or **64 subnets are possible**..
and,total hosts=2^{10} or **1024 hosts**..again no need to subtract 2 since question is asking maximum no of hosts possible not how much we can configure...
so **option d should be right** according to what they mean by maximum...

EDIT:
this is becoming a very debatable question now....firstly whatever explanation i have given is right according to question formation...people are arguing that we should subtract 2 hosts from the available, for use..i agree..but this question was about maximum possible and one option also matched..so i gone with this...

now what to do if something like this happens again in future?

from all previous year questions over this topic it seems like we have to mind read them as what they actually mean...means for the gate questions **they are treating maximum possible hosts and available hosts all as same**....so go only according to that else it would be very difficult to prove their thoughts wrong..

now if asked **how many maximum subnets** we can use..**dont subtract anything**...this atleast i can prove easily but mind it..**GATE still uses previous conventions of subtracting 2 subnets**..atleast this is what shown here in 2007..

if they ask **maximum hosts** or **configurable hosts** ,anything...**they actually wants us to subtract 2** from the hosts and then answer..**.for gate questions i think english doesnt matter..u should answer according to the past experiences and questions they have asked**...

at last..for this question **maximum subnets are 64** and **hosts are 1022 is the actual answer but according to old conventions 62 and 1022**...so go with
option c(closest)...choose wisely in the exam.... i have explained each aspect of the question...
i rest here and there shouldnt be any more confusion regarding this..!!

23 votes -- Shobhit (17.8k points)

In class B .. first 2 octet are reserved for NID and remaining for HID .. so first 6 bits of 3rd octet are used for subnet and remaining 10 bits for hosts ..

Maximum number of subnets = $2^6 - 2 = 62$

Note that 2 is subtracted because subnet values consisting of all zeros and all ones (broadcast), reducing the number of available subnets by two in classic subnetting. In modern networks, we can have 64 as well. See here: http://www.weird.com/~woods/classb.html

and no of hosts = $2^{10} - 2 = 1022$.

2 is subtracted for Number of hosts is also. The address with all bits as 1 is reserved as broadcast address and address with all host id bits as 0 is used as network address of subnet.

So option (C) is correct..

28 votes -- sonam vyas (13.2k points)

2.41.9 Subnetting: GATE2008-57 top http://gateoverflow.in/480

Selected Answer

number of zeros are to be counted for calculating the total number of possible hosts per subnet.

255-248 = 7 can be represented using 3 bits these 3bits + 8bits more = 11 bits

so possible subnets $= 2^{11}$ out of these 2 are reserved as Subnet ID and DBA

therefore we have maximum possible usable hosts = $2^{11} - 2 = 2046$

13 votes -- Amar Vashishth (28.7k points)

2.41.10 Subnetting: GATE2008-IT-85 top

http://gateoverflow.in/3409

Selected Answer

X must be able to reach the gateway using the net mask.
Subnet number of host X = 192.168.1.97 & 255.255.255.224 =192.168.1.96

Now, the gateway must also have the same subnet number. Lets take IP 192.168.1.110 of R1. 192.168.1.110 & 255.255.255.224 =192.168.1.96 and hence this can be used by X.

(To quickly identify the matching mask divide the last part of mask (224 here) into powers of 2. So, 224 = 128 + 64 + 32. Now, our host X has 97 as the last part of IP = 64 + 32 + 1. So, the last part of subnet number becomes 64 +32 =96. Now, we need to consider only those IPs whose last part will contain 64 as well as 32)

http://courses.washington.edu/css432/joemcc/slides/03_cidr.ppt

24 votes -- Arjun Suresh (294k points)

2.41.11 Subnetting: GATE2010-47 top

http://gateoverflow.in/2349

Selected Answer

D is correct answer because

when we perform AND operation between ip addres **10.105.1.113 and 255.255.255.224** result is **10.105.1.96**

when we perform AND operation between ip address **10.105.1.91** and **255.255.255.224** result is **10.105.1.64**

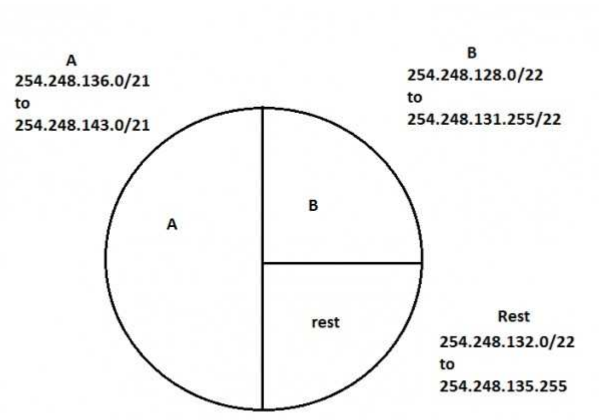
10.105.1.96 and 10.105.1.64 are different network so D is correct answer

20 votes -- R.B. Tiwari (357 points)

2.41.12 Subnetting: GATE2012_34 top

http://gateoverflow.in/1752

Selected Answer



Correct option will be **A**

12 votes -- Ashish Patel (205 points)

ans should be a) , the mask are /21 and/22 respectively, acc. to the half and quarter chunks requirement... and option b) can creat problem as address can get clashed between the two..

10 votes -- Sneha Goel (1.2k points)

2.41.13 Subnetting: GATE2015-2_41 top http://gateoverflow.in/8213

option A is correct .. do the AND operation of group1 with net mask you will get the answer

12 votes -- Anoop Sonkar (4.9k points)

2.41.14 Subnetting: GATE2015-3_38 top http://gateoverflow.in/8497

Selected Answer

Answer=158

144 in binary = 100 10000

out of this 3 bits in left are subnet bits. (27 bits are used for subnet, which means top 3 bytes and leftmost 3 bits from the last byte)

so the 4th octet in the last ip address of the network which can be assigned to a host is 100 11110. (its not 100 11111 because its network broadcast address)

so 10011110 is 158 in decimal.

30 votes -- overtomanu (1.2k points)

2.42 Tcp(12) top

2.42.1 Tcp: GATE 2016-2-25 top http://gateoverflow.in/39572

Identify the correct sequence in which the following packets are transmitted on the network by a host when a browser requests a webpage from a remote server, assuming that the host has just been restarted.

A. HTTP GET request, DNS query, TCP SYN
B. DNS query, HTTP GET request, TCP SYN
C. DNS query, TCP SYN, HTTP GET request.
D. TCP SYN, DNS query, HTTP GET request.``

gate2016-2 computer-networks normal tcp

Answer

2.42.2 Tcp: GATE2004-IT-23 top http://gateoverflow.in/3664

Which one of the following statements is FALSE?

A. TCP guarantees a minimum communication rate
B. TCP ensures in-order delivery
C. TCP reacts to congestion by reducing sender window size
D. TCP employs retransmission to compensate for packet loss

gate2004-it computer-networks tcp normal

Answer

2.42.3 Tcp: GATE2004-IT-28 top http://gateoverflow.in/3669

In TCP, a unique sequence number is assigned to each

A. byte
B. word
C. segment
D. message

gate2004-it computer-networks tcp normal

Answer

2.42.4 Tcp: GATE2007-IT-13 top

http://gateoverflow.in/3446

Consider the following statements about the timeout value used in TCP.

i. The timeout value is set to the RTT (Round Trip Time) measured during TCP connection establishment for the entire duration of the connection.
ii. Appropriate RTT estimation algorithm is used to set the timeout value of a TCP connection.
iii. Timeout value is set to twice the propagation delay from the sender to the receiver.

Which of the following choices hold?

A. (i) is false, but (ii) and (iii) are true
B. (i) and (iii) are false, but (ii) is title
C. (i) and (ii) are false, but (iii) is true
D. (i), (ii) and (iii) are false

gate2007-it computer-networks tcp normal

Answer

2.42.5 Tcp: GATE2007-IT-14 top

http://gateoverflow.in/3447

Consider a TCP connection in a state where there are no outstanding ACKs. The sender sends two segments back to back. The sequence numbers of the first and second segments are 230 and 290 respectively. The first segment was lost, but the second segment was received correctly by the receiver. Let X be the amount of data carried in the first segment (in bytes), and Y be the ACK number sent by the receiver.
The values of X and Y (in that order) are

A. 60 and 290
B. 230 and 291
C. 60 and 231
D. 60 and 230

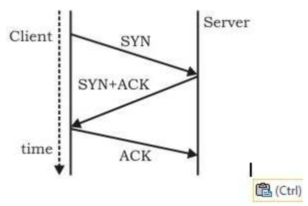
gate2007-it computer-networks tcp normal

Answer

2.42.6 Tcp: GATE2008-IT-69 top

http://gateoverflow.in/3383

The three way handshake for TCP connection establishment is shown below.



Which of the following statements are TRUE?
S1: Loss of SYN + ACK from the server will not establish a connection

S2: Loss of ACK from the client cannot establish the connection

S3: The server moves LISTEN → SYN_RCVD → SYN_SENT → ESTABLISHED in the state machine on no packet loss

S4: The server moves LISTEN → SYN_RCVD → ESTABLISHED in the state machine on no packet loss

A. S2 and S3 only
B. S1 and S4 only
C. S1 and S3 only
D. S2 and S4 only

gate2008-it computer-networks tcp normal

Answer

2.42.7 Tcp: GATE2009-47 top http://gateoverflow.in/1333

While opening a TCP connection, the initial sequence number is to be derived using a time-of-day (ToD) clock that keeps running even when the host is down. The low order 32 bits of the counter of the ToD clock is to be used for the initial sequence numbers. The clock counter increments once per milliseconds. The maximum packet lifetime is given to be 64s.

Which one of the choices given below is closest to the minimum permissible rate at which sequence numbers used for packets of a connection can increase?

A. 0.015/s
B. 0.064/s
C. 0.135/s
D. 0.327/s

gate2009 computer-networks tcp difficult

Answer

2.42.8 Tcp: GATE2012_22 top http://gateoverflow.in/1605

Which of the following transport layer protocols is used to support electronic mail?

(A) SMTP
(B) IP
(C) TCP
(D) UDP

gate2012 computer-networks tcp easy

Answer

2.42.9 Tcp: GATE2015-1_19 top http://gateoverflow.in/8217

Suppose two hosts use a TCP connection to transfer a large file . Which of the following statements is/are FALSE with respect to the TCP connection?

I. If the sequence number of a segment is m, then the sequence number of the subsequent segment is always m+1.
II. If the estimated round trip time at any given point of time is t sec, the value of the retransmission timeout is always set to greater than or equal to t sec.
III. The size of the advertised window never changes during the course of the TCP connection.
IV. The number of unacknowledged bytes at the sender is always less than or equal to the advertised window.

A. III only
B. I and III only
C. I and IV only
D. II and IV only

gate2015-1 computer-networks tcp normal

Answer

2.42.10 Tcp: GATE2015-2-34 top http://gateoverflow.in/8154

Assume that the bandwidth for a TCP connection is 1048560 bits/sec. Let α be the value of RTT in milliseconds (rounded off to the nearest integer) after which the TCP window scale option is needed. Let β be the maximum possible window size with window scale option. Then the values of α and β are

A. 63 milliseconds, 65535 $\times 2^{14}$
B. 63 milliseconds, 65535 $\times 2^{16}$
C. 500 milliseconds, 65535 $\times 2^{14}$
D. 500 milliseconds, 65535 $\times 2^{16}$

gate2015-2 computer-networks difficult tcp

Answer

2.42.11 Tcp: GATE2015-3_22 top

http://gateoverflow.in/8425

Consider the following statements.

I. TCP connections are full duplex
II. TCP has no option for selective acknowledgement
III. TCP connections are message streams

A. Only I is correct
B. Only I and III are correct
C. Only II and III are correct
D. All of I, II and III are correct

gate2015-3 computer-networks tcp normal

Answer

2.42.12 Tcp: GATE2017-1-14 top

http://gateoverflow.in/118194

Consider a TCP client and a TCP server running on two different machines. After completing data transfer, the TCP client calls close to terminate the connection and a FIN segment is sent to the TCP server. Server-side TCP responds by sending an ACK, which is received by the client-side TCP. As per the TCP connection state diagram (RFC 793), in which state does the client-side TCP connection wait for the FIN from the server-side TCP?

(A) LAST-ACK

(B) TIME-WAIT

(C) FIN-WAIT-1

(D) FIN-WAIT-2

gate2017-1 computer-networks tcp

Answer

Answers: Tcp

2.42.1 Tcp: GATE 2016-2-25 top

http://gateoverflow.in/39572

Selected Answer

Here

C) Seems correct answer.

Say you type www.google.com

FIrst you send DNS request to get IP address. Then you establish connection with IP of google using TCP. Finally you start talking in HTTP !

21 votes -- Akash (43.8k points)

2.42.2 Tcp: GATE2004-IT-23 top

http://gateoverflow.in/3664

Selected Answer

Option B: "Sequence numbers allow receivers to discard duplicate packets and properly sequence reordered packets."

Option C: "When congestion is detected, the transmitter decreases the transmission rate by a multiplicative factor; for example, cut the congestion window in half after loss." (Additive Increase/multiplicative decrease)

Option D: "Acknowledgments allow senders to determine when to retransmit lost packets."

So, A is answer.

http://en.wikipedia.org/wiki/Transmission_Control_Protocol#Error_detection

http://en.wikipedia.org/wiki/Additive_increase/multiplicative_decrease

10 votes -- Arjun Suresh (294k points)

2.42.3 Tcp: GATE2004-IT-28 top

http://gateoverflow.in/3669

Selected Answer

a) it should be byte

http://www.industrialethernetu.com/courses/202_2.htm

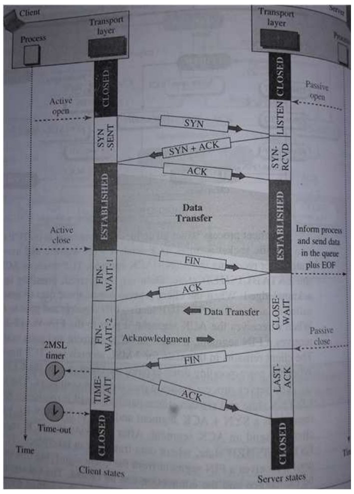
13 votes -- Parul Agarwal (793 points)

2.42.4 Tcp: GATE2007-IT-13 top

http://gateoverflow.in/3446

Selected Answer

i) TCP connection established in 3 phase between SYN send and SYN received (SYN,SYN+ACK,ACK).After this connection establishment data transfer takes place. Now, FIN flag is called to close the connection. FIN flag can close the connection after the ACK get from the receiver. If ACK is not received,then, a timer set. Which wait for the time out. So, there is no relationship between TCP connection establishment with Timeout of RTT.



ii)This is Jacobson's algorithm .(Thanks @Anirudh)

```
ERTT=p*IRTT+(1-p)*NRTT
p is scalling factor
IRTT initial RTT
NRTT is new RTT
```

Link here

iii)Actually TO value more than twice propagation delay from sender to receiver.Because after connection establishment completes and data transfer completes, then only timeout occurs. So, if we start timer at the begining of transaction, Time Out occurs after RTT completes and after final ACK comes. So, Time Out time must be more than RTT.

So, only (II) is TRUE

7 votes -- srestha (58.4k points)

2.42.5 Tcp: GATE2007-IT-14 top

http://gateoverflow.in/3447

Selected Answer

Ans is D

Because it is said that the connection is TCP and the sender has sent first two segments which is clear from the text "The sequence numbers of the first and second segments are 230 and 290 respectively." That means there must be 3 Way handshaking that has been done before the connection has been established and when sender has sent SYN packet then reciever must have ACKED him with next packet .In response to it reciever only recieved only 1 packet so he will come to know that 1st packet has been lost and again he will send ACK for lost packet

10 votes -- Aditi Tiwari (1.1k points)

ans d)

14 votes -- Aditi Dan (5.3k points)

2.42.6 Tcp: GATE2008-IT-69 top

http://gateoverflow.in/3383

Selected Answer

(S1) Loss of SYN + ACK from the server will not establish a connection => True.
(S2) Loss of ACK from the client cannot establish the connection => No this is not true. Detail reasoning -> http://stackoverflow.com/questions/16259774/what-if-a-tcp-handshake-segment-is-lost

If after ACK client immediately sends data then everything goes on without worry. (Though if along with ACK, first data packet is dropped, connection is reset)

(S3) The server moves LISTEN → SYN_RCVD → SYN_SENT → ESTABLISHED in the state machine on no packet loss =>False .
(S4) The server moves LISTEN → SYN_RCVD → ESTABLISHED in the state machine on no packet loss. => True

ANswer => S1 and S4 are true.

Reference for S4 => https://www.rfc-editor.org/rfc/rfc793.txt

```
September 1981
                                           Transmission Control Protocol
                                                Functional Specification




                              +---------+ ---------\      active OPEN
                              |  CLOSED |            \    -----------
                              +---------+<---------\   \   create TCB
                                |     ^              \   \  snd SYN
                   passive OPEN |     |   CLOSE        \   \
                   ------------ |     | ----------       \   \
                    create TCB  |     | delete TCB         \   \
                                V     |                      \   \
                              +---------+            CLOSE    |    \
                              |  LISTEN |          ---------- |     |
                              +---------+          delete TCB |     |
                   rcv SYN      |     |     SEND              |     |
                  -----------   |     |    -------            |     V
 +---------+      snd SYN,ACK  /       \   snd SYN          +---------+
 |         |<-----------------           ------------------>|         |
 |   SYN   |                    rcv SYN                     |   SYN   |
 |   RCVD  |<-----------------------------------------------|   SENT  |
 |         |                    snd ACK                     |         |
 |         |------------------           -------------------|         |
 +---------+   rcv ACK of SYN  \       /  rcv SYN,ACK       +---------+
```

```
   |           --------------    |     |   -----------
   |                  x          |     |     snd ACK
   |                             V     V
   |  CLOSE                    +---------+
   | -------                   |  ESTAB  |
   | snd FIN                   +---------+
   |                   CLOSE    |     |    rcv FIN
   V                  -------   |     |    -------
+---------+           snd FIN  /       \   snd ACK          +---------+
|  FIN    |<-----------------           ------------------>|  CLOSE  |
| WAIT-1  |------------------                              |   WAIT  |
+---------+           rcv FIN  \                            +---------+
  | rcv ACK of FIN   -------   |                            CLOSE  |
  | --------------   snd ACK   |                           ------- |
  V        x                   V                           snd FIN V
+---------+                  +---------+                   +---------+
|FINWAIT-2|                  | CLOSING |                   | LAST-ACK|
+---------+                  +---------+                   +---------+
  |                rcv ACK of FIN |                 rcv ACK of FIN |
  |  rcv FIN       -------------- |    Timeout=2MSL -------------- |
  |  -------              x       V    ------------        x       V
   \ snd ACK                 +---------+delete TCB         +---------+
    ------------------------>|TIME WAIT|------------------>| CLOSED  |
                             +---------+                   +---------+

                      TCP Connection State Diagram
                               Figure 6.
```

15 votes -- Akash (43.8k points)

2.42.7 Tcp: GATE2009-47 top http://gateoverflow.in/1333

Selected Answer

Ans is option A .

3 information present in the question.

(1)The low order 32 bits of the counter of the ToD clock is to be used for the initial sequence numbers - That means only 32 bits are used to represent a sequence number.So we have 2^32 different sequence number.

(2)The maximum packet lifetime is 64s. So by 1 & 2 we can calculate maximum data rate possible(bandwidth) to avoid the wraparound=2^32/64=2^26 Byte/sec .

(3)The clock counter increments once per milliseconds -That means when then counter increments next possible sequence number is generated.

Suppose we make a TCP connection by picking initial sequence number that is derived by clock.If the connection terminate after sending few bytes of data then to avoid the ambiguity of sequence number we don't reestablish the connection immediately because of counter increment happen after 1 msec.

Suppose the sender sends 2^24 Byte data.

Time required to sent 2^24 Byte data is 2^24/2^26=250 ms. So 2^24 Byte takes 2^24 sequence number . (2^24 * 1)ms required to increment the counter .

So the permissible rate of sequence number used for packets is in 64 sec we use only sequence number .

So 1/64= 0.015(approx) which is option A here .

17 votes -- Abhishek Verma (335 points)

A. Because sequence number is incremented once every 64 sec.

Rate = 1/64=0.015

13 votes -- Viral Kapoor (2k points)

2.42.8 Tcp: GATE2012_22 top http://gateoverflow.in/1605

Selected Answer

answer = option C : TCP

There are three primary TCP/IP protocols for E-Mail management:

- Post Office Protocol (POP)
- Simple Mail Transfer Protocol (SMTP)
- Internet Message Access Protocol (IMAP)

They all are Application Layer Protocols

Once a client connects to the E-mail Server, there may be 0(zero) or more SMTP transactions. If the client has no mail to send, then there are no SMTP transactions. Every e-mail message sent is an SMTP transfer.

SMTP is only used to send (push) messages to the server. POP and IMAP are used to receive messages as well as manage the mailbox contents(which includes tasks such as deleting, moving messages etc.).

15 votes -- Amar Vashishth (28.7k points)

2.42.9 Tcp: GATE2015-1_19 top

http://gateoverflow.in/8217

Selected Answer

Option B

III. False. It is the size of the receiver's buffer that's never changed. RcvWindow is the part of the receiver's buffer that's changing all the time depending on the processing capability at the receiver's side and the network traffic.

http://web.eecs.utk.edu/~qi/teaching/ece453f06/hw/hw7_sol.htm

15 votes -- GATERush (1.2k points)

2.42.10 Tcp: GATE2015-2-34 top

http://gateoverflow.in/8154

Selected Answer

In TCP when the **bandwidth delay product** increases beyond 64K receiver window scaling is needed.

The bandwidth delay product is the maximum amount of data on the network circuit at any time and is measured as RTT * Bandwidth. This is not the time for sending data rather just the time for sending data without acknowledgement.

So, here, we have bandwidth delay product = (1048560 / 8) B * α = 64 K
α = (64 K * 8) / 1048560 = 0.5 s = 500 milliseconds.

When window scaling happens, a 14 bit shift count is used in TCP header. So, the maximum possible window size gets increased from 2^{16}-1 to (2^{16}-1) * 2^{14} or from 65535 to 65535 * 2^{14}

http://en.wikipedia.org/wiki/TCP_window_scale_option

26 votes -- Arjun Suresh (294k points)

2.42.11 Tcp: GATE2015-3_22 top

http://gateoverflow.in/8425

Selected Answer

answer is (A) since TCP has options for selective ACK and TCP uses byte streams that is every byte that is send using TCP is numbered.

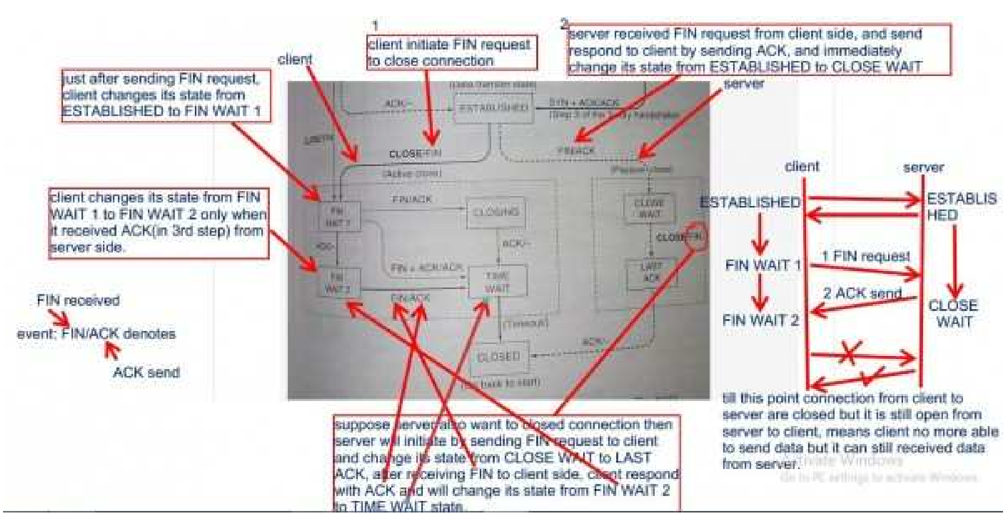
http://repo.hackerzvoice.net/depot_madchat/ebooks/TCP-IP_Illustrated/tcp_tran.htm

17 votes -- Tamojit Chatterjee (2.2k points)

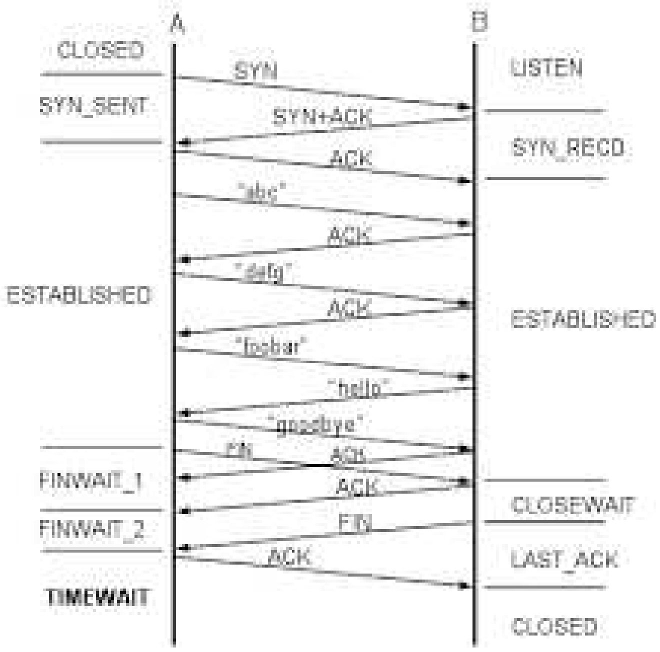
2.42.12 Tcp: GATE2017-1-14 top

http://gateoverflow.in/118194

Selected Answer



so D is ans.



7 votes -- 2018 (5.2k points)

2.43 Token Bucket(2) top

2.43.1 Token Bucket: GATE 2016-1-54 top

http://gateoverflow.in/39720

For a host machine that uses the token bucket algorithm for congestion control, the token bucket has a capacity of 1 mega byte and the maximum output rate is 20 mega bytes per second. Tokens arrive at a rate to sustain output at a rate of 10 mega bytes per second. The token bucket is currently full and the machine needs to send 12 mega bytes of data. The minimum time required to transmit the data is _____________ seconds.

gate2016-1 computer-networks token-bucket normal numerical-answers

Answer

2.43.2 Token Bucket: GATE2008-58 top

http://gateoverflow.in/481

A computer on a 10Mbps network is regulated by a token bucket. The token bucket is filled at a rate of 2Mbps. It is initially filled to capacity with 16Megabits. What is the maximum duration for which the computer can transmit at the full 10Mbps?

A. 1.6 seconds
B. 2 seconds
C. 5 seconds
D. 8 seconds

gate2008 computer-networks token-bucket

Answer

Answers: Token Bucket

2.43.1 Token Bucket: GATE 2016-1-54 top

http://gateoverflow.in/39720

Selected Answer

Initially token bucket is full.

Rate at which it is emptying is $(20-10)$ **MBps**.

Time taken to empty token bucket of 1 **MB** is $\frac{1}{10}$ i.e 0.1 sec.

Data send in this time is $0.1*20=2$ **MB (rate at which bucket is emptying is different from rate at which data is send)** .

Data left to send is $12-2=10$ **MB** .

Now bucket is empty and rate of token arriving is less than that of going out so effective data speed will be 10 **MBps**.

Time to send remaining 10 **MB** will be 1 sec. So total time is $1+0.1$=1.1sec

32 votes -- Vaibhav Singh (601 points)

Reffer: Token-Bucket .

- Token bucket has a capacity of 1 mega **byte** (maximum capacity C)

  Here one **byte** is considered as one token

  $\Rightarrow C = 1\text{M tokens}$

- output rate is 20 mega bytes per second ($M = 20\text{MBps}$)
- Tokens arrive at a rate to **sustain output** at a rate of 10 mega bytes per second

  $20 - R = 10$

  $\Rightarrow$ Input Rate $R = 10\text{MBps}$

  Unlike Leaky Bucket , idle hosts can capture and save up $c \leq C$ tokens in order to send larger bursts later.

  When we begin transfer the tokens present in token buckt is transmitted at once to the network

  ie. if initally capacity of token bucket is **'c'** then c tokens will be instantly be present in the network.

Time to Empty the token bucket

c: is the inital capacity of token bucket
R: every sec we are getting R tokens
M : evey seconds M tokens are produced

INPUT FLOW : Then the number of packets that are ready to enter the network during a time interval 't' is $c + Rt$

OUTPUT FLOW : Then the number of packets that are ready to enter the network during a time interval 't' is Mt

INPUT FLOW = OUTPUT FLOW

$$\Rightarrow c + Rt = Mt$$

$$t = \frac{c}{M - R}$$
$$= \frac{1}{20 - 10}$$
$$= 0.1 \text{sec}$$

- Given that Token bucket is full ($c = C$)

Now , We have got two cases

- To transfer 1M tokens , Will it be instantly with t=0
- Or to transfer 1M tokens , we take 10/ 20-10 = 0.1sec ?

To transfer 1M (inital token) tokens , Will it be instantly with t=0

Consider the equation

INPUTFLOW = c+Rt

This means that
" c tokens (initally contained in token bucket) are transmitted without any delays "

Unlike Leaky bucket , token buckets can keep on reserving token if the sender is idle .Once it is ready to send the packets . Packets will take the token and will be transmitted to the network. $\Rightarrow c$ And then we are adding the R tokens produced in $'t'$ time to finnaly get the INPUTFLOW

$\Rightarrow 1\text{MB}$ is *transmitted instantly* . Now we are left with 11 MB to transmit

To trnasfer remaining 11 MB

at $t = 0$ we begin transmitting 11 MB data.

at $t = 0.1$sec : 1MB (1 MB transfered)

at $t = 0.2$sec : 1MB (2 MB transfered)

..
..

at $t = 1.1$ sec : 1MB (11 MB transfered)

Therefore to transfer 12MB it takes **1.1sec + 0 sec = 1.1 sec**

Transfer 1M (inital token) tokens , we take = 0.1sec

(if it take 0.1 sec for 1MB i could argue that it will take 1.2ssec for 12MB)

then during 0.1sec . 01 *10MBps = 1M tokens are fulled up .

t=0s : begin to transfer 12 MB data.

t=0.1s : 1MB

t=0.2s : 1MB (2 MB transfered)

t=0.3s : 1MB (3 MB transfered)
..
..

t=1.2s : 1MB (12 MB transfered)

Therefore to transfer 12MB it takes **1.2sec**

Question does clearly mention about this part . Hence it is common practice to always follw the best case .
Therefore the answer would be **1.1 sec**

Reference

- http://www.slideshare.net/vimal25792/leaky-bucket-tocken-buckettraffic-shaping
- http://web.mst.edu/~saifullaha/courses/lecture19.pdf
- https://onl.wustl.edu/Tutorial/Filters,_Queues_and_Bandwidth/NSP_Architecture/Link_Rate.html
- http://quiz.geeksforgeeks.org/gate-gate-cs-2016-set-1-question-64/
- http://www.slideshare.net/UmeshGupta3/leaky-bucket-algorithm

10 votes -- pC (21.4k points)

2.43.2 Token Bucket: GATE2008-58 top http://gateoverflow.in/481

Selected Answer

New tokens are added at the rate of r bits/sec which is
2Mbps in the given question.

Capacity of the token bucket (b) = 16 Mbits
Maximum possible transmission rate (M) = 10Mbps
So the maximum burst time = b/(M-r) = 16/(10-2) = 2 seconds

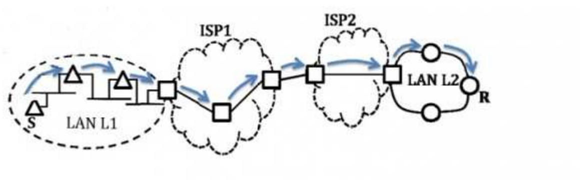
here is the animation for token bucket hope this will help us to understand the concept.

18 votes -- Vikrant Singh (13.4k points)

2.44 Token Ring(1) top

2.44.1 Token Ring: GATE2014-2-25 top http://gateoverflow.in/1983

In the diagram shown below, L1 is an Ethernet LAN and L2 is a Token-Ring LAN. An IP packet originates from sender S and traverses to R, as shown. The links within each ISP and across the two ISPs, are all point-to-point optical links. The initial value of the TTL field is 32. The maximum possible value of the TTL field when R receives the datagram is ________.



gate2014-2 computer-networks numerical-answers lan-technologies ethernet token-ring normal

Answer

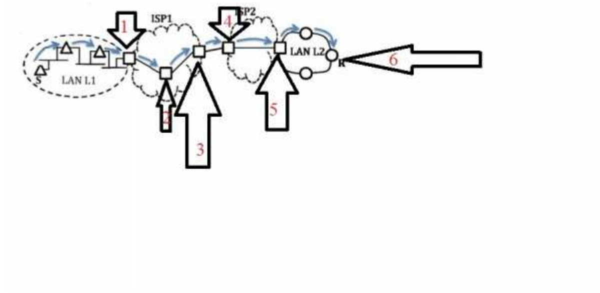
Answers: Token Ring

2.44.1 Token Ring: GATE2014-2-25 top http://gateoverflow.in/1983

Selected Answer

Each time a packet visits network layer it decrements it's TTL field. Source initializes it and others decreaments it. Inside

LAN it never goes to network layer, it is forwarded from data link layer itself.. in routers it goes upto network layer to make a routing decision.. and the router decrements it because the packet has visited the network layer.. and at the receiver too, the packet has visited the network layer and network layer will do it's job and decrements the TTL value.



There are 5 routers, So Network Layer will be visited 5 times and 1 time on destination

So, TTL $= 26$

PS:) A receiver decrements TTL value and then checks whether it is 0 (or) not. So, 26 is the answer (not 27)

25 votes -- Kalpish Singhal (2.1k points)

TTL field reduced at each router, there are total 5 routers and finally at receiver.

=32 -(5+1)=26

11 votes -- Keith Kr (6.3k points)

2.45 Udp(4) top

2.45.1 Udp: GATE2005-23 top http://gateoverflow.in/1359

Packets of the same session may be routed through different paths in:

A. TCP, but not UDP
B. TCP and UDP
C. UDP, but not TCP
D. Neither TCP nor UDP

gate2005 computer-networks tcp udp easy

Answer

2.45.2 Udp: GATE2006-IT-69 top http://gateoverflow.in/3613

A program on machine X attempts to open a UDP connection to port 5376 on a machine Y, and a TCP connection to port 8632 on machine Z. However, there are no applications listening at the corresponding ports on Y and Z. An ICMP Port Unreachable error will be generated by

A. Y but not Z
B. Z but not Y
C. Neither Y nor Z
D. Both Y and Z

gate2006-it computer-networks tcp udp normal

Answer

2.45.3 Udp: GATE2013_12 top http://gateoverflow.in/1421

The transport layer protocols used for real time multimedia, file transfer, DNS and email, respectively are

(A) TCP, UDP, UDP and TCP

(B) UDP, TCP, TCP and UDP

(C) UDP, TCP, UDP and TCP

(D) TCP, UDP, TCP and UDP

gate2013 computer-networks tcp udp easy

Answer

2.45.4 Udp: GATE2017-2-18 top

http://gateoverflow.in/118209

Consider socket API on a Linux machine that supports connected UDP sockets. A connected UDP socket is a UDP socket on which *connect* function has already been called. Which of the following statements is/are CORRECT?

I. A connected UDP socket can be used to communicate with multiple peers simultaneously.
II. A process can successfully call *connect* function again for an already connected UDP socket.

A. I only
B. II only
C. Both I and II
D. Neither I nor II

gate2017-2 computer-networks udp

Answer

Answers: Udp

2.45.1 Udp: GATE2005-23 top

http://gateoverflow.in/1359

Selected Answer

b) TCP and UDP.

Routing happens in Network layer and hence has no dependency with the the transport layer protocols TCP and UDP. The transport layer protocol- whether TCP or UDP is hidden to the router and the routing path is determined based on the the network configuration at the time and hence can change even during a session.

Ref: http://stackoverflow.com/questions/15601389/if-tcp-is-connection-oriented-why-do-packets-follow-different-paths

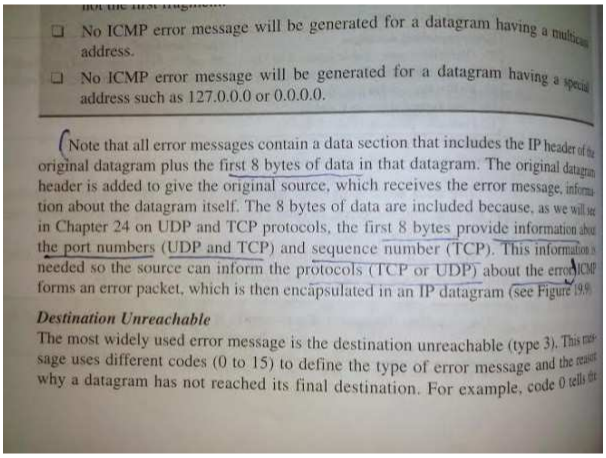
29 votes -- Arjun Suresh (294k points)

2.45.2 Udp: GATE2006-IT-69 top

http://gateoverflow.in/3613

Selected Answer

yes , for both TCP & UDP packet , an ICMP port unreachable error will be generated. icmp packet contains 8 byte data (both from tcp and udp header) where it contains dummy port no just for checking trace rout . References below from forouzan book--



No ICMP error message will be generated for a datagram having a multicast address.

No ICMP error message will be generated for a datagram having a special address such as 127.0.0.0 or 0.0.0.0.

Note that all error messages contain a data section that includes the IP header of the original datagram plus the first 8 bytes of data in that datagram. The original datagram header is added to give the original source, which receives the error message, information about the datagram itself. The 8 bytes of data are included because, as we will see in Chapter 24 on UDP and TCP protocols, the first 8 bytes provide information about the port numbers (UDP and TCP) and sequence number (TCP). This information is needed so the source can inform the protocols (TCP or UDP) about the error. ICMP forms an error packet, which is then encapsulated in an IP datagram (see Figure 19.9).

Destination Unreachable

The most widely used error message is the destination unreachable (type 3). This message uses different codes (0 to 15) to define the type of error message and the reason why a datagram has not reached its final destination. For example, code 0 tells the

8 votes -- koushik sinha (1.3k points)

2.45.3 Udp: GATE2013_12 top

http://gateoverflow.in/1421

Selected Answer

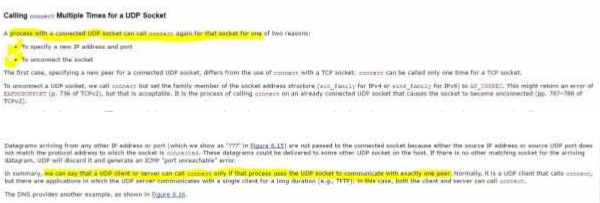
Real Time Multimedia: Data packets should be delivered faster. Also it can be unreliable. Therefore UDP.
File Transfer: For example downloading a file. It should be secure and reliable. Therefore TCP.
DNS: uses both UDP and TCP for its transport. But to acheive efficiency DNS uses UDP. To start a TCP connection a minimum of three packets are required (SYN out, SYN+ACK back, ACK out). UDP uses a simple transmission model with a minimum of protocol mechanism. UDP has no handshaking dialogues.
Email: uses SMTP protocol which uses TCP protocol.

Therefore, **C** is the answer.

19 votes -- Pyuri sahu (2.2k points)

2.45.4 Udp: GATE2017-2-18 top

http://gateoverflow.in/118209



Calling connect Multiple Times for a UDP Socket

A process with a connected UDP socket can call connect again for that socket for one of two reasons:

- To specify a new IP address and port
- To unconnect the socket

The first case, specifying a new peer for a connected UDP socket, differs from the use of connect with a TCP socket: connect can be called only one time for a TCP socket.

To unconnect a UDP socket, we call connect but set the family member of the socket address structure (sin_family for IPv4 or sin6_family for IPv6) to AF_UNSPEC. This might return an error of EAFNOSUPPORT (p. 736 of TCPv2), but that is acceptable. It is the process of calling connect on an already connected UDP socket that causes the socket to become unconnected (pp. 787–788 of TCPv2).

Datagrams arriving from any other IP address or port (which we show as "???" in Figure 8.15) are not passed to the connected socket because either the source IP address or source UDP port does not match the protocol address to which the socket is connected. These datagrams could be delivered to some other UDP socket on the host. If there is no other matching socket for the arriving datagram, UDP will discard it and generate an ICMP "port unreachable" error.

In summary, we can say that a UDP client or server can call connect only if that process uses the UDP socket to communicate with exactly one peer. Normally, it is a UDP client that calls connect, but there are applications in which the UDP server communicates with a single client for a long duration (e.g., TFTP); in this case, both the client and server can call connect.

The DNS provides another example, as shown in Figure 8.16.

http://www.masterraghu.com/subjects/np/introduction/unix_network_programming_v1.3/ch08lev1sec11.html

so option B should be ans.

for 1st part if not "connected" then i ll be true http://stackoverflow.com/questions/3329641/how-do-multiple-clients-connect-simultaneously-to-one-port-say-80-on-a-server

4 votes -- 2018 (5.2k points)

2.46 Wifi(1) top

2.46.1 Wifi: GATE 2016-2-54 top

http://gateoverflow.in/39593

For the IEEE 802.11 MAC protocol for wireless communication, which of the following statements is/are **TRUE**?

(I) At least three non-overlapping channels are available for transmissions.

(II) The RTS-CTS mechanism is used for collision detection.

(III) Unicast frames are ACKed.

A. All I, II, and III
B. I and III only
C. II and III only
D. II only

gate2016-2 computer-networks wifi normal

Answer

Answers: Wifi

2.46.1 Wifi: GATE 2016-2-54 top

http://gateoverflow.in/39593

Selected Answer

802.11 MAC = Wifi

I) This is true, maximum 3 overlapping channels are possible in Wifi !

II) This is false. Collusion detection is not really possible in Wireless, because signal strength of sending & receiving signal need not be same ! So Wifi uses **collusion Avoidance** instead ! In this RTS-CTS are used to announce to all nodes, that for which node wireless channel is reserved for communication. So this is collusion avoidance, not detection

III) This is true. Every frame in Wifi is acked, because Wifi station do not use collusion detection, in Ethernet we use collusion detection, in which it is possible for us to listen channel for collusion & use exponential back off in case of collusion detection. As in case of wifi, due to more error rate and not using collusion detection strategy , we instead use ACK frame, in case of not getting ACK Host will retransmit after Random back off period

Ans => B

Source => Kurose & Ross Top down appraoch to internet

18 votes -- Akash (43.8k points)

3 Databases (203) top

3.0.1 GATE1990-2-iv top http://gateoverflow.in/83977

Match the pairs in the following questions:

(a) Secondary index	(p) Function dependency
(b) Non-procedural query language	(q) B-tree
(c) Closure of a set of attributes	(r) Domain calculus.
(d) Natural join	(s) Relational algebraic operations

gate1990 match-the-following databases

Answer

3.0.2 GATE2017-2-17 top http://gateoverflow.in/118157

An ER model of a database consists of entity types A and B. These are connected by a relationship R which does not have its one attribute. Under which one of the following conditions, can the relational table for R be merged with that of A?

A. Relationship R is one-to-many and the participation of A in R is total
B. Relationship R is one-to-many and the participation of A in R is partial
C. Relationship R is many-to-one and the participation of A in R is total
D. Relationship R is many-to-one and the participation of A in R is partial

gate2017-2 databases

Answer

Answers:

3.0.1 GATE1990-2-iv top http://gateoverflow.in/83977

Selected Answer

a-q

b-r

c-p

d-s

2 votes -- Amitabh Tiwari (2.5k points)

3.0.2 GATE2017-2-17 top http://gateoverflow.in/118157

Selected Answer

The relation table for R should always be merged with the entity that has total participation and relationship should be many to one.

Ans: C

10 votes -- Arnabi (6.4k points)

3.1 B Tree(22) top

3.1.1 B Tree: GATE 2016-2-21 top

http://gateoverflow.in/39569

B+ Trees are considered BALANCED because.

A. The lengths of the paths from the root to all leaf nodes are all equal.
B. The lengths of the paths from the root to all leaf nodes differ from each other by at most 1.
C. The number of children of any two non-leaf sibling nodes differ by at most 1.
D. The number of records in any two leaf nodes differ by at most 1.

gate2016-2 databases b-tree normal

Answer

3.1.2 B Tree: GATE1989-12a top

http://gateoverflow.in/91199

Fig.7 shows a B-tree where only key values are indicated in the records. Each block can hold upto three records. A record with a key value 34 is inserted into the B-tree. Obtain the modified B-tree after insertion.

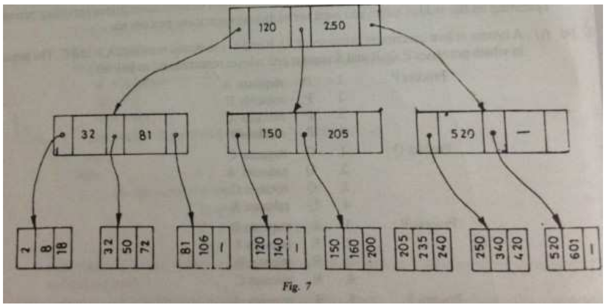


Fig. 7

descriptive gate1989 databases b-tree

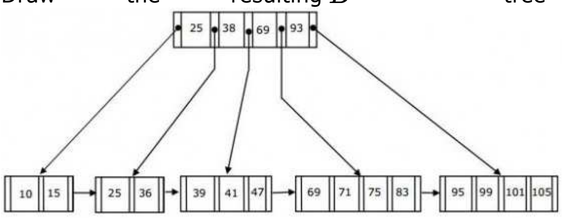
Answer

3.1.3 B Tree: GATE1994_14 top

http://gateoverflow.in/2510

Consider B^{+} - tree of order d shown in figure. (A B^{+} - tree of order d contains between d and $2d$ keys in each node)

a. Draw the resulting B^{+} - tree after 100 is inserted in the figure below.



b. For a B^{+} - tree of order d with n leaf nodes, the number of nodes accessed during a search is $O(-)$.

gate1994 databases b-tree normal

Answer

3.1.4 B Tree: GATE1997_19 top

http://gateoverflow.in/2279

A B^+ - tree of order d is a tree in which each internal node has between d and $2d$ key values. An internal node with M key values has $M + 1$ children. The root (if it is an internal node) has between 1 and $2d$ key values. The distance of a node from the root is the length of the path from the root to the node. All leaves are at the same distance from the root. The height of the tree is the distance of a leaf from the root.

a. What is the total number of key values in the internal nodes of a B^+-tree with l leaves ($l \geq 2$)?

b. What is the maximum number of internal nodes in a B^+ - tree of order 4 with 52 leaves?

c. What is the minimum number of leaves in a B^+-tree of order d and height $h(h \geq 1)$?

gate1997 databases b-tree normal

Answer

3.1.5 B Tree: GATE1999_1.25 top

http://gateoverflow.in/1478

Which of the following is correct?

A. B-trees are for storing data on disk and B$^+$ trees are for main memory.

B. Range queries are faster on B$^+$ trees.

C. B-trees are for primary indexes and B$^+$ trees are for secondary indexes.

D. The height of a B$^+$ tree is independent of the number of records.

gate1999 databases b-tree normal

Answer

3.1.6 B Tree: GATE1999_21 top

http://gateoverflow.in/1520

Consider a B-tree with degree m, that is, the number of children, c, of any internal note (except the root) is such that $m \leq c \leq 2m - 1$. Derive the maximum and minimum number of records in the leaf nodes for such a B-tree with height $h, h \geq 1$. (Assume that the root of a tree is at height 0).

gate1999 databases b-tree normal

Answer

3.1.7 B Tree: GATE2000-1.22, UGCNET-June2012-II-11 top

http://gateoverflow.in/646

B$^+$-trees are preferred to binary trees in databases because

A. Disk capacities are greater than memory capacities
B. Disk access is much slower than memory access
C. Disk data transfer rates are much less than memory data transfer rates
D. Disks are more reliable than memory

gate2000 databases b-tree normal ugcnetjune2012ii

Answer

3.1.8 B Tree: GATE2002-17 top

http://gateoverflow.in/870

a. The following table refers to search items for a key in B-trees and B^+ trees.

B−tree		B+−tree	
Successful search	Unsuccessful search	Successful search	Unsuccessful search
X1	X2	X3	X4

A successful search means that the key exists in the database and unsuccessful means that it is not present in the database. Each of the entries X_1, X_2, X_3 and X_4 can have a value of either Constant or Variable. Constant means that the search time is the same, independent of the specific key value, where variable means that it is dependent on the specific key value chosen for the search.

Give the correct values for the entries X_1, X_2, X_3 and X_4 (for example $X_1 = \text{Constant}, X_2 = \text{Constant}\ , X_3 = \text{Constant}, X_4 = \text{ Constant }$).

b. Relation R(A,B) has the following view defined on it:

```
CREATE VIEW V AS
(SELECT R1.A,R2.B
FROM R AS R1, R as R2
WHERE R1.B=R2.A)
```

i. The current contents of relation R are shown below. What are the contents of the view V?

A	B
1	2
2	3
2	4
4	5
6	7
6	8
9	10

ii. The tuples (2,11) and (11,6) are now inserted into R. What are the *additional* tuples that are inserted in V?

gate2002 databases b-tree normal descriptive

Answer

3.1.9 B Tree: GATE2002-2.23, UGCNET-June2012-II-26 top http://gateoverflow.in/853

A B^+ - tree index is to be built on the *Name* attribute of the relation *STUDENT.* Assume that all the student names are of length 8 bytes, disk blocks are of size 512 bytes, and index pointers are of size 4 bytes. Given the scenario, what would be the best choice of the degree (i.e. number of pointers per node) of the B^+ - tree?

A. 16
B. 42
C. 43
D. 44

gate2002 databases b-tree normal ugcnetjune2012ii

Answer

3.1.10 B Tree: GATE2004-52 top http://gateoverflow.in/1048

The order of an internal node in a B+ tree index is the maximum number of children it can have. Suppose that a child pointer takes 6 bytes, the search field value takes 14 bytes, and the block size is 512 bytes. What is the order of the internal node?

A. 24
B. 25
C. 26
D. 27

gate2004 databases b-tree normal

Answer

3.1.11 B Tree: GATE2004-IT-79 top http://gateoverflow.in/3723

Consider a table T in a relational database with a key field K. A B-tree of order p is used as an access structure on K, where p denotes the maximum number of tree pointers in a B-tree index node. Assume that K is 10 bytes long; disk block size is

512 bytes; each data pointer P_D is 8 bytes long and each block pointer P_B is 5 bytes long. In order for each B-tree node to fit in a single disk block, the maximum value of p is

A. 20
B. 22
C. 23
D. 32

gate2004-it databases b-tree normal

Answer

3.1.12 B Tree: GATE2005-28 top

http://gateoverflow.in/1364

Which of the following is a key factor for preferring B^+-trees to binary search trees for indexing database relations?

A. Database relations have a large number of records

B. Database relations are sorted on the primary key

C. B^+-trees require less memory than binary search trees

D. Data transfer form disks is in blocks

gate2005 databases b-tree normal

Answer

3.1.13 B Tree: GATE2005-IT-23, ISRO2017-67 top

http://gateoverflow.in/3768

A B-Tree used as an index for a large database table has four levels including the root node. If a new key is inserted in this index, then the maximum number of nodes that could be newly created in the process are

A. 5
B. 4
C. 3
D. 2

gate2005-it databases b-tree normal isro2017

Answer

3.1.14 B Tree: GATE2006-IT-61 top

http://gateoverflow.in/3605

In a database file structure, the search key field is 9 bytes long, the block size is 512 bytes, a record pointer is 7 bytes and a block pointer is 6 bytes. The largest possible order of a non-leaf node in a B+ tree implementing this file structure is

A. 23
B. 24
C. 34
D. 44

gate2006-it databases b-tree normal

Answer

3.1.15 B Tree: GATE2007-63, ISRO2016-59 top

http://gateoverflow.in/1261

The order of a leaf node in a B^+ - tree is the maximum number of (value, data record pointer) pairs it can hold. Given that the block size is 1K bytes, data record pointer is 7 bytes long, the value field is 9 bytes long and a block pointer is 6 bytes long, what is the order of the leaf node?

A. 63
B. 64
C. 67
D. 68

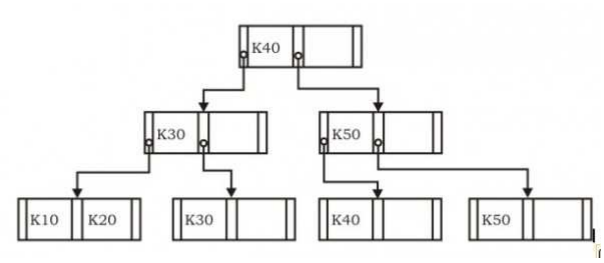
gate2007 databases b-tree normal isro2016

Answer

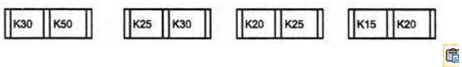
3.1.16 B Tree: GATE2007-IT-84 top

http://gateoverflow.in/3536

Consider the B^+ tree in the adjoining figure, where each node has at most two keys and three links.



Keys K 15 and then K 25 are inserted into this tree in that order. Exactly how many of the following nodes (disregarding the links) will be present in the tree after the two insertions?



A. 1
B. 2
C. 3
D. 4

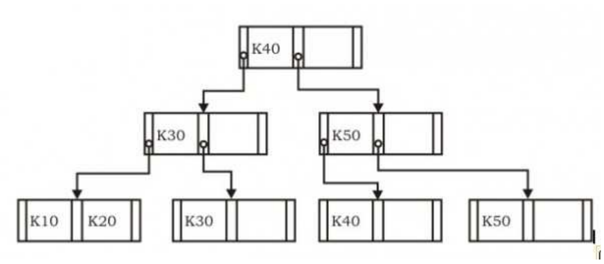
gate2007-it databases b-tree normal

Answer

3.1.17 B Tree: GATE2007-IT-85 top

http://gateoverflow.in/3537

Consider the B^+ tree in the adjoining figure, where each node has at most two keys and three links.



Now the key K 50 is deleted from the B^+ tree resulting after the two insertions made earlier. Consider the following statements about the B^+ tree resulting after this deletion.

i. The height of the tree remains the same.
ii. The node
   k20

   (disregarding the links) is present in the tree.

iii. The root node remains unchanged (disregarding the links)1

Which one of the following options is true ?

A. Statements (i) and (ii) are true
B. Statements (ii) and (iii) are true
C. Statements (iii) and (i) are true
D. All the statements are false

gate2007-it databases b-tree normal

Answer

3.1.18 B Tree: GATE2008-41 top http://gateoverflow.in/453

A B-tree of order 4 is built from scratch by 10 successive insertions. What is the maximum number of node splitting operations that may take place?

A. 3
B. 4
C. 5
D. 6

gate2008 databases b-tree normal

Answer

3.1.19 B Tree: GATE2009-44 top http://gateoverflow.in/1330

The following key values are inserted into a B+ - tree in which order of the internal nodes is 3, and that of the leaf nodes is 2, in the sequence given below. The order of internal nodes is the maximum number of tree pointers in each node, and the order of leaf nodes is the maximum number of data items that can be stored in it. The B+ - tree is initially empty

10, 3, 6, 8, 4, 2, 1

The maximum number of times leaf nodes would get split up as a result of these insertions is

A. 2
B. 3
C. 4
D. 5

gate2009 databases b-tree normal

Answer

3.1.20 B Tree: GATE2010-18 top http://gateoverflow.in/2191

Consider a B^+-tree in which the maximum number of keys in a node is 5. What is the minimum number of keys in any non-root node?

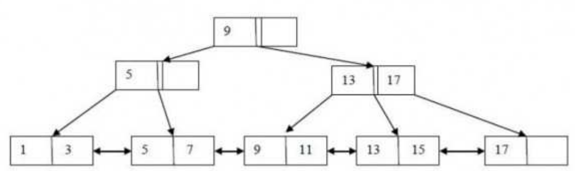
A. 1
B. 2
C. 3
D. 4

gate2010 databases b-tree easy

Answer

3.1.21 B Tree: GATE2015-2_6 top http://gateoverflow.in/8052

With reference to the B+ tree index of order 1 shown below, the minimum number of nodes (including the Root node) that must be fetched in order to satisfy the following query. "Get all records with a search key greater than or equal to 7 and less than 15" is _______.



gate2015-2 databases b-tree normal numerical-answers

Answer

3.1.22 B Tree: GATE2015-3_46 top http://gateoverflow.in/8555

Consider a B+ tree in which the search key is 12 bytes long, block size is 1024 bytes, recorder pointer is 10 bytes long and the block pointer is 8 byte long. The maximum number of keys that can be accommodated in each non-leaf node of the tree is _______.

gate2015-3 databases b-tree normal numerical-answers

Answer

Answers: B Tree

3.1.1 B Tree: GATE 2016-2-21 top http://gateoverflow.in/39569

Selected Answer

A:In B+ Tree all leaves are at same level.

16 votes -- Anurag Semwal (8k points)

3.1.2 B Tree: GATE1989-12a top http://gateoverflow.in/91199

B Tree after inserting 34.

120

34 250

32 81 150,205 520

4 votes -- Mehak Sharma (1.5k points)

3.1.3 B Tree: GATE1994_14 top http://gateoverflow.in/2510

Selected Answer

For n leaves we have n-1 keys in internal node. (see 'part a' of thisquestion)

Total keys in internal nodes = n-1, each node can have keys between d and 2d.

for n-1 keys there will be minimum $\left\lceil \frac{n-1}{2d} \right\rceil$ internal nodes, and

maximum $\left\lceil \frac{n-1}{d} \right\rceil$ internal nodes.

To calculate Big-Omega I am taking maximum everywhere.

if every node contains d+1 pointers (d keys) then height will be maximum, because number of nodes to be accommodated are fixed $\left(\left\lceil \frac{n-1}{d} \right\rceil\right)$.

if height is h then equation becomes

$$1+(d+1)+(d+1)^2+(d+1)^3+\ldots..+(d+1)^{h-1} = \frac{n-1}{d} \implies \frac{(d+1)^h-1}{(d+1)-1} = \frac{n-1}{d} \implies (d+1)^h = n \implies h$$

this is maximum height possible or say maximum number of levels possible.

Now using h traverse we can get to leaf node, and then we may need to traverse 'd' more keys if our desired record is present in rightmost of leaf.

Answer is O(h+d) i.e. $O(log_{(d+1)}n+d) = O(log_d n+d)$

4 votes -- Sachin Mittal (7.1k points)

3.1.4 B Tree: GATE1997_19 top

http://gateoverflow.in/2279

Selected Answer

Let us understand specification of B+ tree first
For a non root node ------>>>>>>
min no of keys =d so min no of children =d+1
max no of keys =2d so max no of children =2d+1
For a root node ---------->>>>>>>>
min no of keys =1 so min no of children =2
max no of keys =2d so max no of children =2d+1
now come 2 our actual question
Part a). For a given no of leaf node (L>=2) what ll b total no of keys in internal nodes. ??
So think there are several ways 2 calculate it
1. assuming max nodes at each level

height	nodes	keys
0	1	2d
1	2d+1	2d (2d +1)
...	....	...
h	(2d +1)^(h)	.2d [(2d +1) ^(h)]

no of leaf nodes= (2d +1)^ (h)=L
Total no of keys in internal nodes= $2d +2d(2d+1)+2d(2d+1)^2 +.........+2d(2d+1)^{h-1}$
$= (2d+1)^h -1=$ **L-1**
2. assuming min nodes at each level

height	nodes	keys
0	1	1
1	2	2d
...	....	...
h	2(d +1)^(h)	.2d [(d +1) ^(h)]

so no of leaf nodes $=2(d+1)^h =L$
Total no of keys in internal nodes $=1+2d+2d(d+1)+....+2d(d+1)^{h-1}$
$=2(d+1)^h -1 =$ **L-1**
3. Whenever there is an overflow in a leaf node(or whenever no of leaf node increases by one) , then we move a key in the internal node(or we can say, no of internal keys increases by one).

Now let's start with the base case. - Only 2 leaf node(as given L>=2).so no of keys in root node =1or L-1.
Once there is an overflow in a single leaf node then no of leaf nodes now would become 3 and at the same the time we will have one more key in our root node.......
part b.) maximum number of internal nodes in a B+ tree of order 4 with 52 leaves. ??
Using Bulk loading approach, here we ll use minimum fill factor(d=4 hence min keys =d =4 and min children/block pointer =d+1=5)
so we have 52 leaves so so we need total 52 block pointer and one node can have min 5 block pointer
so for 52 leaves we require floor(52/5) = 10 nodes
for 11 block pointer we req. floor(10/5) = 2 nodes
for 2 block pointer we require 1 node "it is root node"
so max no of internal nodes=10+2+1= 13 nodes
part c) minimum number of leaves in a B+ tree of order d and height h(h≥1) ??
by part a " assuming min nodes at each level" case
min no of leaves = $\mathbf{2 (d +1)^{h-1}}$

4 votes -- saurabh rai (10.9k points)

3.1.5 B Tree: GATE1999_1.25 top

http://gateoverflow.in/1478

Selected Answer

A) False. Both r stored in disk

B) True. By searching leaf level linearly in B+ tree, we can say a node is present or not in B+ tree. But for B tree we have to traverse the whole tree

C)False. B tree and B+ tree uses dynamic multilevel indexes http://home.iitj.ac.in/~ramana/ch10-storage-2.pdf

D)False. Height depends on number of record and also max no of keys in each node (order of tree)

12 votes -- srestha (58.4k points)

3.1.6 B Tree: GATE1999_21 top http://gateoverflow.in/1520

Selected Answer

Given a B tree :

max children at a node : 2m - 1 => max keys : 2m -2

min children at a node : m => min keys : m -1

At Root node : min keys : 1 min children : 2

Here , leaf level is at level h (becz root is at level 0)

Now, we have to find

1) Minimum keys at leaf level(complete bottommost level , not just a node) -

For this we have to consider minimum everywhere.

Firstly we will count minimum possible nodes at leaf level.

At Root Node (level 0) : It can have minimum 2 child (mean 2 nodes minimum for next level)

At level 1 : It has 2 nodes , each can have minimum m child (so , this gives 2 * m minimum possible nodes at next level)

At level 2 : min $2 * m^2$ Child and so on.

At level (h-1) : $2 * (m)^{h-1}$ child (these are min number of leaf nodes possible)

At level h(leaf level) : $2 * (m)^{h-1}$ nodes each having minimum (m-1) keys.

So, this gives the answer as $\mathbf{2 * (m)^{h-1} * (m-1)}$ minimum keys possible at leaf level.

---

2) Maximum keys at leaf level(complete bottommost level , not just a node) -

For this we have to count max everywhere.

At root (level 0) : max child possible 2m-1 (nodes for next level)

At level 1 : 2m-1 nodes give $(2m-1)^2$ child

At level (h-1) : $(2m-1)^h$ child (these are maximum possible nodes at leaf level)

At level h (leaf level) : $(2m-1)^h$ nodes each having a maximum of (2m-2) keys ,

Giving a total of - $\mathbf{(2m-1)^h * (2m-2)}$ maximum keys at leaf level.

17 votes -- Himanshu Agarwal (16.2k points)

3.1.7 B Tree: GATE2000-1.22, UGCNET-June2012-II-11 top http://gateoverflow.in/646

Selected Answer

Answer is B. The major advantage of B+ tree is in reducing the number of last level access which would be from disk in case of large data size.

http://stackoverflow.com/questions/15485220/advantage-of-b-trees-over-bsts

11 votes -- Arjun Suresh (294k points)

3.1.8 B Tree: GATE2002-17 top http://gateoverflow.in/870

Selected Answer

For A)

X1 = Variable (Key can be found @ Internal nodes at various levels)
X2 = Constant
X3 = Variable, We need to just check where key is present/absent, not to access Data. (A successful search means that the key exists in the database and unsuccessful means that it is not present in the database.) So Variable
X4 = Constant

For Part B) i) Write down two copies of the same table for comparison side by side. Just map B of first to A of the second copy. Those matching tuples take A of first table & B of seconds.

Content of View A

A	B
1	3
1	4
2	5

For Part B) ii)

Additional tuples getting inserted ->

A	B
11	7
11	8
2	6
1	11

7 votes -- Akash (43.8k points)

3.1.9 B Tree: GATE2002-2.23, UGCNET-June2012-II-26 top http://gateoverflow.in/853

Selected Answer

Answer: C
In a B^+ tree we want en entire node content to be in a disk block. A node can contain up to$p$ pointers to child nodes and up to $p-1$ key values for a B^+ tree of order p. Here, key size is 8 bytes and pointer size is 4 bytes. Thus we can write

$8(p-1)+4p \leq 512 \implies 12p \leq 520 \implies p = 43.$

http://www.cburch.com/cs/340/reading/btree/index.html

22 votes -- Rajarshi Sarkar (35k points)

3.1.10 B Tree: GATE2004-52 top http://gateoverflow.in/1048

Selected Answer

Answer: C

14(p-1) + 6p <= 512
20p - 14 <= 512
20p <= 526
Therefore, p = 26.

15 votes -- Rajarshi Sarkar (35k points)

3.1.11 B Tree: GATE2004-IT-79 top http://gateoverflow.in/3723

Selected Answer

It's 23

(p-1)(key_ptr_size + record_ptr_size) + p. (block_ptr_size) <= 512

we get , p=23

22 votes -- Sandeep_Uniyal (7.3k points)

3.1.12 B Tree: GATE2005-28 top http://gateoverflow.in/1364

Selected Answer

Answer: D

A: Cannot compare both the trees solely on basis of this.
B: Both trees are BST.
C: False. High fanout in B+ ensures that it takes more memory than BST.
D: True. Records are stored in disk blocks.

13 votes -- Rajarshi Sarkar (35k points)

3.1.13 B Tree: GATE2005-IT-23, ISRO2017-67 top http://gateoverflow.in/3768

Selected Answer

suppose all nodes are completely full means every node has n-1 keys. tree has 4 levels if a new key is inserted then at every level there will be created a new node. and in worst case root node will also be broken into two parts. and we have 4 levels so answer should be 5 because tree will be increased with one more level

24 votes -- Manu Thakur (6k points)

3.1.14 B Tree: GATE2006-IT-61 top http://gateoverflow.in/3605

Selected Answer

ans is (C)

from the structure of B+ tree we can get this equation:

n*p + (n-1)*(k) <= B (for non leaf node)

here, n=order, p=tree/block/index pointer, B=size of block i non leaf node no record pointer is there in B+ tree.

so n*p + (n-1)k <= B

n*6 + (n-1)*9 <= 512

n <= 34.77

largest possible is 34

16 votes -- jayendra (8.1k points)

3.1.15 B Tree: GATE2007-63, ISRO2016-59 top http://gateoverflow.in/1261

Selected Answer

The answer = **option A**

B_p + P(R_p + Key) $\leq$ BlockSize

$1 \times 6 + n(7+9) \leq 1024$

$n \leq 63.625$.

so 63 is the answer

29 votes -- Gate Keeda (19.1k points)

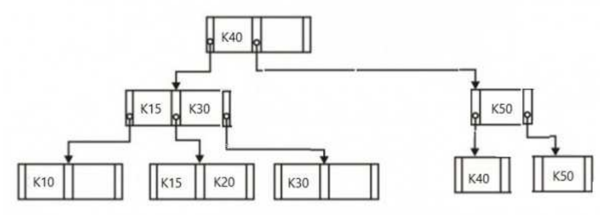
3.1.16 B Tree: GATE2007-IT-84 top http://gateoverflow.in/3536

Selected Answer

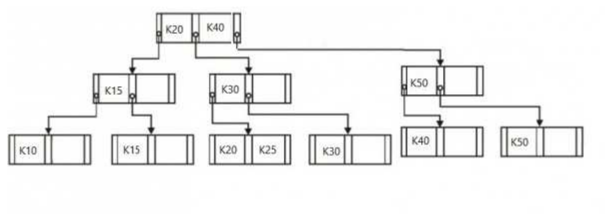
Option A is correct.

It is a B^+ Tree.

After inserting K15 we get -



Now, we insert K25 , which gives -



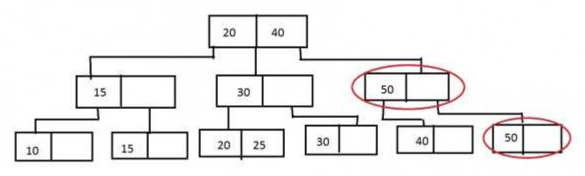
so, we see in the final tree only (K20,K25) is present. Hence, **1 (Ans).**

19 votes -- Himanshu Agarwal (16.2k points)

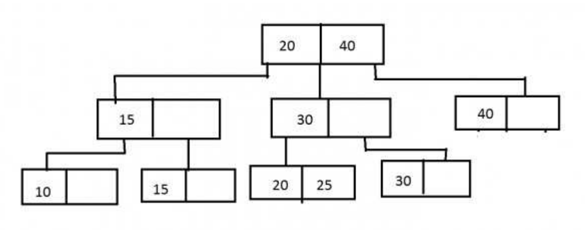
3.1.17 B Tree: GATE2007-IT-85 top

http://gateoverflow.in/3537

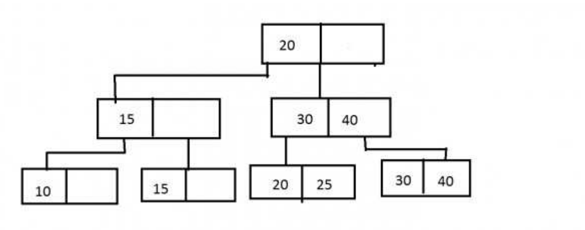
Selected Answer



Now merge 40 in upper level



Now redistribute



So ans is 1)

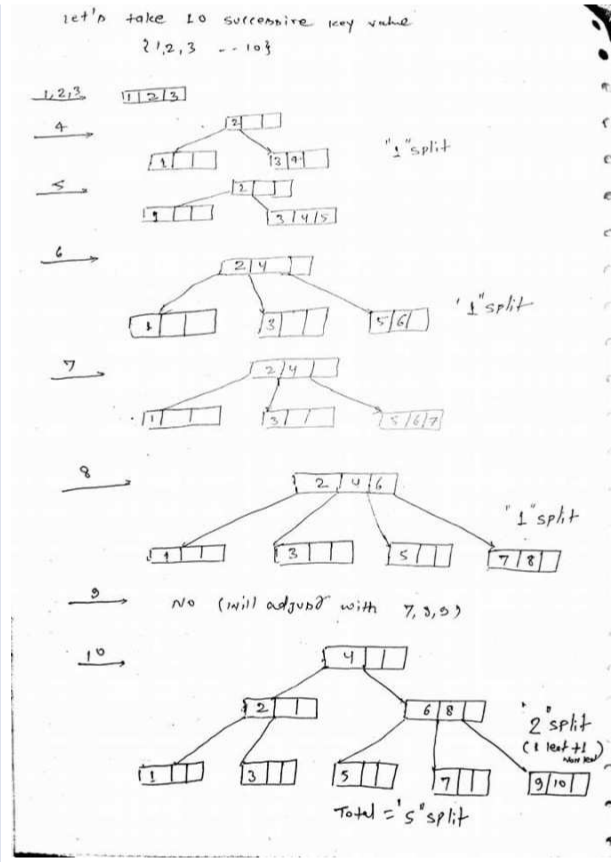
15 votes -- srestha (58.4k points)

3.1.18 B Tree: GATE2008-41 top

http://gateoverflow.in/453

Selected Answer

Total 5 splitting will occur while 10 successive insertion



11 votes -- Prateek kumar (6k points)

Let 1 to 10 be inserted

Insertion of 123 does not cause any split

When we insert 4 split occurs

We use right bias

2

1 3456

Again on insertion of 6 split occurs

2 4

1 3 56

7 does not cause split

2 4

1 3 5678

8 cause split

2 4 6

1 3 5 7 8

Inserting 9 wont cause any split

2 4 6

1 3 5 7 8 9

Inserting 10 causes split at leaf and non leaf node

4

2 6 8

1 3 5 7 9 10

So total 5 splits

12 votes -- Pooja Palod (32.4k points)

3.1.19 B Tree: GATE2009-44 top http://gateoverflow.in/1330

Selected Answer

In this question they have asked only to count leaf node splits.

So after discussing with my friends on fb, I found that you will get two different answers depending on which convention you follow.

Convention 1: put the middle element in the left node, if you follow this you will get 4 as answer.

Convention 2: put the middle element in the right node, if you follow this you will get 3 as answer.

4 splits

1. after inserting 6
2. after inserting 4
3. after inserting 2 (there will be an internal node split and a leaf node split)
4. after inserting 1

20 votes -- Vikrant Singh (13.4k points)

3.1.20 B Tree: GATE2010-18 top http://gateoverflow.in/2191

Selected Answer

Answer: B

Order = 5+1 = 6

Minimum children in a non root node = $\lceil \frac{Order}{2} \rceil = \lceil \frac{6}{2} \rceil = 3$

Keys = Minimum children in a non root node - 1 = 2

20 votes -- Rajarshi Sarkar (35k points)

In a b+ tree if a non-root node can be a leaf-node or a non-leaf-node:

case 1) when a non-root, leaf node is full and a new key is inserted in it:

a) the initial keys in the row + the newly inserted key is arranged in asc/desc order

b) the medium key is copied to an upward node without the record pointer

c) the medium key is retained in the leaf node with the record pointer

d) the keys in the leaf node are split in half and moved to two separate nodes

here there are maximum 5 keys, so when an additional key comes, the medium key is copied upwards, and a total of 6 keys are split in two nodes having 3 keys each.

case 2) when a non-root, non-leaf node is full and a new key is inserted in it:

a) the initial keys in the row + the newly inserted key is arranged in asc/desc order

b) the medium key is moved to an upward node

c) the medium key is removed from the current node

d) the keys in the current node are split in half and moved to two separate nodes

here there are maximum 5 keys, so when an additional key comes, the medium key is moved upwards, and a total of 5 remaining keys are split in two nodes having 2 keys and 3 keys respectively.

SO the minimum number of keys in a non-root leaf node is 3 and the minimum number of keys in a non-root non-leaf node is 2.

SO the minimum number of keys in a non-root node is 2.

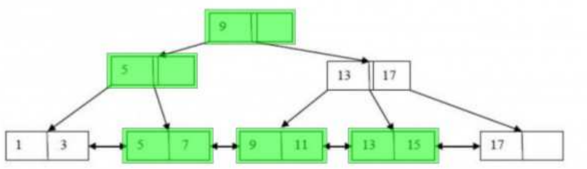
Hence answer is (B)

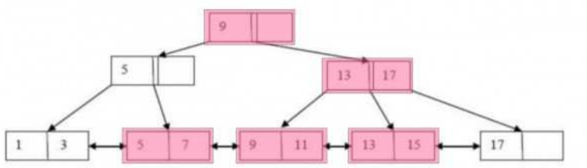
12 votes -- Danish (3.6k points)

3.1.21 B Tree: GATE2015-2_6 top http://gateoverflow.in/8052

Selected Answer

whichever way you go from the root to leaves, you'll always end up counting 5 nodes.





18 votes -- Amar Vashishth (28.7k points)

3.1.22 B Tree: GATE2015-3_46 top http://gateoverflow.in/8555

Selected Answer

(n-1)12 + n*8<=1024

n<=51

in non leaf node number of keys = n-1

=51-1=50

20 votes -- ppm (627 points)

3.2 Candidate Keys(5) top

3.2.1 Candidate Keys: GATE1994_3.7 top http://gateoverflow.in/2493

An instance of a relational scheme $R(A, B, C)$ has distinct values for attribute A. Can you conclude that A is a candidate key for R?

gate1994 databases easy candidate-keys

Answer

3.2.2 Candidate Keys: GATE2011-12 top

http://gateoverflow.in/2114

Consider a relational table with a single record for each registered student with the following attributes:

1. Registration_Num: Unique registration number for each registered student
2. UID: Unique identity number, unique at the national level for each citizen
3. BankAccount_Num: Unique account number at the bank. A student can have multiple accounts or joint accounts. This attribute stores the primary account number.
4. Name: Name of the student
5. Hostel_Room: Room number of the hostel

Which of the following options is **INCORRECT**?

(A) BankAccount_Num is a candidate key

(B) Registration_Num can be a primary key

(C) UID is a candidate key if all students are from the same country

(D) If S is a super key such that $S \cap \text{UID}$ is NULL then $S \cup \text{UID}$ is also a superkey

gate2011 databases normal candidate-keys

Answer

3.2.3 Candidate Keys: GATE2014-2-21 top

http://gateoverflow.in/1978

The maximum number of superkeys for the relation schema $R(E, F, G, H)$ with E as the key is _____.

gate2014-2 databases numerical-answers easy candidate-keys

Answer

3.2.4 Candidate Keys: GATE2014-2-22 top

http://gateoverflow.in/1980

Given an instance of the STUDENTS relation as shown as below

StudentID	StudentName	StudentEmail	StudentAge	CPI
2345	Shankar	Shankar@math	X	9.4
1287	Swati	swati@ee	19	9.5
7853	Shankar	Shankar@cse	19	9.4
9876	Swati	swati@mech	18	9.3
8765	Ganesh	ganesh@civil	19	8.7

For $(StudentName, StudentAge)$ to be a key for this instance, the value X should NOT be equal to______.

gate2014-2 databases numerical-answers easy candidate-keys

Answer

3.2.5 Candidate Keys: GATE2014-3-22 top

http://gateoverflow.in/2056

A *prime attribute* of a relation scheme R is an attribute that appears

A. in all candidate keys of R
B. in some candidate key of R
C. in a foreign key of R
D. only in the primary key of R

gate2014-3 databases easy candidate-keys

Answer

Answers: Candidate Keys

3.2.1 Candidate Keys: GATE1994_3.7 top http://gateoverflow.in/2493

Selected Answer

No.

A	B	C
1	5	6
2	4	7
3	4	5

Suppose this is the relational instance at any point of time.

Now we may see that A->BC holds for this instance ,hence A^+={ABC}.

But FD s are defined on the schema itself not the instance, so based on the state of the instance we cannot say what holds for schema (there can be a many instances for R).

16 votes -- Sourav Roy (3.6k points)

3.2.2 Candidate Keys: GATE2011-12 top http://gateoverflow.in/2114

Selected Answer

A relation is given **(Registration_Num, UID, BankAccount_Num, Name, Hostel_Room)**.

Now, **Registration_Num** is unique for each student. So with this, we can identify each student. Hence, this can be the primary key.

UID: It's an identification number for a person in a country. (Say you're in India and your **UID** is 0243. Someone in Pakistan may also have the same **UID** as 0243). So, if all students are from India (that is, the same country) then their **UID** will be different and then **UID** will be a Candidate key.

If **S** is a super key then **S** ∪ **UID** will be a Super key. e.g. **R(A, B, C, D)**, If **AB** is a superkey then **ABC**, **ABCD** are also superkey.

BankAccount_Num is not a candidate key, because a student can have multiple accounts or joint accounts. We can not identify each student uniquely with **BankAccount_Num**.

19 votes -- Pranay Datta (9.7k points)

3.2.3 Candidate Keys: GATE2014-2-21 top http://gateoverflow.in/1978

Selected Answer

Super Key is any set of attributes that uniquely determines a tuple in a relation.

Since E is **the only key**, E should be present in any super key.

Excluding E, there are three attributes in the relation, namely F, G, H. Hence, if we add E to any subset of those three attributes, then the resulting set is a super key. Number of subsets of $\{F, G, H\}$ is 8. **Hence the answer is** 8**.**

The following are Super Keys:

$$\left\{\begin{matrix} E \\ EF \\ EG \\ EH \\ EFG \\ EFH \\ EGH \\ EFGH \end{matrix}\right\}$$

👍 18 votes -- Sankaranarayanan P.N (11.2k points)

3.2.4 Candidate Keys: GATE2014-2-22 top http://gateoverflow.in/1980

Selected Answer

should not eqaul to 19.

Since if it is equal the same key will have two different values which cannot be true by the definition of candidate/primary/super key.

👍 16 votes -- Aravind (3.3k points)

3.2.5 Candidate Keys: GATE2014-3-22 top http://gateoverflow.in/2056

Selected Answer

prime attribute is a constituent of a candidate key. it need not present in all candidate keys. hence option B is correct

correct me if i went wrong

👍 17 votes -- Sankaranarayanan P.N (11.2k points)

3.3 Concurrency(1) top

3.3.1 Concurrency: GATE 2016-2-51 top http://gateoverflow.in/39590

Consider the following database schedule with two transactions T_1 and T_2.

$$S = r_2(X); r_1(X); r_2(Y); w_1(X); r_1(Y); w_2(X); a_1; a_2$$

Where $r_i(Z)$ denotes a read operation by transaction T_i on a variable Z, $w_i(Z)$ denotes a write operation by T_i on a variable Z and a_i denotes an abort by transaction T_i.

Which one of the following statements about the above schedule is **TRUE**?

A. S is non-recoverable.
B. S is recoverable, but has a cascading abort.
C. S does not have a cascading abort.
D. S is strict.

gate2016-2 databases concurrency transactions normal

Answer

Answers: Concurrency

3.3.1 Concurrency: GATE 2016-2-51 top http://gateoverflow.in/39590

Selected Answer

Answer is C

T_1	T_2
	R(x)
R(x)	
	R(y)
W(x)	

R(y)	
	W(x)
a_1	
	a_2

(A) => This is not possible, because we have no dirty read ! No dirty read => Recoverable

(B) => This is not possible, because of no Dirty read ! No dirty read => No cascading aborts !

(D) => This is not true, because we can see clearly in image that after W1(X) before T1 commit or aborts T2 does W2(x) !

C is only option remaining !

17 votes -- Akash (43.8k points)

3.4 Conflict Serializable(1) top

3.4.1 Conflict Serializable: GATE2017-2-44 top

http://gateoverflow.in/118640

Two transactions T_1 and T_2 are given as

$T_1 : r_1(X)w_1(X)r_1(Y)w_1(Y)$

$T_2 : r_2(Y)w_2(Y)r_2(Z)w_2(Z)$

where $r_i(V)$ denotes a $read$ operation by transaction T_i on a variable V and $w_i(V)$ denotes a $write$ operation by transaction T_i on a variable V. The total number of conflict serializable schedules that can be formed by T_1 and T_2 is ______

gate2017-2 databases transactions numerical-answers conflict-serializable

Answer

Answers: Conflict Serializable

3.4.1 Conflict Serializable: GATE2017-2-44 top

http://gateoverflow.in/118640

Selected Answer

T1 : R1(A) W(A) R1(B) W1(B)
1 2 3 4
↙

T2 : R2(B) W2(B) R2(C) W2(C)
5 6 7 8

Conflict condition RW WR WW

There are total 5 conflict operation

1. T(1) & T(2) operations should execute in given ordered sequence
1-2-3-4 and 5-6-7-8

2.NO operation should come between any two conflict schedule operation e.g. between 5 and 6 no other operation can come otherwise it will violate the condition.

Let us count how many combination can be made from given condition-:

1) Execute all T(1) first then T(2)
i.e. 1-2-3-4-5-6-7-8 ----------------- 1 way

2)Since there is conflict between 3 and 6 so we can say that 6 should execute before 3 to avoid violation.
6<3
To count this first let us count how many total concurrent process can be possible .

__5__6__7__8__

so we have 5 empty space out which we have to fill with 4 operation (1,2,3,4) with repetition.
At each empty space any number of operation can come.
It is similar problem to chocolate problem.

Total Number of concurrent process = (5+4-1)C4 = 70
(n=5(empty space) r=4(total operation) therefore (n+r-1Cr))

But this also include in which our condition are violating. 6

1) 1 2 3 4 occur before 6
here n= 2 r =4
therefore (2+4-1)C4 = 5

2) 1 2 3 occur before 6
here n= 2 r= 3
therefore (2+3-1)C3 = 4 but here d can be at 3 place so total 4 *3 = 12 arrangement

so total 12 +5 = 17 arrangement are violating our condition out 0f 70 concurrent arrangement
So total arrangement = 70 -17 = 53

So total arrangement = serial arrangement + concurrent arrangement
= 53 + 1 = 54

11 votes -- Umang Raman (15.2k points)

3.5 Data Independence(1) top

3.5.1 Data Independence: GATE1994-3.11 top http://gateoverflow.in/2497

State True or False with reason

Logical data independence is easier to achieve than physical data independence

gate1994 databases normal data-independence

Answer

Answers: Data Independence

3.5.1 Data Independence: GATE1994-3.11 top http://gateoverflow.in/2497

Selected Answer

This is False.

Generally, physical data independence exists in most databases and file environments where physical details such as the exact location of data on disk, and hardware details of storage encoding, placement, compression, splitting, merging of
records, and so on are hidden from the user. Applications remain unaware of these
details. On the other hand, logical data independence is harder to achieve because it
allows structural and constraint changes without affecting application programs—a
much stricter requirement. This paragraph is taken from Navathe book of DBMS, Page no 36, Chapter 2.

12 votes -- Akash (43.8k points)

3.6 Database Normalization(27) top

3.6.1 Database Normalization: GATE 2016-1-21 top http://gateoverflow.in/39637

Which of the following is NOT a superkey in a relational schema with attributes V, W, X, Y, Z and primary key $V\ Y$?

A. $VXYZ$
B. $VWXZ$
C. $VWXY$
D. $VWXYZ$

gate2016-1 databases database-normalization easy

Answer

3.6.2 Database Normalization: GATE 2016-1-23 top http://gateoverflow.in/39646

A database of research articles in a journal uses the following schema.

$$(\text{VOLUME}, \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE}, \text{TITLE}, \text{YEAR}, \text{PRICE})$$

The primary key is '$(\text{VOLUME}, \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE})$

and the following functional dependencies exist in the schema.

$$\begin{array}{cl} (\text{VOLUME}\ , \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE}) & \rightarrow \text{TITLE} \\ (\text{VOLUME}, \text{NUMBER}) & \rightarrow\ \text{YEAR} \\ (\text{VOLUME}, \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE}) & \rightarrow \text{PRICE} \end{array}$$

The database is redesigned to use the following schemas

$$(\text{VOLUME}, \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE}, \text{TITLE}, \text{PRICE})(\text{VOLUME}, \text{NUMBER}, \text{YEAR})$$

Which is the weakest normal form that the new database satisfies, but the old one does not?

A. 1NF
B. 2NF
C. 3NF
D. BCNF

gate2016-1 databases database-normalization normal

Answer

3.6.3 Database Normalization: GATE1994_3.6 top http://gateoverflow.in/2492

State True or False with reason

There is always a decomposition into Boyce-Codd normal form (BCNF) that is lossless and dependency preserving.

gate1994 databases database-normalization easy

Answer

3.6.4 Database Normalization: GATE1995_26 top http://gateoverflow.in/2665

Consider the relation scheme R(A, B, C) with the following functional dependencies:

- A, B → C,
- C → A

a. Show that the scheme R is in 3NF but not in BCNF.
b. Determine the minimal keys of relation R.

gate1995 databases database-normalization normal

Answer

3.6.5 Database Normalization: GATE1997_6.9 top http://gateoverflow.in/2265

For a database relation $R(a,b,c,d)$, where the domains a,b,c,d include only atomic values, only the following functional dependencies and those that can be inferred from them hold

- $a \rightarrow c$
- $b \rightarrow d$

This relation is

A. in first normal form but not in second normal form

B. in second normal form but not in first normal form

C. in third normal form

D. none of the above

gate1997 databases database-normalization normal

Answer

3.6.6 Database Normalization: GATE1998_1.34 top http://gateoverflow.in/1671

Which normal form is considered adequate for normal relational database design?

A. 2 NF
B. 5 NF
C. 4 NF
D. 3 NF

gate1998 databases database-normalization easy

Answer

3.6.7 Database Normalization: GATE1998_26 top http://gateoverflow.in/1741

Consider the following database relations containing the attributes

- Book_id
- Subject_Category_of_book
- Name_of_Author
- Nationality_of_Author

With Book_id as the primary key.

a. What is the highest normal form satisfied by this relation?

b. Suppose the attributes Book_title and Author_address are added to the relation, and the primary key is changed to {Name_of_Author, Book_title}, what will be the highest normal form satisfied by the relation?

gate1998 databases database-normalization normal

Answer

3.6.8 Database Normalization: GATE1999-2.7, UGCNET-June2014-III-25 top

Consider the schema $R = (S, T, U, V)$ and the dependencies $S \to T, T \to U, U \to V$ and $V \to S$. Let $R = (R1 \text{ and } R2)$ be a decomposition such that $R1 \cap R2 \neq \phi$. The decomposition is

A. not in 2NF
B. in 2NF but not 3NF
C. in 3NF but not in 2 NF
D. in both 2NF and 3NF

gate1999 databases database-normalization normal ugcnetjune2014iii

Answer

3.6.9 Database Normalization: GATE1999_1.24 top http://gateoverflow.in/1477

Let $R = (A, B, C, D, E, F)$ be a relation scheme with the following dependencies $C \to F, E \to A, EC \to D, A \to B$. Which one of the following is a key for R?

A. CD
B. EC
C. AE
D. AC

gate1999 databases database-normalization easy

Answer

3.6.10 Database Normalization: GATE2001-1.23, UGCNET-June2012-III-18 top

Consider a schema $R(A, B, C, D)$ and functional dependencies $A \rightarrow B$ and $C \rightarrow D$. Then the decomposition of R into $R_1(A, B)$ and $R_2(C, D)$ is

A. dependency preserving and lossless join
B. lossless join but not dependency preserving
C. dependency preserving but not lossless join
D. not dependency preserving and not lossless join

gate2001 databases database-normalization normal ugcnetjune2012iii

Answer

3.6.11 Database Normalization: GATE2001-2.23 top

http://gateoverflow.in/741

R(A,B,C,D) is a relation. Which of the following does not have a lossless join, dependency preserving BCNF decomposition?

A. $A \rightarrow B, B \rightarrow CD$
B. $A \rightarrow B, B \rightarrow C, C \rightarrow D$
C. $AB \rightarrow C, C \rightarrow AD$
D. $A \rightarrow BCD$

gate2001 databases database-normalization normal

Answer

3.6.12 Database Normalization: GATE2002-16 top

http://gateoverflow.in/869

For relation **R=(L, M, N, O, P),** the following dependencies hold:

$M \rightarrow O$, $NO \rightarrow P$, $P \rightarrow L$ and $L \rightarrow MN$

R is decomposed into **R_1 = (L, M, N, P)** and **R_2 = (M, O)**.

a. Is the above decomposition a lossless-join decomposition? Explain.
b. Is the above decomposition dependency-preserving? If not, list all the dependencies that are not preserved.
c. What is the highest normal form satisfied by the above decomposition?

gate2002 databases database-normalization normal descriptive

Answer

3.6.13 Database Normalization: GATE2002-2.24 top

http://gateoverflow.in/854

Relation R is decomposed using a set of functional dependencies, F, and relation S is decomposed using another set of functional dependencies, G. One decomposition is definitely BCNF, the other is definitely 3NF, but it is not known which is which. To make a guaranteed identification, which one of the following tests should be used on the decompositions? (Assume that the closures of F and G are available).

A. Dependency-preservation
B. Lossless-join
C. BCNF definition
D. 3NF definition

gate2002 databases database-normalization easy

Answer

3.6.14 Database Normalization: GATE2003-85 top http://gateoverflow.in/968

Consider the following functional dependencies in a database.

Date_of_Birth -> Age	Age -> Eligibility
Name -> Roll_number	Roll_number -> Name
Course_number -> Course_name	Course_number -> Instructor
(Roll_number, Course_number) -> Grade	

The relation (Roll_number, Name, Date_of_birth, Age) is

A. in second normal form but not in third normal form

B. in third normal form but not in BCNF

C. in BCNF

D. in none of the above

gate2003 databases database-normalization normal

Answer

3.6.15 Database Normalization: GATE2004-50 top http://gateoverflow.in/1046

The relation scheme $\text{Student Performance (name, courseNo, rollNo, grade)}$ has the following functional dependencies:

- name, courseNo, $\rightarrow$ grade
- rollNo, courseNo $\rightarrow$ grade
- name $\rightarrow$ rollNo
- rollNo $\rightarrow$ name

The highest normal form of this relation scheme is

A. 2 NF
B. 3 NF
C. BCNF
D. 4 NF

gate2004 databases database-normalization normal

Answer

3.6.16 Database Normalization: GATE2004-IT-75 top http://gateoverflow.in/3719

A relation Empdtl is defined with attributes empcode (unique), name, street, city, state and pincode. For any pincode, there is only one city and state. Also, for any given street, city and state, there is just one pincode. In normalization terms, Empdtl is a relation in

A. 1NF only
B. 2NF and hence also in 1NF
C. 3NF and hence also in 2NF and 1NF
D. BCNF and hence also in 3NF, 2NF an 1NF

gate2004-it databases database-normalization normal

Answer

3.6.17 Database Normalization: GATE2005-29, UGCNET-June2015-III-9 http://gateoverflow.in/1365 top

Which one of the following statements about normal forms is FALSE?

A. BCNF is stricter than 3NF

B. Lossless, dependency-preserving decomposition into 3NF is always possible

C. Lossless, dependency-preserving decomposition into BCNF is always possible

D. Any relation with two attributes is in BCNF

gate2005 databases database-normalization easy ugcnetjune2015iii

Answer

3.6.18 Database Normalization: GATE2005-78 top http://gateoverflow.in/1401

Consider a relation scheme R = (A, B, C, D, E, H) on which the following functional dependencies hold: {A$\longrightarrow$ B, BC $\longrightarrow$ D, E $\longrightarrow$ C, D $\longrightarrow$ A}. What are the candidate keys R?

A. AE, BE
B. AE, BE, DE
C. AEH, BEH, BCH
D. AEH, BEH, DEH

gate2005 databases database-normalization easy

Answer

3.6.19 Database Normalization: GATE2005-IT-22 top http://gateoverflow.in/3767

A table has fields Fl, F2, F3, F4, F5 with the following functional dependencies
F1 → F3   F2→ F4   (F1 . F2) → F5
In terms of Normalization, this table is in

A. 1 NF
B. 2 NF
C. 3 NF
D. None of these

gate2005-it databases database-normalization easy

Answer

3.6.20 Database Normalization: GATE2007-62, UGCNET-June2014-II-47 http://gateoverflow.in/1260 top

Which one of the following statements is **FALSE?**

A. Any relation with two attributes is in BCNF

B. A relation in which every key has only one attribute is in 2NF

C. A prime attribute can be transitively dependent on a key in a 3 NF relation

D. A prime attribute can be transitively dependent on a key in a BCNF relation

gate2007 databases database-normalization normal ugcnetjune2014ii

Answer

3.6.21 Database Normalization: GATE2008-69 top http://gateoverflow.in/492

Consider the following relational schemes for a library database:

```
Book (Title, Author, Catalog_no, Publisher, Year, Price)
Collection(Title, Author, Catalog_no)
```

with the following functional dependencies:

I. $\text{Title Author} \rightarrow \text{Catalog\_no}$
II. $\text{Catalog\_no} \rightarrow \text{Title Author Publisher Year}$
III. $\text{Publisher Title Year} \rightarrow \text{Price}$

Assume $\{\text{Author, Title}\}$ is the key for both schemes. Which of the following statements is true?

A. Both Book and Collection are in BCNF
B. Both Book and Collection are in 3NF only
C. Book is in 2NF and Collection in 3NF
D. Both Book and Collection are in 2NF only

gate2008 databases database-normalization normal

Answer

3.6.22 Database Normalization: GATE2008-IT-61 top

http://gateoverflow.in/3371

Let R (A, B, C, D) be a relational schema with the following functional dependencies :
A → B, B → C, C → D and D → B. The decomposition of R into (A, B), (B, C), (B, D)

A. gives a lossless join, and is dependency preserving
B. gives a lossless join, but is not dependency preserving
C. does not give a lossless join, but is dependency preserving
D. does not give a lossless join and is not dependency preserving

gate2008-it databases database-normalization normal

Answer

3.6.23 Database Normalization: GATE2008-IT-62 top

http://gateoverflow.in/3372

Let R (A, B, C, D, E, P, G) be a relational schema in which the following functional dependencies are known to hold: AB → CD, DE → P, C → E, P → C and B → G. The relational schema R is

A. in BCNF
B. in 3NF, but not in BCNF
C. in 2NF, but not in 3NF
D. not in 2NF

gate2008-it databases database-normalization normal

Answer

3.6.24 Database Normalization: GATE2009-55 top

http://gateoverflow.in/1339

Consider the following relational schema:

$\text{Suppliers}(\underline{\text{sid:integer}}, \text{sname:string, city:string, street:string})$

$\text{Parts}(\underline{\text{pid:integer}}, \text{pname:string, color:string})$

$\text{Catalog}(\underline{\text{sid:integer, pid:integer}}, \text{cost:real})$

Consider the following relational query on the above database:

```
SELECT S.sname
FROM    Suppliers S
WHERE S.sid NOT IN (SELECT C.sid
                    FROM Catalog C
                    WHERE C.pid NOT IN (SELECT P.pid
                                        FROM Parts P
                                        WHERE P.color<>'blue'))
```

Assume that relations corresponding to the above schema are not empty. Which one of the following is the correct interpretation of the above query?

A. Find the names of all suppliers who have supplied a non-blue part.

B. Find the names of all suppliers who have not supplied a non-blue part.

C. Find the names of all suppliers who have supplied only non-blue part.

D. Find the names of all suppliers who have not supplied only blue parts.

gate2009 databases sql database-normalization normal

Answer

3.6.25 Database Normalization: GATE2009-56 top http://gateoverflow.in/43474

Consider the following relational schema:

$\text{Suppliers}(\underline{\text{sid:integer}}, \text{ sname:string, city:string, street:string})$

$\text{Parts}(\underline{\text{pid:integer}}, \text{ pname:string, color:string})$

$\text{Catalog}(\underline{\text{sid:integer, pid:integer}}, \text{cost:real})$

Assume that, in the suppliers relation above, each supplier and each street within a city has unique name, and (sname, city) forms a candidate key. No other functional dependencies are implied other than those implied by primary and candidate keys. Which one of the following is TRUE about the above schema?

A. The schema is in BCNF
B. The schema is in 3NF but not in BCNF
C. The schema is in 2 NF but not in 3NF
D. The schema is not in 2NF

gate2009 databases sql database-normalization normal

Answer

3.6.26 Database Normalization: GATE2012-2 top http://gateoverflow.in/34

Which of the following is **TRUE**?

A. Every relation in 3NF is also in BCNF
B. A relation R is in 3NF if every non-prime attribute of R is fully functionally dependent on every key of R
C. Every relation in BCNF is also in 3NF
D. No relation can be in both BCNF and 3NF

gate2012 databases easy database-normalization

Answer

3.6.27 Database Normalization: GATE2014-1-30 top http://gateoverflow.in/1797

Given the following two statements:

S1: Every table with two single-valued attributes is in 1NF, 2NF, 3NF and BCNF.

S2: $AB \to C$. $D \to E$, $E \to C$ is a minimal cover for the set of functional dependencies $AB \to C$, $D \to E$, $AB \to E$, $E \to C$.

Which one of the following is **CORRECT**?

A. S1 is TRUE and S2 is FALSE.
B. Both S1 and S2 are TRUE.
C. S1 is FALSE and S2 is TRUE.
D. Both S1 and S2 are FALSE.

gate2014-1 databases database-normalization normal

Answer

Answers: Database Normalization

3.6.1 Database Normalization: GATE 2016-1-21 top

http://gateoverflow.in/39637

Selected Answer

Any superset of a key is also a superkey from definition of a superkey.
So Answer B.

> a superkey can be defined as a set of attributes of a relation schema upon which all attributes of the schema are functionally dependent

21 votes -- Abhilash Panicker (8.8k points)

3.6.2 Database Normalization: GATE 2016-1-23 top

http://gateoverflow.in/39646

Selected Answer

the actual design is in 1NF coz there are partial dependencies in the given FD set so the original db design is in 1 NF but not 2NF

now the new design is removing all the partial dependencies so its in 2NF

so the weakest form that the new schema satisfies that the old one couldnt is 2NF answer is B

14 votes -- Bharani Viswas (671 points)

Original Database schema is not in 2NF, modified one is in BCNF.. so weakest form would be 2NF
Answer B

24 votes -- Abhilash Panicker (8.8k points)

3.6.3 Database Normalization: GATE1994_3.6 top

http://gateoverflow.in/2492

Selected Answer

False

BCNF decomposition can always be lossless, but it may not be always possible to get a dependency preserving BCNF decomposition.

18 votes -- Sourav Roy (3.6k points)

3.6.4 Database Normalization: GATE1995_26 top

http://gateoverflow.in/2665

Selected Answer

The Candidate Keys are AB and BC.

None of the given functional dependencies are partial. So, the scheme qualifies for 2 NF.

There is no transitive dependency. So, the scheme qualifies for 3 NF.

All determinants are not Candidate Keys. So, the scheme do not qualify for BCNF.

19 votes -- Rajarshi Sarkar (35k points)

3.6.5 Database Normalization: GATE1997_6.9 top

http://gateoverflow.in/2265

Selected Answer

Ck is ab.

Since all a,b,c,d are atomic so the relation is in 1 NF.

Now check the FD s.

a->c(P->NP)

b->d(P->NP)

Since there are partial dependencies,so it is not 2 NF.

a}Ans 1NF but not 2NF

16 votes -- Sourav Roy (3.6k points)

3.6.6 Database Normalization: GATE1998_1.34 top http://gateoverflow.in/1671

Selected Answer

3 NF,
because we can always have a 3NF decomposition which is dependency preserving and lossless (not possible for any higher forms).

20 votes -- Digvijay (47k points)

3.6.7 Database Normalization: GATE1998_26 top http://gateoverflow.in/1741

Selected Answer

- Book_id —————————————— i
- Subject_Category_of_book —————— c
- Name_of_Author ——————————— a
- Nationality_of_Author ————————— n
- Book_title ———————————— t
- Author_address —————————— d

first part) i --> c a n

which satisfies **BCNF**

second part)

i --> c a n

a t --> i c n d

CKs = { {a t} , {i t} }
first FD satisfies BCNF
second FD violates 2NF

Hence, in 1NF

20 votes -- Amar Vashishth (28.7k points)

No FDs are given. So, assuming them from the attributes.

Since Book_id is the key we have,

- Book_id -> Subject_Category_of_book
- Book_id -> Name_of_Author
- Book_id -> Nationality_of_Author

We can also have the following FDs

- Name_of_Author -> Nationality_of_Author

This FD won't be there if two authors exist with the same name. But Author_id being not there and {Name_of_Author, Book_title} in (b) part, shows that Name_of_Author is indeed unique.

Now, Name_of_Author -> Nationality_of_Author is a transitive functional dependency as both side of the FD are non-key attributes and the FD is non-trivial. So, the relation is not in 3NF. Since there is only one key (since no other attribute determine Book_id and Book_id is a key), it is in 2NF.

a. 2NF

b. New set of FDs are

- Book_id -> Subject_Category_of_book
- Book_id -> Name_of_Author
- Book_id -> Nationality_of_Author
- Book_id -> Book_title
- Name_of_Author -> Nationality_of_Author
- Name_of_Author -> Author_address
- {Book_title, Name_of_Author} -> Book_id

One thing to notice here is only the primary key is being changed from Book_id to {Book_title, Name_of_Author}, but Book_id is still a key as based on convention Book_id always determines Book_title.

So, now Name_of_Author -> Author_address becomes a partial FD as Name_of_Author is a part of a key and Author_address is not a key attribute. So, relation is now just in 1NF.

16 votes -- Arjun Suresh (294k points)

3.6.8 Database Normalization: GATE1999-2.7, UGCNET-June2014-III-25 top

http://gateoverflow.in/1485

Selected Answer

$R_1 \cap R_2 \neq \phi$. This makes the decomposition lossless join, as all the attributes are keys, $R_1 \cap R_2$ will be a key of the decomposed relations (lossless condition says the common attribute must be a key in at least one of the decomposed relation). Now, even the original relation R is in 3NF (even BCNF) as all the attributes are prime attributes (in fact each attribute is a candidate key). Hence, any decomposition will also be in 3NF (even BCNF). Option D.

PS: Decomposition in 3NF means decomposed relations are in 3NF.

26 votes -- Arjun Suresh (294k points)

Answer : **In both 2NF and 3NF**

Dependencies are

S --> T, T --> U, U -->V V --> S

S+ = STUV U+ = UVST

T+ = UVST V+ = VSTU

There is no Partial Dependencies here So it is in 2 NF

RHS of every Dependencies is a Key as well as all are Prime Attributes So it is in 3 NF.

12 votes -- shekhar chauhan (42.9k points)

3.6.9 Database Normalization: GATE1999_1.24 top

http://gateoverflow.in/1477

Selected Answer

Answer: B

EC is the key for R. Both E and C are not coming on the right hand side of any functional dependency. So, both of them must be present in any key. Now, with EC and the given FDs, we can derive all other attributes making EC a key.

13 votes -- Rajarshi Sarkar (35k points)

3.6.10 Database Normalization: GATE2001-1.23, UGCNET-June2012-III-18 top

http://gateoverflow.in/716

Selected Answer

ans is C.

here no common attribute in R1 and R2, therefore lossy join will be there.

and both the dependencies are preserved in composed relations so dependency preserving.

16 votes -- jayendra (8.1k points)

3.6.11 Database Normalization: GATE2001-2.23 top

http://gateoverflow.in/741

Selected Answer

taking up **option A** first :
We have, R(A, B, C, D) and the Functional Dependency set = {A→B, B→CD}.
Now we will try to decompose it such that the decomposition is a Lossless Join, Dependency Preserving and new relations thus formed are in BCNF.
We decomposed it to R_1(A, B) and R_2(B, C, D). This decomposition satisfies all three properties we mentioned prior.

taking up **option B** :
we have, R(A, B, C, D) and the Functional Dependency set = {A→B, B→C, C→D}.
we decomposed it as R_1(A, B), R_2(B, C) and R_3(C, D). This decomposition too satisfies all properties as decomposition in *option A*.

taking up **option D** :
we have, R(A, B, C, D) and the Functional Dependency set = {A→BCD}.
This set of FDs is equivalent to set = {A→B, A→C, A→D} on applying decomposition rule which is derived from Armstrong's Axioms.
we decomposed it as R_1(A, B), R_2(A, C) and R_3(A, D). This decomposition also satisfies all properties as required.

taking up **option C** :
we have, R(A, B, C, D) and the Functional Dependency set = {AB→C, C→AD}.
we decompose it as R_1(A, B, C) and R_2(C, D). This preserves all dependencies and the join is lossless too, but the relation R_1 is not in BCNF. In R_1 we keep ABC together otherwise preserving {AB→C} will fail, but doing so also causes {C→A} to appear in R_1. {C→A} violates the condition for R_1 to be in BCNF as C is not a superkey. Condition that all relations formed after decomposition should be in BCNF is not satisfied here.

We need to identify the INCORRECT, Hence mark **option C**.

41 votes -- Amar Vashishth (28.7k points)

(C) is the answer. Because of AB -> C and C -> A, we cannot have A, B and C together in any BCNF relation- in relation ABC, C is not a super key and C->A exists violating BCNF condition. So, we cannot preserve AB -> C dependency in any decomposition of ABCD.

For (A) we can have AB, BCD, A and B the respective keys
For (B) we can have AB, BC, CD, A, B and C the respective keys
For (D) we can have ABCD, A is key

20 votes -- Arjun Suresh (294k points)

3.6.12 Database Normalization: GATE2002-16 top

http://gateoverflow.in/869

Selected Answer

a) Yes as R1 ∩ R2 = M and M → O
b) NO

From the Dependencies obtained from R1 and R2, we CANNOT infer NO → P

Mistake That CAN be made: Here we CANNOT apply Pseudo Transitivity Rule using M→O & MN →P to obtain NO → P because the rule says :if M→O and NO→P then NM→P or MN→P , But here we have M→O and MN→P ... SO we CANNOT apply the rule here to obtain NO→P from it.

c) BCNF
R1 keys : P,L,MN hence BCNF
R2 key : M hence BCNF

13 votes -- Danish (3.6k points)

3.6.13 Database Normalization: GATE2002-2.24 top

http://gateoverflow.in/854

Selected Answer

A) False. BCNF may or may not satisfy Dependency preservation, 3NF always does. But we can't make any guaranteed decision, regarding BCNF if it satisfies Dependency preservation

B) False. Both are lossless.

C) True. Using this we can always decide between BCNF & 3NF.

D) False. Every BCNF relation is also 3NF trivially.

ANswer -> C (& Only C)

23 votes -- Akash (43.8k points)

A. dependency preservation.
in 3NF Dependency always preserved but in BCNF it may or may not be preserved.
For a particular set of FDs it may not differentiate BCNF and 3NF.

B.Lossless join always possible in both BCNF as well as 3NF.

D. 3NF definition also unable to differentiate BCNF & 3NF bcoz every BCNF is trivially 3NF.

C. every 3NF which is not BCNF fails BCNF Definition so it may used to differentiate which is BCNF & which is 3NF ..

12 votes -- Digvijay (47k points)

3.6.14 Database Normalization: GATE2003-85 top

http://gateoverflow.in/968

Selected Answer

There are three FDs that are valid from the above set of FDs for the given relation :

Date_of_Birth -> Age

Name -> Roll_number

Roll_number -> Name

candidate keys for the above are : (Date_of_Birth,Name) and (Date_of_Birth,Roll_number)

clearly there is partial dependency here (Date_of_Birth -> Age) and Age is not a prime attribute. So it is only in 1NF.

Option (D).

20 votes -- Danish (3.6k points)

3.6.15 Database Normalization: GATE2004-50 top

http://gateoverflow.in/1046

Selected Answer

option B is correct, because

Here candidate keys are,

Name+course

roll_no+course

that makes name, roll_no and course_no prime attribute(or park of key)

functional dependencies 3 and 4 are not partial FDs

rule of FD not belonging to 2NF is,

for FD x-->y, x should be prime attribute and y should be non prime attribute, here y is also a partial key

so this is 2NF, because y is also prime attribute

but for BCNF, for every FD, of x-->y , x should be super key, so this is not BCNF, because x is not super key

in 3NF, for every FD, x-->y , condition is x can be super key or y can be prime attribute, x is not super key, but y is prime attribute

thats why this condition holds ans relation is in 3NF

11 votes -- rameshbabu (3.3k points)

If we proceed with given FDs then either Name,courseno or RollNo,courseNo becomes the candidate key. So no non-prime attributes are partially dependent on any Key attributes. Hence 2NF test passed.

Again for 3rd and 4th FD, Name,roll are part of the key and for first 2 FDs, determinants are candidate key itself. So 3NF test passed but not BCNF. Hence 3NF answer. b.

13 votes -- shreya ghosh (3.4k points)

3.6.16 Database Normalization: GATE2004-IT-75 top http://gateoverflow.in/3719

Selected Answer

It is in 2nf - for 2NF all non prime attribute should be fully functionally dependent on key. Here key is empcode and contains only one attribute hence no partial dependency. But there is transitive dependency in this (pincode -> city, state). So it is not in 3 NF.

answer: B

22 votes -- Sankaranarayanan P.N (11.2k points)

3.6.17 Database Normalization: GATE2005-29, UGCNET-June2015-III-9 http://gateoverflow.in/1365 top

Selected Answer

option c

16 votes -- Sankaranarayanan P.N (11.2k points)

3.6.18 Database Normalization: GATE2005-78 top http://gateoverflow.in/1401

Selected Answer

(d) AEH, BEH, DEH

using the given functional dependencies and looking at the dependent attributes, E and H are not dependent on any. So, they must be part of any candidate key. So, only option is D. If we see the FD's, adding A, B or D to EH do form candidate keys.

17 votes -- Aravind (3.3k points)

3.6.19 Database Normalization: GATE2005-IT-22 top http://gateoverflow.in/3767

Selected Answer

ans : 1

key is f1f2

f1->f3, f2-> f4 are partial dependencies

20 votes -- rajsh3kar (1.3k points)

3.6.20 Database Normalization: GATE2007-62, UGCNET-June2014-II-47 http://gateoverflow.in/1260 top

Selected Answer

1. Any relation with two attributes is in BCNF => This is true. It is trivial
2. A relation in which every key has only one attribute is in 2NF => This is true. As it is not possible to have Partial Functional Dependency !
3. A prime attribute can be transitively dependent on a key in a 3 NF relation => This is true. As For 3NF to be voilated we have something like Key => Non Key, Non Key => Non key

   . 3NF defination say x->y, either x should be key or y should be prime atrribute. Then we can have something like Key=> Non Key, Non key => Prime Attribute, resulting in Transitive FD on Prime Attribute, still in 3NF.
4. LHS must be always key, so No Transitive dependency is allowed. So answer => D

20 votes -- Akash (43.8k points)

(d)

Defn from wiki:

The 3NF version of the definition is weaker than Date's BCNF variation, as the former is concerned only with ensuring that *non-key* attributes are dependent on keys. Prime attributes (which are keys or parts of keys) must not be functionally dependent at all; they each represent a fact about the key in the sense of providing part or all of the key itself. (It should be noted here that this rule applies only to functionally dependent attributes, as applying it to all attributes would implicitly prohibit composite candidate keys, since each part of any such key would violate the "whole key" clause.)

12 votes -- Aravind (3.3k points)

3.6.21 Database Normalization: GATE2008-69 top http://gateoverflow.in/492

Selected Answer

Answer: C

It is given that *{Author , Title}* is the key for both schemas.

The given dependencies are :

- {Title, Author} --> {Catalog_no}
- Catalog_no --> {Title , Author , Publisher , Year }
- {Publisher , Title , Year} --> {Price}

First , let's take schema *Collection (Title , Author , Catalog_no) :*

{Title , Author} --> Catalog_no

{Title, Author} is a candidate key and hence super key also and by definition of BCNF this is in BCNF.

Now , let's see *Book (Title , Author , Catalog_no , Publisher , Year , Price) :*

{Title , Author}+ --> {Title , Author , Catalog_no , Publisher , Year , Price}

{Catalog_no}+--> {Title , Author , Publisher , Year , Price , Catalog_no}

So candidate keys are : Catalog_no , {Title , Author}

But in the given dependencies , {Publisher , Title , Year} --> Price , which has Transitive Dependency. **So , Book is in 2NF.**

16 votes -- worst_engineer (5.6k points)

3.6.22 Database Normalization: GATE2008-IT-61 top

http://gateoverflow.in/3371

Selected Answer

Option A.

(A,B) (B,C) -> common attribute is B and due to B->C, B is a key for (B,C) and hence ABC can be losslessly decomposed into (A,B) and (B,C).

(A, B, C) (B, D), common attribute is B and B->D is a FD (via B->C, C->D), and hence B is a key for (B, D). So, decomposition of (A, B, C, D) into (A, B, C) (B, D) is lossless.

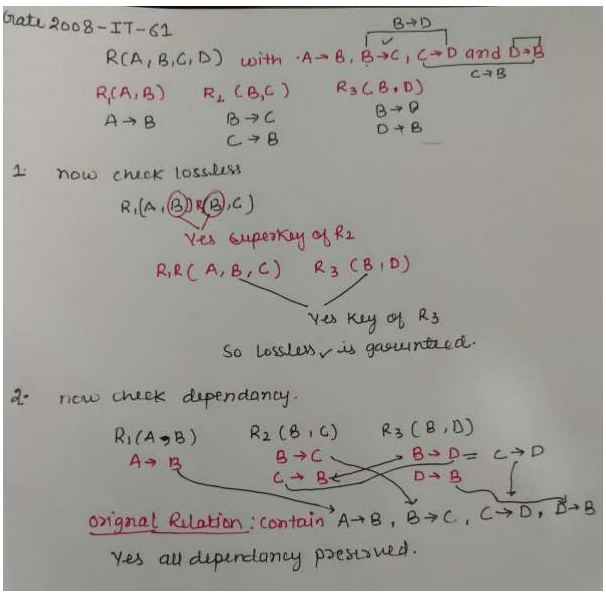
Thus the given decomposition is lossless.

The given decomposition is also dependency preserving as the dependencies A->B is present in (A, B), B->C is present in (B, C), D->B is present in (B, D) and C->D is indirectly present via C->B in (B, C) and B->D in (B, D).

http://www.sztaki.hu/~fodroczi/dbs/dep-pres-own.pdf

37 votes -- Arjun Suresh (294k points)

Answer is a i.e. dependancy preserved and lossless decompostion.



22 votes -- Prashant Singh (49.2k points)

3.6.23 Database Normalization: GATE2008-IT-62 top

http://gateoverflow.in/3372

Selected Answer

Answer: D

Here AB is the candidate key and B->G is a partial dependency. So, R is not in 2 NF.

19 votes -- Rajarshi Sarkar (35k points)

3.6.24 Database Normalization: GATE2009-55 top

http://gateoverflow.in/1339

Selected Answer

```
SELECT P.pid FROM Parts P WHERE P.color<>'blue'
```

Select all non blue parts

```
SELECT C.sid FROM Catalog C WHERE C.pid NOT IN
```

Selects all suppliers who have supplied a blue part

```
SELECT S.sname
FROM    Suppliers S
WHERE S.sid NOT IN
```

Selects suppliers who have not supplied any blue parts.

So, **none** of the options matches.

Option C is wrong as it does not select suppliers who have not supplied any parts which the given query does.

Option A is wrong because it even selects those suppliers who have supplied blue and non-blue parts and also does not include those suppliers who have not supplied any parts.

24 votes -- Arjun Suresh (294k points)

3.6.25 Database Normalization: GATE2009-56 top

http://gateoverflow.in/43474

Selected Answer

56. The non-trivial FDs are
(sname, city) → street
sid → street
(sname, city) → sid
sid → sname
sid → city

For all these, LHS is a super key and hence BCNF condition satisfied. But we have some more dependencies here:

> "each supplier and each street within a city has unique name"

This basically means each supplier in a city has unique name making (sname, city) determine sid and hence making it a candidate key. Each street within a city also has a unique name and so (street, city) is also a candidate key. Even then with all 3 candidate keys (for Suppliers schema), for any FD, the LHS is a super key here, and hence the relation schema (for other two relations it is straight forward) is in BCNF.

http://db.grussell.org/section009.html

21 votes -- Arjun Suresh (294k points)

3.6.26 Database Normalization: GATE2012-2 top http://gateoverflow.in/34

Selected Answer

(C) Every relation in BCNF is also in 3NF. Striaght from definition of BCNF.

16 votes -- Arjun Suresh (294k points)

3.6.27 Database Normalization: GATE2014-1-30 top http://gateoverflow.in/1797

Selected Answer

(A) S1 is TRUE and S2 is FALSE.

a relation with 2 attributes is always in bcnf

the two sets of fnuctional dependecy are not the same , could not derive ab -> E from the 1 st set

15 votes -- Aravind (3.3k points)

3.7 Er Diagram(7) top

3.7.1 Er Diagram: GATE2004-IT-73 top http://gateoverflow.in/3717

Consider the following entity relationship diagram (ERD), where two entities E1 and E2 have a relation R of cardinality 1 : m.

The attributes of E1 are A11, A12 and A13 where A11 is the key attribute. The attributes of E2 are A21, A22 and A23 where A21 is the key attribute and A23 is a multi-valued attribute. Relation R does not have any attribute. A relational database containing minimum number of tables with each table satisfying the requirements of the third normal form (3NF) is designed from the above ERD. The number of tables in the database is

A. 2
B. 3
C. 5
D. 4

gate2004-it databases er-diagram normal

Answer

3.7.2 Er Diagram: GATE2005-75 top http://gateoverflow.in/1398

Let E_1 and E_2 be two entities in an E/R diagram with simple-valued attributes. R_1 and R_2 are two relationships between E_1 and E_2, where R_1 is one-to-many and R_2 is many-to-many. R_1 and R_2 do not have any attributes of their own. What is the minimum number of tables required to represent this situation in the relational model?

A. 2
B. 3
C. 4
D. 5

gate2005 databases er-diagram normal

Answer

3.7.3 Er Diagram: GATE2005-IT-21 top http://gateoverflow.in/3766

Consider the entities 'hotel room', and 'person' with a many to many relationship 'lodging' as shown below:

If we wish to store information about the rent payment to be made by person (s) occupying different hotel rooms, then this information should appear as an attribute of

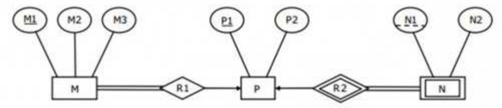
A. Person
B. Hotel Room
C. Lodging
D. None of these

gate2005-it databases er-diagram easy

Answer

3.7.4 Er Diagram: GATE2008-82 top http://gateoverflow.in/390

Consider the following ER diagram



The minimum number of tables needed to represent M, N, P, R1, R2 is

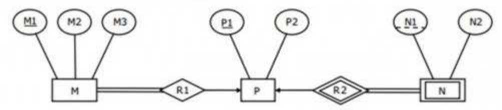
A. 2
B. 3
C. 4
D. 5

gate2008 databases er-diagram normal

Answer

3.7.5 Er Diagram: GATE2008-83 top http://gateoverflow.in/87025

Consider the following ER diagram



The minimum number of tables needed to represent M, N, P, R1, R2 is

Which of the following is a correct attribute set for one of the tables for the minimum number of tables needed to represent M, N, P, R1, R2?

A. {M1, M2, M3, P1}
B. {M1, P1, N1, N2}
C. {M1, P1, N1}
D. {M1, P1}

gate2008 databases er-diagram normal

Answer

3.7.6 Er Diagram: GATE2012-14 top http://gateoverflow.in/46

Given the basic ER and relational models, which of the following is **INCORRECT**?

A. An attribute of an entity can have more than one value
B. An attribute of an entity can be composite
C. In a row of a relational table, an attribute can have more than one value
D. In a row of a relational table, an attribute can have exactly one value or a NULL value

gate2012 databases normal er-diagram

Answer

3.7.7 Er Diagram: GATE2015-1_41 top

http://gateoverflow.in/8309

Consider an Entity-Relationship (ER) model in which entity sets E_1 and E_2 are connected by an m:n relationship R_{12}. E_1 and E_3 are connected by a 1 : n (1 on the side of E_1 and n on the side of E_3) relationship R_{13}.

E_1 has two-singled attributes a_{11} and a_{12} of which a_{11} is the key attribute. E_2 has two singled-valued attributes a_{21} and a_{22} of which a_{21} is the key attribute. E_3 has two single-valued attributes a_{31} and a_{32} of which a_{31} is the key attribute. The relationships do not have any attributes.

If a relational model is derived from the above ER model, then the minimum number of relations that would be generated if all relation are in 3NF is________________.

gate2015-1 databases er-diagram normal numerical-answers

Answer

Answers: Er Diagram

3.7.1 Er Diagram: GATE2004-IT-73 top

http://gateoverflow.in/3717

Selected Answer

We need just two tables for 1NF.

T1: {A11, A12, A13}

T2: {A21, A22, A23, A11}

A23 being multi-valued, {A21, A23} becomes the key for T2 as we need to repeat multiple values corresponding to the multi-valued attribute to make it 1NF. But, this causes partial FD A21 -> A22 and makes the table not in 2NF. In order to make the table in 2NF, we have to create a separate table for multi-valued attribute. Then we get

T1: {A11, A12, A13} - key is A11
T2: {A21, A22, A11} - key is A21
T3: {A21, A23} - key is {A21, A23}

Here, all determinants of all FDs are keys and hence the relation is in BCNF and so 3NF also. So, we need minimum 3 tables.

29 votes -- Arjun Suresh (294k points)

3.7.2 Er Diagram: GATE2005-75 top

http://gateoverflow.in/1398

Selected Answer

We need a separate table for many-to-many relation.
one-to-many relation doesn't need a separate table and can be handled using a foreign key.
So, answer is B. 3 tables.

Ref: http://web.cse.ohio-state.edu/~gurari/course/cse670/cse670Ch9.xht

18 votes -- Arjun Suresh (294k points)

3.7.3 Er Diagram: GATE2005-IT-21 top

http://gateoverflow.in/3766

Selected Answer

since it is many to many. rent cannot be an attribute of room or person entities alone. if depending on number of persons sharing a room the rent for each person for the room will be different. otherwise rent can be attribute of room. hence i go for attribute of Lodging

22 votes -- Sankaranarayanan P.N (11.2k points)

3.7.4 Er Diagram: GATE2008-82 top

http://gateoverflow.in/390

Selected Answer

First strong entity types are made to tables. So, we get two tables M and P.

I assume R1 is 1:1 or 1:n as that would minimize the number of tables as asked in question.

Now participation of M in R1 is total (indicated by double arrow) meaning every entity of M participate in R1. Since R1 is not having an attribute, we can simple add the primary key of P to the table M and add a foreign key reference to M. This handles R1 and we don't need an extra table. So, M becomes {M1, M2, M3, P1}.

N here is a weak entity weakly related to P. So, we form a new table N, and includes the primary key of P (P1) as foreign key reference. Now (P1, N1) becomes the primary key of N.

Thus we get 3 tables.

M: {M1, M2, M3, P1} - M1 primary key, P1 references P

P: {P1, P2} - P1 primary key

N: {P1, N1, N2} - (P1, N1) primary key, P1 references P.

So, answers are 82: B and 83: A.

36 votes -- Arjun Suresh (294k points)

3.7.5 Er Diagram: GATE2008-83 top

http://gateoverflow.in/87025

Selected Answer

First strong entity types are made to tables. So, we get two tables M and P.

I assume R1 is 1:1 or 1:n as that would minimize the number of tables as asked in question.

Now participation of M in R1 is total (indicated by double arrow) meaning every entity of M participate in R1. Since R1 is not having an attribute, we can simple add the primary key of P to the table M and add a foreign key reference to M. This handles R1 and we don't need an extra table. So, M becomes {M1, M2, M3, P1}.

N here is a weak entity weakly related to P. So, we form a new table N, and includes the primary key of P (P1) as foreign key reference. Now (P1, N1) becomes the primary key of N.

Thus we get 3 tables.

M: {M1, M2, M3, P1} - M1 primary key, P1 references P

P: {P1, P2} - P1 primary key

N: {P1, N1, N2} - (P1, N1) primary key, P1 references P.

So, answers is A.

9 votes -- Arjun Suresh (294k points)

3.7.6 Er Diagram: GATE2012-14 top

http://gateoverflow.in/46

Selected Answer

(C) is incorrect as a relational table requires that, in a row, an attribute can have exactly one value or NULL value.

16 votes -- Arjun Suresh (294k points)

3.7.7 Er Diagram: GATE2015-1_41 top

http://gateoverflow.in/8309

Selected Answer

Answer is 4. The relations are as shown:

<a11, a12> for E1

<a21, a22> for E2

<a31, a32, a11> for E3 and E1-E3 relationship

<a11, a21> for m:n relationship E1-E2

We cannot combine any relation here as it will give rise to partial functional dependency and thus violate 3NF.

http://cisnet.baruch.cuny.edu/holowczak/classes/9440/entityrelationship/

30 votes -- Arjun Suresh (294k points)

3.8 Functional Dependencies(13) top

3.8.1 Functional Dependencies: GATE1987-2n top http://gateoverflow.in/80609

State whether the following statements are TRUE or FALSE:

A relation r with schema (X, Y) satisfies the function dependency $X \rightarrow Y$, The tuples $\langle 1, 2 \rangle$ and $\langle 2, 2 \rangle$ can both be in r simultaneously.

gate1987 databases functional-dependencies

Answer

3.8.2 Functional Dependencies: GATE2000-2.24 top http://gateoverflow.in/671

Given the following relation instance.

X	Y	Z
1	4	2
1	5	3
1	6	3
3	2	2

Which of the following functional dependencies are satisfied by the instance?

A. XY → Z and Z → Y
B. YZ → X and Y → Z
C. YZ → X and X → Z
D. XZ → Y and Y → X

gate2000 databases functional-dependencies easy

Answer

3.8.3 Functional Dependencies: GATE2002-1.19 top http://gateoverflow.in/824

Relation R with an associated set of functional dependencies, F, is decomposed into BCNF. The redundancy (arising out of functional dependencies) in the resulting set of relations is

A. Zero
B. More than zero but less than that of an equivalent 3NF decomposition
C. Proportional to the size of F^+
D. Indeterminate

gate2002 databases functional-dependencies database-normalization normal

Answer

3.8.4 Functional Dependencies: GATE2002-2.25 top http://gateoverflow.in/855

Form the following instance of a relation schema R(A,B,C), we can conclude that:

A	B	C
1	1	1
1	1	0
2	3	2
2	3	2

A. A functionally determines B and B functionally determines C
B. A functionally determines B and B does not functionally determine C
C. B does not functionally determine C
D. A does not functionally determine B and B does not functionally determine C

gate2002 databases functional-dependencies

Answer

3.8.5 Functional Dependencies: GATE2005-IT-70 top http://gateoverflow.in/3833

In a schema with attributes A, B, C, D and E following set of functional dependencies are given

A → B
A → C
CD → E
B → D
E → A

Which of the following functional dependencies is NOT implied by the above set?

A. CD → AC
B. BD → CD
C. BC → CD
D. AC → BC

gate2005-it databases functional-dependencies normal

Answer

3.8.6 Functional Dependencies: GATE2006-70 top http://gateoverflow.in/1848

The following functional dependencies are given:

$$AB \rightarrow CD, AF \rightarrow D, DE \rightarrow F,\ C \rightarrow G, F \rightarrow E, G \rightarrow A$$

Which one of the following options is false?

A. $\{CF\}^* = \{ACDEFG\}$
B. $\{BG\}^* = \{ABCDG\}$
C. $\{AF\}^* = \{ACDEFG\}$
D. $\{AB\}^* = \{ABCDG\}$

gate2006 databases functional-dependencies normal

Answer

3.8.7 Functional Dependencies: GATE2006-IT-60 top http://gateoverflow.in/3604

Consider a relation R with five attributes V, W, X, Y, and Z. The following functional dependencies hold:

VY→ W, WX → Z, and ZY → V.

Which of the following is a candidate key for R?

A. VXZ
B. VXY
C. VWXY
D. VWXYZ

gate2006-it databases functional-dependencies normal

Answer

3.8.8 Functional Dependencies: GATE2013-54 top

http://gateoverflow.in/1558

Relation R has eight attributes ABCDEFGH. Fields of R contain only atomic values. F={CH→G, A→BC, B→CFH, E→A, F→EG} is a set of functional dependencies (FDs) so that F^+ is exactly the set of FDs that hold for R.

Q.54 How many candidate keys does the relation R have?

(A) 3 (B) 4 (C) 5 (D) 6

gate2013 databases functional-dependencies database-normalization normal

Answer

3.8.9 Functional Dependencies: GATE2013-55 top

http://gateoverflow.in/43290

Relation R has eight attributes ABCDEFGH. Fields of R contain only atomic values. F={CH $\rightarrow$ G, A $\rightarrow$ BC, B $\rightarrow$ CFH, E $\rightarrow$ A, F $\rightarrow$ EG} is a set of functional dependencies (FDs) so that F^+ is exactly the set of FDs that hold for R.

The relation R is

A. in 1NF, but not in 2NF.
B. in 2NF, but not in 3NF.
C. in 3NF, but not in BCNF.
D. in BCNF.

gate2013 databases functional-dependencies database-normalization normal

Answer

3.8.10 Functional Dependencies: GATE2014-1-21 top

http://gateoverflow.in/1788

Consider the relation scheme $R = (E, F, G, H, I, J, K, L, M, N)$ and the set of functional dependencies

$$\{\{E, F\} \rightarrow \{G\}, \{F\} \rightarrow \{I, J\}, \{E, H\} \rightarrow \{K, L\}, \{K\} \rightarrow \{M\}, \{L\} \rightarrow \{N\}\}$$

on R. What is the key for R?

A. $\{E, F\}$
B. $\{E, F, H\}$
C. $\{E, F, H, K, L\}$
D. $\{E\}$

gate2014-1 databases functional-dependencies normal

Answer

3.8.11 Functional Dependencies: GATE2015-3_20 top

http://gateoverflow.in/8420

Consider the relation $X(P, Q, R, S, T, U)$ with the following set of functional dependencies

$F = \{ \ \{P, R\} \rightarrow \{S, T\}, \ \{P, S, U\} \rightarrow \{Q, R\} \ \}$

Which of the following is the trivial functional dependency in F^+, where F^+ is closure to F?

A. $\{P, R\} \rightarrow \{S, T\}$
B. $\{P, R\} \rightarrow \{R, T\}$
C. $\{P, S\} \rightarrow \{S\}$
D. $\{P, S, U\} \rightarrow \{Q\}$

gate2015-3 databases functional-dependencies easy

Answer

3.8.12 Functional Dependencies: GATE2017-1-16 top

http://gateoverflow.in/118296

The following functional dependencies hold true for the relational schema $R\{V, W, X, Y, Z\}$:

V $\rightarrow$ W

VW $\rightarrow$ X
Y $\rightarrow$ VX
Y $\rightarrow$ Z

Which of the following is irreducible equivalent for this set of functional dependencies?

(A) V $\rightarrow$ W
V $\rightarrow$ X
Y $\rightarrow$ V
Y $\rightarrow$ Z

(B) V $\rightarrow$ W
W $\rightarrow$ X
Y $\rightarrow$ V
Y $\rightarrow$ Z

(C) V $\rightarrow$ W
V $\rightarrow$ X
Y $\rightarrow$ V
Y $\rightarrow$ X
Y $\rightarrow$ Z

(D) V $\rightarrow$ W
W $\rightarrow$ X
Y $\rightarrow$ V
Y $\rightarrow$ X
Y $\rightarrow$ Z

gate2017-1 databases functional-dependencies normal

Answer

3.8.13 Functional Dependencies: ISI2011-CS-5b top http://gateoverflow.in/48168

Suppose we have a relation $R(A, B, C, D, E)$ with the functional dependencies: $A \rightarrow D, B \rightarrow C, D \rightarrow E, CE \rightarrow B$.

If we project R and therefore its functional dependencies onto the schema ABC, what will the key(s) for ABC be?

descriptive isi2011 databases functional-dependencies

Answer

Answers: Functional Dependencies

3.8.1 Functional Dependencies: GATE1987-2n top http://gateoverflow.in/80609

Selected Answer

True is answer

X-> y says when X is same , Same Y will come. SInce X is not repeated so Y can repeat.

X	y
1	2
2	2

10 votes -- Prashant Singh (49.2k points)

3.8.2 Functional Dependencies: GATE2000-2.24 top http://gateoverflow.in/671

Selected Answer

(b)

if a->b then for each same value of a , b should be same,

we have to get the opposite of the defn i.e if no values of a are same then b need be same

17 votes -- Aravind (3.3k points)

3.8.3 Functional Dependencies: GATE2002-1.19 top http://gateoverflow.in/824

Selected Answer

Answer: A

If a relation schema is in BCNF then all redundancy based on functional dependency has been removed, although other types of redundancy may still exist. A relational schema *R* is in Boyce–Codd normal form if and only if for every one of its dependencies $X \rightarrow Y$, at least one of the following conditions hold:

- $X \rightarrow Y$ is a trivial functional dependency (Y ⊆ X)
- *X* is a super key for schema *R*
- http://en.wikipedia.org/wiki/Boyce%E2%80%93Codd_normal_form

21 votes -- Priya_das (775 points)

should be zero..
BCNF can have Multi valued dependency but no redundancy due to FDs..

13 votes -- Digvijay (47k points)

3.8.4 Functional Dependencies: GATE2002-2.25 top http://gateoverflow.in/855

Selected Answer

Ans. C

Generally Normalization is done on the schema itself.

From the relational instance given,we may strike out FD s that do not hold.

e.g.B does not functionally determine C(This is true).

But we cannot say that A functionally determines B for the entire relation itself.This is because that ,A->B holds for this instance,but in future there might be some tuples added to the instance that may violate A->B.

So overall on the relation we cannot conclude that A->B,from the relational instance which is just a subset of an entire relation.

24 votes -- Sourav Roy (3.6k points)

3.8.5 Functional Dependencies: GATE2005-IT-70 top http://gateoverflow.in/3833

Selected Answer

Answer is B.

Apply membership test for all the given Functional Dependencies.

1.) CD-->AC

CD^+ = CDEAB

2.) BD-->CD

BD^+ = BD

i.e. BD cannot derive CD and hence is not implied.

Similarly do for rest two.

16 votes -- Gate Keeda (19.1k points)

3.8.6 Functional Dependencies: GATE2006-70 top http://gateoverflow.in/1848

Selected Answer

{AF}* ={AFDE}. Hence option C is wrong

15 votes -- Sankaranarayanan P.N (11.2k points)

3.8.7 Functional Dependencies: GATE2006-IT-60 top http://gateoverflow.in/3604

Selected Answer

As we can see attr X Y do not appear in rhs of any fd they need to be part of key
Candidate keys are VXY,WXY,ZXY.

Ans is b

9 votes -- Pooja Palod (32.4k points)

3.8.8 Functional Dependencies: GATE2013-54 top http://gateoverflow.in/1558

Selected Answer

54) B.

4 candidate keys namely DA,DB,DE,DF.

17 votes -- kalpashri (357 points)

3.8.9 Functional Dependencies: GATE2013-55 top http://gateoverflow.in/43290

Selected Answer

Here Candidate keys are AD, BD, ED and FD .

Partial dependency exists $A \rightarrow BC$, $B \rightarrow CFH$ and $F \rightarrow EG$ etc in the following FDs.

For example partial dependency $A \rightarrow C$ exists in $A \rightarrow BC$ and $B \rightarrow C$ and $B \rightarrow H$ in $B \rightarrow CFH$. etc.

So given relation is in 1NF ,but not in 2NF.

14 votes -- Manoj Kumar (37.5k points)

3.8.10 Functional Dependencies: GATE2014-1-21 top http://gateoverflow.in/1788

Selected Answer

since H cannot be derived from anything else H should be there in key

using Find {EFH}+ it contains all the attributes of the relation

hence it is key

14 votes -- Sankaranarayanan P.N (11.2k points)

3.8.11 Functional Dependencies: GATE2015-3_20 top

http://gateoverflow.in/8420

Selected Answer

option C is correct because $\{P, S\} \rightarrow \{S\}$
for trivial FD, if $X \rightarrow Y$ then Y must be a subset of X and for non trivial FD $X \cap Y = \emptyset$. and here $\{S\}$ is subset of $\{P, S\}$.

PS: Trivial means something which is always there. An attribute set always determines any of the component attributes and this is always true irrespective of the relation instance. Hence this FD becomes trivial.

23 votes -- Anoop Sonkar (4.9k points)

3.8.12 Functional Dependencies: GATE2017-1-16 top

http://gateoverflow.in/118296

Selected Answer

in option B and option D there is a dependency W->X which is not implied by the question and hence they are definitely wrong

Now in option C) Y->X can be removed as it can be implied as Y->V and V->X

hence OPTION (A) is correct

6 votes -- sriv_shubham (2.7k points)

3.8.13 Functional Dependencies: ISI2011-CS-5b top

http://gateoverflow.in/48168

A+ = ADE B+ =BC C+ =C

AB+ = ABCDE First Key : AB+ =ABC

AC+ = ABCDE Second Key : AC+ =ACB

BC+ = BC

So on schema ABC we Got 2 keys.

7 votes -- shekhar chauhan (42.9k points)

3.9 Indexing(9) top

3.9.1 Indexing: GATE1993_14 top

http://gateoverflow.in/2311

An ISAM (indexed sequential) file consists of records of size 64 bytes each, including key field of size 14 bytes. An address of a disk block takes 2 bytes. If the disk block size is 512 bytes and there are 16 K records, compute the size of the data and index areas in terms of number blocks. How many levels of tree do you have for the index?

gate1993 databases indexing normal

Answer

3.9.2 Indexing: GATE1998_1.35 top

http://gateoverflow.in/1672

There are five records in a database.

Name	Age	Occupation	Category
Rama	27	CON	A
Abdul	22	ENG	A
Jennifer	28	DOC	B
Maya	32	SER	D
Dev	24	MUS	C

There is an index file associated with this and it contains the values 1, 3, 2, 5 and 4. Which one of the fields is the index built from?

A. Age
B. Name
C. Occupation
D. Category

gate1998 databases indexing normal

Answer

3.9.3 Indexing: GATE2002-2.22 top

http://gateoverflow.in/852

In the index allocation scheme of blocks to a file, the maximum possible size of the file depends on

A. the size of the blocks, and the size of the address of the blocks.
B. the number of blocks used for the index, and the size of the blocks.
C. the size of the blocks, the number of blocks used for the index, and the size of the address of the blocks.
D. None of the above

gate2002 databases indexing normal

Answer

3.9.4 Indexing: GATE2008-16, ISRO2016-60 top

http://gateoverflow.in/414

A clustering index is defined on the fields which are of type

A. non-key and ordering
B. non-key and non-ordering
C. key and ordering
D. key and non-ordering

gate2008 easy databases indexing isro2016

Answer

3.9.5 Indexing: GATE2008-70 top

http://gateoverflow.in/259

Consider a file of 16384 records. Each record is 32 bytes long and its key field is of size 6 bytes. The file is ordered on a non-key field, and the file organization is unspanned. The file is stored in a file system with block size 1024 bytes, and the size of a block pointer is 10 bytes. If the secondary index is built on the key field of the file, and a multi-level index scheme is used to store the secondary index, the number of first-level and second-level blocks in the multi-level index are respectively

A. 8 and 0
B. 128 and 6
C. 256 and 4
D. 512 and 5

gate2008 databases indexing normal

Answer

3.9.6 Indexing: GATE2011_39 top

http://gateoverflow.in/2141

Consider a relational table r with sufficient number of records, having attributes $A_1, A_2, \dots, A_n$ and let $1 \leq p \leq n$. Two queries $Q1$ and $Q2$ are given below.

- $Q1 : \pi_{A_1,\dots,A_p} \left(\sigma_{A_p=c}\left(r\right)\right)$ where c is a constant
- $Q2 : \pi_{A_1,\dots,A_p} \left(\sigma_{c_1 \leq A_p \leq c_2}\left(r\right)\right)$ where c_1 and c_2 are constants.

The database can be configured to do ordered indexing on A_p or hashing on A_p. Which of the following statements is **TRUE**?

(A) Ordered indexing will always outperform hashing for both queries

(B) Hashing will always outperform ordered indexing for both queries

(C) Hashing will outperform ordered indexing on $Q1$, but not on $Q2$

(D) Hashing will outperform ordered indexing on $Q2$, but not on $Q1$

gate2011 databases indexing normal

Answer

3.9.7 Indexing: GATE2013_15 top http://gateoverflow.in/1437

An index is clustered, if

(A) it is on a set of fields that form a candidate key.

(B) it is on a set of fields that include the primary key.

(C) the data records of the file are organized in the same order as the data entries of the index.

(D) the data records of the file are organized not in the same order as the data entries of the index.

gate2013 databases indexing normal

Answer

3.9.8 Indexing: GATE2015-1_24 top http://gateoverflow.in/8222

A file is organized so that the ordering of the data records is the same as or close to the ordering of data entries in some index. Than that index is called

A. Dense
B. Sparse
C. Clustered
D. Unclustered

gate2015-1 databases indexing easy

Answer

3.9.9 Indexing: GATE2017-2-49 top http://gateoverflow.in/118561

In a B^+ Tree , if the search-key value is 8 bytes long , the block size is 512 bytes and the ointer size is 2 B , then the maximum order of the B^+ Tree is _____

gate2017-2 databases indexing b-tree numerical-answers

Answer

Answers: Indexing

3.9.1 Indexing: GATE1993_14 top http://gateoverflow.in/2311

Selected Answer

Answer: 3

Size of each index entry = 14 + 2 = 16 B

Blocking factor of record file = $\frac{\text{Block size}}{\text{Record size}}$ = 512 B/64 B = 8

Blocking factor of index file = $\frac{\text{Block size}}{\text{Index entry size}}$ = 512 B/16 B = 32

No. of Blocks needed for data file = $\frac{\text{No. of Records}}{\text{Blocking factor of record file}}$ = 16 K/8 = 2 K

No. of first level index entries = No. of Data Blocks needed for data file = 2 K

No. of first level index blocks = $\left\lceil \frac{\text{No. of first level index entries}}{\text{Blocking factor of index file}} \right\rceil = \left\lceil \frac{2K}{32} \right\rceil$ = 64

No. of second level index entries = No. of first level index blocks = 64

No. of second level index blocks = $\left\lceil \frac{\text{No. of second level index entries}}{\text{Blocking factor of index file}} \right\rceil = \left\lceil \frac{64}{32} \right\rceil$ = 2

No. of third level index entries = No. of second level index blocks = 2

No. of third level index blocks = $\left\lceil \frac{\text{No. of third level index entries}}{\text{Blocking factor of index file}} \right\rceil = \left\lceil \frac{2}{32} \right\rceil$ = 1

19 votes -- Rajarshi Sarkar (35k points)

3.9.2 Indexing: GATE1998_1.35 top http://gateoverflow.in/1672

Selected Answer

Indexing will be on Occupation field because Occupation field lexicographically sorted will give the sequence 1,3,2,5,4.

23 votes -- Digvijay (47k points)

3.9.3 Indexing: GATE2002-2.22 top http://gateoverflow.in/852

Selected Answer

In Index allocation size of maximum file can be derived like following :-

No of addressable blocks using one Index block (A)= Size of block / Size of block address

No of block addresses available for addressing one file (B) = No of Maximum blocks we can use for the Index * No of addressable blocks using one Index block (A)

Size of File = B * Size of Block

So it is clear that ->

Answer is (C).

A & B are incomplete.

17 votes -- Akash (43.8k points)

3.9.4 Indexing: GATE2008-16, ISRO2016-60 top http://gateoverflow.in/414

Selected Answer

There are several types of ordered indexes. A **primary index** is specified on the *ordering key field* of an **ordered file** of records. Recall from Section 17.7 that an ordering key field is used to *physically order* the file records on disk, and every record has a *unique value* for that field. If the ordering field is not a key field—that is, if numerous records in the file can have the same value for the ordering field— another type of index, called a **clustering index**, can be used. The data file is called a **clustered file** in this latter case. Notice that a file can have at most one physical ordering field, so it can have at most one primary index or one clustering index, *but not both*.

Ref -> Database Systems book BY Navathe, 6th Edition ,18.1 Types of Single-Level Ordered Indexes Page no 632

Answer should be A.

16 votes -- Akash (43.8k points)

A clustered index can be created on any attribute set, which is ordered (but maximum one for a table). By default, it is created for the primary key. We can change this to any non-key also. So, (A) and (C) can have clustered index. I guess the question assumes primary index as not being called clustered index, so answer should be A.

http://msdn.microsoft.com/en-us/library/ms186342.aspx

13 votes -- Arjun Suresh (294k points)

3.9.5 Indexing: GATE2008-70 top http://gateoverflow.in/259

Selected Answer

Content of an index will be <key, block pointer> and so will have size 6 + 10 = 16.

In the first level, there will be an entry for each record of the file. So,total size of first-level index

= 16384 * 16

No. of blocks in the first-level = Size of first-level index / block size
= 16384 * 16 / 1024
= 16 * 16 = 256

In the second-level there will be an entry for each block in the first level. So, total number of entries = 256 and total size of second-level index

= No. of entries * size of an entry
= 256 * 16

No. of blocks in second-level index = Size of second-level index / block size
= 256 * 16 / 1024

= 4

25 votes -- gatecse (13.4k points)

3.9.6 Indexing: GATE2011_39 top http://gateoverflow.in/2141

Selected Answer

(c) Hashing works well on the 'equal' queries, while ordered indexing works well better on range queries too. For ex consider B+ Tree, once you have searched a key in B+ tree , you can find range of values via the block pointers pointing to another block of values on the leaf node level.

19 votes -- Prateeksha Keshari (2.1k points)

3.9.7 Indexing: GATE2013_15 top http://gateoverflow.in/1437

Selected Answer

Ans C)

Index can be created using any column or combination of column which need not be unique. So A,B are not the ans.

Indexed column is used to sort rows of table.Whole data record of file is sorted using index so C is correct option. https://www.youtube.com/watch?v=NGslt99VOCw(Simple video explains this).

12 votes -- prashant singh (475 points)

3.9.8 Indexing: GATE2015-1_24 top http://gateoverflow.in/8222

Selected Answer

Clustered- this is the definition of clustered indexing and for the same reason a table can have only one clustered index.

http://www.ece.rutgers.edu/~yyzhang/spring03/notes/7-B+tree.ppt

21 votes -- Arjun Suresh (294k points)

3.9.9 Indexing: GATE2017-2-49 top http://gateoverflow.in/118561

Selected Answer

let order of B+ tree is **p** then maximum number of child pointers = p and maximum number of keys = p-1.

To accommodate all child pointers and search key, total size of these together can not exceed 512 bytes.

$$2(p) + 8(p-1) \leq 512$$

$$\implies p \leq 52$$

Therefore maximum order must be **52**.

14 votes -- Sachin Mittal (7.1k points)

3.10 Joins(3) top

3.10.1 Joins: GATE2005-IT-82a top http://gateoverflow.in/3847

A database table T_1 has 2000 records and occupies 80 disk blocks. Another table T_2 has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for T_1 and one block of records for T_2 simultaneously at any point in time. No index is available on either table.

If Nested-loop join algorithm is employed to perform the join, with the most appropriate choice of table to be used in outer loop, the number of block accesses required for reading the data are

A. 800000
B. 40080
C. 32020
D. 100

gate2005-it databases normal joins

Answer

3.10.2 Joins: GATE2005-IT-82b top http://gateoverflow.in/3848

A database table T_1 has 2000 records and occupies 80 disk blocks. Another table T_2 has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for T_1 and one block of records for T_2 simultaneously at any point in time. No index is available on either table.

If, instead of Nested-loop join, Block nested-loop join is used, again with the most appropriate choice of table in the outer loop, the reduction in number of block accesses required for reading the data will be

A. 0
B. 30400
C. 38400
D. 798400

gate2005-it databases normal joins

Answer

3.10.3 Joins: GATE2014-2-30 top http://gateoverflow.in/1989

Consider a join (relation algebra) between relations $r(R)$ and $s(S)$ using the nested loop method. There are 3 buffers each of size equal to disk block size, out of which one buffer is reserved for intermediate results. Assuming size(r(R))<size(s(S)) , the join will have fewer number of disk block accesses if

A. relation $r(R)$ is in the outer loop.
B. relation $s(S)$ is in the outer loop.
C. join selection factor between $r(R)$ and $s(S)$ is more than 0.5.
D. join selection factor between $r(R)$ and $s(S)$ is less than 0.5.

gate2014-2 databases normal joins

Answer

Answers: Joins

3.10.1 Joins: GATE2005-IT-82a top http://gateoverflow.in/3847

Selected Answer

Refer : http://en.wikipedia.org/wiki/Nested_loop_join

as per this reference This algorithm will involve $n_r * b_s + b_r$ block transfers

either T1 can be R or T2

if R is T1 then total number of block access is 2000*20 + 80 = 40080

if R is T2 then total number of block access is 400*80+20 = 32020

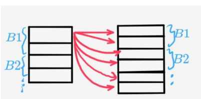
so better is the second case (32020) Hence i go for option C

20 votes -- Sankaranarayanan P.N (11.2k points)

3.10.2 Joins: GATE2005-IT-82b top http://gateoverflow.in/3848

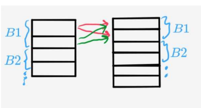
Selected Answer

In Nested loop join for each tuple in first table we scan through all the tuples in second table.



Here we will take table T2 as the outer table in nested loop join algorithm. The number of block accesses then will be 20 + (400 × 80) = 32020

In block nested loop join we keep 1 block of T1 in memory and 1 block of T2 in memory and do join on tuples.



For every block in T1 we need to load all blocks of T2. So number of block accesses is 80*20 + 20 = 1620

So the difference is 32020 - 1620 =30400

(B) 30400

20 votes -- Omesh Pandita (2.7k points)

3.10.3 Joins: GATE2014-2-30 top http://gateoverflow.in/1989

Selected Answer

Nested loop join is one of the methods to implement database in memory. A nested loop join is an algorithm that joins two sets by using two nested loops.

According to nested join,given relation R and S

For each tuple r in R do

For each tuple s in S do

If r and s satisfy the join condition

Then output the tuple <r,s>

Cost estimations for the above loop:

– b(R) and b(S) number of blocks in R and in S

– Each block of outer relation is read once

– Inner relation is read once for each block of outer relation

Summing up : IO= b(R)+b(R)*b(S) total IO operations

Lets assume |R|>|S| i.e b(R) =10 and b(s) =4

Now, if R is outer relation then, IO= 10+10*4=50

if S is outer relation then IO=4+4*10=44

As it can be observed , that total IO is lesser if the value of outer variable is less and as it is already given that |R|<|S|.Therefore, Relation r(R) should be in the outer loop to have fewer number of disk block accesses.

So, option (a) is correct.

17 votes -- Lubna Khan (331 points)

3.11 Multivalued Dependency 4nf(1) top

3.11.1 Multivalued Dependency 4nf: GATE2007-IT-67 top

http://gateoverflow.in/3512

Consider the following implications relating to functional and multivalued dependencies given below, which may or may not be correct.

i. If $A \to\to B$ and $A \to\to C$ then $A \to BC$
ii. If $A \to B$ and $A \to C$ then $A \to\to BC$
iii. If $A \to\to BC$ and $A \to B$ then $A \to C$
iv. If $A \to BC$ and $A \to B$ then $A \to\to C$

Exactly how many of the above implications are valid?

A. 0
B. 1
C. 2
D. 3

gate2007-it databases functional-dependencies multivalued-dependency-4nf normal

Answer

Answers: Multivalued Dependency 4nf

3.11.1 Multivalued Dependency 4nf: GATE2007-IT-67 top

http://gateoverflow.in/3512

Selected Answer

a. If $A \to\to B$ and $A \to\to C$ then $A \to BC$. So FALSE

b. If $A \to B$ and $A \to C$ then $A \to BC$. So $A \to\to BC$ TRUE..

c. If A →→ BC and A → B here B is Subset of AB and (A intersection BC) is phi so
A → B but not A → C so FALSE (**Coalescence rule**)
d. If A → BC then A → C so A →→ C TRUE
if A → B then A →→ B holds but reverse not true.

10 votes -- Digvijay (47k points)

3.12 Natural Join(2) top

3.12.1 Natural Join: GATE2010-43 top

http://gateoverflow.in/2344

The following functional dependencies hold for relations $R(A,B,C)$ and $S(B,D,E)$.

- $B \to A$
- $A \to C$

The relation R contains 200 tuples and the relation S contains 100 tuples. What is the maximum number of tuples possible in the natural join $R \bowtie S$?

A. 100
B. 200
C. 300
D. 2000

gate2010 databases normal natural-join functional-dependencies

Answer

3.12.2 Natural Join: GATE2015-2_32 top

http://gateoverflow.in/8151

Consider two relations $R_1(A,B)$ with the tuples $(1,5),(3,7)$ and $R_2(A,C)=(1,7),(4,9)$. Assume that $R(A,B,C)$ is the full natural outer join of R_1 and R_2. Consider the following tuples of the form (A,B,C):

$a=(1,5,null), b=(1,null,7), c=(3,null,9), d=(4,7,null), e=(1,5,7), f=(3,7,null), g=(4,null,9)$.

Which one of the following statements is correct?

A. R contains a,b,e,f,g but not c,d.
B. R contains all a,b,c,d,e,f,g .
C. R contains e,f,g but not a,b.
D. R contains e but not f,g.

gate2015-2 databases normal natural-join

Answer

Answers: Natural Join

3.12.1 Natural Join: GATE2010-43 top

http://gateoverflow.in/2344

Selected Answer

(A) 100

natural join will combine tuples with same value of the common rows(if there are two common rows then both vaues must be equal to get into the resultant set). So by this defn: we can get at the max only 100 common values :P

21 votes -- Aravind (3.3k points)

3.12.2 Natural Join: GATE2015-2_32 top

http://gateoverflow.in/8151

Selected Answer

$R_1(A,B)$

A	B
1	5
3	7

$R_2(A,C)$:

A	C
1	7
4	9

Now , if we do full natural outer join :

A	B	C
1	5	7
3	7	NULL
4	NULL	9

So, option (c) is correct.

13 votes -- worst_engineer (5.6k points)

3.13 Referential Integrity(3) top

3.13.1 Referential Integrity: GATE1997-6.10, ISRO2016-54 top http://gateoverflow.in/2266

Let $R(a,b,c)$ and $S(d,e,f)$ be two relations in which d is the foreign key of S that refers to the primary key of R. Consider the following four operations R and S

I. Insert into R

II. Insert into S

III. Delete from R

IV. Delete from S

Which of the following can cause violation of the referential integrity constraint above?

A. Both I and IV

B. Both II and III

C. All of these

D. None of these

gate1997 databases referential-integrity easy isro2016

Answer

3.13.2 Referential Integrity: GATE2005-76 top http://gateoverflow.in/1399

The following table has two attributes A and C where A is the primary key and C is the foreign key referencing A with on-delete cascade.

A	C
2	4
3	4

A	C
5	2
7	2
9	5
6	4

The set of all tuples that must be additionally deleted to preserve referential integrity when the tuple (2, 4) is deleted is:

A. (3, 4) and (6, 4)
B. (5, 2) and (7, 2)
C. (5, 2), (7, 2) and (9, 5)
D. (3, 4), (4, 3) and (6, 4)

gate2005 databases referential-integrity normal

Answer

3.13.3 Referential Integrity: GATE2017-2-19 top http://gateoverflow.in/118236

Consider the following tables T1 and T2.

T1	
P	**Q**
2	2
3	8
7	3
5	8
6	9
8	5
9	8

T2	
R	**S**
2	2
8	3
3	2
9	7
5	7
7	2

In table T1. **P** is the primary key and **Q** is the foreign key referencing **R** in table T2 with on-delete cascade and on-update cascade. In table T2, **R** is the primary key and **S** is the foreign key referencing **P** in table T1 with on-delete set NULL and on-update cascade. In order to delete record $\rangle 3,8 \langle$ from the table T1, the number of additional records that need to be deleted from table T1 is ________

gate2017-2 databases numerical-answers referential-integrity

Answer

Answers: Referential Integrity

3.13.1 Referential Integrity: GATE1997-6.10, ISRO2016-54 top http://gateoverflow.in/2266

Selected Answer

R

a Let(**PK**)	**b**	**c**
1		
2		

S

d(FK referring to PK of R)	e	f
2		
1		

Insert into R cannot cause any violation.

Insert into S can cause violation if any value is inserted into d of S, which value is not in a of R.

Delete from S would cause no violation.

Delete from R would cause violation if it any tuple is deleted,and as a result a value in a gets deleted which is refereed to by d in S.

20 votes -- Sourav Roy (3.6k points)

3.13.2 Referential Integrity: GATE2005-76 top

http://gateoverflow.in/1399

Selected Answer

(c)

since deleting (2,4) , since 2 is a primary key, u have to delete its foreign key occurence i.e (5,2) and (7,2)

since we are delting 5 , and 7 we have delete it foreign key occurence i.e (9,5)

there is no foreign key occurence for 9

19 votes -- Aravind (3.3k points)

3.13.3 Referential Integrity: GATE2017-2-19 top

http://gateoverflow.in/118236

Selected Answer

As Q refers to R so, deleting 8 from Q won't be an issue, however S refers P. But as the relationship given is on delete set NULL, 3 will be deleted from T1 and the entry in T2 having 3 in column S will be set to NULL. So, no more deletions. Answer is **0**.

14 votes -- Prateek Kumar (507 points)

3.14 Relational Algebra(16) top

3.14.1 Relational Algebra: GATE1992-13b top

http://gateoverflow.in/43581

Suppose we have a database consisting of the following three relations:

FREQUENTS	(CUSTOMER, HOTEL)
SERVES	(HOTEL, SNACKS)
LIKES	(CUSTOMER, SNACKS)

The first indicates the hotels each customer visits, the second tells which snacks each hotel serves and last indicates which snacks are liked by each customer. Express the following query in relational algebra:

Print the hotels the serve the snack that customer Rama likes.

gate1992 databases relational-algebra normal

Answer

3.14.2 Relational Algebra: GATE1994_13 top

http://gateoverflow.in/2509

Consider the following relational schema:

- COURSES (cno, cname)
- STUDENTS (rollno, sname, age, year)
- REGISTERED FOR (cno, rollno)

The underlined attributes indicate the primary keys for the relations. The 'year' attribute for the STUDENTS relation indicates the year in which the student is currently studying (First year, Second year etc.)

a. Write a relational algebra query to print the roll number of students who have registered for cno 322.

b. Write a SQL query to print the age and year of the youngest student in each year.

gate1994 databases relational-algebra sql normal

Answer

3.14.3 Relational Algebra: GATE1995_27 top http://gateoverflow.in/2666

Consider the relation scheme.

AUTHOR	(ANAME, INSTITUTION, ACITY, AGE)
PUBLISHER	(PNAME, PCITY)
BOOK	(TITLE, ANAME, PNAME)

Express the following queries using (one or more of) SELECT, PROJECT, JOIN and DIVIDE operations.

a. Get the names of all publishers.

b. Get values of all attributes of all authors who have published a book for the publisher with PNAME='TECHNICAL PUBLISHERS'.

c. Get the names of all authors who have published a book for any publisher located in Madras

gate1995 databases relational-algebra normal

Answer

3.14.4 Relational Algebra: GATE1996_27 top http://gateoverflow.in/2779

A library relational database system uses the following schema

- USERS (User#, User Name, Home Town)
- BOOKS (Book#, Book Title, Author Name)
- ISSUED (Book#, User#, Date)

Explain in one English sentence, what each of the following relational algebra queries is designed to determine

a. $\sigma_{\text{User\#}=6}\left(\pi_{\text{User\#, Book Title}}\left((\text{USERS} \bowtie \text{ISSUED}) \bowtie \text{BOOKS}\right)\right)$
b. $\pi_{\text{Author Name}}\left(\text{BOOKS} \bowtie \sigma_{\text{Home Town}=\text{Delhi}}\left(\text{USERS} \bowtie \text{ISSUED}\right)\right)$

gate1996 databases relational-algebra normal

Answer

3.14.5 Relational Algebra: GATE1998_1.33 top http://gateoverflow.in/1670

Given two union compatible relations $R_1(A,B)$ and $R_2(C,D)$, what is the result of the operation $R_1 \bowtie_{A=C \wedge B=D} R_2$?

A. $R_1 \cup R_2$

B. $R_1 \times R_2$

C. $R_1 - R_2$

D. $R_1 \cap R_2$

gate1998 normal relational-algebra

Answer

3.14.6 Relational Algebra: GATE1998_27 top

http://gateoverflow.in/1742

Consider the following relational database schemes:

- COURSES (Cno.name)
- PRE-REQ(Cno, pre-Cno)
- COMPLETED (student_no, Cno)

COURSES gives the number and name of all the available courses.

PRE-REQ gives the information about which courses are pre-requisites for a given course.

COMPLETED indicates what courses have been completed by students

Express the following using relational algebra:

List all the courses for which a student with student_no 2310 has completed all the pre-requisites.

gate1998 databases relational-algebra normal

Answer

3.14.7 Relational Algebra: GATE1999-1.18, ISRO2016-53 top

http://gateoverflow.in/1471

Consider the join of a relation R with a relation S. If R has m tuples and S has n tuples then the maximum and minimum sizes of the join respectively are

A. $m + n$ and 0
B. mn and 0
C. $m + n$ and $|m - n|$
D. mn and $m + n$

gate1999 databases relational-algebra easy isro2016

Answer

3.14.8 Relational Algebra: GATE2000-1.23, ISRO2016-57 top

http://gateoverflow.in/647

Given the relations

- employee (name, salary, dept-no), and
- department (dept-no, dept-name,address),

Which of the following queries cannot be expressed using the basic relational algebra operations $(\sigma, \pi, \times, \bowtie, \cup, \cap, -)$?

A. Department address of every employee
B. Employees whose name is the same as their department name
C. The sum of all employees' salaries
D. All employees of a given department

gate2000 databases relational-algebra easy isro2016

Answer

3.14.9 Relational Algebra: GATE2001-1.24 top

http://gateoverflow.in/717

Suppose the adjacency relation of vertices in a graph is represented in a table Adj (X,Y). Which of the following queries cannot be expressed by a relational algebra expression of constant length?

A. List all vertices adjacent to a given vertex
B. List all vertices which have self loops
C. List all vertices which belong to cycles of less than three vertices
D. List all vertices reachable from a given vertex

gate2001 databases relational-algebra normal

Answer

3.14.10 Relational Algebra: GATE2001-1.25 top

http://gateoverflow.in/718

Let r and s be two relations over the relation schemes R and S respectively, and let A be an attribute in R. The relational algebra expression $\sigma_{A=a}(r \bowtie s)$ is always equal to

A. $\sigma_{A=a}(r)$
B. r
C. $\sigma_{A=a}(r) \bowtie s$
D. None of the above

gate2001 databases relational-algebra difficult

Answer

3.14.11 Relational Algebra: GATE2007-59 top

http://gateoverflow.in/2428

Information about a collection of students is given by the relation $\text{studInfo}(\underline{\text{studId}}, \text{name}, \text{sex})$. The relation $\text{enroll}(\underline{\text{studId}}, \underline{\text{courseId}})$ gives which student has enrolled for (or taken) what course(s). Assume that every course is taken by at least one male and at least one female student. What does the following relational algebra expression represent?

$$\pi_{courceId}\left(\left(\pi_{\text{studId}}\left(\sigma_{sex=\text{"}female\text{"}}\left(\text{studInfo}\right)\right) \times \pi_{courseId}\left(\text{enroll}\right)\right) - \text{enroll}\right)$$

A. Courses in which all the female students are enrolled.
B. Courses in which a proper subset of female students are enrolled.
C. Courses in which only male students are enrolled.
D. None of the above

gate2007 databases relational-algebra normal

Answer

3.14.12 Relational Algebra: GATE2008-68 top

http://gateoverflow.in/491

Let R and S be two relations with the following schema

$$R(\underline{P}, \underline{Q}, R1, R2, R3)$$

$$S(\underline{P}, \underline{Q}, S1, S2)$$

where $\{P, Q\}$ is the key for both schemas. Which of the following queries are equivalent?

I. $\Pi_P(R \bowtie S)$

II. $\Pi_P(R) \bowtie \Pi_P(S)$

III. $\Pi_P(\Pi_{P,Q}(R) \cap \Pi_{P,Q}(S))$

IV. $\Pi_P(\Pi_{P,Q}(R) - (\Pi_{P,Q}(R) - \Pi_{P,Q}(S)))$

A. Only I and II
B. Only I and III
C. Only I, II and III
D. Only I, III and IV

gate2008 databases relational-algebra normal

Answer

3.14.13 Relational Algebra: GATE2015-1_7 top

http://gateoverflow.in/8094

SELECT operation in SQL is equivalent to

A. The selection operation in relational algebra
B. The selection operation in relational algebra, except that SELECT in SQL retains duplicates
C. The projection operation in relational algebra
D. The projection operation in relational algebra, except that SELECT in SQL retains duplicates

gate2015-1 databases sql relational-algebra easy

Answer

3.14.14 Relational Algebra: GATE2017-1-46 top

http://gateoverflow.in/118329

Consider a database that has the relation schema CR(StudentName, CourseName). An instance of the schema CR is as given below.

CR

StudentName	CourseName
SA	CA
SA	CB
SA	CC
SB	CB
SB	CC
SC	CA
SC	CB
SC	CC
SD	CA
SD	CB
SD	CC
SD	CD
SE	CD
SE	CA
SE	CB
SF	CA
SF	CB
SF	CC

The following query is made on the database.

$$T1 \leftarrow \pi_{CourseName} \left(\sigma_{StudentName=SA} \left(CR\right)\right)$$

$$T2 \leftarrow CR \div T1$$

The number of rows in $T2$ is ______________ .

gate2017-1 databases relational-algebra normal numerical-answers

Answer

3.14.15 Relational Algebra: TIFR2010-B-33 top

http://gateoverflow.in/19246

In a relational database there are three relations:

- Customers = C (C Name)
- Shops = S (S Name)
- Buys = B (C Name, S Name)

Then the Relational Algebra expression (Π is the projection operator).

$$C - \Pi_{CName}((C \times S) - B)$$

returns the names of

a. Customers who buy from at least one shop.

b. Customers who buy from at least two shops.
c. Customers who buy from all shops.
d. Customers who do not buy buy anything at all.
e. None of the above.

tifr2010 databases relational-algebra

Answer

3.14.16 Relational Algebra: TIFR2013-B-19 top

http://gateoverflow.in/25872

In a relational database there are three relations:

- Customers = C(CName),
- Shops = S(SName),
- Buys = B(CName, SName).

Which of the following relational algebra expressions returns the names of shops that have no customers at all? [HereΠ is the projection operator.]

a. $\Pi_{SName} B$
b. $S - B$
c. $S - \Pi_{SName} B$
d. $S - \Pi_{SName}((C \times S) - B)$
e. None of the above

tifr2013 databases relational-algebra

Answer

Answers: Relational Algebra

3.14.1 Relational Algebra: GATE1992-13b top

http://gateoverflow.in/43581

Selected Answer

OPTIMIZED ANSWER

$$\pi_{\text{hotel}}\left(\left(\sigma_{\text{customer="Rama"}}(\text{LIKES})\right) * \text{SERVES}\right)$$

9 votes -- Shubham Pandey (6.3k points)

3.14.2 Relational Algebra: GATE1994_13 top

http://gateoverflow.in/2509

Selected Answer

(a)$\pi_{roll\_no.}(\sigma_{cno.=322}$(registered for))

(b)SELECT year,min(age)

FROM students

GROUP BY year

in second question we hav to find year nd youngest student from that year so, we have to applied minn aggregate function on group of year

12 votes -- SAKET NANDAN (4k points)

3.14.3 Relational Algebra: GATE1995_27 top

http://gateoverflow.in/2666

Selected Answer

Same answer as given by Manu Thakur, just translating into relational algebra:

a) $\pi_{pname}\,(publishers)$

---

b) $\pi_{authers.*}\,(\sigma_{book.pname="TECHNICAL\ PUBLISHERS"}\,(book)\ \bowtie\ authers)$

---

c) $\pi_{book.aname}\,(\sigma_{publishers.pcity="Madras"}\,(publishers)\ \bowtie\ book)$

9 votes -- Sheshang M. Ajwalia (2.8k points)

3.14.4 Relational Algebra: GATE1996_27 top

http://gateoverflow.in/2779

Selected Answer

(a) Select the (user# and) titles of the books issued to User# 6
(b) Select author names of the books issued to users whose home town is Delhi

18 votes -- Arjun Suresh (294k points)

3.14.5 Relational Algebra: GATE1998_1.33 top

http://gateoverflow.in/1670

Selected Answer

The join here will be selecting only those tuples where A = C and B = D, meaning it is the intersection. D option.

13 votes -- Arjun Suresh (294k points)

3.14.6 Relational Algebra: GATE1998_27 top

http://gateoverflow.in/1742

SQL query will be

```
SELECT cno
FROM Completed, Pre-Req
WHERE student_no = '2310'
GROUP BY cno
HAVING pre-Cno IN (
    SELECT C.cno
    FROM Completed AS C
    WHERE C.student_no = '2310';
    )
```

3 votes -- Amar Vashishth (28.7k points)

3.14.7 Relational Algebra: GATE1999-1.18, ISRO2016-53 top

http://gateoverflow.in/1471

Selected Answer

B

mn if every row of r matches with each row of s- i.e., the join attribute has the same value in all rows of both r and s,

0 if nothing matches- the join attribute in r and s have no common value.

21 votes -- Anurag Semwal (8k points)

3.14.8 Relational Algebra: GATE2000-1.23, ISRO2016-57 top http://gateoverflow.in/647

Selected Answer

possible solutions , relational algebra

(a) join relation using attribute dpart_no.

Π_{address} (emp ⊠ depart)

or

Π_{address} (σ $_{\text{emp.depart\_no.=depart.depart\_no.}}$ (emp X depat))

(b) Π_{name} (σ $_{\text{emp.depart\_no.=depart.depart\_no. } \wedge \text{ emp.name = depart.depart\_name}}$ (emp X depat))

or

Π_{name} (emp ⊠$_{\text{emp.name = depart.depart\_name}}$ depart)

(d) Let given department number is = 'x'

Π_{name} (σ $_{\text{emp.depart\_no.=depart.depart\_no. } \wedge \text{ depart\_no. = 'x'}}$ (emp X depat))

or

Π_{name} (emp ⊠$_{\text{depart\_no.='x'}}$ depart)

(c) but we can't generate relational algebra of aggregate function using basic operation , so we need extended operation here , option (c) is false .

18 votes -- Mithlesh Upadhyay (5.4k points)

3.14.9 Relational Algebra: GATE2001-1.24 top http://gateoverflow.in/717

Selected Answer

Answer :- D

(A) :-> This is simple select query query.

(B) -> This is simple query we need to check X=Y in where clause.

(C) :-> Cycle < 3 . Means cycle of length 1 & 2. Cycle of length 1 is easy., Same as self loop. Cycle of length 2 is is also not too hard to compute. Though it'll be little complex, will need to do like (X,Y) & (Y, X) both present & X != Y,. We can do this with constant RA query.

(D) :-> This is most hard part. Here we need to find closure of vertices. This willl need kind of loop. If the graph is like skewed tree, our query must loop for O(N) Times. We can't do with constant length query here.

Answer :-> D

12 votes -- Akash (43.8k points)

3.14.10 Relational Algebra: GATE2001-1.25 top http://gateoverflow.in/718

Selected Answer

ans is C.

C is just the better form of query, more execution friendly because requires less memory while joining. query, given in question takes more time and memory while joining.

13 votes -- jayendra (8.1k points)

3.14.11 Relational Algebra: GATE2007-59 top http://gateoverflow.in/2428

Selected Answer

STUDENTINFO
1 A M
2 A F
3 A F

ENROLL

1 C1
1 C2
2 C1
2 C2
3 C2

πstudId(σsex="female"(studInfo))×πcourseId(enroll)

2 C1
*
3 C2

=

2 C1
2 C2
3 C1
3 C2

(πstudId(σsex="female"(studInfo))×πcourseId(enroll))−enroll)
3 C1

πcourceId((πstudId(σsex="female"(studInfo))×πcourseId(enroll))−enroll)

C1..
C1 is course id in which not all girl students enrolled.
i.e. proper subset of girls student appeared..

Hence B is the correct answer .

20 votes -- Digvijay (47k points)

Ans is b,

First it does a cross join between female students id and all course ids, then subtract the entries which are already present in enroll table.

Remaining are the courseids which are **NOT** done by **at least one** female student

19 votes -- Anurag Semwal (8k points)

3.14.12 Relational Algebra: GATE2008-68 top http://gateoverflow.in/491

Selected Answer

(d) i, iii, iv

iv) is expansion for natural join represented with other operators.

Why ii is not equivalent? Consider the following instances of R and S

$$R : \{\langle"1","abc","p1","p2","p3"\rangle, \langle"2","xyz","p1","p2","p3"\rangle\}$$

$S : \{\langle "1", "abc", "q1", "q2", "q3" \rangle \langle "2", "def", "q1", "q2", "q3" \rangle\}$

Now, consider the given queries:

i. $R \bowtie S$ gives

$\{\langle "1", "abc", "p1", "p2", "p3", "q1", "q2", "q3" \rangle\}$

Projecting P gives $\{\langle "1" \rangle\}$

ii. $\pi_P (R) \bowtie \pi_P (S)$ gives

$\{\langle "1" \rangle \langle "2" \rangle\} \bowtie \{\langle "1" \rangle \langle "2" \rangle\}$

$= \{\langle "1", "2" \rangle\}$

iii. $\Pi_P (\Pi_{P,Q} (R) \cap \Pi_{P,Q} (S))$ gives

$\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} \cap \{\langle "1", "abc" \rangle, \langle "2", "def" \rangle\} = \{\langle "1", "abc" \rangle\}$

Projecting P gives $\{\langle "1" \rangle\}$

iv. $\Pi_P (\Pi_{P,Q} (R) - (\Pi_{P,Q} (R) - \Pi_{P,Q} (S)))$ gives

$\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - (\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - \{\langle "1", "abc" \rangle, \langle "2", "def" \rangle\})$

$= \{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - \{\langle "2", "xyz" \rangle\} = \{\langle "1", "abc" \rangle\}$

Projecting P gives $\{\langle "1" \rangle\}$

27 votes -- Aravind (3.3k points)

Natural join is based on the common column**S** of the two tables.
We have 2 common columns in R and S which are **P** and **Q**

Option **1:** Both P and Q are used while doing the join. i.e both P and Q are used to filter.
Option 2**:** Q is **not** used here for filtering. Natural join is done on (all P's from R*and* all P's from S). Clearly different from option 1.

For Option 3 and Option 4, draw a venn diagram and it will be clear that: **R-(R-S) = R $\bigcap$ S**. And both these options use P and Q as filters. So 1,3 and 4 are equivalent.
Option **D** is the answer.

10 votes -- swagnikd (553 points)

3.14.13 Relational Algebra: GATE2015-1_7 top http://gateoverflow.in/8094

Selected Answer

option D is correct because SELECT operation in SQL is equivalent to The projection operation in relational algebra, except that SELECT in SQL retains duplicates but projection gives only distinct

25 votes -- Anoop Sonkar (4.9k points)

3.14.14 Relational Algebra: GATE2017-1-46 top http://gateoverflow.in/118329

Selected Answer

ANS) 4

T1 WILL GIVE**:-**

1.CA
2.CB
3.CC

T2 = CR
÷ **T1**= All the tupples in **CR** which are matched with every tupple in T1

1.SA
2.SC
3.SD
4.SF

//**SB** IS NOT MATCHED WITH **CA** , **SE** IS NOT MATCHED WITH **CC**

11 votes -- jatin saini (2.1k points)

3.14.15 Relational Algebra: TIFR2010-B-33 top

http://gateoverflow.in/19246

Selected Answer

It is division in relational algebra
Division = >
$\Pi_{AB}(R)/\Pi_B(S)$ Results in 'A' values for which here should be 'B' in R for every 'B' of S.

$\Pi_{AB}(R)/\Pi_B(S) = \Pi_A(R) - \Pi_A(\Pi_A(R) \times S - R)$ Retrieve all A's who are related to every B

$C - \Pi_{CName}((C \times S) - B)$

$C \times S$ gives the complete relation of each customer to every shop

$(C \times S) - B)$:gives the relation of the customer which is not related to every shop.

$\Pi_{CName}((C \times S) - B)$: gives the customer name who is not related to every shop.

$C - \Pi_{CName}((C \times S) - B)$: gives the customer who is related to every shop.

Option C) Customers who buy from all shops.

14 votes -- Umang Raman (15.2k points)

lets solve by taking example

Customer

Customer name
A
B
C

Shop

name
1
2

C*S will be possible combinations of customers and shop(cartesian product)

∏name (C*S-B) will give names of customers who do not went to all shop in our example its B and C

now when we C-∏name (C*S-B) we get A as output so output will be name of employees who went to every shop

11 votes -- Pooja Palod (32.4k points)

3.14.16 Relational Algebra: TIFR2013-B-19 top http://gateoverflow.in/25872

Selected Answer

Answer will be (c)

It subtract shopnames to those shop which sells something

So as a result we are getting shops which have no customer

13 votes -- srestha (58.4k points)

3.15 Relational Calculus(25) top

3.15.1 Relational Calculus: GATE1993_23,24 top http://gateoverflow.in/2320

For questions 1 and 2:

The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '*'.

```
Students (rollno*, sname, saddr)
courses (cno*, cname)
enroll(rollno*, cno*, grade)
teach(tno*, tname, cao*)
```

(cno is course number cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

1. Write a SQL query for retrieving roll number and name of students who got A grade in at least one course taught by teacher names Ramesh for the above relational database.
2. For the relational database given above, the following functional dependencies hold:

   rollno $\rightarrow$ sname, sdaddr cno $\rightarrow$ cname

   tno $\rightarrow$ tname rollno, cno $\rightarrow$ grade

   a. Is the database in 3rd normal form (3NF)?
   b. If yes, prove that it is in 3 NF. If not normalize, the relations so that they are in 3NF (without proving)?

gate1993 databases sql relational-calculus normal

Answer

3.15.2 Relational Calculus: GATE1998_2.19 top http://gateoverflow.in/1692

Which of the following query transformations (i.e., replacing the l.h.s. expression by the r.h.s expression) is incorrect? R_1 and R_2 are relations, C_1 and C_2 are selection conditions and A_1 and A_2 are attributes of R_1.

A. $\sigma_{C_1}(\sigma_{C_2}(R_1)) \rightarrow \sigma_{C_2}(\sigma_{C_1}(R_1))$

B. $\sigma_{C_1}(\pi_{A_1}(R_1)) \rightarrow \pi_{A_1}(\sigma_{C_1}(R_1))$

C. $\sigma_{C_1}(R_1 \cup R_2) \rightarrow \sigma_{C_1}(R_1) \cup \sigma_{C_1}(R_2)$

D. $\pi_{A_1}(\sigma_{C_1}(R_1)) \rightarrow \sigma_{C_1}(\pi_{A_1}(R_1))$

gate1998 databases relational-calculus normal

Answer

3.15.3 Relational Calculus: GATE1999_1.19 top

http://gateoverflow.in/1472

The relational algebra expression equivalent to the following tuple calculus expression:

$\{t \mid t \in r \wedge (t[A] = 10 \wedge t[B] = 20)\}$ is

A. $\sigma_{(A=10 \vee B=20)}(r)$
B. $\sigma_{(A=10)}(r) \cup \sigma_{(B=20)}(r)$
C. $\sigma_{(A=10)}(r) \cap \sigma_{(B=20)}(r)$
D. $\sigma_{(A=10)}(r) - \sigma_{(B=20)}(r)$

gate1999 databases relational-calculus normal

Answer

3.15.4 Relational Calculus: GATE2001-2.24 top

http://gateoverflow.in/742

Which of the rational calculus expression is not safe?

A. $\{t \mid \exists u \in R_1 (t[A] = u[A]) \wedge \neg \exists s \in R_2 (t[A] = s[A])\}$
B. $\{t \mid \forall u \in R_1 (u[A] =" x " \Rightarrow \exists s \in R_2 (t[A] = s[A] \wedge s[A] = u[A]))\}$
C. $\{t \mid \neg(t \in R_1)\}$
D. $\{t \mid \exists u \in R_1 (t[A] = u[A]) \wedge \exists s \in R_2 (t[A] = s[A])\}$

gate2001 relational-calculus normal databases

Answer

3.15.5 Relational Calculus: GATE2002-1.20 top

http://gateoverflow.in/825

With regards to the expressive power of the formal relational query languages, which of the following statements is true?

A. Relational algebra is more powerful than relational calculus
B. Relational algebra has the same power as relational calculus
C. Relational algebra has the same power as safe relational calculus
D. None of the above

gate2002 databases relational-calculus normal

Answer

3.15.6 Relational Calculus: GATE2002-15 top

http://gateoverflow.in/868

A university placement center maintains a relational database of companies that interview students on campus and make job offers to those successful in the interview. The schema of the database is given below:

COMPANY(cname, clocation)	STUDENT (scrollno, sname, sdegree)
INTERVIEW (cname, srollno, idate)	OFFER(cname, srollno, osalary

The COMPANY relation gives the name and location of the company. The STUDENT relation gives the student's roll number, name and the degree program for which the student is registered in the university. The INTERVIEW relation gives the date on which a student is interviewed by a company. The OFFER relation gives the salary offered to a student who is successful in a company's interview. The key for each relation is indicated by the underlined attributes

a. Write a **relational algebra** expressions (using only the operator $\sigma, \pi, \cup, -$) for the following queries.
   i. List the rollnumbers and names of students who attended at least one interview but did not receive *any* job offer.
   ii. List the rollnumbers and names of students who went for interviews and received job offers from *every* company with which they interviewed.
b. Write an SQL query to list, for each degree program in which more than five students were offered jobs, the name of the degree and the average offered salary of students in this degree program.

gate2002 databases relational-calculus normal descriptive

Answer

3.15.7 Relational Calculus: GATE2003-30 top

http://gateoverflow.in/920

Consider the following SQL query

Select distinct $a_1, a_2, \dots, a_n$

from $r_1, r_2, \dots, r_m$

where P

For an arbitrary predicate P, this query is equivalent to which of the following relational algebra expressions?

A. $\Pi_{a_1, a_2, \dots a_n} \sigma_p (r_1 \times r_2 \times \dots \times r_m)$
B. $\Pi_{a_1, a_2, \dots a_n} \sigma_p (r_1 \bowtie r_2 \bowtie \dots \bowtie r_m)$
C. $\Pi_{a_1, a_2, \dots a_n} \sigma_p (r_1 \cup r_2 \cup \dots \cup r_m)$
D. $\Pi_{a_1, a_2, \dots a_n} \sigma_p (r_1 \cap r_2 \cap \dots \cap r_m)$

gate2003 databases relational-calculus normal

Answer

3.15.8 Relational Calculus: GATE2004-13 top

http://gateoverflow.in/1010

Let $R_1(\underline{A}, B, C)$ and $R_2(\underline{D}, E)$ be two relation schema, where the primary keys are shown underlined, and let C be a foreign key in R_1 referring to R_2. Suppose there is no violation of the above referential integrity constraint in the corresponding relation instances r_1 and r_2. Which of the following relational algebra expressions would necessarily produce an empty relation?

A. $\Pi_D(r_2) - \Pi_C(r_1)$
B. $\Pi_C(r_1) - \Pi_D(r_2)$
C. $\Pi_D(r_1 \bowtie_{C \neq D} r_2)$
D. $\Pi_C(r_1 \bowtie_{C = D} r_2)$

gate2004 databases relational-calculus easy

Answer

3.15.9 Relational Calculus: GATE2004-14 top

http://gateoverflow.in/1011

Consider the following relation schema pertaining to a students database:

- Students(<u>rollno,</u> name, address)
- Enroll(<u>rollno, courseno</u>, coursename)

where the primary keys are shown underlined. The number of tuples in the student and Enroll tables are 120 and 8 respectively. What are the maximum and minimum number of tuples that can be present in (Student * Enroll), where '*' denotes natural join?

A. 8, 8
B. 120, 8

C. 960, 8
D. 960, 120

gate2004 databases relational-calculus easy

Answer

3.15.10 Relational Calculus: GATE2004-51 top http://gateoverflow.in/1047

Consider the relation Student (name, sex, marks), where the primary key is shown underlined, pertaining to students in a class that has at least one boy and one girl. What does the following relational algebra expression produce? (Note: ρ is the rename operator).

$$\pi_{name} \{r_{sex=female}\ (Student)\} - \pi_{name}\ (Student_{(sex=female \wedge x=male \wedge marks \leq m)}\ \ \rho_{n,x,m}\ (Student))$$

A. names of girl students with the highest marks
B. names of girl students with more marks than some boy student
C. names of girl students with marks not less than some boy students
D. names of girl students with more marks than all the boy students

gate2004 databases relational-calculus normal

Answer

3.15.11 Relational Calculus: GATE2005-30 top http://gateoverflow.in/1366

Let r be a relation instance with schema R = (A, B, C, D). We define $r_1 = \pi_{A,B,C}\,(R)$ and $r_2 = \pi_{A,D}\,(r)$. Let $s = r_1\ *\ r_2$ where $*$ denotes natural join. Given that the decomposition of r into r_1 and r_2 is lossy, which one of the following is TRUE?

A. $s \subset r$

B. $r \cup s = r$

C. $r \subset s$

D. $r^* s = s$

gate2005 databases relational-calculus normal

Answer

3.15.12 Relational Calculus: GATE2005-IT-68 top http://gateoverflow.in/3831

A table 'student' with schema (roll, name, hostel, marks), and another table 'hobby' with schema (roll, hobbyname) contains records as shown below:

Table: Student

Roll	Name	Hostel	Marks
1798	Manoj Rathod	7	95
2154	Soumic Banerjee	5	68
2369	Gumma Reddy	7	86
2581	Pradeep Pendse	6	92
2643	Suhas Kulkarni	5	78
2711	Nitin Kadam	8	72
2872	Kiran Vora	5	92
2926	Manoj Kunkalikar	5	94
2959	Hemant Karkhanis	7	88
3125	Rajesh Doshi	5	82

Table: hobby

Roll	Hobbyname
1798	chess
1798	music
2154	music
2369	swimming

Roll	Hobbyname
2581	cricket
2643	chess
2643	hockey
2711	volleyball
2872	football
2926	cricket
2959	photography
3125	music
3125	chess

The following SQL query is executed on the above tables:

```
select hostel
from student natural join hobby
where marks > = 75 and roll between 2000 and 3000;
```

Relations S and H with the same schema as those of these two tables respectively contain the same information as tuples. A new relation S' is obtained by the following relational algebra operation:

$S' = \Pi_{hostel}((\sigma_{s.roll = H.roll}(\sigma_{marks > 75 \text{ and } roll > 2000 \text{ and } roll < 3000}(S)) X (H))$

The difference between the number of rows output by the SQL statement and the number of tuples in S' is

A. 6
B. 4
C. 2
D. 0

gate2005-it databases sql relational-calculus normal

Answer

3.15.13 Relational Calculus: GATE2006-IT-14 top

http://gateoverflow.in/3553

Consider the relations $r_1(P, Q, R)$ and $r_2(R, S, T)$ with primary keys P and R respectively. The relation r_1 contains 2000 tuples and r_2 contains 2500 tuples. The maximum size of the join $r_1 \bowtie r_2$ is :

A. 2000
B. 2500
C. 4500
D. 5000

gate2006-it databases relational-calculus normal

Answer

3.15.14 Relational Calculus: GATE2006-IT-15 top

http://gateoverflow.in/3554

Which of the following relational query languages have the same expressive power?

I. Relational algebra
II. Tuple relational calculus restricted to safe expressions
III. Domain relational calculus restricted to safe expressions

A. II and III only
B. I and II only
C. I and III only
D. I, II and III

gate2006-it databases relational-algebra relational-calculus easy

Answer

3.15.15 Relational Calculus: GATE2007-60 top

http://gateoverflow.in/1258

Consider the relation **employee**(name, sex, supervisorName) with *name* as the key, *supervisorName* gives the name of the supervisor of the employee under consideration. What does the following Tuple Relational Calculus query produce?

$$\{e.name \mid employee(e) \wedge (\forall x)\,[\neg employee\,(x) \vee x.supervisorName \neq e.name \vee x.sex = \text{"male"}]\}$$

A. Names of employees with a male supervisor.
B. Names of employees with no immediate male subordinates.
C. Names of employees with no immediate female subordinates.
D. Names of employees with a female supervisor.

gate2007 databases relational-calculus normal

Answer

3.15.16 Relational Calculus: GATE2007-IT-68 top http://gateoverflow.in/3513

Consider the following relation schemas :

- b-Schema = (b-name, b-city, assets)
- a-Schema = (a-num, b-name, bal)
- d-Schema = (c-name, a-number)

Let branch, account and depositor be respectively instances of the above schemas. Assume that account and depositor relations are much bigger than the branch relation.

Consider the following query:

$\Pi_{\text{c-name}}\ (\sigma_{\text{b-city = "Agra"} \wedge \text{ bal < 0}}\ (\text{branch} \bowtie (\text{account} \bowtie \text{depositor})$

Which one of the following queries is the most efficient version of the above query ?

A. $\Pi_{\text{c-name}}\ (\sigma_{\text{bal < 0}}\ (\sigma_{\text{b-city = "Agra"}}\ \text{branch} \bowtie \text{account}) \bowtie \text{depositor})$
B. $\Pi_{\text{c-name}}\ (\sigma_{\text{b-city = "Agra"}}\ \text{branch} \bowtie (\sigma_{\text{bal < 0}}\ \text{account} \bowtie \text{depositor}))$
C. $\Pi_{\text{c-name}}\ ((\sigma_{\text{b-city = "Agra"}}\ \text{branch} \bowtie \sigma_{\text{b-city = "Agra"} \wedge \text{ bal < 0}}\ \text{account}) \bowtie \text{depositor})$
D. $\Pi_{\text{c-name}}\ (\sigma_{\text{b-city = "Agra"}}\ \text{branch} \bowtie (\sigma_{\text{b-city = "Agra"} \wedge \text{ bal < 0}}\ \text{account} \bowtie \text{depositor}))$

gate2007-it databases relational-calculus normal

Answer

3.15.17 Relational Calculus: GATE2008-15 top http://gateoverflow.in/413

Which of the following tuple relational calculus expression(s) is/are equivalent to $\forall t \in r\,(P\,(t))$?

I. $\neg \exists t \in r\,(P\,(t))$
II. $\exists t \notin r\,(P\,(t))$
III. $\neg \exists t \in r\,(\neg P\,(t))$
IV. $\exists t \notin r\,(\neg P\,(t))$

A. I only
B. II only
C. III only
D. III and IV only

gate2008 databases relational-calculus normal

Answer

3.15.18 Relational Calculus: GATE2008-IT-75 top http://gateoverflow.in/3389

Student (school-id, sch-roll-no, sname, saddress)
School (school-id, sch-name, sch-address, sch-phone)
Enrolment(school-id sch-roll-no, erollno, examname)
ExamResult(erollno, examname, marks)

Consider the following tuple relational calculus query.
{t | ∃ E ∊ Enrolment t = E.school-id ∧
| {x | x ∊ Enrolment ∧ x.school-id = t ∧
(∃ B ∊ ExamResult B.erollno = x.erollno ∧ B.examname = x.examname ∧ B.marks > 35)}| /

| {x | x ∈ Enrolment ∧ x.school-id = t}| * 100 > 35}

If a student needs to score more than 35 marks to pass an exam, what does the query return?

A. The empty set
B. schools with more than 35% of its students enrolled in some exam or the other
C. schools with a pass percentage above 35% over all exams taken together
D. schools with a pass percentage above 35% over each exam

gate2008-it databases relational-calculus normal

Answer

3.15.19 Relational Calculus: GATE2009-45 top http://gateoverflow.in/1331

Let R and S be relational schemes such that R={a,b,c} and S={c}. Now consider the following queries on the database:

1. $\pi_{R-S}(r) - \pi_{R-S}\left(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r)\right)$

2. $\{t \mid t \in \pi_{R-S}(r) \land \forall u \in s\left(\exists v \in r\left(u = v[S] \land t = v\left[R-S\right]\right)\right)\}$

3. $\{t \mid t \in \pi_{R-S}(r) \land \forall v \in r\left(\exists u \in s\left(u = v[S] \land t = v\left[R-S\right]\right)\right)\}$

4.

```
Select R.a,R.b
    From R,S
    Where R.c = S.c
```

Which of the above queries are equivalent?

A. 1 and 2
B. 1 and 3
C. 2 and 4
D. 3 and 4

gate2009 databases relational-calculus difficult

Answer

3.15.20 Relational Calculus: GATE2012-50 top http://gateoverflow.in/2180

Consider the following relations A, B and C:

A

Id	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B

Id	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C

Id	Phone	Area
10	2200	02
99	2100	01

How many tuples does the result of the following relational algebra expression contain? Assume that the schema of $A \cup B$ is the same as that of A.

$$(A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C$$

A. 7
B. 4
C. 5
D. 9

gatc2012 databases sql relational-calculus normal

Answer

3.15.21 Relational Calculus: GATE2012-51 top

http://gateoverflow.in/43313

Consider the following relations A, B and C:

A		
Id	**Name**	**Age**
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
Id	**Name**	**Age**
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
Id	**Phone**	**Area**
10	2200	02
99	2100	01

How many tuples does the result of the following SQL query contain?

```
SELECT A.Id
FROM A
WHERE A.Age > ALL (SELECT B.Age
                   FROM B
                   WHERE B.Name = 'Arun')
```

A. 4
B. 3
C. 0
D. 1

gate2012 databases sql relational-calculus normal

Answer

3.15.22 Relational Calculus: GATE2012_43 top http://gateoverflow.in/2151

Suppose $R_1(\underline{A}, B)$ and $R_2(\underline{C}, D)$ are two relation schemas. Let r_1 and r_2 be the corresponding relation instances. B is a foreign key that refers to C in R_2. If data in r_1 and r_2 satisfy referential integrity constraints, which of the following is **ALWAYS TRUE**?

(A) $\prod_B(r_1) - \prod_C(r_2) = \varnothing$
(B) $\prod_C(r_2) - \prod_B(r_1) = \varnothing$
(C) $\prod_B(r_1) = \prod_C(r_2)$
(D) $\prod_B(r_1) - \prod_C(r_2) \neq \varnothing$

gate2012 databases relational-calculus normal

Answer

3.15.23 Relational Calculus: GATE2013_35 top http://gateoverflow.in/1546

Consider the following relational schema.

- Students(rollno: integer, sname: string)
- Courses(courseno: integer, cname: string)
- Registration(rollno: integer, courseno: integer, percent: real)

Which of the following queries are equivalent to this query in English?

"Find the distinct names of all students who score more than 90% in the course numbered 107"

(I)

```
SELECT DISTINCT S.sname
FROM Students as S, Registration as R
WHERE R.rollno=S.rollno AND R.courseno=107 AND R.percent >90
```

(II) $\prod_{sname}\left(\sigma_{courseno=107 \wedge percent>90}\ (Registration \bowtie Students)\right)$

(III)
$\{T \mid \exists S \in Students, \exists R \in Registration(S.rollno = R.rollno \wedge R.courseno = 107 \wedge R.percent > 90 \wedge T.sname = S.$

(IV) $\{\langle S_N\rangle \mid \exists S_R \exists R_P (\langle S_R, S_N\rangle \in Students \wedge \langle S_R, 107, R_P\rangle \in Registration \wedge R_P > 90)\}$

(A) I, II, III and IV

(B) I, II and III only

(C) I, II and IV only

(D) II, III and IV only

gate2013 databases sql relational-calculus normal

Answer

3.15.24 Relational Calculus: GATE2014-3-21 top

http://gateoverflow.in/2055

What is the optimized version of the relation algebra expression $\pi_{A1}(\pi_{A2}(\sigma_{F1}(\sigma_{F2}(r))))$, where $A1, A2$ are sets of attributes in r with $A1 \subset A2$ and $F1, F2$ are Boolean expressions based on the attributes in r?

A. $\pi_{A1}\left(\sigma_{(F1 \wedge F2)}(r)\right)$
B. $\pi_{A1}\left(\sigma_{(F1 \vee F2)}(r)\right)$
C. $\pi_{A2}\left(\sigma_{(F1 \wedge F2)}(r)\right)$
D. $\pi_{A2}\left(\sigma_{(F1 \vee F2)}(r)\right)$

gate2014-3 databases relational-calculus easy

Answer

3.15.25 Relational Calculus: GATE2014-3-30 top

http://gateoverflow.in/2064

Consider the relational schema given below, where **eId** of the relation **dependent** is a foreign key referring to **empId** of the relation **employee**. Assume that every employee has at least one associated dependent in the **dependent** relation.

employee (empId, empName, empAge)

dependent(depId, eId, depName, depAge)

Consider the following relational algebra query:

$$\Pi_{empId}\ (employee) - \Pi_{empId}\ (employee \bowtie_{(empId=eID)\wedge(empAge\leq depAge)}\ dependent)$$

The above query evaluates to the set of **empId**s of employees whose age is greater than that of

A. some dependent.
B. all dependents.
C. some of his/her dependents.
D. all of his/her dependents.

gate2014-3 databases relational-calculus normal

Answer

Answers: Relational Calculus

3.15.1 Relational Calculus: GATE1993_23,24 top

http://gateoverflow.in/2320

23) select student.rollno,student.sname

from student natural join enroll on student.rollno=enroll.rollno

where enroll.grade='A' AND enroll.cno in (select cno from teach where tname='Ramesh')

24) In teach relation cno(non prime attribute) does not depend upon any super key

so split them like

teach1(tno,tnaem)

teach2(tno,cno)

9 votes -- Aravind (3.3k points)

3.15.2 Relational Calculus: GATE1998_2.19 top http://gateoverflow.in/1692

Selected Answer

D) if the selection condition is on attribute A2, then we cannot replace it by RHS as there will not be any attribute A2 due to projection of A1 only.

23 votes -- Shaun Patel (6.9k points)

3.15.3 Relational Calculus: GATE1999_1.19 top http://gateoverflow.in/1472

Selected Answer

Answer: C

Tuple t should have two attributes A and B such that t.A = 10 and t.B = 20.

So, (Tuples having A = 10) ∩ (Tuples having B = 20) = (Tuples having A = 10 and B = 20).

11 votes -- Rajarshi Sarkar (35k points)

3.15.4 Relational Calculus: GATE2001-2.24 top http://gateoverflow.in/742

Selected Answer

Answer: C

It returns tuples not belonging to R1 (which is infinitely many). So, it is not safe.

Ref: http://nptel.ac.in/courses/IIT-MADRAS/Intro_to_Database_Systems_Design/pdf/3.1_Tuple_Relational_Calculus.pdf

12 votes -- Rajarshi Sarkar (35k points)

3.15.5 Relational Calculus: GATE2002-1.20 top http://gateoverflow.in/825

Selected Answer

Answer: C

Relational algebra has the same power as safe relational calculus as:

- A query can be formulated in safe Tuple Relational Calculus if and only if it can be formulated in Relational Algebra.
- A query can be formulated in Relational Algebra if and only if it can be formulated in safe Tuple Relational Calculus.

16 votes -- Rajarshi Sarkar (35k points)

3.15.6 Relational Calculus: GATE2002-15 top http://gateoverflow.in/868

Answer a) part i)

$\prod_{srollno,sname} (\sigma_{student.srollno=interview.srollno}$ (Student ⋈ Interview)) − $\prod_{srollno,sname} (\sigma_{srollno=offer.srollno}$ (Offer ⋈ Student))

Answer part ii)

Temp = $\prod_{srollno,cname}$ (Interview) − $\prod_{srollno,cname}$ (Offer)

Temp will store those students roll no who where interviewed but still did not get the job atleast in some companies.

Temp1 = $\prod_{srollno}$ {$\sigma_{student.srollno=Interview.srollno \wedge student.srollno=offer.srollno \wedge offer.cname=Interview.cname}$ (Student ⋈ Interview ⋈ Offer) }

Temp1 will contain all those students who appeared for interview into different companies and their interview turned into offer letters .

Answer : Temp1 − $\prod_{srollno}$ (Temp)

This will result in students who got the job in all the companies they sat for interview .

Answer part b)

Select sdegree , avg(salary) from student , Offer where Student.srollno = Offer.srollno group by sdegree having count(distinct student.srollno) > 5

6 votes -- Riya Roy(Arayana) (7.1k points)

3.15.7 Relational Calculus: GATE2003-30 top

http://gateoverflow.in/920

Selected Answer

select distinct in SQL is equivalent to project and by default relation 1, relation 2 in SQL corresponds to cross-product. So, option A.

17 votes -- Arjun Suresh (294k points)

3.15.8 Relational Calculus: GATE2004-13 top

http://gateoverflow.in/1010

Selected Answer

ans (B)

C in R1 is a foreign key referring to the primary key D in R2. So, every element of C must come from some D element.

15 votes -- Vicky Bajoria (4.9k points)

3.15.9 Relational Calculus: GATE2004-14 top

http://gateoverflow.in/1011

Selected Answer

Rollno in students is key, ans students table has 120 tuples, In Enroll table rollno is FK referencing to Students table. in natural join it'll return the records where the rollno value of enroll matches with the rollno of students so in both conditions min and max records will be resulted (8,8).
hence A is the answer.

Hint: table which has non-key, no of records of that will be resulted.

16 votes -- Manu Thakur (6k points)

3.15.10 Relational Calculus: GATE2004-51 top

http://gateoverflow.in/1047

Selected Answer

OPTION : (d)

The following query states the following conditions :-

$$\boxed{\begin{array}{l} sex = Female \wedge \\ x = Male \wedge \\ Marks \le m \end{array}}$$

Let the relation student (Name, Sex, Marks)

Name	Sex	Marks
S1	Female	30
S2	Female	10
S3	Male	20

Student (Name, Sex, Marks) Relation is renamed as student (n, x, m).

Taking cross product of the relations

Name	Sex	Marks	n	x	m
S1	Female	30	S1	Female	30
S1	Female	30	S2	Female	10
S1	Female	30	S3	Male	20
S2	Female	10	S1	Female	30
S2	Female	10	S2	Female	10
S2	Female	10	S3	Male	20
S3	Male	20	S1	Female	30
S3	Male	20	S2	Female	10
S3	Male	20	S3	Male	20

selecting the tuple which satisfy the condition i.e

$$\boxed{\begin{array}{l} sex = Female \wedge \\ x = Male \wedge \\ Marks \le m \end{array}}$$

PROJECTING : $\pi_{name} = \boxed{S2}$

$$\pi_{name}\left[\sigma_{sex=female}(Student)\right] = \boxed{\begin{array}{c} S1 \\ S2 \end{array}}$$

Hence the query:

$$\pi_{name}\left[\sigma_{sex=female}(student)\right] - \pi_{name}\left[student \bowtie_{\substack{sex=female \wedge \\ x=male \wedge \\ marks \le m}} \sigma_{n,x,m}(student)\right]$$

$$\boxed{\begin{array}{c} S1 \\ S2 \end{array}} - \boxed{S2} = \boxed{S1}$$

Let us take another relation data of student (Name, sex, marks)

Name	Sex	Marks
S1	M	100
S2	F	50
S3	M	40
S4	F	30

→ Highest ~~maks~~ marks of Male students

→ Highest mark of female students.

Taking cross product :

Name	Sex	Marks	n	x	m
S1	M	100	S1	M	100
S1	M	100	S2	F	50
S1	M	100	S3	M	40
S1	M	100	S4	F	30
S2	F	50	S1	M	100
S2	F	50	S2	F	50
S2	F	50	S3	M	40
S2	F	50	S4	F	30
S3	M	100	S1	M	100
S3	M	100	S2	F	50
S3	M	100	S3	M	40
S3	M	100	S4	F	30
S4	F	50	S1	M	100
S4	F	50	S2	F	50
S4	F	50	S3	M	40
S4	F	50	S4	F	30

$\Rightarrow \boxed{\begin{array}{c} S2 \\ S4 \end{array}}$ $\Downarrow$

female students who scored less than equal to some male students

$$\pi_{name}\left[\sigma_{sex=female}(student)\right] = \boxed{\begin{array}{c} S2 \\ S4 \end{array}}$$

Hence, the result of the query will be :

$$\boxed{\begin{array}{c} S2 \\ S4 \end{array}} - \boxed{\begin{array}{c} S2 \\ S4 \end{array}} = \text{empty relation}$$

From the above relational data of table student (Name, Sex, Marks)

(d) is the correct option

In short,

$\{>= All\} = |universal| - |< some\ male|$

$\{> All\} = |universal| - |<= some\ male|$

$\{>= some\} = |universal| - |< all\ male|$

Source : http://www.edugrabs.com/questions-based-on-relational-algebra/

26 votes -- pC (21.4k points)

3.15.11 Relational Calculus: GATE2005-30 top http://gateoverflow.in/1366

Selected Answer

Answer is **C.** $r \subset s$

R

A	**B**	**C**	**D**
1	2	3	3
1	5	3	4

R1

A	**B**	**C**
1	2	3
1	5	3

R2

A	**D**
1	3
1	4

S = R1 * R2

A	**B**	**C**	**D**
1	**2**	**3**	**3**
1	2	3	4
1	5	3	3
1	**5**	**3**	**4**

Red color rows of S are present in R so $R \subset S$

and one more result R * S = R.

23 votes -- Vikrant Singh (13.4k points)

3.15.12 Relational Calculus: GATE2005-IT-68 top http://gateoverflow.in/3831

Selected Answer

Sql query will return

Roll	**Hostel**
2369	7
2581	6
2643	5
2643	5 Duplicate Row is present in Hobby table
2872	5
2926	5
2959	7

Total 7 rows are selected.

In RA only distinct values of hostels are selected i.e. 5,6,7

SQL row count - RA row count = 7 - 3 = 4

Answer is **B**

27 votes -- Vikrant Singh (13.4k points)

3.15.13 Relational Calculus: GATE2006-IT-14 top

http://gateoverflow.in/3553

Selected Answer

the common attribute is R and it is primary key in the second relation. hence the R value is distinct for 2500 rows. hence when we join max possible number of tuples is 2000

option A

15 votes -- Sankaranarayanan P.N (11.2k points)

3.15.14 Relational Calculus: GATE2006-IT-15 top

http://gateoverflow.in/3554

Selected Answer

Answer: D

All are equivalent in expressive power.

14 votes -- Rajarshi Sarkar (35k points)

3.15.15 Relational Calculus: GATE2007-60 top

http://gateoverflow.in/1258

Selected Answer

Query is selecting e such that e is an employee and for all x, either x is not an employee or x's supervisor's name is not e.name or x is male.

So, this is equivalent to saying, select all employees who don't have an immediate female subordinate. (Assuming there is no transgender). (C) option.

21 votes -- Arjun Suresh (294k points)

OR ($\vee$) is commutative and associative, therefore i can rewrite given query as:

$$\{e.name \mid employee(e) \wedge (\forall x)\left[\neg employee\left(x\right) \vee x.sex = \text{``}male\text{''} \vee x.supervisorName \neq e.name\right]\}$$

$$\{e.name \mid employee(e) \wedge (\forall x)\left[\neg (employee\left(x\right) \wedge x.sex \neq \text{``}male\text{''}) \vee x.supervisorName \neq e.name\right]\}$$

$$\{e.name \mid employee(e) \wedge (\forall x)\left[(employee\left(x\right) \wedge x.sex \neq \text{``}male\text{''}) \Rightarrow x.supervisorName \neq e.name\right]\}$$

$$\{e.name \mid employee(e) \wedge (\forall x)\left[(employee\left(x\right) \wedge x.sex = \text{``}female\text{''}) \Rightarrow x.supervisorName \neq e.name\right]\}$$

It is clear now they are saying something about female employees, This query does not say anything about male employees. Therefore Option A and B are out of consideration.

This query retrieves those $e.name$ who satisfies this condition:

\forall x\right)\left[(employee\left(x \right) \wedge x.sex =``female") \Rightarrow x.supervisorName \neq e.name \right]\right\}

Means retrieves those e.name, who is not a supervisor of any female employees.
i.e it retrieves name of employees with no female subordinate.
(here "immediate" is obvious, as we are checking first level supervisor.)

Hence Option C.

19 votes -- Sachin Mittal (7.1k points)

3.15.16 Relational Calculus: GATE2007-IT-68 top

http://gateoverflow.in/3513

Selected Answer

It should be A. As in B we are doing a join between two massive table whereas in A we are doing join between relatively smaller table and larger one and the output that this inner table gives (which is smaller in comparison to joins that we are doing in B) is used for join with depositer table with the selection condition.

Options C and D are invalid as there is no b-city column in a-Schema.

Lets see in detail. Let there be 100 different branches. Say about 10% of accounts are below 0. Also, let there be 10,000 accounts in a branch amounting to 1,000,000 total accounts. A customer can have multiple accounts, so let there be on average 2 accounts per customer. So, this amounts to 2,000,000 total entries in depositor table. Lets assume these assumptions are true for all the branches. So, now lets evaluate options A and B.

1. All the accounts in Agra branch, filter by positive balance, and then depositor details of them. So,

- Get branch name from branch table after processing 100 records
- Filter 10,000 accounts after processing 1,000,000 accounts belonging to Agra
- Filter 1000 accounts after processing 10,000 accounts for positive balance
- Get 500 depositor details after processing 2,000,000 entries for the given 1000 accounts (asuming 1 customer having 2 accounts). So, totally this amounts to 2,000,000,000 record processing.
- So totally $\approx$ 2 billion records needs processing.

2. All the positive balance accounts are found first, and then those in Agra are found.

- Filter 100,000 accounts after processing 1,000,000 accounts having positive balance
- Find the deposito details of these accounts. So, 100,000 * 2,000,000 records need processing and this is a much larger value than for query A. Even if we reduce the percentage of positive balance (10 we assumed) the record processing of query A will also get reduced by same rate. So, overall query A is much better than query B.

24 votes -- Shaun Patel (6.9k points)

3.15.17 Relational Calculus: GATE2008-15 top

http://gateoverflow.in/413

Selected Answer

Only III is correct.
The given statement means for all tuples from r, P is true. III means there does not exist a tuple in r where P is not true. Both are equivalent.

IV is not correct as it as saying that there exist a tuple, not in r for which P is not true, which is not what the given expression means.

23 votes -- Arjun Suresh (294k points)

3.15.18 Relational Calculus: GATE2008-IT-75 top

http://gateoverflow.in/3389

{t | ∃ E ∊ Enrolment t = E.school-id ∧
| {x | x ∊ Enrolment ∧ x.school-id = t ∧

(∃ B ∊ ExamResult B.erollno = x.erollno ∧ B.examname = x.examname ∧ B.marks > 35)}

In this first query it is picking up tuple of the student who Enroll in some exam and who got >35 marks in that exam

{x | x ∊ Enrolment ∧ x.school-id = t}| * 100 > 35}

in second part of the query **t** is tuples of first query and x is their enrollment , and enrollment >35%

So,The query returns the tuples where 35% students enrolled and all of them got >35 marks in some exam

B) division will pick 35% enrollment of the student in **some exams**

5 votes -- srestha (58.4k points)

3.15.19 Relational Calculus: GATE2009-45 top

http://gateoverflow.in/1331

Selected Answer

1. $\pi_{R-S}(r) - \pi_{R-S}\left(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r)\right)$

= $\pi_{a,b}(r) - \pi_{a,b}\left(\pi_{a,b}(r) \times s - \pi_{R}(r)\right)$
= (r/s)

2. Expanding logically the statement means to select t (a,b) from r such that for all tuples u in s, there is a tuple v in r, such that u = v[S] and t = v[R-S]. This is just equivalent to

$$(r/s)$$

3. Expanding logically the statement means that select t (a,b) from r such that for all tuples v in r, there is a tuple u in s, such that u = v[S] and t = v[R-S]. This is equivalent to saying to select (a,b) values from r, where the c value is in some tupe of s.

4. This selects (a,b) from all tuples from r which has an equivalent c value in s.

So, 1 and 2 are equivalent

r

a	b	c
Arj	TY	12
Arj	TY	14
Cell	TR	13
Tom	TW	12
Ben	TE	14

s

c
12
14

1. will give <Arj, TY>
2. will give <Arj, TY>
3. will not return any tuple as the c value 13, is not in s.
4. will give <Arj, TY>, <Arj, TY>, Tom, TW>, <Ben, TE>

http://pages.cs.wisc.edu/~dbbook/openAccess/firstEdition/slides/pdfslides/mod3l1.pdf

25 votes -- Arjun Suresh (294k points)

3.15.20 Relational Calculus: GATE2012-50 top

http://gateoverflow.in/2180

Selected Answer

50. For C.ID = 10, all tuples from $A \cup B$ satisfies the join condition, hence 5 tuples (union of A and B has only 5 tuples are 2 of them are repeating for Shreya and Rohit) will be returned. Now, for C.ID = 99, A.ID = 99 and A.ID = 98 (for A.ID = 98, we need to assume A ∪ B, has the same schema s A as told in the question) satisfies the condition A.ID>40, and hence two tuples are returned. So, number of tuples = 5 + 2 = 7.

The output will be:

```
Id   Name    Age  Id   Phone  Area
---------------------------------
12   Arun    60   10   2200   02
15   Shreya  24   10   2200   02
99   Rohit   11   10   2200   02
25   Hari    40   10   2200   02
98   Rohit   20   10   2200   02
99   Rohit   11   99   2100   01
98   Rohit   20   99   2100   01
```

17 votes -- Arjun Suresh (294k points)

3.15.21 Relational Calculus: GATE2012-51 top http://gateoverflow.in/43313

Selected Answer

51. <cond> ALL evaluates to TRUE if inner query returns no tuples. So, Number of tuples returned will be number of tuples in A = 3.

Ref: http://dcx.sap.com/1200/en/dbusage/all-test-quantified-subquery.html

13 votes -- Arjun Suresh (294k points)

3.15.22 Relational Calculus: GATE2012_43 top http://gateoverflow.in/2151

Selected Answer

(a)

Referential integrity means, all the values in foreign key should be present in primary key

r2(c) is the super set of r1(b)

so {subset - superset} is always empty set

19 votes -- Aravind (3.3k points)

3.15.23 Relational Calculus: GATE2013_35 top http://gateoverflow.in/1546

Selected Answer

Answer: A

Four queries given in SQL, RA, TRC and DRC in four statements respectively retrieve the required information.

15 votes -- Rajarshi Sarkar (35k points)

3.15.24 Relational Calculus: GATE2014-3-21 top http://gateoverflow.in/2055

Selected Answer

(A) $\pi_{A1}(\sigma_{(F1 \wedge F2)}(r))$

since A1 is subset of A2 will get only A1 attributes as it is in the outside, so we can remove project A2.

Two Selects with boolean expression can be combined into one select with And of two boolean expressions.

20 votes -- Aravind (3.3k points)

3.15.25 Relational Calculus: GATE2014-3-30 top http://gateoverflow.in/2064

Selected Answer

(D) all of his/her dependents.

The inner query selects the employees whose age is less than or equal to at least one of his dependents. So, subtracting from the set of employees, gives employees whose age is greater than all of his dependents.

25 votes -- Arjun Suresh (294k points)

3.16 Safe Query(1) top

3.16.1 Safe Query: GATE2017-1-41 top http://gateoverflow.in/118324

Consider a database that has the relation schemas EMP(EmpId, EmpName, DeptId), and DEPT(DeptName, DeptId). Note that the DeptId can be permitted to be NULL in the relation EMP. Consider the following queries on the database expressed in tuple relational calculus.

(I) $\{t$ | ∃u ∈ EMP(t[EmpName] = u[EmpName] ∧ ∀v ∈ DEPT(t[DeptId] ≠ v[DeptId]))}

(II) $\{t$ | ∃u ∈ EMP(t[EmpName] = u[EmpName] ∧ ∃v ∈ DEPT(t[DeptId] ≠ v[DeptId]))}

(III) $\{t$ | ∃u ∈ EMP(t[EmpName] = u[EmpName] ∧ ∃v ∈ DEPT(t[DeptId] = v[DeptId]))}

Which of the above queries are safe?

(A) (I) and (II) only.

(B) (I) and (III) only.

(C) (II) and (III) only.

(D) (I), (II) an(III).

gate2017-1 databases relational-calculus safe-query normal

Answer

Answers: Safe Query

3.16.1 Safe Query: GATE2017-1-41 top http://gateoverflow.in/118324

Selected Answer

Ans should be D) as all the bounded variables are tied with one specific Emp and Dept table and does not range over the universe

5 votes -- yg92 (2.3k points)

3.17 Sql(37) top

3.17.1 Sql: GATE 2016-2-52 top http://gateoverflow.in/39604

Consider the following database table named water_schemes:

Water_schemes		
scheme_no	district_name	capacity
1	Ajmer	20
1	Bikaner	10
2	Bikaner	10
3	Bikaner	20
1	Churu	10
2	Churu	20
1	Dungargarh	10

The number of tuples returned by the following SQL query is __________.

```
with total (name, capacity) as
    select district_name, sum (capacity)
    from water_schemes
    group by district_name
with total_avg (capacity) as
   select avg (capacity)
   from total
select name
   from total, total_avg
   where total.capacity ≥ total_avg.capacity
```

gate2016-2 databases sql normal numerical-answers

Answer

3.17.2 Sql: GATE1990-10a top

http://gateoverflow.in/85686

Consider the following relational database:

- employees (eno, ename, address, basic-salary)
- projects (pno, pname, nos-of-staffs-allotted)
- working (pno, eno, pjob)

The queries regarding data in the above database are formulated below in SQL. Describe in english sentences the two queries that have been posted:

(i)

```
SELECT ename
FROM employees
WHERE eno IN
    (SELECT eno
    FROM working
    GROUP BY eno
    HAVING COUNT(*)=
        (SELECT COUNT(*)
        FROM projects))
```

(ii)

```
SELECT pname
FROM projects
WHERE pno IN
    (SELECT pno
    FROM projects
    MINUS
    SELECT DISTINCT pno
    FROM working);
```

gate1990 descriptive databases sql

Answer

3.17.3 Sql: GATE1991_12,a top

http://gateoverflow.in/539

Suppose a database consist of the following relations:

```
SUPPLIER (SCODE,SNAME,CITY).

PART (PCODE,PNAME,PDESC,CITY).

PROJECTS (PRCODE,PRNAME,PRCITY).

SPPR (SCODE,PCODE,PRCODE,QTY).
```

a. Write SQL programs corresponding to the following queries:
   i. Print PCODE values for parts supplied to any project in DEHLI by a supplier in DELHI.
   ii. Print all triples <CITY, PCODE, CITY> such that a supplier in first city supplies the specified part to a project in the second city, but do not print the triples in which the two CITY values are same.

gate1991 databases sql normal

Answer

3.17.4 Sql: GATE1997_76 top http://gateoverflow.in/19838

Consider the following relational database schema:

EMP (eno name, age)

PROJ (pno name)

INVOLVED (eno, pno)

EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

a. What is the relational algebra expression containing one or more of $\{\sigma, \pi, x, u, -\}$ which is equivalent to SQL query.

```
select eno  from EMP|INVOLVED where EMP.eno=INVOLVED.eno  and INVOLVED.pno=3
```

b. State in English (in not more than 15 words)

   What the following relational algebra expressions are designed to determine

   i. $\pi_{eno}(INVOLVED) - \pi_{eno}((\pi_{eno}(INVOLVED) \times \pi_{pno}(PROJ) - INVOLVED)$
   ii. $\pi_{age}(EMP) - \pi_{Eage} < EMP.age(\rho E(EMP) \times EMP))$

(Note: $\rho E(EMP)$ conceptually makes a copy of EMP and names it K (ρ is called the rename operator))

gate1997 databases sql

Answer

3.17.5 Sql: GATE1998_7a top http://gateoverflow.in/1721

Suppose we have a database consisting of the following three relations.

- $\text{FREQUENTS (student, parlor)}$ giving the parlors each student visits.
- $\text{SERVES (parlor, ice-cream)}$ indicating what kind of ice-creams each parlor serves.
- $\text{LIKES (student, ice-cream)}$ indicating what ice-creams each student likes.

(Assume that each student likes at least one ice-cream and frequents at least one parlor)

Express the following in SQL:

Print the students that frequent at least one parlor that serves some ice-cream that they like.

gate1998 databases sql descriptive

Answer

3.17.6 Sql: GATE1999_2.25 top http://gateoverflow.in/1502

Which of the following is/are correct?

A. An SQL query automatically eliminates duplicates
B. An SQL query will not work if there are no indexes on the relations
C. SQL permits attribute names to be repeated in the same relation
D. None of the above

gate1999 databases sql easy

Answer

3.17.7 Sql: GATE1999_22 top http://gateoverflow.in/1521

Consider the set of relations

- EMP (Employee-no. Dept-no, Employee-name, Salary)
- DEPT (Dept-no. Dept-name, Location)

Write an SQL query to:

a. Find all employees names who work in departments located at 'Calcutta' and whose salary is greater than Rs.50,000.

b. Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000

gate1999 databases sql easy

Answer

3.17.8 Sql: GATE2000-2.25 top http://gateoverflow.in/672

Given relations r(w, x) and s(y, z) the result of

```
select distinct w, x
from r, s
```

is guaranteed to be same as r, provided.

A. r has no duplicates and s is non-empty
B. r and s have no duplicates
C. s has no duplicates and r is non-empty
D. r and s have the same number of tuples

gate2000 databases sql

Answer

3.17.9 Sql: GATE2000-2.26 top http://gateoverflow.in/673

In SQL, relations can contain null values, and comparisons with null values are treated as unknown. Suppose all comparisons with a null value are treated as false. Which of the following pairs is not equivalent?

A. x = 5 not (not (x = 5))
B. x = 5 x > 4 and x < 6, where x is an integer
C. x ≠ 5 not (x = 5)
D. none of the above

gate2000 databases sql normal

Answer

3.17.10 Sql: GATE2001-2.25 top http://gateoverflow.in/743

Consider a relation geq which represents "greater than or equal to", that is, $(x, y) \in$ geq only if $y \geq x$.

```
create table geq
(
    ib integer not null,
    ub integer not null,
    primary key ib,
    foreign key (ub) references geq on delete cascade
);
```

Which of the following is possible if tuple (x,y) is deleted?

A. A tuple (z,w) with z > y is deleted
B. A tuple (z,w) with z > x is deleted
C. A tuple (z,w) with w < x is deleted
D. The deletion of (x,y) is prohibited

gate2001 databases sql normal

Answer

3.17.11 Sql: GATE2001-21 top

http://gateoverflow.in/762

Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

a. Write a relational algebra using $(\Pi, \sigma, \rho, \times)$ to find the list of names which appear more than once in examinee.
b. Write an SQL query to list the *regno* of examinees who have a score greater than the average score.
c. Suppose the relation *appears* (regno, centr_code) specifies the center where an examinee appears. Write an SQL query to list the *centr_code* having an examinee of score greater than 80.

gate2001 databases sql normal descriptive

Answer

3.17.12 Sql: GATE2003-86 top

http://gateoverflow.in/969

Consider the set of relations shown below and the SQL query that follows.

Students: (Roll_number, Name, Date_of_birth)

Courses: (Course_number, Course_name, Instructor)

Grades: (Roll_number, Course_number, Grade)

```
Select distinct Name
from Students, Courses, Grades
where Students.Roll_number=Grades.Roll_number
 and Courses.Instructor = 'Korth'
 and Courses.Course_number = Grades.Course_number
 and Grades.Grade = 'A'
```

Which of the following sets is computed by the above query?

A. Names of students who have got an A grade in all courses taught by Korth

B. Names of students who have got an A grade in all courses

C. Names of students who have got an A grade in at least one of the courses taught by Korth

D. None of the above

gate2003 databases sql easy

Answer

3.17.13 Sql: GATE2004-53 top

http://gateoverflow.in/1049

The employee information in a company is stored in the relation

- Employee (name, sex, salary, deptName)

Consider the following SQL query

```
Select deptName
    From Employee
    Where sex = 'M'
    Group by deptName
    Having avg(salary) >
        (select avg (salary) from Employee)
```

It returns the names of the department in which

A. the average salary is more than the average salary in the company

B. the average salary of male employees is more than the average salary of all male employees in the company

C. the average salary of male male employees is more than the average salary of employees in same the department

D. the average salary of male employees is more than the average salary in the company

gate2004 databases sql normal

Answer

3.17.14 Sql: GATE2004-IT-74 top

http://gateoverflow.in/3718

A relational database contains two tables student and department in which student table has columns roll_no, name and dept_id and department table has columns dept_id and dept_name. The following insert statements were executed successfully to populate the empty tables:

```
Insert into department values (1, 'Mathematics')
Insert into department values (2, 'Physics')
Insert into student values (1, 'Navin', 1)
Insert into student values (2, 'Mukesh', 2)
Insert into student values (3, 'Gita', 1)
```

How many rows and columns will be retrieved by the following SQL statement?

```
Select * from student, department
```

A. 0 row and 4 columns
B. 3 rows and 4 columns
C. 3 rows and 5 columns
D. 6 rows and 5 columns

gate2004-it databases sql normal

Answer

3.17.15 Sql: GATE2004-IT-76 top

http://gateoverflow.in/3720

A table T1 in a relational database has the following rows and columns:

roll no.	marks
1	10
2	20
3	30
4	Null

The following sequence of SQL statements was successfully executed on table T1.

```
Update T1 set marks = marks + 5
Select avg(marks) from T1
```

What is the output of the select statement?

A. 18.75
B. 20
C. 25
D. Null

gate2004-it databases sql normal

Answer

3.17.16 Sql: GATE2004-IT-78 top

http://gateoverflow.in/3722

Consider two tables in a relational database with columns and rows as follows:

Table: Student

Roll_no	**Name**	**Dept_id**
1	ABC	1
2	DEF	1
3	GHI	2
4	JKL	3

Table: Department

Dept_id	**Dept_name**
1	A

Dept_id	Dept_name
2	B
3	C

Roll_no is the primary key of the Student table, Dept_id is the primary key of the Department table and Student.Dept_id is a foreign key from Department.Dept_id
What will happen if we try to execute the following two SQL statements?

i. update Student set Dept_id = Null where Roll_on = 1
ii. update Department set Dept_id = Null where Dept_id = 1

A. Both i and ii will fail
B. i will fail but ii will succeed
C. i will succeed but ii will fail
D. Both i and ii will succeed

gate2004-it databases sql normal

Answer

3.17.17 Sql: GATE2005-77, ISRO2016-55 top http://gateoverflow.in/1400

The relation **book** (title,price) contains the titles and prices of different books. Assuming that no two books have the same price, what does the following SQL query list?

```
select title
from book as B
where (select count(*)
    from book as T
    where T.price>B.price) < 5
```

A. Titles of the four most expensive books

B. Title of the fifth most inexpensive book

C. Title of the fifth most expensive book

D. Titles of the five most expensive books

gate2005 databases sql easy isro2016

Answer

3.17.18 Sql: GATE2005-IT-69 top http://gateoverflow.in/3832

In an inventory management system implemented at a trading corporation, there are several tables designed to hold all the information. Amongst these, the following two tables hold information on which items are supplied by which suppliers, and which warehouse keeps which items along with the stock-level of these items.

Supply = (supplierid, itemcode)
Inventory = (itemcode, warehouse, stocklevel)

For a specific information required by the management, following SQL query has been written

```
Select distinct STMP.supplierid
From Supply as STMP
Where not unique (Select ITMP.supplierid
                            From Inventory, Supply as ITMP
                            Where STMP.supplierid = ITMP.supplierid
                            And ITMP.itemcode = Inventory.itemcode
                            And Inventory.warehouse = 'Nagpur');
```

For the warehouse at Nagpur, this query will find all suppliers who

A. do not supply any item
B. supply exactly one item
C. supply one or more items
D. supply two or more items

gate2005-it databases sql normal

Answer

3.17.19 Sql: GATE2006-67 top

http://gateoverflow.in/1845

Consider the relation account (customer, balance) where customer is a primary key and there are no null values. We would like to rank customers according to decreasing balance. The customer with the largest balance gets rank 1. Ties are not broke but ranks are skipped: if exactly two customers have the largest balance they each get rank 1 and rank 2 is not assigned.

Query1:	select A.customer, count(B.customer) from account A, account B where A.balance <=B.balance group by A.customer
Query2:	select A.customer, 1+count(B.customer) from account A, account B where A.balance < B.balance group by A.customer

Consider these statements about Query1 and Query2.

1. Query1 will produce the same row set as Query2 for some but not all databases.
2. Both Query1 and Query2 are correct implementation of the specification
3. Query1 is a correct implementation of the specification but Query2 is not
4. Neither Query1 nor Query2 is a correct implementation of the specification
5. Assigning rank with a pure relational query takes less time than scanning in decreasing balance order assigning ranks using ODBC.

Which two of the above statements are correct?

A. 2 and 5
B. 1 and 3
C. 1 and 4
D. 3 and 5

gate2006 databases sql normal

Answer

3.17.20 Sql: GATE2006-68 top

http://gateoverflow.in/1846

Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints.
Given the following four queries:

Query1:

```
select student from enrolled where student in (select student from paid)
```

Query2:

```
select student from paid where student in (select student from enrolled)
```

Query3:

```
select E.student from enrolled E, paid P where E.student = P.student
```

Query4:

```
select student from paid where exists
    (select * from enrolled where enrolled.student = paid.student)
```

Which one of the following statements is correct?

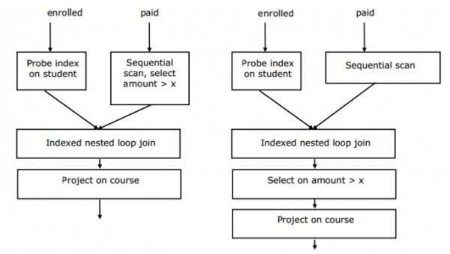
A. All queries return identical row sets for any database
B. Query2 and Query4 return identical row sets for all databases but there exist databases for which Query1 and Query2 return different row sets
C. There exist databases for which Query3 returns strictly fewer rows than Query2
D. There exist databases for which Query4 will encounter an integrity violation at runtime

gate2006 databases sql normal

Answer

3.17.21 Sql: GATE2006-69 top http://gateoverflow.in/1847

Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints. Assume that amounts 6000, 7000, 8000, 9000 and 10000 were each paid by 20% of the students. Consider these query plans (Plan 1 on left, Plan 2 on right) to *"list all courses taken by students who have paid more than x"*



A disk seek takes 4ms, disk data transfer bandwidth is 300 MB/s and checking a tuple to see if amount is greater than x takes 10µs. Which of the following statements is correct?

A. Plan 1 and Plan 2 will not output identical row sets for all databases
B. A course may be listed more than once in the output of Plan 1 for some databases
C. For x = 5000, Plan 1 executes faster than Plan 2 for all databases
D. For x = 9000, Plan I executes slower than Plan 2 for all databases

gate2006 databases sql normal

Answer

3.17.22 Sql: GATE2006-IT-84 top http://gateoverflow.in/3640

Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are *did* and *cid* respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

did	dname	rating	age
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Amoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

R: Reserves relation

did	cid	day
22	101	10/10/06
22	102	10/10/06
22	103	08/10/06
22	104	07/10/06
31	102	10/11/06
31	103	06/11/06
31	104	12/11/06
64	101	05/09/06
64	102	08/09/06
74	103	08/09/06

C: cars relation

cid	cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

What is the output of the following SQL query?

```
select D.dname
from Drivers D
where D.did in  (
                        select R.did
                        from Cars C, Reserves R
                        where R.cid = C.cid and C.colour = 'red'
                        intersect
                        select R.did
                        from Cars C, Reserves R
                        where R.cid  = C.cid and C.colour = 'green'
                         )
```

A. Karthikeyan, Boris
B. Sachin, Salman
C. Karthikeyan, Boris, Sachin
D. Schumacher, Senna

gate2006-it databases sql normal

Answer

3.17.23 Sql: GATE2006-IT-85 top

http://gateoverflow.in/3641

Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are *did* and *cid* respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

did	dname	rating	age
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Amoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

R: Reserves relation

did	cid	day
22	101	10/10/06
22	102	10/10/06
22	103	08/10/06
22	104	07/10/06
31	102	10/11/06
31	103	06/11/06

did	cid	day
21	104	12/11/06
64	101	05/09/06
64	102	08/09/06
74	103	08/09/06

C: cars relation

cid	cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

```
select D.dname
from Drivers D
where D.did in  (
                        select R.did
                        from Cars C, Reserves R
                        where R.cid = C.cid and C.colour = 'red'
                        intersect
                        select R.did
                        from Cars C, Reserves R
                        where R.cid  = C.cid and C.colour = 'green'
                         )
```

Let n be the number of comparisons performed when the above SQL query is optimally executed. If linear search is used to locate a tuple in a relation using primary key, then n lies in the range

A. 36 - 40
B. 44 - 48
C. 60 - 64
D. 100 - 104

gate2006-it databases sql normal

Answer

3.17.24 Sql: GATE2007-61 top http://gateoverflow.in/1259

Consider the table **employee**(empId, name, department, salary) and the two queries Q_1, Q_2 below. Assuming that department 5 has more than one employee, and we want to find the employees who get higher salary than anyone in the department 5, which one of the statements is **TRUE** for any arbitrary employee table?

Q_1 :
```
Select e.empId
From employee e
Where not exists
    (Select * From employee s Where s.department = "5" and s.salary >= e.salary)
```

Q_2 :
```
Select e.empId
From employee e
Where e.salary > Any
    (Select distinct salary From employee s Where s.department = "5")
```

A. Q_1 is the correct query

B. Q_2 is the correct query

C. Both Q_1 and Q_2 produce the same answer

D. Neither Q_1 nor Q_2 is the correct query

gate2007 databases sql normal verbal-ability

Answer

3.17.25 Sql: GATE2008-IT-74 top http://gateoverflow.in/3388

Student (school-id, sch-roll-no, sname, saddress)
School (school-id, sch-name, sch-address, sch-phone)
Enrolment(school-id sch-roll-no, erollno, examname)

ExamResult(erollno, examname, marks)

What does the following SQL query output?

```
SELECT sch-name, COUNT (*)
FROM School C, Enrolment E, ExamResult R
WHERE E.school-id = C.school-id
AND
E.examname = R.examname AND E.erollno = R.erollno
AND
R.marks = 100 AND S.school-id IN (SELECT school-id
                                FROM student
                                GROUP BY school-id
                                 HAVING COUNT (*) > 200)
GROUP By school-id
```

A. for each school with more than 200 students appearing in exams, the name of the school and the number of 100s scored by its students

B. for each school with more than 200 students in it, the name of the school and the number of 100s scored by its students

C. for each school with more than 200 students in it, the name of the school and the number of its students scoring 100 in at least one exam

D. nothing; the query has a syntax error

gate2008-it databases sql normal

Answer

3.17.26 Sql: GATE2010-19 top

http://gateoverflow.in/2194

A relational schema for a train reservation database is given below.

passenger(pid, pname, age)

reservation(pid, class, tid)

Table: Passenger

pid	pname	Age
0	'Sachin'	65
1	'Rahul'	66
2	'Sourav'	67
3	'Anil'	69

Table: Reservation

pid	class	tid
0	'AC'	8200
1	'AC'	8201
2	'SC'	8201
5	'AC'	8203
1	'SC'	8204
3	'AC'	8202

What **pids** are returned by the following SQL query for the above instance of the tables?

```
SELECT pid
FROM Reservation
WHERE class='AC' AND
    EXISTS (SELECT *
            FROM Passenger
            WHERE age>65 AND
            Passenger.pid=Reservation.pid)
```

A. 1, 0
B. 1, 2
C. 1, 3
D. 1, 5

gate2010 databases sql normal

Answer

3.17.27 Sql: GATE2011_32 top

http://gateoverflow.in/2134

Consider a database table T containing two columns X and Y each of type integer. After the creation of the table, one record $(X=1, Y=1)$ is inserted in the table.

Let MX and MY denote the respective maximum values of X and Y among all records in the table at any point in time. Using MX and MY, new records are inserted in the table 128 times with X and Y values being $MX+1, 2*MY+1$ respectively. It may be noted that each time after the insertion, values of MX and MY change.

What will be the output of the following SQL query after the steps mentioned above are carried out?

```
SELECT Y FROM T WHERE X=7;
```

(A) 127

(B) 255

(C) 129

(D) 257

gate2011 databases sql normal

Answer

3.17.28 Sql: GATE2011_46 top

http://gateoverflow.in/2148

Database table by name
Loan_Records is given below.

Borrower	Bank_Manager	Loan_Amount
Ramesh	Sunderajan	10000.00
Suresh	Ramgopal	5000.00
Mahesh	Sunderajan	7000.00

What is the output of the following SQL query?

```
SELECT count(*)
FROM (
    SELECT Borrower, Bank_Manager FROM Loan_Records) AS S
    NATURAL JOIN
    (SELECT Bank_Manager, Loan_Amount FROM Loan_Records) AS T
);
```

(A) 3

(B) 9

(C) 5

(D) 6

gate2011 databases sql normal

Answer

3.17.29 Sql: GATE2012_15 top

http://gateoverflow.in/47

Which of the following statements are **TRUE** about an SQL query?
P : An SQL query can contain a HAVING clause even if it does not have a GROUP BY clause
Q : An SQL query can contain a HAVING clause only if it has a GROUP BY clause
R : All attributes used in the GROUP BY clause must appear in the SELECT clause
S : Not all attributes used in the GROUP BY clause need to appear in the SELECT clause

(A) P and R
(B) P and S

(C) Q and R
(D) Q and S

gate2012 databases easy sql ambiguous

Answer

3.17.30 Sql: GATE2014-1-22 top

http://gateoverflow.in/1789

Given the following statements:

S1: A foreign key declaration can always be replaced by an equivalent check assertion in SQL.

S2: Given the table $R(a, b, c)$ where a and b together form the primary key, the following is a valid table definition.

```
CREATE TABLE S (
     a INTEGER,
     d INTEGER,
     e INTEGER,
     PRIMARY KEY (d),
     FOREIGN KEY (a) references R)
```

Which one of the following statements is **CORRECT**?

A. S1 is TRUE and S2 is FALSE
B. Both S1 and S2 are TRUE
C. S1 is FALSE and S2 is TRUE
D. Both S1 and S2 are FALSE

gate2014-1 databases normal sql

Answer

3.17.31 Sql: GATE2014-1-54 top

http://gateoverflow.in/1934

Given the following schema:

employees(emp-id, first-name, last-name, hire-date, dept-id, salary)

departments(dept-id, dept-name, manager-id, location-id)

You want to display the last names and hire dates of all latest hires in their respective departments in the location ID 1700. You issue the following query:

```
SQL>SELECT last-name, hire-date
    FROM employees
    WHERE (dept-id, hire-date) IN
    (SELECT dept-id, MAX(hire-date)
    FROM employees JOIN departments USING(dept-id)
    WHERE location-id =1700
    GROUP BY dept-id);
```

What is the outcome?

A. It executes but does not give the correct result
B. It executes and gives the correct result.
C. It generates an error because of pairwise comparison.
D. It generates an error because of the GROUP BY clause cannot be used with table joins in a sub-query.

gate2014-1 databases sql normal

Answer

3.17.32 Sql: GATE2014-2-54 top

http://gateoverflow.in/2021

SQL allows duplicate tuples in relations, and correspondingly defines the multiplicity of tuples in the result of joins. Which one of the following queries always gives the same answer as the nested query shown below:

```
select * from R where a in (select S.a from S)
```

A. select R.* from R, S where R.a=S.a
B. select distinct R.* from R,S where R.a=S.a
C. select R.* from R,(select distinct a from S) as S1 where R.a=S1.a
D. select R.* from R,S where R.a=S.a and is unique R

gate2014-2 databases sql normal

Answer

3.17.33 Sql: GATE2014-3-54 top

http://gateoverflow.in/2089

Consider the following relational schema:

employee(empId,empName,empDept)

customer(custId,custName,salesRepId,rating)

salesRepId is a foreign key referring to **empId** of the employee relation. Assume that each employee makes a sale to at least one customer. What does the following query return?

```
SELECT empName   FROM employee E
WHERE NOT EXISTS (SELECT custId
    FROM customer C
    WHERE C.salesRepId = E.empId
    AND C.rating <> 'GOOD');
```

A. Names of all the employees with at least one of their customers having a ‘GOOD’ rating.
B. Names of all the employees with at most one of their customers having a 'GOOD' rating.
C. Names of all the employees with none of their customers having a 'GOOD' rating.
D. Names of all the employees with all their customers having a 'GOOD' rating.

gate2014-3 databases sql easy

Answer

3.17.34 Sql: GATE2015-1_27 top

http://gateoverflow.in/8225

Consider the following relation:

Student

Roll-No	Student name
1	Raj
2	Rohit
3	Raj

Performance

Roll-No	Course	Marks
1	Math	80
1	English	70
2	Math	75
3	English	80
2	Physics	65
3	Math	80

Consider the following SQL query.

```
SELECT S. student_Name, Sum(p. Marks)
FROM student S, performance P
WHERE S.Roll_No= P.Roll_No
GROUP BY S.STUDENT_Name
```

The numbers of rows that will be returned by the SQL query is__________________.

gate2015-1 databases sql normal numerical-answers

Answer

3.17.35 Sql: GATE2015-3_3 top

http://gateoverflow.in/8396

Consider the following relation

Cinema($theater, address, capacity$)

Which of the following options will be needed at the end of the SQL query

```
SELECT P1.address
FROM Cinema P1
```

such that it always finds the addresses of theaters with maximum capacity?

A.
```
A. WHERE P1.capacity >= All (select P2.capacity from Cinema P2)
```
B.
```
B. WHERE P1.capacity >= Any (select P2.capacity from Cinema P2)
```
C.
```
C. WHERE P1.capacity > All (select max(P2.capacity) from Cinema P2)
```
D.
```
D. WHERE P1.capacity > Any (select max(P2.capacity) from Cinema P2)
```

gate2015-3 databases sql normal

Answer

3.17.36 Sql: GATE2017-1-23 top

http://gateoverflow.in/118303

Consider a database that has the relation schema EMP (EmpId, EmpName, and DeptName). An instance of the schema EMP and a SQL query on it are given below:

EMP

EmpId	EmpName	DeptName
1	XYA	AA
2	XYB	AA
3	XYC	AA
4	XYD	AA
5	XYE	AB
6	XYF	AB
7	XYG	AB
8	XYH	AC
9	XYI	AC
10	XYJ	AC
11	XYK	AD
12	XYL	AD
13	XYM	AE

```
SELECT AVG(EC.Num)
FROM EC
WHERE (DeptName, Num) IN
    (SELECT DeptName, COUNT(EmpId) AS
                        EC(DeptName, Num)
    FROM EMP
    GROUP BY DeptName)
```

The output of executing the SQL query is _____________ .

gate2017-1 databases sql numerical-answers

Answer

3.17.37 Sql: GATE2017-2-46 top

http://gateoverflow.in/118391

Consider the following database table named top_scorer.

top_scorer		
player	**country**	**goals**
Klose	Germany	16
Ronaldo	Brazil	15

G Muller	Germany	14
Fontaine	France	13
Pele	Brazil	12
Klinsmann	Germany	11
Kocsis	Hungary	11
Batistuta	Argentina	10
Cubillas	Peru	10
Lato	Poland	10
Lineker	England	10
T Muller	Germany	10
Rahn	Germany	10

Consider the following SQL query:

```
SELECT ta.player FROM top_scorer AS ta
WHERE ta.goals >ALL (SELECT tb.goals
    FROM top_scorer AS tb
    WHERE tb.country = 'Spain')
AND ta.goals > ANY (SELECT tc.goals
    FROM top_scorer AS tc
    WHERE tc.country='Germany')
```

The number of tuples returnrf by the above SQL query is _______

gate2017-2 databases sql numerical-answers

Answer

Answers: Sql

3.17.1 Sql: GATE 2016-2-52 top

http://gateoverflow.in/39604

Selected Answer

1^{st} query will return following:

Table Name : Total**(name,capacity)**

Name	Capacity
Ajmer	20
Bikaner	40
Churu	30
Dungargarh	10

2^{nd} Query will return, **Total_avg(capacity)**

25

Since sum of capacity = 100/4=25

3^{rd} query will be final and it's tupples will be considered as output,
where name of district and its total capacity should be more than or equal to 25

Name
Bikaner
Churu

Hence, **2 tuples** returned.

34 votes -- Shashank Chavan (3.4k points)

3.17.2 Sql: GATE1990-10a top

http://gateoverflow.in/85686

Selected Answer

```
1.SELECT ename
  FROM employees
  WHERE eno IN
                 (SELECT eno
                 FROM working
                 GROUP BY eno
                 HAVING COUNT (*)=
                                   (SELECT COUNT (*)
                                   FROM projects));
This will return : Employee name who is working for all projects.
(ii)
SELECT pname
FROM projects
WHERE pno IN
                 (SELECT pno
                 FROM projects
                 MINUS
                 SELECT DISTINCT pno
                 FROM working);
```

This will return : Project name for which no employee is working.

8 votes -- Prashant Singh (49.2k points)

3.17.3 Sql: GATE1991_12,a top http://gateoverflow.in/539

i) $\pi_{pcode}(\sigma_{city==prcity=="Delhi"}(sppr \bowtie supplier \bowtie project))$

ii) $\pi_{city,\ pcode,\ prcity}(\sigma_{city!=prcity}(sppr \bowtie supplier \bowtie project))$

5 votes -- Sheshang M. Ajwalia (2.8k points)

3.17.4 Sql: GATE1997_76 top http://gateoverflow.in/19838

1) $\Pi_{\text{eno}}(\text{EMP} \bowtie_{\textbf{EMP.eno=INVOLVED.eno and INVOLVED.pno=3}} \text{INVOLVED})$
2) $\Pi_{\textbf{eno}}(\text{INVOLVED}) - \Pi_{\textbf{eno}}((\Pi_{\textbf{eno}}(\text{INVOLVED}) \times \Pi_{\textbf{pno}}(\text{PROJ}) - \text{INVOLVED})$

A. $\Pi_{\textbf{eno}}(\text{INVOLVED})$ All involved emplyee in projects.

B. $\Pi_{\textbf{eno}}((\Pi_{\textbf{eno}}(\text{INVOLVED}) \times \Pi_{\textbf{pno}}(\text{PROJ}) - \text{INVOLVED})$ gives all employee who not involved in atleast one project.

A-B = **employeeNo. of employee involved on the all project. (simple dived query)**

3) $\Pi_{\text{age}}(\text{EMP}) - \Pi_{\text{age}}(\boldsymbol{\sigma}_{\textbf{Eage<EMP.age}}(\rho E(\text{EMP}) \times \text{EMP}))$

A. $\Pi_{\text{age}}(\text{EMP})$ Age of all emplyee .

B. $\Pi_{\text{age}}(\boldsymbol{\sigma}_{\textbf{Eage<EMP.age}}(\rho E(\text{EMP}) \times \text{EMP}))$ Employee who have age less than atleast one emplyee.

A- B = Maximum of **(all ages of employee)**

9 votes -- Prashant Singh (49.2k points)

3.17.5 Sql: GATE1998_7a top http://gateoverflow.in/1721

Selected Answer

```
SELECT DISTINCT A.student FROM
    FREQUENTS A, SERVES B, LIKES C
    WHERE
        A.parlor=B.parlor
        AND
```

```
        B.ice-cream=C.ice-cream
        AND
        A.student=C.student;
```

OR

```
SELECT DISTINCT A.student FROM FREQUENTS A
    WHERE
    parlor IN
        (SELECT parlor FROM SERVES B
            WHERE B.ice-cream IN
                (SELECT ice-cream
                FROM LIKES C
                WHERE C.student = A.student));
```

9 votes -- Arjun Suresh (294k points)

3.17.6 Sql: GATE1999_2.25 top

http://gateoverflow.in/1502

Selected Answer

(d)

SQL wont remove duplicates like relational algebra projection, we have to remove it explicilty by distinct.

If there are no indexes on the relation SQL will either chose one/more on its own or simply work without any index. No index would just slow the query but it will surely work.

SQL does not permit 2 attributes to have same name in a relation.

16 votes -- Aravind (3.3k points)

3.17.7 Sql: GATE1999_22 top

http://gateoverflow.in/1521

Selected Answer

(a)

```
select Employee-name
from EMP, DEPT
where Salary>50000 and EMP.Dept-no=DEPT.Dept-no and Location="Calcutta"
```

(b)

```
select Dept-no, count(*)
from EMP where salary > 100000
group by Dept-no
```

11 votes -- Aravind (3.3k points)

3.17.8 Sql: GATE2000-2.25 top

http://gateoverflow.in/672

Selected Answer

This question is about SQL, in SQL Relations are **MULTISET**, not SET. So R or S can have duplicated.

Answer :-A.

A -> If R has duplicates, in that case, due to distinct keyword those duplicates will be eliminated in final result. So R can not have duplicates. If S is empty RXS becomes empty, so S must be non empty. This is true.

B. Here assume that S is empty. (No duplicates.) Then R X S will be empty. SO this is false.

C. Same argument as B.

D. Assume that R has duplicates. Then Distinct keyword will remove duplicates. So Result of query != R, so This is false.

20 votes -- Akash (43.8k points)

3.17.9 Sql: GATE2000-2.26 top http://gateoverflow.in/673

Selected Answer

answer = **option C**

Value at hand	Option A		Option B		Option C	
6	✗	✗	✗	✗	✓	✓
5	✓	✓	✓	✓	✗	✗
null	✗	✗	✗	✗	✗	✓

21 votes -- Amar Vashishth (28.7k points)

Answer: C

As (null) != 5 gives false.
But, not((null) = 5) gives not(false) gives true.

19 votes -- Aravind (3.3k points)

3.17.10 Sql: GATE2001-2.25 top http://gateoverflow.in/743

Selected Answer

Answer: C

The table can be depicted as:

ib (PK)	ub (FK)
z	w=u
u	v=x
x	y

If (x,y) is deleted then from the above table:

- v<=y (as v=x)
- u<v<=y, u!=v (as v=x and ib is the Primary Key)
- w<v<=y (as w=u)
- z<w<v<=y, z!=w (as w=u and ib is the Primary Key)

As, it can be seen that w<v or w<x (as v=x) so C is the answer.

12 votes -- Rajarshi Sarkar (35k points)

3.17.11 Sql: GATE2001-21 top http://gateoverflow.in/762

1) ρ (exm1,examinee) , ρ(exm2,examinee)

$\Pi_{exm1.name}(emx1 \times exm2)$

$\sigma_{((emp1.regno \,!= emp2.regno) \text{ and } (emp1.name = emp2.name))}$

2) select reg no

from examinee where score IN (select score

from examinee

where score< select avg(score) from examinee)

3)select centre_code from apprears

where regno IN (SELECT regno from examinee where score>80)

2 votes -- Tauhin Gangwar (9.3k points)

3.17.12 Sql: GATE2003-86 top http://gateoverflow.in/969

Selected Answer

C. Names of the students who have got an A grade in at least one of the courses taught by Korth.

15 votes -- Arjun Suresh (294k points)

3.17.13 Sql: GATE2004-53 top http://gateoverflow.in/1049

Selected Answer

D is the answer.

The inner query is over all department and over both male and female employees while the outer query is only for male employees.

12 votes -- Arjun Suresh (294k points)

3.17.14 Sql: GATE2004-IT-74 top http://gateoverflow.in/3718

Selected Answer

since there is no specific joining condition specified it will retrieve cartesian product of the table

number of rows = product of number of rows in each realtion = 3*2 = 6

number of columns = sum of number of columns = 3+2 = 5

answer: D

24 votes -- Sankaranarayanan P.N (11.2k points)

3.17.15 Sql: GATE2004-IT-76 top http://gateoverflow.in/3720

Selected Answer

Update on null gives null. Now, avg function ignores null values. So, here avg will be (15 + 25 + 35) / 3 = 25.

http://msdn.microsoft.com/en-us/library/ms177677.aspx

15 votes -- Arjun Suresh (294k points)

3.17.16 Sql: GATE2004-IT-78 top http://gateoverflow.in/3722

Selected Answer

ans is C

here in (i) when we update in STUDENT table dept id =NULL then it will not cause any problem to referenced table

but in (II) if we set in DEPARTMENT table dept id =NULL then it will produce inconsistency because in STUDENT table we still have the tuples containing the dept id =1

14 votes -- neha pawar (4.4k points)

3.17.17 Sql: GATE2005-77, ISRO2016-55 top http://gateoverflow.in/1400

Selected Answer

Answer: D

The outer query selects all titles from book table. For every selected book, the subquery returns count of those books which are more expensive than the selected book. The where clause of outer query will be true for 5 most expensive book. For example count (*) will be 0 for the most expensive book and count(*) will be 1 for second most expensive book.

25 votes -- Rajarshi Sarkar (35k points)

3.17.18 Sql: GATE2005-IT-69 top http://gateoverflow.in/3832

Ans D) supply two or more items
The whole query returns the distinct list of suppliers who supply two or more items.

16 votes -- Bran Stark (391 points)

Answer is d, nested query ensures that for only those suppliers it returns true which supplies more than 1 item in which case supplier id in inner query will be repeated for that supplier.

10 votes -- Anurag Semwal (8k points)

3.17.19 Sql: GATE2006-67 top http://gateoverflow.in/1845

Selected Answer

Both Query1 and Query2 are not correct implementations because: Assume that we have a table with n customers having same balance. In that case Query1 will give rank n to each customer. But according to the question the rank assigned should be 1. And Query2 will return an empty result set (as it will never return rank 1). So statement 4 is correct. For same reason Query 1 is wrong though it is true if we assume relation set is empty. Statements 2 and 3 are false as 4 is TRUE. Statement 5 is false as a single scan should be faster than a join query. So, best option should be C, though 1 is not technically correct.

A correct query to achieve the task would be:

```
select A.customer, (
    select 1+count(*)
    from account B
    where A.balance < B.balance
) from account A
```

22 votes -- Rajarshi Sarkar (35k points)

3.17.20 Sql: GATE2006-68 top http://gateoverflow.in/1846

Selected Answer

Query 1 and Query 3: output will be same

and Query 2 and 4, output will be same

I have run these queries on online compiler, this what I get

```
BEGIN TRANSACTION;

-- /* Create a table called NAMES */
-- CREATE TABLE E(Id integer);
-- CREATE TABLE P(Id integer);
--
-- /* Create few records in this table */
-- INSERT INTO E VALUES(1);
-- INSERT INTO E VALUES(1);
-- INSERT INTO E VALUES(3);
-- INSERT INTO E VALUES(3);
--
-- INSERT INTO P VALUES(1);
-- INSERT INTO P VALUES(2);
-- INSERT INTO P VALUES(3);
-- INSERT INTO P VALUES(4);


COMMIT;

/* Display all the records from the table */
-- SELECT * FROM E;
-- select "------";
-- SELECT * FROM P;
-- select "------";
select "Query 1:";
select E.id from E
where E.id in (select P.id from P);



select "Query 2:";
select id from P
where id in (select id from E);


select "Query 3:";

select E.id from E e, P p
where e.id = p.id;

select "Query 4:";
select id from P
where exists (select * from E where E.id = P.id);


/* output */
Query 1:
1
1
3
3
Query 2:
1
3
Query 3:
1
1
3
3
Query 4:
1
3
```

So according to me answer should be **B.**

👍 17 votes -- Vikrant Singh (13.4k points)

---

query 1 and 3:In enrolled table student is not a key, so duplicate student values might be present which will be printed in final result

query 2 and 4:In Paid table 'Student' is a key, ensuring it has unique values only therefore these two queries will return distinct student values.

Therefore only b is correct.

👍 12 votes -- Anurag Semwal (8k points)

3.17.21 Sql: GATE2006-69 top

http://gateoverflow.in/1847

I think it should be C)

in all cases plan 1 is faster than plan 2 cause in plan 1 we are reducing the load by doing select amount >x and then the loop

but in case of plan 2 its in the nested loop so it need to check every time and will take more time to execute .

12 votes -- Pranay Datta (9.7k points)

3.17.22 Sql: GATE2006-IT-84 top

http://gateoverflow.in/3640

Selected Answer

For color = "Red"

did = {22, 22, 31, 64}

For color = "Green"

did = {22, 31, 74}

intersection of Red and Green will give = {22, 31}

which is Karthikeyan and Boris

Ans: A

17 votes -- Vikrant Singh (13.4k points)

3.17.23 Sql: GATE2006-IT-85 top

http://gateoverflow.in/3641

Selected Answer

```
select D.dname
from Drivers D
where D.did in  (
                        select R.did
                        from Cars C, Reserves R
                        where R.cid = C.cid and C.colour = 'red'
                        intersect
                        select R.did
                        from Cars C, Reserves R
                        where R.cid  = C.cid and C.colour = 'green'
                         )
```

```
select R.did from Cars C, Reserves R where R.cid = C.cid and C.colour = 'red'
```

So, first get 2 red cars by scanning 4 tuples of the cars relation. Now, for each of the two 'red' cars, we scan all the 10 tuples of the 'Reserves' relation and thus we get 2*10 + 4 = 24 comparisons. But this is not optimal. We can check in the reverse order for each tuple of the 'Reserves' relation because 'cid' is a primary key (hence unique) of 'Cars' relation. Supposing our earlier selection is <102, 104> then this requires 3 + 7*2 = 17 comparisons. If the order was <104, 102>, then 2 + 8*2 = 18 comparisons. Thus toally 21-22 comparisons and gives <22, 31, 64> as did.

Similarly for the 'green' car we get 4+10 - 14 comparisons. Gives <22, 31, 74>.

Intersect requires 1+2+3 = 6 comparisons in the best case and 3 + 2 + 3 = 8 in the worst case and this gives <22, 31>.

Finally we have to locate the did - 22 and did 31 from the driver table and did is the primary key. As told in the question, we use linear search and for 22, we hit on the first try and for 31 we hit on the third try. So, 1 + 3 = 4 comparisons.

Thus total no. of comparisons = 21-22 + 14 + 6-8 + 4 = 45-48.

12 votes -- Arjun Suresh (294k points)

4 for finding red cars with 20 for Did & 4 for finding green cars with 10 for Did

red Did :22 31 64

green Did : 22 31 74

6 for intersection

1 for searching 22 in driver relation

& 3 for 31

total 38+6+4=48

therefore **B is the answer**

11 votes -- paras17jain (115 points)

3.17.24 Sql: GATE2007-61 top http://gateoverflow.in/1259

Selected Answer

Answer: A

Create a table like this:

```
create table employee(empId int(50), name varchar(50), department int(50), salary int(50));
insert into employee values (1, 'a', 4, 90);
insert into employee values (2, 'b', 5, 30);
insert into employee values (3, 'c', 5, 50);
insert into employee values (4, 'd', 5, 80);
insert into employee values (8, 'f', 7, 10);
```

Q1 returns 1 for the above table. See here: http://sqlfiddle.com/#!9/9acce/1

Q2 returns empId of those employees who get salary more than the minimum salary offered in department 5. It returns 1,3,4 for the above table. See here: http://sqlfiddle.com/#!9/9acce/2

According the question the answer should be 1 for the above table.

PS: The question implies that the required employee must not be from department 5.

18 votes -- Rajarshi Sarkar (35k points)

3.17.25 Sql: GATE2008-IT-74 top http://gateoverflow.in/3388

Selected Answer

D:

If Select clause consist aggregate and non - aggregate columns.All non aggregate columns in the Select clause must appear in Group By clause. But in this query Group by clause consists school-id instead of school-name

http://weblogs.sqlteam.com/jeffs/archive/2007/07/20/but-why-must-that-column-be-contained-in-an-aggregate.aspx

20 votes -- erravi90 (171 points)

3.17.26 Sql: GATE2010-19 top http://gateoverflow.in/2194

Selected Answer

(c)1,3

the inner query gives passenger_id with age above 65 i.e. 1,2,3

the outer query chooses the class as AC, which are 1 and 3

17 votes -- Aravind (3.3k points)

3.17.27 Sql: GATE2011_32 top http://gateoverflow.in/2134

Selected Answer

X = 1, Y = 1

X = 2, Y = 2*1 +1 = 3

X = 3, Y = 2*3 + 1 = 7

X = 4, Y = 2*7 + 1 = 15

X = 5, Y = 2*15 + 1 = 31

X = 6, Y = 2*31+1 = 63

X = 7, Y = 2*63 + 1 = 127

20 votes -- Arjun Suresh (294k points)

3.17.28 Sql: GATE2011_46 top http://gateoverflow.in/2148

Selected Answer

i think ans is (c)

when we perform natural join on S and T then result will be like this

Borrower	Bank Manager	Loan Amount
Ramesh	Sunderajan	10,000
Ramesh	Sunderajan	7000
Suresh	Ramgopala	5000
Mahesh	Sunderajan	10,000
Mahesh	Sunderajan	7000

after that count (*) will count total tuples present in this table so here it is 5

18 votes -- neha pawar (4.4k points)

3.17.29 Sql: GATE2012_15 top http://gateoverflow.in/47

Selected Answer

GATE 2012 Answer key is (C) Q and R are true.

But correct answer should be B.

- When group by is not present, having is applied to the whole table

"A grouped table is a set of groups derived during the evaluation of a <group by clause> or a <having clause>. A group is a multiset of rows in which all values of the grouping column or columns are equal if a <group by clause> is specified, or the group is the entire table if no <group by clause> is specified. A grouped table may be considered as a collection of tables. Set functions may operate on the individual tables within the grouped table."

This shows that P is indeed correct.

Also see "having clause section"
http://www.contrib.andrew.cmu.edu/~shadow/sql/sql1992.txt

http://searchsqlserver.techtarget.com/answer/ISO-ANSI-SQL-and-the-GROUP-BY-clause

The above link says that all columns used in group by must be present in select clause as per SQL-92 standard but later standards doesn't enforce it. I tried this on MySQL and it works. It is allowed in MSSQL also- see below link.

From Microsoft (obviously applicable only to MS-SQL)

http://msdn.microsoft.com/en-us/library/ms177673.aspx

> Expressions in the GROUP BY clause can contain columns of the tables, derived tables or views in the FROM clause. The columns are not required to appear in the SELECT clause <select> list.
>
> Each table or view column in any nonaggregate expression in the <select> list must be included in the GROUP BY list:

So, as per standard it is not allowed, but in most current DBMS it is allowed. And there is no reason why this shouldn't be allowed. So, ideally 'S' is more correct than 'R' or both are debatable and marks should have been given to all.

18 votes -- Arjun Suresh (294k points)

3.17.30 Sql: GATE2014-1-22 top

http://gateoverflow.in/1789

Selected Answer

(D)both are false

S1: Foreign key constraint means a lot of constraints it has to be a primary key(which intrun has few constraints)

Alternate reason: Using a check condition we can have the same effect as Foreign key while adding elements to the child table. But when we delete an element from the parent table the referential integrity constraint is no longer valid. So, a check constraint cannot replace a foreign key.
So, we cannot replace it with a single check

S2: if a and b forms a primary key in R, a alone cannot form a foreign key. **i.e.** R(**a**,**b**,c) and S(a,d,e) a of S references to a of R but a of R is not candidate key but a prime attribute since a,b combine a key.

Foreign key definition: it should be a candidate key in some other table(in our case it is only a prime attribute)

23 votes -- Aravind (3.3k points)

3.17.31 Sql: GATE2014-1-54 top

http://gateoverflow.in/1934

Selected Answer

```
SELECT dept-id, MAX(hire-date)
FROM employees JOIN departments USING(dept-id)
WHERE location-id =1700
GROUP BY dept-id
```

this inner query will give the max hire date of each department whose location_id =1700

and outer query will give the last name and hire-date of all those employees who joined on max hire date.
answer should come to (B) no errors
And we can use group by and where together, who said we can not :(

Example: create table departments(dept_id number, dept_name varchar2(25), location_id number);
Query: select d1.dept_name,max(d1.location_id)
from departments d1, departments d2
where d1.dept_name = d2.dept_name
and d1.dept_name='AA'
group by d1.dept_name;

will give output

23 votes -- Manu Thakur (6k points)

3.17.32 Sql: GATE2014-2-54 top

http://gateoverflow.in/2021

Selected Answer

C)

Consider the following instances of R & S

Let R

A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

Let S:-

A	X	Z
1	2	3
3	5	7
7	6	5
7	5	4

Now output of given Query

```
select * from R where a in (select S.a from S)
```

A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

For Option,

A) since multiplicity of tuples is disturbed

```
select R.* from R, S where R.a=S.a
```

∴ Output will be

A	B	C
1	2	3
1	2	3
7	8	9
7	8	9
7	8	9
7	8	9

B)

```
select distinct R.* from R,S where R.a=S.a
```

∵only Distinct R will be chosen in the end so , Output will look like

A	B	C
1	2	3
7	8	9

C) **ANSWER**

```
select R.* from R,(select distinct a from S) as S1 wher
```

Multiplicity of tuples is maintained. ∵ Multiplicity of duplicate tuples will be distributed when there is a match between R.a and S.a and for that match S.a's value is repeated.

So, Output will be

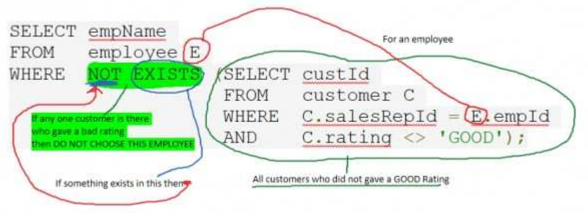
A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

29 votes -- Kalpish Singhal (2.1k points)

3.17.33 Sql: GATE2014-3-54 top

http://gateoverflow.in/2089

Selected Answer



So, an employee whose
ALL customers gives him GOOD rating is chosen;

All such employees are chosen.
ans = option **D**

15 votes -- Amar Vashishth (28.7k points)

(D)

inner query selects "employees with atleast one bad rating"

so negation on the above stmt give -> "employees with all ratings as good"

PS:put a ven diagram and practice for these kind of questions

10 votes -- Aravind (3.3k points)

3.17.34 Sql: GATE2015-1_27 top

http://gateoverflow.in/8225

Selected Answer

answer is 2 as there are only 2 distinct student names.

16 votes -- naresh1845 (1.4k points)

3.17.35 Sql: GATE2015-3_3 top

http://gateoverflow.in/8396

Selected Answer

A is the answer

B - Returns the addresses of all theaters.
C - Returns null set. max() returns a single value and there won't be any value > max.
D - Returns null set. Same reason as C. All and ANY works the same here as max returns a single value.

27 votes -- Arjun Suresh (294k points)

3.17.36 Sql: GATE2017-1-23 top

http://gateoverflow.in/118303

Selected Answer

The inner query will return

DeptName	Num
AA	4
AB	3
AC	3
AD	2
AE	1

now AVG(EC.Num) will find average of Num values in above returned query

which is (4+3+3+2+1)/5=2.6

so according to me answer should be 2.6

12 votes -- sriv_shubham (2.7k points)

3.17.37 Sql: GATE2017-2-46 top

http://gateoverflow.in/118391

Selected Answer

ALL(EMPTY SET) always returns TRUE. So first where condition is always satisfied.

Second where condition will return all those rows who have more goals than ANY German player. Since, minimum goals by a German is 10, all the rows which are greater than 10 Goals will be returned.

i.e. first 7 rows in the table.

Hence, ans: 7

9 votes -- tvkkk (1.1k points)

3.18 Timestamp Ordering(1) top

3.18.1 Timestamp Ordering: GATE2017-1-42 top

http://gateoverflow.in/118325

In a database system, unique timestamps are assigned to each transaction using Lamport's logical clock. Let $TS(T_1)$ and $TS(T_2)$ be the timestamps of transactions T_1 and T_2 respectively. Besides, T_1 holds a lock on the resource R, and T_2 has requested a conflicting lock on the same resource R. The following algorithm is used to prevent deadlocks in the database system assuming that a killed transaction is restarted with the same timestamp.

if $TS(T_2) < TS(T_1)$ then

T_1 is killed

else T_2 waits.

Assume any transaction that is not killed terminates eventually. Which of the following is TRUE about the database system that uses the above algorithm to prevent deadlocks?

(A) The database system is both deadlock-free and starvation-free.

(B) The database system is deadlock-free, but not starvation-free.

(C) The database system is starvation-free, but not deadlock-free.

(D) The database system is neither deadlock-free nor starvation-free.

gate2017-1 databases timestamp-ordering deadlock normal

Answer

Answers: Timestamp Ordering

3.18.1 Timestamp Ordering: GATE2017-1-42 top

http://gateoverflow.in/118325

Selected Answer

In a database system, **unique** timestamps are assigned to each transaction using Lamport's logical clock

Since Unique Timestamps are assigned, so there is no question of two transaction having same timestamp.

Moreover, there is nothing mentioned about the size of the counter by which it can be determined that whether there will be case of timestamp wrap around or not.

So, there will be no timestamp wrap around.

In Lamport's logical clock Timestamps are assigned in increasing order of enumeration.

So, $T_i<T_j$ if Transaction T_i came into system before T_j.

The above scheme given is nothing but " **Wound-Wait** " Scheme in which younger transaction is killed by older transaction that came into system before this younger transaction came.[1][2]

So, this is a part of Basic Time-Stamp Ordering in Concurrency Control.

And Basic Time Stamp ordering protocol is deadlock free and **not starvation free , in general**.

Here in this question according to given condition, the database system is both deadlock free and starvation free as well , as it is Wound wait scheme and in case of wound wait it **avoid starvation**, because in Wound Wait scheme **we restart a transaction that has been aborted , with it's same original Timestamp** . If it restart with a new Timestamp then there is a possibility of Starvation (as larger TimeStamp transaction is aborted here and new Transaction which is coming next have always greater TimeStamp than previous one). But that is Not the case here...

Reference:

[1] http://www.cs.colostate.edu/~cs551/CourseNotes/Deadlock/WaitWoundDie.html

[2] http://stackoverflow.com/questions/32794142/what-is-the-difference-between-wait-die-and-wound-wait

Hence Answer is (A)

PS: The **Wound-wait scheme means :**

- The ***newer*** **transactions** are ***killed*** when an ***older*** **transaction** make a ***request*** for a **lock** being **held** by the ***newer*** **transactions .**
- Here the algorithm says TS(T2) < TS(T1) means T2 is **older** transaction (as TS of T2 is less than TS of T1 ..means **T2 come first then T1 come and TS is assign in increasing order**) , so **newer one is T1** and also question says **T1 holds a lock on the resource R, and T2 has requested a conflicting lock on the same resource R.**
- So T1 is killed as per Wound-wait scheme .

Reference :

http://www.mathcs.emory.edu/~cheung/Courses/554/Syllabus/8-recv+serial/deadlock-compare.html

----

timestamps are assigned to each transaction using Lamport's logical clock.

This line means timestamps are assigns in increasing order .

We can divide the answer into 3 parts :

Part 1 : Is it Wound wait scheme ?

Yes, given algorithm

if TS(T2) < TS(T1) then

T1 is killed

else T2 waits.

comes under wound wait scheme..as here old transaction is always survive and older transaction wounds newer transaction when both want to apply lock on same resource ..

Part 2 : Wound Wait avoid Starvation

yes, How ?

as newer one is die and restart with same timestamp and older one is survive always so after execute older transaction that newer one can definitely execute .. and new transactions which are coming can die and restart again (previous newer became older that time) ..

Part 3 : Does Starvation freedom implies Deadlock freedom ?

Yes, here no starvation means also No deadlock possibility ..

In one line - wound wait -> no starvation -> no deadlock -> option A

7 votes -- Ayush Upadhyaya (1.9k points)

3.19 Transaction And Concurrency(1) top

3.19.1 Transaction And Concurrency: GATE2004-IT-21 top http://gateoverflow.in/3662

Which level of locking provides the highest degree of concurrency in a relational database ?

A. Page
B. Table
C. Row
D. Page, table and row level locking allow the same degree of concurrency

gate2004-it databases normal transaction-and-concurrency

Answer

Answers: Transaction And Concurrency

3.19.1 Transaction And Concurrency: GATE2004-IT-21 top http://gateoverflow.in/3662

Selected Answer

row level locking provides more concurrency. because different transactions can access different rows in a table / page at same time

13 votes -- Sankaranarayanan P.N (11.2k points)

3.20 Transactions(24) top

3.20.1 Transactions: GATE 2016-1-22 top http://gateoverflow.in/39644

Which one of the following is NOT a part of the ACID properties of database transactions?

A. Atomicity
B. Consistency
C. Isolation
D. Deadlock-freedom

gate2016-1 databases transactions easy

Answer

3.20.2 Transactions: GATE 2016-1-51 top

http://gateoverflow.in/39703

Consider the following two phase locking protocol. Suppose a transaction T accesses (for read or write operations), a certain set of objects $\{O_1, \dots . O_k\}$. This is done in the following manner:

$\text{Step } 1$. T acquires exclusive locks to $O_1, \dots \dots, O_k$ in increasing order of their addresses.

$\text{Step } 2$. The required operations are performed .

$\text{Step } 3$. All locks are released

This protocol will

A. guarantee serializability and deadlock-freedom
B. guarantee neither serializability nor deadlock-freedom
C. guarantee serializability but not deadlock-freedom
D. guarantee deadlock-freedom but not serializability.

gate2016-1 databases transactions normal

Answer

3.20.3 Transactions: GATE 2016-2-22 top

http://gateoverflow.in/39550

Suppose a database schedule S involves transactions $T_1, \dots \dots \dots, T_n$. Construct the precedence graph of S with vertices representing the transactions and edges representing the conflicts.If S is serializable, which one of the following orderings of the vertices of the precedence graph is guaranteed to yield a serial schedule?

A). Topological order

B). Depth-first order

C). Breadth- first order

D). Ascending order of the transaction indices.

gate2016-2 databases transactions normal

Answer

3.20.4 Transactions: GATE1999_2.6 top

http://gateoverflow.in/1484

For the schedule given below, which of the following is correct:

1	Read A	
2		Read B
3	Write A	
4		Read A
5		Write A
6		Write B
7	Read B	
8	Write B	

A. This schedule is serializable and can occur in a scheme using 2PL protocol

B. This schedule is serializable but cannot occur in a scheme using 2PL protocol

C. This schedule is not serializable but can occur in a scheme using 2PL protocol

D. This schedule is not serializable and cannot occur in a scheme using 2PL protocol

gate1999 databases transactions normal

Answer

3.20.5 Transactions: GATE2003-29, ISRO2009-73 top http://gateoverflow.in/919

Which of the following scenarios may lead to an irrecoverable error in a database system?

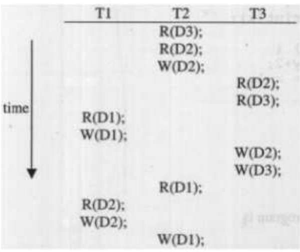
A. A transaction writes a data item after it is read by an uncommitted transaction
B. A transaction reads a data item after it is read by an uncommitted transaction
C. A transaction reads a data item after it is written by a committed transaction
D. A transaction reads a data item after it is written by an uncommitted transaction

gate2003 databases transactions easy isro2009

Answer

3.20.6 Transactions: GATE2003-87 top http://gateoverflow.in/970

Consider three data items D1, D2, and D3, and the following execution schedule of transactions T1, T2, and T3. In the diagram, R(D) and W(D) denote the actions reading and writing the data item D respectively.



Which of the following statements is correct?

A. The schedule is serializable as T2; T3; T1

B. The schedule is serializable as T2; T1; T3

C. The schedule is serializable as T3; T2; T1

D. The schedule is not serializable

gate2003 databases transactions normal

Answer

3.20.7 Transactions: GATE2004-IT-77 top http://gateoverflow.in/3721

Consider the following schedule S of transactions T1 and T2:

T1	**T2**
Read(A) A = A - 10	Read (A) Temp = 0.2*A Write(A) Read(B)
Write(A) Read(B) B = B + 10 Write(B)	B = B + Temp Write(B)

Which of the following is TRUE about the schedule S ?

A. S is serializable only as T1, T2
B. S is serializable only as T2, T1
C. S is serializable both as T1, T2 and T2, T1
D. S is serializable either as T1 or as T2

gate2004-it databases transactions normal

Answer

3.20.8 Transactions: GATE2005-IT-24 top

http://gateoverflow.in/3769

Amongst the ACID properties of a transaction, the 'Durability' property requires that the changes made to the database by a successful transaction persist

A. Except in case of an Operating System crash
B. Except in case of a Disk crash
C. Except in case of a power failure
D. Always, even if there is a failure of any kind

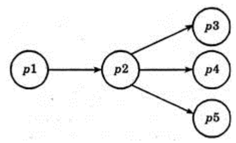
gate2005-it databases transactions easy

Answer

3.20.9 Transactions: GATE2005-IT-66 top

http://gateoverflow.in/3828

In a data flow diagram, the segment shown below is identified as having transaction flow characteristics, with p2 identified as the transaction center



A first level architectural design of this segment will result in a set of process modules with an associated invocation sequence. The most appropriate architecture is

A. p1 invokes p2, p2 invokes either p3, or p4, or p5
B. p2 invokes p1, and then invokes p3, or p4, or p5
C. A new module Tc is defined to control the transaction flow. This module Tc first invokes pl and then invokes p2. p2 in turn invokes p3, or p4, or p5
D. A new module Tc is defined to control the transaction flow. This module Tc invokes p2. p2 invokes p1, and then invokes p3, or p4, or p5

gate2005-it databases transactions normal

Answer

3.20.10 Transactions: GATE2005-IT-67 top

http://gateoverflow.in/3830

A company maintains records of sales made by its salespersons and pays them commission based on each individual's total sales made in a year. This data is maintained in a table with following schema:

salesinfo = (salespersonid, totalsales, commission)

In a certain year, due to better business results, the company decides to further reward its salespersons by enhancing the commission paid to them as per the following formula:

If commission < = 50000, enhance it by 2%
If 50000 < commission < = 100000, enhance it by 4%
If commission > 100000, enhance it by 6%

The IT staff has written three different SQL scripts to calculate enhancement for each slab, each of these scripts is to run as a separate transaction as follows:

T1
```
Update salesinfo
Set commission = commission * 1.02
Where commission < = 50000;
```

T2
```
Update salesinfo
Set commission = commission * 1.04
Where commission > 50000 and commission is < = 100000;
```

T3
```
Update salesinfo
Set commission = commission * 1.06
Where commission > 100000;
```

Which of the following options of running these transactions will update the commission of all salespersons correctly

A. Execute T1 followed by T2 followed by T3
B. Execute T2, followed by T3; T1 running concurrently throughout
C. Execute T3 followed by T2; T1 running concurrently throughout
D. Execute T3 followed by T2 followed by T1

gate2005-it databases transactions normal

Answer

3.20.11 Transactions: GATE2006-20, ISRO2015-17 top http://gateoverflow.in/981

Consider the following log sequence of two transactions on a bank account, with initial balance 12000, that transfer 2000 to a mortgage payment and then apply a 5% interest.

1. T1 start
2. T1 B old=1200 new=10000
3. T1 M old=0 new=2000
4. T1 commit
5. T2 start
6. T2 B old=10000 new=10500
7. T2 commit

Suppose the database system crashes just before log record 7 is written. When the system is restarted, which one statement is true of the recovery procedure?

A. We must redo log record 6 to set B to 10500
B. We must undo log record 6 to set B to 10000 and then redo log records 2 and 3
C. We need not redo log records 2 and 3 because transaction T1 has committed
D. We can apply redo and undo operations in arbitrary order because they are idempotent

gate2006 databases transactions normal isro2015

Answer

3.20.12 Transactions: GATE2007-64 top http://gateoverflow.in/1262

Consider the following schedules involving two transactions. Which one of the following statements is **TRUE**?

- $S_1 : r_1(X); r_1(Y); r_2(X); r_2(Y); w_2(Y); w_1(X)$
- $S_2 : r_1(X); r_2(X); r_2(Y); w_2(Y); r_1(Y); w_1(X)$

A. Both S_1 and S_2 are conflict serializable.

B. S_1 is conflict serializable and S_2 is not conflict serializable.

C. S_1 is not conflict serializable and S_2 is conflict serializable.

D. Both S_1 and S_2 are not conflict serializable.

gate2007 databases transactions normal

Answer

3.20.13 Transactions: GATE2007-IT-66 top http://gateoverflow.in/3511

Consider the following two transactions : T_1 and T2.

T_1 : read (A);
read (B);
if A = 0 then B ← B + 1;
write (B);

T_2 : read (B);
read (A);
if B ≠ 0 then A ← A - 1;
write (A);

Which of the following schemes, using shared and exclusive locks, satisfy the requirements for strict two phase locking for the above transactions?

A.

S1 :	S2 :
lock S(A);	lock S(B);
read (A);	read (B);
lock S(B);	lock S(A);
read (B);	read (A);
if A = 0 then B ← B + 1;	if B ≠ 0 then A ← A - 1;
write (B);	write (A);
commit;	commit;
unlock (A);	unlock (B);
unlock (B);	unlock (A);

B.

S1 :	S2 :
lock X(A);	lock X(B);
read (A);	read (B);
lock X(B);	lock X(A);
read (B);	read (A);
if A = 0 then B ← B + 1;	if B ≠ 0 then A ← A - 1;
write (B);	write (A);
unlock (A);	unlock (A);
commit;	commit;
unlock (B);	unlock (A);

C.

S1 :	S2 :
lock S(A);	lock S(B);
read (A);	read (B);
lock X(B);	lock X(A);
read (B);	read (A);
if A = 0 then B ← B + 1;	if B ≠ 0 then A ← A - 1;
write (B);	write (A);
unlock (A);	unlock (B);
commit;	commit;
unlock	unlock

(B);	(A);

D.

S1	S2
lock : S(A);	lock : S(B);
read (A);	read (B);
lock X(B);	lock X(A);
read (B);	read (A);
if A = 0 then B ← B + 1;	if B ≠ 0 then A ← A - 1;
write (B);	write (A);
unlock (A);	unlock (A);
unlock (B);	unlock (B);
commit;	commit;

gate2007-it databases transactions normal

Answer

3.20.14 Transactions: GATE2008-IT-63 top

http://gateoverflow.in/3374

Consider the following three schedules of transactions T1, T2 and T3. [Notation: In the following NYO represents the action Y (R for read, W for write) performed by transaction N on object O.]

(S1) 2RA 2WA 3RC 2WB 3WA 3WC 1RA 1RB 1WA 1WB
(S2) 3RC 2RA 2WA 2WB 3WA 1RA 1RB 1WA 1WB 3WC
(S3) 2RZ 3RC 3WA 2WA 2WB 3WC 1RA 1RB 1WA 1WB

Which of the following statements is TRUE?

A. S1, S2 and S3 are all conflict equivalent to each other
B. No two of S1, S2 and S3 are conflict equivalent to each other
C. S2 is conflict equivalent to S3, but not to S1
D. S1 is conflict equivalent to S2, but not to S3

gate2008-it databases transactions normal

Answer

3.20.15 Transactions: GATE2009-43 top

http://gateoverflow.in/1329

Consider two transactions T_1 and T_2, and four schedules S_1, S_2, S_3, S_4 , of T_1 and T_2 as given below:

$T_1 : R_1[x]W_1[x]W_1[y]$

$T_2 : R_2[x]R_2[y]W_2[y]$

$S_1 : R_1[x]R_2[x]R_2[y]W_1[x]W_1[y]W_2[y]$

$S_2 : R_1[x]R_2[x]R_2[y]W_1[x]W_2[y]W_1[y]$

$S_3 : R_1[x]W_1[x]R_2[x]W_1[y]R_2[y]W_2[y]$

$S_4 : R_2[x]R_2[y]R_1[x]W_1[x]W_1[y]W_2[y]$

Which of the above schedules are conflict-serializable?

A. S_1 and S_2
B. S_2 and S_3
C. S_3 only
D. S_4 only

gate2009 databases transactions normal

Answer

3.20.16 Transactions: GATE2010-20 top

http://gateoverflow.in/2196

Which of the following concurrency control protocols ensure both conflict serializability and freedom from deadlock?

I. 2-phase locking
II. Time-stamp ordering

A. I only
B. II only
C. Both I and II
D. Neither I nor II

gate2010 databases transactions normal

Answer

3.20.17 Transactions: GATE2010-42 top

http://gateoverflow.in/2343

Consider the following schedule for transactions T1, T2 and T3:

T1	**T2**	**T3**
Read(X)		
	Read(Y)	
		Read(Y)
	Write(Y)	
Write(X)		
		Write(X)
	Read(X)	
	Write(X)	

Which one of the schedules below is the correct serialization of the above?

A. $T1 \to T3 \to T2$
B. $T2 \to T1 \to T3$
C. $T2 \to T3 \to T1$
D. $T3 \to T1 \to T2$

gate2010 databases transactions normal

Answer

3.20.18 Transactions: GATE2012_27 top

http://gateoverflow.in/1612

Consider the following transactions with data items P and Q initialized to zero:

T_1	`read (P);`
	`read (Q);`
	`if P = 0 then Q := Q + 1 ;`
	`write (Q).`

T_2	`read (Q);`
	`read (P);`
	`if Q = 0 then P := P + 1 ;`
	`write (P)`

Any non-serial interleaving of $\mathbf{T_1}$ and $\mathbf{T_2}$ for concurrent execution leads to

(A) a serializable schedule
(B) a schedule that is not conflict serializable
(C) a conflict serializable schedule
(D) a schedule for which a precedence graph cannot be drawn

gate2012 databases transactions normal

Answer

3.20.19 Transactions: GATE2014-1-29 top http://gateoverflow.in/1796

Consider the following four schedules due to three transactions (indicated by the subscript) using *read* and *write* on a data item x, denoted by $r(x)$ and $w(x)$ respectively. Which one of them is conflict serializable?

A. $r_1(x)$; $r_2(x)$; $w_1(x)$; $r_3(x)$; $w_2(x)$;
B. $r_2(x)$; $r_1(x)$; $w_2(x)$; $r_3(x)$; $w_1(x)$;
C. $r_3(x)$; $r_2(x)$; $r_1(x)$; $w_2(x)$; $w_1(x)$;
D. $r_2(x)$; $w_2(x)$; $r_3(x)$; $r_1(x)$; $w_1(x)$;

gate2014-1 databases transactions numerical-answers normal

Answer

3.20.20 Transactions: GATE2014-2-29 top http://gateoverflow.in/1988

Consider the following schedule **S** of transactions T1, T2, T3, T4:

T1	**T2**	**T3**	**T4**
--			
	Reads(X)		
		Writes(X)	
		Commit	
Writes(X)			
Commit			
	Writes(Y)		
	Reads(Z)		
	Commit		
			Reads(X)
			Reads(Y)
			Commit

Which one of the following statements is CORRECT?

A. **S** is conflict-serializable but not recoverable
B. **S** is not conflict-serializable but is recoverable
C. **S** is both conflict-serializable and recoverable
D. **S** is neither conflict-serializable not is it recoverable

gate2014-2 databases transactions normal

Answer

3.20.21 Transactions: GATE2014-3-29 top http://gateoverflow.in/2063

Consider the transactions $T1, T2, \text{and } T3$ and the schedules $S1 \text{ and } S2$ given below.

$T1 : r1(X); r1(Z); w1(X); w1(Z)$

$T2 : r2(Y); r2(Z); w2(Z)$

$T3 : r3(Y); r3(X); w3(Y)$

$S1 : r1(X); r3(Y); r3(X); r2(Y); r2(Z); w3(Y); w2(Z); r1(Z); w1(X); w1(Z)$

$S2: r1(X); r3(Y); r2(Y); r3(X); r1(Z); r2(Z); w3(Y); w1(X); w2(Z); w1(Z)$

Which one of the following statements about the schedules is **TRUE**?

A. Only $S1$ is conflict-serializable.
B. Only $S2$ is conflict-serializable.
C. Both $S1$ and $S2$ are conflict-serializable.
D. Neither $S1$ nor $S2$ is conflict-serializable.

gate2014-3 databases transactions normal

Answer

3.20.22 Transactions: GATE2015-2_1 top http://gateoverflow.in/8047

Consider the following transaction involving two bank accounts x and y.

```
read(x); x:=x-50; write (x); read(y); y:=y+50; write(y)
```

The constraint that the sum of the accounts x and y should remain constant is that of

A. Atomicity
B. Consistency
C. Isolation
D. Durability

gate2015-2 databases transactions easy

Answer

3.20.23 Transactions: GATE2015-2_46 top http://gateoverflow.in/8246

Consider a simple checkpointing protocol and the following set of operations in the log.

(start, T4); (write, T4, y, 2, 3); (start, T1); (commit, T4); (write, T1, z, 5, 7);

(checkpoint);

(start, T2); (write, T2, x, 1, 9); (commit, T2); (start, T3); (write, T3, z, 7, 2);

If a crash happens now and the system tries to recover using both undo and redo operations, what are the contents of the undo list and the redo list?

A. Undo: T3, T1; Redo: T2
B. Undo: T3, T1; Redo: T2, T4
C. Undo: none; Redo: T2, T4, T3, T1
D. Undo: T3, T1, T4; Redo: T2

gate2015-2 databases transactions normal

Answer

3.20.24 Transactions: GATE2015-3_29 top http://gateoverflow.in/8482

Consider the partial Schedule S involving two transactions $T1$ and $T2$. Only the $read$ and the $write$ operations have been shown. The $read$ operation on data item P is denoted by $read(P)$ and $write$ operation on data item P is denoted by $write(P)$.

Schedule S

Time Instance	Transaction id	
	$T1$	$T2$
1	$read(A)$	
2	$write(A)$	
3		$read(C)$
4		$write(C)$
5		$read(B)$
6		

7		$write(B)$ $read(A)$
8		$commit$
9	$read(B)$	

Suppose that the transaction $T1$ fails immediately after time instance 9. Which of the following statements is correct?

A. $T2$ must be aborted and then both $T1$ and $T2$ must be re-started to ensure transaction atomicity
B. Schedule S is non-recoverable and cannot ensure transaction atomicity
C. Only $T2$ must be aborted and then re-started to ensure transaction atomicity
D. Schedule S is recoverable and can ensure transaction atomicity and nothing else needs to be done

gate2015-3 databases transactions normal

Answer

Answers: Transactions

3.20.1 Transactions: GATE 2016-1-22 top

http://gateoverflow.in/39644

Selected Answer

A- Atomicity
C- Consistency
I-Isolation
D-Durability..
Answer D

21 votes -- Abhilash Panicker (8.8k points)

3.20.2 Transactions: GATE 2016-1-51 top

http://gateoverflow.in/39703

Selected Answer

Two Phase Locking protocol is conflict serializable. So this is a modified version of the basic 2PL protocol, So serializabilty should be guarenteed.. and we can get a serializable scheduling by ordering based on Lock points(same as in basic 2PL).. Now in Step 1, exclusive locks are aquired to O_1,O_2,O_3.... in increasing order of addresses..since it is mentioned as exclusive lock, only one transaction can lock the object..
`Due to acquiring of locks based on ordering of addresses.. and locks aren't released until the transaction completes its operation.. we can prevent the circular wait condition`, and hence making it deadlock free.

So, the answer should be A) guarentees serializability and deadlock freedom

31 votes -- Abhilash Panicker (8.8k points)

3.20.3 Transactions: GATE 2016-2-22 top

http://gateoverflow.in/39550

Selected Answer

Topological Order.

15 votes -- Sharathkumar Anbu (717 points)

3.20.4 Transactions: GATE1999_2.6 top

http://gateoverflow.in/1484

Selected Answer

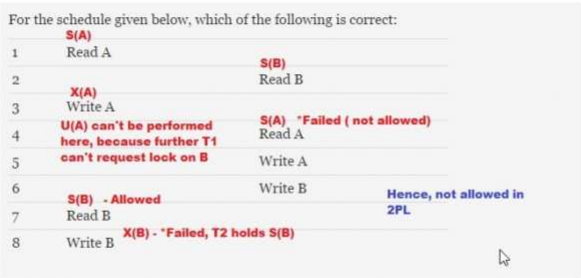
2PL ---> Conflict Serializable Schedule (if p then q)

Precedence graph of this given schedule is cyclic hence, this shcedule is not CSS hence not allowed by 2PL (contra positive)

This schedule is not even serializable because
if T1->T2 we'll lose Last Updated by T1 on item B
if T2->T1 we'll lose initial value of A read by T1

Hence (D) is correct choice!

Why 2PL won't allow this schedule:


For the schedule given below, which of the following is correct:

1	S(A) Read A		
2		S(B) Read B	
3	X(A) Write A		
4	U(A) can't be performed here, because further T1 can't request lock on B	S(A) *Failed (not allowed) Read A	
5		Write A	
6		Write B	Hence, not allowed in 2PL
7	S(B) - Allowed Read B		
8	Write B X(B) - *Failed, T2 holds S(B)		

8 votes -- Vijay Thakur (15.4k points)

3.20.5 Transactions: GATE2003-29, ISRO2009-73 top http://gateoverflow.in/919

Selected Answer

D) This is dirty read. In case if transaction reading uncommited data commits, irrecoverable error occurs of uncommited transaction fails. So D is answer

B) This is non issue.Both transaction reading data.

C) This is non issue.

A) Here if transaction writing data commits , then transaction which read the data might get phantom tuple/ Unrepeatable error. Though there is no irrecoverable error possible even in this option.

17 votes -- Akash (43.8k points)

3.20.6 Transactions: GATE2003-87 top http://gateoverflow.in/970

Selected Answer

der is cycle in precedence graph so schedule is not conflict serialisable.
check View Serialization.
checking View Serialization is NPC problem so proving by contradiction..

1. Initial Read
T2 read D2 value from initial database and T1 modify D2 so T2 should execute before T1.
i.e. T2 ------> T1
2. final write.
final write of D1 in given schedule done by T2 and T1 modify D1 i.e. W(D1)..
that means T2 should execute after T1..
i.e. T1 -------> T2

clearly schedule not even view Serializable.
Not Serializable..

14 votes -- Digvijay (47k points)

3.20.7 Transactions: GATE2004-IT-77 top http://gateoverflow.in/3721

Selected Answer

This schedule is not serializable(not even view serializable). So none of the first 3 options match. Option (d), even I don't understand.

According to me there should have been an option saying that schedule is not serializable; neither as T1,T2 nor as T2,T1.

17 votes -- Sandeep_Uniyal (7.3k points)

3.20.8 Transactions: GATE2005-IT-24 top

http://gateoverflow.in/3769

Selected Answer

answer d. irrespective of any failure the successful result of transaction should persist.

suppose we book ticket 2 months in advance in irctc and transaction success

then when we are going to board the train on that time they tells because of system/disk/power crash they dont have your seat information and you are not allowed in the seat

it is a serious problem. hence result should persist irrespective of all crashes

33 votes -- Sankaranarayanan P.N (11.2k points)

3.20.9 Transactions: GATE2005-IT-66 top

http://gateoverflow.in/3828

Selected Answer

Answer: C

A new module T_c is defined to invoke p1 as p1 isn't being invoked in the diagram. Later, p1 invokes p2 which then invokes p3, p4 or p5.

9 votes -- Rajarshi Sarkar (35k points)

3.20.10 Transactions: GATE2005-IT-67 top

http://gateoverflow.in/3830

Selected Answer

T3 followed by T2 followed by T1 will be correct execution sequence

other cases some people will get two times increment

eg if we have T1 followed by T2

if initial commision is 49500

then he is belonging to < 50000

hence 49500*1.02 = 50490

now he is eligible in second category

then 50490*1.04 = 52509.6

so he wil get increment two times. but he is eligible for only one slab of commision

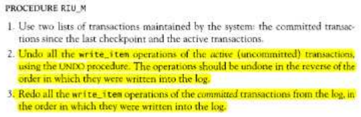
21 votes -- Sankaranarayanan P.N (11.2k points)

3.20.11 Transactions: GATE2006-20, ISRO2015-17 top

http://gateoverflow.in/981

Selected Answer

ans should be B here we arent using checkpoints so redo log records 2 and 3 and undo log record 6.
Consider the following screenshot taken from the book 'Navathe':



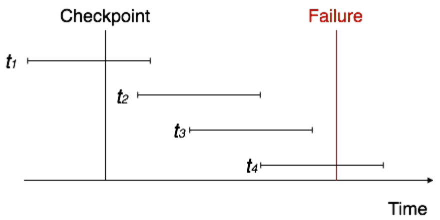
PROCEDURE RIU_M

1. Use two lists of transactions maintained by the system: the committed transactions since the last checkpoint and the active transactions.
2. Undo all the `write_item` operations of the *active* (uncommitted) transactions, using the UNDO procedure. The operations should be undone in the reverse of the order in which they were written into the log.
3. Redo all the `write_item` operations of the *committed* transactions from the log, in the order in which they were written into the log.

32 votes -- Pooja Palod (32.4k points)

Checkpoint : Checkpoint is a mechanism where all the previous logs are removed from the system and stored permanently in a storage disk. Checkpoint declares a point before which the DBMS was in consistent state, and all the transactions were committed.

When a system with concurrent transactions crashes and recovers, it behaves in the following manner −



=>The recovery system reads the logs backwards from the end to the last checkpoint.

=>It maintains two lists, an undo-list and a redo-list.

=>If the recovery system sees a log with <tn, start=""> and <tn, commit=""> or just <tn, commit="">, it puts the transaction in the redo-list.

=>If the recovery system sees a log with <tn, start=""> but no commit or abort log found, it puts the transaction in undo-list.

All the transactions in the undo-list are then undone and their logs are removed. All the transactions in the redo-list and their previous logs are removed and then redone before saving their logs

so we must undo log record 6 to set B to 10000 and then redo log records 2 and 3 because system fail before commit operation. So we need to undone active transactions(T2) and redo committed transactions (T1)

So Answer is B redo log records 2 and 3 and undo log record 6

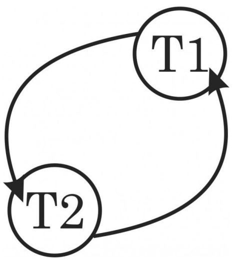
17 votes -- Leen Sharma (32.3k points)

3.20.12 Transactions: GATE2007-64 top

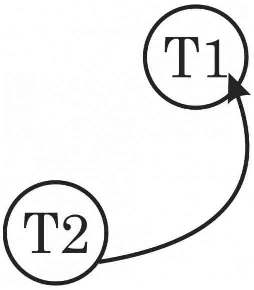
http://gateoverflow.in/1262

Selected Answer

For $S1$: it is **not conflict serializable**



for $S2$: it is **conflict serializable**



answer = **option C**

15 votes -- Amar Vashishth (28.7k points)

3.20.13 Transactions: GATE2007-IT-66 top http://gateoverflow.in/3511

Selected Answer

Answer is (C)

Many of you would point a DEADLOCK and I won't deny But see Question just asks for requirement to follow Strict 2PL .Requirement is that

1. Exclusive locks should be released after the commit . and

2. No Locking can be done after the first Unlock and vice versa.

In 2Pl deadlock may occur BUT it may be that it doesn't occur at all.

Consider that in option (C) if both execute in serial order without concurrency.Then that is perfectly valid and YES it follows Strict 2PL.

17 votes -- Sandeep_Uniyal (7.3k points)

3.20.14 Transactions: GATE2008-IT-63 top http://gateoverflow.in/3374

Selected Answer

Though answer is (D) but it seems that it's a miss printing in schedule (S3) because being conflict equivalent there should same operations on same data items.
first operation in schedule (S3) should be 2RA
Furthermore, if it's 2RA in S3 then S3 is not even Conflict Serializable schedule.

5 votes -- Vijay Thakur (15.4k points)

3.20.15 Transactions: GATE2009-43 top http://gateoverflow.in/1329

Selected Answer

The answer is B.

S1 has a cycle from T1-->T2 and T2-->T1.

S2-- . It is uni-directional and has only T2-->T1.

S3-- It is uni-directional and has only T1-->T2.

S4-- same as S1.

A schedule is conflict serializable if there is no cycle in the directed graph made by the schedules.

In the schedules we check for RW, WR, WW conflicts between the schedules. and these conflicts only contribute in the edges of the graph.

11 votes -- Gate Keeda (19.1k points)

3.20.16 Transactions: GATE2010-20 top

http://gateoverflow.in/2196

Selected Answer

in basic two phase locking there is a chance for deadlock

conservative 2pl is deadlock free

i go with B

22 votes -- Sankaranarayanan P.N (11.2k points)

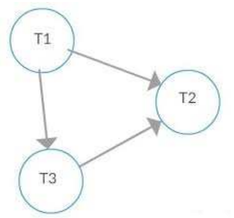
3.20.17 Transactions: GATE2010-42 top

http://gateoverflow.in/2343

Selected Answer

answer = **option A**

create precedence graph and apply Topological sort on it to obtain
$T1 \rightarrow T3 \rightarrow T2$



20 votes -- Amar Vashishth (28.7k points)

3.20.18 Transactions: GATE2012_27 top

http://gateoverflow.in/1612

Selected Answer

Ans is (B): explanation: T1:r(P),r(Q),w(Q) T2:r(Q),r(P),w(P) now consider any non serial schedule for example, S:r1(P),r2(Q),r1(Q),r2(P),w1(Q),w2(P) now draw a precedence graph for this schedule. here there is a conflict from T1->T2 and there is a conflict from T2->T1 therefore, the graph will contain a cycle. so we can say that the schedule is not conflict serializable.

36 votes -- jayendra (8.1k points)

3.20.19 Transactions: GATE2014-1-29 top

http://gateoverflow.in/1796

Selected Answer

(D) make precedence graph for all the options, for option D only graph will be acyclic, hence D is CSS.

8 votes -- Manu Thakur (6k points)

3.20.20 Transactions: GATE2014-2-29 top

http://gateoverflow.in/1988

Selected Answer

Answer: S is both conflict serializable and recoverable.

Recoverable? Look if there are any dirty reads? Since there are no dirty read, it simply implies schedule is recoverable(if there were dirty read, then we would have taken into consideration the order in which transactions commit)

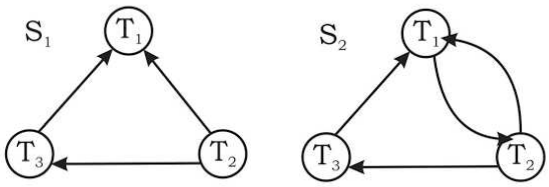
Conflict serializable? Draw the precedence graph(make edges if there is a conflict instruction among Ti and Tj. But for the given schedule, no cycle exists in precedence graph, thus it's conflict serializable.

Hope this helps.

17 votes -- Ramandeep Singh (175 points)

3.20.21 Transactions: GATE2014-3-29 top http://gateoverflow.in/2063

Selected Answer



S_1 has no cycle hence, **Conflict-Serializable**

S_2 has cycle hence **NOT Conflict-Serializable**

answer = **option A**

18 votes -- Amar Vashishth (28.7k points)

3.20.22 Transactions: GATE2015-2_1 top http://gateoverflow.in/8047

Selected Answer

B. Consistency

In the given transaction Atomicity guarantees that the said constraint is satisfied. But this constraint is not part of Atomicity property. It is just that Atomicity implies Consistency here.

11 votes -- Arjun Suresh (294k points)

3.20.23 Transactions: GATE2015-2_46 top http://gateoverflow.in/8246

Selected Answer

T1	T2	T3	T4
			start
			W(y,2,3)
start			
			commit
W(z,5,7)			
Checkpoint	Checkpoint	Checkpoint	Checkpoint
	start		
	W(x,1,9)		
	commit		
		start	
		W(z,7,2)	
crash	crash	crash	crash

Now from the table we can find , T1 and T3 has uncommitted write operation , so they must be undone. and even though T2 has committed after writing , but it is after checkpoint. So , it needs to be redone. So answer is A.

26 votes -- worst_engineer (5.6k points)

3.20.24 Transactions: GATE2015-3_29 top http://gateoverflow.in/8482

Selected Answer

I think the correct option is B.

Why A is not correct **because it says abort transaction T2 and then redo all the operations .**

But is there a gaurantee that it will succed this time ??(no maybe again T1 will fail)..

now as to why b is correct **because as the other answer points out it is by definition an irrecoverable schedule** now even if **we start to undo the actions on by one(after t1 fails) in order to ensure transaction atomicity. Still we cannot undo a commited transaction.** hence this schedule is unrecoverable by definition and also not atomic since it leaves the data base in an inconsistent state.

25 votes -- Tamojit Chatterjee (2.2k points)

3.21 Uniform Distribution(1) top

3.21.1 Uniform Distribution: GATE2007-IT-65 top http://gateoverflow.in/3510

Consider a selection of the form $\sigma_{A \leq 100}(r)$, where r is a relation with 1000 tuples. Assume that the attribute values for A among the tuples are uniformly distributed in the interval [0, 500]. Which one of the following options is the best estimate of the number of tuples returned by the given selection query ?

A. 50
B. 100
C. 150
D. 200

gate2007-it databases relational-calculus probability uniform-distribution normal

Answer

Answers: Uniform Distribution

3.21.1 Uniform Distribution: GATE2007-IT-65 top http://gateoverflow.in/3510

Selected Answer

$\sigma_{A \leq 100}(r)$
r has 1000 tuples

Values for A among the tuples are uniformly distributed in the interval [0, 500]. This can be split to 5 mutually exclusive (non-overlapping) and exhaustive (no other intervals) intervals of same width of 100 ([0-100], [101-200], [201-300], [301-400], [401-500], 0 makes the first interval larger - this must be a typo in question) and we can assume all of them have same number of values due to Uniform distribution. So, number of tuples with A value in first interval should be

$$\frac{\text{Total no. of tuples}}{5} = 1000/5 = 200$$

19 votes -- Abhinav Rana (707 points)

4 Digital Logic (238) top

4.1 Adder(7) top

4.1.1 Adder: GATE 2016-1-33 top

http://gateoverflow.in/39688

Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

A. $\Theta(1)$
B. $\Theta(\log(n))$
C. $\Theta(\sqrt{n})$
D. $\Theta(n)$)

gate2016-1 digital-logic adder normal

Answer

4.1.2 Adder: GATE 2016-2-07 top

http://gateoverflow.in/39575

Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is ___________

gate2016-2 digital-logic adder normal numerical-answers

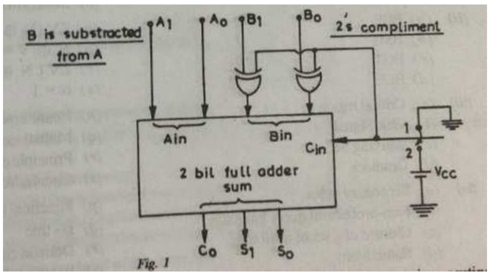
Answer

4.1.3 Adder: GATE1990-1-i top

http://gateoverflow.in/83829

Fill in the blanks:

In the two bit full-adder/subtractor unit shown in below figure, when the switch is in position 2 ___________ using _________ arithmetic.



gate1990 digital-logic adder

Answer

4.1.4 Adder: GATE1997-2.5 top

http://gateoverflow.in/2231

An N-bit carry lookahead adder, where N is a multiple of 4, employs ICs 74181 (4 bit ALU) and 74182 (4 bit carry lookahead generator).

The minimum addition time using the best architecture for this adder is

A. proportional to N

B. proportional to $\log N$

C. a constant

D. None of the above

gate1997 digital-logic normal adder

Answer

4.1.5 Adder: GATE1999-2.16 top

http://gateoverflow.in/1494

The number of full and half-adders required to add 16-bit numbers is

A. 8 half-adders, 8 full-adders

B. 1 half-adder, 15 full-adders

C. 16 half-adders, 0 full-adders

D. 4 half-adders, 12 full-adders

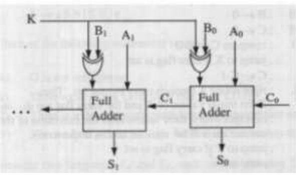
gate1999 digital-logic normal adder

Answer

4.1.6 Adder: GATE2003-46 top

http://gateoverflow.in/937

Consider the ALU shown below.



If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines *K* and C_0 only (+ and – denote addition and subtraction respectively)?

A. $A+B$, and $A–B$, but not $A+1$
B. $A+B$, and $A+1$, but not $A–B$
C. $A+B$, but not $A–B$ or $A+1$
D. $A+B$, and $A–B$, and $A+1$

gate2003 digital-logic normal adder

Answer

4.1.7 Adder: GATE2004-62 top

http://gateoverflow.in/1057

A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

A. 4 time units
B. 6 time units
C. 10 time units
D. 12 time units

gate2004 digital-logic normal adder

Answer

Answers: Adder

4.1.1 Adder: GATE 2016-1-33 top

http://gateoverflow.in/39688

Selected Answer

Look ahead carry generator gives output in constant time if fan in = number of inputs.

Example, it will take O(1) to calculate $c_4 = g_3 + p_3g_2 + p_3p_2g_1 + p_3p_2p_1g0 + p_3p_2p_1p_0c_0$, if OR gate with 5 inputs is present.

If we have 8 inputs, and OR gate with 2 inputs, to build an OR gate with 8 inputs, we will need 4 gates in level-1, 2 in level-2 and 1 in level-3. Hence 3 gate delays, for each level.

Similarly an n-input gate constructed with 2-input gates, total delay will be O(log n).

Hence **answer is option B**.

23 votes -- ryan sequeira (3k points)

option "b"

$O(\log_2 n)$

because as fan-in is at most 2 then we can use two variable to the i/p of one XOR gate and then one i/p and one o/p from previous XOR gate and so, on ..

https://www.cs.umd.edu/class/fall2003/cmsc311/Lectures/lecture22/lookahead.pdf

13 votes -- Gate Target (101 points)

4.1.2 Adder: GATE 2016-2-07 top http://gateoverflow.in/39575

Selected Answer

ans is -1.

in case of -1 we get bit sequence 11111111 adding this we get a carry upto carry flag,so largest time to ripple !

20 votes -- viv696 (2.2k points)

4.1.3 Adder: GATE1990-1-i top http://gateoverflow.in/83829

Selected Answer

When the switch is at position 2 , it is connected to Vcc thus , the value of control input M = 1 which is fed to XOR gates as well..So

$B_1 \oplus 1 = B_1'$ and

$B_0 \oplus 1 = B_0'$ ..

And the basic hardware is of adder only..

Now C_{in} is connected to V_{cc} as well hence $C_{in} = 1$.

Hence net operation can be denoted as : $S_0 = A_0 + B_0' + 1$ and similarly for S_1 as well..

So this is nothing but an expression of substraction using 2's complement ..(Had it been $A_0 + B_0'$, it would have been addition of 1's complement merely but for substraction we need to have 2's complement of other operand which is B here)..

Hence the correct answer should be : substraction , 2's complement

4 votes -- HABIB MOHAMMAD KHAN (76.8k points)

4.1.4 Adder: GATE1997-2.5 top http://gateoverflow.in/2231

Selected Answer

For N = 64 bits

Suppose you want to build a 64 bit adder then you need 16 4-bit ALU and 16 4-bit carry generator, at this point there will be 16 carries that will ripple through these 16 ALU modules, to speed up the adder we need to get rid of these 16 rippling carries, now we can again use 4 4-bit carry generator to generate these 16 carries, now we have only 4 carries to ripple through, again we can use the same trick to minimize the rippling of these 4 carries, we can use an additional 4-bit carry generator which will generate these carry and we are done :) there will be no more propagation of carry among the ALU modules.

So the we have used 3 level of 4-bit carry generator, and the time taken to add 64 bits will be proportional to 3 which is $\log_4 64$.

So in general to add N-bits it takes $\text{Log}_4 N$ time.

11 votes -- Vikrant Singh (13.4k points)

4.1.5 Adder: GATE1999-2.16 top

http://gateoverflow.in/1494

Selected Answer

answer - B

for LSB addition we do not need a full adder

for addition of subsequent bits we need full adders since carry from previous addition has to be fed into the addition operation

16 votes -- ankitrokdeonsns (9.1k points)

4.1.6 Adder: GATE2003-46 top

http://gateoverflow.in/937

Selected Answer

There are two control line one is K and another is C_0 .

When $K = 1$, $C_0 = 1$ we can perform $A - B$

When $K = 0$, $C_0 = 0$ we can perform $A + B$

But without manipulating $B(B_0, B_1 \ldots.)$ we cannot perform A+1. But here we have only two control lines which is K, C_0. Therefore the answer is A.

Note:

For A+B,
$C_0 = 0$ ***,***
$K = 1$***, and***
$0 \oplus x = x$

$$\begin{array}{ccccc} & A3 & A2 & A1 & A0 \\ + & B3 & B2 & B1 & B0 \\ \hline & S3 & S2 & S1 & S0 \end{array}$$

$$\begin{array}{rcccc} & C3 & C2 & C1 & C0{=}0 \\ & A3 & A2 & A1 & A0 \\ + & B3 & B2 & B1 & B0 \\ \hline Sum\ \ Output: & S3 & S2 & S1 & S0 \\ Carry\ \ Output: & C4 & C3 & C2 & C1 \end{array}$$

For A- B,
$C_0 = 1$ ***,***
$K = 1$***, and***

$1 \oplus x = \bar{x}$

Subtraction Using 1's complement, (A -B)

1. Find 1's complement of B= $2^n - 1 - B$, We do 1's complement but change bits 0 to 1 or 1 to 0 (where n is no of bits)

2. Add A , $2^n - 1 - B + A = 2^n - 1 + (A - B)$ but we need only A-B , 2^n is last carry , That is, C_4 will be discarded, to remove -1, add $C_0 = 1$.

$$\begin{array}{ccccc} & A3 & A2 & A1 & A0 \\ - & B3 & B2 & B1 & B0 \\ \hline & S3 & S2 & S1 & S0 \end{array}$$

Subtraction using 1's complement

$$\begin{array}{cccccc} & & C3 & C2 & C1 & C0{=}1 \\ & & A3 & A2 & A1 & A0 \\ & + & \overline{B3} & \overline{B2} & \overline{B1} & \overline{B0} \\ \hline Sum\ \ Output: & & S3 & S2 & S1 & S0 \\ Carry\ \ Output: & & C4 & C3 & C2 & C1 \end{array}$$

7 votes -- Riya Roy(Arayana) (7.1k points)

4.1.7 Adder: GATE2004-62 top

http://gateoverflow.in/1057

Selected Answer

It would take 6 time units.

We know that

$G_i = A_i B_i$,

$P_i = A_i \oplus B_i$ and

$S_i = P_i \oplus C_i$

Also

$C_1 = G_0 + P_0 C_0$

$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

XOR can be implemented in 2 levels; level-1 ANDs and Level-2 OR. Hence it would take 2 time units to calculate P_i and S_i

The 4-bit addition will be calculated in 3 stages

1. **(2 time units)** In 2 time units we can compute G_i and P_i in parallel. 2 time units for P_i since its an XOR operation and 1 time unit for G_i since its an AND operation.

2. **(2 time units)** Once G_i and P_i are available, we can calculate the caries, C_i, in 2 time units.

   Level-1 we compute all the conjunctions (AND). Example $P_3 G_2, P_3 P_2 G_1, P_3 P_2 P_1 G_0$ and

$P_3P_2P_1P_0C_0$ which are required for C_4.

Level-2 we get the carries by computing the disjunction (OR).

3. **(2 time units)** Finally we compute the Sum in 2 time units, as its an XOR operation.

Hence the total is 2 + 2 + 2 = **6 time units**.

20 votes -- ryan sequeira (3k points)

4.2 Array Multiplier(2) top

4.2.1 Array Multiplier: GATE1999-1.21 top http://gateoverflow.in/1474

The maximum gate delay for any output to appear in an array multiplier for multiplying two n bit numbers is

A. $O(n^2)$
B. $O(n)$
C. $O(\log n)$
D. $O(1)$

gate1999 digital-logic normal array-multiplier

Answer

4.2.2 Array Multiplier: GATE2003-11 top http://gateoverflow.in/902

Consider an array multiplier for multiplying two n bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is

A. $\Theta(1)$
B. $\Theta(\log n)$
C. $\Theta(n)$
D. $\Theta(n^2)$

gate2003 digital-logic normal array-multiplier

Answer

Answers: Array Multiplier

4.2.1 Array Multiplier: GATE1999-1.21 top http://gateoverflow.in/1474

Selected Answer

In a N X M array multiplier we have N * M AND gates and (M-1) N bit adders used.

Total delay in N X M (N>=M) array multiplier due to AND gate in partial products at all level is just 1 unit AND gate delay as the operation is done parallel wise at each step. Now delays at level 1 to (M-1) is = (M-1)*delay due to 1 unit of N bit adder. Therefore the maximum gate delay is O(M) but here M=N therefore O(N).

http://www.dauniv.ac.in/downloads/CArch_PPTs/CompArchCh03L06ArrayMult.pdf

Refer this article page 16.

3 votes -- Riya Roy(Arayana) (7.1k points)

4.2.2 Array Multiplier: GATE2003-11 top http://gateoverflow.in/902

Selected Answer

Take A = A1 A2 A3 A4

B= B1 B2 B3 B4

NOW TO MULTIPLY THESE TWO NUMBER .

1 AND GATE REQUIRE B1 MULTIPLY WITH A1 A2 A3 A4.

1 AND GATE REQUIRE B2 MULTIPLY WITH A1 A2 A3 A4.

1 AND GATE REQUIRE B3 MULTIPLY WITH A1 A2 A3 A4.

1 AND GATE REQUIRE B4 MULTIPLY WITH A1 A2 A3 A4.

NOW 3 OR GATE REQUIRE.

TOTAL 7 GATE REQUIRE FOR 4 BIT TAKE N BIT U FIND 2N-1.

SO TIME COMPLEXITY WILL BE = Θ(n)

9 votes -- Prashant Singh (49.2k points)

4.3 Boolean Algebra(4) top

4.3.1 Boolean Algebra: GATE 2016-2-08 top http://gateoverflow.in/39540

Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and $\oplus$ is the XOR operator.

Which one of the following must always be **TRUE**?

A. $x_1 x_2 x_3 x_4 = 0$
B. $x_1 x_3 + x_2 = 0$
C. $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
D. $x_1 + x_2 + x_3 + x_4 = 0$

gate2016-2 digital-logic boolean-algebra normal

Answer

4.3.2 Boolean Algebra: GATE1987-1-II top http://gateoverflow.in/80032

The total number of Boolean functions which can be realised with four variables is:

A. 4
B. 17
C. 256
D. $65,536$

gate1987 digital-logic boolean-algebra functions permutations-and-combinations

Answer

4.3.3 Boolean Algebra: GATE2000-2.10 top http://gateoverflow.in/657

The simultaneous equations on the Boolean variables x, y, z and w,

$$x + y + z = 1 xy = 0 xz + w = 1 xy + \bar{z}\bar{w} = 0$$

have the following solution for x, y, z and w, respectively:

A. 0 1 0 0
B. 1 1 0 1
C. 1 0 1 1

D. 1 0 0 0

gate2000 digital-logic boolean-algebra easy

Answer

4.3.4 Boolean Algebra: TIFR2010-B-21 top

http://gateoverflow.in/18621

For $x \in \{0,1\}$, let $\neg x$ denote the negation of x, that is

$$\neg x = \begin{cases} 1 & \text{iff } x = 0 \\ 0 & \text{iff } x = 1 \end{cases}$$

.

If $x \in \{0,1\}^n$, then $\neg x$ denotes the component wise negation of x; that is:

$(\neg x)_i =$ $\Big($

Consider a circuit C, computing a function $f : \{0,1\}^n \to \{0,1\}$ using **AND** $(\wedge)$, **OR** $(\vee)$,and **NOT** $(\neg)$ gates. Let D be the circuit obtained from C by replacing each **AND** gate by an **OR** gate and replacing each **OR** gate by an **AND**. Suppose D computes the function g. Which of the following is true for all inputs x?

a. $g(x) = \neg f(x)$
b. $g(x) = f(x) \wedge f(\neg x)$
c. $g(x) = f(x) \vee f(\neg x)$
d. $g(x) = \neg f(\neg x)$
e. None of the above.

tifr2010 digital-logic boolean-algebra

Answer

Answers: Boolean Algebra

4.3.1 Boolean Algebra: GATE 2016-2-08 top

http://gateoverflow.in/39540

Selected Answer

Let $x_1 = 1$ $x_2 = 1$ $x_3 = 1$ and $x_4 = 1$

such that $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 1 \oplus 1 \oplus 1 \oplus 1 = 0$

option A) $x_1 x_2 x_3 x_4 = 1.1.1.1 = 1$, False

option B) $x_1 x_3 + x_2 = 1.1 + 1 = 1$, False

option D) $x_1 + x_2 + x_3 + x_4 = 1 + 1 + 1 + 1 = 1$, False.

Option C) is always True.

20 votes -- Praveen Saini (53.6k points)

4.3.2 Boolean Algebra: GATE1987-1-II top

http://gateoverflow.in/80032

Selected Answer

A Boolean function of 4 variables is a function from a set of $2^4 = 16$ elements (all combinations of 4 variables) to a set of 2 $(\{0,1\})$ elements. So, number of such functions will be $2^{16} = 65,536$

9 votes -- Prashant Singh (49.2k points)

4.3.3 Boolean Algebra: GATE2000-2.10 top http://gateoverflow.in/657

Selected Answer

Take each option one by one and try to put the values of x ,y ,z , and w in question

1.

0+1+0 =1

0.1 =0

0.0+0 =0 (went wrong) ....SO this is not the right option

2.

1+1+0 =1

1.1 =1 (went wrong) ....not right

3 .

1+0+1 =1

1.0 =0

1.1+1=1

1.0 +1.0 =0 .....This is the right option

7 votes -- shekhar chauhan (42.9k points)

4.3.4 Boolean Algebra: TIFR2010-B-21 top http://gateoverflow.in/18621

Selected Answer

Option d is answer.

The circuit D is the dual of the function f(x)(i.e., replace and by or and vice versa)

We can find dual of any function f(x) by $\neg f(\neg x)$

5 votes -- Mari Ganesh Kumar (2.2k points)

4.4 Boolean Expressions(20) top

4.4.1 Boolean Expressions: GATE 2016-1-06 top http://gateoverflow.in/39629

Consider the Boolean operator # with the following properties :

x#0=x, x#1=$\overline{x}$,x#x=0 and x# $\overline{x}$=1. Then x#y is equivalent to

A. $x\overline{y} + \overline{x}y$
B. $x\overline{y} + \overline{x}\,\overline{y}$
C. $\overline{x}y + xy$
D. $xy + \overline{x}\,\overline{y}$

gate2016-1 digital-logic boolean-expressions easy

Answer

4.4.2 Boolean Expressions: GATE1987-12a top http://gateoverflow.in/82556

The Boolean expression $A \oplus B \oplus A$ is equivalent to

A. $AB + \bar{A}\bar{B}$
B. $\bar{A}B + A\bar{B}$
C. B
D. $\bar{A}$

gate1987 digital-logic boolean-expressions

Answer

4.4.3 Boolean Expressions: GATE1988-2iii top http://gateoverflow.in/91679

Let $*$ be defined as a Boolean operation given as $x * y = \bar{x}\bar{y} + xy$ and let $C = A * B$. If $C = 1$ then prove that $A = B$.

gate1988 digital-logic descriptive boolean-expressions

Answer

4.4.4 Boolean Expressions: GATE1989-5a top http://gateoverflow.in/88230

Find values of Boolean variables A, B, C which satisfy the following equations:

- A+ B = 1
- AC = BC
- A + C = 1
- AB = 0

gate1989 descriptive digital-logic boolean-expressions

Answer

4.4.5 Boolean Expressions: GATE1994-4 top http://gateoverflow.in/2500

a. Let $*$ be a Boolean operation defined as $A * B = AB + \overline{A}\,\overline{B}$. If $C = A * B$ then evaluate and fill in the blanks:
   i. $A * A = \_\_\_\_$
   ii. $C * A = \_\_\_\_$
b. Solve the following boolean equations for the values of A, B and C:
   $AB + \overline{A}C = 1$
   $AC + B = 0$

gate1994 digital-logic normal boolean-expressions

Answer

4.4.6 Boolean Expressions: GATE1995_2.5 top http://gateoverflow.in/2617

What values of A, B, C and D satisfy the following simultaneous Boolean equations?

$\overline{A} + AB = 0, AB = AC, AB + A\overline{C} + CD = \overline{C}D$

A. $A = 1, B = 0, C = 0, D = 1$

B. $A = 1, B = 1, C = 0, D = 0$

C. $A = 1, B = 0, C = 1, D = 1$

D. $A = 1, B = 0, C = 0, D = 0$

gate1995 digital-logic boolean-expressions easy

Answer

4.4.7 Boolean Expressions: GATE1997-2.1 top http://gateoverflow.in/2227

Let $*$ be defined as $x * y = \bar{x} + y$. Let $z = x * y$. Value of $z * x$ is

A. $\bar{x} + y$
B. x
C. 0
D. 1

gate1997 digital-logic normal boolean-expressions

Answer

4.4.8 Boolean Expressions: GATE2002-2.3 top http://gateoverflow.in/833

Let $f(A, B) = A' + B$. Simplified expression for function $f(f(x + y, y), z)$ is

A. $x' + z$
B. xyz
C. $xy' + z$
D. None of the above

gate2002 digital-logic boolean-expressions normal

Answer

4.4.9 Boolean Expressions: GATE2004-17 top http://gateoverflow.in/1014

A Boolean function $x'y' + xy + x'y$ is equivalent to

A. $x' + y'$
B. $x + y$
C. $x + y'$
D. $x' + y$

gate2004 digital-logic easy boolean-expressions

Answer

4.4.10 Boolean Expressions: GATE2004-IT-44 top http://gateoverflow.in/3687

The function AB′C + A′BC + ABC′ + A′B′C + AB′C′ is equivalent to

A. AC′ + AB + A′C
B. AB′ + AC′ + A′C
C. A′B + AC′ + AB′
D. A′B + AC + AB′

gate2004-it digital-logic boolean-expressions easy

Answer

4.4.11 Boolean Expressions: GATE2005-IT-7 top http://gateoverflow.in/3752

Which of the following expressions is equivalent to $(A \oplus B) \oplus C$

A. $(A + B + C)(\bar{A} + \bar{B} + \bar{C})$
B. $(A + B + C)(\bar{A} + \bar{B} + C)$
C. $ABC + \bar{A}(B \oplus C) + \bar{B}(A \oplus C)$
D. None of these

gate2005-it digital-logic normal boolean-expressions

Answer

4.4.12 Boolean Expressions: GATE2007-32 top

http://gateoverflow.in/1230

Let $f(w, x, y, z) = \sum(0, 4, 5, 7, 8, 9, 13, 15)$. Which of the following expressions are NOT equivalent to f?

P: $x'y'z' + w'xy' + wy'z + xz$

Q: $w'y'z' + wx'y' + xz$

R: $w'y'z' + wx'y' + xyz + xy'z$

S: (S) $x'y'z' + wx'y' + w'y$

A. P only
B. Q and S
C. R and S
D. S only

gate2007 digital-logic normal boolean-expressions

Answer

4.4.13 Boolean Expressions: GATE2007-33 top

http://gateoverflow.in/1231

Define the connective $*$ for the Boolean variables X and Y as:

$$X * Y = XY + X'Y'.$$

Let $Z = X * Y$. Consider the following expressions P, Q and R.

$$P : X = Y * Z, Q : Y = X * Z, R : X * Y * Z = 1$$

Which of the following is **TRUE**?

A. Only P and Q are valid.
B. Only Q and R are valid.
C. Only P and R are valid.
D. All P, Q, R are valid.

gate2007 digital-logic normal boolean-expressions

Answer

4.4.14 Boolean Expressions: GATE2008-26 top

http://gateoverflow.in/424

If P, Q, R are Boolean variables, then

$(P + \bar{Q})(P.\bar{Q} + P.R)(\bar{P}.\bar{R} + \bar{Q})$ simplifies to

A. $P.\bar{Q}$

B. $P.\bar{R}$

C. $P.\bar{Q} + R$

D. $P.\bar{R} + Q$

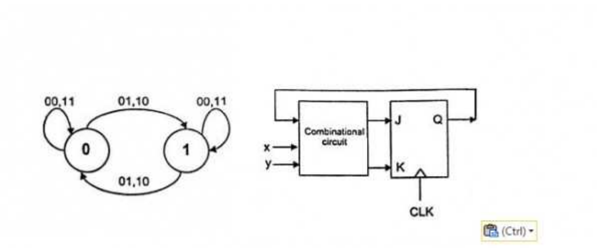
gate2008 easy digital-logic boolean-expressions

Answer

4.4.15 Boolean Expressions: GATE2008-IT-37 top

http://gateoverflow.in/3347

Consider the following state diagram and its realization by a JK flip flop



The combinational circuit generates J and K in terms of x, y and Q.
The Boolean expressions for J and K are :

A. $\overline{x \oplus y}$ and $\overline{x \oplus y}$
B. $\overline{x \oplus y}$ and $x \oplus y$
C. $x \oplus y$ and $\overline{x \oplus y}$
D. $x \oplus y$ and $x \oplus y$

gate2008-it digital-logic boolean-expressions normal

Answer

4.4.16 Boolean Expressions: GATE2012-6 top http://gateoverflow.in/38

The truth table

X	Y	(X,Y)
0	0	0
0	1	0
1	0	1
1	1	1

represents the Boolean function

A. X
B. $X + Y$
C. $X \oplus Y$
D. Y

gate2012 digital-logic easy boolean-expressions

Answer

4.4.17 Boolean Expressions: GATE2013-21 top http://gateoverflow.in/1532

Which one of the following expressions does **NOT** represent exclusive NOR of x and y?

A. $xy + x'y'$
B. $x \oplus y'$
C. $x' \oplus y$
D. $x' \oplus y'$

gate2013 digital-logic easy boolean-expressions

Answer

4.4.18 Boolean Expressions: GATE2014-3-55 top http://gateoverflow.in/2090

Let $\oplus$ denote the exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q:

$$F(P,Q) = ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$$

The equivalent expression for F is

A. $P + Q$
B. $\overline{P + Q}$
C. $P \oplus Q$
D. $\overline{P \oplus Q}$

gate2014-3 digital-logic normal boolean-expressions

Answer

4.4.19 Boolean Expressions: GATE2015-2_37 top http://gateoverflow.in/8162

The number of min-terms after minimizing the following Boolean expression is ________.

[D'+AB'+A'C+AC'D+A'C'D]'

gate2015-2 digital-logic boolean-expressions normal numerical-answers

Answer

4.4.20 Boolean Expressions: GATE2017-2-27 top http://gateoverflow.in/118494

If w, x, y, z are Boolean variables, then which one of the following is INCORRECT?

A. $wz + w(x+y) + x(x_y) = x + wy$
B. $\overline{w\bar{x}(y+\bar{z})} + \bar{w}x = \bar{w} + x + \bar{y}z$
C. $(w\bar{x}(y + x\bar{z}) + \bar{w}\bar{x})y = x\bar{y}$
D. $(w+y)(wxy + wyz) = wxy + wyz$

gate2017-2 digital-logic boolean-expressions normal

Answer

Answers: Boolean Expressions

4.4.1 Boolean Expressions: GATE 2016-1-06 top http://gateoverflow.in/39629

Selected Answer

These are properties of XOR function.. so answer is A) $x\bar{y}+\bar{x}y$

18 votes -- Abhilash Panicker (8.8k points)

4.4.2 Boolean Expressions: GATE1987-12a top http://gateoverflow.in/82556

Selected Answer

Option C) **B**

A⊕A= 0 and **0 ⊕ A = A**

A ⊕ B ⊕ A= (A⊕ A) ⊕ B = 0 ⊕ B =**B**

10 votes -- Prajwal Bhat (11.9k points)

4.4.3 Boolean Expressions: GATE1988-2iii top

http://gateoverflow.in/91679

C = $\bar{A}\bar{B}$ + AB

C = Complement of (A XOR B)

C = A XNOR B

Truth table is

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

When C = 1 , observing the truth table we can say A=B

3 votes -- Arnab Bhadra (5.3k points)

4.4.4 Boolean Expressions: GATE1989-5a top

http://gateoverflow.in/88230

Selected Answer

from A+B=1 and AB=0 we get either of A,b is 1 and another is 0

now AC=BC ,here C has to be 0 (because A,b has different values)

C=0

now A+c=1

so A=1 and Ab=0 so B=0

so we get

A=1 B=0 C=0

these are the values

8 votes -- Aboveallplayer (18.5k points)

4.4.5 Boolean Expressions: GATE1994-4 top

http://gateoverflow.in/2500

Selected Answer

a) i) A* A = AA+A'A' = A + A' = 1

ii) C*A= (A*B)*A = (AB + A'B')*A= (AB + A'B')A +(AB + A'B')'A'

=(AB + A'B')A+(A'B+AB')A' = AB +0 +A'B+0 = B.

b) AB + A'C= 1 , AC + B = 0

AC + B = 0 , means both B = 0 and AC = 0

AB+ A'C = 1

A'C = 1 [bcoz B = 0 so AB = 0]

So C = 1 and A= 0

so A = 0 , B = 0 and C = 1

11 votes -- Praveen Saini (53.6k points)

4.4.6 Boolean Expressions: GATE1995_2.5 top http://gateoverflow.in/2617

Selected Answer

Answer is A.

For verification, just put up the values and check for AND, OR operations and their outputs.

12 votes -- Gate Keeda (19.1k points)

4.4.7 Boolean Expressions: GATE1997-2.1 top http://gateoverflow.in/2227

Selected Answer

answer = **option B**

$z * x = (x * y) * x$

$= (\bar{x} + y) * x$

$= \overline{\bar{x} + y} + x$

$x.\bar{y} + x = x$

7 votes -- Arjun Suresh (294k points)

4.4.8 Boolean Expressions: GATE2002-2.3 top http://gateoverflow.in/833

Selected Answer

$f(f(x + y, y), z) = f((x + y)' + y), z)$

$= ((x + y)' + y)' + z$

$= (x + y).y' + z(\because (a + b)' = a'.b')$

$= xy' + z$

10 votes -- Arjun Suresh (294k points)

4.4.9 Boolean Expressions: GATE2004-17 top http://gateoverflow.in/1014

Selected Answer

answer = **option D**

x'y' + x'y = x'(y+y') = x'
x' + xy = x' + y

5 votes -- Arjun Suresh (294k points)

4.4.10 Boolean Expressions: GATE2004-IT-44 top http://gateoverflow.in/3687

Selected Answer

K-map

	A'B'	**A'B**	**AB**	**AB'**
C'	0	0	1	1
C	1	1	0	1

So, the equivalent expression will be A'C + AC' + AB'

(B) option

12 votes -- Arjun Suresh (294k points)

4.4.11 Boolean Expressions: GATE2005-IT-7 top http://gateoverflow.in/3752

Selected Answer

Correct answer is C

$(A \oplus B) \oplus C$

At $C = 0$,$(A \oplus B) \oplus C = (A \oplus B)$ ----(I) [as $0 \oplus x = 0.x' + 0.'x = x$]

At $C = 0$, $ABC + A'(B \oplus C) + B'(A \oplus C)$

$= 0 + A'(B \oplus 0) + B'(A \oplus 0) = A'B + AB' = A \oplus B$ -----(II)

At $C = 1$, $(A \oplus B) \oplus C = (A \odot B)$ --- (III) [as $1 \oplus x = 1.x' + 1'.x = x'$]

At $C = 1$, $ABC + A'(B \oplus C) + B'(A \oplus C)$

$= AB + A'(B \oplus 1) + B'(A \oplus 1) = AB + A'B' = (A \odot B)$ --(IV)

from eq (I), (II), (III) and (IV) it is clear
$(A \oplus B) \oplus C = ABC + A'(B \oplus C) + B'(A \oplus C)$

9 votes -- Praveen Saini (53.6k points)

4.4.12 Boolean Expressions: GATE2007-32 top http://gateoverflow.in/1230

Selected Answer

K-map

	w'x'	w'x	wx	wx'
y'z'	1	1		1
y'z		1	1	1
yz		1	1	
yz'				

So, minimized expression will be

$xz + w'y'z' + wx'y'$ which is Q. From the K-map, we can also get P and R. So, only S is NOT equivalent to f.

http://www.eecs.berkeley.edu/~newton/Classes/CS150sp98/lectures/week4_2/sld011.htm

6 votes -- Arjun Suresh (294k points)

Let me show u a very simple method

Let w =1 ,x =1 ,y=1 ,z=1 then the value of f is 1

consider each statement

x'y'z' + w' x y' +w y' z +x z = 0.0.0 + 0.1.0 + 1.0.1 + 1.1 =1

w' y' z' +w x' z' y' +x z = 0.0.0 +1.0.0 +1.1 =1

w' y' z' +w x' y' +x y z +x y' z =0.0.0 +1.0.0 +1.1.1 +1.0.1 =1 x' y' z' +w x' y' + w' y = 0.0.0 + 1.0.0 + 0.1 =0

So statement (d) is false because w=1 x=1 y=1 z=1 the value of f is 0 .

(d) does not contain the essential Minterms .

10 votes -- shekhar chauhan (42.9k points)

4.4.13 Boolean Expressions: GATE2007-33 top

http://gateoverflow.in/1231

Selected Answer

P:

Y * Z = Y * (X*Y)
= Y * (XY + X'Y')
= Y (XY + X'Y') + Y' (XY + X'Y')'
= XY + Y' ((X' + Y') (X+ Y))
= XY + Y' (X'Y + XY')
= XY + XY'
= X(Y + Y')
= X

So, P is valid.

Q:

X * Z = X * (X*Y)
= X * (XY + X'Y')
= X (XY + X'Y') + X' (XY + X'Y')'
= XY + X' ((X' + Y') (X+ Y))
= XY + X' (X'Y + XY')
= XY + X'Y
= Y(X + X')
= Y

So, Q is also valid.

R:

X * Y * Z = (X * Y) * (X * Y)

= (XY + X'Y') * (XY + X'Y')
= (XY + X'Y') (XY + X'Y') + (XY + X'Y')' (XY + X'Y')'
= (XY + X'Y') + (XY + X'Y')' (Since, AA = A)
= 1 (Since A + A' = 1)

So, R is also valid.

Hence, D choice.

13 votes -- Arjun Suresh (294k points)

4.4.14 Boolean Expressions: GATE2008-26 top

http://gateoverflow.in/424

Selected Answer

Ans is (A) $P\bar{Q}$

$(P+\bar{Q})(P\bar{Q}+PR)(\bar{P}\bar{R}+\bar{Q})$

$= (PP\bar{Q}+PPR+P\bar{Q}+P\bar{Q}R)(\bar{P}\bar{R}+\bar{Q})$

$= (P\bar{Q} + PR + P\bar{Q} + P\bar{Q}R)(\bar{P}\bar{R} + \bar{Q})$

$= P\bar{Q} + P\bar{Q}\bar{R} + P\bar{Q}R$

$= P\bar{Q} + P\bar{Q}(\bar{R} + R)$

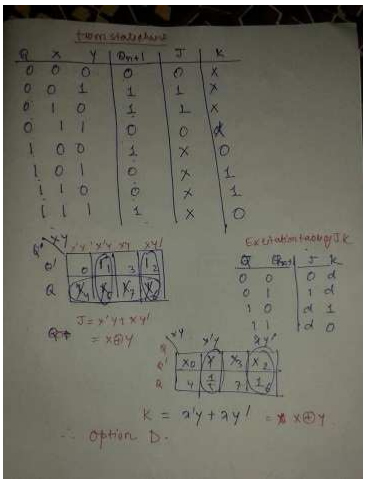
$= P\bar{Q} + P\bar{Q}$

$= P\bar{Q}$

13 votes -- Keith Kr (6.3k points)

4.4.15 Boolean Expressions: GATE2008-IT-37 top http://gateoverflow.in/3347

Selected Answer



D is correct

27 votes -- Riya Roy(Arayana) (7.1k points)

4.4.16 Boolean Expressions: GATE2012-6 top http://gateoverflow.in/38

Selected Answer

Whenever X is true (X,Y) is true and whenever X is false (X,Y) is false, so the answer is (A) X.

16 votes -- Omesh Pandita (2.7k points)

4.4.17 Boolean Expressions: GATE2013-21 top http://gateoverflow.in/1532

Selected Answer

A : means both are either true OR both are false. then it will be true = ExNOR

B & C : whenever any one of the literal is complemented then ExOR can be turned to ExNOR and complement sign on the literal can be removed. So these two also represents ExNOR operation of x and y.

answer = **option D** it is the ExOR operation b/w the two.

10 votes -- Amar Vashishth (28.7k points)

4.4.18 Boolean Expressions: GATE2014-3-55 top http://gateoverflow.in/2090

Selected Answer

XOR is associative and commutative. Also,
$A \oplus A = 0$ and
$A \oplus 1 = \overline{A}$ and
$A \oplus 0 = A$. So
$((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$
$\implies (1 \oplus P) \oplus ((P \oplus Q) \oplus (P \oplus Q)) \oplus (Q \oplus 0)$
$\implies (1 \oplus 0) \oplus (P \oplus Q)$
$\implies 1 \oplus (P \oplus Q)$
$\implies \overline{(P \oplus Q)}$

11 votes -- Arjun Suresh (294k points)

4.4.19 Boolean Expressions: GATE2015-2_37 top http://gateoverflow.in/8162

Selected Answer

F = [D'+AB'+A'C+AC'D+A'C'D]'

F' = D'+AB'+A'C+AC'D+A'C'D

Now we have **F'** , so fill **0**'s (maxterms) in K-map for each term

As for **D'**

	C'D'	**C'D**	**CD**	**CD'**
A'B'	0			0
A'B	0			0
AB	0			0
AB'	0			0

Similarly for AB', A'C, AC'D and A'C'D. We will get

	C'D'	**C'D**	**CD**	**CD'**
A'B'	0	0	0	0
A'B	0	0	0	0
AB	0	0		0
AB'	0	0	0	0

We get one place for minterm and that is **ABCD**

20 votes -- Praveen Saini (53.6k points)

Let's First Simplify it

[D' + AB' + A'C + AC'D + A'C'D]'

[D' + AB' + A'C + C'D (A + A')]'   // A + A' =1

[AB' +A'C + (D' + C') (D' + D)]'   // Apply Distributive Rule Among D' and C'D

[AB' + A'C + D' + C']'

[AB' + (A' + C') (C + C') + D'] '   //Apply distributive Law B/w A'C and C'

[AB' + A' +C' +D']'

[(A+ A') (A' + B') + C' + D']'   //Apply Distributive law b/w AB' and A'

Finally we got

[A' +B' +C' + D']'

Apply ***Demorgan's*** Law

ABCD

👍 11 votes -- shekhar chauhan (42.9k points)

4.4.20 Boolean Expressions: GATE2017-2-27 top http://gateoverflow.in/118494

Selected Answer

Option C-(wx'(y+xz')+w'.x')y= (wx'y+wx'xz'+w'x')y=
xx'=0 ..so
Wx'y+w'x'y=x'y(w+w')=x'y

👍 4 votes -- Joker (1.5k points)

4.5 Boolean Operations(3) top

4.5.1 Boolean Operations: GATE1992_02,i top http://gateoverflow.in/555

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

The operation which is commutative but not associative is:

A. AND
B. OR
C. EX-OR
D. NAND

gate1992 easy digital-logic boolean-operations

Answer

4.5.2 Boolean Operations: GATE1998-2.8 top http://gateoverflow.in/1680

Which of the following operations is commutative but not associative?

A. AND
B. OR
C. NAND
D. EXOR

gate1998 digital-logic easy boolean-operations

Answer

4.5.3 Boolean Operations: GATE1999-1.7 top http://gateoverflow.in/1460

Which of the following expressions is not equivalent to $\bar{x}$?

A. $x \text{ NAND } x$
B. $x \text{ NOR } x$
C. $x \text{ NAND } 1$
D. $x \text{ NOR } 1$

gate1999 digital-logic easy boolean-operations

Answer

Answers: Boolean Operations

4.5.1 Boolean Operations: GATE1992_02,i top http://gateoverflow.in/555

Selected Answer

answer - D

10 votes -- ankitrokdeonsns (9.1k points)

4.5.2 Boolean Operations: GATE1998-2.8 top http://gateoverflow.in/1680

Selected Answer

we all know AND ,OR are both associative and commutative.we dont know about EXOR and NAND

we can consume some time and prove it by truth table..and come up with the results that EXOR is also associative and commutative so the only left out is NAND its commutative but not associative

7 votes -- Bhagirathi Nayak (13.3k points)

4.5.3 Boolean Operations: GATE1999-1.7 top http://gateoverflow.in/1460

Selected Answer

answer - D

x OR 1 = 1 and so x NOR 1 = 0.

7 votes -- ankitrokdeonsns (9.1k points)

4.6 Booth Recoding(1) top

4.6.1 Booth Recoding: GATE2006-IT-38 top http://gateoverflow.in/3577

When multiplicand Y is multiplied by multiplier $X = x_{n-1}x_{n-2}\dots x_0$ using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

Row	x_{i+1}	x_i	x_{i-1}	Partial Product
1	0	0	0	0
2	0	0	1	Y
3	0	1	0	Y
4	0	1	1	2Y
5	1	0	0	?
6	1	0	1	-Y
7	1	1	0	-Y
8	1	1	1	?

The partial products for rows 5 and 8 are

A. 2Y and Y
B. -2Y and 2Y
C. -2Y and 0
D. 0 and Y

gate2006-it digital-logic booths-algorithm booth-recoding difficult

Answer

Answers: Booth Recoding

4.6.1 Booth Recoding: GATE2006-IT-38 top http://gateoverflow.in/3577

Selected Answer

Partial product is calculated by using bit pair recording in booths algorithm, which is improvement technique used in booths algorithm. Here we consider 3 bits at a time for getting the partial product. This eliminates the worst case behaviour of normal Booth's algorithm. Partial Product calculation can be seen in the below link:

http://www.geoffknagge.com/fyp/booth.shtml
"100" corresponds to -2M and "111" corresponds to 0
-2 X(i+1) + x (i) + X(i-1)

ANS : C

4 votes -- pramod (3.3k points)

4.7 Booths Algorithm(4) top

4.7.1 Booths Algorithm: GATE1996_1.23 top

http://gateoverflow.in/2727

Booth’s algorithm for integer multiplication gives worst performance when the multiplier pattern is

A. 101010 1010
B. 100000 0001
C. 111111 1111
D. 011111 1110

gate1996 digital-logic booths-algorithm normal

Answer

4.7.2 Booths Algorithm: GATE1999_1.20 top

http://gateoverflow.in/1473

Booth's coding in 8 bits for the decimal number -57 is

A. 0-100+1000
B. 0-100+100-1
C. 0-1+100-10+1
D. 00-10+100-1

gate1999 digital-logic number-representation booths-algorithm normal

Answer

4.7.3 Booths Algorithm: GATE2005-IT-8 top

http://gateoverflow.in/3753

Using Booth's Algorithm for multiplication, the multiplier -57 will be recoded as

A. 0 -1 0 0 1 0 0 -1
B. 1 1 0 0 0 1 1 1
C. 0 -1 0 0 1 0 0 0
D. 0 1 0 0 -1 0 0 1

gate2005-it digital-logic booths-algorithm normal

Answer

4.7.4 Booths Algorithm: GATE2008-IT-42 top

http://gateoverflow.in/3352

The two numbers given below are multiplied using the Booth's algorithm.

Multiplicand : 0101 1010 1110 1110
Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for the multiplication of the above two numbers?

A. 6
B. 8
C. 10
D. 12

gate2008-it digital-logic booths-algorithm normal

Answer

Answers: Booths Algorithm

4.7.1 Booths Algorithm: GATE1996_1.23 top

http://gateoverflow.in/2727

Selected Answer

Answer: A

The worst case of an implementation using Booth's algorithm is when pairs of 01s or 10s occur very frequently in the multiplier.

9 votes -- Rajarshi Sarkar (35k points)

4.7.2 Booths Algorithm: GATE1999_1.20 top

http://gateoverflow.in/1473

Selected Answer

There are 2 ways for answering This questions.

1. Way 1 -> Convert 57 to Binary & Get 2's complement. It is "11000111" & Attach one extra 0 to right of it

110001110 To calculate booth code substract right digit from left digit in every consecutive 2 digt.

So 11-> 0 , 10 -> +1, .. finally 10 -> +1

So answer is B)

There is another way to solve this question.

0-100+100-1 -> If you check binary weigted sum of this code you will get -57. This is trick to quick check. Booth code is always equivalent to it's original value if checked as weighted code. IF you check it before doing above procedure & if only one of option maps, you don't need to do above procedure, just mark the answer.

Here -1 * 64 + +1 * 8 + -1 * 1 = -57 .

11 votes -- Akash (43.8k points)

4.7.3 Booths Algorithm: GATE2005-IT-8 top

http://gateoverflow.in/3753

Selected Answer

2's complement of -57 is (11000111)

Booth multiplier :

1 1 0 0 0 1 1 1

1 0 0 0 1 1 1 0 (put 0 in lst and shift multiplier left by 1 bit)

----

0 -1 0 0 1 0 0 -1

Use this encoded scheme:00-> 0 , 01-> +1, 10-> -1, 11->0

5 votes -- Prashant Singh (49.2k points)

4.7.4 Booths Algorithm: GATE2008-IT-42 top http://gateoverflow.in/3352

Selected Answer

Answer : 8

If you want to find out How many additions/Subtractions are required for the multiplication using Booth's algorithm. then Rules are like this

Take multiplicand and multiplier like they are given in the question :

Multiplicand :	0101	1010	1110	1110
Multiplier:	0111	0111	1011	1101

Now find out the 01 and 10 pairs combinedly means see both Multiplicand and Multiplier simultaneously first pair is 00 then 11 ,**01** ,11 , **10** **01** 11 **01** 11 **10** 11 **01** 11 11 **10** **01**

why i asked you to do this because this is the rule a/c to Booth's algorithm. to find out no of additions/Subtractions it also says don't do anything if you got 11 or 00 .

18 votes -- shekhar chauhan (42.9k points)

4.8 Canonical Normal Form(7) top

4.8.1 Canonical Normal Form: GATE1990-5a top http://gateoverflow.in/85396

Find the minimum product of sums of the following expression

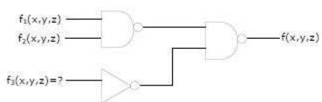
$f = ABC + \bar{A}\bar{B}\bar{C}$

gate1990 descriptive digital-logic canonical-normal-form

Answer

4.8.2 Canonical Normal Form: GATE2002-2.1 top http://gateoverflow.in/831

Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f



Given that

$f_1(x, y, z) = \Sigma(0, 1, 3, 5)$

$f_2(x, y, z) = \Sigma(6, 7)$, and

$f(x, y, z) = \Sigma(1, 4, 5)$.

f_3 is

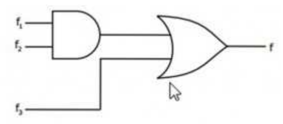
A. $\Sigma(1, 4, 5)$
B. $\Sigma(6, 7)$
C. $\Sigma(0, 1, 3, 5)$
D. None of the above

gate2002 digital-logic normal canonical-normal-form circuit-output

Answer

4.8.3 Canonical Normal Form: GATE2008-8 top http://gateoverflow.in/406

Given f_1, f_3 and f in canonical sum of products form (in decimal) for the circuit



$f_1 = \Sigma m(4,5,6,7,8)$

$f_3 = \Sigma m(1,6,15)$

$f = \Sigma m(1,6,8,15)$

then f_2 is

A. $\Sigma m(4,6)$

B. $\Sigma m(4,8)$

C. $\Sigma m(6,8)$

D. $\Sigma m(4,6,8)$

gate2008 digital-logic canonical-normal-form easy

Answer

4.8.4 Canonical Normal Form: GATE2010-6 top http://gateoverflow.in/2177

The minterm expansion of $f(P,Q,R) = PQ + Q\bar{R} + P\bar{R}$ is

A. $m_2 + m_4 + m_6 + m_7$
B. $m_0 + m_1 + m_3 + m_5$
C. $m_0 + m_1 + m_6 + m_7$
D. $m_2 + m_3 + m_4 + m_5$

gate2010 digital-logic canonical-normal-form normal

Answer

4.8.5 Canonical Normal Form: GATE2015-3_43 top http://gateoverflow.in/8503

The total number of prime implicants of the function $f(w,x,y,z) = \sum(0,2,4,5,6,10)$ is __________.

gate2015-3 digital-logic canonical-normal-form normal numerical-answers

Answer

4.8.6 Canonical Normal Form: GATE2015-3_44 top http://gateoverflow.in/8504

Given the function $F = P' + QR$, where F is a function in three Boolean variables P,Q and R and $P' = !P$, consider the following statements.

$(S1) F = \sum(4,5,6)$

$(S2) F = \sum(0,1,2,3,7)$

$(S3) F = \Pi(4,5,6)$

$(S4) F = \Pi(0,1,2,3,7)$

Which of the following is true?

A. (S1)-False, (S2)-True, (S3)-True, (S4)-False
B. (S1)-True, (S2)-False, (S3)-False, (S4)-True
C. (S1)-False, (S2)-False, (S3)-True, (S4)-True

D. (S1)-True, (S2)-True, (S3)-False, (S4)-False

gate2015-3 digital-logic canonical-normal-form normal

Answer

4.8.7 Canonical Normal Form: TIFR2015-B-9 top

http://gateoverflow.in/30030

A Boolean expression is an expression made out of propositional letters (such as p, q, r) and operators $\wedge$, $\vee$ and $\neg$; e.g. $p \wedge \neg(q \vee \neg r)$. An expression is said to be in sum of product form (also called disjunctive normal form) if all $\neg$ occur just before letters and no $\vee$ occurs in scope of $\wedge$; e.g. $(p \wedge \neg q) \vee (\neg p \wedge q)$. The expression is said to be in product of sum form (also called conjunctive normal form) if all negations occur just before letters and no $\wedge$ occurs in the scope of $\vee$; e.g. $(p \vee \neg q) \wedge (\neg p \vee q)$. Which of the following is not correct?

A. Every Boolean expression is equivalent to an expression is sum of product form.
B. Every Boolean expression is equivalent to an expression in product of sum form.
C. Every Boolean expression is equivalent to an expression without $\vee$ operator.
D. Every Boolean expression is equivalent to an expression without $\wedge$ operator.
E. Every Boolean expression is equivalent to an expression without $\neg$ operator.

tifr2015 canonical-normal-form

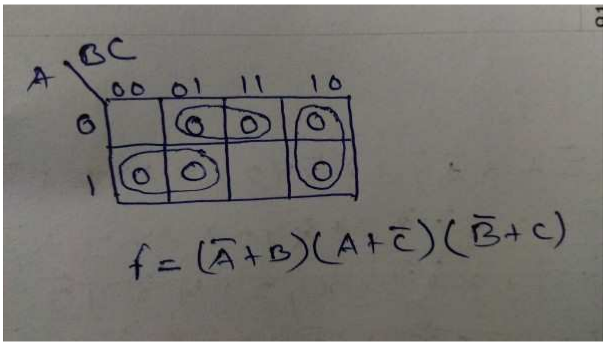
Answer

Answers: Canonical Normal Form

4.8.1 Canonical Normal Form: GATE1990-5a top

http://gateoverflow.in/85396

Minimal POS



5 votes -- Lokesh . (9.8k points)

4.8.2 Canonical Normal Form: GATE2002-2.1 top

http://gateoverflow.in/831

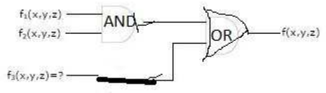
Selected Answer

$f = ((f_1 f_2)' f_3')' = f_1 f_2 + f_3$

In minimum sum of products form, AND of two expressions will contain the common terms. Since f_1 and f_2 don't have any common term, $f_1 f_2$ is 0 and hence $f = f3 = \Sigma(1, 4, 5)$.

22 votes -- Arjun Suresh (294k points)

Here we have NAND - NAND Circuit, we can convert it to following AND - OR circuit. (As NAND is bubbled OR). Now it is easy to solve this question. F1 AND F2 = 0. SO whatever f3 is directly passed to output. So answer is A.



10 votes -- Akash (43.8k points)

4.8.3 Canonical Normal Form: GATE2008-8 top http://gateoverflow.in/406

Selected Answer

answer - C

with AND gates we will choose intersection of min-terms

with OR gates we will take union of min-terms

15 votes -- ankitrokdeonsns (9.1k points)

4.8.4 Canonical Normal Form: GATE2010-6 top http://gateoverflow.in/2177

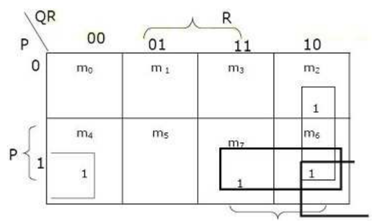
Selected Answer

PQ + QR' + PR' = PQR + PQR' + PQR' + P'QR' + PQR' + PQ'R'

= PQR + PQR' + P'QR' + PQ'R' (111 + 110 + 010 + 100)

$=m_7 + m_6 + m_2 + m_4$

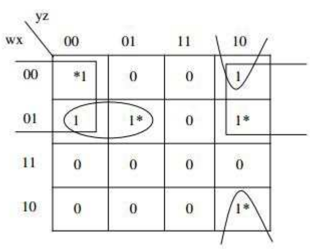
Option A.
Alternatively ,
Using K-map



11 votes -- Arjun Suresh (294k points)

4.8.5 Canonical Normal Form: GATE2015-3_43 top http://gateoverflow.in/8503

Selected Answer



as u can see that there is 1 4-set and 2 2-set that are covering the star marked 1's(i.e. the ones that are not covered by any other combinations).

So, the answer is 3.

23 votes -- Tamojit Chatterjee (2.2k points)

4.8.6 Canonical Normal Form: GATE2015-3_44 top

http://gateoverflow.in/8504

Selected Answer

F=P'+QR, draw the Kmap for this

we can find the minterm $\sum(0,1,2,3,7)$
and maxterm $\Pi(4,5,6)$
so option A is correct ...(S1)-False, (S2)-True, (S3)-True, (S4)-False

13 votes -- Anoop Sonkar (4.9k points)

4.8.7 Canonical Normal Form: TIFR2015-B-9 top

http://gateoverflow.in/30030

Selected Answer

Basically they are saying all the same thing as what we have see. for ex just simplify this. use and operator (.) for ^ . so sop will become (p.q') + (p'.q)

so no meaning have been changed and we can move further with all the boolean logic we have read.

we know every expression can be expressed in pos or sop form so 1 and 2 are true.

we know that AND and NOT are functionally complete. so any expression can be expressed using these two only. so all the expression can be expresed in a form which does not contain OR but contain and and not,
with the same logic point 4 will be true because we know not and OR are also functionally complete.

But without NOT we can't get a functionally complete gate. so E is wrong.

6 votes -- No Need (14.1k points)

4.9 Carry Generator(2) top

4.9.1 Carry Generator: GATE2006-36 top

http://gateoverflow.in/1294

Given two three bit numbers $a_2a_1a_0$ and $b_2b_1b_0$ and c the carry in, the function that represents the *carry* generate function when these two numbers are added is:

A. $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$
B. $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$
C. $a_2 + b_2 + (a_2 \oplus b_2)(a_1 + b_1 + (a_1 \oplus b_1) + (a_0 + b_0))$
D. $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2a_1}a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2b_1}b_0$

gate2006 digital-logic normal carry-generator

Answer

4.9.2 Carry Generator: GATE2007-35 top

http://gateoverflow.in/1233

In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$$P_i = A_i \oplus B_i \text{ and } G_i = A_iB_i$$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look ahead carry adder are given by:

$$S_i = P_i \oplus C_i \text{ and } C_{i+1} = G_i + P_i C_i, \text{ where } C_0 \text{ is the input carry.}$$

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively:

A. 6, 3
B. 10, 4
C. 6, 4
D. 10, 5

gate2007 digital-logic normal carry-generator adder

Answer

Answers: Carry Generator

4.9.1 Carry Generator: GATE2006-36 top

http://gateoverflow.in/1294

Selected Answer

$c_1 = a_0 b_0$

$c_2 = a_1 b_1 + a_1 c_1 + b_1 c_1$

$c_3 = a_2 b_2 + a_2 c_2 + b_2 c_2 = a_2 b_2 + a_2 a_1 b_1 + a_2 a_1 c_1 + a_2 b_1 c_1 + b_2 a_1 b_1 + b_2 a_1 c_1 + b_2 b_1 c_1 = a_2 b_2 + a_2 a_1 b_1 + a_2 a_1 a_0 b_0 + a$

Option A.

Considering the carry in function c, $c_1 = a_0 b_0 + a_0 c + b_0 c$, but c is missing in all options and hence ignored.

20 votes -- Arjun Suresh (294k points)

4.9.2 Carry Generator: GATE2007-35 top

http://gateoverflow.in/1233

Selected Answer

C1 = G0 + C0.P0

C2 = G1 + G0.P1 + C0.P0.P1

C3 = G2 + G1.P2 + G0.P1.P2 + C0.P0.P1.P2

C4 = G3 + G2.P3 + G1.P2.P3 + G0.P1.P2.P3 + C0.P0.P1.P2.P3 // read this as carry is generated in 3rd stage OR carry is generated in 2nd stage AND propagated to 3rd stage OR carry is generated in 1st stage AND carry is propagated through 2nd AND 3rd stage OR carry is generated in 0th stage AND propagated through 1st,2nd AND 3rd stage OR initial carry is propagated through 0th, 1st ,2nd AND 3rd stage.

4 OR gates are required for C1, C2, C3, C4

1 AND gate for C1

2 AND gate for C2

3 AND gate for C3

4 AND gate for C4

AND = 10

OR = 4

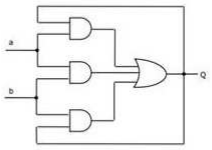
16 votes -- Vikrant Singh (13.4k points)

4.10 Circuit Output(34) top

4.10.1 Circuit Output: GATE1991-5,a top http://gateoverflow.in/531

Analyse the circuit in Fig below and complete the following table

a	b	Q_n
0	0	
0	1	
1	0	
1	1	

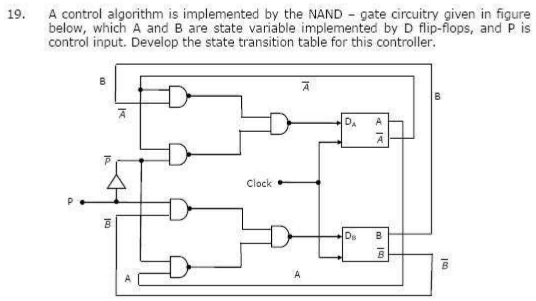


gate1991 digital-logic normal circuit-output

Answer

4.10.2 Circuit Output: GATE1993_19 top http://gateoverflow.in/2316

A control algorithm is implemented by the NAND – gate circuitry given in figure below, where A and B are state variable implemented by D flip-flops, and P is control input. Develop the state transition table for this controller.

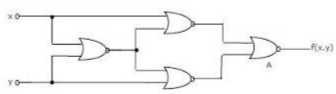


gate1993 digital-logic circuit-output normal

Answer

4.10.3 Circuit Output: GATE1993_6.1 top http://gateoverflow.in/2288

Identify the logic function performed by the circuit shown in figure.



A. exclusive OR
B. exclusive NOR
C. NAND
D. NOR
E. None of the above

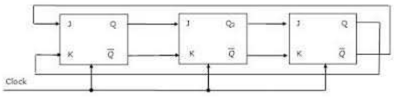
gate1993 digital-logic circuit-output normal

Answer

4.10.4 Circuit Output: GATE1993_6.3 top http://gateoverflow.in/17237

Multiple choices can be correct. Mark all of them.

For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:



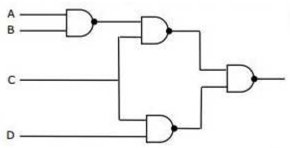
A. Shift Register
B. Mod- 3 Counter
C. Mod- 6 Counter
D. Mod- 2 Counter
E. None of the above

gate1993 digital-logic circuit-output normal

Answer

4.10.5 Circuit Output: GATE1994_1.8 top http://gateoverflow.in/2445

The logic expression for the output of the circuit shown in figure below is:



A. $\overline{AC} + \overline{BC} + CD$

B. $A\overline{C} + B\overline{C} + CD$

C. $ABC + \overline{C}\,\overline{D}$

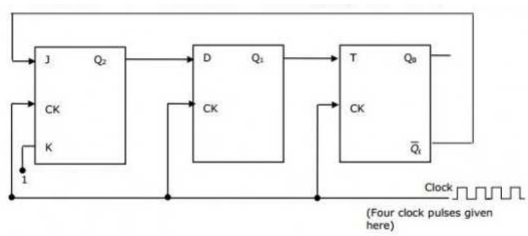
D. $\overline{A}\,\overline{B} + \overline{B}\,\overline{C} + CD$

gate1994 digital-logic circuit-output normal

Answer

4.10.6 Circuit Output: GATE1994_11 top http://gateoverflow.in/2507

Find the contents of the flip-flop Q_2, Q_1 and Q_0 in the circuit of figure, after giving four clock pulses to the clock terminal. Assume $Q_2Q_1Q_0 = 000$ initially.

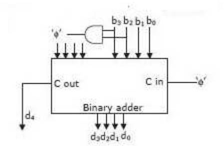


gate1994 digital-logic circuit-output normal

Answer

4.10.7 Circuit Output: GATE1996_2.21 top http://gateoverflow.in/2750

Consider the circuit in Fig.2.21 which has a four bit binary number $b_3b_2b_1b_0$ as input and a five bit binary number, $d_4d_3d_2d_1d_0$ as output.



A. Binary to Hex conversion

B. Binary to BCD conversion

C. Binary to grey code conversion

D. Binary to radix-12 conversion

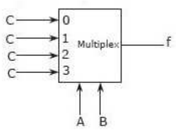
gate1996 digital-logic circuit-output normal

Answer

4.10.8 Circuit Output: GATE1996_2.22 top

http://gateoverflow.in/2751

Consider the circuit in figure. f implements



A. $\overline{A}\overline{B}C + \overline{A}B\overline{C} + ABC$

B. $A + B + C$

C. $A \oplus B \oplus C$

D. $AB + BC + CA$

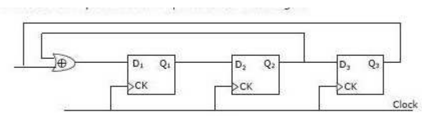
gate1996 digital-logic circuit-output easy

Answer

4.10.9 Circuit Output: GATE1996_24 top

http://gateoverflow.in/2776

Consider the synchronous sequential circuit in the below figure



a. Draw a state diagram, which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

Q1	**Q2**	**Q3**	**State**
0	0	0	S_0
0	0	1	S_1
-	-	-	-
-	-	-	-
-	-	-	-
1	1	1	S_7

b. Given that the initial state of the circuit is S_4, identify the set of states, which are not reachable.

gate1996 digital-logic circuit-output normal

Answer

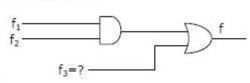
4.10.10 Circuit Output: GATE1997_5.5 top http://gateoverflow.in/2256

Consider a logic circuit shown in figure below. The functions $f_1, f_2 \text{ and } f$ (in canonical sum of products form in decimal notation) are :

$f_1(w, x, y, z) = \sum 8, 9, 10$

$f_2(w, x, y, z) = \sum 7, 8, 12, 13, 14, 15$

$f(w, x, y, z) = \sum 8, 9$



The function
f_3 is

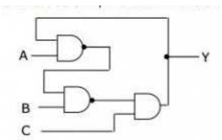
A. $\sum 9, 10$
B. $\sum 9$
C. $\sum 1, 8, 9$
D. $\sum 8, 10, 15$

gate1997 digital-logic circuit-output normal

Answer

4.10.11 Circuit Output: GATE1999_2.8 top http://gateoverflow.in/1486

Consider the circuit shown below. In a certain steady state, the line Y is at $'1'$. What are the possible values of A, B and C in this state?



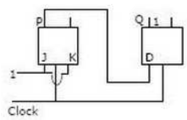
A. $A = 0, B = 0, C = 1$
B. $A = 0, B = 1, C = 1$
C. $A = 1, B = 0, C = 1$
D. $A = 1, B = 1, C = 1$

gate1999 digital-logic circuit-output normal

Answer

4.10.12 Circuit Output: GATE2000-2.12 top http://gateoverflow.in/659

The following arrangement of master-slave flip flops



has the initial state of P, Q as 0, 1 (respectively). After a clock cycle the output state P, Q is (respectively),

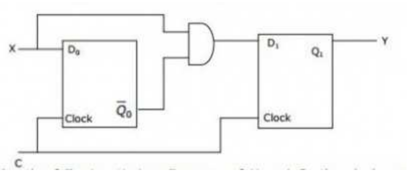
A. 1, 0
B. 1, 1
C. 0, 0
D. 0, 1

gate2000 digital-logic circuit-output normal

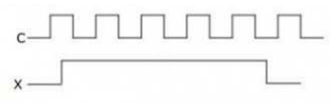
Answer

4.10.13 Circuit Output: GATE2001-2.8 top http://gateoverflow.in/726

Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of X and C. The clock period of $C \geq 40$ nanosecond. Which one is the correct plot of Y?



A. 

B. 

C. 

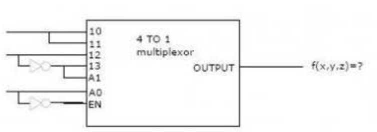
D. 

gate2001 digital-logic circuit-output normal

Answer

4.10.14 Circuit Output: GATE2002-2.2 top http://gateoverflow.in/832

Consider the following multiplexer where 10, 11, 12, 13 are four data input lines selected by two address line combinations A1A0=00,01,10,11 respectively and f is the output of the multiplexor. EN is the Enable input.



The function f(x,y,z) implemented by the above circuit is

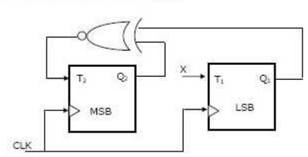
A. xyz'
B. xy + z
C. x + y
D. None of the above

gate2002 digital-logic circuit-output normal

Answer

4.10.15 Circuit Output: GATE2004-61 top http://gateoverflow.in/1056

Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below.



To complete the circuit, the input X should be

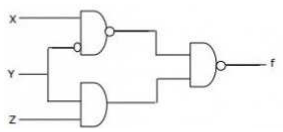
A. Q_2^c
B. $Q_2 + Q_1$
C. $(Q_1 + Q_2)^c$
D. $Q_1 \oplus Q_2$

gate2004 digital-logic circuit-output normal

Answer

4.10.16 Circuit Output: GATE2005-15 top http://gateoverflow.in/1351

Consider the following circuit.



Which one of the following is TRUE?

A. f is independent of X

B. f is independent of Y

C. f is independent of Z

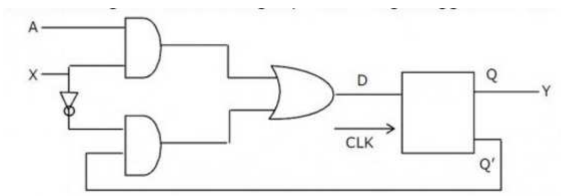
D. None of X, Y, Z is redundant

gate2005 digital-logic circuit-output normal

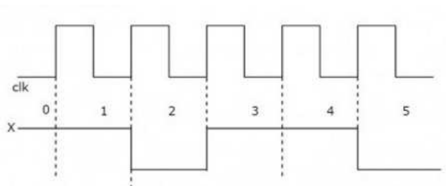
Answer

4.10.17 Circuit Output: GATE2005-62 top http://gateoverflow.in/264

Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram. Let A_i represents the logic level on the line a in the i-th clock period.



Let A' represent the compliment of A. The correct output sequence on Y over the clock periods 1 through 5 is:

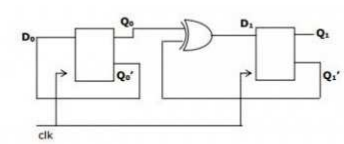
A. $A_0 A_1 A_1' A_3 A_4$
B. $A_0 A_1 A_2' A_3 A_4$
C. $A_1 A_2 A_2' A_3 A_4$
D. $A_1 A_2' A_3 A_4 A_5'$

gate2005 digital-logic circuit-output normal

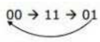
Answer

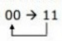
4.10.18 Circuit Output: GATE2005-64 top http://gateoverflow.in/1387

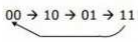
Consider the following circuit:

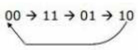


The flip-flops are positive edge triggered D FFs. Each state is designated as a two-bit string $Q_0 Q_1$. Let the initial state be 00. The state transition sequence is

A. 

B. 

C. 

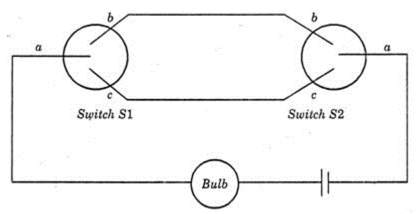
D. 

gate2005 digital-logic circuit-output

Answer

4.10.19 Circuit Output: GATE2005-IT-10 top http://gateoverflow.in/3755

A two-way switch has three terminals a, b and c. In ON position (logic value 1), *a* is connected to b, and in OFF position, *a* is connected to c. Two of these two-way switches S1 and S2 are connected to a bulb as shown below.



Which of the following expressions, if true, will always result in the lighting of the bulb ?

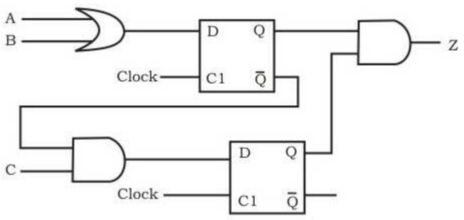
A. $S1.\overline{S2}$
B. $\overline{S1 + S2}$
C. $\overline{S1 \oplus S2}$
D. $S1 \oplus S2$

gate2005-it digital-logic circuit-output normal

Answer

4.10.20 Circuit Output: GATE2005-IT-43 top http://gateoverflow.in/3804

Which of the following input sequences will always generate a 1 at the output z at the end of the third cycle?



A.

A	B	C
0	0	0
1	0	1
1	1	1

B.

A	B	C
1	0	1
1	1	0
1	1	1

C.

A	B	C
0	1	1
1	0	1
1	1	1

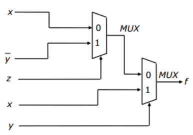
D.

A	B	C
0	0	1
1	1	0
1	1	1

gate2005-it digital-logic circuit-output normal

Answer

4.10.21 Circuit Output: GATE2006-35 top http://gateoverflow.in/1292



Consider the circuit above. Which one of the following options correctly represents $f(x, y, z)$

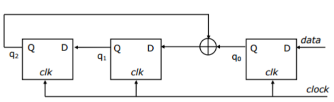
A. $x\bar{z} + xy + \bar{y}z$
B. $x\bar{z} + xy + \overline{yz}$
C. $xz + xy + \overline{yz}$
D. $xz + x\bar{y} + \bar{y}z$

gate2006 digital-logic circuit-output normal

Answer

4.10.22 Circuit Output: GATE2006-37 top http://gateoverflow.in/1295

Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of $q_2q_1q_0$ are:

A. 000
B. 001
C. 010

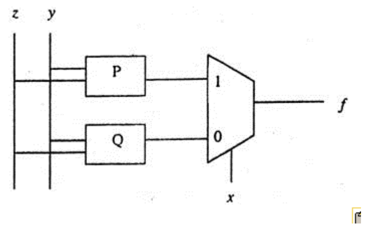
D. 101

gate2006 digital-logic circuit-output easy

Answer

4.10.23 Circuit Output: GATE2006-IT-36 top http://gateoverflow.in/3575

The majority function is a Boolean function $f(x, y, z)$ that takes the value 1 whenever a majority of the variables x, y, z are 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled P and Q are, respectively,



A. XOR, AND
B. XOR, XOR
C. OR, OR
D. OR, AND

gate2006-it digital-logic circuit-output normal

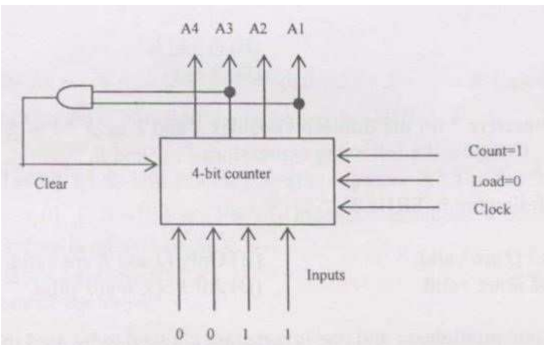
Answer

4.10.24 Circuit Output: GATE2007-36 top http://gateoverflow.in/1234

The control signal functions of a 4-bit binary counter are given below (where X is "don't care"):

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

A. 0, 3, 4
B. 0, 3, 4, 5
C. 0, 1, 2, 3, 4
D. 0, 1, 2, 3, 4, 5

gate2007 digital-logic circuit-output normal

Answer

4.10.25 Circuit Output: GATE2007-IT-38 top http://gateoverflow.in/3471

The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates. (a.b).c + (a'.c).d + (b.c).d + a. d

What is the function finally realized ?

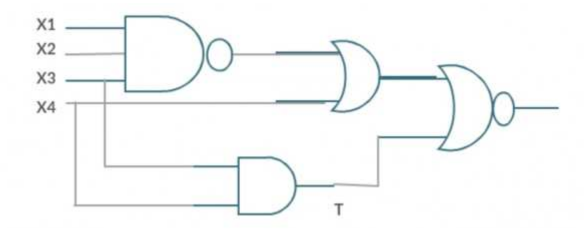
A. 1
B. a' + b' + c' + d'
C. a' + b + c' + d'
D. a' + b' + c + d'

gate2007-it digital-logic circuit-output normal

Answer

4.10.26 Circuit Output: GATE2007-IT-45 top http://gateoverflow.in/3480

The line T in the following figure is permanently connected to the ground.



Which of the following inputs (X1 X2 X3 X4) will detect the fault ?

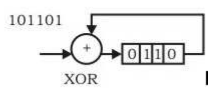
A. 0000
B. 0111
C. 1111
D. None of these

gate2007-it digital-logic circuit-output normal

Answer

4.10.27 Circuit Output: GATE2007-IT_40 top http://gateoverflow.in/3473

What is the final value stored in the linear feedback shift register if the input is 101101?



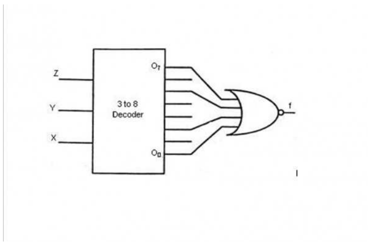
A. 0110
B. 1011
C. 1101
D. 1111

gate2007-it digital-logic circuit-output normal

Answer

4.10.28 Circuit Output: GATE2008-IT-9 top http://gateoverflow.in/3269

What Boolean function does the circuit below realize?



A. $xz + \bar{x}\bar{z}$
B. $x\bar{z} + \bar{x}z$
C. $\bar{x}\bar{y} + yz$
D. $xy + \bar{y}\bar{z}$

gate2008-it digital-logic circuit-output normal

Answer

4.10.29 Circuit Output: GATE2010-31 top

http://gateoverflow.in/2205

What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below?

A. $\overline{Q+R}$
B. $\overline{P+Q}$
C. $\overline{P+R}$
D. $\overline{P+Q+R}$

gate2010 digital-logic circuit-output normal

Answer

4.10.30 Circuit Output: GATE2010-32 top

http://gateoverflow.in/2206

In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00. What are the next four values of Q_1Q_0?

A. 11,10,01,00
B. 10,11,01,00
C. 10,00,01,11
D. 11,10,00,01

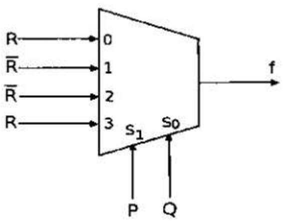
gate2010 digital-logic circuit-output normal

Answer

4.10.31 Circuit Output: GATE2010-9 top

http://gateoverflow.in/2182

The Boolean expression of the output f of the multiplexer shown below is



A. $\overline{P \oplus Q \oplus R}$
B. $P \oplus Q \oplus R$
C. $P + Q + R$
D. $\overline{P + Q + R}$

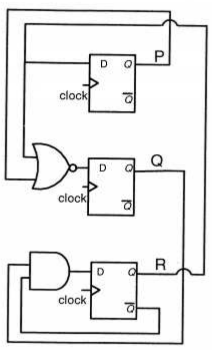
gate2010 digital-logic circuit-output easy

Answer

4.10.32 Circuit Output: GATE2011-50 top

http://gateoverflow.in/2157

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

A. 000
B. 001
C. 010
D. 011

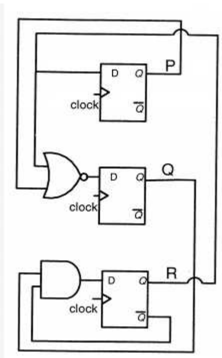
gate2011 digital-logic circuit-output normal

Answer

4.10.33 Circuit Output: GATE2011-51 top

http://gateoverflow.in/43318

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

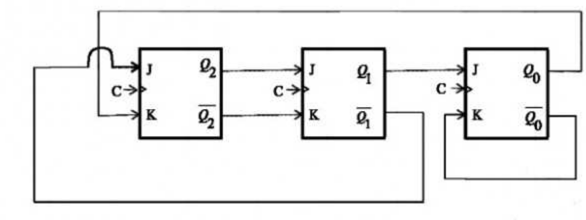
A. 3
B. 4
C. 5
D. 6

gate2011 digital-logic circuit-output normal numerical-answers

Answer

4.10.34 Circuit Output: GATE2014-3-45 top

http://gateoverflow.in/2079



The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is

A. 001, 010, 011
B. 111, 110, 101
C. 100, 110, 111
D. 100, 011, 001

gate2014-3 digital-logic circuit-output normal

Answer

Answers: Circuit Output

4.10.1 Circuit Output: GATE1991-5,a top

http://gateoverflow.in/531

Selected Answer

(a) The output of the circuit given as :-

$Q_n = aQ_{n-1} + ab + bQ_{n-1}$

Hence,

$Q_n = Q_{n-1}(a+b) + ab$

00 => $Q_{n-1}(0+0) + 0.0 = Q_{n-1}(0) + 0 = 0+0 = 0$

01 => $Q_{n-1}(0+1) + 0.1 = Q_{n-1}(1) + 0 = Q_{n-1}+0 = Q_{n-1}$

10 => $Q_{n-1}(1+0) + 1.0 = Q_{n-1}(1) + 0 = Q_{n-1}+0 = Q_{n-1}$

11 => $Q_{n-1}(1+1) + 1.1 = Q_{n-1}(1) + 1 = Q_{n-1}+1 = 1$

a	b	Qn
0	0	0
0	1	Q_{n-1}
1	0	Q_{n-1}
1	1	1

(c)

All the flip flops are operated by same clock , together all takes one propagation delay .

All the AND gates consumes one propagation delay individually.

Total propagation delay = $T_{CLK} >= T_{\text{flip-flop}} + T_{\text{AND gates}}$

$= 10ns+(10+10+10)ns = 40ns$

Maximum clock frequency $=1/T_{CLK} = 1/40ns = 10^9/40 = 25$ MHz

So,Maximum clock frequency at which the counter can operate is 25 MHz

8 votes -- Kalpna Bhargav (3.2k points)

4.10.2 Circuit Output: GATE1993_19 top http://gateoverflow.in/2316

Selected Answer

A(t+1) = DA = A'B +A'P'

B(t+1)= DB = PB' + P'A

Present State		**Input**	**Next State**	
A	B	P	A(t+1)	B(t+1)
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Note: Recheck the table by putting value of A, B , P in equations of A(t+1) and B (t+1)

5 votes -- Praveen Saini (53.6k points)

4.10.3 Circuit Output: GATE1993_6.1 top http://gateoverflow.in/2288

Selected Answer

6.1 (x+x'y') .(y+x'y') = (x+y')(x'+y) = xy + x'y' = exclusive nor

6.2 missing data

6.3

it follow the sequence 000, 100,110,111,011,001,000 It is a johnson counter so answer is e none of these

3 votes -- Praveen Saini (53.6k points)

4.10.4 Circuit Output: GATE1993_6.3 top http://gateoverflow.in/17237

Selected Answer

circuit behaves as shift register and mod6 counter

clock cycle output

1 100

2 110

3 111

4 011

5 001

6 000

EDIT- This is **J**ohnson counter which is application of **S**hift Register. And **J**ohnson counter is mod **2N** counter.

13 votes -- Pooja Palod (32.4k points)

4.10.5 Circuit Output: GATE1994_1.8 top http://gateoverflow.in/2445

Selected Answer

(((AB)' C)' (CD)')' = ((AB)'C) + CD) = (A' + B')C + CD = A'C + B'C + CD

10 votes -- Arjun Suresh (294k points)

4.10.6 Circuit Output: GATE1994_11 top

http://gateoverflow.in/2507

Selected Answer

Initial Q2=0,Q1=0,Q0=0

Clock 1

Q2=1 [J = (old Q0)'=1, K=1 , New Q2= Complement of old Q2=1]

Q1 =0 [D =old Q2=0, new Q1= D =0]

Q0=0 [T= old Q1=0, New Q0 = old Q0 =0]

Clock 2

Q2=0 [J = (old Q0)'=1, K=1 , New Q2= Complement of old Q2=0]

Q1 =1 [D =old Q2=1, new Q1= D =1]

Q0=0 [T= old Q1=0, New Q0 = old Q0 =0]

Clock 3

Q2=1 [J = (old Q0)'=1, K=1 , New Q2= Complement of old Q2=1]

Q1 =0 [D =old Q2=0, new Q1= D =0]

Q0=1 [T= old Q1=1, New Q0 = complement of old Q0 =1]

Clock 4

Q2=0 [J = (old Q0)'=0, K=1 , New Q2= Reset=0]

Q1 =1 [D =old Q2=1, new Q1= D =1]

Q0=1 [T= old Q1=0, New Q0 = old Q0 =1]

After 4 clock pulses Q2Q1Q0 is 011

Note : for JK FF Q(t+1) = JQ' +K'Q , for D FF Q(t+1) = D , and for T FF Q(t+1)= T⊕Q Where Q(t+1) represent new value of Q

12 votes -- Praveen Saini (53.6k points)

4.10.7 Circuit Output: GATE1996_2.21 top

http://gateoverflow.in/2750

Selected Answer

when b3b2 is 11 restore circuit to 0000..
it counts from 0 to 11 i.e. Radix 12 no ..
circuit used for binary to radix 12 conversion..

4 votes -- Digvijay (47k points)

4.10.8 Circuit Output: GATE1996_2.22 top

http://gateoverflow.in/2751

Selected Answer

Options for this question seem wrong, its expression f will come to A'B'C + A'BC + AB'C + ABC, that further can be minimized to C.

10 votes -- Manu Thakur (6k points)

4.10.9 Circuit Output: GATE1996_24 top http://gateoverflow.in/2776

Selected Answer

state Diagram :

S_7 -> S_3 -> S_1 -> S_4 -> S_2 -> S_5 -> S_6 -> S_7

b. Given the initial state S_4, S_0 state will not be reachable. If the system enters in S_0 state then Q_0=Q_1=Q_2=0 and after that it will stay in S_0 state indefinitely and can't go to any other state.

7 votes -- shreya ghosh (3.4k points)

4.10.10 Circuit Output: GATE1997_5.5 top http://gateoverflow.in/2256

Selected Answer

$f = (f_1 \wedge f_2) \vee f_3$

Since f_1 and f_2 are in canonical sum of products form, $f_1 \wedge f_2$ will only contain their common terms- that is $f_1 \wedge f_2 = \Sigma 8$

Now, $\Sigma 8 \vee f_3 = \Sigma 8, 9$
So, $f_3 = \Sigma 9$

7 votes -- Arjun Suresh (294k points)

4.10.11 Circuit Output: GATE1999_2.8 top http://gateoverflow.in/1486

Selected Answer

The figure is not clear- I assume there is a NOT gate just before taking Y making the final AND gate a NAND gate.

We have a steady state- meaning output is not changing. Y is 1 and remains 1 in the next state(s). So, we can write

$$Y = \overline{(\overline{(\overline{AY}).B}).C}$$

$$1 = \overline{A}.B + \overline{C}$$

So, $C = 0$ or $\overline{A}.B = 1$

So, option B is TRUE.

4 votes -- Arjun Suresh (294k points)

4.10.12 Circuit Output: GATE2000-2.12 top http://gateoverflow.in/659

Selected Answer

Here clocks are applied to both flip flops simultaneously

When 11 is applied to jk flip flop it toggles the value of P so op at P will be 1

Input to D flip flop will be 0(initial value of P) so op at Q will be 0

So ans is a

16 votes -- Pooja Palod (32.4k points)

4.10.13 Circuit Output: GATE2001-2.8 top

http://gateoverflow.in/726

Selected Answer

Answer is (a)

Given clock is + edge triggered.

See the first positive edge. X is 0, and hence the output is 0. Q_0 is 0 and Q_0' is 1.

Second + edge, X is 1 and Q_0' is also one. So, output is 1. (When second positive edge of the clock arrives, Q_0' would surely be 1 because the setup time of flip-flop is given as 20 ns and the clock period is >= 40 ns)

Third + edge, X is 1 and Q_0' is 0, So, output is 0. (Q_0' becomes 0 before the 3rd positive edge, but output Y won't change as the flip-flop is positive edge triggered)

Now, output never changes back to 1 as Q_0' is always 0 and when Q_0' finally becomes 1, X is 0.

Set up time and hold times are given just to ensure that edge triggering works properly.

15 votes -- Arjun Suresh (294k points)

Setup Time

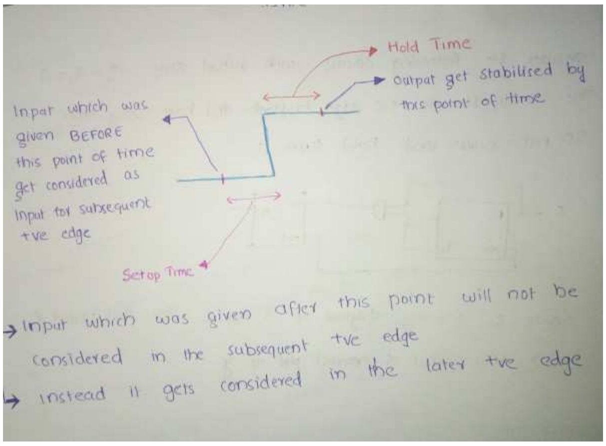
Minimum amount of time BEFORE the clock's active edge that the data must be stable for it to be latched correctly

Hold Time

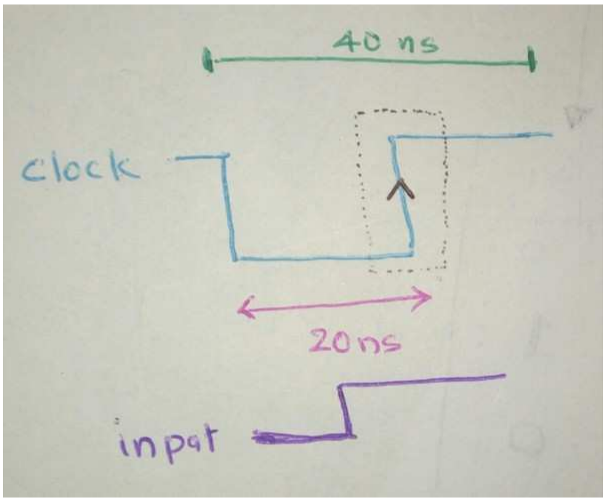
Minimum amount of Time AFTER the clock's active edge during which data must be stable

- Setup and Hold time measured with respect to active clock edge

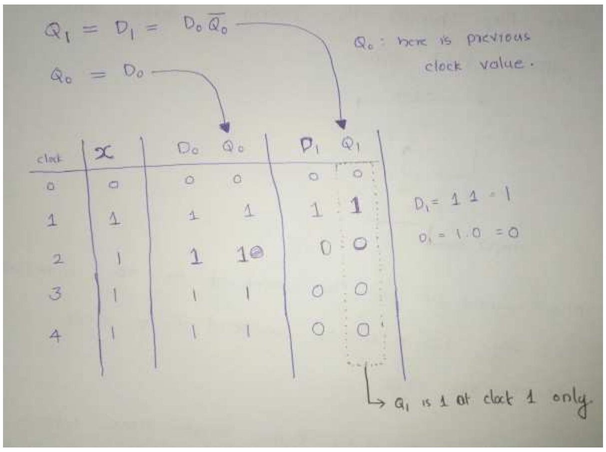
Read This



- Initial state
  $Q_0 = Q_1 = 0$ (given)
  Setup Time = 20ns
  Hold Time = 0ns
  Clock Period = 40ns
- Behaviour of Flip Flp depends on setup time and hold time
- Flip Flop responds to the input during +ve edge but it consider the stable input which was given even before setup time
- Flip-Flop changes its output to stable state within hold time

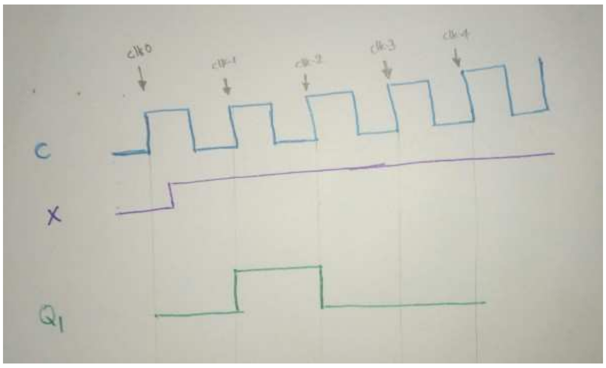


- Above input will not be considered in the immediate +ve edge but it will be considered in the next coming +ve edge
- In our Question X goes to $0 \rightarrow 1$ before stable time which get considered in the immediate +ve edge



clock	x	D_0	Q_0	D_1	Q_1
0	0	0	0	0	0
1	1	1	1	1	1
2	1	1	1	0	0
3	1	1	1	0	0
4	1	1	1	0	0

- From the truth table it is clear that Q_1 is **HIGH** at $\text{clock } 1$ only



11 votes -- pC (21.4k points)

4.10.14 Circuit Output: GATE2002-2.2 top

http://gateoverflow.in/832

Selected Answer

As X connected to $\mathbf{I_0}$ & $\mathbf{I_1}$ .Y connected to $\mathbf{I_2}$, Y' connected to $\mathbf{I_3}$ & A1 , Z connected to A0 and Z' connected to ENABLE (EN).

[F= (

$\overline{A1}$.

$\overline{A0}.\mathbf{I_0}$+

$\overline{A1}$.**A0**.$\mathbf{I_1}$ +**A1**.

$\overline{A0}$.$\mathbf{I_2}$ + **A1**.**A0**.$\mathbf{I_3}$).**EN**]

F = (XYZ' +XYZ + Y'ZY + ZY')Z'

= (XYZ' +XYZ + ZY')Z'

=XYZ'

18 votes -- Digvijay (47k points)

4.10.15 Circuit Output: GATE2004-61 top http://gateoverflow.in/1056

Selected Answer

sequence is
$0 - 2 - 3 - 1 - 0$

From the given sequence, we have state table as

Q_2	Q_1	Q_2^+	Q_1^+
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	1

Now we have present state and next state, use excitation table of T flip-flop

Q_2	Q_1	Q_2^+	Q_1^+	T_2	T_1
0	0	1	0	1	0
0	1	0	0	0	1
1	0	1	1	0	1
1	1	0	1	1	0

From state table,
$T_2 = Q_2 \odot Q_1$, and
$T_1 = Q_2 \oplus Q_1$

$X = T_1 = Q_2 \oplus Q_1$

21 votes -- Praveen Saini (53.6k points)

4.10.16 Circuit Output: GATE2005-15 top http://gateoverflow.in/1351

Selected Answer

The expression will be

f = [(x.y')'.(y.z)]'=[(x'+y).(y.z)] =[x'.y.z+y.z]'=[(x'+1).(y.z)]'=[1.(y.z)]'=[y.z]'=y'+z'

The final expression only contains y and z,

Therefore, answer will be (a) f is Independent of x

12 votes -- jec.himanshu (273 points)

4.10.17 Circuit Output: GATE2005-62 top http://gateoverflow.in/264

Selected Answer

D = AX + X'Q'

Y = D

A_i represent the logic level on the line A at the i-th clock period. If we see the timing diagram carefully, we can see that during the rising edge, the output Y is determined by the X value just before that rising edge. i.e., during the rising edge say for clk2, X value that determines the output is 1 and not 0 (because it takes some propagation delay for the 0 to reach the flip flop). Similarly, the A output that determines the output for clk i, is A_{i-1}

For clk1, X is 1, so, D = A = A_0

For clk2, X is 1, so D = A = A_1

For clk 3, X is 0, so D = Q_2' = A_1'

For clk4, X is 1, so D = A = A_3

For clk5, X is 1, so D = A = A_4

So, answer is A choice.

22 votes -- Arjun Suresh (294k points)

Answer: (A)

Explanation: The Flip Flop used here is a Positive edge triggered D Flip Flop, which means that only at the " **rising edge of the clock**" flip flop will capture the input provided at D and accordingly give the output at Q. And at other times of the clock the output doesn't change. The output of D flip flop is same as input, i.e. Y=Q=D (at the rising edge).

Now, in the question above, 5 clock periods are given, and we have to find the output Q or Y in those clock periods.

First, let's derive the boolean expression for the Logic gate.

which is :

D = AX + X' Q'

Now,

In the 1st clock period, (i.e. when t = 0 to 1)

here the clock has rising edge at t= 0, hence at this moment only, D flip flop will change its state.

In the 1st clock, X = 1, So, D = A. Now A logic line may have different levels at different clock periods, i.e. may be high or low, therefore we have to answer with respect to the ith clock period where Ai is the logic level (high or low) of logic line A in the ith clock.

So in the 1st clock period, A logic value should be A1 (i.e. value of A in 1st clock period), but due to the **delay provided by the Logic Gates (Propagation Delay)** the value of A used by Flip Flop is previous value of A only, i.e.it will capture the value of D resulted by using the logic line A in the 0th clock period, which is A0. Same happens with the value of X, i.e. instead of Xi, previous value of X is used in the in the ith clock period, which is Xi-1.

Now, In the 1st clock period value of X is same as in the 0th clock, i.e. logic 1. So, X = 1 ,and A = A0, therefore, D = A0, and hence Q = **Y = A0**

Similarly we have to do for other clock periods, i.e. instead of taking Ai and Xi, Ai-1 and Xi-1 need to be taken for getting the output in the ith clock period.

In the 2nd clock period, (i.e. when t = 1 to 2)

X = 1 (value in the previous clock), So, D = A1 (value of A in the previous clock) , therefore Q = **Y = A1**

In the 3rd clock period, (i.e. when t = 2 to 3)

X = 0 (value in the previous clock,see the timing diagram), So, D = Q' = A1′ , therefore Q = **Y = A1′** (because of the feedback line)

In the 4th clock period, (i.e. when t = 3 to 4)

X = 1 (value in the previous clock,), So, D = A3 , therefore Q = **Y = A3**

In the 5th clock period, (i.e. when t = 4 to 5)

X = 1 (value in the previous clock), so, D = A4 , therefore Q = **Y = A4**

Hence the output sequence is : **A0 A1 A1′ A3 A4**

Source : http://geeksquiz.com/gate-gate-cs-2005-question-62/

10 votes -- Prasanna Ranganathan (4.3k points)

4.10.18 Circuit Output: GATE2005-64 top http://gateoverflow.in/1387

Selected Answer

Clearly Q_0 alternates in every clk cycle as Q_0' is fed as input and it is D flipflop.

Q_1 becomes 1 if its prev value and current Q_0 differs (EXOR).

So, the sequence of transitions will be 00 -> 11 -> 01 -> 10 -> 00 (D) choice.

10 votes -- Arjun Suresh (294k points)

4.10.19 Circuit Output: GATE2005-IT-10 top http://gateoverflow.in/3755

Selected Answer

If it's looked carefully, bulb will be on when both switch s1 and s2 are in same state, either off or on. that is exnor operation

S1	S2	Bulb
0	0	On
0	1	Off
1	0	Off
1	1	On

it's Ex-NOR operation hence (C) is the correct option.

17 votes -- Manu Thakur (6k points)

4.10.20 Circuit Output: GATE2005-IT-43 top http://gateoverflow.in/3804

	A	B	C	Q1	Q2	Z	Comment
After 1st cycle	X	X	X	X	X	X	
After 2nd cycle	0	0	X	0	X	X	Q1 is 0 making A and B 0.
After 3rd cycle	X	X	1	1	1	1	Z is 1 making Q1 and Q2 1, Either A or B is 1. Q1' of previous cycle is 1.

The filling is done in reverse order. Here, none of the options matches. So, something wrong somewhere.

4 votes -- Arjun Suresh (294k points)

4.10.21 Circuit Output: GATE2006-35 top http://gateoverflow.in/1292

Selected Answer

if you solve this you will get XY' + Y'Z + XY (this can be simplified to X + Y'Z) with min terms as (1,4,5,6,7)

and option A has the same min terms

so option A is equivalent to XY' + Y'Z + XY

Ans (A)

5 votes -- Vikrant Singh (13.4k points)

Result of MUX (first one), is,say f1, = xz'+ y'z
Result of MUX(second one , f= f1y' +xy

=(xz'+y'z)y'+xy = xy'z' +y'z +xy =x(y'z' +y) +y'z = x(y'+y)(z'+y) +y'z =xz'+xy+y'z .

Option A.

Note:

1. f =I_0S' +I_1S ,for 2:1 MUX , where I0 and I1 are inputs , S is select line

2. Distributive property , A+BC = (A+B)(A+C)

3. A+A' =1

14 votes -- Praveen Saini (53.6k points)

4.10.22 Circuit Output: GATE2006-37 top http://gateoverflow.in/1295

Selected Answer

Data	Q0	Q1	Q2
1	1	$Q0_{start}$ XOR $Q2_{start}$ = 0 XOR 0 = 0	$Q1_{start}$ = 0
0	0	1 XOR 0 = 1	0
0	0	0 XOR 0 = 0	1
1	1	0 XOR 1 = 1	0
1	1	1 XOR 0 = 1	1
0	0	1 XOR 1 = 0	1
0	0	0 XOR 1 = 1	0
0	0	0 XOR 0 = 0	1
0	0	0 XOR 1 = 1	0

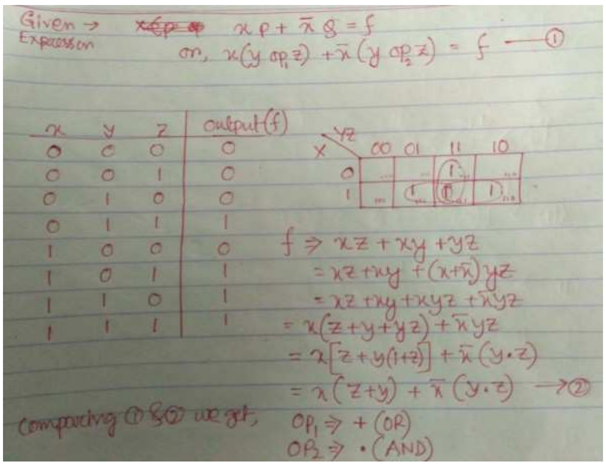
So, option C.

7 votes -- Arjun Suresh (294k points)

4.10.23 Circuit Output: GATE2006-IT-36 top http://gateoverflow.in/3575

Selected Answer

Solution



12 votes -- Subhankar Das (1.8k points)

Ans : D) OR,AND

This is because the value of 'f' should be 1 whenever a majority of the variables is 1. If we select x as '1' , the either of z or y or both z& y needs to be 1 for the output 'f' to be '1'

The output can be low only if less than 2 variables are high. ie.atleast 2 variables are low. hence z & y should be 0. therefore AND gates can be used.

13 votes -- Afaque Ahmad (849 points)

4.10.24 Circuit Output: GATE2007-36 top

http://gateoverflow.in/1234

Selected Answer

whenever A4 A3 A2 A1 =0 1 0 1 then clear line will be enabled as A3 and A1 set.

given table says that whenever clear control signal set , it clears to 0 0 0 0 , before the current clock cycle completes.

so 5 is cleared to 0 in the same clock cycle.

so counter sequence is 0, 1 , 2, 3, 4

Hence option C .

11 votes -- pramod (3.3k points)

4.10.25 Circuit Output: GATE2007-IT-38 top

http://gateoverflow.in/3471

Selected Answer

the final answer will come as --

a'+c'+d'+a'c+ab+bc

= a'(c+1)+c'+d'+ab+bc

=a'+c'+d'+ab+bc

=(a'+a)(a'+b)+(c'+c)(c'+b)+d'

=a'+b+c'+b+d'

=a'+b+c'+d'

Option C

9 votes -- Manali (2.8k points)

4.10.26 Circuit Output: GATE2007-IT-45 top

http://gateoverflow.in/3480

Selected Answer

To detect the fault, we should get an unexpected output. The final gate here is a NOR gate which produces output 0 if either of its input is 1 and else 1. i.e., the output will be 0 for inputs $(0,1),(1,0)$ and $(1,1)$ and output will be 1 for (0,0).

By grounding T is at 0. So, we can ignore the inputs $(1,0)$ and $(0,0)$ to the final NOR gate as they won't be detecting faults. Now, expected $(1,1)$ input will become $(1,0)$ due to grounding of T but produces same output 0 as for $(1,1)$. Hence this also cannot detect the defect. So, to detect the defect, the input to the final gate must be $(0,1)$ which is expected to produce a 0 but will produce a 1 due to grounding of T.

Now, for $(0,1)$ input for the final gate, we must have,

$X_3 = X_4 = 1$

But if $X_4 = 1$,the OR gate makes 1 output and we won't get $(0,1)$ input for the final gate. This means, no input sequence can detect the fault of the circuit.

Alternatively, we can write equation for the circuit as

$$(((x_1.x_2.x_3)' + x_4) + x_3.x_4)' = ((x_1.x_2.x_3)' + x_4)'.(x_3.x_4)' = x_1.x_2.x_3.x_4'.(x_3' + x_4') = x_1.x_2.x_3.x_4'$$

For the faulty circuit output will be

$$((x_1.x_2.x_3)' + x_4)' = x_1.x_2.x_3.x_4'$$

So, there is no effect of T being grounded here. Answer is D option.

13 votes -- Arjun Suresh (294k points)

4.10.27 Circuit Output: GATE2007-IT_40 top http://gateoverflow.in/3473

Selected Answer

Answer: A

The four bit register contains: 1011, 1101, 0110, 1011, 1101, **0110** after each shift.

10 votes -- Rajarshi Sarkar (35k points)

4.10.28 Circuit Output: GATE2008-IT-9 top http://gateoverflow.in/3269

Selected Answer

Answer: B

F = (x'z' + xz)' = xz' + x'z

15 votes -- Rajarshi Sarkar (35k points)

4.10.29 Circuit Output: GATE2010-31 top http://gateoverflow.in/2205

Selected Answer

Level 1:

$\overline{(P+Q)}\overline{(Q+R)}\overline{(P+R)}\overline{(Q+R)}$

Level 2:

$\overline{\overline{(P+Q)} + \overline{(Q+R)}} = (P+Q)(Q+R) = PQ + PR + Q + QR$

$\overline{\overline{(P+R)}\,\overline{(Q+R)}} = (P+R)(Q+R) = PQ + R + QR + PR$

Level 3:

$= \overline{PR + QR + PQ + Q + R}$

$= \overline{Q+R}$

$\therefore$ Answer: Option A

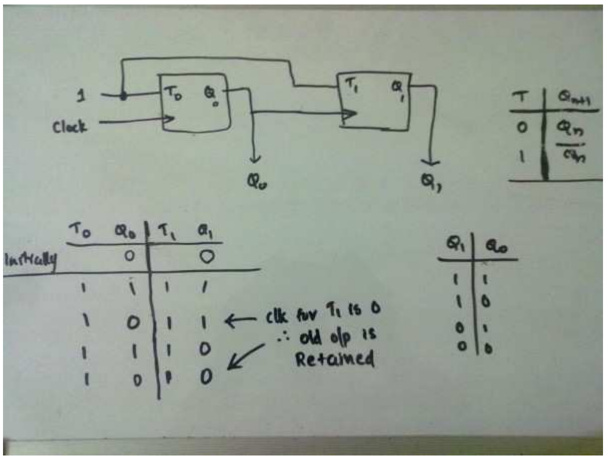
Answer is **A.**

6 votes -- Sona Praneeth Akula (4k points)

4.10.30 Circuit Output: GATE2010-32 top http://gateoverflow.in/2206

Selected Answer

Option A



2nd Flip-Flop will be active only when 1st Flip Flop produce output 1 . For clock 2 and 4 Old output is retained by Flip-Flop 2

8 votes -- pC (21.4k points)

answer - A

Initially Q0Q1 = 00

after first clock signal Q0 will be toggled and change to 1. It will activate clock of second FF in sequence and toggle that one as well.

Hence next output Q0Q1=11

Similarly next few sequences for Q0Q1 will be 01, 00

Hence answer sequence Q1Q0 will be 11,10,01,00

11 votes -- ankitrokdeonsns (9.1k points)

4.10.31 Circuit Output: GATE2010-9 top http://gateoverflow.in/2182

Selected Answer

$$f = S_0'S_1'R + S_0'S_1R' + S_0S_1'R' + S_0S_1R$$

$$= Q'P'R + Q'PR' + QP'R' + QPR = Q'(P \oplus R) + Q(P \oplus R)' = Q \oplus P \oplus R = P \oplus Q \oplus R$$

Doing truth value substitution,

P	Q	R	f	$P \oplus Q \oplus R$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

13 votes -- Arjun Suresh (294k points)

4.10.32 Circuit Output: GATE2011-50 top http://gateoverflow.in/2157

Selected Answer

Answer - D
As in D-flip-flop , next output is $Q^{+} = D$

$P_{i+1} = R_i$

$Q_{i+1} = (P_i + R_i)'$

$R_{i+1} = R_i' Q_i$

CLOCK	Inputs			Outputs		
	$D_1 = R$	$D_2 = \overline{(P+R)}$	$D_3 = Q\,\bar{R}$	P	Q	R
1	0	1	0	0	1	0
2	0	1	1	0	1	1
3	1	0	0	1	0	0
4	0	0	0	0	0	0

So Total number of distinct outputs is 4

10 votes -- ankitrokdeonsns (9.1k points)

4.10.33 Circuit Output: GATE2011-51 top

http://gateoverflow.in/43318

Selected Answer

Characteristic equation of D FF is ,
$Q(t+1) = D$

so
$P^{+} = R,\ Q^{+} = \overline{P+R},\ \text{and } R^{+} = Q.R'$

Sequence of states will be as

Clock Pulse	PQR
Initially	000
1	010
2	011
3	100
4	000

4 is the number of distinct states.

9 votes -- Praveen Saini (53.6k points)

4.10.34 Circuit Output: GATE2014-3-45 top

http://gateoverflow.in/2079

Selected Answer

Initial State			Input						Next State		
Q2	Q1	Q0	J2	K2	J1	K1	J0	K0	Q2'	Q1'	Q0'
0	0	0	1	0	0	1	0	1	1	0	0

1 **Initial State**	0	0	1 **Input**	0	1	0	0	1	1 **Next State**	1	0
1	1	0	0	0	1	0	1	1	1	1	1

∴ Option C

13 votes -- Gate_15_isHere (639 points)

4.11 Conjunctive Normal Form(1) top

4.11.1 Conjunctive Normal Form: GATE2007-48 top

http://gateoverflow.in/1246

Which of the following is TRUE about formulae in Conjunctive Normal Form?

A. For any formula, there is a truth assignment for which at least half the clauses evaluate to true.

B. For any formula, there is a truth assignment for which all the clauses evaluate to true.

C. There is a formula such that for each truth assignment, at most one-fourth of the clauses evaluate to true.

D. None of the above.

gate2007 digital-logic normal conjunctive-normal-form

Answer

Answers: Conjunctive Normal Form

4.11.1 Conjunctive Normal Form: GATE2007-48 top

http://gateoverflow.in/1246

Selected Answer

answer = **option A**

To Prove: For any formula, there is a truth assignment for which at least half the clauses evaluate to true

Proof:
Consider an arbitrary truth assignment. For each of its clause i, introduce a random variable.

$$X_i = \begin{cases} 1 & \text{if clause } i \text{ is satisfied;} \\ 0 & \text{otherwise.} \end{cases}$$

Then, $X = \sum_i X_i$ is the number of satisfied clauses.

Given any clause c, it is unsatisfied only if all of its k constituent literals evaluates to false; as they are joined by OR operator coz the formula is in CNF.
Now, because each literal within a clause has a $\frac{1}{2}$ chance of evaluating to true independently of any of the truth value of any of the other literals, the probability that they are all false is $\left(\frac{1}{2}\right)^k = \frac{1}{2^k}$.
Thus, the probability that c is satisfied(true) is $1 - \frac{1}{2^k}$

So, $E(X_i) = 1 \times \left(1 - \frac{1}{2^k}\right) = 1 - \frac{1}{2^k}$
This means that
$E(X_i) \geq \frac{1}{2}$
(try putting arbitrary valid values of k to see that)

Summation on both sides to get $E(X)$,
Therefore, we have $E(X) = \sum_i E(X_i) \geq \frac{m}{2}$; where m is the number of clauses.
$E(X)$ represents expected number of satisfied(to true) clauses.

So, there must exist an assignment that satisfies(to true) at least half of the clauses.

👍 12 votes -- Amar Vashishth (28.7k points)

4.12 Decoder(1) top

4.12.1 Decoder: GATE2007-8, ISRO2011-31 top http://gateoverflow.in/1206

How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

A. 7
B. 8
C. 9
D. 10

gate2007 digital-logic normal isro2011 decoder

Answer

Answers: Decoder

4.12.1 Decoder: GATE2007-8, ISRO2011-31 top http://gateoverflow.in/1206

Selected Answer

ans is C:

to get 6:64 we need 64 o/p

we have 3:8 decode with 8 o/p. so we need 64/8=8 decoders

now to select any of this 8 decoder we need one more decoder.

total=8+1= 9 decoders

👍 12 votes -- jayendra (8.1k points)

4.13 Digital Circuits(3) top

4.13.1 Digital Circuits: GATE1996-5 top http://gateoverflow.in/2757

A logic network has two data inputs A and B, and two control inputs C_0 and C_1. It implements the function F according to the following table.

C_1	C_2	F
0	0	$\overline{A+B}$
0	1	$A+B$
1	0	$A \oplus B$

Implement the circuit using one 4 to 1 Multiplexer, one 2-input Exclusive OR gate, one 2-input AND gate, one 2-input OR gate and one Inverter.

gate1996 digital-logic normal digital-circuits

Answer

4.13.2 Digital Circuits: GATE2013-5 top http://gateoverflow.in/1414

In the following truth table, $V = 1$ if and only if the input is valid.

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

What function does the truth table represent?

A. Priority encoder
B. Decoder
C. Multiplexer
D. Demultiplexer

gate2013 digital-logic normal digital-circuits

Answer

4.13.3 Digital Circuits: GATE2014-3-8 top

http://gateoverflow.in/2042

Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.

```
f(x, a, b, y)
{
    if(x is 1) y = a;
    else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

A. Full adder
B. Priority encoder
C. Multiplexor
D. Flip-flop

gate2014-3 digital-logic easy digital-circuits

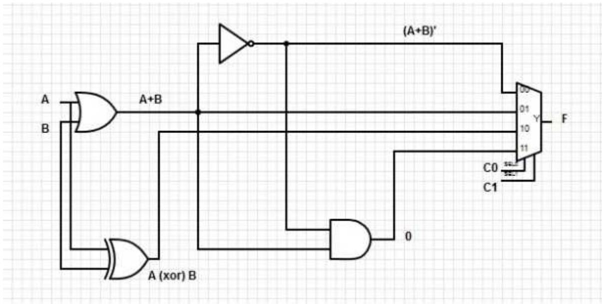
Answer

Answers: Digital Circuits

4.13.1 Digital Circuits: GATE1996-5 top

http://gateoverflow.in/2757

Selected Answer



This is the implementation asked in question

C0 = 0 , C1 = 0 line 00 will be selected and F will give (A+B)'

C0 = 0 , C1 = 1 line 01 will be selected and F will give (A+B)

C0 = 1 , C1 = 0 line 10 will be selected and F will give (A⊕B)

C0 = 1 , C1 = 1 line 11 will be selected and F will give (A+B)'.(A+B) =0

6 votes -- Praveen Saini (53.6k points)

4.13.2 Digital Circuits: GATE2013-5 top http://gateoverflow.in/1414

Selected Answer

Answer is **A.**

For 2^n inputs we are having n outputs. Here n=2.

http://en.wikipedia.org/wiki/Priority_encoder

10 votes -- Sona Praneeth Akula (4k points)

4.13.3 Digital Circuits: GATE2014-3-8 top http://gateoverflow.in/2042

Selected Answer

2X1 multiplexer

12 votes -- Arpit Dhuriya (3k points)

4.14 Digital Counter(7) top

4.14.1 Digital Counter: GATE1994-2.1 top http://gateoverflow.in/2468

The number of flip-flops required to construct a binary modulo N counter is ___________

gate1994 digital-logic easy digital-counter

Answer

4.14.2 Digital Counter: GATE2005-IT-11 top http://gateoverflow.in/3756

How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?

A. 134
B. 133
C. 124
D. 123

gate2005-it digital-logic digital-counter normal

Answer

4.14.3 Digital Counter: GATE2011-15 top

http://gateoverflow.in/2117

The minimum number of D flip-flops needed to design a mod-258 counter is

A. 9
B. 8
C. 512
D. 258

gate2011 digital-logic normal digital-counter

Answer

4.14.4 Digital Counter: GATE2014-2-7 top

http://gateoverflow.in/1959

Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an $n\text{-to-}2^n$ bit decoder. This circuit is equivalent to a

A. k-bit binary up counter.
B. k-bit binary down counter.
C. k--bit ring counter.
D. k-bit Johnson counter.

gate2014-2 digital-logic normal digital-counter

Answer

4.14.5 Digital Counter: GATE2015-1_20 top

http://gateoverflow.in/8219

Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

A. 0, 1, 3, 7, 15, 14, 12, 8, 0
B. 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
C. 0, 2, 4, 6, 8, 10, 12, 14, 0
D. 0, 8, 12, 14, 15, 7, 3, 1, 0

gate2015-1 digital-logic digital-counter easy

Answer

4.14.6 Digital Counter: GATE2015-2_7 top

http://gateoverflow.in/8054

The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, ...) is ________.

gate2015-2 digital-logic digital-counter normal numerical-answers

Answer

4.14.7 Digital Counter: GATE2017-2-42 top

http://gateoverflow.in/118557

The next state table of a 2-bit saturating up-counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expressions for T_1 and T_0 are

A. $T_1 = Q_1 Q_0, \quad T_0 = \bar{Q}_1 \bar{Q}_0$
B. $T_1 = \bar{Q}_1 Q_0, \quad T_0 = \bar{Q}_1 + \bar{Q}_0$
C. $T_1 = Q_1 + Q_0, \quad T_0 = \bar{Q}_1 \bar{Q}_0$
D. $T_1 = \bar{Q}_1 Q_0, \quad T_0 = Q_1 + Q_0$

gate2017-2 digital-logic digital-counter

Answer

Answers: Digital Counter

4.14.1 Digital Counter: GATE1994-2.1 top

http://gateoverflow.in/2468

Selected Answer

Let say we have to Design mod-8 counter i.e 000 to 111. so we need 3 bit to represent i.e 3 FF

for Mod N

$2^x = N$

x = ceiling ($\log_2 N$)

12 votes -- Praveen Saini (53.6k points)

4.14.2 Digital Counter: GATE2005-IT-11 top

http://gateoverflow.in/3756

Selected Answer

D.123 Pulses.

As in a 2^8 Counter the range would be from 0-255. Hence to go from 10101100 (172) to 00100111 (39) , the counter has to go initially from 172 to 255 and then from 0 to 39.

Hence to go from 172 to 255, 255-172 = 83 Clock pulses would be required. then from 255 to 0 , again 1 clock pulse would be required.Then from 0 to 39 , 39 clock pulses would be required. Hence in total 83+1+39 =123 Clock pulses would be required.

22 votes -- Afaque Ahmad (849 points)

4.14.3 Digital Counter: GATE2011-15 top

http://gateoverflow.in/2117

Selected Answer

mod 258 counter has 258 states. We need to find no. of bits to represent 257 at max.
$2^n \geq 258 \Rightarrow n \geq 9.$

Answer is **A**

12 votes -- Sona Praneeth Akula (4k points)

4.14.4 Digital Counter: GATE2014-2-7 top

http://gateoverflow.in/1959

Selected Answer

In binary counter of n bits can count upto 2^n numbers..when this op from counter is fed to decoder one of n out of 2^n will be activated..so this arrangement of counter and decoder is behaving as 2^n(k) ring counter..

12 votes -- Pooja Palod (32.4k points)

4.14.5 Digital Counter: GATE2015-1_20 top

http://gateoverflow.in/8219

Selected Answer

option D

0000 - 0

1000 - 8

1100 - 12

and so on.

http://en.wikipedia.org/wiki/Ring_counter

12 votes

-- GATERush (1.2k points)

4.14.6 Digital Counter: GATE2015-2_7 top

http://gateoverflow.in/8054

Selected Answer

First, lets design a counter for 0, 1, 2, 3. It is a MOD - 4 counter. Hence, number of Flip Flops required will be two. Count sequence will be:

00
01
10
11

Count sequence you mentioned is:

00
00
01
01
10
10
11
11

Now, two flip flops won't suffice, since we are confronted with repeated sequence, we may add another bit to the above sequence:

000
100
001
101
010
110
011
111

Now each and every count is unique, occurring only once. Meanwhile, our machine has been extended to a MOD - 8 counter. Hence, three Flip Flops would do.

Just neglect the MSB flip flop output and take the o/p of only other two. So, we have :
0,0,1,1,2,2,3,3,repeat -->

42 votes

-- Mithlesh Upadhyay (5.4k points)

4.14.7 Digital Counter: GATE2017-2-42 top

http://gateoverflow.in/118557

Selected Answer

Ans B)

q1	q0	(q1)+	(q0)+	T1	T2	
0	0	0	1	0	1	
0	1	1	0	1	1	
1	0	1	1	0	1	
1	1	1	1	0	0	

By using above excitation table,

T1=q1'q0,

T2=(q1q0)'=q1'+q0'

2 votes -- jatin saini (2.1k points)

4.15 Dual Function(1) top

4.15.1 Dual Function: GATE2014-2-6 top http://gateoverflow.in/1958

The dual of a Boolean function $F(x_1, x_2, \ldots, x_n, +, ., ')$, written as F^D is the same expression as that of F with $+$ and $\cdot$ swapped. F is said to be self-dual if $F = F^D$. The number of self-dual functions with n Boolean variables is

A. 2^n
B. 2^{n-1}
C. 2^{2^n}
D. $2^{2^{n-1}}$

gate2014-2 digital-logic normal dual-function

Answer

Answers: Dual Function

4.15.1 Dual Function: GATE2014-2-6 top http://gateoverflow.in/1958

Selected Answer

A function is self dual if it is equal to its dual (A dual function is obtained by interchanging $.$ and $+$).

For self-dual functions,

1. Number of min terms equals number of max terms
2. Function should not contain two complementary minterms - whose sum equals $2^n - 1$, where n is the number of variables.

	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

so here
(0,7) (1,6) (2,5) (3,4) are complementary terms so in self-dual we can select any one of them but not both.

totally $2 \times 2 \times 2 \times 2 = 2^4$ possibility because say from $(0, 7)$ we can pick anyone in minterm but not both.

For example, let $f = \sum(0,6,2,3)$

NOTE:here i have taken only one of the complementary term for min term from the sets.

so remaining numbers will go to MAXTERMS

For above example, $2^4 = 16$ self dual functions are possible

so if we have N variables, total Minterms possible is 2^n

then half of them we selected so 2^{n-1}.

and now we have 2 choices for every pair for being selected.

so total such choices $= \underbrace{2 \times 2 \times 2 \times 2 \ldots 2}_{2^{n-1}\text{ times}}$

$\therefore 2^{2^{n-1}}$ (option D)

21 votes -- Kalpish Singhal (2.1k points)

4.16 Fixed Point Representation(1) top

4.16.1 Fixed Point Representation: GATE2017-1-7 top http://gateoverflow.in/118287

The n-bit fixed-point representation of an unsigned real number X uses f bits for the fraction part. Let $i = n - f$. The range of decimal values for X in this representation is

(A) 2^{-f} to 2^i

(B) 2^{-f} to $\left(2^i - 2^{-f}\right)$

(C) 0 to 2^i

(D) 0 to $\left(2^i - 2^{-f}\right)$

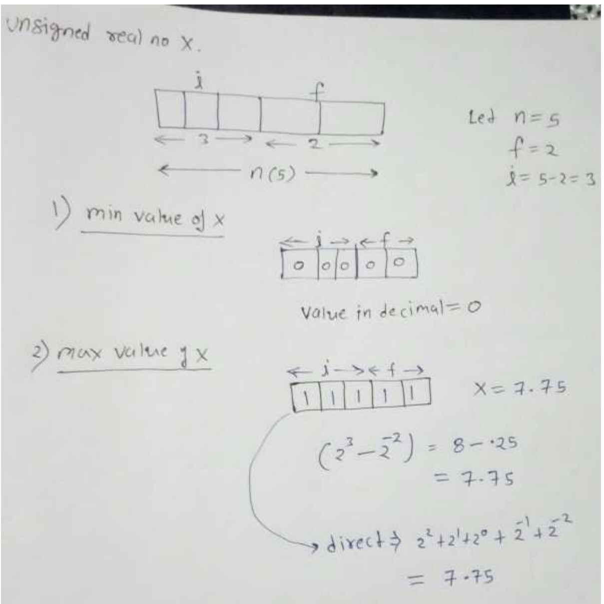
gate2017-1 digital-logic number-representation fixed-point-representation

Answer

Answers: Fixed Point Representation

4.16.1 Fixed Point Representation: GATE2017-1-7 top http://gateoverflow.in/118287

Selected Answer



so D is the ans.

👍 8 votes -- 2018 (5.2k points)

4.17 Flip Flop(8) top

4.17.1 Flip Flop: GATE 2016-1-8 top http://gateoverflow.in/39670

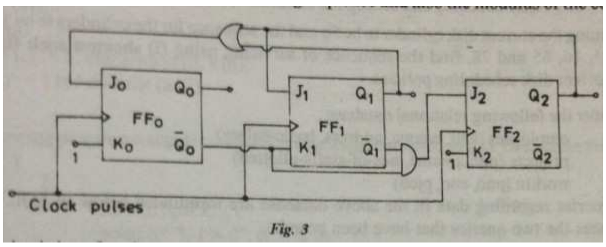
We want to design a synchronous counter that counts the sequence $0-1-0-2-0-3$ and then repeats. The minimum number of J-K flip-flops required to implement this counter is ______________.

gate2016-1 digital-logic digital-counter flip-flop normal numerical-answers

Answer

4.17.2 Flip Flop: GATE1990-5c top http://gateoverflow.in/85400

For the synchronous counter shown in Fig.3, write the truth table of Q_0, Q_1, and Q_2 after each pulse, starting from $Q_0 = Q_1 = Q_2 = 0$ and determine the counting sequence and also the modulus of the counter.



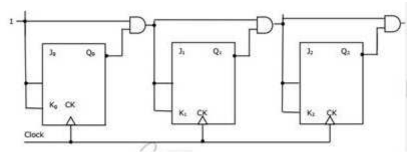
gate1990 descriptive digital-logic flip-flop

Answer

4.17.3 Flip Flop: GATE1991_5,c top http://gateoverflow.in/26442

Find the maximum clock frequency at which the counter in the figure below can be operated. Assume that the propagation delay through each flip flop and each AND gate is
10

ns. Also assume that the setup time for the JK inputs of the flip flops is negligible.



gate1991 digital-logic flip-flop

Answer

4.17.4 Flip Flop: GATE1992_04_c top http://gateoverflow.in/17408

Design a 3-bit counter using D-flip flops such that not more than one flip-flop changes state between any two consecutive states.

gate1994 digital-logic flip-flop

Answer

4.17.5 Flip Flop: GATE2001-11 top http://gateoverflow.in/752

A sequential circuit takes an input stream of 0's and 1's and produces an output stream of 0's and 1's. Initially it replicates the input on its output until two consecutive 0's are encountered on the input. From then onward, it produces an output stream, which is the bit-wise complement of input stream until it encounters two consecutive 1's, whereupon the process repeats. An example input and output stream is shown below.

The input stream:	101100|01001011	0|11
The desired output	101100|10110100	0|11

J-K master-slave flip-flops are to be used to design the circuit.

a. Give the state transition diagram
b. Give the minimized sum-of-product expression for J and K inputs of one of its state flip-flops

gate2001 digital-logic normal descriptive flip-flop

Answer

4.17.6 Flip Flop: GATE2004-18, ISRO2007-31 top http://gateoverflow.in/1015

In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

A. $Q = 0, Q' = 1$
B. $Q = 1, Q' = 0$
C. $Q = 1, Q' = 1$
D. Indeterminate states

gate2004 digital-logic easy isro2007 flip-flop

Answer

4.17.7 Flip Flop: GATE2015-1_37 top http://gateoverflow.in/8287

A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the state holding mode of the JK flip-flops. Both the flip-flops have non-zero propagation delays.

A. 0110110...
B. 0100100...
C. 011101110...
D. 011001100...

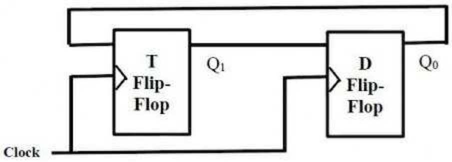
gate2015-1 digital-logic flip-flop normal

Answer

4.17.8 Flip Flop: GATE2017-1-33 top

http://gateoverflow.in/118315

Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

(A) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively.

(B) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 01 respectively.

(C) Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively.

(D) Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively.

gate2017-1 digital-logic flip-flop normal

Answer

Answers: Flip Flop

4.17.1 Flip Flop: GATE 2016-1-8 top

http://gateoverflow.in/39670

Selected Answer

we need four JK flipflops..
0->1->0->2->0->3
0000->0001->0100->0010->1000->0011
There are 6 states and 3 of them correspond to same state..
to differentiate between 0,1,2,3 we need 2 bits.
to differentiate between 3 0's we need 2 bits..
So total 4 bits=4 FF

Edit:
whether using extra combinational logic for output is allowed in a counter..???
Page No. 10/11 http://textofvideo.nptel.iitm.ac.in/117105080/lec23.pdf

Now, if you see the counters, now a counter we can define in this way the counter is a degenerate finite state machine, where the **state** is the **only** output. So, there is **no other primary output** from this machine, so the counter is defined like that.

ALSO

Page No. 3 http://textofvideo.nptel.iitm.ac.in/117106086/lec24.pdf

Counter you know what counter it is, that's what we want we count the output of counter what is the particular count what is the current count that is the output of a count so no external output. **The counter is a case of a state machine in which there are no external inputs, no external outputs.**

Page No. 10 http://textofvideo.nptel.iitm.ac.in/117106086/lec24.pdf always do that let us say 1 0 0 you want count twice you can put 1 0 0 to 1 0 0 but then when you draw the Karnaugh Map you don't know which 1 0 0 you are talking about so instead of doing that you can have an external input defined when x is equal to 0 it remains there so you can put x is equal to 0 and for all of those x is equal to 1. So from S_0 to S_1 it will remain, both 0 and 1 it will take here, from here it will take here only if x is equal to 1 and if x is equal to 0 it will remain here so external input can be used more elegantly for that design.

at 35:30 www**[dot]**youtube**[dot]**com/watch?v=MiuMYEn3dpg

Here In Counter, we cannot use external variable, that purpose will be served by FF's only
We have four distinct states 0,1,2,3 so 2 FF for them for 3 0's to distinguish we need 2 more FF's

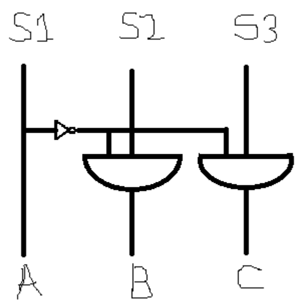
4 FF required.

41 votes -- Abhilash Panicker (8.8k points)

I am using two AND gates and a NOT gate along with 3 flip flops.

there are 6 unique states. lets assume there is a synchronous counter the generates below sequence:

100->001->101->010->110->011->100.



Let output of 3 flip flops be S1, S2 , S3. Take them through below circuit

S1	S2	S3	A	B	C
1	0	0	1	0	0
0	0	1	0	0	1
1	0	1	1	0	0
0	1	0	0	1	0
1	1	0	1	0	0
0	1	1	0	1	1

if we take B C as final output we can generate 0->1->0->2->0->3.

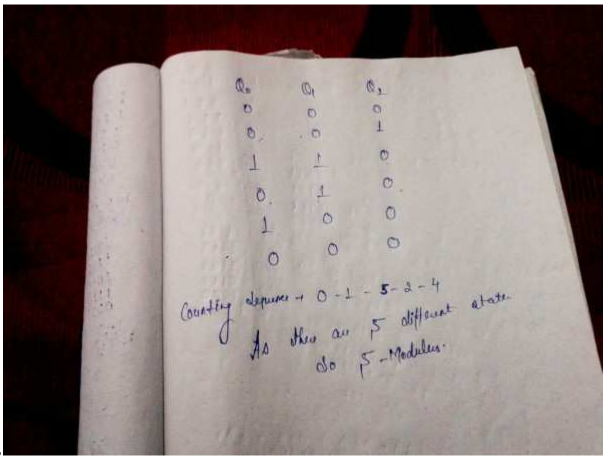
So I think it is possible with 3 flip flops.

Requesting comments.

10 votes -- vinayk (107 points)

4.17.2 Flip Flop: GATE1990-5c top http://gateoverflow.in/85400

Selected Answer



.....

1 votes -- kirti singh (3.4k points)

4.17.3 Flip Flop: GATE1991_5,c top http://gateoverflow.in/26442

Selected Answer

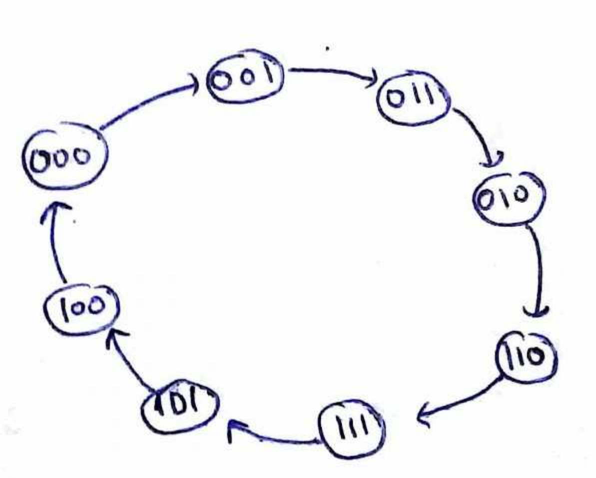
In a JK flip flop the output toggles when both J and K inputs are 1. So, we must ensure that with each clock the output from the previous stage reaches the current stage. From the figure, there is an AND gate between each stage and $2 \times 10 = 20ns$ (10ns for output to reach the gate and 10ns for the output of AND gate to reach the next flipflop) is needed for the output to reach the next stage. So, minimum time period needed for clock is 20ns which would mean a maximum clock frequency of $1/20GHz = 50MHz$

21 votes -- Arjun Suresh (294k points)

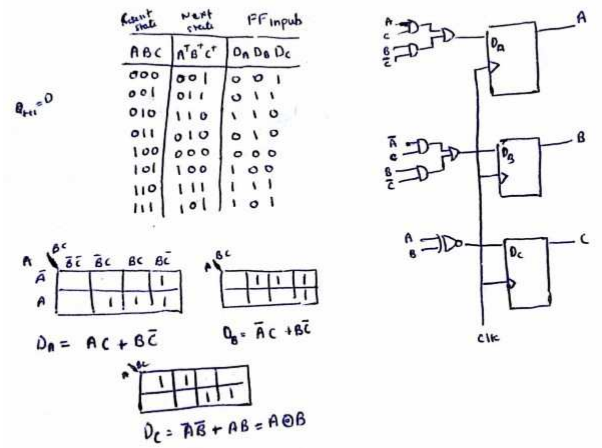
4.17.4 Flip Flop: GATE1992_04_c top http://gateoverflow.in/17408

Selected Answer

State diagram will be as (remember concept of gray code)



State table and 3-bit synchronous counter with D FFs, will be as



👍 9 votes -- Praveen Saini (53.6k points)

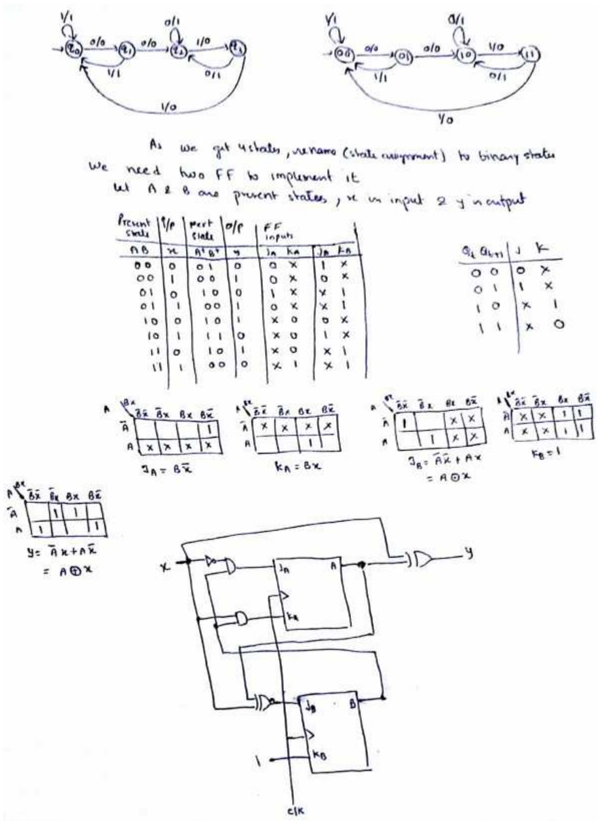
4.17.5 Flip Flop: GATE2001-11 top

http://gateoverflow.in/752

Selected Answer

We can design a Mealy Machine as per the requirement given in the question.

From which we will get state table, and we can design sequential circuit using any Flip-flop from the state table (with the help of excitation table) :



👍 7 votes -- Praveen Saini (53.6k points)

4.17.6 Flip Flop: GATE2004-18, ISRO2007-31 top

http://gateoverflow.in/1015

Selected Answer

If both R =0 ,S=0 ,then both Q and Q' tend to be '1'. NAND gate says if both inputs are 1,the output is 0. The logic of the circuit (Q' is complement of Q) not satisfied, Logic state is said to be indeterminate state or racing state. Each state, Q ='1'and Q ='0', and Q ='0', Q='1' trying to race through so "RACE CONDITION" occurs and output become unstable. So ans is (D).

21 votes -- shekhar chauhan (42.9k points)

4.17.7 Flip Flop: GATE2015-1_37 top http://gateoverflow.in/8287

Selected Answer

Q_{prev}	D	Q (JK)	Explanation
-	1	0	Now, the D output is 1, meaning J and K = 1, for next cycle
0	0	1	J = K = 1 (D output from prev state), so output toggles from 0 to 1
1	1	1	J = K = 0, so output remains 1
1	1	0	J = K = 1, so output toggles from 1 to 0
0	0	1	J = K = 1, so output toggles from 0 to 1
1	1	1	J = K = 0, so output remains 1

D flipflop output will be same as its input and JK flipflop output toggles when 1 is given to both J and K inputs.

i.e., $Q = D_{prev}(Q_{prev}') + (D_{prev}')Q_{prev}$

9 votes -- Arjun Suresh (294k points)

4.17.8 Flip Flop: GATE2017-1-33 top http://gateoverflow.in/118315

Selected Answer

Since it is synchronous so
After every clock cycle **T will toggle if input is 1** and **Hold State if input is 0**...D's Output always follows input

- **After 1 clock cycles :** **Q1**=0(Toggle) **Q0**=1
- **After 2 clock cycles :** **Q1**=1(toggles) **Q0**=0
- **After 3 clock cycles:** **Q1**=1(hold) **Q0**=1
- **After 4 clock cycles:** **Q1**=0(toggles) **Q0**=1

Hence OPTION (B) CORRECT

6 votes -- sriv_shubham (2.7k points)

4.18 Floating Point Representation(6) top

4.18.1 Floating Point Representation: GATE1987-1-vii top http://gateoverflow.in/80201

The exponent of a floating-point number is represented in excess-N code so that:

A. The dynamic range is large.
B. The precision is high.
C. The smallest number is represented by all zeros.
D. Overflow is avoided.

gate1987 digital-logic number-representation floating-point-representation

Answer

4.18.2 Floating Point Representation: GATE1990-1-iv top http://gateoverflow.in/83830

Fill in the blanks:

A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,

(a) The range of the exponent is ____________

(b) The range of the exponent is ____________, if the scale factor is represented in excess-64 format.

gate1990 descriptive digital-logic number-representation floating-point-representation

Answer

4.18.3 Floating Point Representation: GATE2003-43 top http://gateoverflow.in/934

The following is a scheme for floating point number representation using 16 bits.

Bit Position	15	14 9	8 0
	s	*e*	*m*
	Sign	Exponent	Mantissa

Let *s*, *e*, and *m* be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:

$$\begin{cases} (-1)^s \left(1 + m \times 2^{-9}\right) 2^{e-31}, & \text{if the exponent} \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

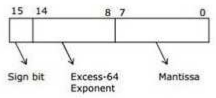
A. 2^{-40}
B. 2^{-9}
C. 2^{22}
D. 2^{31}

gate2003 digital-logic number-representation floating-point-representation normal

Answer

4.18.4 Floating Point Representation: GATE2005-85a top http://gateoverflow.in/1407

Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The decimal number 0.239×2^{13} has the following hexadecimal representation (without normalization and rounding off):

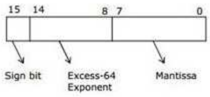
A. 0D 24
B. 0D 4D
C. 4D 0D
D. 4D 3D

gate2005 digital-logic number-representation floating-point-representation normal

Answer

4.18.5 Floating Point Representation: GATE2005-85b top http://gateoverflow.in/82139

Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field.

The normalized representation of the above number (0.239×2^{13}) is:

A. 0A 20
B. 11 34
C. 49 D0
D. 4A E8

gate2005 digital-logic number-representation floating-point-representation normal

Answer

4.18.6 Floating Point Representation: GATE2017-2-12 top http://gateoverflow.in/118434

Given the following binary number in 32-bit (single precision) $IEEE - 754$ format :

$$00111110011011010000000000000000$$

The decimal value closest to this floating-point number is :

A. $1.45 * 10^{1}$
B. $1.45 * 10^{-1}$
C. $2.27 * 10^{-1}$
D. $2.27 * 10^{1}$

gate2017-2 digital-logic number-representation floating-point-representation

Answer

Answers: Floating Point Representation

4.18.1 Floating Point Representation: GATE1987-1-vii top http://gateoverflow.in/80201

Selected Answer

Ans : C) The smallest number is represented by all zeros.

In computer system, a floating-point number is represented as S E M, i.e. using Sign bit, Exponent bits and Mantissa bits.

The exponent can be a positive as well as a negative number. So to represent negative number we can use 1's complement or 2's complement. Better choice would be 2's complement.

If we use 2's complement system to represent exponent, then problem will arise while comparing 2 floating point numbers. For example, if exponent of the 2 numbers are negative then for comparing we will have to convert them into positive number.

So to avoid this extra work, excess-N code is used so that all exponent can be represented in positive numbers, starting with 0.

4 votes -- Kantikumar (3.5k points)

4.18.2 Floating Point Representation: GATE1990-1-iv top http://gateoverflow.in/83830

Selected Answer

a) range of exponent

as given exponent bits are 7 bits ....

so min it could be all 7 bit are 0's and maximum it could all 1's ...

minimum number =0 , and maximum number = 127

as in a) part nothing is given about bias .. so bias = $2^{7-1} - 1 = 63$ (nothing is given about single precision also so i used general method)

so exponent range will be 0-63 to 127-63 = - 63 to 64 .

----

b) minimum number = 0 , maximum number = 127 ,

as here given excess 64 so bias number is 64 ,

then range will be 0-64=-64 to (127-64=63) 63..

here in question given that base is 16 , it will get simply shifting of mantissa bit ... yes range of value is increased by large base ...$(-1)^s$ (0.M) $16^{\text{E-bias}}$.

correct me if i am wrong

2 votes -- sonam vyas (13.2k points)

4.18.3 Floating Point Representation: GATE2003-43 top http://gateoverflow.in/934

Selected Answer

Maximum difference between two successive real number will occur at extremes. This is because numbers are represented upto mantissa bits and as the exponent grows larger, the difference gets multiplied by a larger value. (The minimum difference happens for the least positive exponent value).
Biasing will be done by adding 31 as given in question. So, actual value of exponent will be represented value - 31. Also, we can not have exponent field as all 1's as given in question (usually taken for representing infinity, NAN etc). So, largest value that can be stored is 111110 = 62.
Largest number will be $1.111111111 \times 2^{62-31} = (2 - 2^{-9}) \times 2^{31}$
Second largest number will be $1.111111110 \times 2^{62-31} = (2 - 2^{-8})\, 2^{31}$
So, difference between these two numbers $= (2 - 2^{-9}) \times 2^{31} - (2 - 2^{-8}) \times 2^{31} = 2^{31}\left[(2 - 2^{-9}) - (2 - 2^{-8})\right] = 2^{31}\left[2^{-8} - 2^{-9}\right] = 2^{31} \times 2^{-9} = 2^{22}$

10 votes -- Ashish Gupta (921 points)

4.18.4 Floating Point Representation: GATE2005-85a top http://gateoverflow.in/1407

Selected Answer

answer = **option D** in both questions.

0.239 = $(0.00111101)_2$

a)Store exponent = actual + biasing

13 + 64 = 77

$(77)_{10} = (1001101)_2$

ans is 1001101 00111101 =$4D3D$

b) For normalized representation

0.00111101 $*2^{13}$

1.11101 $*2^{10}$

Store exponent = 10+64=74

$(74)_{10}$ = $(1001010)_2$

ans 0 1001010 11101000=$4AE8$

10 votes -- Pooja Palod (32.4k points)

4.18.5 Floating Point Representation: GATE2005-85b top http://gateoverflow.in/82139

Selected Answer

For finding normalised representation we need to find unnormalised one first..So we have ,

0.239 * 2^{13} as the number ..So we find the binary equivalent of 0.239 till 8 digits as capacity of mantissa field is 8 bits..

So following the procedure we have ,

0.239 * 2 = 0.478

0.478 * 2 = 0.956

0.956 * 2 = 1.912

0.912 * 2 = 1.824

0.824 * 2 = 1.648

0.648 * 2 = 1.296

0.296 * 2 = 0.512

0.512 * 2 = 1.024

We stop here as we have performed 8 iterations and hence 8 digits of mantissa of unnormalised number is obtained.So we have

Mantissa of given number = 0011 1101

So the number can be written as : 0.00111101 * 2^{13}

Now we need to align the mantissa towards left to get normalised number..And in the question it is mentioned that during alignment process 0's will be padded in the right side as a result of mantissa alignment to left..

So to get normalised number , we align to left 3 times , so new mantissa = 11101 000

So exponent will also decrease by 3 hence new exponent = 10

So normalised number = 1.11101000 * 2^{10}

So actual exponent = 10

Given excess 64 is used..So bias value = 64

So exponent field value = 74

And of course sign bit = 0 being a positive number.

Thus the final representation of number = 0 1001010 11101000

= 0100 1010 1110 1000

= $(4AE8)_{16}$

Hence D) should be the correct answer.

11 votes -- HABIB MOHAMMAD KHAN (76.8k points)

4.18.6 Floating Point Representation: GATE2017-2-12 top http://gateoverflow.in/118434

Selected Answer

In 32 bit (single precision) IEEE-754 format, binary number is represented as

S(1 bit) E(8 bit) M(23 bits) with implicit normalization and exponent is represented with Excess-127 code.

Here, Sign bit = 0 $\Rightarrow$ Number is positive.

Exponent bits = 01111100 = 124 $\Rightarrow$ E = 124 - 127 = -3 (Excess-127)

Mantissa bits = 11011010000000000000000 $\Rightarrow$ Number = 1.1101101 (Implicit normalization).

$\therefore$ Number = 1.1101101 * 2^{-3} = 0.0011101101 = 0.227 = 2.27 x 10^{-1}

$\therefore$ Answer should be C

6 votes -- Kantikumar (3.5k points)

4.19 Functional Completeness(4) top

4.19.1 Functional Completeness: GATE1989-4-iii top http://gateoverflow.in/87883

Provide short answers to the following questions:

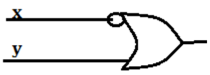
Show that {NOR} is a functionally complete set of Boolean operations.

gate1989 descriptive digital-logic functional-completeness

Answer

4.19.2 Functional Completeness: GATE1998_5 top http://gateoverflow.in/1696

a. The implication gate, shown below has two inputs $(x \text{ and } y)$; the output is 1 except when $x = 1 \text{ and } y = 0, \text{realize } f = \bar{x}y + x\bar{y}$ using only four implication gates.



b. Show that the implication gate is functionally complete.

gate1998 digital-logic functional-completeness descriptive

Answer

4.19.3 Functional Completeness: GATE1999-2.9 top http://gateoverflow.in/1487

Which of the following sets of component(s) is/are sufficient to implement any arbitrary Boolean function?

A. XOR gates, NOT gates
B. 2 to 1 multiplexers
C. AND gates, XOR gates
D. Three-input gates that output (A.B) + C for the inputs A, B and C.

gate1999 digital-logic normal functional-completeness

Answer

4.19.4 Functional Completeness: GATE2008-IT-1 top http://gateoverflow.in/3222

A set of Boolean connectives is functionally complete if all Boolean functions can be synthesized using those. Which of the following sets of connectives is NOT functionally complete?

A. EX-NOR
B. implication, negation
C. OR, negation
D. NAND

gate2008-it digital-logic easy functional-completeness

Answer

Answers: Functional Completeness

4.19.1 Functional Completeness: GATE1989-4-iii top http://gateoverflow.in/87883

Selected Answer

Functionally complete set is by which you can perform all operations . so if any logical set is able to implement the operation {And ., NOT} or {OR, NOT} ; it is known as functionally complete .

now come to NOR gate .

A(NOR)B= (A+B)'

A(NOR)A =(A+A)' =(A)' , so we can perform the NOT operation .

(A+B)' NOR (A+B)' =((A+B)' + (A+B)')' =((A+B)')' =(A+B) , so OR operation is also performed successfully .

so NOR is the functionally complete .

5 votes -- Amit Pal (3.5k points)

4.19.2 Functional Completeness: GATE1998_5 top http://gateoverflow.in/1696

implication gate is A->B which becomes A'+B

so let f(A,B)=A'+B

f(A,0)=A' (we get complement)

f(f(A,0),B)=f(A',B)=A+B (we get OR gate)

Thus it is functionally complete.

Let F(X,Y) =X'+Y

F(Y,X)=Y'+X

F(F(Y'+X),0)=X'Y

F(F(X,Y),X'Y)=XY'+XY' Therefore the above function is implemented with 4 implication gates.

3 votes -- Riya Roy(Arayana) (7.1k points)

4.19.3 Functional Completeness: GATE1999-2.9 top http://gateoverflow.in/1487

Selected Answer

1. XOR and NOT gates can only make XOR and XNOR which are not functionally complete- $a \oplus \bar{a} = 1, a \oplus a = 0.$

2. 2-1 multiplexer is functionally complete provided we have external 1 and 0 available. For NOT gate, use x as select line and use 0 and 1 as inputs. For AND gate, use y and 0 as inputs and x as select. With {AND, NOT} any other gate can be made.

3. XOR can be used to make a NOT gate ($a \oplus 1 = \bar{a}$) and {AND, NOT} is functionally complete. Again this requires external 1.

4. We have $AB + C$. Using $C = 1$, we get an AND gate. Using $B = 1$ we get an OR gate. But we cannot derive a NOT gate here.

So, options B and C are true provided external 1 and 0 are available.

11 votes -- Arjun Suresh (294k points)

4.19.4 Functional Completeness: GATE2008-IT-1 top http://gateoverflow.in/3222

Selected Answer

EX-NOR is not functionally complete. NOR and NAND are functionally complete logic gates, OR , AND, NOT any logic gate can be generated using them.

And (Implication, Negation) also

p->q = p'+q = apply negation (p+q')' = pq+p'q'= apply again negation =(pq)' + p'q' = (p'+q') + p'q' = p'+q' + p'q' = p'+q' = again apply negation = (p'+q')' = pq that's how we got AND logic gate.

13 votes -- Manu Thakur (6k points)

4.20 Gray Code(2) top

4.20.1 Gray Code: GATE2006-40 top http://gateoverflow.in/1816

Consider numbers represented in 4-bit Gray code. Let $h_3h_2h_1h_0$ be the Gray code representation of a number n and let $g_3g_2g_1g_0$ be the Gray code of $(n+1)(modulo 16)$ value of the number. Which one of the following functions is correct?

A. $g_0(h_3h_2h_1h_0) = \sum(1, 2, 3, 6, 10, 13, 14, 15)$
B. $g_1(h_3h_2h_1h_0) = \sum(4, 9, 10, 11, 12, 13, 14, 15)$
C. $g_2(h_3h_2h_1h_0) = \sum(2, 4, 5, 6, 7, 12, 13, 15)$
D. $g_3(h_3h_2h_1h_0) = \sum(0, 1, 6, 7, 10, 11, 12, 13)$

gate2006 digital-logic number-representation gray-code normal

Answer

4.20.2 Gray Code: TIFR2017-B-8 top http://gateoverflow.in/95703

For any natural number n, an ordering of all binary strings of length n is a Gray code if it starts with 0^n, and any successive strings in the ordering differ in exactly one bit (the first and last string must also differ by one bit). Thus, for $n = 3$, the ordering (000, 100, 101, 111, 110, 010, 011, 001) is a Gray code. Which of the following must be TRUE for all Gray codes over strings of length n?

A. the number of possible Gray codes is even
B. the number of possible Gray codes is odd
C. In any Gray code, if two strings are separated by k other strings in the ordering, then they must differ in exactly $k+1$ bits
D. In any Gray code, if two strings are separated by k other strings in the ordering, then they must differ in exactly k bits
E. none of the above

tifr2017 digital-logic binary-codes gray-code

Answer

Answers: Gray Code

4.20.1 Gray Code: GATE2006-40 top http://gateoverflow.in/1816

Selected Answer

answer is C

Decimal n	Binary n	H(x) = gray(n)	G(x) = gray[(n+1) mod16]
0	0000	0000 (00)	0001
1	0001	0001 (01)	0011
2	0010	0011 (03)	0010
3	0011	0010 (02)	0110
4	0100	0110 (06)	0111
5	0101	0111 (07)	0101
6	0110	0101 (05)	0100
7	0111	0100 (04)	1100
8	1000	1100 (12)	1101
9	1001	1101 (13)	1111
10	1010	1111 (15)	1110
11	1011	1110 (14)	1010
12	1100	1010 (10)	1011
13	1101	1011 (11)	1001
14	1110	1001 (09)	1000
15	1111	1000 (08)	0000

We need to map min terms of $g_3g_2g_1g_0$ w.r.t $h_3h_2h_1h_0$.

Hence as highlighted g_2 matches with option C

Edit :
we have to map h(x) with g(x)...mod 16 is used in g(x) only because since we have 4 bits ,mamximum possible no that can be represented is 15..so after 15 we shouldn't get 16 and go back to 0.. thats why..
now mapping is simple...we just have to map such that **h(x)---->g(x+1)**
means if **h represents gray code of 0 then g will represent gray code of 1**
if **h represents gray code of 1 then g will represent for 2** and so on....
for last number **h(15)** ,mod 16 actually comes into picture which will make it to represent as **g(0)**
so draw table as mentioned above...
now write g as a function of f ..simply how we do minimisation...see the min terms..
be careful only in one thing here...
example... for **2**..gray code representation is **0011 meaning 3 in decimal**..so if **we select this row as a min term**(just an example) then **we have selected 3 and not 2** ..**means row numbers are not representing min terms**...rest everything is fine!

20 votes -- ryan sequeira (3k points)

4.20.2 Gray Code: TIFR2017-B-8 top http://gateoverflow.in/95703

Selected Answer

1). In the question it is stated that -> Thus, for n=3, the ordering (000, 100, 101, 111, 110, 010, 011, 001) is a Gray code.

2). We have to find orderings such that they start with 0^n , must contain all bit strings of length n and successive strings must differ in one bit.

Option c&d are clearly wrong.
Now, consider n=1. The only Gray code possible is {0,1}. Hence no of Gray code = odd for n=1.
For n=2 only two Gray code exists {00, 10, 11, 01} and {00, 01, 11, 10}. Thus no of Gray code = even for n=2.
Thus it is not that gray codes could be only even or only odd.
Hence option e is correct.

2 votes -- tarun_svbk (1k points)

4.21 Half Adder(2) top

4.21.1 Half Adder: GATE1993-9 top http://gateoverflow.in/2306

Assume that only half adders are available in your laboratory. Show that any binary function can be implemented using half adders only.

gate1993 digital-logic half-adder

Answer

4.21.2 Half Adder: GATE2015-2_48 top

http://gateoverflow.in/8250

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit-ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _______.

gate2015-2 digital-logic half-adder normal numerical-answers

Answer

Answers: Half Adder

4.21.1 Half Adder: GATE1993-9 top

http://gateoverflow.in/2306

Selected Answer

Half Adder give two output

$S = A \oplus B$

$C = A.B$

We can Perform any operation using Half adder if we can implement basic gates using half adder

AND operation $C = AB$

Not operation = S (with A and 1) = $A \oplus 1 = A'.1 + A.1' = A'$

OR operation = $((A \oplus 1).(B \oplus 1)) \oplus 1 = (A'.B')' = A+B$

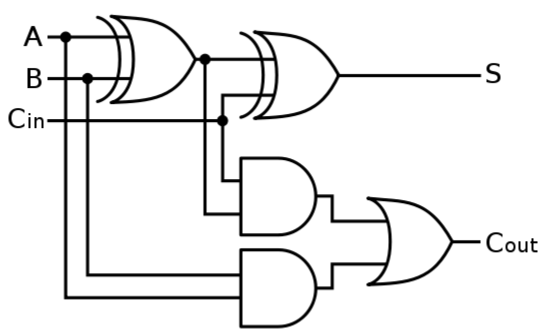
8 votes

-- Praveen Saini (53.6k points)

4.21.2 Half Adder: GATE2015-2_48 top

http://gateoverflow.in/8250

Selected Answer



S1 should wait for C1 to be ready. Delay for generating C is 1 EXOR + 1 AND + 1 OR = 2.4 + 1.2 + 1.2 = 4.8 μs

Delay for sum is XOR + XOR = 2.4 + 2.4 = 4.8 μs

But for the second adder, there the first EXOR can be done even before waiting for the previous output. So, we can get the sum in another 2.4 μs and carry in another 2.4 μs. In this way, 4-bit sum can be obtained after

4.8 μs + 3 * 2.4 μs = 12 μs.

But the question says we use ripple-carry adder. So, each adder must wait for the full output from the previous adder. This would make the total delay = 4 * 4.8 = 19.2 μs and this is the key given by GATE, so obviously they meant this.

Ref: http://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Comb/adder.html

32 votes -- Arjun Suresh (294k points)

Ans is 12 ns

It took me a while but here's how it is :

The first carry and sum will be available after 4.8 ns. This should be straight forward.

However, for the subsequent stages, you need to keep in mind that the output of half adders is already there at 2.4 ns. So in a sense, it is already computed. The remaining half adder for each full adder is just waiting for the previous carry, which when available from the previous stage can be processed in 2.4 ns. So each next stage will take only 2.4 ns each.

The catch here is that half of the output in each next stage is already computed, only half needs to be processed.

11 votes -- Vikrant Singh (13.4k points)

4.22 Hamming Code(1) top

4.22.1 Hamming Code: GATE2017-2-34 top http://gateoverflow.in/118376

Consider the binary code that consists of only four valid codewords as given below:

00000, 01011, 10101, 11110

Let the minimum Hamming distance of the code p and the maximum number of erroneous bits that can be corrected by the code be q. Then the values of p and q are

A. $p = 3$ and $q = 1$
B. $p = 3$ and $q = 2$
C. $p = 4$ and $q = 1$
D. $p = 4$ and $q = 2$

gate2017-2 digital-logic hamming-code

Answer

Answers: Hamming Code

4.22.1 Hamming Code: GATE2017-2-34 top http://gateoverflow.in/118376

Selected Answer

00000**(code1)**,01011**(code2)**,10101**(code3)**,11110**(code4)**

Haming distance = min of all hamming distances.

which is 3 b/w **(code1) and (code2) so p = 3**

Now to correct d bit error we need hamming distance = 2d+1

so 2d+1 = 3 will gives d= 1.

A is answer

11 votes -- Prashant Singh (49.2k points)

4.23 Ieee Representation(3) top

4.23.1 Ieee Representation: GATE2008-4 top http://gateoverflow.in/402

In the IEEE floating point representation the hexadecimal value $0x00000000$ corresponds to

A. The normalized value 2^{-127}
B. The normalized value 2^{-126}
C. The normalized value $+0$
D. The special value $+0$

gate2008 digital-logic floating-point-representation ieee-representation easy

Answer

4.23.2 Ieee Representation: GATE2008-IT-7 top http://gateoverflow.in/3267

The following bit pattern represents a floating point number in IEEE 754 single precision format

1 10000011 101000000000000000000000

The value of the number in decimal form is

A. -10
B. -13
C. -26
D. None of the above

gate2008-it digital-logic number-representation floating-point-representation ieee-representation normal

Answer

4.23.3 Ieee Representation: GATE2012-7 top http://gateoverflow.in/39

The decimal value 0.5 in IEEE single precision floating point representation has

A. fraction bits of $000 \dots 000$ and exponent value of 0
B. fraction bits of $000 \dots 000$ and exponent value of -1
C. fraction bits of $100 \dots 000$ and exponent value of 0
D. no exact representation

gate2012 digital-logic normal number-representation ieee-representation

Answer

Answers: Ieee Representation

4.23.1 Ieee Representation: GATE2008-4 top http://gateoverflow.in/402

Selected Answer

S	BE	M	Value
0/1	All 0's	All 0's	0
0	All 1's	All 0's	+∞
1	All 1's	All 0's	-∞
0/1	All 1's	Non zero	NaN

answer = **option D**

13 votes -- Amar Vashishth (28.7k points)

4.23.2 Ieee Representation: GATE2008-IT-7 top

http://gateoverflow.in/3267

Selected Answer

Sign bit is 1 -> number is negative

Exponent bits- 10000011

Exponent is added with 127 bias in IEEE single precision format. So, Actual exponent = 10000011 - 127 = 131 - 127 = 4

Mantissa bits- 10100000000000000000000

In IEEE format, an implied 1 is before mantissa, and hence the actual number is

$-1.101 * 2^4$

$=- (11010)_2 = - 26$

http://steve.hollasch.net/cgindex/coding/ieeefloat.html

19 votes -- Arjun Suresh (294k points)

4.23.3 Ieee Representation: GATE2012-7 top

http://gateoverflow.in/39

Selected Answer

(B) is the answer. In IEEE uses normalized representation and hence an implicit '1' is used before the decimal point. So, if mantissa is

0000..0

it would be treated as

1.000..0

and hence the exponent need to be -1 for us to get 0.1 which is the binary representation of 0.5.

More into IEEE floating point representation:
http://steve.hollasch.net/cgindex/coding/ieeefloat.html

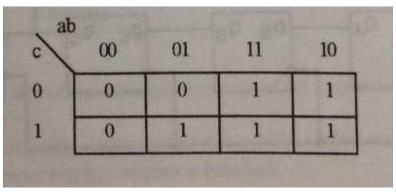
15 votes -- gatecse (13.4k points)

4.24 K Map(16) top

4.24.1 K Map: GATE1987-16a top

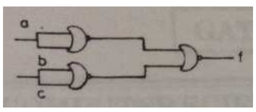
http://gateoverflow.in/82698

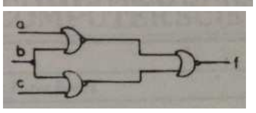
A Boolean function f is to be realized only by NOR gates. Its K-map is given below:

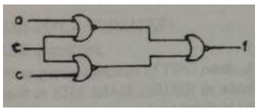


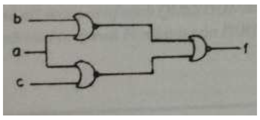
c \ ab	00	01	11	10
0	0	0	1	1
1	0	1	1	1

The realization is

A. 

B. 

C. 

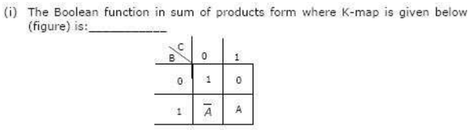
D. 

gate1987 digital-logic k-map

Answer

4.24.2 K Map: GATE1992_01,i top http://gateoverflow.in/545

The Boolean function in sum of products form where K-map is given below (figure) is ________



(i) The Boolean function in sum of products form where K-map is given below (figure) is:__________

B \ C	0	1
0	1	0
1	$\overline{A}$	A

gate1992 digital-logic k-map normal

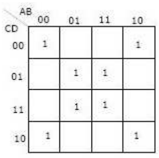
Answer

4.24.3 K Map: GATE1995_15 top http://gateoverflow.in/2651

a. Implement a circuit having the following output expression using an inverter and a nand gate

$$Z = \overline{A} + \overline{B} + C$$

b. What is the equivalent minimal Boolean expression (in sum of products form) for the Karnaugh map given below?



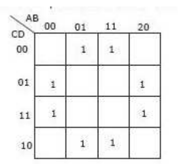
CD \ AB	00	01	11	10
00	1			1
01		1	1	
11		1	1	
10	1			1

gate1995 digital-logic k-map normal

Answer

4.24.4 K Map: GATE1996_2.24 top http://gateoverflow.in/2753

What is the equivalent Boolean expression in product-of-sums form for the Karnaugh map given in Fig



CD \ AB	00	01	11	20
00		1	1	
01	1			1
11	1			1
10		1	1	

A. $B\overline{D} + \overline{B}D$

B. $(B + \overline{C} + D)(\overline{B} + C + \overline{D})$

C. $(B + D)(\overline{B} + \overline{D})$

D. $(B + \overline{D})(\overline{B} + D)$

gate1996 digital-logic k-map easy

Answer

4.24.5 K Map: GATE1998_2.7 top http://gateoverflow.in/1679

The function represented by the Karnaugh map is given below is

A \ BC	00	01	10	11
0	1	1	0	1
1	1	0	0	1

A. $A.B$
B. $AB + BC + CA$
C. $\overline{B \oplus C}$
D. $A.BC$

gate1998 digital-logic k-map normal

Answer

4.24.6 K Map: GATE1999_1.8 top http://gateoverflow.in/1461

Which of the following functions implements the Karnaugh map shown below?

CD **AB**	**00**	**01**	**11**	**10**
00	0	0	1	0
01	X	X	1	X
11	0	1	1	0
10	0	1	1	0

A. $\bar{A}B + CD$
B. $D(C + A)$
C. $AD + \bar{A}B$
D. $(C + D)(\bar{C} + D) + (A + B)$

gate1999 digital-logic k-map easy

Answer

4.24.7 K Map: GATE2000-2.11 top http://gateoverflow.in/658

Which functions does NOT implement the Karnaugh map given below?

wz → xy↓	00	01	11	10
00	0	×	0	0
01	0	×	1	1
11	1	1	1	1
10	0	×	0	0

A. $(w + x)y$
B. $xy + yw$
C. $(w + x)(\bar{w} + y)(\bar{x} + y)$
D. None of the above

gate2000 digital-logic k-map normal

Answer

4.24.8 K Map: GATE2001-1.11 top http://gateoverflow.in/704

Given the following karnaugh map, which one of the following represents the minimal Sum-Of-Products of the map?

yz \ wx	00	01	11	10
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

A. $XY + Y'Z$
B. $WX'Y' + XY + XZ$
C. $W'X + Y'Z + XY$
D. $XZ + Y$

gate2001 k-map digital-logic normal

Answer

4.24.9 K Map: GATE2002-1.12 top http://gateoverflow.in/816

Minimum sum of product expression for f(w,x,y,z) shown in Karnaugh-map below

yz \ wx	00	01	11	10
00	0	1	1	0
01	x	0	0	1
11	x	0	0	1
10	0	1	1	x

A. xz + y'z
B. xz' + zx'
C. x'y + zx'
D. None of the above

gate2002 digital-logic k-map normal

Answer

4.24.10 K Map: GATE2003-45 top http://gateoverflow.in/936

The literal count of a Boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of $(xy + xz')$ is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following Karnaugh map? Here, X denotes "don't care"

xy \ zw	00	01	11	10
00	X	1	0	1
01	0	1	X	0
11	1	X	X	0
10	X	0	0	X

A. (11, 9)
B. (9, 13)
C. (9, 10)
D. (11,11)

gate2003 digital-logic k-map normal

Answer

4.24.11 K Map: GATE2006-IT-35 top http://gateoverflow.in/3574

The boolean function for a combinational circuit with four inputs is represented by the following Karnaugh map.

RS \ PQ	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	1	1	1	0
10	1	0	0	1

Which of the product terms given below is an essential prime implicant of the function?

A. QRS
B. PQS
C. PQ'S'
D. Q'S'

gate2006-it digital-logic k-map normal

Answer

4.24.12 K Map: GATE2007-IT-78 top http://gateoverflow.in/3530

Consider the following expression

$a\bar{d} + \bar{a}\bar{c} + b\bar{c}d$

Which of the following Karnaugh Maps correctly represents the expression?

A.

	c'd'	**c'd**	**cd**	**cd'**
a'b'	X	X		
a'b	X	X		
ab	X	X		X
ab'	X			X

B.

	c'd'	**c'd**	**cd**	**cd'**
a'b'	X	X		
a'b	X			
ab	X	X		X
ab'	X	X		X

C.

	c'd'	**c'd**	**cd**	**cd'**
a'b'	X	X		
a'b	X	X		X
ab	X	X		X
ab'	X			X

D.

	c'd'	**c'd**	**cd**	**cd'**
a'b'	X	X		
a'b	X	X		X
ab	X	X		X
ab'	X		X	X

gate2007-it digital-logic k-map normal

Answer

4.24.13 K Map: GATE2007-IT-79 top http://gateoverflow.in/3531

Consider the following expression

$a\bar{d} + \bar{a}\bar{c} + b\bar{c}d$

Which of the following expressions does not correspond to the Karnaugh Map obtained for the given expression?

A. $\bar{c}\bar{d} + a\bar{d} + ab\bar{c} + \bar{a}\bar{c}d$
B. $\bar{a}\bar{c} + \bar{c}\bar{d} + a\bar{d} + ab\bar{c}d$
C. $\bar{a}\bar{c} + a\bar{d} + ab\bar{c} + \bar{c}d$

D. $\bar{b}\bar{c}\bar{d} + ac\bar{d} + \bar{a}\bar{c} + ab\bar{c}$

gate2007-it digital-logic k-map normal

Answer

4.24.14 K Map: GATE2008-5 top

http://gateoverflow.in/403

In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

cd \ ab	00	01	11	10
00	1	1		1
01	X			
11	X			
10	1	1		X

A. $\bar{b}.\bar{d} + \bar{a}.\bar{d}$

B. $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.b.\bar{d}$

C. $\bar{b}.\bar{d} + \bar{a}.b.\bar{d}$

D. $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{d}$

gate2008 digital-logic k-map easy

Answer

4.24.15 K Map: GATE2012_30 top

http://gateoverflow.in/1615

What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term

cd \ ab	00	01	11	10
00	1	X	X	1
01	X			1
11				
10	1			X

(A) $\bar{b}\bar{d}$
(B) $\bar{b}\bar{d} + \bar{b}\bar{c}$
(C) $\bar{b}\bar{d} + a\bar{b}\bar{c}d$
(D) $\bar{b}\bar{d} + \bar{b}\bar{c} + \bar{c}\bar{d}$

gate2012 digital-logic k-map easy

Answer

4.24.16 K Map: GATE2017-1-21 top

http://gateoverflow.in/118301

Consider the Karnaugh map given below, where X represents *"don't care"* and blank represents 0.

dc \ ba	00	01	11	10
00		x	x	
01	1			x
11	1			1
10		x	x	

Assume for all inputs (a, b, c, d), the respective complements $(\bar{a}, \bar{b}, \bar{c}, \bar{d})$ are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is ____________ .

gate2017-1 digital-logic k-map numerical-answers normal

Answer

Answers: K Map

4.24.1 K Map: GATE1987-16a top http://gateoverflow.in/82698

Selected Answer

A. can't be ans.

ans wants without solving ??

Two Max Terms are:

(a+b)(a+c) so "a" is common here only possibility is option D.

Kmap will give min terms = a[4 1's circle] + bc[2 1's box]

Option D ckt will give = (a+b) (b+c) = a+bc

D will be answer

7 votes -- papesh (24.1k points)

4.24.2 K Map: GATE1992_01,i top http://gateoverflow.in/545

Selected Answer

answer - ABC + B'C' + A'C' [EDIT]

expand this K map of 2 variables (4 cells) to K map of three variable (8 cells)

entries which are non zero are A'B'C', AB'C', A'BC' and ABC

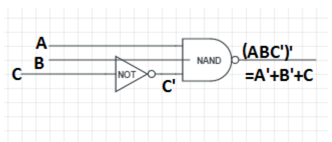
minimize SOP expression using that K map

7 votes -- ankitrokdeonsns (9.1k points)

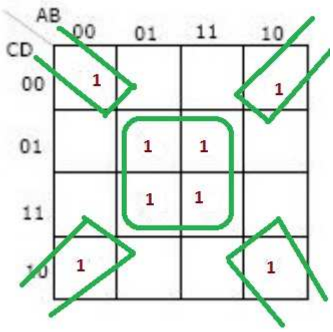
4.24.3 K Map: GATE1995_15 top http://gateoverflow.in/2651

Selected Answer

(a)



(B)



$BD + \bar{B}\bar{D}$ = $\overline{(B \bigoplus D)}$ = $B \bigodot D$

3 votes -- Leen Sharma (32.3k points)

4.24.4 K Map: GATE1996_2.24 top

http://gateoverflow.in/2753

Selected Answer

If all the empty cells are filled with '0' and then the POS expression is calculated as:

CD\AB	00	01	11	10
00	0			0
01		0	0	
11		0	0	
10	0			0

Then the POS expression of f = (D+B)(D'+B') = BD' + B'D

9 votes -- Ujjwal Saini (527 points)

4.24.5 K Map: GATE1998_2.7 top

http://gateoverflow.in/1679

Selected Answer

Here we cant make pair of 4 so we have to go with pair of 2 each

BC + B'C'

B (EX-NOR) C

it can be represented as negation of EX -OR

[B (EX-OR) C]'

Option C is correct .

5 votes -- shekhar chauhan (42.9k points)

4.24.6 K Map: GATE1999_1.8 top

http://gateoverflow.in/1461

Selected Answer

answer - B

CD+AD

6 votes -- ankitrokdeonsns (9.1k points)

4.24.7 K Map: GATE2000-2.11 top

http://gateoverflow.in/658

Selected Answer

answer - D

solving K map gives xy +wy

13 votes -- ankitrokdeonsns (9.1k points)

4.24.8 K Map: GATE2001-1.11 top

http://gateoverflow.in/704

Selected Answer

yz \ wx	00	01	11	10
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

answer

2 votes -- Priya Sukumaran (115 points)

answer - A

11 votes -- ankitrokdeonsns (9.1k points)

4.24.9 K Map: GATE2002-1.12 top

http://gateoverflow.in/816

Selected Answer

m1,m3,m9,m11 form one quad xz'

m4,m6,m12,m14 form one quad x'z

So f=x'z+z'x

Ans is b

9 votes -- Pooja Palod (32.4k points)

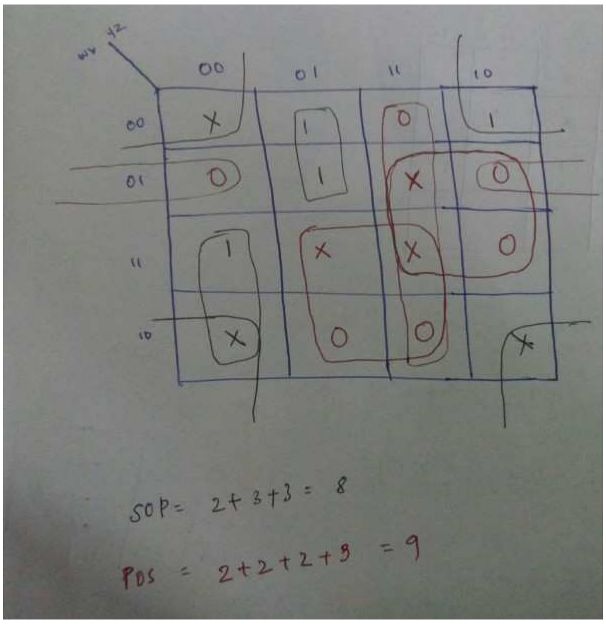
4.24.10 K Map: GATE2003-45 top

http://gateoverflow.in/936

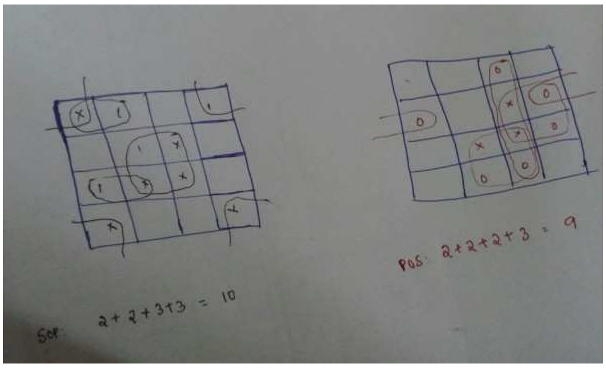
Selected Answer

We will be getting two different grouping..

Grouping 1 (9,8)



GROUPING 2 (9,10)



Both the grouping are correct representation of the function . f(xyzw)

(PS: There were statements decribing dont cares in many of the comments

""once you have assumed a don't care as '1' u can't use the same don't care for grouping zeros and vice versa"

" if dont care has been used in pos than can't be used in sop "

Both these statements are wrong . Don't care simply means just Dont care , say we use dont care d3 for grouping 1 in SOP we can use d3 for grouping 0 in POS. the literals in SOP and POS May not be same)

K Map- is not unique . And the question says about minimal literals . So the **best answer would be (9,8)** Since there is no option in GATE we can go with (9,10)

16 votes -- pC (21.4k points)

4.24.11 K Map: GATE2006-IT-35 top

http://gateoverflow.in/3574

Selected Answer

essential prime implicants which r grouped only by only one method or way

so in above question cornor's ones r grouped by only one method

d) will be the answer

8 votes -- SAKET NANDAN (4k points)

4.24.12 K Map: GATE2007-IT-78 top

http://gateoverflow.in/3530

ans.. (a)

3 votes -- Vicky Bajoria (4.9k points)

4.24.13 K Map: GATE2007-IT-79 top

http://gateoverflow.in/3531

Selected Answer

ad' [fill minterm in K-map in front for a and d']

	c'd'	c'd	cd	cd'
a'b'				
a'b				
ab	1			1
ab'	1			1

similarly fill all minterms for ad'+a'c' +bc'd , resulting K-map will be

	c'd'	c'd	cd	cd'
a'b'	1	1		
a'b	1	1		
ab	1	1		1
ab'	1			1

option a) c'd'+ ad' + abc' + a'c'd

	c'd'	c'd	cd	cd'
a'b'	1	1		
a'b	1	1		
ab	1	1		1
ab'	1			1

is equivalent to given expression

option b) a'c' + c'd' + ad' + abc'd

	c'd'	c'd	cd	cd'
a'b'	1	1		
a'b	1	1		
ab	1	1		1
ab'	1			1

is equivalent to given expression.

option c) a'c' + ad' + abc' + c'd

	c'd'	c'd	cd	cd'
a'b'	1	1		
a'b	1	1		
ab	1	1		1
ab'	1	1		1

is not equivalent to given expression.

option d) b'c'd' + acd' + a'c' + abc'

	c'd'	c'd	cd	cd'
a'b'	1	1		
a'b	1	1		
ab	1	1		1
ab'	1			1

is equivalent to given expression.

So, answer is C.

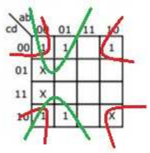
14 votes -- Praveen Saini (53.6k points)

4.24.14 K Map: GATE2008-5 top

http://gateoverflow.in/403

Selected Answer

2 Quads are getting formed



Value for First one is a'd' and value for 2nd one is b'd'.

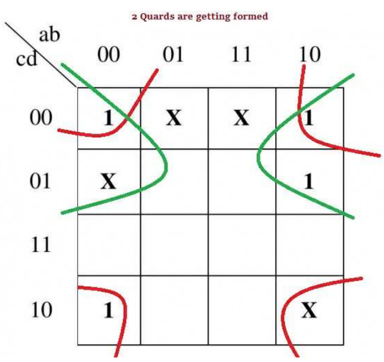
Ans is Option A

10 votes -- GATE_2016 (447 points)

4.24.15 K Map: GATE2012_30 top

http://gateoverflow.in/1615

Selected Answer



2 quads are getting formed.

Value for First one is b'd' and value for 2nd one is b'c'.So,**Ans is option B**

14 votes -- GATE_2016 (447 points)

4.24.16 K Map: GATE2017-1-21 top http://gateoverflow.in/118301

Selected Answer

From K-map simplification we get the min-term as CA' . So We can simplyfy it for NOR gate expression

i.e. C' **NOR** A = (C'+A)' = CA'
Now complemented inputs are also given to us so for 2 input NOR gate **we need only 1 NOR gate.**

1 is correct answer

13 votes -- Aboveallplayer (18.5k points)

4.25 Logic Gates(5) top

4.25.1 Logic Gates: GATE1992-02,ii top http://gateoverflow.in/556

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

(ii) All digital circuits can be realized using only

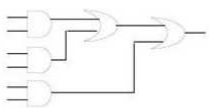
a. Ex-OR gates
b. Multiplexers
c. Half adders
d. OR gates

gate1992 normal digital-logic logic-gates

Answer

4.25.2 Logic Gates: GATE2002-7 top http://gateoverflow.in/860

a. Express the function $f(x, y, z) = xy' + yz'$ with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.
b. Transform the following logic circuit (without expressing its switching function) into an equivalent logic circuit that employs only 6 NAND gates each with 2-inputs.

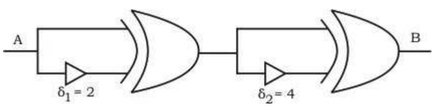


gate2002 digital-logic normal descriptive logic-gates

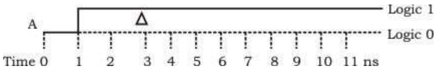
Answer

4.25.3 Logic Gates: GATE2003-47 top http://gateoverflow.in/29098

Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays $\delta_1 = 2ns$ and $\delta_2 = 4ns$ as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?



A. 1
B. 2
C. 3
D. 4

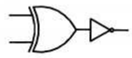
gate2003 digital-logic logic-gates digital-circuits

Answer

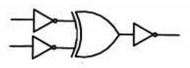
4.25.4 Logic Gates: GATE2011-13 top http://gateoverflow.in/2115

Which one of the following circuits is **NOT** equivalent to a 2-input XNOR (exclusive NOR) gate?

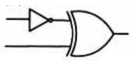
(A)



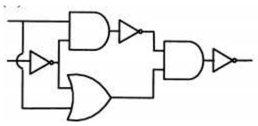
(B)



(C)



(D)



gate2011 digital-logic normal logic-gates

Answer

4.25.5 Logic Gates: TIFR2015-A-4 top http://gateoverflow.in/29162

The Boolean function obtained by adding an inverter to each and every input of an AND gate is:

a. OR
b. XOR
c. $NAND$
d. NOR
e. None of the above.

tifr2015 digital-logic logic-gates

Answer

Answers: Logic Gates

4.25.1 Logic Gates: GATE1992-02,ii top http://gateoverflow.in/556

Selected Answer

Answer: B, C

NOR gate, NAND gate, Multiplexers and Half adders can also be used to realise all digital circuits.

5 votes -- Rajarshi Sarkar (35k points)

4.25.2 Logic Gates: GATE2002-7 top http://gateoverflow.in/860

Selected Answer

$f(x, y, z) = xy' + yz' = xy'z' + xy'z + x'yz' + xyz'$

$f(x, y, z) = \sum_m (2, 4, 5, 6)$

K-map

	$y'z'$	$y'z$	yz	yz'
x'	0	0	0	1
x	1	1	0	1

By pairing of $1's$, we get two pairs $(2, 6), (4, 5)$ resulting in same expression $F = xy' + yz'$

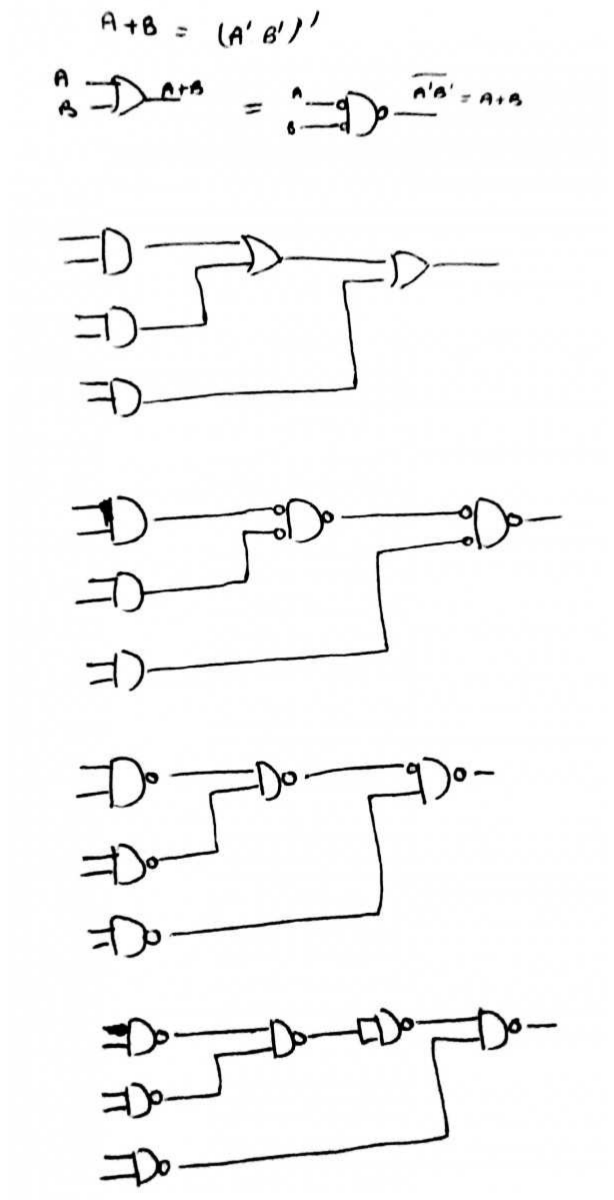
But by pairing of $0's$, we get two pairs $(0, 1), (2, 7)$, we get $F' = yz + x'y'$

Take complement, $F = \overline{(yz)}.(x + y)$

so we can implement the function with 1 NOT , 1 OR and 2 AND gates.

For the second part , we need to implement given circuit using NANDs only.

so best way is to replace OR with Invert NAND, $A + B = \overline{(A'B')}$



9 votes -- Praveen Saini (53.6k points)

4.25.3 Logic Gates: GATE2003-47 top http://gateoverflow.in/29098

Selected Answer

Let output first xor gate is P .

on completion of:-	o/p of P	o/p of B
0th sec	0	0
1st sec	1xor0=1	1xor0=1

This status will same for two seconds.After o/p of first non-inverting buffer reach at i/p of first xor gate then,

3rd sec	1xor1=0	0xor0=0

This status will same for two seconds more. So, at 5th sec o/p of second non-inverting buffer reach at i/p of second xor gate because of its delay of 4sec i.e 1.

5th sec	1xor1=0	0xor1=1

At 7th sec o/p of p which was changed at 3rd sec reach at i/p second xor gate.

7th sec	1xor1=0	0xor0=0

Now this status same for 3 seconds more. So total 4 logic level changes at 1st,3rd,5th and 7th sec.
So option is d

4 votes -- Avdhesh Singh Rana (2.3k points)

4.25.4 Logic Gates: GATE2011-13 top http://gateoverflow.in/2115

Selected Answer

A) $(AB' + A'B)' = A \odot B$

B) $(A'(B')' + (A')'B')' = (A \oplus B)' = A \odot B$

C) $A'B' + (A')'B = A \odot B$

D) $((AB')(A+B'))' = ((A'+B)(A+B'))' = (A'B' + AB)' = A \oplus B$

So, Ans D)

5 votes -- srestha (58.4k points)

4.25.5 Logic Gates: TIFR2015-A-4 top http://gateoverflow.in/29162

Selected Answer

Invert-AND = NOR

for example,
$A'B' = \overline{A+B}$

[Note : Invert-OR = NAND ,
$A' + B' = \overline{A.B}$]

7 votes -- Praveen Saini (53.6k points)

4.26 Memory Interfacing(1) top

4.26.1 Memory Interfacing: GATE1995_2.2 top http://gateoverflow.in/2614

The capacity of a memory unit is defined by the number of words multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 4K $\times$ 16?

A. 10 address, 16 data lines
B. 11 address, 8 data lines
C. 12 address, 16 data lines
D. 12 address, 12 data lines

gate1995 digital-logic memory-interfacing normal

Answer

Answers: Memory Interfacing

4.26.1 Memory Interfacing: GATE1995_2.2 top http://gateoverflow.in/2614

Selected Answer

ROM memory size $=2^m$ x n

m=no. of address lines n= no. of data lines

given 4K x 16

$= 2^2 \times 2^{10} \times 16$

$= 2^{12} \times 16$

address lines =12

data lines= 16

7 votes -- Sanket_ (4k points)

4.27 Min No Gates(4) top

4.27.1 Min No Gates: GATE2000-9 top http://gateoverflow.in/680

Design a logic circuit to convert a single digit BCD number to the number modulo six as follows (Do not detect illegal input):

a. Write the truth table for all bits. Label the input bits I_1, I_2, ... with I_1 as the least significant bit. Label the output bits R_1, R_2.... with R_1 as the least significant bit. Use 1 to signify truth.
b. Draw one circuit for each output bit using, ***altogether***, two two-input AND gates, one two-input OR gate and two NOT gates.

gate2000 digital-logic min-no-gates descriptive

Answer

4.27.2 Min No Gates: GATE2004-58 top http://gateoverflow.in/1053

A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, …, 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit $\geq$ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

A. 2
B. 3
C. 4
D. 5

gate2004 digital-logic normal min-no-gates

Answer

4.27.3 Min No Gates: GATE2004-IT-8 top http://gateoverflow.in/3649

What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?

A. 2
B. 4
C. 5
D. 6

gate2004-it digital-logic min-no-gates normal

Answer

4.27.4 Min No Gates: GATE2009-6 top http://gateoverflow.in/1298

What is the minimum number of gates required to implement the Boolean function (AB+C) if we have to use only 2-input NOR gates?

A. 2
B. 3
C. 4
D. 5

gate2009 digital-logic min-no-gates normal

Answer

Answers: Min No Gates

4.27.1 Min No Gates: GATE2000-9 top http://gateoverflow.in/680

Selected Answer

A	B	C	D		Y3	Y2	Y1	Y0	
0	0	0	0	**0**	0	0	0	0	
0	0	0	1	**1**	0	0	0	1	
0	0	1	0	**2**	0	0	1	0	
0	0	1	1	**3**	0	0	1	1	
0	1	0	0	**4**	0	1	0	0	
0	1	0	1	**5**	0	1	0	1	
0	1	1	0	**6**	0	0	0	0	
0	1	1	1	**7**	0	0	0	1	
1	0	0	0	**8**	0	0	1	0	
1	0	0	1	**9**	0	0	1	1	

Y3=0

Y2=A'BC'

Y1=A'B'C+AB'C'

Y0=A'D+B'C'D

0 votes -- Savir husen khan (323 points)

4.27.2 Min No Gates: GATE2004-58 top http://gateoverflow.in/1053

Selected Answer

Answer should be (B) As according to question .. truth table will be like

A B C D f

0 0 0 0 0

0 0 0 1 0

0 0 1 0 0

0 0 1 1 0

0 1 0 0 0

0 1 0 1 1

0 1 1 0 1

0 1 1 1 1

1 0 0 0 1

1 0 0 1 1

1 0 1 0 dont care

1 0 1 1 dont care

1 1 0 0 dont care

1 1 0 1 dont care

1 1 1 0 dont care

1 1 1 1 dont care

using this truth table we get 3 sub cube which are combined with following minterms A (8,9,10,11,12,13,14,15) , BD(5,13,7,15) and BC(6,7,14,15)

SO f = A+ BD +BC= A+ B(C+D)

SO minimum gate required 2 OR gate and 1 AND gate = 3 minimum gate ...

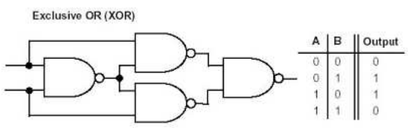
16 votes -- sonam vyas (13.2k points)

4.27.3 Min No Gates: GATE2004-IT-8 top

http://gateoverflow.in/3649

Selected Answer

Option B 4. See the diagram.



3 votes -- Manu Madhavan (1.2k points)

4.27.4 Min No Gates: GATE2009-6 top

http://gateoverflow.in/1298

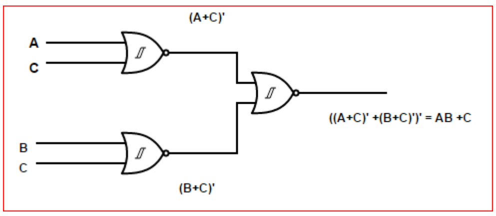
Selected Answer

given boolean function is

f = AB + C

= (A+C) . (B +C)

=((A+C)' +(B+C)')'



therefore 3 NOR gate required .

28 votes -- Mithlesh Upadhyay (5.4k points)

4.28 Min Product Of Sums(1) top

4.28.1 Min Product Of Sums: GATE2017-2-28 top http://gateoverflow.in/118370

Given $f(w, x, y, z) = \Sigma_m(0, 1, 2, 3, 7, 8, 10) + \Sigma_d(5, 6, 11, 15)$; where d represents the '*don't-care*' condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of $f(w, x, y, z)$?

A. $f = (\bar{w} + \bar{z})(\bar{x} + z)$
B. $f = (\bar{w} + z)(x + z)$
C. $f = (w + z)(\bar{x} + z)$
D. $f = (w + \bar{z})(\bar{x} + z)$

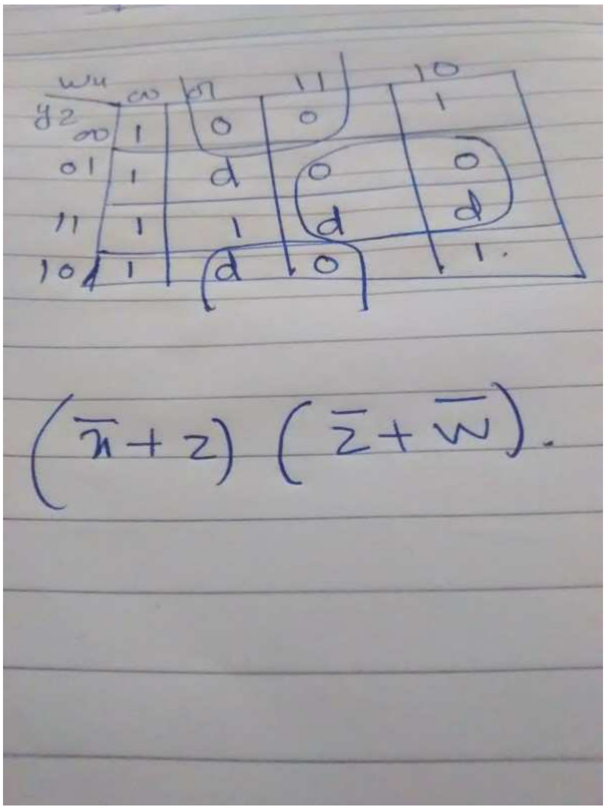
gate2017-2 digital-logic min-product-of-sums

Answer

Answers: Min Product Of Sums

4.28.1 Min Product Of Sums: GATE2017-2-28 top http://gateoverflow.in/118370

Selected Answer



I am not quite sure..please do correct me if I m wrong

11 votes -- Joker (1.5k points)

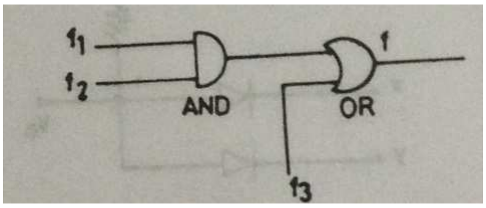
4.29 Min Sum Of Products Form(11) top

4.29.1 Min Sum Of Products Form: GATE1988-2v top http://gateoverflow.in/91685

Three switching functions f_1, f_2 and f_3 are expressed below as sum of minterms.

- $f_1(w, x, y, z) = \sum 0, 1, 2, 3, 5, 12$
- $f_2(w, x, y, z) = \sum 0, 1, 2, 10, 13, 14, 15$
- $f_3(w, x, y, z) = \sum 2, 4, 5, 8$

Express the function f realised by the circuit shown in the below figure as the sum of minterms (in decimal notation).



gate1988 descriptive digital-logic easy circuit-output min-sum-of-products-form

Answer

4.29.2 Min Sum Of Products Form: GATE1991-5,b top http://gateoverflow.in/26437

Find the minimum sum of products form of the logic function $f(A, B, C, D) = \Sigma m(0, 2, 8, 10, 15) + \Sigma d(3, 11, 12, 14)$ where m and d represent minterm and don't care term respectively.

gate1991 digital-logic min-sum-of-products-form

Answer

4.29.3 Min Sum Of Products Form: GATE1997_71 top http://gateoverflow.in/19701

Let $f = (\bar{w} + y)(\bar{x} + y)(w + \bar{x} + z)(\bar{w} + z)(\bar{x} + z)$

a. Express f as the minimal sum of products. Write only the answer.

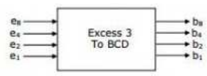
b. If the output line is stuck at 0, for how many input combinations will the value of f be correct?

gate1997 digital-logic min-sum-of-products-form

Answer

4.29.4 Min Sum Of Products Form: GATE2001-10 top http://gateoverflow.in/751

a. Is the 3-variable function $f = \Sigma(0, 1, 2, 4)$ its self-dual? Justify your answer.
b. Give a minimal product-of-sum form of the b output of the following excess-3 to BCD converter.



gate2001 digital-logic normal descriptive min-sum-of-products-form

Answer

4.29.5 Min Sum Of Products Form: GATE2005-18 top http://gateoverflow.in/1354

The switching expression corresponding to $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$ is:

A. $BC'D' + A'C'D + AB'D$

B. $ABC' + ACD + B'C'D$

C. $ACD' + A'BC' + AC'D'$

D. $A'BD + ACD' + BCD'$

gate2005 digital-logic normal min-sum-of-products-form

Answer

4.29.6 Min Sum Of Products Form: GATE2007-9 top http://gateoverflow.in/1207

Consider the following Boolean function of four variables:

$$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$$

The function is

A. independent of one variables.

B. independent of two variables.

C. independent of three variables.

D. dependent on all variables

gate2007 digital-logic normal min-sum-of-products-form

Answer

4.29.7 Min Sum Of Products Form: GATE2008-IT-8 top http://gateoverflow.in/3268

Consider the following Boolean function of four variables

$f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$

The function is

A. independent of one variable
B. independent of two variables
C. independent of three variable
D. dependent on all the variables

gate2008-it digital-logic normal min-sum-of-products-form

Answer

4.29.8 Min Sum Of Products Form: GATE2011-14 top http://gateoverflow.in/2116

The simplified SOP (Sum of Product) from the Boolean expression

$$(P + \bar{Q} + \bar{R}).(P + \bar{Q} + R).(P + Q + \bar{R})$$

is

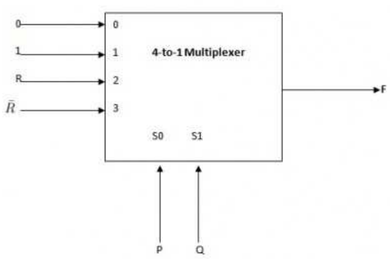
A. $(\bar{P}.Q + \bar{R})$
B. $(P + \bar{Q}.\bar{R})$
C. $(\bar{P}.Q + R)$
D. $(P.Q + R)$

gate2011 digital-logic normal min-sum-of-products-form

Answer

4.29.9 Min Sum Of Products Form: GATE2014-1-45 top http://gateoverflow.in/1923

Consider the 4-to-1 multiplexer with two select lines S_1 and S_0 given below



The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

A. $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
B. $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
C. $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$
D. $PQ\bar{R}$

gate2014-1 digital-logic normal multiplexer min-sum-of-products-form

Answer

4.29.10 Min Sum Of Products Form: GATE2014-1-7 top http://gateoverflow.in/1764

Consider the following Boolean expression for F:

$F(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$

The minimal sum—of—products form of F is

A. $PQ + QR + QS$
B. $P + Q + R + S$
C. $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
D. $\bar{P}R + \bar{R}\bar{P}S + P$

gate2014-1 digital-logic normal min-sum-of-products-form

Answer

4.29.11 Min Sum Of Products Form: GATE2014-3-7 top http://gateoverflow.in/2041

Consider the following minterm expression for F:

$$F(P, Q, R, S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$$

The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for F is

A. $Q\bar{S} + \bar{Q}S$
B. $\bar{Q}\bar{S} + QS$
C. $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$
D. $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

gate2014-3 digital-logic min-sum-of-products-form normal

Answer

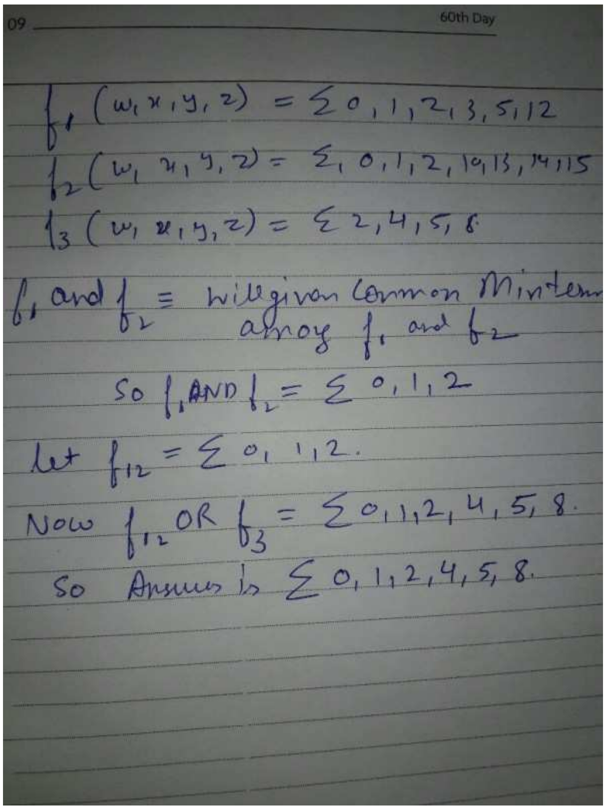
Answers: Min Sum Of Products Form

4.29.1 Min Sum Of Products Form: GATE1988-2v top http://gateoverflow.in/91685

Selected Answer

final output

Σ(0,1,2,4,5,8)


09 60th Day
$f_1(w,x,y,z) = \Sigma\, 0,1,2,3,5,12$
$f_2(w,x,y,z) = \Sigma\, 0,1,2,10,13,14,15$
$f_3(w,x,y,z) = \Sigma\, 2,4,5,8$
f_1 and f_2 = will given Common Minterm among f_1 and f_2
So f_1 AND $f_2 = \Sigma\, 0,1,2$
let $f_{12} = \Sigma\, 0,1,2.$
Now f_{12} OR $f_3 = \Sigma\, 0,1,2,4,5,8.$
So Answer is $\Sigma\, 0,1,2,4,5,8.$

5 votes -- kunal (20.8k points)

4.29.2 Min Sum Of Products Form: GATE1991-5,b top http://gateoverflow.in/26437

Selected Answer

(b)

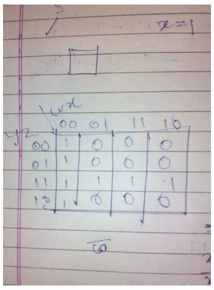
0 1 A'B'C'D'	1	3 x	2 1 A'B'CD'
4	5	7	6
12 x	13	15 1 ABCD	14 x ABCD'
8 1 AB'C'D'	9	11 X AB'CD	10 1 ABCD'

The minimum SOP form of the logic function is given as : f(A,B,C,D) = B'D'+AC

9 votes -- Kalpna Bhargav (3.2k points)

4.29.3 Min Sum Of Products Form: GATE1997_71 top http://gateoverflow.in/19701

Selected Answer



Answer of question 1 :- w'x'+yz

Answer of Question 2 :-

stuck at 0 , means output is fixed at 0(No matter what is input).we got 0 for 9 input combinations(Check Kmpa) ,So answer is 9,

4 votes -- Akash (43.8k points)

4.29.4 Min Sum Of Products Form: GATE2001-10 top http://gateoverflow.in/751

Selected Answer

checking self dual of a function.

$\text{f} = \Sigma(0, 1, 2, 4) = \text{a'b'c'} + \text{a'b'c} + \text{a'bc'} + \text{ab'c'}$

now write it in max term form $(\text{a'+b'+c'})\ (\text{a'+b'+c})(\text{a'+b+c'})(\text{a+b'+c'})$

7 6 5 3

$=$
$\prod(3{,}5{,}6{,}7) =$
$\sum(0, 1, 2, 4) =$ given function so its a self dual

8 votes -- Umang Raman (15.2k points)

there are two condition for a function being self dual.

1- it should be neutral function. (no. of minter = no . of max term)

2-no mutually two exclusive term should be there like (0-7 are mutaully exclusive 1-6, 2-5, 3-4) from these pairs only one should be there.

clearly there are 4 minterm, so number of minterms = no of maxterms.

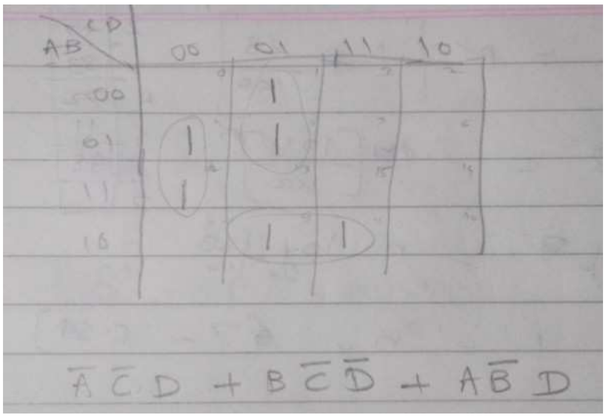
and scond condition is also satisfied. so it is a self dual function .

10 votes -- No Need (14.1k points)

4.29.5 Min Sum Of Products Form: GATE2005-18 top http://gateoverflow.in/1354

Selected Answer

Answer is : [A]



6 votes -- Desert_Warrior (9.6k points)

4.29.6 Min Sum Of Products Form: GATE2007-9 top

http://gateoverflow.in/1207

Selected Answer

The K-map would be

	w'x'	w'x	wx	wx'
y'z'		1	1	
y'z	1			1
yz	1			1
yz'		1	1	

So, the minimized expression would be

x'z + xz'.

So, option B.

5 votes -- Arjun Suresh (294k points)

4.29.7 Min Sum Of Products Form: GATE2008-IT-8 top

http://gateoverflow.in/3268

Selected Answer

Option A

Map

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	1	1
$\bar{A}B$	0	0	1	1
AB	1	1	0	0
$A\bar{B}$	1	1	1	1

(2,3,6,7)	$\bar{A}C$
(2,3,10,11)	$\bar{B}C$
(8,9,12,13)	$A\bar{C}$

$y = \bar{A}C + \bar{B}C + A\bar{C}$

6 votes -- Aditi Tiwari (1.1k points)

4.29.8 Min Sum Of Products Form: GATE2011-14 top

http://gateoverflow.in/2116

Selected Answer

Karnaugh map

1	0	0	0
1	1	1	1

Answer is **B**

11 votes -- Sona Praneeth Akula (4k points)

4.29.9 Min Sum Of Products Form: GATE2014-1-45 top http://gateoverflow.in/1923

Selected Answer

S0 and S1 are used to select the input given to be given as output.

S0	S1	Output
0	0	0
0	1	1
1	0	R
1	1	R'

So, output becomes 1 for
$S0'S1 + S0S1'R + S0S1R'$

$= P'Q + PQ'R + PQR'$

$= P'Q + PQR' + PQ'R$

$= Q(P' + PR') + PQ'R$

$= Q(P' + R') + PQ'R \, (\because A + A'B = A + B)$

$= P'Q + QR' + PQ'R$

Option (A)

12 votes -- Arjun Suresh (294k points)

4.29.10 Min Sum Of Products Form: GATE2014-1-7 top http://gateoverflow.in/1764

Selected Answer

$PQ \; RS$	$\bar{R}\bar{S}$	$\bar{R}S$	RS	$R\bar{S}$
$\bar{P}\bar{Q}$	0	0	0	0
$\bar{P}Q$	0	1	1	1
PQ	1	1	1	1
$P\bar{Q}$	0	0	0	0

Minimal SOP $= PQ + QR + QS$

Hence, **option A** is correct.

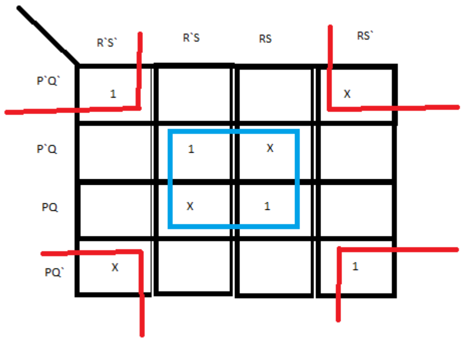
7 votes -- Amar Vashishth (28.7k points)

4.29.11 Min Sum Of Products Form: GATE2014-3-7 top

http://gateoverflow.in/2041

Selected Answer

While putting the terms to K-map the 3rd and 4th columns are swapped so do 3rd and 4th rows. So, term 2 is going to (0,3) column instead of (0,2), 8 is going to (3,0) instead of (2,0) etc..



Solving this k-map gives B) as the answer.

Reference: http://www.cs.uiuc.edu/class/sp08/cs231/lectures/04-Kmap.pdf

13 votes -- Srinath Jayachandran (3.7k points)

4.30 Minimal State Automata(1) top

4.30.1 Minimal State Automata: GATE2003-44 top

http://gateoverflow.in/935

A 1-input, 2-output synchronous sequential circuit behaves as follows:

Let z_k, n_k denote the number of 0's and 1's respectively in initial k bits of the input

$(z_k + n_k = k)$. The circuit outputs 00 until one of the following conditions holds.

- $z_k - n_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 10.
- $n_k - z_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 01.

What is the minimum number of states required in the state transition graph of the above circuit?

A. 5
B. 6
C. 7
D. 8

gate2003 digital-logic finite-automata minimal-state-automata normal

Answer

Answers: Minimal State Automata

4.30.1 Minimal State Automata: GATE2003-44 top

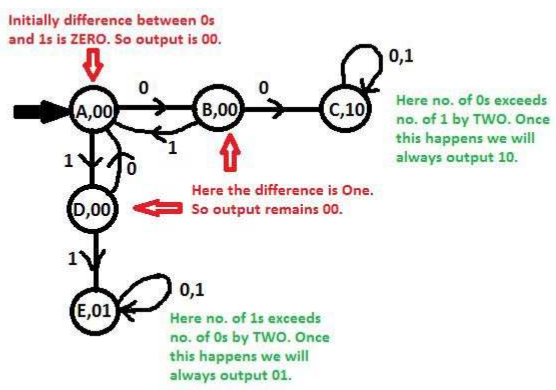
http://gateoverflow.in/935

Selected Answer

Though the question is from digital logic, answer is purely from automata. As per question, we just need to count the difference of the number of 0's and 1's in the first k bit of a number. And we just need to count till this count reaches 2 or -2 (negative when number of 0's is less than number of 1's) . So, the possibilities are -2, -1, 0, 1 and 2 which represents the five states of the state transition diagram.

For state -2, the output of the circuit will be 01, for state 2, output will be 10 (both these states not having any outgoing transitions) and for other 3 states, output will be 00 as per the given description of the circuit.

👍 23 votes -- gatecse (13.4k points)



The Automaton will look like this. :D

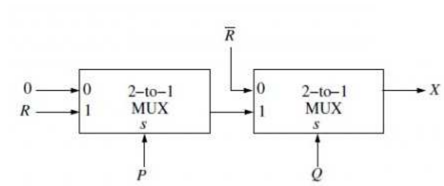
👍 11 votes -- Rajendra Dangwal (685 points)

4.31 Multiplexer(10) top

4.31.1 Multiplexer: GATE 2016-1-30 top

http://gateoverflow.in/39722

Consider the two cascade 2 to 1 multiplexers as shown in the figure .



The minimal sum of products form of the output X is

A). $\overline{P}\,\overline{Q}+PQR$

B). $\overline{P}\,Q+QR$

C). $PQ+\overline{P}\,\overline{Q}R$

D). $\overline{Q}\,\overline{R}+PQR$

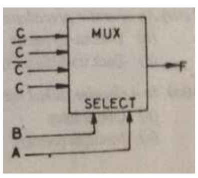
gate2016-1 digital-logic multiplexer normal

Answer

4.31.2 Multiplexer: GATE1987-1-IV top

http://gateoverflow.in/80193

The output F of the below multiplexer circuit can be represented by



A. $AB+B\bar{C}+\bar{C}A+\bar{B}\bar{C}$
B. $A\oplus B\oplus C$

C. $A \oplus B$
D. $\bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C}$

gate1987 digital-logic circuit-output multiplexer

Answer

4.31.3 Multiplexer: GATE1990-5b top http://gateoverflow.in/85398

Show with the help of a block diagram how the Boolean function :

$f = AB + BC + CA$

can be realised using only a $4:1$ multiplexer.

gate1990 descriptive digital-logic multiplexer

Answer

4.31.4 Multiplexer: GATE1992_04_b top http://gateoverflow.in/17407

A priority encoder accepts three input signals (A, B and C) and produce a two-bit output (X1 , X0) corresponding to the highest priority active input signal. Assume A has the highest priority followed by B and C has the lowest priority. If none of the inputs are active the output should be 00, design the priority encoder using 4:1 multiplexers as the main components.

gate1994 digital-logic multiplexer

Answer

4.31.5 Multiplexer: GATE1998_1.14 top http://gateoverflow.in/1651

A multiplexer with a $4-bit$ data select input is a

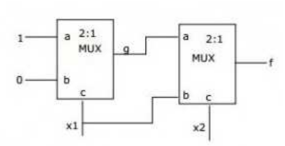
A. $4:1$ multiplexer
B. $2:1$ multiplexer
C. $16:1$ multiplexer
D. $8:1$ multiplexer

gate1998 digital-logic multiplexer easy

Answer

4.31.6 Multiplexer: GATE2001-2.11 top http://gateoverflow.in/729

Consider the circuit shown below. The output of a 2:1 Mux is given by the function $(ac' + bc)$.



Which of the following is true?

A. $f = X1' + X2$
B. $f = X1'X2 + X1X2'$
C. $f = X1X2 + X1'X2'$
D. $f = X1 + X2'$

gate2001 digital-logic normal multiplexer

Answer

4.31.7 Multiplexer: GATE2004-60 top http://gateoverflow.in/1055

Consider a multiplexer with X and Y as data inputs and Z the as control input. $Z = 0$ selects input X, and $Z = 1$ selects input Y. What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

A. R to X, 1 to Y, T to Z
B. T to X, R to Y, T to Z
C. T to X, R to Y, 0 to Z
D. R to X, 0 to Y, T to Z

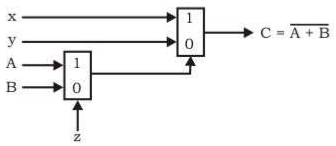
gate2004 digital-logic normal multiplexer

Answer

4.31.8 Multiplexer: GATE2005-IT-48 top

http://gateoverflow.in/3809

The circuit shown below implements a 2-input NOR gate using two $2-4$ MUX (control signal 1 selects the upper input). What are the values of signals x, y and z?



A. 1, 0, B
B. 1, 0, A
C. 0, 1, B
D. 0, 1, A

gate2005-it digital-logic normal multiplexer

Answer

4.31.9 Multiplexer: GATE2007-34 top

http://gateoverflow.in/1232

Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

A. 2^n line to 1 line

B. 2^{n+1} line to 1 line

C. 2^{n-1} line to 1 line

D. 2^{n-2} line to 1 line

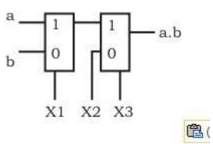
gate2007 digital-logic normal multiplexer

Answer

4.31.10 Multiplexer: GATE2007-IT-8 top

http://gateoverflow.in/3441

The following circuit implements a two-input AND gate using two 2-1 multiplexers.



What are the values of $X1, X2, X3$?

A. $X1 = b, X2 = 0, X3 = a$
B. $X1 = b, X2 = 1, X3 = b$
C. $X1 = a, X2 = b, X3 = 1$
D. $X1 = a, X2 = 0, X3 = b$

gate2007-it digital-logic normal multiplexer

Answer

Answers: Multiplexer

4.31.1 Multiplexer: GATE 2016-1-30 top http://gateoverflow.in/39722

Selected Answer

For $2:1$ MUX, output $Y = S'I_o + SI_1$

So, output of MUX1 ,$f_1 = P'0 + PR = PR$

Output of MUX2 , $f_2 = Q'R' + Qf_1 = Q'R' + PQR$

which is option **D**

19 votes -- Monanshi Jain (8.5k points)

4.31.2 Multiplexer: GATE1987-1-IV top http://gateoverflow.in/80193

Selected Answer

Ans B)

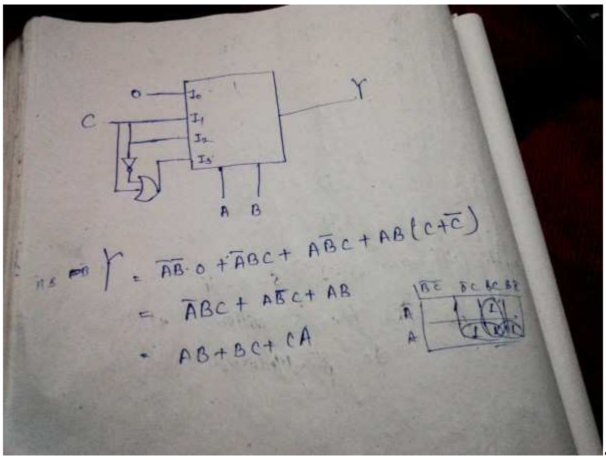
A'B'C+AB'C'+A'BC+ABC

=(A+B')(A'+B)C+A'BC'+AB'C'

=$A \oplus B \oplus C$

5 votes -- srestha (58.4k points)

4.31.3 Multiplexer: GATE1990-5b top http://gateoverflow.in/85398

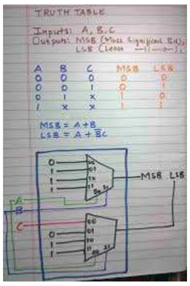


.....

2 votes -- kirti singh (3.4k points)

4.31.4 Multiplexer: GATE1992_04_b top http://gateoverflow.in/17407

Selected Answer



It can be implemented using two 4 x 1 Multiplexers.

3 votes -- Anurag Pandey (13.1k points)

4.31.5 Multiplexer: GATE1998_1.14 top http://gateoverflow.in/1651

Selected Answer

for n bit data select input

$2^n : 1$

for 4 it is $16 : 1$

12 votes -- Bhagirathi Nayak (13.3k points)

4.31.6 Multiplexer: GATE2001-2.11 top http://gateoverflow.in/729

Selected Answer

g = x1'
So, f = ac' + bc

= x1'x2' + x1x2

So, (C).

14 votes -- Arjun Suresh (294k points)

4.31.7 Multiplexer: GATE2004-60 top http://gateoverflow.in/1055

Selected Answer

answer = **option A**

Z'X + ZY..
Put Z = T, X = R, Y = 1 in Z'X + ZY..
= T'R + 1*T

= (T+T') (T+R)
= T + R

8 votes -- Digvijay (47k points)

4.31.8 Multiplexer: GATE2005-IT-48 top http://gateoverflow.in/3809

Selected Answer

$f = Az + B\bar{z}$ (As A will be selected when z is high) .

So next function will become $g = xf + y\bar{f}$

$= x\,(Az + B\bar{z}) + y(\overline{Az + B\bar{z}})$

Putting x = 0, y = 1, z = A,we get $g = \overline{AA + B\bar{A}} = \overline{A + B}$ $(\because A + B\bar{A} = A + B)$ and answer will becomeD

14 votes -- John Carter (951 points)

4.31.9 Multiplexer: GATE2007-34 top

http://gateoverflow.in/1232

Selected Answer

2^{n-1} to 1

We will map $(n-1)$ variables to select lines and 1 variable to input line

13 votes -- Anurag Semwal (8k points)

4.31.10 Multiplexer: GATE2007-IT-8 top

http://gateoverflow.in/3441

Selected Answer

Answer: A

F = (bX_1' + aX_1)X_3 + X_2X_3'

Put X_1 = b, X_2 = 0, X_3 = a to get F = ab.

10 votes -- Rajarshi Sarkar (35k points)

4.32 Number Representation(48) top

4.32.1 Number Representation: GATE 2016-1-07 top

http://gateoverflow.in/39649

The
16 -bit
$2's$ complement representation of an integer is
$1111 \quad 1111 \quad 1111 \quad 0101$; its decimal representation is ______________.

gate2016-1 digital-logic number-representation normal numerical-answers

Answer

4.32.2 Number Representation: GATE 2016-2-09 top

http://gateoverflow.in/39546

Let X be the number of distinct 16-bit integers in $2's$ complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation Then $X - Y$ is______.

gate2016-2 digital-logic number-representation normal numerical-answers

Answer

4.32.3 Number Representation: GATE1988-2vi top

http://gateoverflow.in/91687

Define the value of r in the following: $\sqrt{(41)_r} = (7)_{10}$

gate1988 digital-logic normal number-representation numerical-answers

Answer

4.32.4 Number Representation: GATE1990-1-viii top

http://gateoverflow.in/87055

The condition for overflow in the addition of two 2's complement numbers in terms of the carry generated by the two most significant bits is ____________.

gate1990 descriptive digital-logic number-representation

Answer

4.32.5 Number Representation: GATE1991_01,iii top http://gateoverflow.in/500

Consider the number given by the decimal expression:

$$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$$

The number of 1's in the unsigned binary representation of the number is _______

gate1991 digital-logic number-representation normal

Answer

4.32.6 Number Representation: GATE1991_01,v top http://gateoverflow.in/503

When two $4-bit$ numbers $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ are multiplied, the bit c_1 of the product C is given by _________

gate1991 digital-logic normal number-representation

Answer

4.32.7 Number Representation: GATE1992_04a top http://gateoverflow.in/583

Consider addition in two's complement arithmetic. A carry from the most significant bit does not always correspond to an overflow. Explain what is the condition for overflow in two's complement arithmetic.

gate1992 digital-logic normal number-representation

Answer

4.32.8 Number Representation: GATE1993_6.5 top http://gateoverflow.in/2286

Convert the following numbers in the given bases into their equivalents in the desired bases:

a. $(110.101)_2 = (x)_{10}$
b. $(1118)_{10} = (y)_H$

gate1993 digital-logic number-representation normal

Answer

4.32.9 Number Representation: GATE1994_2.7 top http://gateoverflow.in/2474

Consider n-bit (including sign bit) 2's complement representation of integer numbers. The range of integer values, N, that can be represented is _____ $\leq N \leq$_____ .

gate1994 digital-logic number-representation easy

Answer

4.32.10 Number Representation: GATE1995-2.12, ISRO2015-9 top http://gateoverflow.in/2624

The number of 1's in the binary representation of (3*4096 + 15*256 + 5*16 + 3) are:

A. 8
B. 9
C. 10
D. 12

gate1995 digital-logic number-representation normal isro2015

Answer

4.32.11 Number Representation: GATE1995_18 top

http://gateoverflow.in/2655

The following is an incomplete Pascal function to convert a given decimal integer (in the range -8 to +7) into a binary integer in 2's complement representation. Determine the expression A, B, C that complete program.

```
function TWOSCOMP (N:integer):integer;
    var
    REM, EXPONENT:integer;
    BINARY :integer;
    begin
        if(N>=-8) and (N<=+7) then
        begin
            if N<0 then
                N:=A;
            BINARY:=0;
            EXPONENT:=1;
            while N<>0 do
            begin
                REM:=N mod 2;
                BIANRY:=BINARY + B*EXPONENT;
                EXPONENT:=EXPONENT*10;
                N:=C
            end
            TWOSCOMP:=BINARY
        end
    end;
```

gate1995 digital-logic number-representation normal

Answer

4.32.12 Number Representation: GATE1996_1.25 top

http://gateoverflow.in/2729

Consider the following floating-point number representation.

31	24	23	0
Exponent		Mantissa	

The exponent is in 2's complement representation and mantissa is in the sign magnitude representation. The range of the magnitude of the normalized numbers in this representation is

A. 0 to 1
B. 0.5 to 1
C. 2^{-23} to 0.5
D. 0.5 to $\left(1-2^{-23}\right)$

gate1996 digital-logic number-representation normal

Answer

4.32.13 Number Representation: GATE1997_5.4 top

http://gateoverflow.in/2255

Given $\sqrt{(224)_r} = (13)_r$.

The value of the radix r is:

A. 10
B. 8
C. 5
D. 6

gate1997 digital-logic number-representation normal

Answer

4.32.14 Number Representation: GATE1998_1.17 top

http://gateoverflow.in/1654

The octal representation of an integer is $(342)_8$. If this were to be treated as an eight-bit integer in an 8085 based computer, its decimal equivalent is

A. 226
B. -98
C. 76
D. -30

gate1998 digital-logic number-representation normal

Answer

4.32.15 Number Representation: GATE1998_2.20 top http://gateoverflow.in/1693

Suppose the domain set of an attribute consists of signed four digit numbers. What is the percentage of reduction in storage space of this attribute if it is stored as an integer rather than in character form?

A. 80%
B. 20%
C. 60%
D. 40%

gate1998 digital-logic number-representation normal

Answer

4.32.16 Number Representation: GATE1999_2.17 top http://gateoverflow.in/1495

Zero has two representations in

A. Sign magnitude
B. 2's complement
C. 1's complement
D. None of the above

gate1999 digital-logic number-representation easy

Answer

4.32.17 Number Representation: GATE2000-1.6 top http://gateoverflow.in/629

The number 43 in 2's complement representation is

A. 01010101
B. 11010101
C. 00101011
D. 10101011

gate2000 digital-logic number-representation easy

Answer

4.32.18 Number Representation: GATE2000-2.14 top http://gateoverflow.in/661

Consider the values of A = 2.0 x 10^{30}, B = -2.0 x 10^{30}, C = 1.0, and the sequence

```
X:= A + B          Y:= A + C
X:= X + C          Y:= Y + B
```

executed on a computer where floating point numbers are represented with 32 bits. The values for X and Y will be

A. X = 1.0, Y = 1.0
B. X = 1.0, Y = 0.0
C. X = 0.0, Y = 1.0
D. X = 0.0, Y = 0.0

gate2000 digital-logic number-representation normal

Answer

4.32.19 Number Representation: GATE2001-2.10 top http://gateoverflow.in/728

The 2's complement representation of $(-539)_{10}$ in hexadecimal is

A. ABE
B. DBC
C. DE5
D. 9E7

gate2001 digital-logic number-representation easy

Answer

4.32.20 Number Representation: GATE2002-1.14 top http://gateoverflow.in/818

The decimal value 0.25

A. is equivalent to the binary value 0.1
B. is equivalent to the binary value 0.01
C. is equivalent to the binary value 0.00111...
D. cannot be represented precisely in binary

gate2002 digital-logic number-representation easy

Answer

4.32.21 Number Representation: GATE2002-1.15 top http://gateoverflow.in/819

The 2's complement representation of the decimal value -15 is

A. 1111
B. 11111
C. 111111
D. 10001

gate2002 digital-logic number-representation easy

Answer

4.32.22 Number Representation: GATE2002-1.16 top http://gateoverflow.in/821

Sign extension is a step in

A. floating point multiplication
B. signed 16 bit integer addition
C. arithmetic left shift
D. converting a signed integer from one size to another

gate2002 digital-logic easy number-representation

Answer

4.32.23 Number Representation: GATE2002-1.21 top http://gateoverflow.in/826

In 2's complement addition, overflow

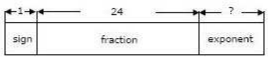
A. is flagged whenever there is carry from sign bit addition
B. cannot occur when a positive value is added to a negative value
C. is flagged when the carries from sign bit and previous bit match
D. None of the above

gate2002 digital-logic number-representation normal

Answer

4.32.24 Number Representation: GATE2002-9 top http://gateoverflow.in/862

Consider the following 32-bit floating-point representation scheme as shown in the format below. A value is specified by 3 fields, a one bit sign field (with 0 for positive and 1 for negative values), a 24 bit fraction field (with the binary point being at the left end of the fraction bits), and a 7 bit exponent field (in excess-64 signed integer representation, with 16 being the base of exponentiation). The sign bit is the most significant bit.



a. It is required to represent the decimal value - 7.5 as a normalized floating point number in the given format. Derive the values of the various fields. Express your final answer in the hexadecimal.
b. What is the largest value that can be represented using this format? Express your answer as the nearest power of 10.

gate2002 digital-logic number-representation normal descriptive

Answer

4.32.25 Number Representation: GATE2003-9 top http://gateoverflow.in/900

Assuming all numbers are in 2's complement representation, which of the following numbers is divisible by 11111011?

A. 11100111

B. 11100100

C. 11010111

D. 11011011

gate2003 digital-logic number-representation normal

Answer

4.32.26 Number Representation: GATE2004-19 top http://gateoverflow.in/1016

If 73_x (in base-x number system) is equal to 54_y (in base y-number system), the possible values of x and y are

A. 8, 16
B. 10, 12
C. 9, 13
D. 8, 11

gate2004 digital-logic number-representation easy

Answer

4.32.27 Number Representation: GATE2004-28 top http://gateoverflow.in/1025

What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

(113. + -111.) + 7.51

113. + (-111. + 7.51)

A. 9.51 and 10.0 respectively

B. 10.0 and 9.51 respectively

C. 9.51 and 9.51 respectively

D. 10.0 and 10.0 respectively

gate2004 digital-logic number-representation normal

Answer

4.32.28 Number Representation: GATE2004-66 top http://gateoverflow.in/1060

Let A = 1111 1010 and B = 0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is

A. 1100 0100
B. 1001 1100
C. 1010 0101
D. 1101 0101

gate2004 digital-logic number-representation easy

Answer

4.32.29 Number Representation: GATE2004-IT-42 top http://gateoverflow.in/3685

Using a 4-bit 2's complement arithmetic, which of the following additions will result in an overflow?

i. 1100 + 1100
ii. 0011 + 0111
iii. 1111 + 0111

A. i only
B. ii only
C. iii only
D. i and iii only

gate2004-it digital-logic number-representation normal

Answer

4.32.30 Number Representation: GATE2004-IT-43 top http://gateoverflow.in/3686

The number $(123456)_8$ is equivalent to

A. $(A72E)_{16}$ and $(22130232)_4$
B. $(A72E)_{16}$ and $(22131122)_4$
C. $(A73E)_{16}$ and $(22130232)_4$
D. $(A62E)_{16}$ and $(22120232)_4$

gate2004-it digital-logic number-representation normal

Answer

4.32.31 Number Representation: GATE2005-16, ISRO2009-18, ISRO2015-2 top

The range of integers that can be represented by an n bit 2's complement number system is:

A. -2^{n-1} to $(2^{n-1}-1)$
B. $-(2^{n-1}-1)$ to $(2^{n-1}-1)$
C. -2^{n-1} to 2^{n-1}
D. $-(2^{n-1}+1)$ to $(2^{n-1}-1)$

gate2005 digital-logic number-representation easy isro2009 isro2015

Answer

4.32.32 Number Representation: GATE2005-17 top http://gateoverflow.in/1353

The hexadecimal representation of 657_8 is:

A. 1AF

B. D78
C. D71
D. 32F

gate2005 digital-logic number-representation easy

Answer

4.32.33 Number Representation: GATE2005-IT-47 top

http://gateoverflow.in/3808

$(34.4)_8 \times (23.4)_8$ evaluates to

A. $(1053.6)_8$
B. $(1053.2)_8$
C. $(1024.2)_8$
D. None of these

gate2005-it digital-logic number-representation normal

Answer

4.32.34 Number Representation: GATE2006-39 top

http://gateoverflow.in/1815

We consider the addition of two $2's$ complement numbers $b_{n-1}b_{n-2}\dots b_0$ and $a_{n-1}a_{n-2}\dots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}\dots c_0$ and the carry-out by c_{out}. Which one of the following options correctly identifies the overflow condition?

A. $c_{out}\left(\overline{a_{n-1}\oplus b_{n-1}}\right)$
B. $a_{n-1}b_{n-1}\overline{c_{n-1}}+\overline{a_{n-1}b_{n-1}}c_{n-1}$
C. $c_{out}\oplus c_{n-1}$
D. $a_{n-1}\oplus b_{n-1}\oplus c_{n-1}$

gate2006 digital-logic number-representation normal

Answer

4.32.35 Number Representation: GATE2006-IT-7, ISRO2009-41 top

http://gateoverflow.in/3546

The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in

A. 0001 and an overflow
B. 1001 and no overflow
C. 0001 and no overflow
D. 1001 and an overflow

gate2006-it digital-logic number-representation normal isro2009

Answer

4.32.36 Number Representation: GATE2007-IT-42 top

http://gateoverflow.in/3477

$(C012.25)_H - (10111001110.101)_B =$

A. (135103.412)o
B. (564411.412)o
C. (564411.205)o
D. (135103.205)o

gate2007-it digital-logic number-representation normal

Answer

4.32.37 Number Representation: GATE2008-6 top

http://gateoverflow.in/404

Let r denote number system radix. The only value(s) of r that satisfy the equation $\sqrt{121_r}=11_r$, is/are

A. decimal 10
B. decimal 11
C. decimal 10 and 11
D. any value > 2

gate2008 digital-logic number-representation normal

Answer

4.32.38 Number Representation: GATE2008-IT-15 top http://gateoverflow.in/3275

A processor that has carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

A. 1, 1, 0
B. 1, 0, 0
C. 0, 1, 0
D. 1, 0, 1

gate2008-it digital-logic number-representation normal

Answer

4.32.39 Number Representation: GATE2009-5, ISRO2017-57 top http://gateoverflow.in/1297

$(1217)_8$ is equivalent to

A. $(1217)_{16}$
B. $(028F)_{16}$
C. $(2297)_{10}$
D. $(0B17)_{16}$

gate2009 digital-logic number-representation isro2017

Answer

4.32.40 Number Representation: GATE2010-8 top http://gateoverflow.in/2179

P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of $8 \times P$ is

A. $(C3D8)_{16}$
B. $(187B)_{16}$
C. $(F878)_{16}$
D. $(987B)_{16}$

gate2010 digital-logic number-representation normal

Answer

4.32.41 Number Representation: GATE2013_4 top http://gateoverflow.in/1413

The smallest integer that can be represented by an 8-bit number in 2's complement form is

(A) -256
(B) -128
(C) -127
(D) 0

gate2013 digital-logic number-representation easy

Answer

4.32.42 Number Representation: GATE2014-1-8 top http://gateoverflow.in/1766

The base (or radix) of the number system such that the following equation holds is____________.

$\frac{312}{20} = 13.1$

gate2014-1 digital-logic number-representation numerical-answers normal

Answer

4.32.43 Number Representation: GATE2014-2-45 top

http://gateoverflow.in/2011

The value of a $float$ type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A $float$ type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is

A. C1640000H
B. 416C0000H
C. 41640000H
D. C16C0000H

gate2014-2 digital-logic number-representation normal

Answer

4.32.44 Number Representation: GATE2014-2-8 top

http://gateoverflow.in/1961

Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____ .

gate2014-2 digital-logic number-representation numerical-answers normal

Answer

4.32.45 Number Representation: GATE2015-3_35 top

http://gateoverflow.in/8494

Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is _____

gate2015-3 digital-logic number-representation normal numerical-answers

Answer

4.32.46 Number Representation: GATE2017-1-9 top

http://gateoverflow.in/118289

When two 8-bit numbers $A_7 \dots A_0$ and $B_7 \dots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a **ripple-carry adder,** the sum bits obtained are $S_7 \dots S_0$ and the carry bits are $C_7 \dots C_0$. An overflow is said to have occurred if

(A) the carry bit C_7 is 1.

(B) all the carry bits $(C_7, \dots, C_0)$ are 1.

(C) $\left(A_7.B_7.\bar{S}_7 + \bar{A}_7.\bar{B}_7.S_7\right)$ is 1.

(D) $\left(A_0.B_0.\bar{S}_0 + \bar{A}_0.\bar{B}_0.S_0\right)$ is 1.

gate2017-1 digital-logic number-representation

Answer

4.32.47 Number Representation: GATE2017-2-1 top

http://gateoverflow.in/118337

The representation of the value of a $16-bit$ unsigned integer X in hexadecimal number system is $BCA9$. The representation of the value of X in octal number system is

A. 571244
B. 736251
C. 571247
D. 136251

gate2017-2 digital-logic number-representation

Answer

4.32.48 Number Representation: TIFR2011-A-16 top http://gateoverflow.in/20253

A variable that takes thirteen possible values can be communicated using?

a. Thirteen bits.
b. Three bits.
c. $\log_2 13$ bits.
d. Four bits.
e. None of the above.

tifr2011 number-representation

Answer

Answers: Number Representation

4.32.1 Number Representation: GATE 2016-1-07 top http://gateoverflow.in/39649

Selected Answer

Answer = -11..

for 2's complement 1 **111 1111 1111 0101** →2'scomplement→2'scomplement 1 000 0000 0000 1011

1st bit is same not involved in 2's complement same with 1's complement. since msb bit for sign.

Take one's complement and add 1 we get 11, and as it is negative number we get answer as -11

Reffer http://www.electronics-tutorials.ws/binary/signed-binary-numbers.html

23 votes -- Abhilash Panicker (8.8k points)

$1111\ 1111\ 1111\ 0101$

$2's$ complement of
$1111\ 1111\ 1111\ 0101$ =
$0000\ 0000\ 0000\ 1011$ =
$+11$

$2's$ complement of
-11 =
$+11$,in
$2's$ complement representation

$2's$ complement of
$+11$ =
-11 , in
$2's$ complement representation

So
-11 it should be

15 votes -- Praveen Saini (53.6k points)

4.32.2 Number Representation: GATE 2016-2-09 top http://gateoverflow.in/39546

Selected Answer

For N bits, Distinct values represented in 2's complement is -2^{n-1} to 2^{n-1} -1

Distinct values represented in Signed Magnitude is $-(2^{n-1}$ -1) to 2^{n-1} -1

Difference is 1.

24 votes -- Sharathkumar Anbu (717 points)

4.32.3 Number Representation: GATE1988-2vi top http://gateoverflow.in/91687

Selected Answer

$\sqrt{41_r} = 7_{10}$

squaring both sides we get

$41_r = (49)_{10}$

4r+1=40+9
4r=48
r=12

6 votes -- kunal (20.8k points)

4.32.4 Number Representation: GATE1990-1-viii top http://gateoverflow.in/87055

Selected Answer

The condition for overflow in the addition of two 2's complement numbers in terms of the carry generated by the two most significant bits is when carry on MSB but not From MSB, or Carry from MSB but not on MSB. i.e.,

$$C_{out} \oplus C_{n-1} = 1.$$

i.e. For overflow to happen during addition of two numbers in 2's complement form

They must have same sign and result is of opposite sign

Overflow occurs if

1. (+A) + (+B) = −C

2.(−A) + (−B) = +C

PS: Overflow is useful for signed numbers and useless for unsigned numbers

4 votes -- Prashant Singh (49.2k points)

4.32.5 Number Representation: GATE1991_01,iii top http://gateoverflow.in/500

Selected Answer

Hex representation of given no. is $(9753)_{16}$

Its binary representation is $(1001\ 0111\ 0101\ 0011)_2$

The no. of 1's is 9

14 votes -- Keith Kr (6.3k points)

4.32.6 Number Representation: GATE1991_01,v top http://gateoverflow.in/503

Selected Answer

$$\begin{array}{cccccccc}
 & & & & a_3 & a_2 & a_1 & a_0 \\
 & & & \times & b_3 & b_2 & b_1 & b_0 \\
 & - & - & - & - & - & - & - \\
 & & & & a_3b_0 & a_2b_0 & a_1b_0 & a_0b_0 \\
 & & & a_3b_1 & a_2b_1 & a_1b_1 & a_0b_1 & \times \\
 & & a_3b_2 & a_2b_2 & a_1b_2 & a_0b_2 & \times & \times \\
 & a_3b_3 & a_2b_3 & a_1b_3 & a_0b_3 & \times & \times & \times \\
- & - & - & - & - & - & - & - \\
c_7 & c_6 & c_5 & c_4 & c_3 & c_2 & c_1 & c_0
\end{array}$$

$c_1 = b_1a_0 \oplus a_1b_0$

14 votes -- Pooja Palod (32.4k points)

4.32.7 Number Representation: GATE1992_04a top http://gateoverflow.in/583

Selected Answer

XOR of C_{in} with C_{out} of the msb position.

5 votes -- Amar Vashishth (28.7k points)

4.32.8 Number Representation: GATE1993_6.5 top http://gateoverflow.in/2286

Selected Answer

a. $1 * 2^2 + 1 * 2^1 + 0 * 2^0 + 1 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} = 6.625$

b. 1118 mod 16 = 14, quotient = 69
69 mod 16 = 5, quotient = 4
4 mod 16 = 4.

Writing the mods in the reverse order (in hex) gives $(45E)_H$

Both can be done using calculator also.

8 votes -- Arjun Suresh (294k points)

4.32.9 Number Representation: GATE1994_2.7 top http://gateoverflow.in/2474

Selected Answer

$-2^{n-1} <= N <= 2^{n-1} -1$

Example : let we have 3 bit binary no (unsigned)

000 (0) to 111(7) total of 8 (2^3) no.

but when we have one signed bit then we have half of negative -4 to -1 and 0 and 1 to 3

```
bit pattern:    100   101  110  111  000  001  010  011

1's comp:       -3     -2   -1    0    0    1    2    3

2's comp.:      -4     -3   -2   -1    0    1    2    3
```

14 votes -- Praveen Saini (53.6k points)

4.32.10 Number Representation: GATE1995-2.12, ISRO2015-9 top http://gateoverflow.in/2624

Selected Answer

I suggest following approach , here we can clearly see that numbers are getting multiplied by powers of 16. So this is nothing but Hexadecimal number in disguise.

$(3 \times 4096 + 15 \times 256 + 5 \times 16 + 3) = (3F53)_{16} = (0011111101010011)_2$ which has total $2 + 4 + 2 + 2 = 10$ 1's

30 votes -- Akash (43.8k points)

$3 = (11)_2$
$3 \times 4096 = 3 \times (2^{12}) = (11)_2 << 12 = (11000000000000)_2$

Similarly, $15 \times 256 = (1111)_2 << 8 = (111100000000)_2$ and $5 \times 16 = (101)_2 << 4 = (1010000)_2$

So, $3 \times 4096 + 15 \times 256 + 5 \times 16 + 3 = (11111101010011)_2$

Number of 1's = 10.

19 votes -- Arjun Suresh (294k points)

4.32.11 Number Representation: GATE1995_18 top

http://gateoverflow.in/2655

Selected Answer

A=16+N, (for N = -1, A = 15 which is the largest value, for N = -8, A = 8)

B=REM

C=N/2

2 votes -- Shaun Patel (6.9k points)

4.32.12 Number Representation: GATE1996_1.25 top

http://gateoverflow.in/2729

Selected Answer

Here, we are asked "magnitude" - so we just need to consider the mantissa bits.

Also, we are told "normalized representation"- so most significant bit of mantissa is always 1 (this is different fromIEEE 754 normalized representation where this 1 is omitted in representation, but here it seems to be added on the right of decimal point as seen from options).

So, the maximum value of mantissa will be 23 1's where a decimal point is assumed before first 1. So, this value will be $1 - 2^{-23}$.

Due to the 1 in normalized representation, the smallest positive number will be 1 followed by 23 0's which will be $2^{-1} = 0.5$.

So ans d.

14 votes -- Pooja Palod (32.4k points)

Given that mantissa is sign magnitude representation so 1 bit for sign and remaining 23 bits for mantissa

and we have to find the range of mantissa in normalized form ....

so smallest will be = .100.....0(normalize form) which is 2^(-1) = .5

and for largest will be .111....1 which is 1-2^(-23) .

so range will be .5 to (1-2^(-23))

11 votes -- sonam vyas (13.2k points)

4.32.13 Number Representation: GATE1997_5.4 top http://gateoverflow.in/2255

Selected Answer

$\sqrt{(224)_r} = (13)_r$

convert r base to decimal

$\sqrt{2r^2 + 2r + 4} = r + 3$

take square both sides

$2r^2 + 2r + 4 = r^2 + 6r + 9$

$r^2 - 4r - 5 = 0$

$r^2 - 5r + r - 5 = 0$

$(r-5)(r+1)=0$

r can not be -1 so

r = 5 is correct answer

9 votes -- Praveen Saini (53.6k points)

4.32.14 Number Representation: GATE1998_1.17 top http://gateoverflow.in/1654

Selected Answer

$(3\ 4\ 2)_8 = (011\ 100\ 010)_2 = (11100010)_2$.

If we treat this as an 8 bit integer, the first bit becomes sign bit and since it is "1", number is negative. Computer uses 2's complement representation for negative numbers and hence the decimal equivalent will be $-(00011110)_2 = -30.$

7 votes -- Arjun Suresh (294k points)

4.32.15 Number Representation: GATE1998_2.20 top http://gateoverflow.in/1693

Selected Answer

I assume byte addressable memory- nothing smaller than a byte can be used.

We have four digits. So, to represent signed 4 digit numbers we need 5 bytes- 4 for four digits and 1 for the sign (like -7354). So, required memory = 5 bytes

Now, if we use integer, the largest number needed to represent is 9999 and this requires 2 bytes of memory for signed representation.

So, memory savings while using integer is $\frac{(5-2)}{5} = \frac{3}{5} = 60\%$

9 votes -- Arjun Suresh (294k points)

4.32.16 Number Representation: GATE1999_2.17 top http://gateoverflow.in/1495

Selected Answer

A and C

Sign Magnitude

+0 = 0000
-0 = 1000

1's complement
+0 = 0000
-0 = 1111

http://cs.anu.edu.au/courses/ENGN3213/Documents/PROJECT_READING_MATERIAL/Binary%20Representation%20and%20Cor

12 votes -- neelansh (327 points)

4.32.17 Number Representation: GATE2000-1.6 top http://gateoverflow.in/629

Selected Answer

2's complement representation is not same as 2's complement of a number. In 2's complement representation positive integers are represented in its normal binary form while negative numbers are represented in its 2's complement form. So (c) is correct here.

http://www.ele.uri.edu/courses/ele447/proj_pages/divid/twos.html

18 votes -- Arjun Suresh (294k points)

4.32.18 Number Representation: GATE2000-2.14 top http://gateoverflow.in/661

Selected Answer

Given 32 bits representation. So, the maximum precision can be 32 bits (In 32-bit IEEE representation, maximum precision is 24 bits but we take best case here). This means approximately 10 digits.

A = 2.0 * 10^{30}, C = 1.0

So, A + C should make the 31^{st} digit to 1, which is surely outside the precision level of A (it is 31^{st} digit and not 31^{st} bit). So, this addition will just return the value of A which will be assigned to Y.

So, Y + B will return 0.0 while X + C will return 1.0.

B choice.

Sample program if any one wants to try:

```
#include<stdio.h>
int main()
{
        float a = 2.0e30;
        float b = -2.0e30;
        float c = 1.0;
        float y = a+c;
        printf("a = %0.25f y = %0.25f\n",a, y);
        y = y + b;
        float x = a + b;
        printf("x = %0.25f\n",x);
        x = x + c;
        printf("x = %0.25f\n",x);
}
```

13 votes -- Arjun Suresh (294k points)

4.32.19 Number Representation: GATE2001-2.10 top http://gateoverflow.in/728

Selected Answer

539 = 512 + 16 + 8 + 2 + 1 = $2^9 + 2^4 + 2^3 + 2^1 + 2^0$
= $(1000011011)_2$

Now all answers have 12 bits, so we add two 0's at beginning = $(001000011011)_2$

To convert to 2's complement invert all bits till the rightmost 1, which will be $(110111100101)_2$

$= (1101\ 1110\ 0101)_2$

$= (DE5)_{16}$

13 votes -- Arjun Suresh (294k points)

4.32.20 Number Representation: GATE2002-1.14 top http://gateoverflow.in/818

Selected Answer

1st Multiplication Iteration

Multiply 0.25 by 2

0.25 x 2 = 0.50(Product) Fractional part=0.50 Carry=0 **(MSB)**

2nd Multiplication Iteration

Multiply 0.50 by 2

0.50 x 2 = 1.00(Product) Fractional part = 1.00 Carry = 1(LSB)

The fractional part in the 2nd iteration becomes zero and hence we stop the multiplication iteration.

Carry from the 1st multiplication iteration becomes **MSB** and carry from 2nd iteration becomes **LSB**

So the Result is 0.01

10 votes -- shekhar chauhan (42.9k points)

4.32.21 Number Representation: GATE2002-1.15 top http://gateoverflow.in/819

Selected Answer

D) is the correct ans.In 2's complement representation, positive numbers are represented in simple binary form and negative numbers are represented in its 2's complement form. So, for -15, we have to complement its binary value - 01111 and add a 1 to it, which gives 10001. Option D.

12 votes -- Ujjwal Saini (527 points)

4.32.22 Number Representation: GATE2002-1.16 top http://gateoverflow.in/821

Selected Answer

(d) is the answer. Sign extension (filling the upper bits using the sign bit) is needed while increasing the number of bits for representing a number. For positive numbers, 0 is extended and for negative numbers 1 is extended.

10 votes -- gatecse (13.4k points)

4.32.23 Number Representation: GATE2002-1.21 top http://gateoverflow.in/826

Selected Answer

(B) is the answer. When a positive value and negative value are added overflow never happens.

http://sandbox.mc.edu/~bennet/cs110/tc/orules.html

19 votes -- Arjun Suresh (294k points)

4.32.24 Number Representation: GATE2002-9 top

http://gateoverflow.in/862

Selected Answer

Here, mantissa is represented in normalized representation and exponent in excess-64 (subtract 64 to get actual value).

a. We have to represent $-(7.5)_{10} = -(111.1)_2$.

Now we are using base 16 for exponent. So, mantissa will be .01111 and this makes exponent as 1 (4 bit positions and no hiding first 1 as in IEEE 754 as this is not mentioned in question) which in excess-64 will be 64 + 1 = 65. Number being negative sign bit is 1. So, we get

$$(1\ 01111\underbrace{000\ldots0}_{19\text{ zeroes}}\ 1000001)_2 = (BC000041)_{16}$$

b. Largest value will be with largest possible mantissa, largest possible exponent and positive sign bit. So, this will be all 1's except sign bit which will be

$$0.\underbrace{111\ldots1}_{24\text{ ones}} \times 16^{127-64} = \left(1-2^{24}\right) \times 16^{63} = \left(1-2^{-24}\right) \times 16^{63}$$

(Again we did not add implicit 1 as in IEEE 754)

$$2^x = 10^y \implies y = \log 2^x = x \log 2$$

So, $\left(1-2^{-24}\right) \times 16^{63} = \left(1-10^{-24\log 2}\right) \times 10^{63\log 16} \approx \left(1-10^{-7}\right) \times 10^{76} = 10^{76}$

Not directly relevant here, but a useful read: https://jeapostrophe.github.io/courses/2015/fall/305/notes/dist/reading/help-floating-point.pdf

9 votes -- Arjun Suresh (294k points)

4.32.25 Number Representation: GATE2003-9 top

http://gateoverflow.in/900

Selected Answer

MSB of 2's compliment number has a weight of - 2^(n-1).

(Trick: (from reversing sign extension) just skip all leading 1's from MSB expect but 1, and then calculate the value as normal signed binary rep.)

so by calculating, we get the given number is -5 in decimal. and options are

a. -25

b. -28

c. -41

d. -37

Therefore it is clear that - 25 is divisible by - 5. so we can say that (a.) is correct.

6 votes -- Nitin Sharma (1.8k points)

4.32.26 Number Representation: GATE2004-19 top

http://gateoverflow.in/1016

Selected Answer

ans d)

x * 7 + 3 = 5 * y + 4 => 7x = 5y + 1.

Only option satisfying this is D.

8 votes -- Aditi Dan (5.3k points)

4.32.27 Number Representation: GATE2004-28 top

http://gateoverflow.in/1025

Selected Answer

$(113. + -111.) = 1.13 * 10^2 + -1.11 * 10^2 = 0.02 * 10^2 = 2.0 * 10^0$

$2.0 * 10^0 + 7.51 * 10^0 = 9.51 * 10^0$

$(-111. + 7.51) = -1.11 * 10^2 + 7.51 * 10^0 = -1.1 * 10^2 + 0.08 * 10^2 = -1.03 * 10^2$

$113. + -1.03 * 10^2 = 1.13 * 10^2 + -1.03 * 10^2 = 0.1 * 10^2 = 10.0$

Ref: https://www.doc.ic.ac.uk/~eedwards/compsys/float/

20 votes -- Arjun Suresh (294k points)

4.32.28 Number Representation: GATE2004-66 top

http://gateoverflow.in/1060

Selected Answer

A = 1111 1010 = -6
B = 0000 1010 = 10
A*B = -60
=1100 0100

10 votes -- Digvijay (47k points)

4.32.29 Number Representation: GATE2004-IT-42 top

http://gateoverflow.in/3685

Selected Answer

Only (ii) is the answer.

In 2's complement arithmetic, overflow happens only when

1. Sign bit of two input numbers is 0, and the result has sign bit 1
2. Sign bit of two input numbers is 1, and the result has sign bit 0.

Overflow is important only for signed arithmetic while carry is important only for unsigned arithmetic.

A carry happens when there is a carry to (or borrow from) the most significant bit. Here, (i) and (iii) cause a carry but only (ii) causes overflow.

http://teaching.idallen.com/dat2343/10f/notes/040_overflow.txt

13 votes -- Arjun Suresh (294k points)

4.32.30 Number Representation: GATE2004-IT-43 top

http://gateoverflow.in/3686

Selected Answer

$(123456)_8$ = $(001\ 010\ 011\ 100\ 101\ 110)_2$ = $(00\ 1010\ 0111\ 0010\ 1110)_2$ = $(A72E)_{16}$

= $(00\ 10\ 10\ 01\ 11\ 00\ 10\ 11\ 10)_2$ = $(22130232)_4$

So, option (A)

11 votes -- Arjun Suresh (294k points)

4.32.31 Number Representation: GATE2005-16, ISRO2009-18, ISRO2015-2 top

http://gateoverflow.in/1352

Selected Answer

An n-bit two's-complement numeral system can represent every integer in the range $-(2^{n-1})$ to $+(2^{n-1}-1)$.

while ones' complement can only represent integers in the range $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$.

A is answer

8 votes -- kvkumar (4.1k points)

4.32.32 Number Representation: GATE2005-17 top

http://gateoverflow.in/1353

Selected Answer

$657_8 = (110\ 101\ 111)_2 = (1\ [10\ 10]\ [1\ 111])_2 = (1AF)_{16}$

6 votes -- Arjun Suresh (294k points)

4.32.33 Number Representation: GATE2005-IT-47 top

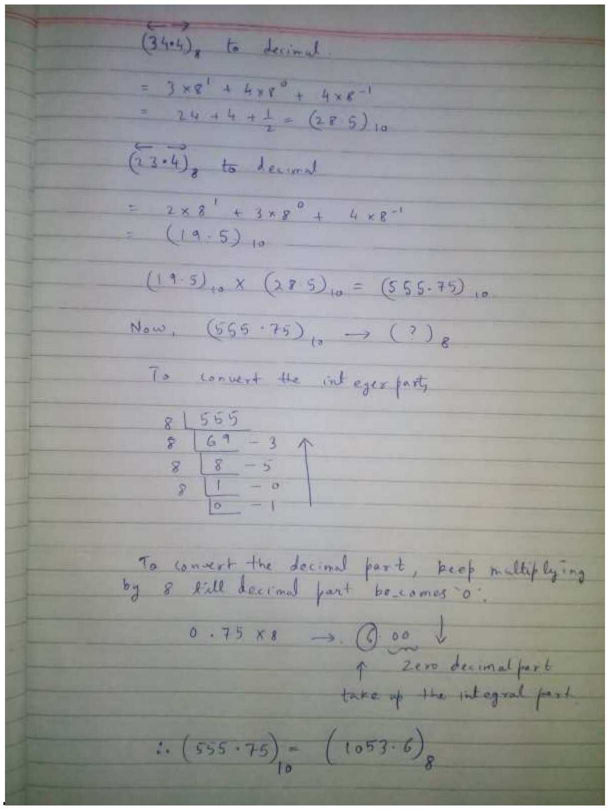
http://gateoverflow.in/3808

Selected Answer

Simply Convert 34.4 and 23.4 to decimal. We can do this by this method :

34.4 = 28.5 in decimal and 23.4 = 19.5 in decimal.

Multiplying 28.5 x 19.5 = 555.75



Now convert 555.75 back to octal which is 1053.6.

12 votes -- Afaque Ahmad (849 points)

4.32.34 Number Representation: GATE2006-39 top

http://gateoverflow.in/1815

Selected Answer

Number representation in 2's complement representation:

- Positive numbers as it is
- Negative numbers in 2's complement form.

So, the overflow conditions are

1. When we add two positive numbers (sign bit 0) and we get a sign bit 1
2. When we add two negative numbers (sign bit 1) and we get sign bit 0
3. **Overflow is relevant only for signed numbers and we use carry for Unsigned numbers**
4. **When the carry out bit and the carry in to the most significant bit differs**

PS: When we add one positive and one negative number we won't get a carry. Also points 1 and 2 is leading to point 4.

Now the question is a bit tricky. It is actually asking the condition of overflow of signed numbers when we use an adder which is meant to work for unsigned numbers.

So, if we see the options, B is the correct one here as the first part takes care of case 2 (negative numbers) and the second part takes care of case 1 (positive numbers) - point 4. We can see a counter example each for other options:

A - Let $n = 4$ and we do $0111 + 0111 = 1110$. This overflows as in $2's$ complement representation we can store only up to 7. But the overflow condition in A returns false as $c_{out} = 0$.

C - This works for the above example. But fails for $1001 + 0001 = 1010$ where there is no actual overflow (-7+1 = -6), but the given condition gives an overflow as $c_{out} = 0$ and $c_{n-1} = 1$.

D - This works for both the above examples, but fails for $1111 + 1111 = 1110$ (-1 + -1 = -2) where there is no actual overflow but the given condition says so.

Ref: http://www.mhhe.com/engcs/electrical/hamacher/5e/graphics/ch02_025-102.pdf

Thanks @Dilpreet for the link and correction.

19 votes -- Digvijay (47k points)

4.32.35 Number Representation: GATE2006-IT-7, ISRO2009-41 top http://gateoverflow.in/3546

Selected Answer

Answer: C

The addition results in 0001 and no overflow with 1 as carry bit.

In 2's complement addition Overflow happens only when :

- Sign bit of two input numbers is 0, and the result has sign bit 1.
- Sign bit of two input numbers is 1, and the result has sign bit 0.

24 votes -- Rajarshi Sarkar (35k points)

4.32.36 Number Representation: GATE2007-IT-42 top http://gateoverflow.in/3477

Selected Answer

$(C012.25)_H$ - $(10111001110.101)_B$

= 1100 0000 0001 0010. 0010 0101
- 0000 0101 1100 1110. 1010 0000

= 1011 1010 0100 0011. 1000 0101

= 1 011 101 001 000 011 . 100 001 010

= $(135103.412)_O$

Binary subtraction is like decimal subtraction: 0-0 = 0, 1-1 = 0, 1-0 = 1, 0-1 = 1 with 1 borrow.

17 votes -- Arjun Suresh (294k points)

4.32.37 Number Representation: GATE2008-6 top http://gateoverflow.in/404

Selected Answer

$\sqrt{(121)_r} = 11_r$

$\sqrt{(1*r^0)+(2*r^1)+(1*r^2)} = (1*r^0)+(1*r^1)$

$\sqrt{(1+r)^2} = 1+r$

$1+r = 1+r$

So any integer r satisfies this but r must be > 2 as we have 2 in 121 and radix must be greater than any of the digits.**(D) is the most appropriate answer**

23 votes -- Keith Kr (6.3k points)

4.32.38 Number Representation: GATE2008-IT-15 top http://gateoverflow.in/3275

Selected Answer

Answer: B

01001101

+ 11101001

100110110

Carry = 1

Overflow = 0 (In 2's complement addition Overflow happens only when : Sign bit of two input numbers is 0, and the result has sign bit 1 OR Sign bit of two input numbers is 1, and the result has sign bit 0.)

Sign bit = 0

15 votes -- Rajarshi Sarkar (35k points)

4.32.39 Number Representation: GATE2009-5, ISRO2017-57 top

http://gateoverflow.in/1297

Selected Answer

$(1217)_8 = (001\ 010\ 001\ 111)_8$
Grouping by 4 bits
$(0010\ 1000\ 1111)_{16} = (28F)_{16}$

Answer is **B.**

13 votes -- Sona Praneeth Akula (4k points)

4.32.40 Number Representation: GATE2010-8 top

http://gateoverflow.in/2179

Selected Answer

Multiplication can be directly carried in 2's complement form. F87B = 1111 1000 0111 1011 can be left shifted 3 times to give 8P = 1100 0011 1101 1000 = C3D8.

Or, we can do as follows:

MSB in (F87B) is 1. So, P is a negative number. So, P = -1 * 2's complement of (F87B) = -1 * (0785) = -1 * (0000 0111 1000 0101)

8 * P = -1 * (0011 1100 0010 1000) (P in binary left shifted 3 times)

In 2's complement representation , this equals, 1100 0011 1101 1000 = C3D8

21 votes -- Arjun Suresh (294k points)

4.32.41 Number Representation: GATE2013_4 top

http://gateoverflow.in/1413

Selected Answer

Range of 2's compliment no = > (- 2^{n-1})to + (2^{n-1} - 1)

Here n = No of bits = 8.

So minimum no = -2 ^ 7 = (B) -128

13 votes -- Akash (43.8k points)

4.32.42 Number Representation: GATE2014-1-8 top

http://gateoverflow.in/1766

Selected Answer

Let 'x' be the base or radix of the number system .

The equation is : $(3.x^2+1.x^1+2.x^0)/(2.x^1+0.x^0)=1.x^1+3.x^0+1.x^{-1}$

$\Rightarrow (3.x^2+x+2)/(2.x)=x+3+1/x$

$\Rightarrow (3.x^2+x+2)/(2.x)=(x^2+3x+1)/x$

By solving above quadratic equation you will get **x=0 and x=5**

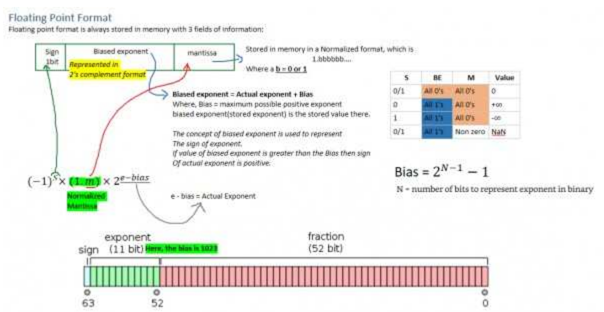
As base or radix of a number system cannot be zero, **here x = 5**

15 votes -- vinodmits (367 points)

4.32.43 Number Representation: GATE2014-2-45 top

http://gateoverflow.in/2011

Selected Answer



14.25 = 1110.01000 = 1.11001000 × 2^3

biased exponent = actual + bias = 3 + bias

where; bias = $2^{8-1}-1$ = 127

biased exponent = 3+127 = 130 = 10000010

Therefore, number represented as = **1 10000010 11001000000000000000000**

on converting to hexadecimal we get = $(C1640000)_{16}$

16 votes -- Amar Vashishth (28.7k points)

4.32.44 Number Representation: GATE2014-2-8 top

http://gateoverflow.in/1961

Selected Answer

Converting both sides to decimal,

25+10+3=x*y+8

So xy=30

Possible pairs are (1,30),(2,15),(3,10) as the minimum base should be greater than 8.

21 votes -- Tejas Jaiswal (661 points)

4.32.45 Number Representation: GATE2015-3_35 top

http://gateoverflow.in/8494

Selected Answer

$$(43)_x = (y3)_8$$

Since a number in base$-k$ can only have digits from 0 to $(k-1)$, we can conclude that: $x \geq 5$ and $y \leq 7$

Now, the original equation, when converted to decimal base gives:

$$\begin{aligned} 4x^1 + 3x^0 &= y(8^1) + 3(8^0) \\ 4x + 3 &= 8y + 3 \\ x &= 2y \end{aligned}$$

So, we have the following constraints:

$$x \geq 5 y \leq 7 x = 2y x, y \text{ are integers}$$

The set of values of (x, y) that satisfy these constraints are:

$$\begin{array}{c} (x\ , y) \\ \hline \\ (6\ , 3) \\ (8\ , 4) \\ (10, 5) \\ (12, 6) \\ (14, 7) \end{array}$$

I am counting 5 pairs of values.

30 votes -- Praveen Saini (53.6k points)

4.32.46 Number Representation: GATE2017-1-9 top http://gateoverflow.in/118289

Selected Answer

Overflow is said to occur in the following cases

c7	c6	Overflow?
0	0	NO
0	1	YES
1	0	YES
1	1	NO

The 3rd condition occurs in the following case A7B7S7', now the question arises how ?

C7	C6
A7	1
B7	1
S7	0

NOW, A7=1 AND B7=1 S7=0 is only possible when C6=0 otherwise s7 would become 1

C7 has to be 1 (1+1+0 generates carry)

ON similar basis we can prove that C7=0 and C6=1 is produced by A7'B7'S7. Hence either of the two conditions cause overflow . Hence ans is C .

Why not A ? when C7=1 and C6 =1 this doesnt indicate overflow (4th row in the table)

Why not B ? if all carry bits are 1 then C7=1 and C6=1 (This also generates 4th row)

Why not D ? These combinations are C0 and C1 , the lower carrys dont indicate overflow

2 votes -- (points)

4.32.47 Number Representation: GATE2017-2-1 top http://gateoverflow.in/118337

Selected Answer

Given: (BCA9)$_{16}$

1011 1100 1010 1001

....for octal number system...grouping of three- three bits from right to left..

1 011 110 010 101 001

1 3 6 2 5 1

Answer: Option D **(1 3 6 2 5 1)$_8$**

6 votes -- Smriti012 (3.1k points)

4.32.48 Number Representation: TIFR2011-A-16 top http://gateoverflow.in/20253

Selected Answer

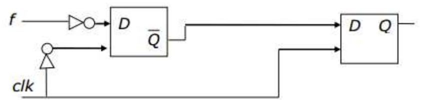
As there are only 13 possible values variable can take, we can use ceil[lg13] = 4 bits. As variable can take only 13 values we don't need to worry what those values are. Answer :- Option D

4 votes -- Akash (43.8k points)

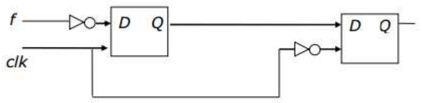
4.33 Phase Shift(1) top

4.33.1 Phase Shift: GATE2006-8 top http://gateoverflow.in/887

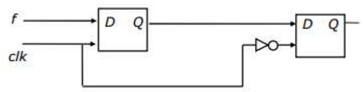
You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of f by 180°?



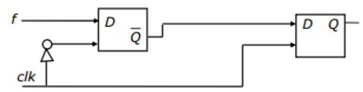
A.



B.



C.



D.

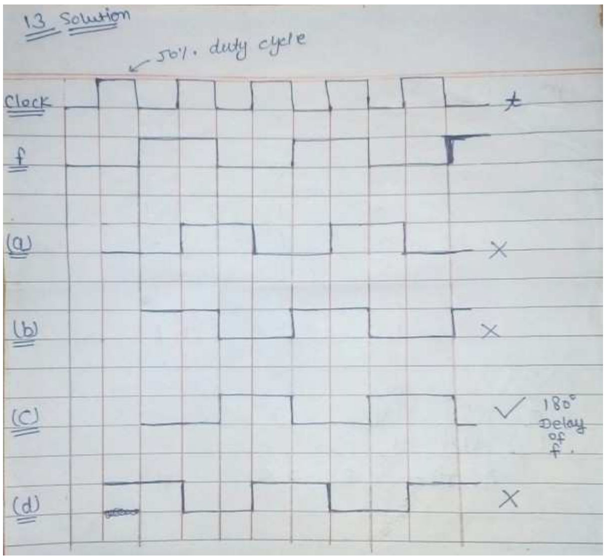
gate2006 digital-logic normal clock-frequency phase-shift

Answer

Answers: Phase Shift

4.33.1 Phase Shift: GATE2006-8 top http://gateoverflow.in/887

Ans- C.



4 votes -- Aaditya Pundir (119 points)

4.34 Prime Implicants(2) top

4.34.1 Prime Implicants: GATE1997-5.1 top http://gateoverflow.in/2252

Let $f(x, y, z) = \bar{x} + \bar{y}x + xz$ be a switching function. Which one of the following is valid?

A. $\bar{y}x$ is a prime implicant of f

B. xz is a minterm of f

C. xz is an implicant of f

D. y is a prime implicant of f

gate1997 digital-logic normal prime-implicants

Answer

4.34.2 Prime Implicants: GATE2004-59 top http://gateoverflow.in/1054

Which are the essential prime implicants of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

A. $a'c$ and ac'
B. $a'c$ and $b'c$
C. $a'c$ only.
D. ac' and bc'

gate2004 digital-logic normal prime-implicants

Answer

Answers: Prime Implicants

4.34.1 Prime Implicants: GATE1997-5.1 top http://gateoverflow.in/2252

Selected Answer

Answer: C

f(x,y,z) = x' + y'x + xz

An implicant of a function is a product term that is included in the function.

so x', y'x and xz ,all are implicants of given function.

A prime implicant of a function is an implicant that is not included in any other implicant of the function.

option a) y'x is not a prime implicant as it is included in xz [**xy'**z+ xyz]

option d) y is not a prime implicant as it include in both x' and xz.

a product term in which all the variables appear is called a ***minterm*** *of the function*

option b) xz is not a minterm

9 votes -- Praveen Saini (53.6k points)

4.34.2 Prime Implicants: GATE2004-59 top http://gateoverflow.in/1054

Selected Answer

answer - A

using K map f = ac' + a'c

8 votes -- ankitrokdeonsns (9.1k points)

4.35 Priority Encoder(1) top

4.35.1 Priority Encoder: GATE1992-4,b top http://gateoverflow.in/31577

A priority encoder accepts three input signals $(A, B$ and $C)$ and produce a two-bit output (X_1, X_0) corresponding to the highest priority active input signal. Assume A has the highest priority followed by B and C has the has the lowest priority. If none of the inputs are active the output should be 00. Design the priority encoder using $4:1$ multiplexers as the main components.

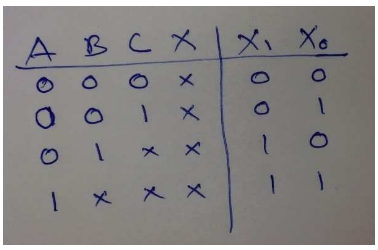
gate1992 digital-logic priority-encoder normal

Answer

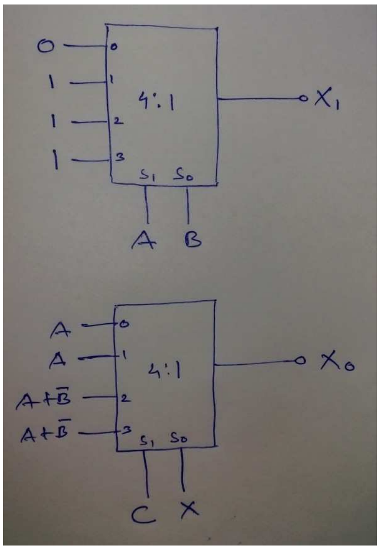
Answers: Priority Encoder

4.35.1 Priority Encoder: GATE1992-4,b top http://gateoverflow.in/31577

We can implement the priority encoder using two 4:1 Multiplexers as main components and 1 NOT gate and 1 OR gate
Using following truth table (Priority encoder with highest priority to A)



A	B	C	X	X_1	X_0
0	0	0	x	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1



3 votes -- Lokesh . (9.8k points)

4.36 Ram(2) top

4.36.1 Ram: GATE2005-IT-9 top http://gateoverflow.in/3754

A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

A. 10
B. 6.4
C. 1
D. 0.64

gate2005-it digital-logic ram normal

Answer

4.36.2 Ram: GATE2010-7 top http://gateoverflow.in/2178

A main memory unit with a capacity of 4 megabytes is built using 1M$\times$ 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

A. 100 nanoseconds
B. 100×2^{10} nanoseconds
C. 100×2^{20} nanoseconds
D. 3200×2^{20} nanosesonds

gate2010 digital-logic ram normal

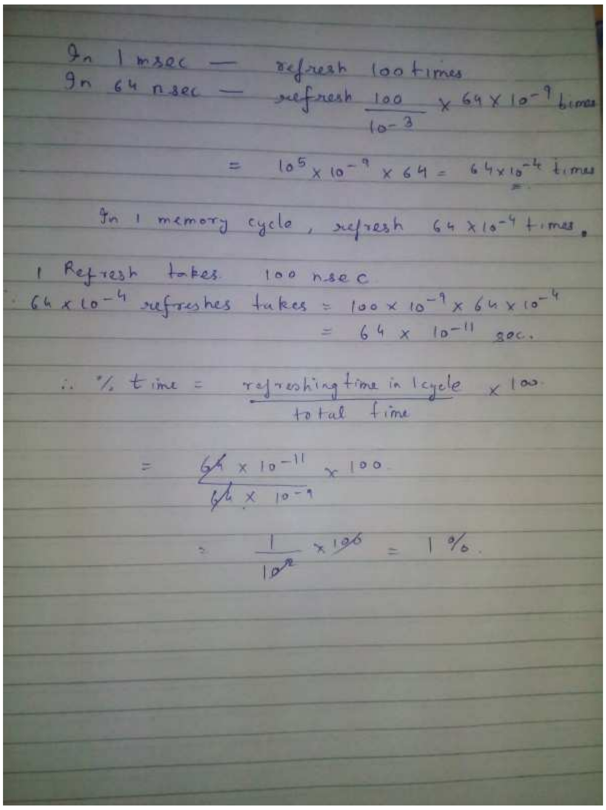
Answer

Answers: Ram

4.36.1 Ram: GATE2005-IT-9 top http://gateoverflow.in/3754

Selected Answer

Ans : C) 1



In 1 msec — refresh 100 times
In 64 nsec — refresh $\frac{100}{10^{-3}} \times 64 \times 10^{-9}$ times
$= 10^5 \times 10^{-9} \times 64 = 64 \times 10^{-4}$ times
In 1 memory cycle, refresh 64×10^{-4} times.
1 Refresh takes 100 nsec
64×10^{-4} refreshes takes $= 100 \times 10^{-9} \times 64 \times 10^{-4}$
$= 64 \times 10^{-11}$ sec.
$\therefore$ % time = $\frac{\text{refreshing time in 1 cycle}}{\text{total time}} \times 100$
$= \frac{64 \times 10^{-11}}{64 \times 10^{-9}} \times 100$
$= \frac{1}{10^2} \times 100 = 1$ %.

16 votes -- Afaque Ahmad (849 points)

4.36.2 Ram: GATE2010-7 top http://gateoverflow.in/2178

Selected Answer

There are 4*8 = 32 DRAM chips to get 4MB from 1M $\times$ 1-bit chips. Now, all chips can be refreshed in parallel so do all cells in a row. So, the total time for refresh will be number of rows times the refresh time

$= 1K \times 100$

$= 100 \times 2^{10}$ nanoseconds

Ref: http://www.downloads.reactivemicro.com/Public/Electronics/DRAM/DRAM%20Refresh.pdf

19 votes -- Arjun Suresh (294k points)

4.37 Rom(4) top

4.37.1 Rom: GATE1993-6.6 top http://gateoverflow.in/2285

A ROM is used to store the Truth table for a binary multiple unit that will multiply two 4-bit numbers. The size of the ROM (number of words $\times$ number of bits) that is required to accommodate the Truth table is $M \text{ words} \times N \text{ bits}$. Write the values of M and N.

gate1993 digital-logic normal rom

Answer

4.37.2 Rom: GATE1996-1.21 top http://gateoverflow.in/2725

A ROM is used to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

A. 256×16
B. $64K \times 8$
C. $4K \times 16$

D. $64K \times 16$

gate1996 digital-logic normal rom

Answer

4.37.3 Rom: GATE2004-IT-10 top

http://gateoverflow.in/3651

What is the minimum size of ROM required to store the complete truth table of an $8-bit \times 8-bit$ multiplier?

A. $32K \times 16$ bits
B. $64K \times 16$ bits
C. $16K \times 32$ bits
D. $64Kx \times 32$ bits

gate2004-it digital-logic normal rom

Answer

4.37.4 Rom: GATE2012-19 top

http://gateoverflow.in/51

The amount of ROM needed to implement a $4-bit$ multiplier is

A. 64 bits
B. 128 bits
C. 1 Kbits
D. 2 Kbits

gate2012 digital-logic normal rom

Answer

Answers: Rom

4.37.1 Rom: GATE1993-6.6 top

http://gateoverflow.in/2285

Selected Answer

A is 4 bit binary no A4A3A2A1

B is 4 bit binary no B4B3B2B1

M is result of multiplication M8M7M6M5M4M3M2M1 [check biggest no 1111 x 1111 =11100001]

A4	A3	A2	A1	B4	B3	B2	B1	M8	M7	M6	M5	M4	M3	M2	M1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1

So 4 bit of A 4 bit of B

input will consist of 8 bit need address 00000000 to 11111111 = 2^8 address

output will be of 8 bits

so memory will be of $2^8 \times 8$

M = 256 , N = 8

5 votes

-- Praveen Saini (53.6k points)

4.37.2 Rom: GATE1996-1.21 top

http://gateoverflow.in/2725

Selected Answer

When we multiply two 8 bit numbers result can go up to 16 bits. So, we need 16 bits for each of the multiplication result. Number of results possible = $2^8 \times 2^8 = 2^{16}$ = 64 K as we need to store all possible results of multiplying two 8 bit numbers. So, 64 K × 16 is the answer.

33 votes -- Arjun Suresh (294k points)

4.37.3 Rom: GATE2004-IT-10 top

http://gateoverflow.in/3651

Selected Answer

answer - B

multiplying 2 8 bit digits will give result in maximum 16 bits

total number of multiplications possible = 2^8 x 2^8

hence space required = 64K x 16 bits

10 votes -- ankitrokdeonsns (9.1k points)

4.37.4 Rom: GATE2012-19 top

http://gateoverflow.in/51

Selected Answer

A ROM cannot be written. So, to implement a 4-bit multiplier we must store all the possible combinations of $2^4 * 2^4$ inputs and their corresponding 8 output bits giving a total of $2^4 * 2^4 * 8$ bits $= 2048$ bits. So, (D) is the answer.

PS: We are not storing the input bits explicitly -- those are considered in order while accessing the output 8 bits. In this way, by storing all the possible outputs in order we can avoid storing the input combinations.

14 votes -- Arjun Suresh (294k points)

4.38 Rs Flip Flop(1) top

4.38.1 Rs Flip Flop: GATE2007-IT-7 top

http://gateoverflow.in/3440

Which of the following input sequences for a cross-coupled R-S flip-flop realized with two NAND gates may lead to an oscillation?

A. 11, 00
B. 01, 10
C. 10, 01
D. 00, 11

gate2007-it digital-logic normal flip-flop rs-flip-flop

Answer

Answers: Rs Flip Flop

4.38.1 Rs Flip Flop: GATE2007-IT-7 top

http://gateoverflow.in/3440

Selected Answer

For R-S flip flop with NAND gates (inputs are active low) 11-no change 00-indeterminate.............so option A may make the system oscillate as "00" is the final input. In option D, after "00" flipflop output may oscillate but after "11", it will be stabilized.

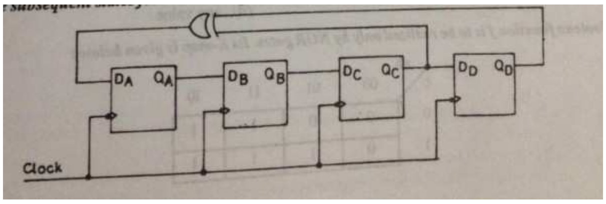
https://en.wikipedia.org/wiki/Flip-flop_(electronics)#SR_NAND_latch

13 votes -- aravind90 (589 points)

4.39 Shift Registers(1) top

4.39.1 Shift Registers: GATE1987-13a top http://gateoverflow.in/82607

The below figure shows four D-type flip-flops connnected as a shift register using an XOR gate. The initial state and three subsequent states for three clock pulses are also given.



State	Q_A	Q_B	Q_C	Q_D
Initial	1	1	1	1
After the first clock	0	1	1	1
After the second clock	0	0	1	1
After the third clock	0	0	0	1

The state $Q_AQ_BQ_CQ_D$ after the fourth clock pulse is

A. 0000
B. 1111
C. 1001
D. 1000

gate1987 digital-logic circuit-output shift-registers

Answer

Answers: Shift Registers

4.39.1 Shift Registers: GATE1987-13a top http://gateoverflow.in/82607

Selected Answer

Option D) **1000**

$Q_{AN} = Q_C \oplus Q_D$, $Q_{BN} = Q_A$, $Q_{CN} = Q_B$ and $Q_{DN} = Q_C$

Q_A	QB	QC	QD
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	**0**	**0**	**0**

2 votes -- Prajwal Bhat (11.9k points)

4.40 Static Hazard(1) top

4.40.1 Static Hazard: GATE2006-38 top http://gateoverflow.in/1814

Consider a Boolean function $f(w, x, y, z)$. Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1 = \langle w_1, x_1, y_1, z_1 \rangle$ and $i_2 = \langle w_2, x_2, y_2, z_2 \rangle$, we would like the function to remain true as the input changes from i_1 to i_2 (i_1 and i_2 differ in exactly one bit position) without becoming false momentarily. Let $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$. Which of the following cube covers of f will ensure that the required property is satisfied?

A. $\overline{w}xz, wx\overline{y}, x\overline{y}z, xyz, wyz$
B. $wxy, \overline{w}xz, wyz$
C. $wx\overline{y}\overline{z}, xz, w\overline{x}yz$
D. $wx\overline{y}, wyz, wxz, \overline{w}xz, x\overline{y}z, xyz$

gate2006 digital-logic min-sum-of-products-form normal static-hazard

Answer

Answers: Static Hazard

4.40.1 Static Hazard: GATE2006-38 top http://gateoverflow.in/1814

Selected Answer

The question is indirctly asking for static hazard in the circuit - that is output becoming 1 momentarily when it is supposed to be 0 or vice verse.

Here $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$

So, K-map will be

	y'z'	y'z	yz	yz'
w'x'				
w'x		5	7	
wx	12	**13**	**15**	
wx'			11	

So, its minimized sum of products expression will be $xz + wxy + w'yz$. Since all the minterms are overlapping, there is no chance of static hazard here.

Now, lets consider the options one by one:

A. $\overline{w}xz, wx\overline{y}, x\overline{y}z, xyz, wyz$

	y'z'	y'z	yz	yz'
w'x'				
w'x		5	7	
wx	12	13	15	
wx'			11	

Chance of static hazard

Here, when y changes from 0 to 1, the GATE for wyz should give 1 (from earlier 0, assuming $w = z = 1$) and that of $wy'z$ should give 0 (from earlier 1). But there is a possibility of circuit giving 0 (static 1 hazard) momentarilly due to gate delays. In order to avoid this, we must add a gate with wxz also which ensures all adjacent blocks in K-map are overlapped.

We can also have the sum of products as $xy'z + w'yz + wxy$ which is of course not minimal. But this also has hazard as when w changes from 0 to 1, the GATE for wxy should give 1 (from earlier 0) and that of $w'yz$ should give 0 (from earlier 1). But there is a possibility of circuit giving 0 momentarilly (assuming $x = 0$). This hazard can be avoided by adding xyz

and similarly we need $w'xz$ and wxz. Thus we get $xy'z + w'yz + wxy + xyz + w'xz + wxz$

Now, each of these term will correspond to a GATE when the circuit is implemented. What we require is to avoid the output to change when any of the input literal changes its value (hazard).

B. $\overline{w}xz, wx\overline{y}, x\overline{y}z, xyz, wyz$

	y'z'	y'z	yz	yz'
w'x'				
w'x		5	7	
wx	12	13	15	
wx'			11	

Chance of static hazard

Here, when y changes from 0 to 1, the GATE for wyz should give 1 (from earlier 0, assuming $w = z = 1$) and that of $wy'z$ should give 0 (from earlier 1). But there is a possibility of circuit giving 0 (static 1 hazard) momentarilly due to gate delays. In order to avoid this, we must add a gate with wxz also which ensures all adjacent blocks in K-map are overlapped.

We can also have the sum of products as $xy'z + w'yz + wxy$ which is of course not minimal. But this also has hazard as when w changes from 0 to 1, the GATE for wxy should give 1 (from earlier 0) and that of $w'yz$ should give 0 (from earlier 1). But there is a possibility of circuit giving 0 momentarily (assuming $x = 0$). This hazard can be avoided by adding xyz and similarly we need $w'xz$ and wxz. Thus we get $xy'z + w'yz + wxy + xyz + w'xz + wxz$

Now, each of these term will correspond to a GATE when the circuit is implemented. What we require is to avoid the output to change when any of the input literal changes its value (hazard).

B. $wxy, \overline{w}xz, wyz$

Is not correct as wxy is not a minterm for the given function

C. $wx\overline{y}\overline{z}, xz, w\overline{x}yz$

	y'z'	y'z	yz	yz'
w'x'				
w'x		5	7	
wx	**12**	13	15	
wx'			**11**	

Here, also there are hazards possible as the middle 4 pairs are separated by 1 bit difference to both $wxy'z'$ as well as $wx'yz$. Could have been avoided by using wxy' instead of $wxy'z'$ and wyz instead of $wx'yz$ which ensures all neighbouring blocks are overlapped.

D. $wx\overline{y}, wyz, wxz, \overline{w}xz, x\overline{y}z, xyz$

These minterms cover all the minterms of f and also, all the neighbouring blocks are overlapping. So, no chance of hazard here and hence is the required answer.

8 votes -- sonam vyas (13.2k points)

4.41 Synchronous Asynchronous Circuits(1) top

4.41.1 Synchronous Asynchronous Circuits: GATE1991-03,ii top http://gateoverflow.in/516

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

(ii). Advantage of synchronous sequential circuits over asynchronous ones is:

a. faster operation
b. ease of avoiding problems due to hazards
c. lower hardware requirement
d. better noise immunity
e. none of the above

gate1991 digital-logic normal synchronous-asynchronous-circuits

Answer

Answers: Synchronous Asynchronous Circuits

4.41.1 Synchronous Asynchronous Circuits: GATE1991-03,ii top http://gateoverflow.in/516

Selected Answer

Synchronization means less chance of hazards but can only increase the delay. So, synchronous circuits cannot have faster operation than asynchronous one but it is easier to avoid hazards in synchronous circuits. So, (a) is false and (b) is true.

(c) is false if we don't consider how to avoid the hazards in asynchronous circuits.

(d) Is not necessarily true - often asynchronous circuits have better noise immunity. Reasons are given here: http://www.cs.columbia.edu/~nowick/async-applications-PIEEE-99-berkel-josephs-nowick-published.pdf

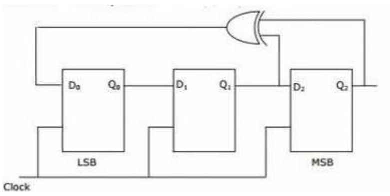
https://en.wikipedia.org/wiki/Asynchronous_circuit

8 votes -- Arjun Suresh (294k points)

4.42 Synchronous Circuit(1) top

4.42.1 Synchronous Circuit: GATE2001-2.12 top http://gateoverflow.in/730

Consider the circuit given below with initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$



Which one of the following is correct state sequence of the circuit?

A. 1, 3, 4, 6, 7, 5, 2
B. 1, 2, 5, 3, 7, 6, 4
C. 1, 2, 7, 3, 5, 6, 4
D. 1, 6, 5, 7, 2, 3, 4

gate2001 digital-logic normal synchronous-circuit

Answer

Answers: Synchronous Circuit

4.42.1 Synchronous Circuit: GATE2001-2.12 top http://gateoverflow.in/730

Selected Answer

Q_0 = Q_{1prev} ⊕ Q_{2prev}	Q_1 = Q_{0prev}	Q_2 = Q_{1prev}
1	0	0
0	1	0
1	0	1
1	1	0
1	1	1

$Q_0 = Q_{1prev} \oplus Q_{2prev}$	$Q_1 = Q_{0prev}$	$Q_2 = Q_{1prev}$
0	1	1
0	0	1
1	0	0

State = $4Q_2 + 2Q_1 + Q_0$
So, state sequence = 1, 2, 5, 3, 7, 6, 4

15 votes -- Arjun Suresh (294k points)

4.43 Synchronous Counter(1) top

4.43.1 Synchronous Counter: GATE1998-16 top http://gateoverflow.in/1730

Design a synchronous counter to go through the following states:

$$1, 4, 2, 3, 1, 4, 2, 3, 1, 4 \ldots$$

gate1998 digital-logic normal descriptive synchronous-counter

Answer

Answers: Synchronous Counter

4.43.1 Synchronous Counter: GATE1998-16 top http://gateoverflow.in/1730

Selected Answer

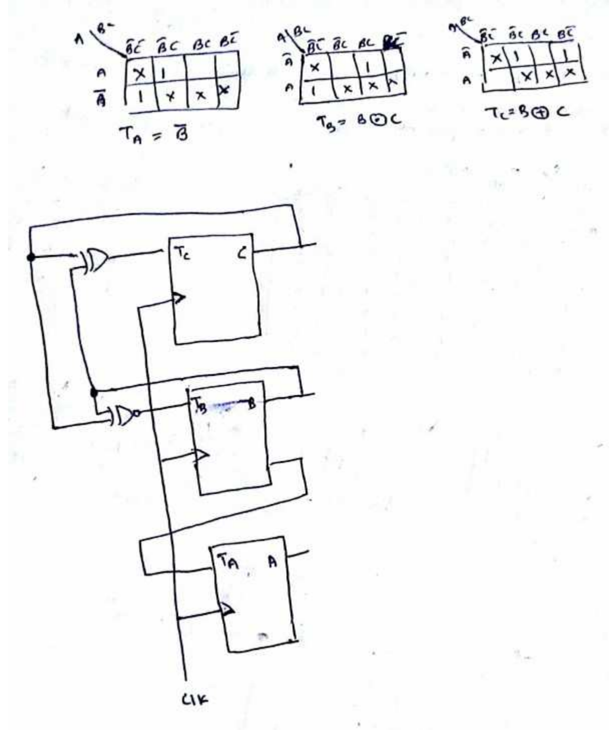
Sequence Given is as

$1, 4, 2, 3, 1......$

From the given sequence of states we can design the state table and Suppose we are using T-FF for sequential circuit of counter.

Present state			Next State			FF Inputs		
A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	x	x	x	x	x	x
0	0	1	1	0	0	1	0	1
0	1	0	0	1	1	0	0	1
0	1	1	0	0	1	0	1	0
1	0	0	0	1	0	1	1	0
1	0	1	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

From the above table , we will find the equation of T_A, T_B and T_C



8 votes -- Praveen Saini (53.6k points)

4.44 Xor(1) top

4.44.1 Xor: GATE1998-1.13 top http://gateoverflow.in/1650

What happens when a bit-string is XORed with itself n-times as shown:

$[B \oplus (B \oplus (B \oplus (B \dots n \text{ times}]$

A. complements when n is even

B. complements when n is odd

C. divides by 2^n always

D. remains unchanged when n is even

gate1998 digital-logic normal boolean-operations xor

Answer

Answers: Xor

4.44.1 Xor: GATE1998-1.13 top http://gateoverflow.in/1650

Selected Answer

It should be D.

Let number of ⊕ be two (even case):

B ⊕ B ⊕ B = B ⊕ 0 = B (remains unchanged)

Let number of ⊕ be three (odd case):

B ⊕ B ⊕ B ⊕ B = B ⊕ B ⊕ 0 = B ⊕ B = 0 (gives 0)

13 votes -- Rajarshi Sarkar (35k points)

5 Operating System (280) top

5.1 Computer Peripherals(1) top

5.1.1 Computer Peripherals: GATE1992_02,xii top

http://gateoverflow.in/569

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

Which of the following is an example of a spooled device?

(a). The terminal used to input data for a program being executed.

(b). The secondary memory device in a virtual memory system

(c). A line printer used to print the output of a number of jobs.

(d). None of the above.

gate1992 operating-system computer-peripherals easy

Answer

Answers: Computer Peripherals

5.1.1 Computer Peripherals: GATE1992_02,xii top

http://gateoverflow.in/569

Selected Answer

Answer: C

Spool stands for simultaneous peripheral operations on-line.

10 votes -- Rajarshi Sarkar (35k points)

5.2 Concurrency(3) top

5.2.1 Concurrency: CMI2012-A-10 top

http://gateoverflow.in/46540

Consider the following functions f and g.

f(){	g( ) {
x = x-50;	a = a+x;
y = y+50;	a = a+y;
}	}

Suppose we start with initial values of 100 for x, 200 for y, and 0 for a, and then execute f and g in parallel—that is, at each step we either execute one statement from f or one statement from g. Which of the following is not a possible final value of a?

A. 300
B. 250
C. 350
D. 200

cmi2012 operating-system concurrency

Answer

5.2.2 Concurrency: GATE2015-1_9 top

http://gateoverflow.in/8121

The following two functions P1 and P2 that share a variable B with an initial value of 2 execute concurrently.

```
P1() {
    C = B - 1;
    B = 2 * C;
}
```

```
P2(){
    D = 2 * B;
    B = D - 1;
}
```

The number of distinct values that B can possibly take after the execution is________________________.

gate2015-1 operating-system concurrency normal numerical-answers

Answer

5.2.3 Concurrency: TIFR2012-B-9 top

http://gateoverflow.in/25109

Consider the concurrent program

```
x := 1;
cobegin
    x := x + x + 1 || x := x + 2
coend;
```

Reading and writing of a variable is atomic, but evaluation of an expression is not atomic. The set of possible values of variable x at the end of execution of the program is

a. $\{3\}$
b. $\{7\}$
c. $\{3, 5, 7\}$
d. $\{3, 7\}$
e. $\{3, 5\}$

tifr2012 concurrency

Answer

Answers: Concurrency

5.2.1 Concurrency: CMI2012-A-10 top

http://gateoverflow.in/46540

Selected Answer

Ans D) 200

if we execute first f() and then g() then we get 300

if we execute1st line of g() , then f() all the lines and then last line of g() ,will get 350

if we execute 1st line of f(), then 1st line of g(), then 2nd line of g() , and then 2nd line of f(), we get 250

4 votes -- srestha (58.4k points)

5.2.2 Concurrency: GATE2015-1_9 top

http://gateoverflow.in/8121

Selected Answer

3 distinct value (2,3,4)

P1-P2: B = 3
P2-P1: B = 4
P1-P2-P1: B = 2

18 votes -- Anoop Sonkar (4.9k points)

5.2.3 Concurrency: TIFR2012-B-9 top http://gateoverflow.in/25109

Selected Answer

1. x = 1, Run x = x + 2 then x= x + x + 1 finally x will be 7.
2. x = 1, run x = x + 2 and x = x + x + 1, parallely ..
x = 5 , 3
Final answer would be {3, 5, 7}

7 votes -- Digvijay (47k points)

5.3 Context Switch(3) top

5.3.1 Context Switch: GATE1999_2.12 top http://gateoverflow.in/1490

Which of the following actions is/are typically not performed by the operating system when switching context from process A to process B?

A. Saving current register values and restoring saved register values for process B.
B. Changing address translation tables.
C. Swapping out the memory image of process A to the disk.
D. Invalidating the translation look-aside buffer.

gate1999 operating-system context-switch normal

Answer

5.3.2 Context Switch: GATE2000-1.20, ISRO2008-47 top http://gateoverflow.in/644

Which of the following need not necessarily be saved on a context switch between processes?

A. General purpose registers
B. Translation look-aside buffer
C. Program counter
D. All of the above

gate2000 operating-system easy isro2008 context-switch

Answer

5.3.3 Context Switch: GATE2011-6, UGCNET-June2013-III-62 top http://gateoverflow.in/2108

Let the time taken to switch from user mode to kernel mode of execution be T1 while time taken to switch between two user processes be T2. Which of the following is correct?

A. T1 > T2
B. T1 = T2
C. T1 < T2
D. Nothing can be said about the relation between T1 and T2

gate2011 operating-system context-switch easy ugcnetjune2013iii

Answer

Answers: Context Switch

5.3.1 Context Switch: GATE1999_2.12 top http://gateoverflow.in/1490

Selected Answer

option C) because swapping out of the memory image of a process to disk is not done on every context switch as it would cause a huge over head but can solve problems like trashing.

24 votes -- GateMaster Prime (1.6k points)

The above answer covers most of the things. Trying to add some more points to make it clear for people like me for those it is quite difficult to understand.

Processes are generally swapped out from memory to Disk (secondary memory) when they are suspended. SoProcesses are not swapped during context switching.

TLB : Whenever any page table entry is referred for the first time it is temporarily saved in TLB. Every element of this memory has a tag. And whenever anything is searched it is compared against TLB and we can get that entry/data with less memory access.

And Invalidation of TLB means resetting TLB which is necessary because A TLB entry may belong to any page table of any process thus resetting ensures that the entry corresponds to the process that we are searching for.

Hence Option (C) is correct.

20 votes -- Manish Joshi (25.2k points)

5.3.2 Context Switch: GATE2000-1.20, ISRO2008-47 top http://gateoverflow.in/644

Selected Answer

Answer: B

We don't need to save TLB or cache to ensure correct program resumption. They are just bonus for ensuring better performance. But PC, stack and registers must be saved as otherwise program cannot resume.

20 votes -- Rajarshi Sarkar (35k points)

5.3.3 Context Switch: GATE2011-6, UGCNET-June2013-III-62 top http://gateoverflow.in/2108

Selected Answer

Time taken to switch two processes is very large as compared to time taken to switch between kernel and user mode of execution because :

When you switch processes, you have to do a context switch, save the PCB of previous process (note that the PCB of a process in Linux has over 95 entries), then save registers and then load the PCB of new process and load its registers etc.

When you switch between kernel and user mode of execution, OS has to just ***change a single bit*** at hardware level which is very fast operation.

So answer is : C

37 votes -- Mojo Jojo (4.2k points)

Context switches can occur only in kernel mode. So, to do context switch first switch from user mode to kernel mode and then do context switch (save the PCB of the previous process and load the PCB of new process)

Context switch = user - kernel switch + save/load PCB + kernel-user switch

C is answer.

17 votes -- Sachin Mittal (7.1k points)

5.4 Critical Section(1) top

5.4.1 Critical Section: GATE1987-1-xvi top http://gateoverflow.in/80362

A critical region is

A. One which is enclosed by a pair of P and V operations on semaphores.
B. A program segment that has not been proved bug-free.
C. A program segment that often causes unexpected system crashes.
D. A program segment where shared resources are accessed.

gate1987 operating-system process-synchronization critical-section

Answer

Answers: Critical Section

5.4.1 Critical Section: GATE1987-1-xvi top

http://gateoverflow.in/80362

Selected Answer

A critical region is a program segment where shared resources are accessed.. that's why we synchronize in the critical section. That is D.

PS: It is not necessary that we must use semaphore for critical section access (any other mechanism for mutual exclusion can also be used) and neither do sections enclosed by P and V operations are called critical sections.

7 votes -- kirti singh (3.4k points)

5.5 Dining Philosopher(1) top

5.5.1 Dining Philosopher: TIFR2011-B-26 top

http://gateoverflow.in/20572

Consider the following two scenarios in the dining philosophers problem:

i. First a philosopher has to enter a room with the table that restricts the number of philosophers to four.
ii. There is no restriction on the number of philosophers entering the room.

Which of the following is true?

a. Deadlock is possible in (i) and (ii).
b. Deadlock is possible in (i).
c. Starvation is possible in (i).
d. Deadlock is not possible in (ii).
e. Starvation is not possible in (ii)

tifr2011 operating-system process-synchronization dining-philosopher

Answer

Answers: Dining Philosopher

5.5.1 Dining Philosopher: TIFR2011-B-26 top

http://gateoverflow.in/20572

Selected Answer

There deadlock may possible or may not possible but it is sure that Starvation possible in case of (i)

option C is definite from 1st case hence it is True only.

1 votes -- Bikram (44.7k points)

5.6 Disk Scheduling(13) top

5.6.1 Disk Scheduling: GATE 2016-1-48 top

http://gateoverflow.in/39716

Cylinder a disk queue with requests for I/O to blocks on cylinders $47, 38, 121, 191, 87, 11, 92, 10.$ The C-LOOK scheduling algorithm is used. The head is initially at cylinder number $63,$ moving towards larger cylinder numbers on its servicing pass. The cylinders are numbered from 0 to 199. The total head movement (in number of cylinders) incurred while servicing these requests is___________.

gate2016-1 operating-system disk-scheduling normal numerical-answers

Answer

5.6.2 Disk Scheduling: GATE1989-4-xii top http://gateoverflow.in/88222

Provide short answers to the following questions:

Disk requests come to disk driver for cylinders $10, 22, 20, 2, 40, 6$ and 38, in that order at a time when the disk drive is reading from cylinder 20. The seek time is 6 msec per cylinder. Compute the total seek time if the disk arm scheduling algorithm is.

A. First come first served.
B. Closest cylinder next.

gate1989 descriptive operating-system disk-scheduling

Answer

5.6.3 Disk Scheduling: GATE1995_20 top http://gateoverflow.in/2658

The head of a moving head disk with 100 tracks numbered 0 to 99 is currently serving a request at track 55. If the queue of requests kept in FIFO order is

10, 70, 75, 23, 65

which of the two disk scheduling algorithms FCFS (First Come First Served) and SSTF (Shortest Seek Time First) will require less head movement? Find the head movement for each of the algorithms.

gate1995 operating-system disk-scheduling normal

Answer

5.6.4 Disk Scheduling: GATE1997-3.6 top http://gateoverflow.in/2237

The correct matching for the following pairs is:

(A) Disk Scheduling	(1) Round robin
(B) Batch Processing	(2) SCAN
(C) Time sharing	(3) LIFO
(D) Interrupt processing	(4) FIFO

A. A-3 B-4 C-2 D-1

B. A-4 B-3 C-2 D-1

C. A-2 B-4 C-1 D-3

D. A-3 B-4 C-3 D-2

gate1997 operating-system normal disk-scheduling interrupts

Answer

5.6.5 Disk Scheduling: GATE1999_1.10 top http://gateoverflow.in/1463

Which of the following disk scheduling strategies is likely to give the best throughput?

A. Farthest cylinder next

B. Nearest cylinder next

C. First come first served

D. Elevator algorithm

gate1999 operating-system disk-scheduling normal

Answer

5.6.6 Disk Scheduling: GATE2004-12 top http://gateoverflow.in/1009

Consider an operating system capable of loading and executing a single sequential user process at a time. The disk head scheduling algorithm used is First Come First Served (FCFS). If FCFS is replaced by Shortest Seek Time First (SSTF), claimed by the vendor to give 50% better benchmark results, what is the expected improvement in the I/O performance of user programs?

A. 50%
B. 40%
C. 25%
D. 0%

gate2004 operating-system disk-scheduling normal

Answer

5.6.7 Disk Scheduling: GATE2004-IT-62 top http://gateoverflow.in/3705

A disk has 200 tracks (numbered 0 through 199). At a given time, it was servicing the request of reading data from track 120, and at the previous request, service was for track 90. The pending requests (in order of their arrival) are for track numbers.

30 70 115 130 110 80 20 25.

How many times will the head change its direction for the disk scheduling policies SSTF(Shortest Seek Time First) and FCFS (First Come Fist Serve)?

A. 2 and 3
B. 3 and 3
C. 3 and 4
D. 4 and 4

gate2004-it operating-system disk-scheduling normal

Answer

5.6.8 Disk Scheduling: GATE2007-IT-82 top http://gateoverflow.in/3534

The head of a hard disk serves requests following the shortest seek time first (SSTF) policy. The head is initially positioned at truck number 180.

Which of the request sets will cause the head to change its direction after servicing every request assuming that the head does not change direction if there is a tie in SSTF and all the requests arrive before the servicing starts?

A. 11, 139, 170, 178, 181, 184, 201, 265
B. 10, 138, 170, 178, 181, 185, 201, 265
C. 10, 139, 169, 178, 181, 184, 201, 265
D. 10, 138, 170, 178, 181, 185, 200, 265

gate2007-it operating-system disk-scheduling normal

Answer

5.6.9 Disk Scheduling: GATE2007-IT-83 top http://gateoverflow.in/3535

The head of a hard disk serves requests following the shortest seek time first (SSTF) policy. The head is initially positioned at track number 180.

What is the maximum cardinality of the request set, so that the head changes its direction after servicing every request if the total number of tracks are 2048 and the head can start from any track?

A. 9
B. 10
C. 11
D. 12

gate2007-it operating-system disk-scheduling normal

Answer

5.6.10 Disk Scheduling: GATE2009-31 top

http://gateoverflow.in/1317

Consider a disk system with 100 cylinders. The requests to access the cylinders occur in following sequence:

4, 34, 10, 7, 19, 73, 2, 15, 6, 20

Assuming that the head is currently at cylinder 50, what is the time taken to satisfy all requests if it takes 1ms to move from one cylinder to adjacent one and shortest seek time first policy is used?

A. 95 ms
B. 119 ms
C. 233 ms
D. 276 ms

gate2009 operating-system disk-scheduling normal

Answer

5.6.11 Disk Scheduling: GATE2010-24 top

http://gateoverflow.in/2203

A system uses FIFO policy for system replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?

A. 196
B. 192
C. 197
D. 195

gate2010 operating-system disk-scheduling normal

Answer

5.6.12 Disk Scheduling: GATE2014-1-19 top

http://gateoverflow.in/1786

Suppose a disk has 201 cylinders, numbered from 0 to 200. At some time the disk arm is at cylinder 100, and there is a queue of disk access requests for cylinders 30, 85, 90, 100, 105, 110, 135 and 145. If Shortest-Seek Time First (SSTF) is being used for scheduling the disk access, the request for cylinder 90 is serviced after servicing ______________ number of requests.

gate2014-1 operating-system disk-scheduling numerical-answers normal

Answer

5.6.13 Disk Scheduling: GATE2015-1_30 top

http://gateoverflow.in/8227

Suppose the following disk request sequence (track numbers) for a disk with 100 tracks is given:

45, 20, 90, 10, 50, 60, 80, 25, 70.

Assume that the initial position of the R/W head is on track 50. The additional distance that will be traversed by the R/W head when the Shortest Seek Time First (SSTF) algorithm is used compared to the SCAN (Elevator) algorithm (assuming that SCAN algorithm moves towards 100 when it starts execution) is_________________tracks.

gate2015-1 operating-system disk-scheduling normal numerical-answers

Answer

Answers: Disk Scheduling

5.6.1 Disk Scheduling: GATE 2016-1-48 top

http://gateoverflow.in/39716

Selected Answer

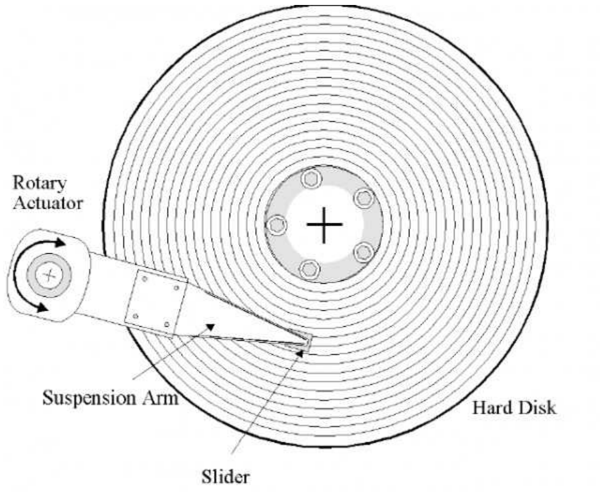
63->191 = 128

191->10 = 181
10->47 = 37
Total = 346

29 votes -- Abhilash Panicker (8.8k points)

Answer is 346 as already calculated in answers here.Those having some doubt regarding long jump ,check this image, Now in question Total Head Movements are asked,When Head reaches any End, **There is no mechanism for head to jump directly to some arbitrary track.It has to Move.So it has to move along the tracks to reach Track Request on other side.Therefore head will move and we must count it.**

since purpose of disk scheduling algorithms is to reduce such Head movements by finding an Optimal algorithm.If you ignore the move which is actually happening in disk,that doesn't serve the purpose of analyzing the algorithms.



13 votes -- Anurag Semwal (8k points)

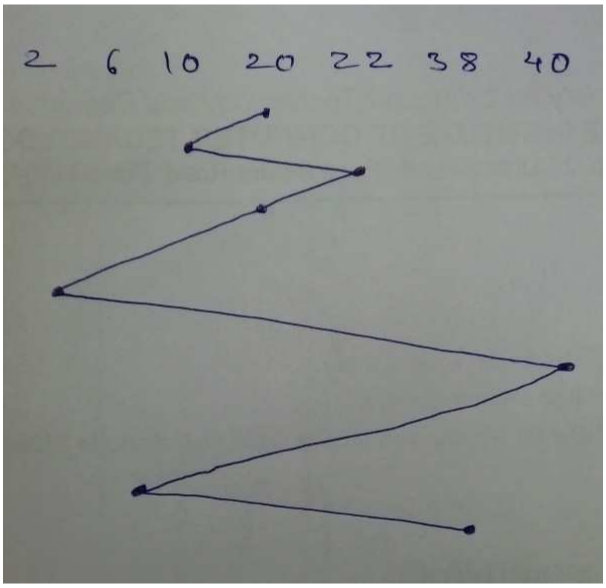
5.6.2 Disk Scheduling: GATE1989-4-xii top

http://gateoverflow.in/88222

Selected Answer

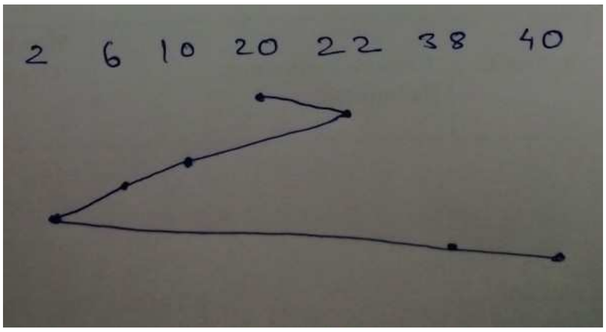
A) In **FCFS** sequence will be ==> 20, 10, 22, 20, 2, 40, 6, 38

total movement: |20-10| + |10-22| + |22-20| + |20-2| + |2-40| + |40-6| + |6-38| = 146
so total seek time = 146 * 6 = **876 msec**



B) In **Closest cylinder next** sequence will be ==> 20, 22, 10, 6, 2, 38, 40

total movement: |20-22| + |22-2| + |2-40| = 60
so total seek time = 60 * 6 = **360 msec**



6 votes -- Lokesh . (9.8k points)

5.6.3 Disk Scheduling: GATE1995_20 top http://gateoverflow.in/2658

Selected Answer

FCS:55->10->70->75->23->65 => 45+60+5+52+42=204.

SSTF:55->65->70->75->23->10 => 10+5+5+52+13=85

Hence SSTF.

13 votes -- kireeti (1.1k points)

5.6.4 Disk Scheduling: GATE1997-3.6 top http://gateoverflow.in/2237

Selected Answer

c is answer. interrupt processing is LIFO because when we are processing an interrupt, we disable the interrupts originating from lower priority devices so lower priority interrupts can not be raised. if an interrupt is detected then it means that it has higher priority than currently executing interrupt so this new interrupt will preempt the current interrupt so LIFO. other matches are easy.cheers.

9 votes -- ashish gusai (359 points)

5.6.5 Disk Scheduling: GATE1999_1.10 top http://gateoverflow.in/1463

Selected Answer

Farthest cylinder next -> This might be candidate for worst algorithm . This is false.

First come first served -> This will not give best throughput. It is random .

Elevator algorithm -> This is good but issue is that once direction is fixed we don't come back, until we go all the other way. So it does not give best throughput.

B) Nearest cylinder next -> This is output.

7 votes -- Akash (43.8k points)

5.6.6 Disk Scheduling: GATE2004-12 top http://gateoverflow.in/1009

Selected Answer

Question says "single sequential user process". So, all the requests to disk scheduler will be in sequence and each one will be blocking the execution and hence there is no use of any disk scheduling algorithm. Any disk scheduling algorithm gives the same input sequence and hence the improvement will be 0% for SSTF over FCFS.

30 votes -- Arjun Suresh (294k points)

5.6.7 Disk Scheduling: GATE2004-IT-62 top http://gateoverflow.in/3705

Selected Answer

Answer is (C)

SSTF: (90) 120 115 110 130 80 70 30 25 20

Direction changes at 120,110,130

FCFS: (90) 120 30 70 115 130 110 80 20 25

direction changes at 120,30,130,20

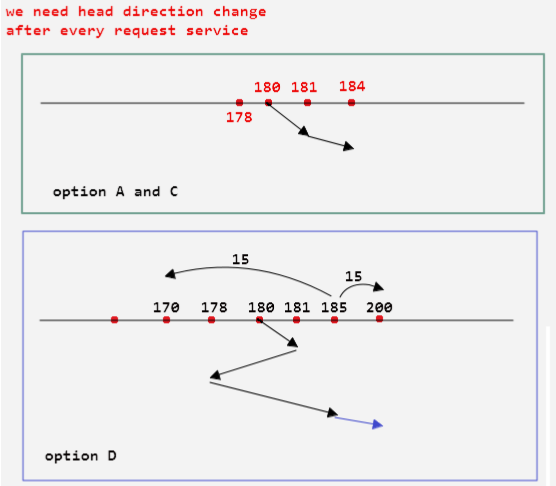
14 votes -- Sandeep_Uniyal (7.3k points)

5.6.8 Disk Scheduling: GATE2007-IT-82 top http://gateoverflow.in/3534

Selected Answer

It should be B.

When the head starts from 180... it seeks the nearest track.. which is 181. Then from 181 it seeks the nearest one which is 178 and 184. But the difference in both from 181 is same and as given in the question... if there is a tie then the head wont change its direction, and therefore to change the direction we need to consider 178. and thus we can eliminate option A and C.



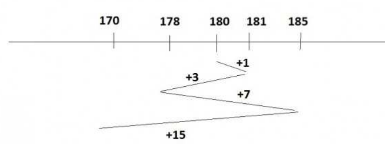
Coming next to option B and D.. following the above procedure you'll see that option D is eliminated on similar ground. And thus you can say option B is correct.

12 votes -- Gate Keeda (19.1k points)

5.6.9 Disk Scheduling: GATE2007-IT-83 top

http://gateoverflow.in/3535

Selected Answer



Here Head is changing it's direction after servicing every request.

Now, we can see distance of SSTF changing like 1,3,7,15,31,63,127,255,511,1023,2047

So, maximum cardinality will be 11.

16 votes -- srestha (58.4k points)

10,138,170,178,180,181,185,201,265,521 should be sequence of access if head is at 180 th track...

Let suppose head is at 512th

So sequence should be ..

171,427,491,507,511,512,514,522,554,684,1194

So ans should be 11...

If same type of question has been asked ...I think we can do it directly... 2028 =2^11..so 11 is the ans...with the condition head can start from any point...

11 votes -- papesh (24.1k points)

5.6.10 Disk Scheduling: GATE2009-31 top

http://gateoverflow.in/1317

Selected Answer

Answer is **B.**

$$= (50-34)+(34-20)+(20-19)+(19-15)+(15-10)+(10-7)+(7-6)+(6-4)+(4-2)+(73-2)$$
$$= 16+14+1+4+5+3+1+2+2+71$$
$$= 119 \text{ ms.}$$

6 votes -- Sona Praneeth Akula (4k points)

Here in case of Shortest seek time first we don't need to do lot of substraction & addition in this type of questions. It seems like it is necessary to actually calculate small differences ! It is better to just draw actual movement & Then do computation.

Here sequence is like

50->34->20->19->15->7->4->2->73

So we can calculate like (50-2) + (73-2) = 71+48 = 119.

10 votes -- Akash (43.8k points)

5.6.11 Disk Scheduling: GATE2010-24 top

http://gateoverflow.in/2203

Selected Answer

ans is A

when we access the 100 distinct page in some order (suppose order is 1 2 3....100) then total page fault occurs are 100. and in last, frame contain the pages 100 99 98 97 .when we reverse the string (100,99,98....1) then first four page will not cause the page fault bcz they already present in frame but the remaining 96 page will cause 96 page fault,so total page fault are 100+96=196

16 votes -- neha pawar (4.4k points)

5.6.12 Disk Scheduling: GATE2014-1-19 top

http://gateoverflow.in/1786

Selected Answer

Requests are serviced in following order

100 105 110 90 85 135 145 30

So request of 90 is serviced after 3 requests

7 votes -- Pooja Palod (32.4k points)

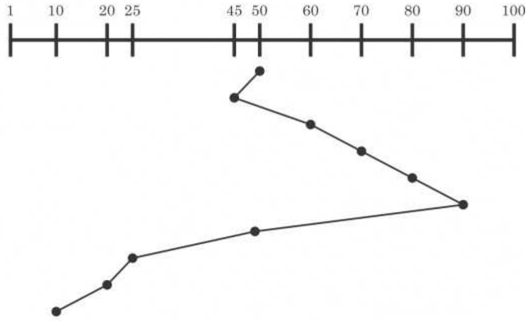
5.6.13 Disk Scheduling: GATE2015-1_30 top

http://gateoverflow.in/8227

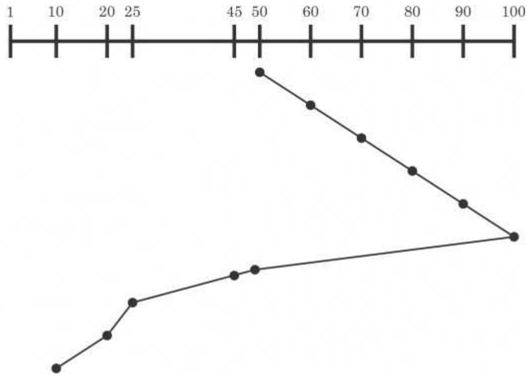
Selected Answer

check : http://www.cs.iit.edu/~cs561/cs450/disksched/disksched.html

SSTF:



Scan:



So, for SSTF it takes 130 head movements and for SCAN it takes 140 head movements.

Hence, not additional but $140 - 130 = 10$ less head movements SSTF takes.

17 votes -- Amar Vashishth (28.7k points)

5.7 Disks(29) top

5.7.1 Disks: GATE1990-7c top http://gateoverflow.in/85406

A certain moving arm disk-storage device has the following specifications:

Number of tracks per surface=404

Track storage capacity=130030 bytes.

Disk speed=3600 rpm

Average seek time=30 m secs.

Estimate the average latency, the disk storage capacity and the data transfer rate.

descriptive operating-system disks gate1990

Answer

5.7.2 Disks: GATE1993_6.7 top http://gateoverflow.in/2289

A certain moving arm disk storage, with one head, has the following specifications:

Number of tracks/recording surface = 200
Disk rotation speed = 2400 rpm
Track storage capacity = 62,500 bits

The average latency of this device is P ms and the data transfer rate is Q bits/sec. Write the values of P and Q.

gate1993 operating-system disks normal

Answer

5.7.3 Disks: GATE1993_7.8 top

http://gateoverflow.in/2296

The root directory of a disk should be placed

(A) at a fixed address in main memory
(B) at a fixed location on the disk
(C) anywhere on the disk
(D) at a fixed location on the system disk
(E) anywhere on the system disk

gate1993 operating-system disks normal

Answer

5.7.4 Disks: GATE1995_14 top

http://gateoverflow.in/2650

If the overhead for formatting a disk is 96 bytes for a 4000 byte sector,

a. Compute the unformatted capacity of the disk for the following parameters:

   Number of surfaces: 8
   Outer diameter of the disk: 12 cm
   Inner diameter of the disk: 4 cm
   Inner track space: 0.1 mm
   Number of sectors per track: 20

b. If the disk in (a) is rotating at 360 rpm, determine the effective data transfer rate which is defined as the number of bytes transferred per second between disk and memory.

gate1995 operating-system disks normal

Answer

5.7.5 Disks: GATE1997_74 top

http://gateoverflow.in/19704

A program P reads and processes 1000 consecutive records from a sequential file F stored on device D without using any file system facilities. Given the following

Size of each record = 3200 bytes

Access time of D = 10 msecs

Data transfer rate of D = 800×10^3 bytes/second

CPU time to process each record = 3 msecs

What is the elapsed time of P if

a. F contains unblocked records and P does not use buffering?
b. F contains unblocked records and P uses one buffer (i.e., it always reads ahead into the buffer)?
c. records of F are organized using a blocking factor of 2 (i.e., each block on D contains two records of F) and P uses one buffer?

gate1997 operating-system disks

Answer

5.7.6 Disks: GATE1998-25a top

http://gateoverflow.in/1740

Free disk space can be used to keep track of using a free list or a bit map. Disk addresses require d bits. For a disk with B blocks, F of which are free, state the condition under which the free list uses less space than the bit map.

gate1998 operating-system disks descriptive

Answer

5.7.7 Disks: GATE1998_2.9 top

http://gateoverflow.in/1681

Formatting for a floppy disk refers to

A. arranging the data on the disk in contiguous fashion
B. writing the directory
C. erasing the system data
D. writing identification information on all tracks and sectors

gate1998 operating-system disks normal

Answer

5.7.8 Disks: GATE1999_2.18, ISRO2008-46 top

http://gateoverflow.in/1496

Raid configurations of the disks are used to provide

A. Fault-tolerance
B. High speed
C. High data density
D. A & B

gate1999 operating-system disks easy isro2008

Answer

5.7.9 Disks: GATE2001-1.22 top

http://gateoverflow.in/715

Which of the following requires a device driver?

A. Register
B. Cache
C. Main memory
D. Disk

gate2001 operating-system disks easy

Answer

5.7.10 Disks: GATE2001-20 top

http://gateoverflow.in/761

Consider a disk with the 100 tracks numbered from 0 to 99 rotating at 3000 rpm. The number of sectors per track is 100 and the time to move the head between two successive tracks is 0.2 millisecond.

a. Consider a set of disk requests to read data from tracks 32, 7, 45, 5 and 10. Assuming that the elevator algorithm is used to schedule disk requests, and the head is initially at track 25 moving up (towards larger track numbers), what is the total seek time for servicing the requests?
b. Consider an initial set of 100 arbitrary disk requests and assume that no new disk requests arrive while servicing these requests. If the head is initially at track 0 and the elevator algorithm is used to schedule disk requests, what is the worse case time to complete all the requests?

gate2001 operating-system disks normal descriptive

Answer

5.7.11 Disks: GATE2001-8 top

http://gateoverflow.in/749

Consider a disk with following specifications: 20 surface, 1000 tracks/surface, 16 sectors/track, data destiny 1 KB/sector, rotation speed 3000 rpm. The operating system initiates the transfer between the disk and the memory sector-wise. Once the head has been placed on the right track, the disk reads a sector in a single scan. It reads bits from the sector while the head is passing over the sector. The read bits are formed into bytes in a serial-in-parallel-out buffer and each byte is then transferred to memory. The disk writing is exactly a complementary process.

For parts (C) and (D) below, assume memory read-write time = 0.1 microsecond/byte, interrupt driven transfer has an interrupt overhead = 0.4 microseconds, the DMA initialization and termination overhead is negligible compared to the total sector transfer time. DMA requests are always granted.

a. What is the total capacity of the desk?
b. What is the data transfer rate?
c. What is the percentage of time the CPU is required for this disk I/O for bite-wise interrupts driven transfer?
d. What is the maximum percentage of time the CPU is held up for this disk I/O for cycle-stealing DMA transfer?

gate2001 operating-system disks normal descriptive

Answer

5.7.12 Disks: GATE2003-25, ISRO2009-12 top

http://gateoverflow.in/915

Using a larger block size in a fixed block size file system leads to

A. better disk throughput but poorer disk space utilization
B. better disk throughput and better disk space utilization
C. poorer disk throughput but better disk space utilization
D. poorer disk throughput and poorer disk space utilization

gate2003 operating-system disks normal isro2009

Answer

5.7.13 Disks: GATE2004-49 top

http://gateoverflow.in/1045

A unix-style I-nodes has 10 direct pointers and one single, one double and one triple indirect pointers. Disk block size is 1 Kbyte, disk block address is 32 bits, and 48-bit integers are used. What is the maximum possible file size?

A. 2^{24} bytes
B. 2^{32} bytes
C. 2^{34} bytes
D. 2^{48} bytes

gate2004 operating-system disks normal

Answer

5.7.14 Disks: GATE2004-68 top

http://gateoverflow.in/1062

A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

A. 5.0%
B. 1.0%
C. 0.5%
D. 0.1%

gate2004 operating-system disks normal co&architecture

Answer

5.7.15 Disks: GATE2004-IT-51 top

http://gateoverflow.in/3694

The storage area of a disk has innermost diameter of 10 cm and outermost diameter of 20 cm. The maximum storage density of the disk is 1400bits/cm. The disk rotates at a speed of 4200 RPM. The main memory of a computer has 64-bit word length and 1µs cycle time. If cycle stealing is used for data transfer from the disk, the percentage of memory cycles stolen for transferring one word is

A. 0.5%
B. 1%
C. 5%
D. 10%

gate2004-it operating-system disks normal

Answer

5.7.16 Disks: GATE2005-21 top http://gateoverflow.in/1357

What is the swap space in the disk used for?

A. Saving temporary html pages
B. Saving process data
C. Storing the super-block
D. Storing device drivers

gate2005 operating-system disks easy

Answer

5.7.17 Disks: GATE2005-IT-63 top http://gateoverflow.in/3824

In a computer system, four files of size 11050 bytes, 4990 bytes, 5170 bytes and 12640 bytes need to be stored. For storing these files on disk, we can use either 100 byte disk blocks or 200 byte disk blocks (but can't mix block sizes). For each block used to store a file, 4 bytes of bookkeeping information also needs to be stored on the disk. Thus, the total space used to store a file is the sum of the space taken to store the file and the space taken to store the book keeping information for the blocks allocated for storing the file. A disk block can store either bookkeeping information for a file or data from a file, but not both.
What is the total space required for storing the files using 100 byte disk blocks and 200 byte disk blocks respectively?

A. 35400 and 35800 bytes
B. 35800 and 35400 bytes
C. 35600 and 35400 bytes
D. 35400 and 35600 bytes

gate2005-it operating-system disks normal

Answer

5.7.18 Disks: GATE2005-IT-81a top http://gateoverflow.in/3845

A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

What is the total amount of data that can be stored on the disk if it is used with a drive that rotates it with

I. Constant Linear Velocity
II. Constant Angular Velocity?

A. I. 80 MB; II. 2040 MB
B. I. 2040 MB; II 80 MB
C. I. 80 MB; II. 360 MB
D. I. 360 MB; II. 80 MB

gate2005-it operating-system disks normal

Answer

5.7.19 Disks: GATE2005-IT-81b top http://gateoverflow.in/3846

A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

If the disk has 20 sectors per track and is currently at the end of the 5^{th} sector of the inner-most track and the head can move at a speed of 10 meters/sec and it is rotating at constant angular velocity of 6000 RPM, how much time will it take to read 1 MB contiguous data starting from the sector 4 of the outer-most track?

A. 13.5 ms
B. 10 ms
C. 9.5 ms
D. 20 ms

gate2005-it operating-system disks normal

Answer

5.7.20 Disks: GATE2007-11, ISRO2009-36, ISRO2016-21 top http://gateoverflow.in/1209

Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively:

A. 256 Mbyte, 19 bits
B. 256 Mbyte, 28 bits
C. 512 Mbyte, 20 bits
D. 64 Gbyte, 28 bits

gate2007 operating-system disks normal isro2016

Answer

5.7.21 Disks: GATE2007-IT-44, ISRO2015-34 top http://gateoverflow.in/3479

A hard disk system has the following parameters :

- Number of tracks = 500
- Number of sectors/track = 100
- Number of bytes /sector = 500
- Time taken by the head to move from one track to adjacent track = 1 ms
- Rotation speed = 600 rpm.

What is the average time taken for transferring 250 bytes from the disk ?

A. 300.5 ms
B. 255.5 ms
C. 255 ms
D. 300 ms

gate2007-it operating-system disks normal isro2015

Answer

5.7.22 Disks: GATE2008-32 top http://gateoverflow.in/443

For a magnetic disk with concentric circular tracks, the seek latency is not linearly proportional to the seek distance due to

A. non-uniform distribution of requests

B. arm starting and stopping inertia

C. higher capacity of tracks on the periphery of the platter

D. use of unfair arm scheduling policies

gate2008 operating-system disks normal

Answer

5.7.23 Disks: GATE2009-51 top http://gateoverflow.in/1337

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple $\langle c, h, s \rangle$, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0th sector is addresses as $\langle 0, 0, 0 \rangle$, the 1st sector as $\langle 0, 0, 1 \rangle$, and so on

51. The address $\langle 400, 16, 29 \rangle$ corresponds to sector number:

A. 505035
B. 505036
C. 505037
D. 505038

gate2009 operating-system disks normal

Answer

5.7.24 Disks: GATE2009-52 top

http://gateoverflow.in/43477

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple $\langle c, h, s \rangle$, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0th sector is addresses as $\langle 0, 0, 0 \rangle$, the 1st sector as $\langle 0, 0, 1 \rangle$, and so on

The address of the 1039th sector is

A. $\langle 0, 15, 31 \rangle$
B. $\langle 0, 16, 30 \rangle$
C. $\langle 0, 16, 31 \rangle$
D. $\langle 0, 17, 31 \rangle$

gate2009 operating-system disks normal

Answer

5.7.25 Disks: GATE2011_44 top

http://gateoverflow.in/2146

An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected.)

(A) 0.50 s

(B) 1.50 s

(C) 1.25 s

(D) 1.00 s

gate2011 operating-system disks normal

Answer

5.7.26 Disks: GATE2012_41 top

http://gateoverflow.in/2149

A file system with 300 GByte disk uses a file descriptor with 8 direct block addresses, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. The maximum possible file size in this file system is

(A) 3 KBytes
(B) 35 KBytes
(C) 280 KBytes
(D) dependent on the size of the disk

gate2012 operating-system disks normal

Answer

5.7.27 Disks: GATE2013_29 top

http://gateoverflow.in/1540

Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each cylinder contains 64 sectors (0-63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is <cylinder no., surface no., sector no.> . A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200, 9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

(A) 1281 (B) 1282 (C) 1283 (D) 1284

gate2013 operating-system disks normal

Answer

5.7.28 Disks: GATE2015-1_48 top

http://gateoverflow.in/8354

Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is____________________.

gate2015-1 operating-system disks normal numerical-answers

Answer

5.7.29 Disks: GATE2015-2_49 top

http://gateoverflow.in/8251

Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50×10^6 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512-byte sector of the disk is ______.

gate2015-2 operating-system disks normal numerical-answers

Answer

Answers: Disks

5.7.1 Disks: GATE1990-7c top

http://gateoverflow.in/85406

Selected Answer

1. Avg Latency = $\frac{1}{2} \times \frac{60}{R} = \frac{1}{2} \times \frac{60}{3600}$ = 8.33 ms

2. Disk Storage Capacity = ***(We need number of surface to calculate it)*** 404 $\times$ 130030 Bytes $\simeq$ 50MB per surface (approx)

3. Data transfer rate = Track capacity$\times \frac{R}{60}$ = $130030 \times \frac{3600}{60}$ = 7801.8 KBPS

2 votes

-- Lokesh . (9.8k points)

5.7.2 Disks: GATE1993_6.7 top

http://gateoverflow.in/2289

Selected Answer

RPM = 2400

So, in 60 s, the disk rotates 2400 times.

Average latency is the time for half a rotation = 0.5 * 60 / 2400 s = 3/240 s = 12.5 ms.

In one full rotation, entire data in a track can be transferred. Track storage capacity = 62500 bits.

So, disk transfer rate = 62500 * 2400 / 60 s = 2.5 * 10^6 bps.

17 votes

-- Arjun Suresh (294k points)

5.7.3 Disks: GATE1993_7.8 top

http://gateoverflow.in/2296

Selected Answer

file system uses directories which are the files containing the name and location of other file in the file system. unlike other file,directory does not store the user data. Directories are the file that can point to other directories. Root directory point to various user directory.so they will be stored in such a way that user cannot easily modify them. They should be placed at fixed location on the disk.

14 votes -- neha pawar (4.4k points)

5.7.4 Disks: GATE1995_14 top http://gateoverflow.in/2650

Selected Answer

For A part :

No of track = Recording widh/ inner space between track

Recording width= (OuterDiameter - Inner Diameter)/2= (12-4)/2= 4 cm

therefore no of track = 4cm / 0.1 mm= 400 track

Since they have ask capacity of unformatted disk , so no 96 bytes in 4000 bytes would be wasted for non data purpose

Whole 4000 is used

So total capacity = 400 *8*20*4000 = 256*10^6 Bytes = **256 MB**

For B part :

its is given 360 rotations in 60 seconds

that is 360 rotations = 60 *10^3 sec

therefore 1 rotations will take (1/6)sec

In (1/6) sec - we can read one track= 20*(4000-96) B = 20 * 3904 B

then in 1 sec it will be = 20*3904*6 bytes = Data transfer rate =**468.480 KBps** (when we consider 1 Read/Write Head **for all** surface)

----

if we consider , **1 Read/Write Heads per surface (which is default approach) ,** then

Number of surfaces = 8

Data transfer rate = (468.480 * 8) KBps = 3747.84 KBps

But for our convenience we consider only 1 surface , it reads from one surface at a time. As data transfer rate is measured wrt a single surface only .

Hence for part B, correct answer is **468.480 KBps .**

14 votes -- spriti1991 (2.1k points)

5.7.5 Disks: GATE1997_74 top http://gateoverflow.in/19704

Selected Answer

here Access time = 10ms
Process each Record = 3ms
Transfer time = 3200/800*10^3 = 4ms
A) Elapsed time = (Access time + Transfer time + processing time)* number of records
(10+4+3)*1000 =17000 ms = 17sec
B) In this case P uses one ' Read ahead' buffer the processing and transferring of records can be overlapped
"Processing time is less than transfer time."
Elapsed time = (Access time + Transfer time)*number of records
= (10+4)*1000 = 14sec
C) In this case each block contain two records so we can access 500 time to transfer 1000 records.
Elapsed time = (Access time + Transfer time)*number of records
= (10+4+4)*500 = 9 sec

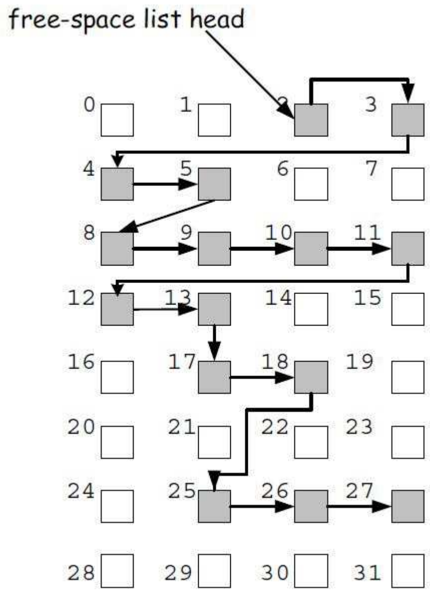
5 votes -- Umang Raman (15.2k points)

5.7.6 Disks: GATE1998-25a top http://gateoverflow.in/1740

Selected Answer

Bit map maintains one bit for each block, If it is free then bit will be "0" if occupied then bit will be "1".
For space purpose, it doesn't matter what bit we are using, only matters that how many blocks are there.
For B blocks, Bit map takes space of "B" bits.

Free list is a list that maintains addresses of free blocks only. If we have 3 free blocks then it maintains 3 addresses in a list, if 4 free blocks then 4 address in a list and like that.



Given that we have F free blocks, therefore F addresses in a list, and each address size is d bits therefore Free list takes space of "Fd".

condition under which the tree list uses less space than the bit map: Fd<B

7 votes -- Sachin Mittal (7.1k points)

5.7.7 Disks: GATE1998_2.9 top http://gateoverflow.in/1681

Selected Answer

Ans is D .

> The formatted disk capacity is always less than the "raw" unformatted capacity specified by the disk's manufacturer, because some portion of each track is used for sector identification and for gaps (empty spaces) between sectors and at the end of the track.

Reference :-https://en.wikipedia.org/wiki/Floppy_disk_format

9 votes -- Akash (43.8k points)

5.7.8 Disks: GATE1999_2.18, ISRO2008-46 top http://gateoverflow.in/1496

Selected Answer

A) Fault tolerance and

B) High Speed

9 votes -- GateMaster Prime (1.6k points)

5.7.9 Disks: GATE2001-1.22 top http://gateoverflow.in/715

Selected Answer

A disk driver is a device driver that allows a specific disk drive to communicate with the remainder of the computer. A good example of this driver is a floppy disk driver.

19 votes -- Bhagirathi Nayak (13.3k points)

5.7.10 Disks: GATE2001-20 top http://gateoverflow.in/761

Selected Answer

Answer A)

We are using SCAN - Elevator algorithms.

We will need to go from 25->99->5. (As we will move up all the way to 99,servicing all request, then come back to 5.)

So total seeks = 74+94= 168

Total time = 168*0.2 = 33.60000

Answer for B)

We need to consider rotational latency too - >

3000 rpm

i.e. 50 rps

1 r = 1000 /50 msec = 20 msec

So rotational latency = 20/2 = 10 msec per access.

In worst case we need to go from tracks 0-99. I.e. 99 seeks

Total time = 99 * 0.2 + 10*100 = 1019.8msec = 1.019 sec

10 votes -- Akash (43.8k points)

5.7.11 Disks: GATE2001-8 top http://gateoverflow.in/749

Selected Answer

Q.a) $20 \times 1000 \times 16 \times 1KB = 3,20,000KB$

Q.b)
$$\begin{aligned} 3000 \text{ rotations} &= 60 \text{ seconds} \\ 1 \text{ rotation} &= \frac{60}{3000} \text{ seconds} \\ 1 \text{ rotation} = 1 \text{ track} &= \frac{1}{50} \text{ seconds} \\ 1 \text{ track} = 16 \times 1KB &= \frac{1}{50} \text{ seconds} \\ 800KB &= 1 \text{ second} \end{aligned}$$

Hence, transfer rate = 800 KB/sec

Q.c) Data is transferred Byte wise; given in the question.
CPU read/write time for a Byte = 0.1 μs
Interrupt overhead (counted in CPU utilization time only) = 0.4 μs

transfer time for 1 Byte data which took place at the rate of 800 KB/sec = 1.25 μs
Percentage of CPU time required for this job = $\frac{0.1+0.4}{0.5+1.25} \times 100 = 28.57\%$

Q.d)
Percentage of CPU time held up for disk I/O for cycle stealing DMA transfer = $\frac{0.1+0}{1.25} \times 100 = 8.00\%$

14 votes -- Amar Vashishth (28.7k points)

5.7.12 Disks: GATE2003-25, ISRO2009-12 top

http://gateoverflow.in/915

Selected Answer

Answer is A. Larger block size means less number of blocks to fetch and hence better throughput. But larger block size also means space is wasted when only small size is required.

25 votes -- Arjun Suresh (294k points)

5.7.13 Disks: GATE2004-49 top

http://gateoverflow.in/1045

Selected Answer

Size of Disk Block = 1024Byte

Disk Blocks address = 4B

No of addresses per block 1024/4 = 256 = 2^8 addresses

we Have

10 Direct

1 SI = 2^8 Indirect* 2^10 = 2^18 Byte

1 DI = 2^8 SI = (2^8)^2 Direct ** 2^10 = 2^26 Byte

1 TI = 2^8 DI = (2^8)^2 SI = (2^8)^3 = 2^24 Direct =2^24 * 2^10 = 2^34 Byte.

So total size = 2^18 + 2^26 + 2^34 Byte + 10240 Byte. Which is nearly 2^34 Bytes. (We don't have exact option available. Choose approximate one)

Answer -> C

12 votes -- Akash (43.8k points)

no of address in one block=$2^{10}/2^2 = 2^8$ as triple pointer used max possible size= $2^8 \times 2^8 \times 2^8 \times 2^{10} = 2^{34}$ Bytes

ans is C

10 votes -- Pooja Palod (32.4k points)

5.7.14 Disks: GATE2004-68 top

http://gateoverflow.in/1062

Selected Answer

Clock cycle time = $\frac{1}{600} \times 10^6$

For DMA initiation and completion = $\frac{(900+300)}{600 \times 10^6}$ = 2 microsec .

Disk Transfer rate = 10 Mbytes/sec

1 byte = $\frac{1}{10^7}$ sec

20 Kbytes = 2 milisec = 2000 micro sec

Percentage = $\left(\frac{2}{2+2000}\right) \times 100$ =0.0999 $\simeq$ 0.1%

option D

% of cpu time consume= x/x+y

Now, when , x= Data preparation time or Total cycle time use by CPU and y= Data transfer time

To calculate the fraction of CPU time to the data transfer time - we use (x/x+y) as it is burst mode .

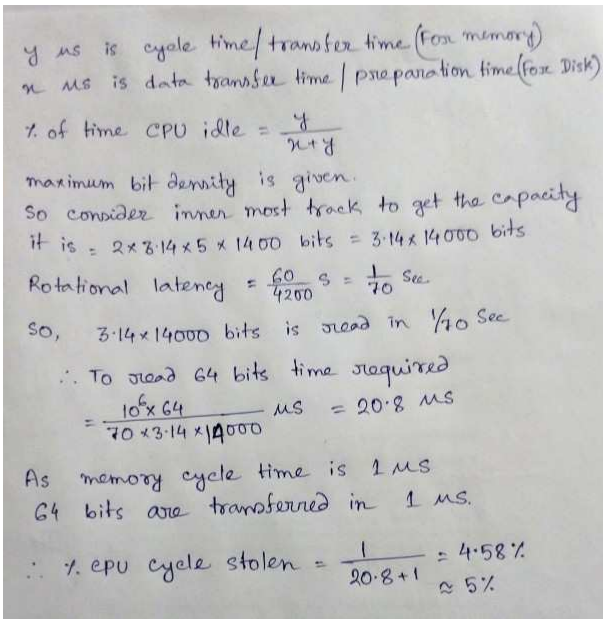
22 votes -- Prashant Singh (49.2k points)

5.7.15 Disks: GATE2004-IT-51 top http://gateoverflow.in/3694

Selected Answer

As the max density is given so we take the inner most diameter as it is denser there(2Rpi). The capacity of each track is pi*D*Density=3.14*10*1400 bits=14000pi bits
Now rotational latency is 60/RPM=60/4200=1/70 s.
So in 1/70 sec the disk can traverse one entire track and can read total 14000pi bits . Now this is done by the cpu. Now the data transfer is done by the DMA controller which will be operated in memory cycle time i.e 1 micro sec and it has 64 bit word length. So in 1 cycle it is able to transfer total of 64 bits. In 1 sec it can transfer 64*10^6 bits.(1sec memory cycle)
In 1 sec the disk can read total of 14000pi*70=3.08*10^6 bits (considering pi=22/7)
So total memory cycle stolen is 3.08*10^6/(64*10^6) %= 5%(approx)

14 votes -- Shaun Patel (6.9k points)



y μs is cycle time / transfer time (For memory)
x μs is data transfer time / preparation time (For Disk)

% of time CPU idle = $\frac{y}{x+y}$

maximum bit density is given.
So consider inner most track to get the capacity
it is = $2\times 3.14\times 5\times 1400$ bits = 3.14×14000 bits

Rotational latency = $\frac{60}{4200}$ s = $\frac{1}{70}$ sec

So, 3.14×14000 bits is read in $1/70$ sec

∴ To read 64 bits time required
$= \frac{10^6\times 64}{70\times 3.14\times 14000}$ μs = 20.8 μs

As memory cycle time is 1 μs
64 bits are transferred in 1 μs.

∴ % cpu cycle stolen = $\frac{1}{20.8+1}$ = 4.58%
≈ 5%

By @Ram Sharma1

11 votes -- Prashant Singh (49.2k points)

5.7.16 Disks: GATE2005-21 top http://gateoverflow.in/1357

Selected Answer

Answer is b.

8 votes -- anshu (3.2k points)

5.7.17 Disks: GATE2005-IT-63 top http://gateoverflow.in/3824

Selected Answer

for 100 bytes block:

11050 = 111 blocks requiring 111 * 4 = 444 bytes of bookkeeping info which requires another 5 disk blocks. So, totally 111 + 5 = 116 disk blocks. Similarly,
4990 = 50 + (50*4)/100 = 52
5170 = 52 + (52*4)/100 = 55
12640 = 127 + (127*4/100) = 133
-----
356 x 100 = 35600 bytes

For 200 bytes block:

56 + (56*4/200) = 58
25 + (25 * 4 / 200) = 26
26 + (26 * 4 / 200) = 27
64 + (64 * 4 / 200) = 66
-----
177 x 200 = 35400

So, C option.

14 votes -- Viral Kapoor (2k points)

5.7.18 Disks: GATE2005-IT-81a top

http://gateoverflow.in/3845

Selected Answer

- With ***Constant Linear Velocity, CLV,*** the density of bits is uniform from cylinder to cylinder. Because there are more sectors in outer cylinders, the disk spins slower when reading those cylinders, causing the rate of bits passing under the read-write head to remain constant. This is the approach used by modern CDs and DVDs.
- With ***Constant Angular Velocity, CAV,*** the disk rotates at a constant angular speed, with the bit density decreasing on outer cylinders. (These disks would have a constant number of sectors per track on all cylinders.)
- CLV=10+20+30+40+..80=360
- CAV=10*8 = 80 so answer should be d

Edit:- for CLV disk capacity

let track diameters like 1cm, 2cm... 8cm.

As described that density is uniform.

So all tracks has equal storage density.

Track capacity=storage density* circumference(2*pi*r)

For 1st track. 10 MB = density* pi*1

Density = 10/pi. MB/cm

For 2nd track capacity = density* circumference

= (10/pi) *(pi*2) MB = 20MB

Now each track capacity can be calculated and added for disk capacity

20 votes -- spriti1991 (2.1k points)

5.7.19 Disks: GATE2005-IT-81b top

http://gateoverflow.in/3846

Selected Answer

Total Time = Seek + Rotation + Transfer.

Seek Time :

Current Track 1

Destination Track 8

Distance Required to travel = 4-0.5= 3.5 Cm

Time required = 10 m/s == 1 Cm/ms == **3.5 ms**

Rotation Time:

6000 RPM in 60 sec

100 RPS in 1 sec

1 Revolution in 10 ms

1 Revolution = Covering entire Track

1 Track = 20 sector

1 sector required = 10/20 = 0.5 ms

Disk is constantly Rotating so when head moved from inner most track to outer most track total movement of disk = (3.5/0.5) = 7 sectors

Which means that when disk reached outer most track head was at end of end of 12 th sector

Total Rotational Delay = Time required to go from end of 12 to end of 3 = 11 sectors

1 sector = 0.5 ms so 11 sector = **5.5 ms**

Transfer Time

Total Data in Outer most track = 10 MB

Data in single Sector = 10 MB/20 = 0.5 MB

Data required to read = 1MB = 2 sector

Time required to read data = 2 * 0.5 = **1ms**

Total Time = Seek + Rotation + Transfer = 3.5ms + 5.5ms +1ms = 10 ms

8 votes -- Keval Malde (7.8k points)

5.7.20 Disks: GATE2007-11, ISRO2009-36, ISRO2016-21 top http://gateoverflow.in/1209

Selected Answer

ans is A.

16 surfaces= 4 bits, 128 tracks= 7 bits, 256 sectors= 8 bits, sector size 512 bytes = 9 bits

capacity of disk = 2^(4+7+8+9) = 2^28 = 256MB

to specify a particular sector we do not need sector size, so bits required = 4+7+8 = 19

17 votes -- jayendra (8.1k points)

5.7.21 Disks: GATE2007-IT-44, ISRO2015-34 top http://gateoverflow.in/3479

Selected Answer

option D

Explanation

Avg. time to transfer = Avg. seek time + Avg. rotational delay + Data transfer time

Avg Seek Time

given that : time to move between successive tracks is 1 ms

time to move from track 1 to track 1 : 0ms
time to move from track 1 to track 2 : 1ms
time to move from track 1 to track 3 : 2ms
..
..

time to move from track 1 to track 500 : 499 ms

Avg Seek time = $\frac{\sum 0+1+2+3+...+499}{500}$
= **249.5 ms**

Avg Rotational Delay

RMP : 600

600 rotations in 60 sec
one Rotation takes 60/600 sec = 0.1 sec

Avg Rotational Delay = $\frac{0.1}{2}$ { usually $\frac{\text{Rotation time}}{2}$ is taken as Avg Roational Delay }

= .05 sec

= **50 ms**

Data Transfer Time

One 1 Roatation we can read data on one complete track .

= 100 * 500 = 50,000 B data is read in one complete rotation

one complete rotation takes 0.1 s (we seen above)

0.1 --- > 50,000 bytes.
250 bytes ---> 0.1 * 250 / 50,000 = **0.5 ms**

Avg. time to transfer = Avg. seek time + Avg. rotational delay + Data transfer time

= 295.5+50+0.5

= 300 ms

47 votes -- pC (21.4k points)

Avg. time to transfer = Avg. seek time + Avg. rotational delay + Data transfer time

RPM = 600

So, rotational delay = 60 / 600 = 0.1 s

In 1 rotations we can transfer the whole data in a track which is equal to number of sectors in a track * bytes per track

= 100 * 500 = 50,000

i.e., in 0.1 s, we can transfer 50,000 bytes.
Hence time to transfer 250 bytes = 0.1 * 250 / 50,000 = 0.5 ms

Avg. rotational delay = 0.5 * rotational delay = 0.5 * 0.1s = 50 ms

Avg. seek time = (0 + 1 + 2 + ... + 499)/500 (as time to move between successive tracks is 1 ms and we have 500 such tracks) = 499 * 250 /500 = 249.5

So, average time for transferring 250 bytes = 249.5 + 50 + 0.5 = 300 ms

11 votes -- Arjun Suresh (294k points)

5.7.22 Disks: GATE2008-32 top

http://gateoverflow.in/443

Selected Answer

According to wiki http://en.wikipedia.org/wiki/Hard_disk_drive_performance_characteristics#Seek_time

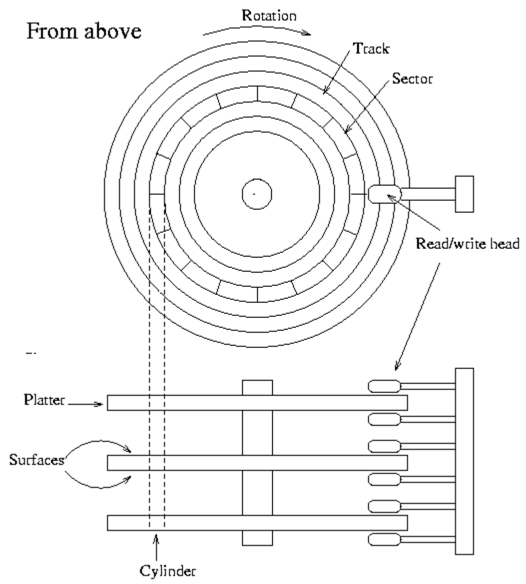
answer should be B.

10 votes -- Vikrant Singh (13.4k points)

5.7.23 Disks: GATE2009-51 top http://gateoverflow.in/1337

Selected Answer

The data on a disk is ordered in the following way. It is first stored on the first sector of the first surface of the first cylinder. Then in the next sector, and next, until all the sectors on the first track are exhausted. Then it moves on to the first sector of the second surface (remains at the same cylinder), then next sector and so on. It exhausts all available surfaces for the first cylinder in this way. After that, it moves on to repeat the process for the next cylinder.



So, to reach to the cylinder numbered 400 (401^{th} cylinder) we need to skip 400 * (10*2) * 63 = 504,000 sectors.

Then, to skip to the 16th surface of the cylinder numbered 400, we need to skip another 16*63 = 1,008 sectors.

Finally, to find the 29 sector, we need to move another 29 sectors.

In total, we moved 504,000 + 1,008 + 29 = 505,037 sectors.

Hence, the answer to 51 is option C.

33 votes -- Pragy Agarwal (19.5k points)

5.7.24 Disks: GATE2009-52 top http://gateoverflow.in/43477

Selected Answer

1039^{th} sector will be stored in track number (1039 + 1)/63 = 16.5 (as counting starts from 0 as given in question) and each track has 63 sectors. So, we need to go to 17^{th} track which will be numbered 16 and each cylinder has 20 tracks (10 platters * 2 recording surface each) . Number of extra sectors needed = 1040-16*63 = 32 and hence the sector number will be 31. So, option C.

18 votes -- Pragy Agarwal (19.5k points)

5.7.25 Disks: GATE2011_44 top http://gateoverflow.in/2146

Selected Answer

disk access time =seek time +rotational latency+transfer time (given that transfer time is neglected)

here seek time=10msec

rotational speed=6000rpm

60sec ----- 6000 rotation

1 rotation------60/6000 sec

rotational latency---1/2 *60/6000 sec=5msec

total time to transfer one library=10+5=15 msec

total time to transfer 100 libraries=100*15msec=1.5 sec

26 votes -- neha pawar (4.4k points)

5.7.26 Disks: GATE2012_41 top http://gateoverflow.in/2149

Selected Answer

direct block addressing will point to 8 disk blocks = 8*128 B = 1 KB

Singly Indirect block addressing will point to 1 disk block which has 128/8 disc block addresses = (128/8)*128 B = 2 KB

Doubly indirect block addressing will point to 1 disk block which has 128/8 addresses to disk blocks which in turn has 128/8 addresses to disk blocks = 16*16*128 B= 32 KB

Total = 35 KB

Ans B

25 votes -- Vikrant Singh (13.4k points)

5.7.27 Disks: GATE2013_29 top http://gateoverflow.in/1540

Selected Answer

I think there is an easy method:

First convert <1200,9,40> into sector address.

(1200 '* **16 * 64**) + (9 * **64**) + 40 = 1229416

number of sectors to store file = (42797 KB) / 512 = 85594

last sector to store file = 1229416+85594=1315010

Now do reverse engineering,

1315010/(**16*64**)=1284.189453 // 1284 will be cylinder number and remaining sectors =194.

194/**64** = 3.03125 // 3 is surface number and remaining sectors are 2.

∴<1284,3,1> is last sector address.

53 votes -- Laxmi (873 points)

42797 KB = 42797 * 1024 bytes require 42797 * 1024 / 512 sectors = 85594 sectors.

<1200, 9, 40> is the starting address. So, we can have 24 sectors in this recording surface. Remaining 85570 sectors.

85570 sectors require 85570/64 = 1337.031 ≈ 1338 recording surfaces. We start with recording surface 9, so we can have 7 more in the given cylinder. So, we have 1338 - 7 = 1331 recording surfaces left.

In a cylinder we have 16 recording surfaces. So, 1331 recording surfaces require 1331/16 = 83.18 ≈ 84 different cylinders.

The first cylinder (after the current one) starts at 1201. So, last one should be 1284.

<1284, 3, 2> will be the end address. (1331 - 16 * 83 = 3, and 85570 - 1337 * 64 = 2)

12 votes -- Arjun Suresh (294k points)

5.7.28 Disks: GATE2015-1_48 top

http://gateoverflow.in/8354

Selected Answer

Since each sector requires a seek,

Total time = 2000 * (seek time + avg. rotational latency + data transfer time)

Since data transfer rate is not given, we can take that in 1 rotation, all data in a track is read. i.e., in 60/10000 = 6ms, 600 * 512 bytes are read. So, time to read 512 bytes = 6/600 ms = 0.01 ms

= 2000 * (4 ms + 60 * 1000 /2* 10000 + 0.01)

= 2000 * (7.01 ms)

= 14020 ms.

http://www.csee.umbc.edu/~olano/611s06/storage-io.pdf

29 votes -- Arjun Suresh (294k points)

Seek time (given) = 4ms

RPM = 10000 rotation in 1 min [60 sec]

So, 1 rotation will be =60/10000 =6ms [rotation speed]

Rotation latency= 1/2 * 6ms=3ms

To access a file, total time includes =seek time + rot. latency +transfer time

TO calc. transfer time, find transfer rate Transfer rate = bytes on track /rotation speed

so, transfer rate = 600*512/6ms =51200 B/ms

transfer time= total bytes to be transferred/ transfer rate

so, Transfer time =2000*512/51200 = 20ms

Given as each sector requires seek tim + rot. latency = 4ms+3ms =7ms

Total 2000 sector takes = 2000*7 ms =14000 ms To read entire file ,total time = 14000 + 20(transfer time) = 14020 ms

10 votes -- Nilam dhatrak (695 points)

5.7.29 Disks: GATE2015-2_49 top

http://gateoverflow.in/8251

Selected Answer

Average time to read/write = Avg. seek time + Avg. rotational delay + Effective transfer time

Rotational delay = $\frac{60}{15} = 4$ ms

Avg. rotational delay = $\frac{1}{2} * 4 = 2$ ms

Avg. seek time = $2 * 2$ = 4 ms

Disk transfer time = $\frac{512 \text{ Bytes}}{50*10^6 \text{ Bytes/sec}}$ = 0.0102 ms

Effective transfer time = 10 * disk transfer time = 0.102 ms

So, avg. time to read/write = $4 + 2 + 0.0102 + 0.102$ = 6.11 ms
$\approx$ 6.1 **ms**

Ref: http://www.csc.villanova.edu/~japaridz/8400/sld012.htm

32 votes -- Arjun Suresh (294k points)

5.8 Dma(1) top

5.8.1 Dma: GATE2005-70 top

http://gateoverflow.in/1393

Consider a disk drive with the following specifications:

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

A. 10
B. 25
C. 40
D. 50

gate2005 operating-system disks normal dma

Answer

Answers: Dma

5.8.1 Dma: GATE2005-70 top

http://gateoverflow.in/1393

Selected Answer

512 KB-1/50 sec

4 Byte transfer will take total :4/(512*50*2^10)=152.58 ns

DMA will transfer 4B in 40nsec

so Cpu will be blocked (40/152.58)=26 % of time

best matching ans is B

7 votes -- Anurag Semwal (8k points)

B. 25

Does 3000 rotations in 60 seconds

$\implies$ 1 rotation in 20 ms

In 1 rotation covers data in 1 track which is = 512×1 KB

20 ms
$\longleftrightarrow$ 512 KB
1 sec

$\longleftrightarrow$ 25600 KB

$\Longrightarrow$ Transfer rate = 25600 KBps

Transfer Rate means we can perform read or write operations(one at a time) with this speed.

In one DMA cycle of 40 ns we are able to transfer 4 Bytes to disk.

CPU Idle Time = 40 ns

Data Prepration Time =

$\frac{4Bytes}{25600KB}$ = 156.25 ns

% Time CPU Blocked =

$\frac{40ns}{40ns+156.25ns} \times 100$ = **20.382**

25 votes -- Amar Vashishth (28.7k points)

5.9 Effective Memory Access(1) top

5.9.1 Effective Memory Access: GATE2000-2.22 top http://gateoverflow.in/669

Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then a 99.99% hit ratio results in average memory access time of

A. 1.9999 milliseconds
B. 1 millisecond
C. 9.999 microseconds
D. 1.9999 microseconds

gate2000 operating-system easy effective-memory-access

Answer

Answers: Effective Memory Access

5.9.1 Effective Memory Access: GATE2000-2.22 top http://gateoverflow.in/669

Selected Answer

Since nothing is told about page tables, we can assume page table access time is included in memory access time.

So, average memory access time

= .9999 * 1 + 0.0001 * 10,000
= 0.9999 + 1
= 1.9999 microseconds

23 votes -- Arjun Suresh (294k points)

5.10 File(1) top

5.10.1 File: GATE2014-2-20 top http://gateoverflow.in/1977

A FAT (file allocation table) based file system is being used and the total overhead of each entry in the FAT is 4 bytes in size. Given a 100×10^6 bytes disk on which the file system is stored and data block size is10^3 bytes, the maximum size of a file that can be stored on this disk in units of 10^6 bytes is __________.

gate2014-2 operating-system disks numerical-answers normal file file-system

Answer

Answers: File

5.10.1 File: GATE2014-2-20 top http://gateoverflow.in/1977

Selected Answer

Each datablock will have its entry.

So, Total Number of entries in the FAT = $\frac{\text{Disk Capacity}}{\text{Block size}} = \frac{100MB}{1KB} = 100K$

each entry takes up $4B$ as overhead

so space occupied by overhead = $100K \times 4B = 400KB = 0.4MB$

We have to give space to Overheads on the same file system and at the rest available space we can store data.

so, assuming that we use all available storage space to store a single file = Maximum file size = $\text{Total File System size} - \text{Overhead} = 100MB - 0.4MB = 99.6MB$

28 votes -- Kalpish Singhal (2.1k points)

5.11 File System(4) top

5.11.1 File System: GATE1996_23 top http://gateoverflow.in/2775

A file system with a one-level directory structure is implemented on a disk with disk block size of $4K$ bytes. The disk is used as follows:

Disk-block 0	File Allocation Table, consisting of one 8-bit entry per data block, representing the data block address of the next data block in the file
Disk-block 1	Directory, with one 32 bit entry per file:
Disk-block 2	Data-block 1;
Disk-block 3	Data-block 2; etc.

a. What is the maximum possible number of files?
b. What is the maximum possible file size in blocks

gate1996 operating-system disks normal file-system

Answer

5.11.2 File System: GATE2004-IT-67 top http://gateoverflow.in/3710

In a particular Unix OS, each data block is of size 1024 bytes, each node has 10 direct data block addresses and three additional addresses: one for single indirect block, one for double indirect block and one for triple indirect block. Also, each block can contain addresses for 128 blocks. Which one of the following is approximately the maximum size of a file in the file system?

A. 512 MB
B. 2 GB
C. 8 GB
D. 16 GB

gate2004-it operating-system file-system normal

Answer

5.11.3 File System: GATE2008-20 top http://gateoverflow.in/418

The data blocks of a very large file in the Unix file system are allocated using

A. continuous allocation
B. linked allocation
C. indexed allocation
D. an extension of indexed allocation

gate2008 file-system operating-system normal

Answer

5.11.4 File System: GATE2017-2-08 top

http://gateoverflow.in/118437

In a file allocation system, which of the following allocation scheme(s) can be used if no external fragmentation is allowed ?

1. Contiguous
2. Linked
3. Indexed

A. 1 and 3 only
B. 2 only
C. 3 only
D. 2 and 3 only

gate2017-2 operating-system file-system normal

Answer

Answers: File System

5.11.1 File System: GATE1996_23 top

http://gateoverflow.in/2775

a) Maximum possible number of files...

As per question, 32 bits (or 4 Bytes) are required per file. And there is only one block to store this, ie the Disk block 1, which is of size 4KB. So number of files possible is 4 KB/4 Bytes=1 K files possible...

b) Max file size..

As per question the Disk Block Address (FAT entry gives DBA) is of 8 bits.. So ideally the max file size should be 2^8=256 Block size.. But question makes it clear that two blocks , DB0 and DB1, stores control information. So efectively we have 256-2 =254 blocks with us.. and the max file size shud be =254 * size of one block= 254 * 4 KB= 1016 KB..

10 votes -- Hunaif (485 points)

5.11.2 File System: GATE2004-IT-67 top

http://gateoverflow.in/3710

Selected Answer

Answer: B

Maximum file size = 10*1024 Bytes + 1*128*1024 Bytes + 1*128*128*1024 Bytes + 1*128*128*128*1024 Bytes = approx 2 GB.

14 votes -- Rajarshi Sarkar (35k points)

5.11.3 File System: GATE2008-20 top

http://gateoverflow.in/418

Selected Answer

The data blocks of a very large file in the unix file system are allocated using an extension of indexed allocation or EXT2 file system. Hence option (d) is the right answer.

22 votes -- Kalpna Bhargav (3.2k points)

5.11.4 File System: GATE2017-2-08 top http://gateoverflow.in/118437

Selected Answer

Both Linked and Indexed allocation free from external fragmentation

refer:galvin

refer:https://webservices.ignou.ac.in/virtualcampus/adit/course/cst101/block4/unit4/cst101-bl4-u4-06.htm

4 votes -- Aboveallplayer (18.5k points)

5.12 Fork(4) top

5.12.1 Fork: GATE2004-IT-64 top http://gateoverflow.in/3707

A process executes the following segment of code :

```
for(i = 1; i < = n; i++)
    fork ();
```

The number of new processes created is

A. n
B. ((n(n + 1))/2)
C. 2^n - 1
D. 3^n - 1

gate2004-it operating-system fork easy

Answer

5.12.2 Fork: GATE2005-72 top http://gateoverflow.in/765

```
Consider the following code fragment:
if (fork() == 0)
{
   a = a + 5;
   printf("%d, %p n", a, &a);
}
else
{
   a = a - 5;
   printf ("%d, %p n", a,& a);
}
```

Let u,v be the values printed by the parent process and x,y be the values printed by the child process. Which one of the following is **TRUE**?

A. u = x + 10 and v = y
B. u = x + 10 and v != y
C. u + 10 = x and v = y
D. u + 10 = x and v != y

gate2005 operating-system fork normal

Answer

5.12.3 Fork: GATE2008-66 top http://gateoverflow.in/489

A process executes the following code

```
for(i=0; i<n; i++) fork();
```

The total number of child processes created is

A. n

B. 2^n-1
C. 2^n
D. $2^{n+1} - 1$

gate2008 operating-system fork normal

Answer

5.12.4 Fork: GATE2012-8 top http://gateoverflow.in/40

A process executes the code

```
fork();
fork();
fork();
```

The total number of **child** processes created is

(A) 3
(B) 4
(C) 7
(D) 8

gate2012 operating-system easy fork

Answer

Answers: Fork

5.12.1 Fork: GATE2004-IT-64 top http://gateoverflow.in/3707

Selected Answer

Option C.

At each fork, the number of processes doubles like from 1 - 2 - 4 - 8 ... 2^n. Of these except 1, all are child processes.

18 votes -- prakash (265 points)

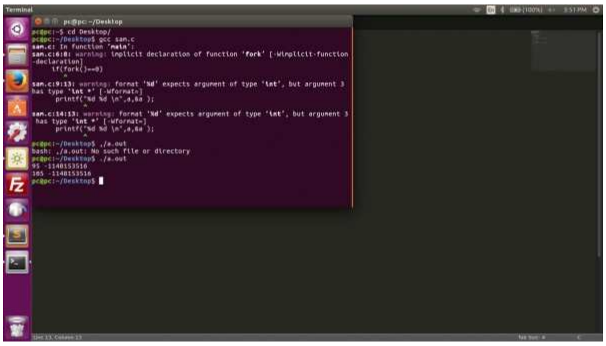
5.12.2 Fork: GATE2005-72 top http://gateoverflow.in/765

Selected Answer

it should be **OptionC**

```
#include<stdio.h>
#include<stdlib.h>
void main()
{
    int a =100;
    if(fork()==0)
    {
     a=a+5;
     printf("%d %d \n",a,&a );
    }
   else
    {
     a=a-5;
     printf("%d %d \n",a,&a );
    }
}
```

Output



fork returns 0 when it is a child process .

```
if ( fork == 0)
```

is true when it is child . Child increment valule of a .

In the above output

- 95 is printed by parent : **u**
- 105 is printed by child : **x**
  => u+10=x

The logical addresses remains the same between the parent and child processes.

Hence answer should be

u+10=x and v=y

17 votes -- pC (21.4k points)

(c) is the answer. Child is incrementing a by 5 and parent is decrementing a by 5. So, x = u + 10.

During fork(), address space of parent is copied for the child. So, any modifications to child variable won't affect the parent variable or vice-verse. But this copy is for physical pages of memory. The logical addresses remains the same between the parent and child processes.

17 votes -- gatecse (13.4k points)

5.12.3 Fork: GATE2008-66 top http://gateoverflow.in/489

Selected Answer

Each fork() creates a child which start executing from that point onward. So, number of child processes created will be 2^n - 1.

At each fork, the number of processes doubles like from 1 - 2- 4 - 8 ... 2^n. Of these except 1, all are child processes.

http://gateoverflow.in/3707/gate2004-it_64

19 votes -- Arjun Suresh (294k points)

5.12.4 Fork: GATE2012-8 top http://gateoverflow.in/40

Selected Answer

At each fork() the no. of processes becomes doubled. So, after 3 fork calls, the total no. of processes will be 8. Out of this 1 is the parent process and 7 are child processes. So, total number of child processes created is 7.

👍 18 votes -- Arjun Suresh (294k points)

5.13 Inter Process Communication(1) top

5.13.1 Inter Process Communication: GATE1997-3.7 top http://gateoverflow.in/2238

I/O redirection

A. implies changing the name of a file
B. can be employed to use an existing file as input file for a program
C. implies connecting 2 programs through a pipe
D. None of the above

gate1997 operating-system normal inter-process-communication

Answer

Answers: Inter Process Communication

5.13.1 Inter Process Communication: GATE1997-3.7 top http://gateoverflow.in/2238

Selected Answer

Answer: B

Typically, the syntax of these characters is as follows, using < to redirect input, and > to redirect output.

```
command1 > file1
```

executes command1, placing the output in file1, as opposed to displaying it at the terminal, which is the usual destination for standard output. This will clobber any existing data in file1.

Using,

```
command1 < file1
```

executes command1, with file1 as the source of input, as opposed to the keyboard, which is the usual source for standard input.

```
command1 < infile > outfile
```

combines the two capabilities: command1 reads from infile and writes to outfile.

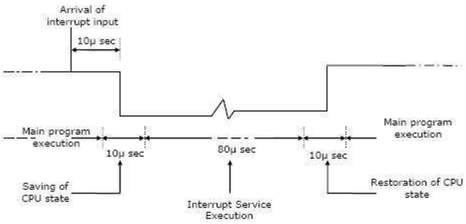
👍 10 votes -- Rajarshi Sarkar (35k points)

5.14 Interrupts(6) top

5.14.1 Interrupts: GATE1993_6.8 top http://gateoverflow.in/2290

The details of an interrupt cycle are shown in figure.

6.8. The details of an interrupt cycle are shown in figure.



Given that an interrupt input arrives every 1 msec, what is the percentage of the total time that the CPU devotes for the main program execution.

Given that an interrupt input arrives every 1 msec, what is the percentage of the total time that the CPU devotes for the main program execution.

gate1993 operating-system interrupts normal

Answer

5.14.2 Interrupts: GATE1997_3.8 top http://gateoverflow.in/2239

When an interrupt occurs, an operating system

A. ignores the interrupt

B. always changes state of interrupted process after processing the interrupt

C. always resumes execution of interrupted process after processing the interrupt

D. may change state of interrupted process to 'blocked' and schedule another process.

gate1997 operating-system interrupts normal

Answer

5.14.3 Interrupts: GATE1998_1.18 top http://gateoverflow.in/1655

Which of the following devices should get higher priority in assigning interrupts?

A. Hard disk
B. Printer
C. Keyboard
D. Floppy disk

gate1998 operating-system interrupts normal

Answer

5.14.4 Interrupts: GATE1999-1.9 top http://gateoverflow.in/1462

Listed below are some operating system abstractions (in the left column) and the hardware components (in the right column)?

(A) Thread	1. Interrupt
(B) Virtual address space	2. Memory
(C) File system	3. CPU
(D) Signal	4. Disk

A. (A) – 2 (B) – 4 (C) – 3 (D) – 1
B. (A) – 1 (B) – 2 (C) – 3 (D) – 4
C. (A) – 3 (B) – 2 (C) – 4 (D) – 1
D. (A) – 4 (B) – 1 (C) – 2 (D) – 3

gate1999 operating-system easy interrupts virtual-memory disks

Answer

5.14.5 Interrupts: GATE2001-1.12 top

http://gateoverflow.in/705

A processor needs software interrupt to

A. test the interrupt system of the processor
B. implement co-routines
C. obtain system services which need execution of privileged instructions
D. return from subroutine

gate2001 operating-system interrupts easy

Answer

5.14.6 Interrupts: GATE2011_11 top

http://gateoverflow.in/2113

A computer handles several interrupt sources of which of the following are relevant for this question.

- Interrupt from CPU temperature sensor (raises interrupt if CPU temperature is too high)
- Interrupt from Mouse (raises Interrupt if the mouse is moved or a button is pressed)
- Interrupt from Keyboard (raises Interrupt if a key is pressed or released)
- Interrupt from Hard Disk (raises Interrupt when a disk read is completed)

Which one of these will be handled at the **HIGHEST** priority?

(A) Interrupt from Hard Disk
(B) Interrupt from Mouse
(C) Interrupt from Keyboard
(D) Interrupt from CPU temperature sensor

gate2011 operating-system interrupts normal

Answer

Answers: Interrupts

5.14.1 Interrupts: GATE1993_6.8 top

http://gateoverflow.in/2290

Selected Answer

Time to service an interrupt= saving of cpu state+ISR execution+restoring of cpu state=(80+10+10)*10^-6=**100 microseconds**

for every **1 msec** an interrupt occurs which is served for **100 microseconds**
1 msec=1000 microseconds .

after every 1000 microseconds of main code execution, 100 microseconds for interrupt overhead exists

thus for every **1000 microseconds,** (**1000 - 100) = 900 microseconds of main program** and **100 microseconds of interrupt overhead exists.**

thus **900/1000 is usage of cpu to execute main program**

% of cpu used time to execute main program is (900 /1000) * 100 =90.00%

4 votes -- Surabhi Kadur (637 points)

5.14.2 Interrupts: GATE1997_3.8 top

http://gateoverflow.in/2239

Selected Answer

Think about this:
When a process is running and after time slot is over, who schedules new process?

- Scheduler.

But to run "scheduler" itself, we have to first schedule scheduler.
This is catch here, We need hardware support to schedule scheduler. That is hardware timer. When timer expires, then hardware generates interrupt and scheduler gets schedule.
Now after servicing that interrupt, schedular may schedule another process.

This was about Hardware interrupt.

Now think if user invokes a system call, System call in effect leads to interrupt, and after this interrupt CPU resumes execution of current running process,

Conclusion: Its about type of interrupt being serviced.
Options with "always" are false.

Hence option D.

14 votes -- Sachin Mittal (7.1k points)

A. Depends on the priority.
B. Not always.
C. Not always. If some high priority interrupt comes during execution of current interrupt, then?
D. Seems to be correct.

15 votes -- Monanshi Jain (8.5k points)

5.14.3 Interrupts: GATE1998_1.18 top

http://gateoverflow.in/1655

Selected Answer

It should be a Hard disk. I don't think there is a rule like that. But hard disk makes sense compared to others here.

http://www.ibm1130.net/functional/IOInterrupts.html

14 votes -- Arjun Suresh (294k points)

5.14.4 Interrupts: GATE1999-1.9 top

http://gateoverflow.in/1462

Selected Answer

Answer: C

10 votes -- Rajarshi Sarkar (35k points)

5.14.5 Interrupts: GATE2001-1.12 top

http://gateoverflow.in/705

Selected Answer

ans is C.

A and B are obviously incorrect. In D no need to change mode while returning from any subroutine. therefore software interrupt is not needed for that. But in C to execute any privileged instruction processor needs software interrupt while changing mode.

14 votes -- jayendra (8.1k points)

5.14.6 Interrupts: GATE2011_11 top

http://gateoverflow.in/2113

Selected Answer

Answer should be (D) Higher priority interrupt levels are assigned to requests which, if delayed or interrupted,could have serious consequences. Devices with high speed transfer such as magnetic disks are given high priority, and slow devices such as keyboard receive low priority. We know that mouse pointer movements are more frequent than keyboard ticks. So its obvious that its data transfer rate is higher than keyboard. Delaying a CPU temperature sensor could have serious consequences, overheat can damage CPU circuitry. From the above information we can conclude that priorities are-

CPU temperature sensor > Hard Disk > Mouse > Keyboard

23 votes -- Tejas Jaiswal (661 points)

5.15 Io Handling(6) top

5.15.1 Io Handling: GATE1996-1.20, ISRO2008-56 top http://gateoverflow.in/2724

Which of the following is an example of spooled device?

A. A line printer used to print the output of a number of jobs

B. A terminal used to enter input data to a running program

C. A secondary storage device in a virtual memory system

D. A graphic display device

gate1996 operating-system io-handling normal isro2008

Answer

5.15.2 Io Handling: GATE1998_1.29 top http://gateoverflow.in/1666

Which of the following is an example of a spooled device?

A. The terminal used to enter the input data for the C program being executed

B. An output device used to print the output of a number of jobs

C. The secondary memory device in a virtual storage system

D. The swapping area on a disk used by the swapper

gate1998 operating-system io-handling easy

Answer

5.15.3 Io Handling: GATE2004-IT-11, ISRO2011-33 top http://gateoverflow.in/3652

What is the bit rate of a video terminal unit with 80 characters/line, 8 bits/character and horizontal sweep time of 100 μs (including 20 μs of retrace time)?

A. 8 Mbps
B. 6.4 Mbps
C. 0.8 Mbps
D. 0.64 Mbps

gate2004-it operating-system io-handling easy isro2011

Answer

5.15.4 Io Handling: GATE2005-19 top http://gateoverflow.in/1355

Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

A. Neither vectored interrupt nor multiple interrupting devices are possible

B. Vectored interrupts are not possible but multiple interrupting devices are possible

C. Vectored interrupts and multiple interrupting devices are both possible

D. Vectored interrupts are possible but multiple interrupting devices are not possible gate2005 operating-system io-handling normal

Answer

5.15.5 Io Handling: GATE2005-20 top

http://gateoverflow.in/1356

Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instruction privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

A. I/O protection is ensured by operating system routine(s)

B. I/O protection is ensured by a hardware trap

C. I/O protection is ensured during system configuration

D. I/O protection is not possible

gate2005 operating-system io-handling normal

Answer

5.15.6 Io Handling: GATE2006-IT-8 top

http://gateoverflow.in/3547

Which of the following DMA transfer modes and interrupt handling mechanisms will enable the highest I/O band-width?

A. Transparent DMA and Polling interrupts
B. Cycle-stealing and Vectored interrupts
C. Block transfer and Vectored interrupts
D. Block transfer and Polling interrupts

gate2006-it operating-system io-handling dma normal

Answer

Answers: Io Handling

5.15.1 Io Handling: GATE1996-1.20, ISRO2008-56 top

http://gateoverflow.in/2724

Selected Answer

ans is A

spooling(simultaneous peripheral operations online) is a technique in which an intermediate device such as disk is interposed between process and low speed i/o device.for ex. in printer if a process attempt to print a document but printer is busy printing another document ,the process,instead of waiting for printer to become available,write its output to disk.when the printer become available the data on disk is printed.spooling allows process to request operation from peripheral device without requiring that the device be ready to service the request.

14 votes -- neha pawar (4.4k points)

5.15.2 Io Handling: GATE1998_1.29 top

http://gateoverflow.in/1666

Selected Answer

Ans B

http://en.wikipedia.org/wiki/Spooling

10 votes -- Keith Kr (6.3k points)

5.15.3 Io Handling: GATE2004-IT-11, ISRO2011-33 top

http://gateoverflow.in/3652

Selected Answer

Answer: B

Bit rate of a video terminal unit = 80*8 bits/100 μs = 6.4 Mbps

12 votes -- Rajarshi Sarkar (35k points)

5.15.4 Io Handling: GATE2005-19 top http://gateoverflow.in/1355

Selected Answer

C) is the correct answer. We can use one Interrupt line for all the devices connected and pass it through OR gate. On receiving by the CPU, it executes the corresponding ISR and after exec INTA is sent via one line. For Vectored Interrupts it is always possible if we implement in daisy chain mechanism.

Ref :Click Here

7 votes -- confused_luck (891 points)

5.15.5 Io Handling: GATE2005-20 top http://gateoverflow.in/1356

Selected Answer

option A. User applications are not allowed to perform I/O in user mode - All I/O requests are handled through system calls that must be performed in kernel mode

19 votes -- Vikrant Singh (13.4k points)

5.15.6 Io Handling: GATE2006-IT-8 top http://gateoverflow.in/3547

Selected Answer

CPU get highest bandwidth in transparent DMA and polling. but it asked for I/O bandwidth not cpu bandwidth so option A is wrong.

In case of Cycle stealing, in each cycle time device send data then wait again after few CPU cycle it sends to memory . So option B is wrong.

In case of Polling CPU takes the initiative so I/O bandwidth can not be high so option D is wrong .

Consider Block transfer, in each single block device send data so bandwidth (means the amount of data) must be high . This makes option C correct.

5 votes -- Bikram (44.7k points)

The answer is option C .

In block transfer the entire block of data is transfered then only CPU again becomes the bus master

And in vectored Interrupts . I/o device along with interrupts send vector address of Interrupt Service routine which guides CPU to execute for a specific I/O device

Hence in both case BW will be required in a good amount !

12 votes -- spriti1991 (2.1k points)

5.16 Linking(1) top

5.16.1 Linking: GATE2002-2.20 top http://gateoverflow.in/850

Dynamic linking can cause security concerns because

A. Security is dynamic

B. The path for searching dynamic libraries is not known till runtime
C. Linking is insecure
D. Cryptographic procedures are not available for dynamic linking

gate2002 operating-system linking easy

Answer

Answers: Linking

5.16.1 Linking: GATE2002-2.20 top http://gateoverflow.in/850

Selected Answer

A) Nonsense option, No idea why it is here.

D) There is no relation between Cryptographic procedures & Dynamic linking.

C) This is not true. Linking in itself not insecure.

B) The path for searching dynamic libraries is not known till runtime -> This seems most correct answer.

18 votes -- Akash (43.8k points)

5.17 Memory Allocation(1) top

5.17.1 Memory Allocation: GATE2015-2_30 top http://gateoverflow.in/8145

Consider 6 memory partitions of sizes 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB, where KB refers to kilobyte. These partitions need to be allotted to four processes of sizes 357 KB, 210 KB, 468 KB, 491 KB in that order. If the best fit algorithm is used, which partitions are NOT allotted to any process?

A. 200 KB and 300 KB
B. 200 KB and 250 KB
C. 250 KB and 300 KB
D. 300 KB and 400 KB

gate2015-2 operating-system memory-allocation easy

Answer

Answers: Memory Allocation

5.17.1 Memory Allocation: GATE2015-2_30 top http://gateoverflow.in/8145

Selected Answer

option A is correct because we have 6 memory partitions of sizes 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB and the partition allotted to the process using best fit is given below-
357 KB process allotted at partition 400 KB.
210 KB process allotted at partition 250 KB
468 KB process allotted at partition 500 KB
491 KB process allotted at partition 600 KB
so we have left only two partitions 200 KB and 300 KB

14 votes -- Anoop Sonkar (4.9k points)

5.18 Memory Management(6) top

5.18.1 Memory Management: GATE1992-12b top http://gateoverflow.in/43582

Let the page reference and the working set window be $c\,c\,d\,b\,c\,e\,c\,e\,a\,d$ and 4, respectively. The initial working set at time $t = 0$ contains the pages $\{a, d, e\}$, where a was referenced at time $t = 0$, d was referenced at time $t = -1$, and e was referenced at time $t = -2$. Determine the total number of page faults and the average number of page frames used by computing the working set at each reference.

gate1992 operating-system memory-management normal

Answer

5.18.2 Memory Management: GATE1995_5 top http://gateoverflow.in/2641

A computer installation has 1000k of main memory. The jobs arrive and finish in the following sequences.

```
Job 1 requiring 200k arrives
Job 2 requiring 350k arrives
Job 3 requiring 300k arrives
Job 1 finishes
Job 4 requiring 120k arrives
Job 5 requiring 150k arrives
Job 6 requiring 80k arrives
```

a. Draw the memory allocation table using Best Fit and First Fit algorithms

b. Which algorithm performs better for this sequence?

gate1995 operating-system memory-management normal

Answer

5.18.3 Memory Management: GATE1996_2.18 top http://gateoverflow.in/2747

A 1000 Kbyte memory is managed using variable partitions but no compaction. It currently has two partitions of sizes 200 Kbytes and 260 Kbytes respectively. The smallest allocation request in Kbytes that could be denied is for

A. 151
B. 181
C. 231
D. 541

gate1996 operating-system memory-management normal

Answer

5.18.4 Memory Management: GATE2006-IT-56 top http://gateoverflow.in/3600

For each of the four processes P_1, P_2, P_3 and P_4. The total size in kilobytes (KB) and the number of segments are given below.

Process	Total size (in KB)	Number of segments
P1	195	4
P2	254	5
P3	45	3
P4	364	8

The page size is 1 KB. The size of an entry in the page table is 4 bytes. The size of an entry in the segment table is 8 bytes. The maximum size of a segment is 256 KB. The paging method for memory management uses two-level paging, and its storage overhead is P. The storage overhead for the segmentation method is S. The storage overhead for the segmentation and paging method is T. What is the relation among the overheads for the different methods of memory management in the concurrent execution of the above four processes ?

A. P < S < T
B. S < P < T
C. S < T < P
D. T < S < P

gate2006-it operating-system memory-management difficult

Answer

5.18.5 Memory Management: GATE2007-IT-11 top

http://gateoverflow.in/3444

Let a memory have four free blocks of sizes 4k, 8k, 20k, 2k. These blocks are allocated following the best-fit strategy. The allocation requests are stored in a queue as shown below.

Request No	J1	J2	J3	J4	J5	J6	J7	J8
Request Sizes	2k	14k	3k	6k	6k	10k	7k	20k
Usage Time	4	10	2	8	4	1	8	6

The time at which the request for J7 will be completed will be

A. 16
B. 19
C. 20
D. 37

gate2007-it operating-system memory-management normal

Answer

5.18.6 Memory Management: GATE2014-2-55 top

http://gateoverflow.in/2022

Consider a main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is _________

gate2014-2 operating-system memory-management numerical-answers normal

Answer

Answers: Memory Management

5.18.1 Memory Management: GATE1992-12b top

http://gateoverflow.in/43582

Selected Answer

Window size of working set = 4

Initial pages in the working set window = { e, d, a}

when page c comes at t=1, working set window = { e, d, a, c} -**miss** - current window size= 4

when page c comes,at t= 2, working set window = { d, a, c} - hit - current window size = 3

when page d comes,at t= 3, working set window = {a, c, d } - hit - current window size = 3

when page b comes,at t= 4, working set window = { c, d, b } -**miss** - current window size = 3

when page c comes,at t= 5, working set window = { d, b, c} - hit - current window size = 3

when page e comes,at t= 6, working set window = { d, b, c, e} -**miss** - current window size = 4

when page c comes,at t= 7, working set window = { b, c,e } - hit - current window size = 3

when page e comes,at t= 8, working set window = { c, e} - hit - current window size = 2

when page a comes,at t= 9, working set window = { c, e, a } -**miss** - current window size = 3 when page d comes,at t=10, working set window = { c, e, a, d} -**miss** - current window size = 4.

Total number of page faults = **5**.

Average no. of page frames used by window set = (4 + 3 + 3 + 3 + 3 + 4 + 3 + 2 + 3 + 4) / 10 = 32/10 =**3.2**

14 votes -- Dhananjay Kumar Sharma (25.2k points)

5.18.2 Memory Management: GATE1995_5 top http://gateoverflow.in/2641

Selected Answer

initial there is 1000k main memory available ...

then job 1 arrive ..and occupied 200k, then job 2 arrive ,occupy 350k,, after that job3 arrive and occupy 300k (assume continuous allocation) now free memory is 1000-850(200+350+300)= 150k ...(till these jobs first fit and best fit are same)

now job1 is finished ...so that space is also free... so here 200k slot and 150k slot are free ....

now job 4 arrive which is 120k ..

case 1: first fit , so it will be in 200 k slot (free slot) and now free is = 200-120=80k ,

now 150k arrive which will be in 150 k slot ...

then 80k arrive which will occupy in 80k slot (200-120) so all jobs will be allocated successfully ...

case 2: best fit : , 120 k job will occupy best fit free space which is 150k so now remaining 150-120=30k ,

then 150k job arrive it will be occupied in 200k slot ..which is best fit for this job ...so free space =200-150= 50,

now job 80k arrive , but there is no continuous 80k memory free ...so it will not be allocated successfully ...

so first fit is better .

11 votes -- sonam vyas (13.2k points)

5.18.3 Memory Management: GATE1996_2.18 top http://gateoverflow.in/2747

Selected Answer

Answer is B. Since the total size of the memory is 1000KB, lets assume that the partitioning for the current allocation is done in such a way that it will leave minimum free space.

Partitioning the 1000kB as below will allow gaps of 180KB each and hence a request of 181kB will not be met.

[180Kb-200kb-180kb-260kb-180kb]. The reasoning is more of an intution rather than any formula.

18 votes -- kireeti (1.1k points)

Answer is B. 181KB

Explanation:

As mentioned by @Arjun sir, to get the smallest allocation request that could be denied, we have to minimize the maximum of the hole partition (that is free memory blocks), let's see why.

First we have to note that we are using **Variable Partitioning** method **without compaction**,

Variable Partitioning:

i. the partitions are of variable length and number, AND
ii. When a process is brought into main memory, it is allocated exactly as much memory as it requires and no more.

In **compaction** we realign the scattered holes to one end of memory, so that a larger hole can be created.

(Initially whole memory is a hole, i.e. free memory, then a process comes and it is allocated exactly the needed space, which creates a partition. In this question we can safely assume that the two given partitions of 200KB and 260KB are allocated to two processes, because otherwise it will all be one single hole of 1000KB and the answer to the question would be 1001KB)

Now let's see all the possible cases:

CASE 1.

If 200KB and 260KB are contiguous, from the beginning of the memory (obviously after the OS partition), then hole has a size of 540KB, so any process asking upto 540KB can be allocated.

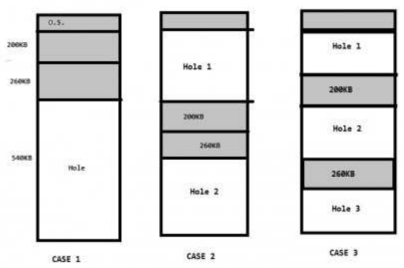
CASE 2.

If 200KB and 260KB are continguous but somewhere in the middle of the memory, then we have two holes left. Hole1 and Hole2 (Refer the image below). If the size of these holes are not equal, say Hole1 = 300KB and Hole2 = 240KB then processes asking for memory upto 300KB can be allocated.

But if we keep hole sizes equal, we can see that Hole 1 = Hole 2 = 270KB, thus maximum 270 KB only can be allocated.

CASE 3

Arguing in a similar manner as in case 2, we can see that size of all three holes must be equal (i.e. 180KB), otherwise we'll have a hole which will allow a process needing more than 180KB to get allocated.



So 181 KB is the smallest allocation request that can be denied.

Wrong reasoning to get 151 KB:

Someone mentioned that if we order in the following way:

200-260-150-150-150-90 [Wrong division for variable partitions, the order looks like fixed partitions]

we can get the answer as 151KB.

The **problem** here is that it's given in the question that there are only two partitions, i.e., two processes are allocated space in main memory. So rest space is free memory, i.e., a hole.

So if 200 and 260 are allocated contiguously from the beginning (Or end), we have a hole of 540KB and any process needing memory upto 540 KB can be allocated.For this case the correct ordering would be: 200KB-260KB-540KB or 540KB-200KB-260KB

16 votes -- Pratyush Madhukar (3.4k points)

5.18.4 Memory Management: GATE2006-IT-56 top http://gateoverflow.in/3600

For 2-level paging.

Page size is 1KB. So, no. of pages required for P_1 = 195. An entry in page table is of size 4 bytes and assuming an inner level page table takes the size of a page (this information is not given in question), we can have up to 256 entries in a second level page table and we require only 195 for P_1. Thus only 1 second level page table is enough. So, memory overhead = 1KB (for first level) (again assumed as page size as not explicitly told in question) + 1KB for second level = 2KB.

For P_2 and P_3 also, we get 2KB each and for P_4 we get 1 + 2 = 3KB as it requires 1 first level page table and 2 second level page tables (364 > 256). So, total overhead for their concurrent execution $= 2 \times 3 + 3 = 9KB$.

Thus $P = 9KB$.

For Segmentation method

http://people.csail.mit.edu/rinard/osnotes/h15.html

P_1 uses 4 segments -> 4 entries in segment table$= 4 \times 8 = 32$ bytes.

Similarly, for P_2, P_3 and P_4 we get 5×8, 3×8 and 8×8 bytes respectively and the total overhead will be $32 + 40 + 24 + 64 = 160$ bytes.

So, $S = 160B$.

For Segmentation with Paging

Here we segment first and then page. So, we need the page table size. We are given maximum size of a segment is 256 KB and page size is 1KB and thus we require 256 entries in the page table. So, total size of page table $= 256 \times 4 = 1024$ bytes (exactly 1 page size).

So, now for P_1 we require 1 segment table of size 32 bytes plus 1 page table of size 1KB. Similarly,

P_2- 40 bytes and 1KB
P_3- 24 bytes and 1KB
P_4- 64 bytes and 1KB.

Thus total overhead = 160 bytes + 4KB = 4096+160 = 4256 bytes.

So, $T = 4256B$.

So, answer would be C- $S < T < P$.

23 votes -- Arjun Suresh (294k points)

5.18.5 Memory Management: GATE2007-IT-11 top http://gateoverflow.in/3444

Selected Answer

At t = 0

Memory Block	Size	Job
A	4k	J3 (finishes at t = 2)
B	8k	J4 (finishes at t = 8)
C	20k	J2 (finishes at t = 10)
D	2k	J1 (finishes at t = 4)

At t = 8

Memory Block	Size	Job
A	4k	
B	8k	J5 (finishes at t = 14)
C	20k	J2 (finishes at t = 10)
D	2k	

At t = 10

Memory Block	Size	Job
A	4k	
B	8k	J5 (finishes at t = 14)
C	20k	J6 (finishes at t = 11)
D	2k	

At t = 11

Memory Block	Size	Job
A	4k	
B	8k	J5 (finishes at t = 14)
C	20k	J7 (finishes at t = 19)
D	2k	

So, J7 finishes at t = 19.

Ref: http://thumbsup2life.blogspot.fr/2011/02/best-fit-first-fit-and-worst-fit-memory.html

16 votes -- Arjun Suresh (294k points)

5.18.6 Memory Management: GATE2014-2-55 top http://gateoverflow.in/2022

Selected Answer

When a write request is made, the bus is occupied for 100 ns. So, between 2 writes at least 100 ns interval must be there.

Now, after a write request, for 100 + 500 = 600 ns, the corresponding memory module is busy storing the data. But, assuming the next stores are to a different memory module (we have totally 8 modules in question), we can have consecutive stores at intervals of 100 ns. So, maximum number of stores in 1 ms

$= 10^{-3} * 1/(100 * 10^{-9}) = 10,000$

31 votes -- Arjun Suresh (294k points)

5.19 Os Protection(1) top

5.19.1 Os Protection: GATE2001-1.13 top http://gateoverflow.in/706

A CPU has two modes -- privileged and non-privileged. In order to change the mode from privileged to non-privileged

A. a hardware interrupt is needed
B. a software interrupt is needed
C. a privileged instruction (which does not generate an interrupt) is needed
D. a non-privileged instruction (which does not generate an interrupt) is needed

gate2001 operating-system normal os-protection

Answer

Answers: Os Protection

5.19.1 Os Protection: GATE2001-1.13 top http://gateoverflow.in/706

Selected Answer

Answer should be D. Changing from privileged to non-privileged doesn't require an interrupt unlike from non-privileged to privileged. Also, to loose a privilege we don't need a privileged instruction though a privileged instruction does no harm.

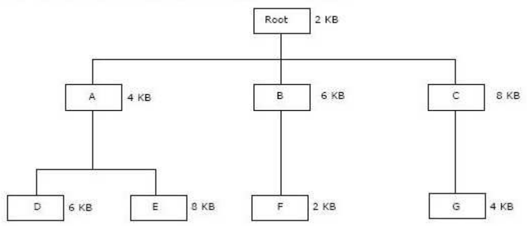
http://web.cse.ohio-state.edu/~teodores/download/teaching/cse675.au08/CSE675.02_MIPS-ISA_part3.pdf

25 votes -- Arjun Suresh (294k points)

5.20 Overlay(1) top

5.20.1 Overlay: GATE1998-2.16 top http://gateoverflow.in/1689

The overlay tree for a program is as shown below:



What will be the size of the partition (in physical memory) required to load (and run) this program?

A. 12 KB
B. 14 KB
C. 10 KB
D. 8 KB

gate1998 operating-system normal memory-management overlay

Answer

Answers: Overlay

5.20.1 Overlay: GATE1998-2.16 top

http://gateoverflow.in/1689

Selected Answer

"To enable a process to be larger than the amount of memory allocated to it, we can use overlays. The idea of overlays is to keep in memory only those instructions and data that are needed at any given time. When other instructions are needed, they are loaded into space occupied previously by instructions that are no longer needed." For the above program, maximum memory will be required when running code portion present at leaves. Max requirement=(max of requirements of D,E,F, and G. =MAX(12,14,10,14) =14 (Ans)

14 votes -- learncp (1.4k points)

5.21 Page Replacement(25) top

5.21.1 Page Replacement: GATE 2016-1-49 top

http://gateoverflow.in/39711

Consider a computer system with ten physical page frames. The system is provided with an access sequence $(a_1, a_2, \ldots, a_{20}, a_1, a_2, \ldots a_{20})$, where each a_i is a distinct virtual page number. The difference in the number of page faults between the last-in-first-out page replacement policy and the optimal page replacement policy is__________.

gate2016-1 operating-system page-replacement normal numerical-answers

Answer

5.21.2 Page Replacement: GATE 2016-2-20 top

http://gateoverflow.in/39559

In which one of the following page replacement algorithms it is possible for the page fault rate to increase even when the number of allocated frames increases?

A. LRU (Least Recently Used)
B. OPT (Optimal Page Replacement)
C. MRU (Most Recently Used)
D. FIFO (First In First Out)

gate2016-2 operating-system page-replacement easy

Answer

5.21.3 Page Replacement: GATE1993_21 top http://gateoverflow.in/2318

The following page addresses, in the given sequence, were generated by a program:

1 2 3 4 1 3 5 2 1 5 4 3 2 3

This program is run on a demand paged virtual memory system, with main memory size equal to 4 pages. Indicate the page references for which page faults occur for the following page replacement algorithms.

a. LRU
b. FIFO

Assume that the main memory is initially empty

gate1993 operating-system page-replacement normal

Answer

5.21.4 Page Replacement: GATE1994_1.13 top http://gateoverflow.in/2454

A memory page containing a heavily used variable that was initialized very early and is in constant use is removed then

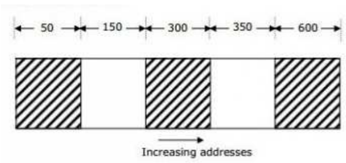
A. LRU page replacement algorithm is used
B. FIFO page replacement algorithm is used
C. LFU page replacement algorithm is used
D. None of the above

gate1994 operating-system page-replacement easy

Answer

5.21.5 Page Replacement: GATE1994_1.24 top http://gateoverflow.in/2467

Consider the following heap (figure) in which blank regions are not in use and hatched region are in use.



The sequence of requests for blocks of sizes $300, 25, 125, 50$ can be satisfied if we use

A. either first fit or best fit policy (any one)
B. first fit but not best fit policy
C. best fit but not first fit policy
D. None of the above

gate1994 operating-system page-replacement normal

Answer

5.21.6 Page Replacement: GATE1995_1.8 top http://gateoverflow.in/2595

Which of the following page replacement algorithms suffers from Belady's anamoly?

A. Optimal replacement

B. LRU
C. FIFO
D. Both (A) and (C)

gate1995 operating-system page-replacement normal

Answer

5.21.7 Page Replacement: GATE1995_2.7 top http://gateoverflow.in/2619

The address sequence generated by tracing a particular program executing in a pure demand based paging system with 100 records per page with 1 free main memory frame is recorded as follows. What is the number of page faults?

$$0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0370$$

A. 13
B. 8
C. 7
D. 10

gate1995 operating-system page-replacement normal

Answer

5.21.8 Page Replacement: GATE1997-3.10, ISRO2008-57, ISRO2015-64 http://gateoverflow.in/2241 top

Dirty bit for a page in a page table

A. helps avoid unnecessary writes on a paging device
B. helps maintain LRU information
C. allows only read on a page
D. None of the above

gate1997 operating-system page-replacement easy isro2008 isro2015

Answer

5.21.9 Page Replacement: GATE1997_3.5 top http://gateoverflow.in/2236

Locality of reference implies that the page reference being made by a process

A. will always be to the page used in the previous page reference
B. is likely to be to one of the pages used in the last few page references
C. will always be to one of the pages existing in memory
D. will always lead to a page fault

gate1997 operating-system page-replacement easy

Answer

5.21.10 Page Replacement: GATE1997_3.9 top http://gateoverflow.in/2240

Thrashing

A. reduces page I/O
B. decreases the degree of multiprogramming
C. implies excessive page I/O
D. improve the system performance

gate1997 operating-system page-replacement easy

Answer

5.21.11 Page Replacement: GATE2002-1.23 top http://gateoverflow.in/828

The optimal page replacement algorithm will select the page that

A. Has not been used for the longest time in the past
B. Will not be used for the longest time in the future
C. Has been used least number of times
D. Has been used most number of times

gate2002 operating-system page-replacement easy

Answer

5.21.12 Page Replacement: GATE2004-21, ISRO2007-44 top http://gateoverflow.in/1018

The number of page frames that must be allocated to a running process in a virtual memory environment is determined by

A. the instruction set architecture
B. page size
C. number of processes in memory
D. physical memory size

gate2004 operating-system virtual-memory page-replacement normal isro2007

Answer

5.21.13 Page Replacement: GATE2005-22, ISRO2015-36 top http://gateoverflow.in/1358

Increasing the RAM of a computer typically improves performance because:

A. Virtual Memory increases

B. Larger RAMs are faster

C. Fewer page faults occur

D. Fewer segmentation faults occur

gate2005 operating-system page-replacement easy isro2015

Answer

5.21.14 Page Replacement: GATE2007-56 top http://gateoverflow.in/1254

A virtual memory system uses First In First Out (FIFO) page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:

P: Increasing the number of page frames allocated to a process sometimes increases the page fault rate.

Q: Some programs do not exhibit locality of reference.

Which one of the following is TRUE?

A. Both P and Q are true, and Q is the reason for P

B. Both P and Q are true, but Q is not the reason for P.

C. P is false but Q is true

D. Both P and Q are false.

gate2007 operating-system page-replacement normal

Answer

5.21.15 Page Replacement: GATE2007-82 top
http://gateoverflow.in/1274

A process, has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references (reference string): **1, 2, 1, 3, 7, 4, 5, 6, 3, 1**

If optimal page replacement policy is used, how many page faults occur for the above reference string?

A. 7
B. 8
C. 9
D. 10

gate2007 operating-system page-replacement normal

Answer

5.21.16 Page Replacement: GATE2007-83 top
http://gateoverflow.in/43510

A process, has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references (reference string): 1, 2, 1, 3, 7, 4, 5, 6, 3, 1

Least Recently Used (LRU) page replacement policy is a practical approximation to optimal page replacement. For the above reference string, how many more page faults occur with LRU than with the optimal page replacement policy?

A. 0
B. 1
C. 2
D. 3

gate2007 normal operating-system page-replacement

Answer

5.21.17 Page Replacement: GATE2007-IT-12 top
http://gateoverflow.in/3445

The address sequence generated by tracing a particular program executing in a pure demand paging system with 100 bytes per page is

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0410.

Suppose that the memory can store only one page and if x is the address which causes a page fault then the bytes from addresses x to x + 99 are loaded on to the memory.

How many page faults will occur ?

A. 0
B. 4
C. 7
D. 8

gate2007-it operating-system virtual-memory page-replacement normal

Answer

5.21.18 Page Replacement: GATE2007-IT-58 top
http://gateoverflow.in/3500

A demand paging system takes 100 time units to service a page fault and 300 time units to replace a dirty page. Memory access time is 1 time unit. The probability of a page fault is p. In case of a page fault, the probability of page being dirty is also p. It is observed that the average access time is 3 time units. Then the value of p is

A. 0.194
B. 0.233
C. 0.514
D. 0.981

gate2007-it operating-system page-replacement probability normal

Answer

5.21.19 Page Replacement: GATE2012_42 top
http://gateoverflow.in/2150

Consider the virtual page reference string

1, 2, 3, 2, 4, 1, 3, 2, 4, 1

on a demand paged virtual memory system running on a computer system that has main memory size of 3 page frames which are initially empty. Let LRU, $FIFO$ and $OPTIMAL$ denote the number of page faults under the corresponding page replacement policy. Then

(A) $OPTIMAL < LRU < FIFO$
(B) $OPTIMAL < FIFO < LRU$
(C) $OPTIMAL = LRU$
(D) $OPTIMAL = FIFO$

gate2012 operating-system page-replacement normal

Answer

5.21.20 Page Replacement: GATE2014-1-33 top http://gateoverflow.in/1805

Assume that there are 3 page frames which are initially empty. If the page reference string is 1, 2, 3, 4, 2, 1, 5, 3, 2, 4, 6, the number of page faults using the optimal replacement policy is__________.

gate2014-1 operating-system page-replacement numerical-answers

Answer

5.21.21 Page Replacement: GATE2014-2-33 top http://gateoverflow.in/1992

A computer has twenty physical page frames which contain pages numbered 101 through 120. Now a program accesses the pages numbered 1, 2, ..., 100 in that order, and repeats the access sequence **THRICE**. Which one of the following page replacement policies experiences the same number of page faults as the optimal page replacement policy for this program?

A. Least-recently-used
B. First-in-first-out
C. Last-in-first-out
D. Most-recently-used

gate2014-2 operating-system page-replacement easy

Answer

5.21.22 Page Replacement: GATE2014-3-20 top http://gateoverflow.in/2054

A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (**LRU**) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string given below?

4, 7, 6, 1, 7, 6, 1, 2, 7, 2

gate2014-3 operating-system page-replacement numerical-answers normal

Answer

5.21.23 Page Replacement: GATE2015-1_47 top http://gateoverflow.in/8353

Consider a main memory with five page frames and the following sequence of page references: 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3. Which one of the following is true with respect to page replacement policies First In First Out (FIFO) and Least Recently Used (LRU)?

A. Both incur the same number of page faults
B. FIFO incurs 2 more page faults than LRU
C. LRU incurs 2 more page faults than FIFO
D. FIFO incurs 1 more page faults than LRU

gate2015-1 operating-system page-replacement normal

Answer

5.21.24 Page Replacement: GATE2017-1-40 top http://gateoverflow.in/118323

Recall that Belady's anomaly is that the page-fault rate may *increase* as the number of allocated frames increases. Now, consider the following statement:

S1: *Random page replacement* algorithm (where a page chosen at random is replaced) suffers from Belady's anomaly.

S2: *LRU page replacement* algorithm suffers from Belady's anomaly.

Which of the following is CORRECT?

(A) S1 is true, S2 is true

(B) S1 is true, S2 is false

(C) S1 is false, S2 is true

(D) S1 is false, S2 is false

gate2017-1 page-replacement operating-system normal

Answer

5.21.25 Page Replacement: TIFR2013-B-14 top

http://gateoverflow.in/25794

Assume a demand paged memory system where ONLY THREE pages can reside in the memory at a time. The following sequence gives the order in which the program references the pages.

$$1, 3, 1, 3, 4, 2, 2, 4$$

Assume that least frequently used page is replaced when necessary. If there is more than one least frequently used pages then the least recently used page among them is replaced. During the program's execution, how many times will the pages $1, 2, 3$ and 4 be brought to the memory?

a. $2, 2, 2, 2$ times, respectively
b. $1, 1, 1, 2$ times, respectively
c. $1, 1, 1, 1$ times, respectively
d. $2, 1, 2, 2$ times, respectively
e. None of the above

tifr2013 operating-system page-replacement

Answer

Answers: Page Replacement

5.21.1 Page Replacement: GATE 2016-1-49 top

http://gateoverflow.in/39711

Selected Answer

Ans is 1

In LIFO first 20 are page faults followed by next 9 hits then next 11 page faults. (After a_{10}, a_{11} replaces a_{10}, a_{12} replaces a_{11} and so on)

In optimal first 20 are page faults followed by next 9 hits then next 10 page faults followed by last page hit.

28 votes -- Krishna murthy (381 points)

5.21.2 Page Replacement: GATE 2016-2-20 top

http://gateoverflow.in/39559

Selected Answer

Option D.FIFO suffers from Belady's anomaly.

:D check this out

http://gateoverflow.in/1301/gate2009_9

http://gateoverflow.in/1254/gate2007_56

http://gateoverflow.in/2595/gate1995_1-8

8 votes -- Shashank Chavan (3.4k points)

5.21.3 Page Replacement: GATE1993_21 top http://gateoverflow.in/2318

LRU : 1,2,3,4,5,2,4,3,2
FIFO : 1,2,3,4,5,1,2,3

5 votes -- Digvijay (47k points)

5.21.4 Page Replacement: GATE1994_1.13 top http://gateoverflow.in/2454

Selected Answer

FIFO replaces a page which was brought into memory first will be removed first so since variable was initialized very early. it is in the set of first in pages. so it will be removed answer: b if you use LRU - since it is used constantly it is a recently used item always. so cannot be removed. If you use LFU - the frequency of the page is more since it is in constant use. So cannot be replaced

13 votes -- Sankaranarayanan P.N (11.2k points)

5.21.5 Page Replacement: GATE1994_1.24 top http://gateoverflow.in/2467

Selected Answer

In first fit, block request will be satisfied from the first free block that fits it.

So, request for 300 will be satisfied by 350 size block reducing the free size to 50.
Request for 25, satisfied by 125 size block, reducing it to 125.
Request for 125 satisfied by 125 size block.
And request for 50 satisfied by the 50 size block.
So, all requests can be satisfied.

In best fit strategy, a block request is satisfied by the smallest block in that can fit it.
So, request for 200 will be satisfied by 350 size block reducing the free size to 50.
Request for 25, satisfied by 50 size block as its the smallest size that fits 25, reducing it to 25.
Request for 125, satisfied by 150 size block, reducing it to 25.
Now, request for 50 cannot be satisfied as the two 25 size blocks are not contiguous.

So, answer (b)

14 votes -- Arjun Suresh (294k points)

5.21.6 Page Replacement: GATE1995_1.8 top http://gateoverflow.in/2595

Selected Answer

ans is C

FIFO sufferes from Belady's anomaly. Optimal replacement never suffers from Belady's anomaly.

6 votes -- jayendra (8.1k points)

5.21.7 Page Replacement: GATE1995_2.7 top http://gateoverflow.in/2619

Selected Answer

0100 - 1 page fault. Records 0100-0199 in memory

0200 - 2 page faults. Records 0200-0299 in memory

0430 - 3 page faults. Records 0400-0499 in memory

0499 - 3 page faults. Records 0400-0499 in memory

0510 - 4 page faults. Records 0500-0599 in memory

0530 - 4 page faults. Records 0500-0599 in memory

0560 - 4 page faults. Records 0500-0599 in memory

0120 - 5 page faults. Records 0100-0199 in memory

0220 - 6 page faults. Records 0200-0299 in memory

0240 - 6 page faults. Records 0200-0299 in memory

0260 - 6 page faults. Records 0200-0299 in memory

0320 - 7 page faults. Records 0300-0399 in memory

0370 - 7 page faults. Records 0300-0399 in memory

So, C - 7 page faults.

17 votes -- Arjun Suresh (294k points)

5.21.8 Page Replacement: GATE1997-3.10, ISRO2008-57, ISRO2015-64 http://gateoverflow.in/2241

top

Selected Answer

The dirty bit allows for a performance optimization. A page on disk that is paged in to physical memory, then read from, and subsequently paged out again does not need to be written back to disk, since the page hasn't changed. However, if the page was written to after it's paged in, its dirty bit will be set, indicating that the page must be written back to the backing store answer: a

19 votes -- Sankaranarayanan P.N (11.2k points)

ans is A...to perform any write operation on page firstly we check the dirty bit status...dirty bit will be set when page will be modified(suppose s=1 set condition) and it will remain s=1(set) until the page modified will write back into the memory..if page was not modified then it will not change the dirty bit value i.e.s=0...now suppose we perform write operation on page then its dirty bit become s=1..and suppose after some time we were performing write operation on that page then firstly we check the dirty bit value here its value is 1 it means page was modified..so firstly we write that page to memory and then perform any modification by this way we were avoiding unnecessary write operation on paging device

10 votes -- neha pawar (4.4k points)

5.21.9 Page Replacement: GATE1997_3.5 top http://gateoverflow.in/2236

Selected Answer

Answer is B

Locality of reference is also called as principle of locality. It means that same data values or related storage locations are frequently accessed. This in turn saves time. There are mainly three types of principle of locality:

1) temporal locality

2) spatial locality

3) sequential locality

This is required because in programs related data are stored in consecutive locations and in loops same locations are referred again and again

9 votes -- Neeraj7375 (769 points)

5.21.10 Page Replacement: GATE1997_3.9 top http://gateoverflow.in/2240

Selected Answer

C. implies excessive page i/o

http://en.wikipedia.org/wiki/Thrashing_%28computer_science%29

13 votes -- Sankaranarayanan P.N (11.2k points)

5.21.11 Page Replacement: GATE2002-1.23 top http://gateoverflow.in/828

Selected Answer

Optimal page replacement algorithm will always select the page that will not be used for the longest time in the future for replacement, and that is why the it is called optimal page replacement algorithm. Hence, (B) choice.

14 votes -- Arjun Suresh (294k points)

5.21.12 Page Replacement: GATE2004-21, ISRO2007-44 top http://gateoverflow.in/1018

Selected Answer

Its instruction architecture architecture .if you have no indirect addressing then you need atleast two pages in physical memory. one for instruction (code part) and another for if the data references memory.if there is one level of indirection then you will need atleast three pages one for the instruction(code) and another two for the indirect addressing. if there three indirection then minimum 4 frames are allocated.

http://stackoverflow.com/questions/11213013/minimum-page-frames

11 votes -- Prasanna Ranganathan (4.3k points)

5.21.13 Page Replacement: GATE2005-22, ISRO2015-36 top http://gateoverflow.in/1358

Selected Answer

So Answer -> C

1. Virtual Memory increases -> This option is false. Because Virtual Memory of Computer do not depend on RAM. Virtual Memory concept iteself was introduced so Programs larger than RAM can be executed.
2. Larger RAMs are faster -> No This option is false. Size of ram does not determine it's speed, Type of ram does, SRAM is faster, DRAM is slower.
3. Fewer page faults occur -> This is true, more pages can be in Main memory .
4. Fewer segmentation faults occur -> "Segementation Fault"-> A **segmentation fault** (aka segfault) is a common condition that causes programs to crash; they are often associated with a file named core . Segfaults are caused by a program trying to read or write an illegal memory location. It is clear that segmentation fault is not related to size of main memory. This is false.

23 votes -- Akash (43.8k points)

5.21.14 Page Replacement: GATE2007-56 top http://gateoverflow.in/1254

Selected Answer

P: Increasing the number of page frames allocated to a process sometimes increases the page fault rate.

This is true,

example :- FIFO suffers from [Bélády's anomaly](#) which means that on Increasing the number of page frames allocated to a process it may sometimes increase the total number of page faults.

Q: Some programs do not exhibit locality of reference.

This is true :- it is easy to write a program which jumps around a lot & which do not exhibit locality of reference.

Example :- Assume that array is stored in Row Major order & We are accessing it in column major order !

So answer = **option B** (As there is no relation between P & Q. As it is clear from example, they are independent.)

21 votes -- Akash (43.8k points)

5.21.15 Page Replacement: GATE2007-82 top http://gateoverflow.in/1274

Selected Answer

Optimal replacement policy

1 1 1 1 1

2 7 4 5 6

3 3 3 3 3

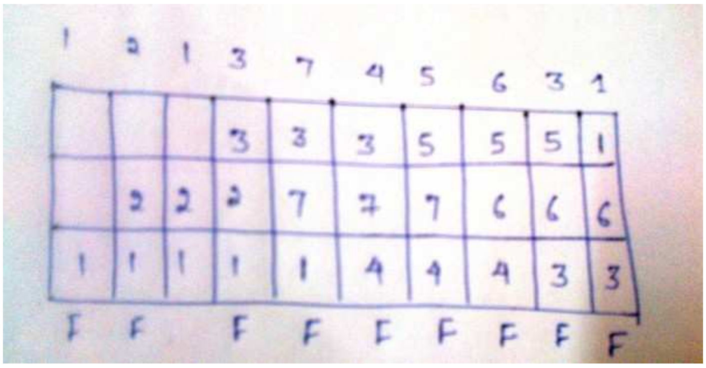
For Pages 1 2 3 6 4 5 6 bpage fault occur so ans for 82 is a

6 votes -- Pooja Palod (32.4k points)

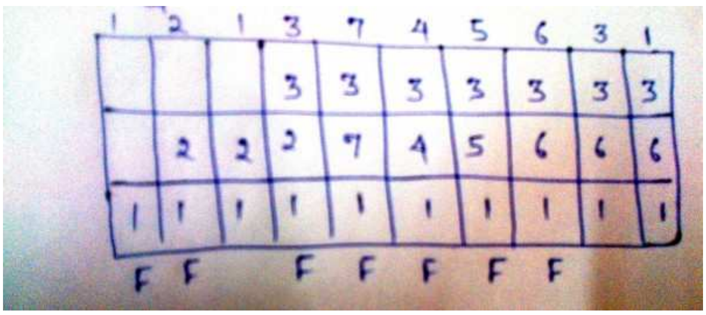
5.21.16 Page Replacement: GATE2007-83 top http://gateoverflow.in/43510

Selected Answer

Using LRU = 9 Page Fault



Using Optimal= 7 Page Fault



So LRU-OPTIMAL =2

option B

9 votes -- Manoj Kumar (37.5k points)

5.21.17 Page Replacement: GATE2007-IT-12 top

http://gateoverflow.in/3445

Selected Answer

0100 - page fault, addresses till 199 in memory

0200 - page fault, addresses till 299 in memory

0430 - page fault, addresses till 529 in memory

0499 - no page fault

0510 - no page fault

0530 - page fault, addresses till 629 in memory

0560 - no page fault

0120 - page fault, addresses till 219 in memory

0220 - page fault, addresses till 319 in memory

0240 - no page fault

0260 - no page fault

0320 - page fault, addresses till 419 in memory

0410 - no page fault

So, 7 is the answer- (C)

28 votes -- Arjun Suresh (294k points)

5.21.18 Page Replacement: GATE2007-IT-58 top

http://gateoverflow.in/3500

Selected Answer

$p(p * 300 + (1-p) * 100) + (1-p) * 1 = 3$

$p(300p + 100 - 100p) + 1-p=3$

$200p^2 + 99p - 2=0$

$p \approx 0.0194$

23 votes -- Laxmi (873 points)

5.21.19 Page Replacement: GATE2012_42 top

http://gateoverflow.in/2150

Selected Answer

Page fault for LRU=9, FIFO=6, OPTIMAL=5

Ans (B)

7 votes -- Keith Kr (6.3k points)

5.21.20 Page Replacement: GATE2014-1-33 top http://gateoverflow.in/1805

Selected Answer

Ans : initially all empty frames fill by 1,2,3 so all time page fault which is 3 .

then next 4 was not available in frame set so **we look at ahead of request which was coming last** we replace 4 with that so 3 will be replace by 4 and like wise next 2 and 1 is present already so no page fault and then next 5 is not present so replace with 1 and then 3 was not present and replace with 5 and then 2 and 4 are present already so no page fault and then last 6th was not already there so page fault.

So total page fault at : 1 , 2 , 3 , 4 , 5 , 3 , 6 . so, total 7 page fault occur ...

12 votes -- Jay (1.2k points)

5.21.21 Page Replacement: GATE2014-2-33 top http://gateoverflow.in/1992

Selected Answer

It will be D i.e Most-recently-used.

To be clear "repeats the access sequence THRICE" means totally the sequence of page numbers are accessed 4 times though this is not important for the answer here.

If we go optimal page replacement algorithm it replaces the page which will be least used in near future.

Now we have frame size 20 and reference string is

$$1, 2, \ldots, 100, 1, 2, \ldots, 100, 1, 2, \ldots, 100, 1, 2, \ldots, 100$$

First 20 accesses will cause page faults - the initial pages are no longer used and hence optimal page replacement replaces them first. Now, for page 21, according to reference string page 1 will be used again after 100 and similarly 2 will be used after 1 so on and so the least likely to be used page in future is page 20. So for 21^{st} reference Page 20 will be replaced and then for 22^{nd} page reference, page 21 will be replaced and so on which is MOST RECENTLY USED page replacement policy.

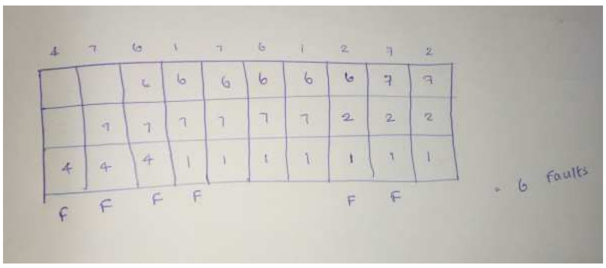
PS: Even for Most Recently Used page replacement at first all empty (invalid) pages frames are replaced and then only most recently used ones are replaced.

17 votes -- Kalpish Singhal (2.1k points)

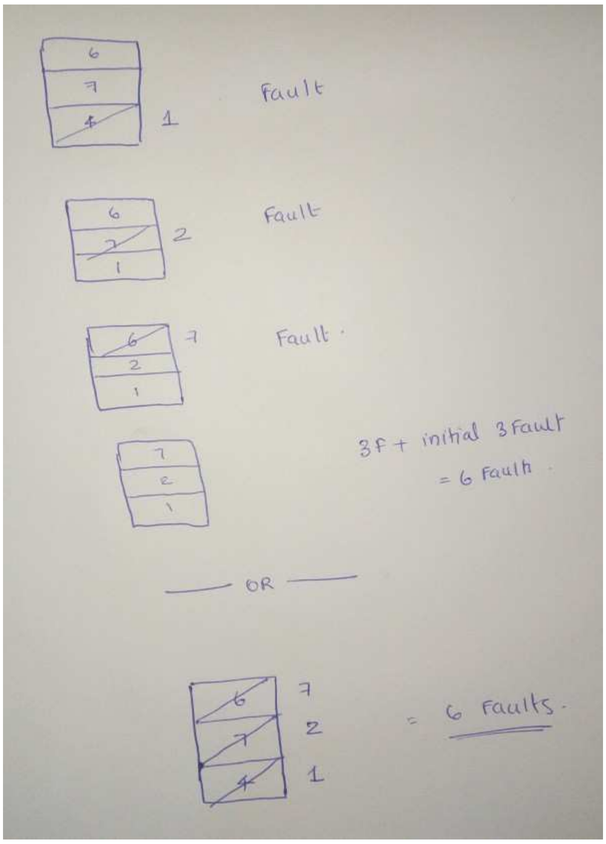
5.21.22 Page Replacement: GATE2014-3-20 top http://gateoverflow.in/2054

Selected Answer

Total page fault 6



Another way of answering the same



5 votes -- pC (21.4k points)

5.21.23 Page Replacement: GATE2015-1_47 top

http://gateoverflow.in/8353

Selected Answer

Requested Page references 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3

and no. of page frame size is 5.

In FIFO Page replacement will take place in sequence in pattern First In first Out, as following

Request	**3**	**8**	**2**	**3**	**9**	**1**	**6**	**3**	**8**	**9**	**3**	**6**	**2**	**1**	**3**
Frame 5						1	1	1	1	1	1	1	1	1	1
Frame 4					9	9	9	9	9	9	9	9	9	2	2
Frame 3			2	2	2	2	2	2	8	8	8	8	8	8	8
Frame 2		8	8	8	8	8	8	3	3	3	3	3	3	3	3
Frame 1	3	3	3	3	3	3	6	6	6	6	6	6	6	6	6
Miss/Hit	F	F	F	H	F	F	F	F	F	H	H	H	H	F	H

No. of Faults = 9 No. of Hits = 6

Using Least Recently Used (LRU) page replacement will be the page which is visited least recently (which is not used by long time), as following

Request	**3**	**8**	**2**	**3**	**9**	**1**	**6**	**3**	**8**	**9**	**3**	**6**	**2**	**1**	**3**
Frame 5						1	1	1	1	1	1	1	2	2	2
Frame 4					9	9	9	9	9	9	9	9	9	9	9
Frame 3			2	2	2	2	2	2	8	8	8	8	8	1	1
Frame 2		8	8	8	8	8	6	6	6	6	6	6	6	6	6
Frame 1	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
Hit/Miss	F	F	F	H	F	F	F	H	F	H	H	H	F	F	H

No. of Faults = 9 No. of Hits = 6

So, both incur the same number of page faults.

12 votes -- Raghuveer Dhakad (1.2k points)

5.21.24 Page Replacement: GATE2017-1-40 top http://gateoverflow.in/118323

Selected Answer

A page replacement algorithm suffers from Belady's anamoly when it is not a stack algorithm.

A stack algorithm is one that satisfies the inclusion property. The inclusion property states that, at a given time, the contents(pages) of a memory of size k page-frames is a subset of the contents of memory of size k+1 page-frames, for the same sequence of accesses. The advantage is that running the same algorithm with more pages(i.e. larger memory) will never increase the number of page faults.

Is LRU a stack algorithm?

Yes, LRU is a stack algorithm. Therefore, it doesn't suffer from Belady's anamoly.

Ref :Ref1 and Ref2

Is Random page replacement algorithm a stack algorithm?

No, as it may choose a page to replace in FIFO manner or in a manner which does not satisfy inclusion property. This means it could suffer from Belady's anamoly.

$\therefore$ B should be answer.

9 votes -- Kantikumar (3.5k points)

5.21.25 Page Replacement: TIFR2013-B-14 top http://gateoverflow.in/25794

Selected Answer

Page reference order:1,3,1,3, 4,2,2,4

First 2 pages causes page fault...ie 1 and 3

Next 2 pages no fault

Next page ie 4 fault occurs

Now for page no 2 we have fault..we will replace less frequently used ie 4

Next page is again 2 so no page fault

Now page no 1 2 and 3 all are used 2 times so we will replace page 1 to accomodate page 4(least recently used is 1)

So page 1 2 3 are brought once in memory and page 4 is brought two times so ans is b

15 votes -- Pooja Palod (32.4k points)

5.22 Precedence Graph(2) top

5.22.1 Precedence Graph: GATE1991_01,xii top http://gateoverflow.in/508

A given set of processes can be implemented by using only **parbegin/parend** statement, if the precedence graph of these processes is _______

gate1991 operating-system normal precedence-graph

Answer

5.22.2 Precedence Graph: GATE1992-12a top http://gateoverflow.in/591

Draw the precedence graph for the concurrent program given below

```
S1
parbegin
    begin
        S2:S4
    end;
    begin
        S3;
        parbegin
            S5;
            begin
                S6:S8
            end
        parend
    end;
    S7
parend;
S9
```

gate1992 operating-system normal concurrency precedence-graph

Answer

Answers: Precedence Graph

5.22.1 Precedence Graph: GATE1991_01,xii top http://gateoverflow.in/508

Selected Answer

A given set of processes can be implemented by using only **parbegin/parend**statement, if the precedence graph of these processes is **properly nested**

ref :http://nob.cs.ucdavis.edu/classes/ecs150-2008-04/handouts/sync.pdf

1. it should be closed under par begin and par end ...

2. process execute concurrently ....

http://gateoverflow.in/1739/gate1998_24#viewbutton

in this question precedence graph is nested ....

1) all the process execute concurrently ..closed under par begin and par end ..

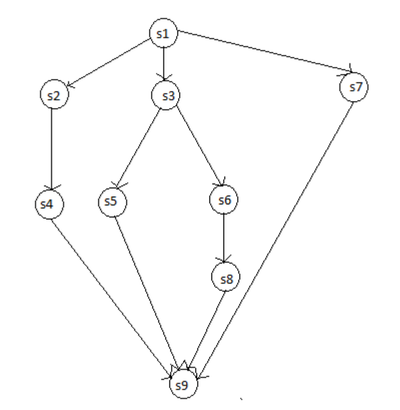
2) if you see all the serial execution come then signal the resource and and parallel process down the value (resource) similar all the process which are which are dependent to other one , other one release the resource then it will be got that with down ..and after release the its own resource .. in the sense all the process are executing concurrently ...

8 votes -- sonam vyas (13.2k points)

5.22.2 Precedence Graph: GATE1992-12a top http://gateoverflow.in/591

Selected Answer

parbegin-parend shows parallel execution while begin-end shows serial execution

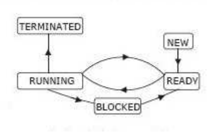


7 votes -- Sheshang M. Ajwalia (2.8k points)

5.23 Process(4) top

5.23.1 Process: GATE1996-1.18 top http://gateoverflow.in/2722

The process state transition diagram in the below figure is representative of



A. a batch operating system
B. an operating system with a preemptive scheduler
C. an operating system with a non-preemptive scheduler
D. a uni-programmed operating system

gate1996 operating-system normal process

Answer

5.23.2 Process: GATE2001-2.20 top http://gateoverflow.in/738

Which of the following does not interrupt a running process?

A. A device
B. Timer
C. Scheduler process
D. Power failure

gate2001 operating-system easy process

Answer

5.23.3 Process: GATE2002-2.21 top http://gateoverflow.in/851

Which combination of the following features will suffice to characterize an OS as a multi-programmed OS?

a. More than one program may be loaded into main memory at the same time for execution
b. If a program waits for certain events such as I/O, another program is immediately scheduled for execution
c. If the execution of a program terminates, another program is immediately scheduled for execution.
    A. a
    B. a and b
    C. a and c

D. a, b and c

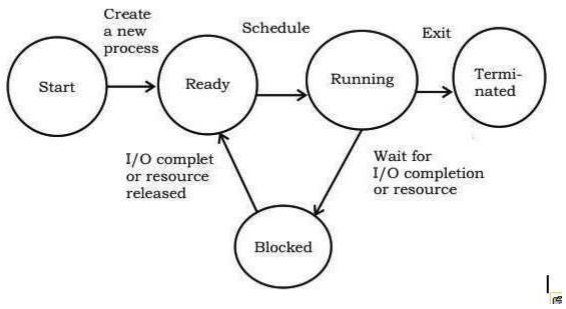
gate2002 operating-system normal process

Answer

5.23.4 Process: GATE2006-IT-13 top http://gateoverflow.in/3552

The process state transition diagram of an operating system is as given below.

Which of the following must be FALSE about the above operating system?



A. It is a multiprogrammed operating system
B. It uses preemptive scheduling
C. It uses non-preemptive scheduling
D. It is a multi-user operating system

gate2006-it operating-system normal process

Answer

Answers: Process

5.23.1 Process: GATE1996-1.18 top http://gateoverflow.in/2722

Selected Answer

Answer is B. The transition from running to ready indicates that the process in the running state can be preempted and bought back to ready state.

13 votes -- kireeti (1.1k points)

5.23.2 Process: GATE2001-2.20 top http://gateoverflow.in/738

Selected Answer

ans is C.

Timer and disk both makes interrupt and power failure will also interrupt the system. Only a scheduler process will not interrupt the running process as schduler process gets called only when no other process is running (preemption if any would have happened before scheduler starts execution).

Quote from wikipedia

> In the Linux kernel, the scheduler is called after each timer interrupt (that is, quite a few times per second). It determines what process to run next based on a variety of factors, including priority, time already run, etc. The implementation of preemption in other kernels is likely to be similar.

https://www.quora.com/How-does-the-timer-interrupt-invoke-the-process-scheduler

18 votes -- jayendra (8.1k points)

5.23.3 Process: GATE2002-2.21 top

http://gateoverflow.in/851

Selected Answer

A and B suffice multi programming concept For multi programming more than one program should be in memory and if any program goes for Io another can be scheduled to use CPU so ans is b

24 votes -- Pooja Palod (32.4k points)

5.23.4 Process: GATE2006-IT-13 top

http://gateoverflow.in/3552

Selected Answer

Answer B

Explanation :-

A) It is a multiprogrammed operating system

Correct, it has ready state. We can have multiple processes in ready state here so this is Multiprogrammed OS.

B) It uses preemptive scheduling

False :- There is no arrow transition from running to read state. So this is non preemptive.

C) It uses non-preemptive scheduling

True.

D) It is a multi-user operating system

We can have multiple user processes in ready state. So this is also correct.

12 votes -- Akash (43.8k points)

5.24 Process Schedule(36) top

5.24.1 Process Schedule: GATE 2016-1-20 top

http://gateoverflow.in/39655

Consider an arbitrary set of CPU-bound processes with unequal CPU burst lengths submitted at the same time to a computer system. Which one of the following process scheduling algorithms would minimize the average waiting time in the ready queue?

A. Shortest remaining time first
B. Round-robin with the time quantum less than the shortest CPU burst
C. Uniform random
D. Highest priority first with priority proportional to CPU burst length

gate2016-1 operating-system process-schedule normal

Answer

5.24.2 Process Schedule: GATE1990-1-vi top

http://gateoverflow.in/83850

Fill in the blanks:

The highest-response ratio next scheduling policy favours ___________ jobs, but it also limits the waiting time of _________ jobs.

gate1990 operating-system process-schedule

Answer

5.24.3 Process Schedule: GATE1993_7.10 top

http://gateoverflow.in/2298

Assume that the following jobs are to be executed on a single processor system

Job Id	CPU Burst Time
p	4
q	1
r	8
s	1
t	2

The jobs are assumed to have arrived at time 0^+ and in the order p, q, r, s, t. Calculate the departure time (completion time) for job p if scheduling is round robin with time slice 1

(a). 4

(b). 10

(c). 11

(d). 12

(e). None of the above

gate1993 operating-system process-schedule normal

Answer

5.24.4 Process Schedule: GATE1995_1.15 top

http://gateoverflow.in/2602

Which scheduling policy is most suitable for a time shared operating system?

A. Shortest Job First
B. Round Robin
C. First Come First Serve
D. Elevator

gate1995 operating-system process-schedule easy

Answer

5.24.5 Process Schedule: GATE1995_2.6 top

http://gateoverflow.in/2618

The sequence .... is an optimal non-preemptive scheduling sequence for the following jobs which leaves the CPU idle for .... unit(s) of time.

Job	Arrival Time	Burst Time
1	0.0	9
2	0.6	5
3	1.0	1

A. $\{3, 2, 1\}, 1$
B. $\{2, 1, 3\}, 0$
C. $\{3, 2, 1\}, 0$
D. $\{1, 2, 3\}, 5$

gate1995 operating-system process-schedule normal

Answer

5.24.6 Process Schedule: GATE1996-2.20, ISRO2008-15 top

http://gateoverflow.in/2749

Four jobs to be executed on a single processor system arrive at time 0 in the order A, B, C, D. Their burst CPU time requirements are $4, 1, 8, 1$ time units respectively. The completion time of A under round robin scheduling with time slice of one time unit is

A. 10
B. 4
C. 8
D. 9

gate1996 operating-system process-schedule normal isro2008

Answer

5.24.7 Process Schedule: GATE1998-2.17, UGCNET-Dec2012-III-43 top http://gateoverflow.in/1690

Consider n processes sharing the CPU in a round-robin fashion. Assuming that each process switch takes s seconds, what must be the quantum size q such that the overhead resulting from process switching is minimized but at the same time each process is guaranteed to get its turn at the CPU at least every t seconds?

A. $q \leq \frac{t-ns}{n-1}$

B. $q \geq \frac{t-ns}{n-1}$

C. $q \leq \frac{t-ns}{n+1}$

D. $q \geq \frac{t-ns}{n+1}$

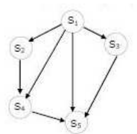
gate1998 operating-system process-schedule normal ugcnetdec2012iii

Answer

5.24.8 Process Schedule: GATE1998_24 top http://gateoverflow.in/1739

a. Four jobs are waiting to be run. Their expected run times are 6, 3, 5 and x. In what order should they be run to minimize the average response time?

b. Write a concurrent program using par begin-par end to represent the precedence graph shown below.



gate1998 operating-system process-schedule descriptive

Answer

5.24.9 Process Schedule: GATE1998_7b top http://gateoverflow.in/12963

a. In a computer system where the 'best-fit' algorithm is used for allocating 'jobs' to 'memory partitions', the following situation was encountered:

Partitions size in KB	4K 8K 20K 2K
Job sizes in KB	2K 14K 3K 6K 6K 10K 20K 2K
Time for execution	4 10 2 1 4 1 8 6

When will the 20K job complete?

gate1998 operating-system process-schedule normal

Answer

5.24.10 Process Schedule: GATE2002_1.22 top http://gateoverflow.in/827

Which of the following scheduling algorithms is non-preemptive?

A. Round Robin
B. First-In First-Out
C. Multilevel Queue Scheduling
D. Multilevel Queue Scheduling with Feedback

gate2002 operating-system process-schedule easy

Answer

5.24.11 Process Schedule: GATE2003-77 top

http://gateoverflow.in/963

A uni-processor computer system only has two processes, both of which alternate 10 ms CPU bursts with 90 ms I/O bursts. Both the processes were created at nearly the same time. The I/O of both processes can proceed in parallel. Which of the following scheduling strategies will result in the *least* CPU utilization (over a long period of time) for this system?

A. First come first served scheduling

B. Shortest remaining time first scheduling

C. Static priority scheduling with different priorities for the two processes

D. Round robin scheduling with a time quantum of 5 ms

gate2003 operating-system process-schedule normal

Answer

5.24.12 Process Schedule: GATE2004-46 top

http://gateoverflow.in/1043

Consider the following set of processes, with the arrival times and the CPU-burst times gives in milliseconds.

Process	**Arrival Time**	**Burst Time**
P1	0	5
P2	1	3
P3	2	3
P4	4	1

What is the average turnaround time for these processes with the preemptive shortest remaining processing time first (SRPT) algorithm?

A. 5.50
B. 5.75
C. 6.00
D. 6.25

gate2004 operating-system process-schedule normal

Answer

5.24.13 Process Schedule: GATE2005-IT-60 top

http://gateoverflow.in/3821

We wish to schedule three processes P1, P2 and P3 on a uniprocessor system. The priorities, CPU time requirements and arrival times of the processes are as shown below.

Process	Priority	CPU time required	Arrival time (hh:mm:ss)
P1	10(highest)	20 sec	00:00:05
P2	9	10 sec	00:00:03
P3	8 (lowest)	15 sec	00:00:00

We have a choice of preemptive or non-preemptive scheduling. In preemptive scheduling, a late-arriving higher priority process can preempt a currently running process with lower priority. In non-preemptive scheduling, a late-arriving higher priority process must wait for the currently executing process to complete before it can be scheduled on the processor.

What are the turnaround times (time from arrival till completion) of P2 using preemptive and non-preemptive scheduling respectively?

A. 30 sec, 30 sec
B. 30 sec, 10 sec
C. 42 sec, 42 sec
D. 30 sec, 42 sec

gate2005-it operating-system process-schedule normal

Answer

5.24.14 Process Schedule: GATE2006-06, ISRO2009-14 top http://gateoverflow.in/885

Consider three CPU-intensive processes, which require 10, 20 and 30 time units and arrive at times 0, 2 and 6, respectively. How many context switches are needed if the operating system implements a shortest remaining time first scheduling algorithm? Do not count the context switches at time zero and at the end.

A. 1
B. 2
C. 3
D. 4

gate2006 operating-system process-schedule normal isro2009

Answer

5.24.15 Process Schedule: GATE2006-64 top http://gateoverflow.in/1842

Consider three processes (process id 0, 1, 2 respectively) with compute time bursts 2, 4 and 8 time units. All processes arrive at time zero. Consider the longest remaining time first (LRTF) scheduling algorithm. In LRTF ties are broken by giving priority to the process with the lowest process id. The average turn around time is:

A. 13 units
B. 14 units
C. 15 units
D. 16 units

gate2006 operating-system process-schedule normal

Answer

5.24.16 Process Schedule: GATE2006-65 top http://gateoverflow.in/1843

Consider three processes, all arriving at time zero, with total execution time of 10, 20 and 30 units, respectively. Each process spends the first 20% of execution time doing I/O, the next 70% of time doing computation, and the last 10% of time doing I/O again. The operating system uses a shortest remaining compute time first scheduling algorithm and schedules a new process either when the running process gets blocked on I/O or when the running process finishes its compute burst. Assume that all I/O operations can be overlapped as much as possible. For what percentage of time does the CPU remain idle?

A. 0%
B. 10.6%
C. 30.0%
D. 89.4%

gate2006 operating-system process-schedule normal

Answer

5.24.17 Process Schedule: GATE2006-IT-54 top http://gateoverflow.in/3597

The arrival time, priority, and duration of the CPU and I/O bursts for each of three processes P_1, P_2 and P_3 are given in the table below. Each process has a CPU burst followed by an I/O burst followed by another CPU burst. Assume that each process has its own I/O resource.

Process	Arrival time	Priority	Burst duration, CPU, I/O CPU

Process	Arrival time	Priority	Burst duration, CPU, I/O CPU
P_1	0	2	1, 5, 3
P_2	2	3 (lowest)	2, 3, 1
P_3	3	1 (highest)	2, 3, 1

The multi-programmed operating system uses preemptive priority scheduling. What are the finish times of the processes P_1, P_2 and P_3 ?

A. 11, 15, 9
B. 10, 15, 9
C. 11, 16, 10
D. 12, 17, 11

gate2006-it operating-system process-schedule normal

Answer

5.24.18 Process Schedule: GATE2007-16 top http://gateoverflow.in/1214

Group 1 contains some CPU scheduling algorithms and Group 2 contains some applications. Match entries in Group 1 to entries in Group 2.

Group I	Group II
(P) Gang Scheduling	(1) Guaranteed Scheduling
(Q) Rate Monotonic Scheduling	(2) Real-time Scheduling
(R) Fair Share Scheduling	(3) Thread Scheduling

A. P-3; Q-2; R-1
B. P-1; Q-2; R-3
C. P-2; Q-3; R-1
D. P-1; Q-3; R-2

gate2007 operating-system process-schedule normal

Answer

5.24.19 Process Schedule: GATE2007-55 top http://gateoverflow.in/1253

An operating system used Shortest Remaining System Time first (SRT) process scheduling algorithm. Consider the arrival times and execution times for the following processes:

Process	Execution Time	Arrival time
P1	20	0
P2	25	15
P3	10	30
P4	15	45

What is the total waiting time for process P2?

A. 5
B. 15
C. 40
D. 55

gate2007 operating-system process-schedule normal

Answer

5.24.20 Process Schedule: GATE2007-IT-26 top http://gateoverflow.in/3459

Consider n jobs $J_1, J_2 \dots J_n$ such that job J_i has execution time t_i and a non-negative integer weight w_i. The weighted mean completion time of the jobs is defined to be $\frac{\sum_{i=1}^{n} w_i T_i}{\sum_{i=1}^{n} w_i}$, where T_i is the completion time of job J_i. Assuming that there is only one processor available, in what order must the jobs be executed in order to minimize the weighted mean completion time of the jobs?

A. Non-decreasing order of t_i
B. Non-increasing order of w_i
C. Non-increasing order of $w_i t_i$
D. None-increasing order of w_i/t_i

gate2007-it operating-system process-schedule normal

Answer

5.24.21 Process Schedule: GATE2008-IT-55 top http://gateoverflow.in/3365

If the time-slice used in the round-robin scheduling policy is more than the maximum time required to execute any process, then the policy will

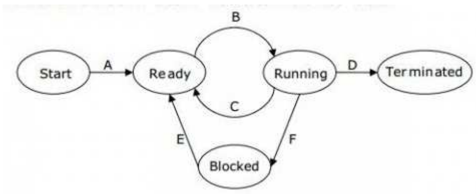
A. degenerate to shortest job first
B. degenerate to priority scheduling
C. degenerate to first come first serve
D. none of the above

gate2008-it operating-system process-schedule easy

Answer

5.24.22 Process Schedule: GATE2009-32 top http://gateoverflow.in/1318

In the following process state transition diagram for a uniprocessor system, assume that there are always some processes in the ready state:



Now consider the following statements:

I. If a process makes a transition D, it would result in another process making transition A immediately.
II. A process P_2 in blocked state can make transition E while another process P_1 is in running state.
III. The OS uses preemptive scheduling.
IV. The OS uses non-preemptive scheduling.

Which of the above statements are TRUE?

A. I and II
B. I and III
C. II and III
D. II and IV

gate2009 operating-system process-schedule normal

Answer

5.24.23 Process Schedule: GATE2010-25 top http://gateoverflow.in/2204

Which of the following statements are true?

I. Shortest remaining time first scheduling may cause starvation
II. Preemptive scheduling may cause starvation
III. Round robin is better than FCFS in terms of response time
  A. I only
  B. I and III only
  C. II and III only

D. I, II and III

gate2010 operating-system process-schedule easy

Answer

5.24.24 Process Schedule: GATE2011_35 top http://gateoverflow.in/2137

Consider the following table of arrival time and burst time for three processes P0, P1 and P2.

Process	Arrival Time	Burst Time
P0	0 ms	9 ms
P1	1 ms	4 ms
P2	2 ms	9 ms

The pre-emptive shortest job first scheduling algorithm is used. Scheduling is carried out only at arrival or completion of processes. What is the average waiting time for the three processes?

(A) 5.0 ms

(B) 4.33 ms

(C) 6.33 ms

(D) 7.33 ms

gate2011 operating-system process-schedule normal

Answer

5.24.25 Process Schedule: GATE2012_31 top http://gateoverflow.in/1749

Consider the 3 processes, P1, P2 and P3 shown in the table.

Process	Arrival time	Time Units Required
P1	0	5
P2	1	7
P3	3	4

The completion order of the 3 processes under the policies FCFS and RR2 (round robin scheduling with CPU quantum of 2 time units) are

(A) **FCFS**: P1, P2, P3 **RR2**: P1, P2, P3
(B) **FCFS**: P1, P3, P2 **RR2**: P1, P3, P2
(C) **FCFS**: P1, P2, P3 **RR2**: P1, P3, P2
(D) **FCFS**: P1, P3, P2 **RR2**: P1, P2, P3

gate2012 operating-system process-schedule normal

Answer

5.24.26 Process Schedule: GATE2013-10 top http://gateoverflow.in/1419

A scheduling algorithm assigns priority proportional to the waiting time of a process. Every process starts with zero (the lowest priority). The scheduler re-evaluates the process priorities every T time units and decides the next process to schedule. Which one of the following is **TRUE** if the processes have no I/O operations and all arrive at time zero?

A. This algorithm is equivalent to the first-come-first-serve algorithm.
B. This algorithm is equivalent to the round-robin algorithm.
C. This algorithm is equivalent to the shortest-job-first algorithm.
D. This algorithm is equivalent to the shortest-remaining-time-first algorithm.

gate2013 operating-system process-schedule normal

Answer

5.24.27 Process Schedule: GATE2014-1-32 top http://gateoverflow.in/1803

Consider the following set of processes that need to be scheduled on a single CPU. All the times are given in milliseconds.

Process Name	Arrival Time	Execution Time
A	0	6
B	3	2
C	5	4
D	7	6
E	10	3

Using the *shortest remaining time first* scheduling algorithm, the average process turnaround time (in msec) is ______________________.

gate2014-1 operating-system process-schedule numerical-answers normal

Answer

5.24.28 Process Schedule: GATE2014-2-32 top http://gateoverflow.in/1991

Three processes A, B and C each execute a loop of 100 iterations. In each iteration of the loop, a process performs a single computation that requires t_c CPU milliseconds and then initiates a single I/O operation that lasts for t_{io} milliseconds. It is assumed that the computer where the processes execute has sufficient number of I/O devices and the OS of the computer assigns different I/O devices to each process. Also, the scheduling overhead of the OS is negligible. The processes have the following characteristics:

Process id	t_c	t_{io}
A	100 ms	500 ms
B	350 ms	500 ms
C	200 ms	500 ms

The processes A, B, and C are started at times 0, 5 and 10 milliseconds respectively, in a pure time sharing system (round robin scheduling) that uses a time slice of 50 milliseconds. The time in milliseconds at which process C would ***complete*** its first I/O operation is ____________.

gate2014-2 operating-system process-schedule numerical-answers normal

Answer

5.24.29 Process Schedule: GATE2014-3-32 top http://gateoverflow.in/2066

An operating system uses *shortest remaining time first* scheduling algorithm for pre-emptive scheduling of processes. Consider the following set of processes with their arrival times and CPU burst times (in milliseconds):

Process	Arrival Time	Burst Time
P1	0	12
P2	2	4
P3	3	6
P4	8	5

The average waiting time (in milliseconds) of the processes is _______.

gate2014-3 operating-system process-schedule numerical-answers normal

Answer

5.24.30 Process Schedule: GATE2015-1_46 top http://gateoverflow.in/8330

Consider a uniprocessor system executing three tasks T_1, T_2 and T_3 each of which is composed of an infinite sequence of jobs (or instances) which arrive periodically at intervals of 3, 7 and 20 milliseconds, respectively. The priority of each task is the inverse of its period, and the available tasks are scheduled in order of priority, which is the highest priority task scheduled first. Each instance of T_1, T_2 and T_3 requires an execution time of 1, 2 and 4 milliseconds, respectively. Given that all tasks initially arrive at the beginning of the 1st millisecond and task preemptions are allowed, the first instance of T_3 completes its execution at the end of_____________________milliseconds.

gate2015-1 operating-system process-schedule normal numerical-answers

Answer

5.24.31 Process Schedule: GATE2015-3-34 top

http://gateoverflow.in/8492

For the processes listed in the following table, which of the following scheduling schemes will give the lowest average turnaround time?

Process	Arrival Time	Process Time
A	0	3
B	1	6
C	4	4
D	6	2

A. First Come First Serve
B. Non-preemprive Shortest job first
C. Shortest Remaining Time
D. Round Robin with Quantum value two

gate2015-3 operating-system process-schedule normal

Answer

5.24.32 Process Schedule: GATE2015-3_1 top

http://gateoverflow.in/8390

The maximum number of processes that can be in $Ready$ state for a computer system with n CPUs is :

A. n
B. n^2
C. 2^n
D. Independent of n

gate2015-3 operating-system process-schedule easy

Answer

5.24.33 Process Schedule: GATE2016-2-47 top

http://gateoverflow.in/39625

Consider the following processes, with the arrival time and the length of the CPU burst given in milliseconds. The scheduling algorithm used is preemptive shortest remaining-time first.

Process	Arrival Time	Burst Time
P_1	0	10
P_2	3	6
P_3	7	1
P_4	8	3

The average turn around time of these processes is ___________ milliseconds.

gate2016-2 operating-system process-schedule normal numerical-answers

Answer

5.24.34 Process Schedule: GATE2017-1-24 top http://gateoverflow.in/118304

Consider the following CPU processes with arrival times (in milliseconds) and length of CPU bursts (in milliseconds) as given below:

Process	Arrival Time	Burst Time
P1	0	7
P2	3	3
P3	5	5
P4	6	2

If the pre-emptive shortest remaining time first scheduling algorithm is used to schedule the processes, then the average waiting time across all processes is _____________ milliseconds.

gate2017-1 operating-system process-schedule numerical-answers

Answer

5.24.35 Process Schedule: GATE2017-2-51 top http://gateoverflow.in/118558

Consider the set of process with arrival time (in milliseonds) , CPU burst time (in millisecods) and priority (0 is the highest priority) shown below . None of the process have I/O burst time

Process	Arival Time	Burst Time	Priority
P1	0	11	2
P2	5	28	0
P3	12	2	3
P4	2	10	1
P5	9	16	4

The average waiting time (in milli seconds) of all the process using premtive priority scheduling algorithm is ______

gate2017-2 operating-system process-schedule numerical-answers

Answer

5.24.36 Process Schedule: ISI2015-CS-6b top http://gateoverflow.in/47333

Consider scheduling n processes $P_1, P_2, \dots, P_n$ which are created in this order at almost the same instant. Assume that all processes have exactly one CPU burst of duration D units (and no I/O bursts). Compute the average waiting time and average turn-around time if the scheduling policy is:

i. FCFS
ii. RR with time slice d units $(d < D)$.

Assume that it takes δ units of time to switch from one running process to another and Δ units of time to switch from a terminated process to a running process.

descriptive isi2015 operating-system process-schedule

Answer

Answers: Process Schedule

5.24.1 Process Schedule: GATE 2016-1-20 top http://gateoverflow.in/39655

Selected Answer

Answer should be A) SRTF

SJF minimizes average waiting time.. provably optimal..
Now here as all processes arrive at the same time, SRTF would be same as SJF.. and hence the answer

Reference: http://www.cs.columbia.edu/~junfeng/10sp-w4118/lectures/l13-sched.pdf See Slide 16,17 and 23

20 votes -- Abhilash Panicker (8.8k points)

5.24.2 Process Schedule: GATE1990-1-vi top http://gateoverflow.in/83850

Selected Answer

Highest response ratio next (**HRRN**) scheduling is a non-preemptive discipline, similar to shortest job next (SJN), in which the priority of each job is dependent on its estimated run time, and also the amount of time it has spent waiting.

Jobs gain higher priority the longer they wait, which prevents indefinite waiting or in other words what we say starvation. In fact, the jobs that have spent a long time waiting compete against those estimated to have short run times.

$$Priority = \frac{waiting\ time + estimated\ run\ time}{estimated\ run\ time} = 1 + \frac{waiting\ time}{estimated\ run\ time}$$

So the conclusion is it gives priority to those processes which have less burst time (or execution time) but also takes care of the waiting time of longer processes,thus preventing starvation.

So the answer is ***"shorter , longer"***

6 votes -- HABIB MOHAMMAD KHAN (76.8k points)

5.24.3 Process Schedule: GATE1993_7.10 top http://gateoverflow.in/2298

Selected Answer

Answer: C

Execution order: pqrstprtpr**p**rrrrr

7 votes -- Rajarshi Sarkar (35k points)

5.24.4 Process Schedule: GATE1995_1.15 top http://gateoverflow.in/2602

Selected Answer

Answer is Round Robin (RR) , option B .

Now question is Why RR is most suitable for time shared OS ?

First of all we are discussing about **Time shared O**S, so obviously **We need to consider pre-emption .**

So FCFS and Elevator these 2 options removed first , remain SJF and RR from two remaining options .

Now in case of pre-emptive SJF which is also known as shortest remaining time first or SRTF (where we can predict the next burst time using exponential averaging) , SRTF would *NOT be optimal* than RR.

- There is **no starvatio**n in case of RR, since every process shares a time slice.
- But In case of SRTF, **there can be a starvation** , in **worse case** you may have the highest priority process, with a huge burst time have to wait.That means long process may have to wait indefinite time in case of SRTF.

That's why RR can be chosen over SRTF in case of time shared OS .

5 votes -- Bikram (44.7k points)

B. Round Robin.

12 votes -- Sankaranarayanan P.N (11.2k points)

5.24.5 Process Schedule: GATE1995_2.6 top http://gateoverflow.in/2618

Selected Answer

ans is A

here, in option B and C they have given CPU idle time is 0 which is not possible as per schedule B and C.

so B and C will be eliminted.

now in A and D:

for A ,

0---1----job 3---2----job 2------7----job 1----16

so idle time is between 0 to 1 which is 1 in case of option A .

for option D,

0---job 1-----9---job 2-----14----job 3----15

we can see there is no idle time at all ..but in option given idle time is 5 , which is not matching with our chart so option D is eliminated.

therefore the correct sequence is option A .

9 votes -- jayendra (8.1k points)

5.24.6 Process Schedule: GATE1996-2.20, ISRO2008-15 top http://gateoverflow.in/2749

Selected Answer

The Completion time of A will be 9 Unit.

Hence Option D is correct.

Here is the sequence

| A | B | C | D | A | C | A | C | A | {Consider each block takes one time unit)

Completion time of A will be 9.

11 votes -- Muktinath Vishwakarma (34.1k points)

here all process arrive at time 0.so there order of execution will be A B C D, in this manner completion time for A is 9

13 votes -- neha pawar (4.4k points)

5.24.7 Process Schedule: GATE1998-2.17, UGCNET-Dec2012-III-43 top http://gateoverflow.in/1690

Selected Answer

Answer: A

Each process runs for q period and if there are n process: p_1, p_2, p_3, ..., p_n.
Then p_1's turn comes again when it has completed time quanta for remaining process p_2 to p_n, i.e, it would take at most (n-1)q time.
So, each process in round robin gets its turn after (n-1)q time when we don't consider overheads but if we consider overheads then it would be ns + (n-1)q

So we have ns + (n-1)q <= t

26 votes -- Rajarshi Sarkar (35k points)

5.24.8 Process Schedule: GATE1998_24 top http://gateoverflow.in/1739

Selected Answer

Part a

Here all we need to do for minimizing response time is to run jobs in increasing order of burst time.

6, 3, 5 and x.

If X < 3 < 5 < 6 then order should be x,3,5,6

If 3 < 5 < 6 < x then order is 3,5,6,x.

If 3 < x < 5 < 6 then order is 3,x,5,6.

Part b :-
Idea is that if you have S1 -> S2 then you create new semaphore a , assume that initial value of all semaphores is 0. Then S2 thread will invoke P(a) & will get blocked. When S1 get executed , after that it'll do V(a) which will enable S2 to run. Do like this for all edges in graph.
Let me write program for it

Begin

Semaphores a,b,c,d,e,f,g

ParBegin S1 V(a) V(b) V(c) V(d) Parend

ParBegin P(a) S2 V(e) Parend

ParBegin P(b) S3 V(f) Parend

ParBegin P(c) P(e) S4 V(g) Parend

ParBegin P(d) P(f) P(g) S5 Parend

End

IF you reverse engineer this program you can get how this diagram came.

Parbegin Parend – Parallel execution

P Down V Up

11 votes -- Akash (43.8k points)

5.24.9 Process Schedule: GATE1998_7b top http://gateoverflow.in/12963

Selected Answer

partitons are 4k , 8k, 20k, 2k, now due to best fit algo ,,

1.size of 2k job will fit in 2k partition and execute for 4 unit

2.size of 14k job will be fit in 20k partition and execute for 10 unit

3. size of3k job will br fit in 4k partition and execute for 2 unit ...

4.size of 6k job will be fit in 8k partition now execute for 1 unit..all partition are full....

and next job size of 10 k (5)wait for the partition of 20k .. and after completion of no 2 job .job no 5 will be executed for 1 unit (10 to 11)..now 20 k is also waiting for partition of 20k.. becoz it is best fit for it... so after completion of job 5 .. it will be fit . so it will execute for 8 unit which is 11 to 19 . so at 19 unit 20k job will be completed .

answer should be 19 units

21 votes -- sonam vyas (13.2k points)

5.24.10 Process Schedule: GATE2002_1.22 top

http://gateoverflow.in/827

Selected Answer

A) Here we preempt when Time quantum is expired.

C) Here we preempt when process of higher priority arrives.

D) Here we preempt when process of higher priority arrives or when time slice of higher level finishes & we need to move process to lower priority.

B) We never preempt, so answer is B) FIFO

14 votes -- Akash (43.8k points)

5.24.11 Process Schedule: GATE2003-77 top

http://gateoverflow.in/963

Selected Answer

CPU utilization = CPU burst time/Total time.

FCFS:
from 0-10: process 1
from 10-20: process 2
from 100-110: process 1
from 110-120: process 2
....
So, in every 100 ms, CPU is utilized for 20 ms, CPU utilization = 20%

SRTF:
same as FCFS as CPU burst time is same for all processes

Static priority scheduling:
Suppose process 1 is having higher priority. Now, the scheduling will be same as FCFS. If process 2 is having higher priority, then the scheduling will be as FCFS with process 1 and process 2 interchanged. So, CPU utilization remains at 20%

Round Robin:
Time quantum given as 5 ms.
from 0-5: process 1
from 5-10: process 2
from 10-15: process 1
from 15-20: process 2
from 105-110: process 1
from 110-115: process 2
...

So, in 105 ms, 20 ms of CPU burst is there. So, utilization = 20/105 = 19.05%

19.05 is less than 20, so answer is D.

(Round robin with time quantum 10ms would have made the CPU utilization same for all the schedules)

40 votes -- Arjun Suresh (294k points)

5.24.12 Process Schedule: GATE2004-46 top

http://gateoverflow.in/1043

Selected Answer

0---p1---1---p2---4---p4---5---p3---8---p1---12

Process	waiting time	turnaround time
P1	8	12
P2	0	3
P3	3	6
P4	0	1

Avg turnaround time=12+3+6+1/4=22/4=5.5

11 votes -- Pooja Palod (32.4k points)

5.24.13 Process Schedule: GATE2005-IT-60 top

http://gateoverflow.in/3821

Selected Answer

Answer will be D.

TAT = Completion Time - Arrival Time.

The Gannt Chart for Non Preemptive scheduling will be (0)P3,(15)P1,(35)P2(45).

from above this can be inferred easily that completion time for P2 is 45, for P1 is 35 and P3 is 15. .

Gantt Chart for Preemptive- (0)P3,(1)P3,(2)P3,(3)P2,(4)P2,(5)P1,(25)P2,(33)P3(45).

Similarly take completion time from above for individual processes and subtract it from the Arrival time to get TAT.

12 votes -- Gate Keeda (19.1k points)

5.24.14 Process Schedule: GATE2006-06, ISRO2009-14 top

http://gateoverflow.in/885

Selected Answer

process execute in this way ...

0 ---- p1---- 10 (switching)--------p2-----30(switching)-----p3-----60

so here only 2 switching possible (when we did not consider the starting and ending switching)

now here might be confusion that at t= 2 p1 is preempted and check that available process have shortest job time or not ...but he did not get anyone so it should not be consider as context switching ..(same happened at t=6)

ref :http://stackoverflow.com/questions/8997616/does-a-context-switch-occur-in-a-system-whose-ready-queue-has-only-one-process-a(thanks to anurag_s)

answer is B)

20 votes -- sonam vyas (13.2k points)

5.24.15 Process Schedule: GATE2006-64 top

http://gateoverflow.in/1842

Selected Answer

A.

Gantt Chart is as follows.

Gantt Chart

P2	P2	P2	P2	P1	P2	P1	P2	P0	P1	P2	P0	P1	P2

Scheduling Table

P.ID	A.T	B.T	C.T	T.A.T.	W.T.
P0	0	2	12	12	10
P1	0	4	13	13	9
P2	0	8	14	14	6
TOTAL				39	25

A.T.= Arrival Time

B.T.= Burst Time

C.T= Completion Time.

T.A.T.= Turn Around Time

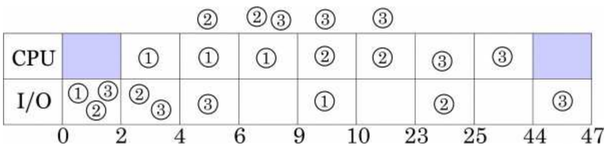
W.T= Waiting Time.

Average TAT = 39/3 = 13 units.

16 votes -- Gate Keeda (19.1k points)

5.24.16 Process Schedule: GATE2006-65 top http://gateoverflow.in/1843

Selected Answer



$$\text{CPU Idle time} = \frac{2+3}{47} \times 100 = 10.6383\%$$

answer = **option B**

23 votes -- Amar Vashishth (28.7k points)

5.24.17 Process Schedule: GATE2006-IT-54 top http://gateoverflow.in/3597

Selected Answer

0---p1----1--- no process---2---p2---3----p3----5----p2---6----p2----8----p3---9----p1----10----p2----11---no process----14--p2---15

From time 1 to 6 p1 is doing i/o

From time 5 to 8 p3 is doing i/o

P2 is doing i/o from11 to 14

So finishing time of p1 p2 p3 are 10 15 9

Ans is b

13 votes -- Pooja Palod (32.4k points)

5.24.18 Process Schedule: GATE2007-16 top http://gateoverflow.in/1214

Selected Answer

A is the answer.

http://en.wikipedia.org/wiki/Rate-monotonic_scheduling

http://en.wikipedia.org/wiki/Gang_scheduling

http://en.wikipedia.org/wiki/Fair-share_scheduling

19 votes -- Arjun Suresh (294k points)

5.24.19 Process Schedule: GATE2007-55 top http://gateoverflow.in/1253

Selected Answer

The answer is B.

The Gantt chart of execution of processes

P1	P2	P3	P2	P4

0 20 30 40 55 70

Waiting time for process P2 = Completion time – Arrival time – burst time = 55 – 15 – 25 = 15

11 votes -- Gate Keeda (19.1k points)

5.24.20 Process Schedule: GATE2007-IT-26 top http://gateoverflow.in/3459

Selected Answer

take an example for

Process	weight	execution time
p1	1	3
p2	2	5
p3	3	2
p4	4	4

for option 1 non decreasing t_i

= (3x2+1x5+4x9+2x14)/10 = (6+5+36+28)/10= 7.5

option 2 non increasing w_i

= (4x4+3x6+2x11+1x14)/10 = (16+18+22+14)/10 =7

option 3 non increasing $w_i t_i$

= (16+2x9+3x11+1x14)10 = (16+18+33+14)/10 = 8.1

option 4 non increasing w_i/t_i

= (3x2+4x6+2x11+1x14) /10 = (6+10+22+14)/10 = 5.2

minimum weighted mean obtained from non increasing w_i/t_i **(option D)**

The solution above is a classical example of greedy algorithm - that is at every point we choose the best available option and this leads to a global optimal solution. In this problem, we require to minimize the weighted mean completion time and the denominator in it is independent of the order of execution of the jobs. So, we just need to focus on the numerator and try to reduce it. Numerator here is a factor of the job weight and its completion time and since both are multiplied, our greedy solution must be

- to execute the shorter jobs first (so that remaining jobs have smaller completion time) and
- to execute highest weighted jobs first (so that it is multiplied by smaller completion time)

So, combining both we can use w_i/t_i to determine the execution order of processes - which must then be executed in non-increasing order.

31 votes -- khush tak (6.8k points)

5.24.21 Process Schedule: GATE2008-IT-55 top http://gateoverflow.in/3365

Selected Answer

ans is c

15 votes -- Sanjay Sharma (45.1k points)

5.24.22 Process Schedule: GATE2009-32 top http://gateoverflow.in/1318

Selected Answer

1. If a process makes a transition D, it would result in another process making transition A immediately. - This is false. It is not said anywhere that one process terminates, another process immediately come into Ready state. It depends on availability of process to run & Long term Scheduler.
2. A process P2 in blocked state can make transition E while another process P2 is in running state. - This is correct. There is no dependency between running process & Process getting out of blocked state.
3. The OS uses preemptive scheduling. :- This is true because we got transition C from Running to Ready.
4. The OS uses non-preemptive scheduling.Well as previous statement is true, this becomes false.

So answer is C) II and III .

20 votes -- Akash (43.8k points)

5.24.23 Process Schedule: GATE2010-25 top http://gateoverflow.in/2204

Selected Answer

ans is D

i)In SRTF ,job with the shortest CPU burst will be scheduled first bcz of this process with large CPU burst may suffer from starvation

ii)In preemptive scheduling , suppose process P1 is executing in CPU and after some time process P2 with high priority then P1 will arrive in ready queue then p1 is prrempted and p2 will brought into CPU for execution.in this way if process which is arriving in ready queue is of higher prioirity then p1 ,then p1 is always preempted and it may possible that it suffer from starvation.

iii)round robin will give better response time then FCFS ,in FCFS when process is executing ,it executed upto its complete burst time,but in round robin it will execute upto time quantum.

20 votes -- neha pawar (4.4k points)

5.24.24 Process Schedule: GATE2011_35 top http://gateoverflow.in/2137

Selected Answer

Answer is **A. 5ms**

Gantt Chart

P_0	P_1	P_1	P_0	P_2

0 1 2 5 13 22

$$\text{Average Waiting Time} = \frac{(0+4)+(0)+(11)}{3} = 5\text{ms}.$$

9 votes -- Sona Praneeth Akula (4k points)

5.24.25 Process Schedule: GATE2012_31 top http://gateoverflow.in/1749

Selected Answer

FCFS First Come First Server

P1	P2	P3

0 5 12 16

RR2

In Round Robin We are using the concept called Ready Queue.

Note
at t=2 ,

- P1 finishes and sent to Ready Queue
- P2 arrives and schedules P2

This is the Ready Queue

--	--	--	P1

At t=3

- P3 arrives at ready queue

--	--	P3	P1

At t =4

- P1 is scheduled as it is the first process to arrive at Ready Queue

p1	p2	p1	p3	p2	p1	p3	p2

Option C is correct

12 votes -- pC (21.4k points)

5.24.26 Process Schedule: GATE2013-10 top http://gateoverflow.in/1419

Selected Answer

Answer is option B.Why?

Given algorithm is : After every 'T' time units, processes are given priority w.r.t. waiting time.

lets analyse each option :

(a) not possible. as in FCFS there is no time quantum.

(C) not possible.. SJF is different. It is not preemptive.

(D) In SRTF although a process with shortest burst time is picked. But here **priority is assigned based on Burst Time of a process.**

The requirement of scheduling algorithm is priority should be assigned based on **WaitingTime** of a process. Hence this is not the answer.

So the remaining option (B) RR is the answer.

10 votes -- Desert_Warrior (9.6k points)

B...........because here the quanta for round robin is T units..after a process is scheduled it gets executed for T time units and waiting time becomes least and it again gets chance when every other process has completed T time units

22 votes -- debanjan sarkar (3.7k points)

5.24.27 Process Schedule: GATE2014-1-32 top http://gateoverflow.in/1803

Selected Answer

A	B	A	C	E	D

0 3 5 8 12 15 21

$$\text{Average turn around time} = \frac{(8-0)+(5-3)+(12-5)+(21-7)+(15-10)}{5}$$

$$= \frac{36}{5} \Rightarrow 7.2\text{ms}$$

So, answer is 7.2 msec..

13 votes -- Jay (1.2k points)

5.24.28 Process Schedule: GATE2014-2-32 top http://gateoverflow.in/1991

Selected Answer

Gantt chart : ABCABCBCBC
C completes it CPU burst at= 500 milli second.
IO time = 500 milli second
C completes 1st IO burst at t = 500 + 500 = 1000ms

16 votes -- Digvijay (47k points)

5.24.29 Process Schedule: GATE2014-3-32 top http://gateoverflow.in/2066

Selected Answer

	Arrival Time	Burst Time	Completion Time	Turn Around Time	Waiting Time = CT - BT - AT
p1	0	12	27	27	15
p2	2	4	6	4	0
p3	3	6	12	9	3
p4	8	5	17	9	4

(15 + 0 + 3 + 4)/4 = 5.5 msecs

p1 p2 p2 p3 p3 p4 p1

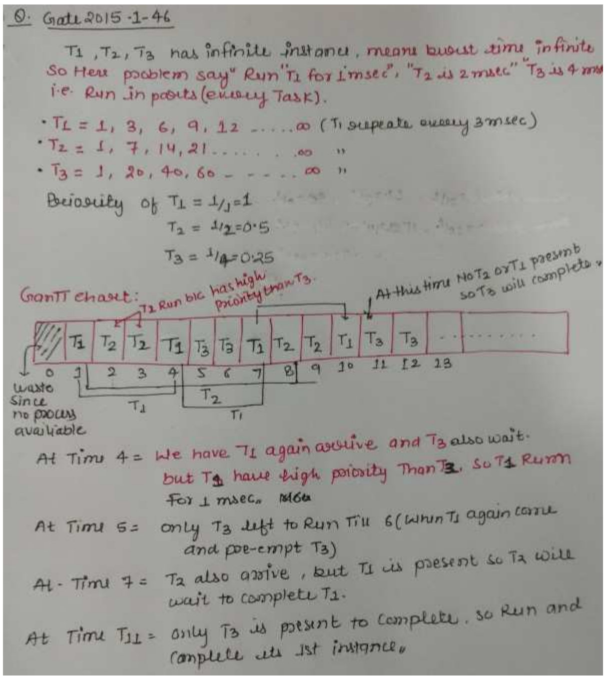
0 2 3 6 8 12 17 27

9 votes -- Sourav Roy (3.6k points)

5.24.30 Process Schedule: GATE2015-1_46 top http://gateoverflow.in/8330

Selected Answer

Check This : Answer is **12**



21 votes -- Prashant Singh (49.2k points)

1: T1
2: T2
3: T2
4: T1
5: T3
6: T3
7: T1
8: T2
9: T2
10: T1
11: T3
12: T3 (First instance of T3 completes 4 ms and finished execution).

So, answer is 12.

27 votes -- Arjun Suresh (294k points)

5.24.31 Process Schedule: GATE2015-3-34 top http://gateoverflow.in/8492

Selected Answer

Turn Around Time = Completion Time - Arrival Time

FCFS

Average turn around time = [3 for A + (2 + 6) for B + (5 + 4) for C + (7 + 2) for D] / 4 = 7.25

Non-preemptive Shortest Job First

Average turn around time = [3 for A + (2 + 6) for B + (3 + 2) for D+ (7 + 4) for C] = 6.75

Shortest Remaining Time

Average turn around time = [3 for A + (2 + 1) for B + (0 + 4) for C + (2 + 2) for D + (6 + 5) for remaining B]/4 = 6.25

Round Robin

Average turn around time =

[2 for A (B comes after 1)
+ (1 + 2) for B {C comes}
+ (2+1) for A (A finishes after 3 cycles with turnaround time of 2 + 3 = 5)
+ (1+2) for C {D comes}
+ (3+2) for B
+ (3+2) for D (D finishes with turnaround time of 3+2 = 5)
+ (4+2) for C (C finishes with turnaround time of 3 + 6 = 9)
+ (4+2) for B (B finishes after turnaround time of 3 + 5 + 6 = 14]
/4
= 8.25

A	B	A	C	B	D	C	B
0-2	2-4	4-5	5-7	7-9	9-11	11-13	13-15

Shortest Remaining Time First scheduling which is the preemptive version of the SJF scheduling is provably optimal for the shortest waiting time and hence always gives the best (minimal) turn around time (waiting time + burst time). So, we can directly give the answer here.

14 votes -- Arjun Suresh (294k points)

5.24.32 Process Schedule: GATE2015-3_1 top http://gateoverflow.in/8390

Selected Answer

D. independent of n.

The number of processes that can be in READY state depends on the Ready Queue size and is independent of the number of CPU's.

24 votes -- Arjun Suresh (294k points)

5.24.33 Process Schedule: GATE2016-2-47 top http://gateoverflow.in/39625

Selected Answer

SRTF Preemptive hence,

P1 P2 P3 P2 P4 P1
0 3 7 8 10 13 20

Process TAT=Completion time- Arrival time
P1 20
P2 7
P3 1
P4 5

AvgTAT= 33/4 = 8.25

22 votes -- Shashank Chavan (3.4k points)

5.24.34 Process Schedule: GATE2017-1-24 top http://gateoverflow.in/118304

Selected Answer

Process	Arrival Time	Burst Time	Completion Time	Turn Around Time	Waiting Time
P1	0	7	12	12	5
P2	3	3	6	3	0
P3	5	5	17	12	7
P4	6	2	8	2	0
					Total: 12

TAT= CT-AT
WT= TAT-BT
Total waiting time= 12
Average Waiting time=
12/4 = 3 (ans)

Hence ans is 3ms.

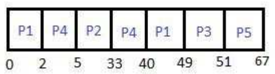
8 votes -- Ahwan Mishra (5.3k points)

5.24.35 Process Schedule: GATE2017-2-51 top

http://gateoverflow.in/118558

Selected Answer

Gantt Chart for above problem looks like :



Waiting Time = Completion time - Arrival time - Burst Time

$\sum AT = 0 + 5 + 12 + 2 + 9 = 28$

$\sum BT = 11 + 28 + 2 + 10 + 16 = 67$

$\sum CT = 67 + 51 + 49 + 40 + 33 = 240$

Waiting time $= 240 - 28 - 67 = 145$

Average Waiting Time $= \frac{145}{5} = 29$ msec.

23 votes -- Manish Joshi (25.2k points)

5.24.36 Process Schedule: ISI2015-CS-6b top

http://gateoverflow.in/47333

Selected Answer

1. FCFS

Waiting time is the time from being ready to being processed.
P_1 does not wait. P_2 wait for $D + \Delta$ and for $2 \leq i \leq n, W(P_i)) = (i-1)(D+\Delta)$. So, average waiting time

$$= \frac{\sum_{i=1}^{n}(i-1)(D+\Delta)}{n} = \frac{n-1}{2}(D+\Delta).$$

Turn around time is the time from being ready to being completed.

$T(P_1) = D$ and $T(P_i) = i.D + (i-1)\Delta$. So, average turn around time

$$= \frac{(n+1)}{2}D + \frac{n-1}{2}\Delta.$$

2. Round Robin.

Here since all processes came at once, once P_1 is preempted, it can come back only after all other processes. Since all processes are identical, we can get the number of times each will be run by $\lceil \frac{D}{d} \rceil = x$. Now for process i, waiting time would be

$W(P_i) = (x-1)(n-1)(\delta + d) + (i-1)(D\%d + \Delta)$. So, average waiting time would be

$$= (x-1)(n-1)(\delta + d) + \frac{(n-1)}{2}(D\%d + \Delta).$$

Turn around time for process P_i will be

$T(P_i) = (x-1)(n)(\delta + d) + i.(D\%d) + (i-1)\Delta$. So, average turn around time would be

$$= (x-1)(n)(\delta + d) + \frac{(n+1)}{2}(D\%d) + \frac{n-1}{2}\Delta$$

.

4 votes -- Arjun Suresh (294k points)

5.25 Process Synchronization(46) top

5.25.1 Process Synchronization: GATE1990-2-iii top http://gateoverflow.in/83859

Match the pairs in the following questions:

(a) Critical region	(p) Hoare's monitor
(b) Wait/Signal	(q) Mutual exclusion
(c) Working Set	(r) Principle of locality
(d) Deadlock	(s) Circular Wait

match-the-following gate1990 operating-system process-synchronization

Answer

5.25.2 Process Synchronization: GATE1993_22 top http://gateoverflow.in/2319

Write a concurrent program using parbegin-parend and semaphores to represent the precedence constraints of the statements S_1 to S_6, as shown in figure below.

gate1993 operating-system process-synchronization normal

Answer

5.25.3 Process Synchronization: GATE1994_27 top http://gateoverflow.in/2523

a. Draw a precedence graph for the following sequential code. The statements are numbered from S_1 to S_6

S_1	read n
S_2	i := 1
S_3	if i > n next
S_4	a(i) := i+1
S_5	i := i+1
S_6	next : write a(i)

b. Can this graph be converted to a concurrent program using parbegin-parend construct only?

gate1994 operating-system process-synchronization normal

Answer

5.25.4 Process Synchronization: GATE1995_19 top http://gateoverflow.in/2656

Consider the following program segment for concurrent processing using semaphore operators P and V for synchronization. Draw the precedence graph for the statements S1 to S9.

```
var
a,b,c,d,e,f,g,h,i,j,k : semaphore;
begin
cobegin
    begin S1; V(a); V(b) end;
    begin P(a); S2; V(c); V(d) end;
    begin P(c); S4; V(e) end;
    begin P(d); S5; V(f) end;
    begin P(e); P(f); S7; V(k) end
    begin P(b); S3; V(g); V(h) end;
    begin P(g); S6; V(i) end;
    begin P(h); P(i); S8; V(j) end;
    begin P(j); P(k); S9 end;
coend
end;
```

gate1995 operating-system process-synchronization normal

Answer

5.25.5 Process Synchronization: GATE1996-1.19, ISRO2008-61 top http://gateoverflow.in/2723

A critical section is a program segment

A. which should run in a certain amount of time
B. which avoids deadlocks
C. where shared resources are accessed
D. which must be enclosed by a pair of semaphore operations, P and V

gate1996 operating-system process-synchronization easy isro2008

Answer

5.25.6 Process Synchronization: GATE1996_2.19 top http://gateoverflow.in/2748

A solution to the Dining Philosophers Problem which avoids deadlock is to

A. ensure that all philosophers pick up the left fork before the right fork

B. ensure that all philosophers pick up the right fork before the left fork

C. ensure that one particular philosopher picks up the left fork before the right fork, and that all other philosophers pick up the right fork before the left fork

D. None of the above

gate1996 operating-system process-synchronization normal

Answer

5.25.7 Process Synchronization: GATE1996_21 top http://gateoverflow.in/2773

The concurrent programming constructs fork and join are as below:

fork <label> which creates a new process executing from the specified label

join <variable> which decrements the specified synchronization variable (by 1) and terminates the process if the new value is not 0.

Show the precedence graph for S1, S2, S3, S4, and S5 of the concurrent program below.

21. The concurrent programming constructs fork and join are as below:
fork <label> which creates a new process executing from the specified label
join <variable> which decrements the specified synchronization variable (by 1) and terminates the process if the new value is not 0.
Show the precedence graph for S1, S2, S3, S4 and S5 of the concurrent program below.

```
N = 2
M = 2
fork L3
fork L4
S1
L1 : join N
S3
L2: join M
S5
L3:S2
goto L1
L4:S4
goto L2
next:
```

gate1996 operating-system process-synchronization normal

Answer

5.25.8 Process Synchronization: GATE1997_6.8 top http://gateoverflow.in/2264

Each Process P_i, i = 1....9 is coded as follows

```
repeat
    P(mutex)
    {Critical section}
    V(mutex)
forever
```

The code for P_{10} is identical except it uses V(mutex) in place of P(mutex). What is the largest number of processes that can be inside the critical section at any moment?

A. 1
B. 2
C. 3
D. None

gate1997 operating-system process-synchronization normal

Answer

5.25.9 Process Synchronization: GATE1998-1.30 top http://gateoverflow.in/1667

When the result of a computation depends on the speed of the processes involved, there is said to be

A. cycle stealing
B. race condition
C. a time lock
D. a deadlock

gate1998 operating-system easy process-synchronization

Answer

5.25.10 Process Synchronization: GATE1999_20 top http://gateoverflow.in/1519

(a) A certain processor provides a 'test and set' instruction that is used as follows:

```
TSET register, flag
```

This instruction atomically copies flag to register and sets flag to 1. Give pseudo-code for implementing the entry and exit code to a critical region using this instruction.

(b) Consider the following solution to the producer-consumer problem using a buffer of size 1. Assume that the initial value of count is 0. Also assume that the testing of count and assignment to count are atomic operations.

```
Producer:
Repeat
    Produce an item;
    if count = 1 then sleep;
    place item in buffer.
    count = 1;
```

```
    Wakeup(Consumer);
Forever

Consumer:
Repeat
    if count = 0 then sleep;
    Remove item from buffer;
    count = 0;
    Wakeup(Producer);
    Consume item;
Forever;
```

Show that in this solution it is possible that both the processes are sleeping at the same time.

gate1999 operating-system process-synchronization normal

Answer

5.25.11 Process Synchronization: GATE2000-1.21 top

http://gateoverflow.in/645

Let m[0]....m[4] be mutexes (binary semaphores) and P[0].......P[4] be processes.
Suppose each process P[i] executes the following:

```
wait (m[i]; wait (m(i+1) mode 4]);
...........
release (m[i]); release (m(i+1) mod 4]);
```

This could cause

A. Thrashing
B. Deadlock
C. Starvation, but not deadlock
D. None of the above

gate2000 operating-system process-synchronization normal

Answer

5.25.12 Process Synchronization: GATE2000-20 top

http://gateoverflow.in/691

(a) Fill in the boxes below to get a solution for the reader-writer problem, using a single binary semaphore, mutex (initialized to 1) and busy waiting. Write the box numbers (1, 2 and 3), and their contents in your answer book.

```
int R = 0, W = 0;

Reader () {
    wait (mutex);
    if (W == 0) {
        R = R + 1;
        ▭ ______________(1)
    }
L1: else {
      ▭ ______________(2)
        goto L1;
    }
    ..../* do the read*/
    wait (mutex);
    R = R - 1;
    signal (mutex);
}
```

```
Writer () {
    wait (mutex);
    if (▭) { _________ (3)
        signal (mutex);
        goto L2;
    }
L2: W=1;
    signal (mutex);
    ...../*do the write*/
    wait( mutex);
    W=0;
    signal (mutex);
}
```

(b) Can the above solution lead to starvation of writers?

gate2000 operating-system process-synchronization normal descriptive

Answer

5.25.13 Process Synchronization: GATE2001-2.22 top http://gateoverflow.in/740

Consider Peterson's algorithm for mutual exclusion between two concurrent processes i and j. The program executed by process is shown below.

```
repeat
    flag[i] = true;
    turn = j;
    while (P) do no-op;
    Enter critical section, perform actions, then
    exit critical section
    Flag[i] = false;
    Perform other non-critical section actions.
Until false;
```

For the program to guarantee mutual exclusion, the predicate P in the while loop should be

A. flag[j] = true and turn = i
B. flag[j] = true and turn = j
C. flag[i] = true and turn = j
D. flag[i] = true and turn = i

gate2001 operating-system process-synchronization normal

Answer

5.25.14 Process Synchronization: GATE2002-18 top http://gateoverflow.in/871

a. Draw the process state transition diagram of an OS in which (i) each process is in one of the five states: created, ready, running, blocked (i.e., sleep or wait), or terminated, and (ii) only non-preemptive scheduling is used by the OS. Label the transitions appropriately.
b. The functionality of atomic TEST-AND-SET assembly language instruction is given by the following C function

```
int TEST-AND-SET (int *x)
{
    int y;
    A1: y=*x;
    A2: *x=1;
    A3: return y;
}
```

i. Complete the following C functions for implementing code for entering and leaving critical sections on the above TEST-AND-SET instruction.

ii.
```
int mutex=0;
void enter-cs()
{
    while(......................);

}
void leave-cs()
{ .........................;

}
```

iii. Is the above solution to the critical section problem deadlock free and starvation-free?
iv. For the above solution, show by an example that mutual exclusion is not ensured if TEST-AND-SET instruction is not atomic?

gate2002 operating-system process-synchronization normal descriptive

Answer

5.25.15 Process Synchronization: GATE2002-20 top http://gateoverflow.in/873

The following solution to the single producer single consumer problem uses semaphores for synchronization.

```
#define BUFFSIZE 100
buffer buf[BUFFSIZE];
int first = last = 0;
semaphore b_full = 0;
semaphore b_empty = BUFFSIZE

void producer()
{
while(1) {
    produce an item;
    p1:.................;
    put the item into buff (first);
    first = (first+1)%BUFFSIZE;
    p2: ...............;
    }
}

void consumer()
{
while(1) {
    c1:............
    take the item from buf[last];
    last = (last+1)%BUFFSIZE;
    c2:............;
    consume the item;
    }
}
```

a. Complete the dotted part of the above solution.

b. Using another semaphore variable, insert one line statement each immediately after p1, immediately before p2, immediately after c1 and immediately before c2 so that the program works correctly for multiple producers and consumers.

gate2002 operating-system process-synchronization normal descriptive

Answer

5.25.16 Process Synchronization: GATE2003-80 top http://gateoverflow.in/964

Suppose we want to synchronize two concurrent processes P and Q using binary semaphores S and T. The code for the processes P and Q is shown below.

Process P:	Process Q:
while(1) {	while(1) {
W:	Y:
print '0';	print '1';
print '0';	print '1';
X:	Z:
}	}

Synchronization statements can be inserted only at points W, X, Y, and Z

Which of the following will always lead to an output staring with '001100110011'?

A. P(S) at W, V(S) at X, P(T) at Y, V(T) at Z, S and T initially 1

B. P(S) at W, V(T) at X, P(T) at Y, V(S) at Z, S initially 1, and T initially 0

C. P(S) at W, V(T) at X, P(T) at Y, V(S) at Z, S and T initially 1

D. P(S) at W, V(S) at X, P(T) at Y, V(T) at Z, S initially 1 , and T initially 0

gate2003 operating-system process-synchronization normal

Answer

5.25.17 Process Synchronization: GATE2003-81 top http://gateoverflow.in/43574

Suppose we want to synchronize two concurrent processes P and Q using binary semaphores S and T. The code for the processes P and Q is shown below.

Process P:	Process Q:

while(1) {	while(1) {
W:	Y:
print '0';	print '1';
print '0';	print '1';
X:	Z:
}	}

Synchronization statements can be inserted only at points W, X, Y, and Z

Which of the following will ensure that the output string never contains a substring of the form 01^n0 and 10^n1 where n is odd?

A. P(S) at W, V(S) at X, P(T) at Y, V(T) at Z, S and T initially 1
B. P(S) at W, V(T) at X, P(T) at Y, V(S) at Z, S and T initially 1
C. P(S) at W, V(S) at X, P(S) at Y, V(S) at Z, S initially 1
D. V(S) at W, V(T) at X, P(S) at Y, P(T) at Z, S and T initially 1

gate2003 operating-system process-synchronization normal

Answer

5.25.18 Process Synchronization: GATE2004-48 top http://gateoverflow.in/1044

Consider two processes P_1 and P_2 accessing the shared variables X and Y protected by two binary semaphores S_X and S_Y respectively, both initialized to 1. P and V denote the usual semaphore operators, where P decrements the semaphore value, and V increments the semaphore value. The pseudo-code of P_1 and P_2 is as follows:

P_1**:**	P_2**:**
While true do {	While true do {
L_1:........	L_3:........
L_2:........	L_4:........
X = X + 1;	Y = Y + 1;
Y = Y -1;	X = Y -1;
$V(S_X)$;	$V(S_Y)$;
$V(S_Y)$; }	$V(S_X)$;

In order to avoid deadlock, the correct operators at L_1, L_2, L_3 and L_4 are respectively.

A. $P(S_Y), P(S_X); P(S_X), P(S_Y)$

B. $P(S_X), P(S_Y); P(S_Y), P(S_X)$

C. $P(S_X), P(S_X); P(S_Y), P(S_Y)$

D. $P(S_X), P(S_Y); P(S_X), P(S_Y)$

gate2004 operating-system process-synchronization normal

Answer

5.25.19 Process Synchronization: GATE2004-IT-65 top http://gateoverflow.in/3708

The semaphore variables full, empty and mutex are initialized to 0, n and 1, respectively. Process P_1 repeatedly adds one item at a time to a buffer of size n, and process P_2 repeatedly removes one item at a time from the same buffer using the programs given below. In the programs, K, L, M and N are unspecified statements.

P_1
```
while (1) {
    K;
    P(mutex);
    Add an item to the buffer;
    V(mutex);
    L;
}
```

P_2
```
while (1) {
    M;
    P(mutex);
    Remove an item from the buffer;
    V(mutex);
    N;
}
```

The statements K, L, M and N are respectively

A. P(full), V(empty), P(full), V(empty)
B. P(full), V(empty), P(empty), V(full)
C. P(empty), V(full), P(empty), V(full)
D. P(empty), V(full), P(full), V(empty)

gate2004-it operating-system process-synchronization normal

Answer

5.25.20 Process Synchronization: GATE2005-IT-41 top

http://gateoverflow.in/3788

Given below is a program which when executed spawns two concurrent processes :
semaphore X : = 0 ;
/* Process now forks into concurrent processes P1 & P2 */

P1	**P2**
repeat forever	repeat forever
V (X) ;	P(X) ;
Compute ;	Compute ;
P(X) ;	V(X) ;

Consider the following statements about processes P1 and P2:

I. It is possible for process P1 to starve.
II. It is possible for process P2 to starve.

Which of the following holds?

A. Both I and II are true.
B. I is true but II is false.
C. II is true but I is false
D. Both I and II are false

gate2005-it operating-system process-synchronization normal

Answer

5.25.21 Process Synchronization: GATE2005-IT-42 top

http://gateoverflow.in/3789

Two concurrent processes P1 and P2 use four shared resources R1, R2, R3 and R4, as shown below.

P1	**P2**
Compute:	Compute;
Use R1;	Use R1;
Use R2;	Use R2;

P1 Use R3; **P2** Use R3;.
Use R4; Use R4;

Both processes are started at the same time, and each resource can be accessed by only one process at a time The following scheduling constraints exist between the access of resources by the processes:

- P2 must complete use of R1 before P1 gets access to R1.
- P1 must complete use of R2 before P2 gets access to R2.
- P2 must complete use of R3 before P1 gets access to R3.
- P1 must complete use of R4 before P2 gets access to R4.

There are no other scheduling constraints between the processes. If only binary semaphores are used to enforce the above scheduling constraints, what is the minimum number of binary semaphores needed?

A. 1
B. 2
C. 3
D. 4

gate2005-it operating-system process-synchronization normal

Answer

5.25.22 Process Synchronization: GATE2006-61 top

http://gateoverflow.in/1839

The atomic *fetch-and-set* x, y instruction unconditionally sets the memory location x to 1 and fetches the old value of x n y without allowing any intervening access to the memory location x. Consider the following implementation of P and V functions on a binary semaphore S.

```
void P (binary_semaphore *s) {
    unsigned y;
    unsigned *x = &(s->value);
    do {
        fetch-and-set x, y;
    } while (y);
}

void V (binary_semaphore *s) {
    S->value = 0;
}
```

Which one of the following is true?

A. The implementation may not work if context switching is disabled in P
B. Instead of using *fetch-and –set*, a pair of normal load/store can be used
C. The implementation of V is wrong
D. The code does not implement a binary semaphore

gate2006 operating-system process-synchronization normal

Answer

5.25.23 Process Synchronization: GATE2006-78 top

http://gateoverflow.in/1853

Barrier is a synchronization construct where a set of processes synchronizes globally i.e., each process in the set arrives at the barrier and waits for all others to arrive and then all processes leave the barrier. Let the number of processes in the set be three and S be a binary semaphore with the usual P and V functions. Consider the following C implementation of a barrier with line numbers shown on left.

```
void barrier (void) {

        P(S);
        process_arrived++;
        V(S);
        while (process_arrived !=3);
        P(S);
        process_left++;
        if (process_left==3) {
            process_arrived = 0;
            process_left = 0;
        }
        V(S);

}
```

The variables *process_arrived* and *process_left* are shared among all processes and are initialized to zero. In a concurrent program all the three processes call the barrier function when they need to synchronize globally.

The above implementation of barrier is incorrect. Which one of the following is true?

A. The barrier implementation is wrong due to the use of binary semaphore S
B. The barrier implementation may lead to a deadlock if two barrier in invocations are used in immediate succession.
C. Lines 6 to 10 need not be inside a critical section
D. The barrier implementation is correct if there are only two processes instead of three.

gate2006 operating-system process-synchronization normal

Answer

5.25.24 Process Synchronization: GATE2006-79 top http://gateoverflow.in/43564

Barrier is a synchronization construct where a set of processes synchronizes globally i.e., each process in the set arrives at the barrier and waits for all others to arrive and then all processes leave the barrier. Let the number of processes in the set be three and S be a binary semaphore with the usual P and V functions. Consider the following C implementation of a barrier with line numbers shown on left.

```
void barrier (void) {
```

```
        P(S);
        process_arrived++;
        V(S);
        while (process_arrived !=3);
        P(S);
        process_left++;
        if (process_left==3) {
            process_arrived = 0;
            process_left = 0;
        }
        V(S);
```

```
}
```

The variables process_arrived and process_left are shared among all processes and are initialized to zero. In a concurrent program all the three processes call the barrier function when they need to synchronize globally.

Which one of the following rectifies the problem in the implementation?

A. Lines 6 to 10 are simply replaced by process_arrived--
B. At the beginning of the barrier the first process to enter the barrier waits until process_arrived becomes zero before proceeding to execute P(S).
C. Context switch is disabled at the beginning of the barrier and re-enabled at the end.
D. The variable process_left is made private instead of shared

gate2006 operating-system process-synchronization normal

Answer

5.25.25 Process Synchronization: GATE2006-IT-55 top http://gateoverflow.in/3598

Consider the solution to the bounded buffer producer/consumer problem by using general semaphores S, F, and E. The semaphore S is the mutual exclusion semaphore initialized to 1. The semaphore F corresponds to the number of free slots in the buffer and is initialized to N. The semaphore E corresponds to the number of elements in the buffer and is initialized to 0.

Producer Process	**Consumer Process**
Produce an item;	Wait(E);
Wait(F);	Wait(S);
Wait(S);	Remove an item from the buffer;
Append the item to the buffer;	Signal(S);
Signal(S);	Signal(F);
Signal(E);	Consume the item;

Which of the following interchange operations may result in a deadlock?

I. Interchanging Wait (F) and Wait (S) in the Producer process
II. Interchanging Signal (S) and Signal (F) in the Consumer process

A. I only
B. II only
C. Neither I nor II
D. Both I and II

gate2006-it operating-system process-synchronization normal

Answer

5.25.26 Process Synchronization: GATE2007-58 top http://gateoverflow.in/1256

Two processes, P1 and P2, need to access a critical section of code. Consider the following synchronization construct used by the processes:

`/* P1 */`
`while (true) {`
`    wants1 = true;`
`    while (wants2 == true);`
`    /* Critical Section */`
`    wants1 = false;`
`}`
`/* Remainder section */`
	`/* P2 */`
	`while (true) {`
	`    wants2 = true;`
	`    while (wants1 == true);`
	`    /* Critical Section */`
	`    wants2=false;`
	`}`
	`/* Remainder section */`

Here, wants1 and wants2 are shared variables, which are initialized to false.

Which one of the following statements is TRUE about the construct?

A. It does not ensure mutual exclusion.

B. It does not ensure bounded waiting.

C. It requires that processes enter the critical section in strict alteration.

D. It does not prevent deadlocks, but ensures mutual exclusion.

gate2007 operating-system process-synchronization normal

Answer

5.25.27 Process Synchronization: GATE2007-IT-10 top http://gateoverflow.in/3443

Processes P1 and P2 use critical_flag in the following routine to achieve mutual exclusion. Assume that critical_flag is initialized to FALSE in the main program.

```
get_exclusive_access ( )
{
    if (critical _flag == FALSE) {
        critical_flag = TRUE ;
        critical_region () ;
        critical_flag = FALSE;
    }
}
```

Consider the following statements.

i. It is possible for both P1 and P2 to access critical_region concurrently.
ii. This may lead to a deadlock.

Which of the following holds?

A. i is flase ii is true
B. Both i and ii are false
C. i is true ii is flase
D. Both i and ii are true

gate2007-it operating-system process-synchronization normal

Answer

5.25.28 Process Synchronization: GATE2007-IT-56 top

http://gateoverflow.in/3498

Synchronization in the classical readers and writers problem can be achieved through use of semaphores. In the following incomplete code for readers-writers problem, two binary semaphores mutex and wrt are used to obtain synchronization

```
wait (wrt)
writing is performed
signal (wrt)
wait (mutex)
readcount = readcount + 1
if readcount = 1 then S1
S2
reading is performed
S3
readcount = readcount - 1
if readcount = 0 then S4
signal (mutex)
```

The values of S1, S2, S3, S4, (in that order) are

A. signal (mutex), wait (wrt), signal (wrt), wait (mutex)
B. signal (wrt), signal (mutex), wait (mutex), wait (wrt)
C. wait (wrt), signal (mutex), wait (mutex), signal (wrt)
D. signal (mutex), wait (mutex), signal (mutex), wait (mutex)

gate2007-it operating-system process-synchronization normal

Answer

5.25.29 Process Synchronization: GATE2008-IT-53 top

http://gateoverflow.in/3363

The following is a code with two threads, producer and consumer, that can run in parallel. Further, S and Q are binary semaphores quipped with the standard P and V operations.

```
semaphore S = 1, Q = 0;
integer x;

producer:                     consumer:
while (true) do               while (true) do
    P(S);                         P(Q);
    x = produce ();               consume (x);
    V(Q);                         V(S);
done                          done
```

Which of the following is TRUE about the program above?

A. The process can deadlock
B. One of the threads can starve
C. Some of the items produced by the producer may be lost
D. Values generated and stored in 'x' by the producer will always be consumed before the producer can generate a new value

gate2008-it operating-system process-synchronization normal

Answer

5.25.30 Process Synchronization: GATE2009-33 top

http://gateoverflow.in/1319

The **enter_CS()** and **leave_CS()** functions to implement critical section of a process are realized using test-and-set instruction as follows:

```
void enter_CS(X)
{
    while(test-and-set(X));
}

void leave_CS(X)
{
    X = 0;
}
```

In the above solution, X is a memory location associated with the CS and is initialized to 0. Now consider the following statements:

I. The above solution to CS problem is deadlock-free

II. The solution is starvation free

III. The processes enter CS in FIFO order

IV. More than one process can enter CS at the same time

Which of the above statements are TRUE?

A. I only
B. I and II
C. II and III
D. IV only

gate2009 operating-system process-synchronization normal

Answer

5.25.31 Process Synchronization: GATE2010-23 top http://gateoverflow.in/2202

Consider the methods used by processes P1 and P2 for accessing their critical sections whenever needed, as given below. The initial values of shared boolean variables S1 and S2 are randomly assigned.

Method used by P1	Method used by P2

`while (S1==S2);`
`Critical Section`
`S1=S2;`
	`while (S1!=S2);`
	`Critical Section`
	`S2 = not(S1)`

Which one of the following statements describes the properties achieved?

A. Mutual excusion but not progress
B. Progress but not mutual exclusion
C. Neither mutual exclusion nor progress
D. Both mutual exclusion and progress

gate2010 operating-system process-synchronization normal

Answer

5.25.32 Process Synchronization: GATE2010-45 top http://gateoverflow.in/2347

The following program consists of 3 concurrent processes and 3 binary semaphores. The semaphores are initialized as S0=1, S1=0 and S2=0.

Process P0	Process P1	Process P2

`while (true) {`
`    wait (S0);`
`    print '0';`
`    release (S1);`
`    release (S2);`
`}`
	`wait  (S1);`
	`release (S0);`
		`wait  (S2);`
		`release (S0);`

How many times will process P0 print '0'?

A. At least twice
B. Exactly twice
C. Exactly thrice
D. Exactly once

gate2010 operating-system process-synchronization normal

Answer

5.25.33 Process Synchronization: GATE2012_32 top http://gateoverflow.in/1750

Fetch_And_Add(X,i) is an atomic Read-Modify-Write instruction that reads the value of memory location X, increments it by the value i, and returns the old value of X. It is used in the pseudocode shown below to implement a busy-wait lock. L is an unsigned integer shared variable initialized to 0. The value of 0 corresponds to lock being available, while any non-zero value corresponds to the lock being not available.

```
AcquireLock(L){
   while (Fetch_And_Add(L,1))
      L = 1;
}

ReleaseLock(L){
   L = 0;
}
```

This implementation

(A) fails as L can overflow
(B) fails as L can take on a non-zero value when the lock is actually available
(C) works correctly but may starve some processes
(D) works correctly without starvation

gate2012 operating-system process-synchronization normal

Answer

5.25.34 Process Synchronization: GATE2013_34 top http://gateoverflow.in/1545

A shared variable x, initialized to zero, is operated on by four concurrent processes W, X, Y, Z as follows. Each of the processes W and X reads x from memory, increments by one, stores it to memory, and then terminates. Each of the processes Y and Z reads x from memory, decrements by two, stores it to memory, and then terminates. Each process before reading x invokes the P operation (i.e., wait) on a counting semaphore S and invokes the V operation (i.e., signal) on the semaphore S after storing x to memory. Semaphore S is initialized to two. What is the maximum possible value of x after all processes complete execution?

(A) −2 (B) −1 (C) 1 (D) 2

gate2013 operating-system process-synchronization normal

Answer

5.25.35 Process Synchronization: GATE2013_39 top http://gateoverflow.in/1550

A certain computation generates two arrays a and b such that a[i] = f(i) for 0 ≤ i < n and b[i] = g(a[i]) for 0 ≤ i < n. Suppose this computation is decomposed into two concurrent processes X and Y such that X computes the array a and Y computes the array b. The processes employ two binary semaphores R and S, both initialized to zero. The array a is shared by the two processes. The structures of the processes are shown below.

Process X:

```
private i;
for (i=0; i< n; i++) {

 a[i] = f(i);

 ExitX(R, S);

}
```

Process Y:

```
private i;
for (i=0; i< n; i++) {

 EntryY(R, S);

 b[i] = g(a[i]);

 }
```

Which one of the following represents the **CORRECT** implementations of ExitX and EntryY?

(A)

```
ExitX(R, S) {
P(R);
V(S);
}
EntryY(R, S) {
 P(S);
 V(R);
}
```

```
(B) ExitX(R, S) {
V(R);
V(S);
}
EntryY(R, S) {
 P(R);
 P(S);
}
```

```
(C) ExitX(R, S) {
P(S);
V(R);
}
EntryY(R, S) {
 V(S);
 P(R);
}
```

```
(D) ExitX(R, S) {
V(R);
P(S);
}
EntryY(R, S) {
 V(S);
 P(R);
}
```

gate2013 operating-system process-synchronization normal

Answer

5.25.36 Process Synchronization: GATE2014-2-31 top http://gateoverflow.in/1990

Consider the procedure below for the *Producer-Consumer* problem which uses semaphores:

```
semaphore n = 0;
semaphore s = 1;
```

```
void producer()
{
    while(true)
    {
        produce();
        semWait(s);
        addToBuffer();
        semSignal(s);
```

```
        semSignal(n);
    }
}
```

```
void consumer()
{
    while(true)
    {
        semWait(s);
        semWait(n);
        removeFromBuffer();
        semSignal(s);
        consume();
    }
}
```

Which one of the following is **TRUE**?

A. The producer will be able to add an item to the buffer, but the consumer can never consume it.
B. The consumer will remove no more than one item from the buffer.
C. Deadlock occurs if the consumer succeeds in acquiring semaphore s when the buffer is empty.
D. The starting value for the semaphore n must be 1 and not 0 for deadlock-free operation.

gate2014-2 operating-system process-synchronization normal

Answer

5.25.37 Process Synchronization: GATE2015-3_10 top

http://gateoverflow.in/8405

Two processes X and Y need to access a critical section. Consider the following synchronization construct used by both the processes

Process X

```
/* other code for process x*/
while (true)  {
    varP = true;
    while (varQ == true)
    {
        /* Critical Section */
        varP = false;
    }
}
/* other code for process X */
```

Process Y

```
/* other code for process Y */
while (true)
{
    varQ = true;
    while (varP == true)
    {
        /* Critical Section */
        varQ = false;
    }
}
/* other code for process Y */
```

Here *varP* and *varQ* are shared variables and both are initialized to false. Which one of the following statements is true?

A. The proposed solution prevents deadlock but fails to guarantee mutual exclusion
B. The proposed solution guarantees mutual exclusion but fails to prevent deadlock
C. The proposed solution guarantees mutual exclusion and prevents deadlock
D. The proposed solution fails to prevent deadlock and fails to guarantee mutual exclusion

gate2015-3 operating-system process-synchronization normal

Answer

5.25.38 Process Synchronization: GATE2016-2-48 top

http://gateoverflow.in/39600

Consider the following two-process synchronization solution.

```
PROCESS 0                               Process 1

Entry: loop while (turn == 1);           Entry: loop while (turn == 0);
  (critical section)                         (critical section)
Exit: turn = 1;                           Exit turn = 0;
```

The shared variable turn is initialized to zero . Which one of the following is TRUE?

A). This is a correct two- process synchronization solution.

B). This solution violates mutual exclusion requirement.

C). This solution violates progress requirement.

D). This solution violates bounded wait requirement.

gate2016-2 operating-system process-synchronization normal

Answer

5.25.39 Process Synchronization: GATE2017-1-27 top

http://gateoverflow.in/118307

A multithreaded program P executes with x number of threads and uses y number of locks for ensuring mutual exclusion while operating on shared memory locations. All locks in the program are *non-reentrant*, i.e., if a thread holds a lock l, then it cannot re-acquire lock l without releasing it. If a thread is unable to acquire a lock, it blocks until the lock becomes available. The *minimum* value of x and the *minimum* value of y together for which execution of P can result in a deadlock are:

(A) x = 1, y = 2

(B) x = 2, y = 1

(C) x = 2, y = 2

(D) x = 1, y = 1

gate2017-1 operating-system process-synchronization normal

Answer

5.25.40 Process Synchronization: ISI2011-CS-5c top

http://gateoverflow.in/48178

One of your classmates has suggested the following modified version of a standard scheme for solving the 2-process critical section problem (CSP).

```
shared char want[2] = {0,0};
shared int turn = 0;
    P_i()
    { while (1) {
        turn = j;
        want[i] = 1;
        while (want[j] && turn!=i);
        critical_section();
        want[i] = 0;
        remainder_section();
        }
    }
```

Show that the above scheme does not guarantee mutual exclusion by constructing an appropriate interleaved sequence of instructions executed by two processes P_0 and P_1.
Modify the above scheme so that it becomes a correct solution to the 2-process CSP.

isi2011 descriptive operating-system process-synchronization

Answer

5.25.41 Process Synchronization: ISI2013-CS-5a top

http://gateoverflow.in/47639

Suppose that an operating system provides two functions, $block()$ which puts the calling process on the blocked queue, and $wakeup(P)$ which moves process P to the runnable queue if it is currently on the blocked queue (otherwise, its behaviour is unpredictable). Consider two processes A and B running the code given below. The intended behaviour of the code is to have A and B run forever, alternately printing their names on the screen.

`void A()`
`{ while(1) {`
`block();`
`printf("A");`
`wakeup(B);`
`}`
`}`
	`void B()`
	`{ while(1) {`
	`printf("B");`
	`wakeup(A);`
	`block();`
	`}`
	`}`

i. Construct a scenario in which the intended behaviour would not be observed.

ii. Redesign the code using semaphore(s) so that it works correctly. You should show the initialisation of the semaphore(s), and the calls to $wait()$ and $signal()$ made by A and B.

descriptive isi2013 operating-system process-synchronization

Answer

5.25.42 Process Synchronization: TIFR2010-B-28 top http://gateoverflow.in/18751

Consider the **concurrent** program:

```
x: 1;
    cobegin
        x:= x + 3 || x := x + x + 2
    coend
```

Reading and writing of variables is atomic, but the evaluation of an expression is not atomic.

The set of possible values of variable x at the end of the execution of the program is:

A. $\{4\}$
B. $\{8\}$
C. $\{4, 7, 10\}$
D. $\{4, 7, 8, 10\}$
E. $\{4, 7, 8\}$

tifr2010 process-synchronization

Answer

5.25.43 Process Synchronization: TIFR2010-B-32 top http://gateoverflow.in/19244

Consider the following solution (expressed in Dijkstra's guarded command notation) to the mutual exclusion problem.

```
process P1 is
begin
    loop
    Non_critical_section;
    while not (Turn=1) do
        skip od;
        Critical_section_1;
        Turn=2;
    end loop
end
```

‖

```
process P2 is
begin
    loop
    Non_critical_section;
    while not (turn=2) do
        skip od;
        Critical_section_2;
        Turn=1;
    end loop
end
```

Initially, Turn=1, Assume that the two process run forever and that no process stays in its critical and non-critical section infinitely. A mutual exclusion program is correct if it satisfies the following requirements.

1) Only one process can be in a critical region at a time.

2) Program is a dead-lock free, i.e., if both processes are trying to enter the critical region then at least one of them does enter the critical region.

3) Program is starvation-free; i.e, a process trying to enter the critical region eventually manages to do so.

The above mutual exclusion solution.

a. Does not satisfy the requirement (1).
b. Satisfy the requirement (1) but does not satisfy the requirement (2).
c. Satisfies the requirements (1) and (2), but does not satisfies the requirement (3).
d. Satisfies the requirement (1) and (3), but does not satisfies the requirement (2).
e. Satisfies all the requirement (1), (2), and (3).

tifr2010 operating-system process-synchronization

Answer

5.25.44 Process Synchronization: TIFR2011-B-22 top http://gateoverflow.in/20330

Consider the program

```
P:: x:=1; y:=1; z:=1; u:=0
```

And the program

```
Q:: x, y, z, u := 1, 1, 1, 1; u:= 0
```

Which of the following is true?

a. P and Q are equivalent for sequential processors.
b. P and Q are equivalent for all multi-processor models.
c. P and Q are equivalent for all multi-core machines.
d. P and Q are equivalent for all networks of computers.
e. None of the above

tifr2011 operating-system process-synchronization

Answer

5.25.45 Process Synchronization: TIFR2011-B-28 top http://gateoverflow.in/20575

Consider a basic block:

```
x:= a[i]; a[j]:= y; z:= a[j]
```

optimized by removing common sub expression a[i] as follows:

```
x:= a[i]; z:= x; a[j]:= y.
```

Which of the following is true?

a. Both are equivalent.
b. The values computed by both are exactly the same.
c. Both give exactly the same values only if i is not equal to j.
d. They will be equivalent in concurrent programming languages with shared memory.
e. None of the above.

tifr2011 process-synchronization

Answer

5.25.46 Process Synchronization: TIFR2015-B-14 top http://gateoverflow.in/30077

Consider the following concurrent program (where statements separated by | | with-in cobegin-coend are executed concurrently).

```
x:=1
cobegin
   x:= x + 1 ||    x:= x + 1  ||    x:= x + 1
coend
```

Reading and writing of variables is atomic but evaluation of expressions is not atomic. The set of possible values of x at the end of execution of the program is

a. $\{4\}$
b. $\{2, 3, 4\}$
c. $\{2, 4\}$
d. $\{2, 3\}$
e. $\{2\}$

tifr2015 process-synchronization

Answer

Answers: Process Synchronization

5.25.1 Process Synchronization: GATE1990-2-iii top

http://gateoverflow.in/83859

a-q

b-p

c-r

d-s

5 votes

-- akshay_845 (543 points)

5.25.2 Process Synchronization: GATE1993_22 top

http://gateoverflow.in/2319

parbegin

begin s1 parbegin V(a) V(b) parend end
begin P(a) s2 parbegin V(c) V(e) parend end
begin P(b) s3 V(d) end
begin P(f) P(c) s4 end
begin P(g) P(d) P(e) s5 end
begin s6 parbegin V(f) V(g) parend end

par end

here the statement between parbegin and parend can execute in any order.But the precedence graph shows the order in which the statements should be executed.This strict ordering is achieved using the semaphores.

Initially all the semaphores are 0.

For s1 there is no need of semaphore because it is the first one to execute.

next s2 can execute only when s1 finishes.For this we have a semaphore a on which signal is executed by s1 ,which makes value of a =1.So that S2 can execute after executing wait on a.making a=0;

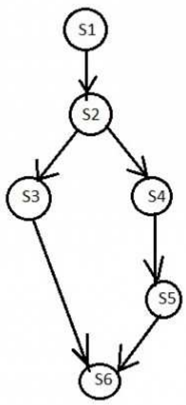
Likewise this is followed for all other statements.

5 votes

-- Sourav Roy (3.6k points)

5.25.3 Process Synchronization: GATE1994_27 top http://gateoverflow.in/2523

precedence graph

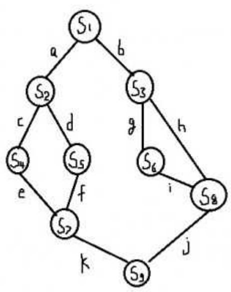


4 votes -- srestha (58.4k points)

5.25.4 Process Synchronization: GATE1995_19 top http://gateoverflow.in/2656

Selected Answer

Precedence graph will be formed as



17 votes -- neha pawar (4.4k points)

5.25.5 Process Synchronization: GATE1996-1.19, ISRO2008-61 top http://gateoverflow.in/2723

Selected Answer

C. is the answer

http://en.wikipedia.org/wiki/Critical_section

A - there is no time guarantee for critical section

B - critical section by default doesn't avoid deadlock. While using critical section, programmer must ensure deadlock is avoided.

D - This is not a requirement of critical section. Only when semaphore is used for critical section management, this becomes a necessity. But, semaphore is just ONE of the ways for managing critical section.

12 votes -- Gate Keeda (19.1k points)

5.25.6 Process Synchronization: GATE1996_2.19 top

http://gateoverflow.in/2748

Selected Answer

acc. to me it should be c) because.. according to condition.. out of all , one philosopher will get both the forks.. so deadlock should not be there.

13 votes -- Sneha Goel (1.2k points)

5.25.7 Process Synchronization: GATE1996_21 top

http://gateoverflow.in/2773

Selected Answer

S1, S2, S3, S4 and S5 are the statements to be executed.

Fork() creates a child to execute in parallel.

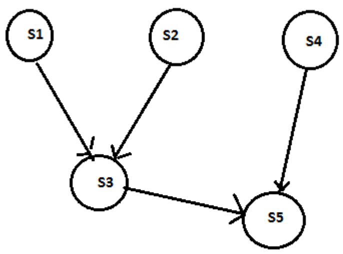
There will be running 3 processes concrruently.
One will execute S1, 2nd will execute S2 and 3rd will execute S4.

Fork L3
L3: S2
Goto L1

now S1 and S2 will join together or it means that one process will terminate and one will continue to execute.

L4: s4
goto L2
Label L2 will be executed by two processes one which was created for S4 and second process S3.

www.csc.lsu.edu/~rkannan/**Fork**_Cobegin_Creationtime.docx
http://www.cis.temple.edu/~giorgio/old/cis307s96/readings/precedence.html



(Precedence Graph)

Initially there was one process which started execution. suppose this process name is p0.

it executed N=2, M=2. after that it executes

Fork: L3,

at L3 these is a statement S2, Fork creates a new process suppose P1 which starts its execution from level L3, means it starts executing S2.

p0 executes fork L4, it creates another new process p2 which starts its execution from level L4 means it starts executing S4.

when p1 finishes execution S2, then it executes next line which is goto L1.
when p2 finishes execution S4, then it executes next line which is goto L2

level L1 is executed by both process p0(S1) and p1(S2)
hence S1 and S2 are combined together, it means either p0 or p1 will terminate and one process will continuate its execution.

Level L2 is executed by two processes S3 and S4 are joined together, it means on of them will terminate and then one which survives will execute final statement S5.

6 votes -- Manu Thakur (6k points)

5.25.8 Process Synchronization: GATE1997_6.8 top

http://gateoverflow.in/2264

Selected Answer

Answer is D
If initial value is 1//execute P1 or P10 first
If initial value is 0, P_10 can execute and make the value 1.
since the both code (ie p1 to p9 and p10)can be executed any number of times and code for p10 is

```
repeat
{
    v(mutex)
    C.S.
    V(mutex)
}
forever
```

now let me say P1 is in c.s
then p10 comes executes the CS(up on mutex)
now P2 comes (down on mutex)
now P10 moves out of CS (again binary semaphore will be 1)
now P3 comes (down on mutex)
now P10 come (up on mutex)
now P4 comes (down on mutex)
so if we take p10 in out of CS recursively all 10 process can be in CS at same time
using Binary semaphore only

20 votes -- Kalpish Singhal (2.1k points)

5.25.9 Process Synchronization: GATE1998-1.30 top

http://gateoverflow.in/1667

Selected Answer

When final result depends on ordering of processes it is called Race condition.
Speed of processes corresponds to ordering of processes.

13 votes -- Digvijay (47k points)

5.25.10 Process Synchronization: GATE1999_20 top

http://gateoverflow.in/1519

Selected Answer

Q-2)

for consumer part

if (count==0)

consumer understands that buffer is full,But before consumer going to sleep It got preempted and went to the Ready Queue

when producer produce an item and make Count=1,it will think consumer is blocked and try to wake up the consumer.

But actually Consumer is not Blocked it is in ready queue

After Some time Consumer come and Go to sleep[as before preemption it had seen that buffer is empty]

producer think that he has woken up consumer and consumer is busy in consuming its produced item and consumer is waitinng for producer wakeup call

After sometime when buffer is full,producer went to sleep thinking that when buffer is empty consumer will wake him up .And consumer is still waiting for producer wakeup call

So now Both are sleeping nd deadlock happens.

After some

8 votes -- Himani Srivastava (699 points)

5.25.11 Process Synchronization: GATE2000-1.21 top

http://gateoverflow.in/645

Selected Answer

P0:m[0] m[1]
P1:m[1] m[2]
P2:m[2] m[3]
P3:m[3] m[0]
P4:m[4] m[1]
po holding mo waiting for m1
p1 holding m1 waiting for m2
p2 holding m2 waiting for m3
p3 holding m3 waiting for m0
p4 holding m4 waiting for m1
So its circular wait and no process can go into critical section even thought its free hence
Answer: B) Deadlock.

21 votes -- Sourav Roy (3.6k points)

Let p[0] , p[1] , p[2] , p[3] and p[4] be the processes.Let p[0] execute the first wait() statement on variable m[0] and preempt then p[1] execute the first wait() statement on m[1] and so on till p[4].

Now lets come back to p[0] and execute the second statement wait(m[(0+1)mod4]) = wait(m[1]) but wait(m[1]) is already done earlier so it will be unsuccessful wait() operation.So we go to p[1] now.It performs m[(1+1)mod4] = m[2].But it is also done earlier so unsuccesful wait() operation.This we continue to do till p[4] so m[(4+1)mod4] = m[1] which is again an unsuccessful wait() operation since it is done earlier..

In short , no process can go into critical section now.Hence the processes are deadlocked.

We should note that preemption of a process can be taken at any point of time i.e. at any line.If by taking a preemption before critical section such that it is leading to deadlock , then we can conclude that the code suffers from deadlock.If we do not find any such instances of preemption , then we can conclude that the code is deadlock free.

Similarly we can check for mutual exclusion also.

Hence , B) option is correct.

14 votes -- HABIB MOHAMMAD KHAN (76.8k points)

5.25.12 Process Synchronization: GATE2000-20 top

http://gateoverflow.in/691

Selected Answer

My attempt :

(a)

1. Give the opportunity for other Readers , so that they can read the C.S. ; Release the mutex ,i.e., Signal(mutex).
2. Similarly to case (1),i.e., Signal(mutex).
3. Check if any Reader(s) or Writer in C.S.(Critical Section) , if there any ; i.e. , R=>1 or W==1.

(b) If atleast one Reader is always present in critical section , then Writer can not be enter in critical section . Hence readers-writers problem may starve writers in the queue.

8 votes -- Mithlesh Upadhyay (5.4k points)

5.25.13 Process Synchronization: GATE2001-2.22 top http://gateoverflow.in/740

Selected Answer

ans is B. suppose two processes p1 and p2. to gurantee mutual exclusion only 1 process must be in CS at a time. now, shared variable is turn P1 P2 f[1]=true f[2]=true turn=2 p1 will now check for condition while(f[2]=true and turn=2) then it will go for busy wait... then p2 will execute and it will update turn=1 p2 will now check condition while(f[1]=true and turn=1) then it will go for busy wait, but here as the value of turn is updated by p2; p1 will be able to enter into CS as the condition will become false therefore p1 will enter CS and p2 will be in busy wai until the p1 will come out and make f[1]=false hence, no two process can enter into CS at a time so predicate p is option B.

14 votes -- jayendra (8.1k points)

5.25.14 Process Synchronization: GATE2002-18 top http://gateoverflow.in/871

B.
i- 1st blank- TestandSet(mutex).
2nd blank- mutext=0;

ii - no.

iii- say given procedure is not atomic. 1st execute process p1. After A1 p1 is preempted. 2nd process p2 now executes full code and enters critical section. P1 resumes and completes the code and enters critical section. So 2 processes are now in critical section.

6 votes -- Avinash MV (179 points)

5.25.15 Process Synchronization: GATE2002-20 top http://gateoverflow.in/873

Selected Answer

a)In Producer Consumer problem Producer produce item and makes the buffer full and after that Consumer consumes that item and makes the buffer empty

Here b_empty and b_full are two semaphore values

```
p1: P(Empty)
```

means, Producer have to wait only if buffer is full and it waits for consumer to remove at least one item. (See, Empty being initialized to BUFFSIZE)

```
p2: V(Full)
```

buffer is filled, now it gives signal to consumer that it can start consuming

```
c1: P(Full)
```

means here consumer have to wait only if buffer is empty, and it waits for Producer to fill the buffer

```
c2: V(Empty)
```

Now buffer is empty and Empty semaphore gives signal to the producer that it can start filling

It is same as giving water to a thirsty man.

Here u are giving water in a glass to that thirsty man, so u are producer here

and the man drinks and makes the glass empty, so he is consumer here

b) If there are multiple user we can use mutex semaphore, so that exclusively one could enter in Critical section at a time. i.e.

```
p1:P(Empty)
   P(mutex)

p2:V(mutex)
     V(Full)

c1:P(Full)
    P(mutex)

c2: V(mutex)
     V(Empty)
```

PS: One thing to see is P(mutex) is after P(Full) and P(empty)- otherwise deadlock can happen when buffer is full and a producer gets mutex or if buffer is empty and a consumer gets mutex.

9 votes -- srestha (58.4k points)

5.25.16 Process Synchronization: GATE2003-80 top http://gateoverflow.in/964

Selected Answer

To get pattern 001100110011

Process p should be executed first then **Process Q** should b executed

So at Process P : **W** P(S) **X** V(T)

and at Process Q :**Y** V(T) **Z** V(S)

with **S=1 and T=0** initially (only **P** has to be run first then only **Q** is run , both process run on alternet way start with **P**)

So ans is B

15 votes -- Pooja Palod (32.4k points)

5.25.17 Process Synchronization: GATE2003-81 top http://gateoverflow.in/43574

Selected Answer

output shouldn't contain substring of given form means no concurrent execution process P as well as Q. one semaphore is enough

So ans is c

15 votes -- Pooja Palod (32.4k points)

5.25.18 Process Synchronization: GATE2004-48 top http://gateoverflow.in/1044

Selected Answer

option A) deadlock p1 : line1|p2:line3| p1: line2(block) |p2 :line4(block)

so here p1 want s(x) which is held by p2 and p2 want s(y) which is held by p1 ...

so its **circular wait (hold and wait condition)** .. so there is **deadlock**

option B) deadlock p1 : line 1| p2 line 3|p1: line 2(block) |p2 : line 4(block)

so here p1 wants sy which is held by p2 and p2 wants sx which is held by p1...so its**circular wait (hold and wait) so deadlock**

option c) p1 :line 1|p2 :line 3| p2 line 4(block) |p1 line 2 (block) here p1 wants sx and p2 wants sy .. but both will not be release by its process p1 and p2 because there is no way to release them ...so stuck in **deadlock** ..

option d) p1 :line 1 |p2 : line 3(block because need sx) |p1 line 2 |p2 : still block |p1 : execute cs then up the value of sx |p2 :line 3 line 4(block need sy)| p1 up the sy |p2 :lin4 4 and easily get cs ..

we can start from p2 also ... as I answered according only p1 ... but we get same answer ....

so **option D)** is correct

13 votes -- sonam vyas (13.2k points)

5.25.19 Process Synchronization: GATE2004-IT-65 top http://gateoverflow.in/3708

Selected Answer

P_1 is the producer. So, it must wait for full condition. But semaphore full is initialized to 0 and semaphore empty is initialized to n, meaning $full = 0$ implies no item and $empty = n$ implies space for n items is available. So, P_1 must wait for semaphore empty - $K - P(\text{empty})$ and similarly P_2 must wait for semaphore full - $M - P(\text{full})$. After accessing the critical section (producing/consuming item) they do their respective V operation. Thus option D.

22 votes -- Arjun Suresh (294k points)

5.25.20 Process Synchronization: GATE2005-IT-41 top http://gateoverflow.in/3788

Selected Answer

Check : What is Starvation?

Here P_2 can go in infinite waiting while process P_1 executes infinitely long.

Also, it can be the case that the Process P_1 starves for ∞ long time on the semaphore S, after it has successfully executed its critical section once, while P_2 executes infinitely long.

Both P_1 and P_2 can starve for ∞ long period of time.

answer = **option A**

23 votes -- Amar Vashishth (28.7k points)

A is the answer.

Case 1:Here P1 is performing signal operation so it is first one to start...Now it may happen that after executing CS it makes X=0 again tries to enter CS my making X=1 so it is possible that P2 can starve(just a possibility)

Case 2:If P1 executes signal operation and its execution is suspended temporarily, P2 executes wait and enter CS and then execute signal operation making X=1 now P2 can enter critical section by executing wait operation..this may happen for infinite amount of time..so in this P1 may starve

18 votes -- Pooja Palod (32.4k points)

5.25.21 Process Synchronization: GATE2005-IT-42 top http://gateoverflow.in/3789

Selected Answer

Answer is (B)

It needs two semaphores. x=0 ,y=0

P1	P2
P(X)	
R1	R1
	V(X)
	P(Y)
R2	R2
V(Y)	
P(X)	
R3	R3
	V(X)
	P(Y)
R4	R4
V(Y)	

20 votes -- Sandeep_Uniyal (7.3k points)

5.25.22 Process Synchronization: GATE2006-61 top http://gateoverflow.in/1839

Selected Answer

Option (B) :- If we use normal load & Store instead of Fetch & Set there is good chance that more than one Process sees S.value as 0 & then mutual exclusion wont be satisfied. So this option is wrong.

Option (C) :- Here we are setting S->value to 0, which is correct. (As in fetch & Set we wait if value of S-> value is 1. So implementation is correct. This option is wrong.

Option (D) :- I don't see why this code does not implement binary semaphore, only one Process can be in critical section here at a time. So this is binary semaphore & Option D is wrong

Answer :- Option A. This is correct because the implementation may not work if context switching is disabled in P , then process which is currently blocked may never give control to the process which might eventually execute V. So Context switching is must !

27 votes -- Akash (43.8k points)

5.25.23 Process Synchronization: GATE2006-78 top http://gateoverflow.in/1853

Selected Answer

B is the correct answer.

Let 3 processes p1, p2 , p3 arrives at the barrier and after 4th step*process_arrived=3*. and the processes enters the barrier. Now suppose process p1 executes the complete code and makes *process_left=1*, and tries to re-enter the barrier. Now, when it executes 4th step, *process_arrived=4*. p1 is now stuck. At this point all other processes p2 and p3 also executes their section of code and resets *process_arrived=0* and *process_left=0*. Now, p2 and p3 also tries to re-enter the barrier making *process_arrived=2*. At this point all processes have arrived, but *process_arrived!=3*. Hence no process can re-enter into the barrier, therefore DEADLOCK!!

Let me know, if i'm right..?

24 votes -- GateMaster Prime (1.6k points)

5.25.24 Process Synchronization: GATE2006-79 top http://gateoverflow.in/43564

Selected Answer

The implementation is incorrect because if two barrier invocations are used in immediate succession the system will fall into a DEADLOCK.

Here's how: Let all three processes make `process_arrived` variable to the value
3, as soon as it becomes
3 previously stuck processes at the while loop are now free, to move out of the while loop.

But for instance let say one process moves out and has bypassed the next `if` statement & moves out of the `barrier` function and The SAME process is invoked again(its second invocation) while other processes are preempted still.

That process on its second invocation makes the `process_arrived` variable to
4 and gets stuck forever in the while loop with other processes.

At this point of time they are in DEADLOCK. as only 3 processes were in the system and all are now stuck in while loop.

Q.79 answer = **option B**

option A here is false as there will always be a need for some process to help some other process to move out of that while loop waiting. Not all processes together can be said to be completed at a time.

option C is false. If context switch is disabled then the process who was stuck in while loop will remain there forever and no other process can play a role in bringing it out of there as Context Switch will be required to bring that other process in the system to do the job.

option D is false. everyone will be in a loop forever, if that happens.

option B is TRUE. at the beginning of the barrier the
1^{st} process to enter Critical section should wait until process_arrived becomes zero(i.e. before starting its second invocation). this is to prevent it from making `process_arrived` value greater than
3 i.e. rectifying the flaw observed in Q.78

13 votes -- Amar Vashishth (28.7k points)

5.25.25 Process Synchronization: GATE2006-IT-55 top http://gateoverflow.in/3598

Selected Answer

Suppose the slots are full -> F = 0. Now, if Wait(F) and Wait(S) are interchanged and Wait(S) succeeds, The producer will wait for Wait(F) which is never going to succeed as Consumer would be waiting for Wait(S). So, deadlock can happen.

If Signal(S) and Signal(F) are interchanged in Consumer, deadlock won't happen. It will just give priority to a producer compared to the next consumer waiting.

So, answer (A)

23 votes -- Arjun Suresh (294k points)

5.25.26 Process Synchronization: GATE2007-58 top http://gateoverflow.in/1256

Selected Answer

P1 can do wants1 = true and then P2 can do wants2 = true. Now, both P1 and P2 will be waiting in the while loop indefinitely without any progress of the system - deadlock.

When P1 is entering critical section it is guaranteed that wants1 = true (wants2 can be either true or false). So, this ensures P2 won't be entering the critical section at the same time. In the same way, when P2 is in critical section, P1 won't be able to enter critical section. So, mutual exclusion condition satisfied.

So, D is the correct choice

Suppose P1 first enters critical section. Now suppose P2 comes and waits for CS by making wants2 = true. Now, P1 cannot get access to CS before P2 gets and similarly if P1 is in wait, P2 cannot continue more than once getting access to CS.

Thus there is a bound (of 1) on the number of times another process gets access to CS after a process requests access to it and hence bounded waiting condition is satisfied.

---

https://cs.stackexchange.com/questions/63730/how-to-satisfy-bounded-waiting-in-case-of-deadlock

26 votes -- Arjun Suresh (294k points)

The answer is D.

At the very 1st line itself you can see that it causes Deadlock.

Execute P1 till wants1=True; then Preempt.

Execute P2 till wants2=True; then Preempt P2 and let it enter into P1 and P1 into P2.

Since,

While (wants2==True);------------> This will lead to infinite loop. Coz of that semicolon, which makes the while loop terminate only when the condition inside the loop becomes False.

Similarly,

While (wants1==True);------------> Will also lead to infinite loop.

Hence the system is in Deadlock and Answer is D which is true.

10 votes -- Gate Keeda (19.1k points)

5.25.27 Process Synchronization: GATE2007-IT-10 top http://gateoverflow.in/3443

Selected Answer

(C).. both process can run the critical section concorrently.. lets say p1 starts and it enters inside if clause.. and just after its enterence and before execution of critical_flag = TRUE, a context switch happens and p2 also gets entrance since the flag is still false.. so now both process are in critical section!! so (i) is true.. (ii) is false there is no way that flat is true and no process' are inside the if clause, if someone enters the critical section, it will definetly make flag = false.. so no deadlock

23 votes -- Vicky Bajoria (4.9k points)

5.25.28 Process Synchronization: GATE2007-IT-56 top http://gateoverflow.in/3498

Selected Answer

Answer is (C)

S1: if readcount is1 i.e some reader is reading, DOWN on wrt so that no writer can write.

S2:After readcount has been updated , UP on mutex.

S3:DOWN on mutex to update readcount

S4: If readcount is zero i.e no reader is reading ,UP on wrt .Allow writer to Write

8 votes -- Sandeep_Uniyal (7.3k points)

5.25.29 Process Synchronization: GATE2008-IT-53 top http://gateoverflow.in/3363

Selected Answer

producer: consumer: while (true) do while (true) do 1 P(S); 1 P(Q); 2 x = produce (); 2 consume (x); 3 V(Q); 3 V(S); done done

Lets explain the working of this code.

It is mentioned that P and C execute parallely.

P:1 2 3

1. S value is 1 ,down on 1 makes it 0.enters the statement 2

2 .item produced.

3.up on Q is done(Since the queue of Q is empty ,value of Q up to 1).

This being an infinite while loop should infinitely iterate.

In the next iteration of while loop st 1 is executed.

But S is already 0 ,further down on 0 sends P to blocked list of S.P is blocked.

C Consumer is scheduled.

Down on Q.value makes Q.value=0;

Enters the statement 2 ,consumes the item.

Up on S,now instead of changing the value of S.value to 1,wakes up the blocked process on Q 's queue.Hence process P is awaken. P resumes from statement 2,since it was blocked at statement 1. So P now produces the next item.

So consumer consumes an item before producer produces the next item.

D)Ans

A)deadlock cannot happen has both producer and consumer are operating on different semaphores(no hold and wait)

B)No starvation happen because there is alteration between P and Consumer.Which also makes them have bounded waiting.

8 votes -- Sourav Roy (3.6k points)

D Consumer can consume only once the producer has produced the item, and producer can produce(except the first time) only once the consumer has consumed the item.

16 votes -- Shaun Patel (6.9k points)

5.25.30 Process Synchronization: GATE2009-33 top http://gateoverflow.in/1319

Selected Answer

The answer is A only.

The solution satisfies:

1) Mutual Exclusion as test-and-set is an indivisible (atomic) instruction (makes option IV wrong)

2) Progress as at initially X is 0 and at least one process can enter critical section at any time.

But no guarantee that a process eventually will enter CS and hence option IV is false. Also, no ordering of processes is maintained and hence III is also false.

So eliminating all the 3 choices remains A.

13 votes -- Gate Keeda (19.1k points)

5.25.31 Process Synchronization: GATE2010-23 top http://gateoverflow.in/2202

Selected Answer

ans is A ..in this mutual exclusion is satisfied,only one process can access the critical section at particular time but here progress will not satisfied because suppose when s1=1 and s2=0 and process p1 is not interested to enter into critical section but p2 want to enter critical section. P2 is not able to enter critical section in this as only when p1 finishes execution, then only p2 can enter (then only s1 = s2 condition be satisfied). Progress will not be satisfied when any process which is not interested to enter into the critical section will not allow other interested process to enter into the critical section.

28 votes -- neha pawar (4.4k points)

5.25.32 Process Synchronization: GATE2010-45 top http://gateoverflow.in/2347

Selected Answer

There are lots of complicated answers, writing just for the simplifications:
there are only 2 possible execution sequence here
1. p0->p1->p0->p2->p0   p0 is executed thrice here will print 0 thrice.

2. p0->p1->p2->p0   p0 is executed twice only.

Hence answer is "atleast twice".

23 votes -- Vijay Thakur (15.4k points)

First P0 will enter the while loop as S0 is 1. Now, it releases both S1 and S2 and one of them must execute next. Let that be P1. Now, P0 will be waiting for P1 to finish. But in the mean time P2 can also start execution. So, there is a chance that before P0 enters the second iteration both P1 and P2 would have done release (S0) which would make S1 1 only (as it is a binary semaphore). So, P0 can do only 1 more iteration printing '0' two times.
If P2 does release (S0) only after P0 starts its second iteration, then P0 would do three iterations printing '0' three times.

If the semaphore had 3 values possible (an integer semaphore and not a binary one), exactly three '0's would have been printed.

12 votes -- Arjun Suresh (294k points)

5.25.33 Process Synchronization: GATE2012_32 top http://gateoverflow.in/1750

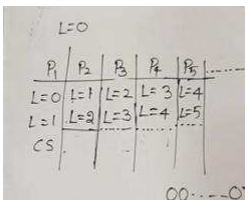
Selected Answer

A process acquires a lock only when L = 0. When L is 1, the process repeats in the while loop- there is no overflow because after each increment to L, L is again made equal to 1. So, the only chance of overflow is if a large number of processes (larger than sizeof(int)) execute the check condition of while loop but not L = 1, which is highly improbable.

Acquire Lock gets success only when Fetch_And_Add gets executed with L = 0. Now suppose P1 acquires lock and make L = 1. P2 waits for a lock iterating the value of L between 1 and 2 (assume no other process waiting for lock). Suppose when P1 releases lock by making L = 0, the next statement P2 executes is L = 1. So, value of L becomes 1 and no process is in critical section ensuring L can never be 0 again. Thus B choice.

To correct the implementation we have to replace Fetch_And_Add with Fetch_And_Make_Equal_1 and remove L=1 in AcquireLock(L).

38 votes -- Arjun Suresh (294k points)



L is a unsigned integer it has limited memory

Have a look at the image

let say initial value of L =0

Let say process P1 entered and it will read L=0 (it will fatch it and add L=1) and enter CS .

Let say next process P2 entered it will read L=1 and when it execute the while loop it will fetch and add L=1 and add 1 to it and make it 2

But in case if p2 preempt after reading while loop and before reading L=1

if p3 comes after it then it will fetch l value which 2 and add 1 to it and make it 3 and preempt at this point before executing next line after while loop which is L=1.

same with P4, P5, P6,.........Pn

in this way after some times L overflow because it is a unsigned Integer .

it makes L Overflow ans ANSWER A as correct.

Consider the situation. when first process P1 Acquired Lock it has
lock value = 0. so it will automatically increment the L value to 1
and return 0. Now returning a value 0 means => While(0) hence loop breaks.
And breaking of while loop implies process has entered the critical section
and has not executed line (L=1;)inside while loop but still currently L=1 since Fetch_And_Add(0,1) has increased the value to 1(L'=L+i //1=0+1) first time P1 executed it.

Now a process P2 comes it reads value of L as 1.It execute statement Fetch_And_Add(L,i)
returning value as 1(i.e old value) but increasing the value of L to 2(L'=L+i //2=1+1)
Now since value returned to while loop is 1 =>(implies) while(1) and process will enter
the while loop and will set the value of L back to 1 by statement (L=1;)
This process P2 or any other process say P3,P4... will read value of L as 1
it will increment to 2, enter the while loop, set it back to 1 hence other process falling in infinite loop.
(L values will be like 1->2->1->2->1->2.... so on)
till P1 doesn't release the Lock(i.e come out of critical section) and set value of L=0;(Release Lock)

now consider the situation of overflow
P1 has already entered the critical section. P2 comes and read the Value of L as 1.
It executes Fetch_And_Add(L,i). In this case Fetch_And_Add(1,1) changing value of
L to 2 //L=L+i;Now before executing the the statement L=1; P3 comes read value of L as 2
and execute Fetch_And_Add(L,i) increasing the value to 3.Again before it could execute the line
L=1;P4 comes read value as 3 and execute Fetch_And_Add(L,i) making value of L as 4.
If same thing happens with rest of the coming process L value will be so large
that variable would be unable to hold and hence there would be overflow.
B is also true as explained in solution.
C is false since there is starvation.consider the case P1 is in critical section P2 is waiting in while loop.As P1 release the lock P3 acquires,P3 release lock P4 acquires.Hence P2 will be in starvation

19 votes -- shekhar chauhan (42.9k points)

5.25.34 Process Synchronization: GATE2013_34 top http://gateoverflow.in/1545

Selected Answer

Since initial value of semaphore is 2, two processes can enter critical section at a time- this is bad and we can see why.

Say, X and Y be the processes. X increments x by 1 and Z decrements x by 2. Now, Z stores back and after this X stores back. So, final value of x is 1 and not -1 and two Signal operations make the semaphore value 2 again. So, now W and Z can also execute like this and the value of x can be **2 which is the maximum possible** in any order of execution of the processes.

(If the semaphore is initialized to 1, processed would execute correctly and we get the final value of x as -2.)

28 votes -- Arjun Suresh (294k points)

5.25.35 Process Synchronization: GATE2013_39 top http://gateoverflow.in/1550

Selected Answer

A choice:

X is waiting on R and Y is waiting on X. So, both cannot proceed.

B choice:

Process X is doing Signal operation on R and S without any wait and hence multiple signal operations can happen on the binary semaphore so Process Y won't be able to get exactly n successful wait operations. i.e., Process Y may not be able to complete all the iterations.

C choice:

Process X does Wait(S) followed by Signal(R) while Process Y does Signal(S) followed by Wait(R). So, this ensures that no two iterations of either X or Y can proceed without an iteration of the other being executed in between. i.e., this ensures that all n iterations of X and Y succeeds and hence the answer.

D choice:

Process X does Signal(R) followed by Wait(S) while Process Y does Signal(S) followed by Wait(R). There is a problem here that X can do two Signal(R) operation without a Wait(R) being done in between by Y. This happens in the following scenario:

Process Y: Does Signal (S); Wait(R) fails; goes to sleep.
Process X: Does Signal(R); Wait(S) succeeds; In next iteration Signal(R) again happens;

So, this can result in some Signal operations getting lost as the semaphore is a binary one and thus Process Y may not be able to complete all the iterations. If we change the order of Signal(S) and Wait(R) in EntryY, then D option also can work.

30 votes -- Arjun Suresh (294k points)

5.25.36 Process Synchronization: GATE2014-2-31 top http://gateoverflow.in/1990

Selected Answer

option A) False :

producer =P (let) , consumer = C(let) , once producer produce the item and put into the buffer .. it will up the s and n to 1 , so consumer can easily consume the item ...so option A Is false ...

code can be execute in this way : P :1 2 3 4 5| C: 1 2 3 4 5... so consumer can consume item after adding the item to buffer.

option B) Is also False , becoz whenever item is added to buffer means after producing the item . consumer can consume the item or we can say remove the item ... if here statement is like The consumer will remove no more than one item from the buffer just after the removing one then it will be true(due n=0 then it will be blocked) ... but here only asking about The consumer will remove no more than one item from the buffer so its false ...

option C) is true , statement says if consumer execute first means buffer is empty ...then execution will be like this

C:1 (wait on s , s=0 now) 2(BLOCK n =-1) |P : 1 2(wait on s which is already 0 so it now block) .. so c wants n which is held by producer or we can say up by only producer and P wants s , which will be up by only consumer ..(circular wait) surely there is deadlock.

option D) is false if n=1 then also it will not free from deadlock ....

for the given execution .. C: 1 2 3 4 5 1 2(BLOCK) | P: 1 2(BLOCK) so deadlock ...

(here 1 2 3 4 5 are the lines of the given code)

hence **answer is C)**

18 votes -- sonam vyas (13.2k points)

5.25.37 Process Synchronization: GATE2015-3_10 top http://gateoverflow.in/8405

Selected Answer

When both processes try to enter critical section simultaneously,both are allowed to do so since both shared variables varP and varQ are true. So, clearly there is **NO mutual exclusion.** Also, **deadlock is prevented** because mutual exclusion is one of the conditions for deadlock to happen. Hence, answer is **A**.

36 votes -- Tanaya Pradhan (409 points)

5.25.38 Process Synchronization: GATE2016-2-48 top http://gateoverflow.in/39600

Selected Answer

There is strict alternation i.e. after completion of process 0 if it wants to start again.It will have to wait until process 1 gives the lock.
This violates progress requirement which is, that no other process outside critical section can stop any other interested process from entering the critical section.
Hence the answer,is that it violates the progress requirement.

The given solution does not violate bounded waiting requirement.

Bounded waiting is : There exists a bound, or limit, on the number of times other processes are allowed to enter their critical sections after a process has made request to enter its critical section and before that request is granted.

Here there are only two processes and when process 0 enters CS, next entry is reserved for process 1 and vice-versa (strict alteration). So, bounded waiting condition is satisfied here.

27 votes -- bahirNaik (3.7k points)

5.25.39 Process Synchronization: GATE2017-1-27 top http://gateoverflow.in/118307

Selected Answer

I think D is the correct answer.

If we see definition of **reentrant Lock :**

In computer science, the **reentrant mutex** (**recursive mutex**, **recursive lock**) is particular type of mutual exclusion (mutex) device that may be locked multiple times by the same process/thread, **without causing a deadlock.** https://en.wikipedia.org/wiki/Reentrant_mutex

A `ReentrantLock` is *owned* by the thread last successfully locking, but not yet unlocking it. A thread invoking `lock` will return, successfully acquiring the lock, when the lock is not owned by another thread. **The method will return immediately if the current thread already owns the lock** https://docs.oracle.com/javase/7/docs/api/java/util/concurrent/locks/ReentrantLock.html

I think Reentrant property is provided, so that a process who owns a lock , can accuire same lock multiple times. Here it is non-reentrant as given, process cant own same lock multiple times, so if process tries to accuire already owned lock, will get blocked , and deadlock will happen.

So answer is D

14 votes -- harkirat31 (361 points)

5.25.40 Process Synchronization: ISI2011-CS-5c top http://gateoverflow.in/48178

Selected Answer

let process p1 enters it executed 3 line i.e turn=j means it made turn=0 (as p1 entered so i=1 j=0) now assume p1 got preempted

now process p0 enterted it executed 3 line made turn=1 (as p0 entered so i=0 j=1)

after that p0 executed 4 line made want[0]=1

next p0 executed 5 line while(0 &&true) which is false so it entered critical section

now p1 resumed and executed 4 line made want[1]=1

next p1 executed 5 line while(1 &&false) which is false so it entered critical section

now both process p0& p1 are in CS at same time so above solution is wrong the correct solution is as follows:

just interchange line 3 & line 4...than solution becomes correct

```
shared char want[2] = {0,0};
shared int turn = 0;
1.  P_i()
2.  { while (1) {
3.      want[i] =1;
4.      turn = j:
5.      while (want[j] && turn!=i);
6.      critical_section();
7.      want[i] = 0;
8.      remainder_section();
9.      }
10. }
```

2 votes -- Tauhin Gangwar (9.3k points)

5.25.41 Process Synchronization: ISI2013-CS-5a top

http://gateoverflow.in/47639

Selected Answer

now.... consider a scenario...process B arrives..and it executes...till the step wakeup(A) & after this step..process B Pr-eemptes..now process A arrives..it get block as it executes block() call..now after that process B ..returns and it also executes block() call...so it is also..blocked..now process A is waiting 4 process B...to wakeup & process B is waiting 4 process A...to wakeup..so this clearly deadlock..

correct code

let binary semphore X = 1 , Y=0;

`void A() { while(1) { P(X) printf("A"); V(Y) } }`	`voidB() { while(1) { P(Y) printf("B"); V(X) } }`

3 votes -- Tauhin Gangwar (9.3k points)

5.25.42 Process Synchronization: TIFR2010-B-28 top

http://gateoverflow.in/18751

Selected Answer

```
cobegin
    x:= x + 3 || x := x + x + 2
coend
```

This implies that the two statements x:=x+3 and x :=x+x+2 can execute sequentially as well as parallelly..

Now,

Sequential part :

x:= x + 3 || x := x + x + 2

x =1(initial value)

First run x = x+3 , value of x becomes 4

Now x=4, run x = x + x + 2 value of x will be 4+4+2=10

Finally x becomes 10.

Parallel part:

Initialized value of x =1

Both will take x as 1 initially and then run independently, So

x= x+3 = 1+3 = 4

x=x+x+2= 1+1+2 = 4

But final write will be done by the process x=x+x+2

It will give value 4.

x=x+x+2 completed its execution before x=x+3.

Then x= x+3 will read value of x as 4 and then x=x+3 i.e. x= 4+3 = 7

so here we get { 4,7 }

Final answer is combination of both sequential and parallel part :

which is { 4,7,10 }

Option C .

2 votes -- Soumya Jain (1.6k points)

5.25.43 Process Synchronization: TIFR2010-B-32 top

http://gateoverflow.in/19244

Selected Answer

Process P1 while loop says : while NOT (turn = 1) do ... so it will not enter the while loop until Turn = 2 which will make Turn=1 false and thus NOT (Turn =1) as true.

Process P2 for the same reason will enter the while loop.

as process P2 has statement Turn = 1 at the end of the while loop so the value of Turn will always remain 1 ... So process P1 will never enter the while loop and So this will result in starvation of Process P1

Hence answer is (C) ... hopefully !!!

3 votes -- Danish (3.6k points)

5.25.44 Process Synchronization: TIFR2011-B-22 top

http://gateoverflow.in/20330

Selected Answer

Both the programs are equivalent in the sense that the output will be the same at the end of execution. Q just writes 1 to u but this will be overwritten by the following write of 0. So, in any computer both P and Q should produce the same result at the end of execution.

6 votes -- Arjun Suresh (294k points)

5.25.45 Process Synchronization: TIFR2011-B-28 top

http://gateoverflow.in/20575

Selected Answer

e)
as in 1st z = a[j] =y

whereas in 2nd z = x ;

so z is getting different values

(Also there's typo in question , expression a[j] has been removed)

3 votes -- Vertika Srivastava (697 points)

5.25.46 Process Synchronization: TIFR2015-B-14 top http://gateoverflow.in/30077

Selected Answer

Reading and writing is atomic but evaluation not atomic

So,

1) read 1, evaluate 1 time, write 2

2)read 1, evaluate 2 time, write 3

3)read 1, evaluate 3 time, write 4

Answer will be (B)2,3,4

5 votes -- srestha (58.4k points)

5.26 Resource Allocation(26) top

5.26.1 Resource Allocation: GATE 2016-1-50 top http://gateoverflow.in/39719

Consider the following proposed solution for the critical section problem. There are n processes : $P_0 \dots P_{n-1}$. In the code, function pmax returns an integer not smaller than any of its arguments .For all $i, t[i]$ is initialized to zero.

Code for P_i;

```
do {
    c[i]=1; t[i]= pmax (t[0],....,t[n-1])+1; c[i]=0;
    for every j != i in {0,....,n-1} {
        while (c[j]);
        while (t[j] != 0 && t[j] <=t[i]);
    }
    Critical Section;
    t[i]=0;

    Remainder Section;

}  while (true);
```

Which of the following is TRUE about the above solution?

A. At most one process can be in the critical section at any time
B. The bounded wait condition is satisfied
C. The progress condition is satisfied
D. It cannot cause a deadlock

gate2016-1 operating-system resource-allocation difficult ambiguous

Answer

5.26.2 Resource Allocation: GATE1992_02,xi top http://gateoverflow.in/568

02. Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

(xi) A computer system has 6 tape devices, with n processes competing for them. Each process may need 3 tape drives. The maximum value of n for which the system is guaranteed to be deadlock free is:

a. 2
b. 3
c. 4
d. 1

gate1992 operating-system resource-allocation normal

Answer

5.26.3 Resource Allocation: GATE1993-7.9, UGCNET-Dec2012-III-41 top http://gateoverflow.in/2297

Consider a system having m resources of the same type. These resources are shared by 3 processes A, B and C which have peak demands of 3, 4 and 6 respectively. For what value of m deadlock will not occur?

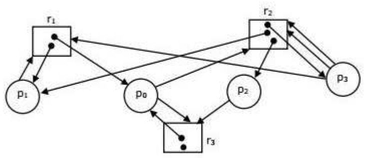
A. 7
B. 9
C. 10
D. 13
E. 15

gate1993 operating-system resource-allocation normal ugcnetdec2012iii

Answer

5.26.4 Resource Allocation: GATE1994_28 top http://gateoverflow.in/2524

Consider the resource allocation graph in the figure.



a. Find if the system is in a deadlock state
b. Otherwise, find a safe sequence

gate1994 operating-system resource-allocation normal

Answer

5.26.5 Resource Allocation: GATE1996_22 top http://gateoverflow.in/2774

A computer system uses the Banker's Algorithm to deal with deadlocks. Its current state is shown in the table below, where P0, P1, P2 are processes, and R0, R1, R2 are resources types.

	Maximum Need				**Current Allocation**			**Available**		
	R0	**R1**	**R2**		**R0**	**R1**	**R2**	**R0**	**R1**	**R2**
P0	4	1	2	**P0**	1	0	2	2	2	0
P1	1	5	1	**P1**	0	3	1			
P2	1	2	3	**P2**	1	0	2			

a. Show that the system can be in this state
b. What will the system do on a request by process P0 for one unit of resource type R1?

gate1996 operating-system resource-allocation normal

Answer

5.26.6 Resource Allocation: GATE1997_6.7 top http://gateoverflow.in/2263

An operating system contains 3 user processes each requiring 2 units of resource R. The minimum number of units of R such that no deadlocks will ever arise is

A. 3
B. 5
C. 4
D. 6

gate1997 operating-system resource-allocation normal

Answer

5.26.7 Resource Allocation: GATE1997_75 top

http://gateoverflow.in/19705

An operating system handles requests to resources as follows.

A process (which asks for some resources, uses them for some time and then exits the system) is assigned a unique timestamp are when it starts. The timestamps are monotonically increasing with time. Let us denote the timestamp of a process P by TS(P).

When a process P requests for a resource the OS does the following:

i. If no other process is currently holding the resource, the OS awards the resource to P.

ii. If some process Q with TS(Q)

iii. If some process Q with TS(Q)>TSP(P) is holding the resource, the OS restarts Q and awards the resources to P. (Restarting means taking back the resources held by a process, killing it and starting it again with the same timestamp)

When a process releases a resource, the process with the smallest timestamp (if any) amongst those waiting for the resource is awarded the resource.

a. Can a deadlock over arise. If yes, show how. If not prove it.

b. Can a process P ever starve? If yes, show how. If not prove it.

gate1997 operating-system resource-allocation

Answer

5.26.8 Resource Allocation: GATE1998_1.32 top

http://gateoverflow.in/1669

A computer has six tape drives, with n processes competing for them. Each process may need two drives. What is the maximum value of n for the system to be deadlock free?

a. 6
b. 5
c. 4
d. 3

gate1998 operating-system resource-allocation normal

Answer

5.26.9 Resource Allocation: GATE2000-2.23 top

http://gateoverflow.in/670

Which of the following is not a valid deadlock prevention scheme?

A. Release all resources before requesting a new resource.
B. Number the resources uniquely and never request a lower numbered resource than the last one requested.
C. Never request a resource after releasing any resource.
D. Request and all required resources be allocated before execution.

gate2000 operating-system resource-allocation normal

Answer

5.26.10 Resource Allocation: GATE2001-19 top http://gateoverflow.in/760

Two concurrent processes P1 and P2 want to use to resources R1 and R2 in a mutually exclusive manner. Initially, R1 and R2 are free. The programs executed by the two processes are given below.

Program for P1:

S1: While (R1 is busy) do no-op;
S2: Set R1 $\leftarrow$ busy;
S3: While R2 is busy do no-op;
S4: Set R2 $\leftarrow$ busy;
S5: Use R1 and R2;
S6: Set R1 $\leftarrow$ free;
S7: Set R2 $\leftarrow$ free;

Program for P2:

Q1: While R1 is busy do no-op
Q2: Set R1 $\leftarrow$ busy
Q3: While (R1 is busy) do no-op;
Q4: Set R1 $\leftarrow$ busy
Q5: Use R1 and R2
Q6: Set R2 $\leftarrow$ free
Q7: Set R2 $\leftarrow$ free

a. Is mutual exclusion guaranteed for R1 and R2? If not show a possible interleaving of the statements of P1 and P2 such mutual exclusion is violated (i.e., both P1 and P2 use R1 and R2 at the same time).
b. Can deadlock occur in the above program? If yes, show a possible interleaving of the statements of P1 and P2 leading to deadlock.
c. Exchange the statements Q1 and Q3 and statements Q2 and Q4. Is mutual exclusion guaranteed now? Can deadlock occur?

gate2001 operating-system resource-allocation normal descriptive

Answer

5.26.11 Resource Allocation: GATE2004-IT-63 top http://gateoverflow.in/3706

In a certain operating system, deadlock prevention is attemped using the following scheme. Each process is assigned a unique timestamp, and is restarted with the same timestamp if killed. Let P_h be the process holding a resource R, P_r be a process requesting for the same resource R, and $T(P_h)$ and $T(P_r)$ be their timestamps respectively. The decision to wait or preempt one of the processes is based on the following algorithm.

```
if T(Pr) < T(Ph) then
    kill Pr
else wait
```

Which one of the following is TRUE?

A. The scheme is deadlock-free, but not starvation-free
B. The scheme is not deadlock-free, but starvation-free
C. The scheme is neither deadlock-free nor starvation-free
D. The scheme is both deadlock-free and starvation-free

gate2004-it operating-system resource-allocation normal

Answer

5.26.12 Resource Allocation: GATE2005-71 top http://gateoverflow.in/1394

Suppose n processes, $P_1, \dots P_n$ share m identical resource units, which can be reserved and released one at a time. The maximum resource requirement of process P_i is s_i, where $s_i > 0$. Which one of the following is a sufficient condition for ensuring that deadlock does not occur?

A. $\forall i,\ s_i, < m$

B. $\forall i,\ s_i < n$

C. $\Sigma_{i=1}^{n}\ s_i < (m + n)$

D. $\Sigma_{i=1}^{n}\ s_i < (m \times n)$

gate2005 operating-system resource-allocation normal

Answer

5.26.13 Resource Allocation: GATE2005-IT-62 top

http://gateoverflow.in/3823

Two shared resources R_1 and R_2 are used by processes P_1 and P_2. Each process has a certain priority for accessing each resource. Let T_{ij} denote the priority of P_i for accessing R_j. A process P_i can snatch a resource R_h from process P_j if T_{ik} is greater than T_{jk}.
Given the following :

I. $T_{11} > T_{21}$
II. $T_{12} > T_{22}$
III. $T_{11} < T_{21}$
IV. $T_{12} < T_{22}$

Which of the following conditions ensures that P_1 and P_2 can never deadlock?

A. I and IV
B. II and III
C. I and II
D. None of the above

gate2005-it operating-system resource-allocation normal

Answer

5.26.14 Resource Allocation: GATE2006-66 top

http://gateoverflow.in/1844

Consider the following snapshot of a system running n processes. Process i is holding x_i instances of a resource R, $1 \leq i \leq n$. Currently, all instances of R are occupied. Further, for all i, process i has placed a request for an additional y_i instances while holding the x_i instances it already has. There are exactly two processes p and q and such that $Y_p = Y_q = 0$. Which one of the following can serve as a necessary condition to guarantee that the system is not approaching a deadlock?

A. $\min(x_p, x_q) < \max_{k \neq p,q} y_k$
B. $x_p + x_q \geq \min_{k \neq p,q} y_k$
C. $\max(x_p, x_q) > 1$
D. $\min(x_p, x_q) > 1$

gate2006 operating-system resource-allocation normal

Answer

5.26.15 Resource Allocation: GATE2007-57 top

http://gateoverflow.in/1255

A single processor system has three resource types X, Y and Z, which are shared by three processes. There are 5 units of each resource type. Consider the following scenario, where the column **alloc** denotes the number of units of each resource type allocated to each process, and the column **request** denotes the number of units of each resource type requested by a process in order to complete execution. Which of these processes will finish **LAST**?

	alloc			request		
	X	Y	Z	X	Y	Z
P0	1	2	1	1	0	3
P1	2	0	1	0	1	2
P2	2	2	1	1	2	0

A. P0

B. P1
C. P2
D. None of the above, since the system is in a deadlock

gate2007 operating-system resource-allocation normal

Answer

5.26.16 Resource Allocation: GATE2008-65 top http://gateoverflow.in/488

Which of the following is NOT true of deadlock prevention and deadlock avoidance schemes?

A. In deadlock prevention, the request for resources is always granted if the resulting state is safe

B. In deadlock avoidance, the request for resources is always granted if the resulting state is safe

C. Deadlock avoidance is less restrictive than deadlock prevention

D. Deadlock avoidance requires knowledge of resource requirements *apriori..*

gate2008 operating-system easy resource-allocation

Answer

5.26.17 Resource Allocation: GATE2008-IT-54 top http://gateoverflow.in/3364

An operating system implements a policy that requires a process to release all resources before making a request for another resource. Select the TRUE statement from the following:

A. Both starvation and deadlock can occur
B. Starvation can occur but deadlock cannot occur
C. Starvation cannot occur but deadlock can occur
D. Neither starvation nor deadlock can occur

gate2008-it operating-system resource-allocation normal

Answer

5.26.18 Resource Allocation: GATE2009-30 top http://gateoverflow.in/1316

Consider a system with 4 types of resources R1 (3 units), R2 (2 units), R3 (3 units), R4 (2 units). A non-preemptive resource allocation policy is used. At any given instance, a request is not entertained if it cannot be completely satisfied. Three processes P1, P2, P3 request the resources as follows if executed independently.

Process P1:	**Process P2:**	**Process P3:**
t=0: requests 2 units of R2 t=1: requests 1 unit of R3 t=3: requests 2 units of R1 t=5: releases 1 unit of R2 and 1 unit of R1. t=7: releases 1 unit of R3 t=8: requests 2 units of R4 t=10: Finishes	t=0: requests 2 units of R3 t=2: requests 1 unit of R4 t=4: requests 1 unit of R1 t=6: releases 1 unit of R3 t=8: Finishes	t=0: requests 1 unit of R4 t=2: requests 2 units of R1 t=5: releases 2 units of R1 t=7: requests 1 unit of R2 t=8: requests 1 unit of R3 t=9: Finishes

Which one of the following statements is TRUE if all three processes run concurrently starting at time t = 0?

A. All processes will finish without any deadlock

B. Only P1 and P2 will be in deadlock

C. Only P1 and P3 will be in deadlock

D. All three processes will be in deadlock

gate2009 operating-system resource-allocation normal

Answer

5.26.19 Resource Allocation: GATE2010-46 top http://gateoverflow.in/2348

A system has n resources $R_0, \dots, R_{n-1}$, and k processes $P_0, \dots, P_{k-1}$. The implementation of the resource request logic of each process P_i is as follows:

```
if (i%2==0) {
    if (i<n) request R_i;
    if (i+2 < n) request R_i+2
}

else {
    if (i<n) request R_n-i;
    if (i+2 <n) request R_n-i-2;
}
```

In which of the following situations is a deadlock possible?

A. $n = 40,\ k = 26$
B. $n = 21,\ k = 12$
C. $n = 20,\ k = 10$
D. $n = 41,\ k = 19$

gate2010 operating-system resource-allocation normal

Answer

5.26.20 Resource Allocation: GATE2013_16 top http://gateoverflow.in/1438

Three concurrent processes X, Y, and Z execute three different code segments that access and update certain shared variables. Process X executes the P operation (i.e., $wait$) on semaphores a, b and c; process Y executes the P operation on semaphores b, c and d; process Z executes the P operation on semaphores c, d, and a before entering the respective code segments. After completing the execution of its code segment, each process invokes the V operation (i.e., $signal$) on its three semaphores. All semaphores are binary semaphores initialized to one. Which one of the following represents a deadlock-free order of invoking the P operations by the processes?

(A) $X : P(a)P(b)P(c)\ \ Y : P(b)P(c)P(d)\ \ Z : P(c)P(d)P(a)$
(B) $X : P(b)P(a)P(c)\ \ Y : P(b)P(c)P(d)\ \ Z : P(a)P(c)P(d)$
(C) $X : P(b)P(a)P(c)\ \ Y : P(c)P(b)P(d)\ \ Z : P(a)P(c)P(d)$
(D) $X : P(a)P(b)P(c)\ \ Y : P(c)P(b)P(d)\ \ Z : P(c)P(d)P(a)$

gate2013 operating-system resource-allocation normal

Answer

5.26.21 Resource Allocation: GATE2014-1-31 top http://gateoverflow.in/1800

An operating system uses the *Banker's algorithm* for deadlock avoidance when managing the allocation of three resource types X, Y, and Z to three processes P0, P1, and P2. The table given below presents the current system state. Here, the *Allocation matrix* shows the current number of resources of each type allocated to each process and the *Max matrix* shows the maximum number of resources of each type required by each process during its execution.

	Allocation			**Max**		
	X	Y	Z	X	Y	Z
P0	0	0	1	8	4	3
P1	3	2	0	6	2	0
P2	2	1	1	3	3	3

There are 3 units of type X, 2 units of type Y and 2 units of type Z still available. The system is currently in a **safe** state. Consider the following independent requests for additional resources in the current state:

REQ1: P0 requests 0 units of X, 0 units of Y and 2 units of Z

REQ2: P1 requests 2 units of X, 0 units of Y and 0 units of Z

Which one of the following is **TRUE**?

A. Only REQ1 can be permitted.
B. Only REQ2 can be permitted.
C. Both REQ1 and REQ2 can be permitted.
D. Neither REQ1 nor REQ2 can be permitted.

gate2014-1 operating-system resource-allocation normal

Answer

5.26.22 Resource Allocation: GATE2014-3-31 top http://gateoverflow.in/2065

A system contains three programs and each requires three tape units for its operation. The minimum number of tape units which the system must have such that deadlocks never arise is _________.

gate2014-3 operating-system resource-allocation numerical-answers easy

Answer

5.26.23 Resource Allocation: GATE2015-2_23 top http://gateoverflow.in/8114

A system has 6 identical resources and N processes competing for them. Each process can request atmost 2 requests. Which one of the following values of N could lead to a deadlock?

A. 1
B. 2
C. 3
D. 4

gate2015-2 operating-system resource-allocation easy

Answer

5.26.24 Resource Allocation: GATE2015-3_52 top http://gateoverflow.in/8561

Consider the following policies for preventing deadlock in a system with mutually exclusive resources.

I. Process should acquire all their resources at the beginning of execution. If any resource is not available, all resources acquired so far are released.
II. The resources are numbered uniquely, and processes are allowed to request for resources only in increasing resource numbers
III. The resources are numbered uniquely, and processes are allowed to request for resources only in deccreasing resource numbers
IV. The resources are numbered uniquely. A processes is allowed to request for resources only for a resource with resource number larger than its currently held resources

Which of the above policies can be used for preventing deadlock?

A. Any one of I and III but not II or IV
B. Any one of I, III and IV but not II
C. Any one of II and III but not I or IV
D. Any one of I, II, III and IV

gate2015-3 operating-system resource-allocation normal

Answer

5.26.25 Resource Allocation: GATE2017-2-33 top http://gateoverflow.in/118375

A system shares 9 tape drives. The current allocation and maximum requirement of tape drives for that processes are shown below:

Process	Current Allocation	Maximum Requirement
P1	3	7
P2	1	6
P3	3	5

Which of the following best describes current state of the system?

A. Safe, Deadlocked
B. Safe, Not Deadlocked
C. Not Safe, Deadlocked
D. Not Safe, Not Deadlocked

gate2017-2 operating-system resource-allocation

Answer

5.26.26 Resource Allocation: ISI2013-CS-5b top http://gateoverflow.in/47644

A system has 4 processes A, B, C, D and 5 allocatable resources R_1, R_2, R_3, R_4, R_5 . The maximum resource requirement for each process and its current allocation are as follows.

Process	Maximum R_1, R_2, R_3, R_4, R_5	Allocation R_1, R_2, R_3, R_4, R_5
A	1, 1, 2, 1, 3	1, 0, 2, 1, 1
B	2, 2, 2, 1, 0	2, 0, 1, 1, 0
C	2, 1, 3, 1, 0	1, 1, 0, 1, 0
D	1, 1, 2, 2, 1	1, 1, 1, 1, 0

Suppose the currently available count of resources is given by $0, 0, X, 1, 1$. What is the minimum value of X for which this is a safe state? Justify your answer.

descriptive isi2013 operating-system resource-allocation

Answer

Answers: Resource Allocation

5.26.1 Resource Allocation: GATE 2016-1-50 top http://gateoverflow.in/39719

Selected Answer

Answer is A.

```
while (t[j] != 0 && t[j] <=t[i]);
```

This ensures that when a process i reaches Critical Section, all processes j which started before it must have its $t[j] = 0$. This means no two process can be in critical section at same time as one of them must be started earlier.

returns an integer not smaller

is the issue here for deadlock. This means two processes can have same t value and hence

```
while (t[j] != 0 && t[j] <=t[i]);
```

can go to infinite wait. ($t[j] == t[i]$). Starvation is also possible as there is nothing to ensure that a request is granted in a timed manner. But bounded waiting (as defined in Galvin) is guaranteed here as when a process i starts and gets $t[i]$ value, no new process can enter critical section before i (as their t value will be higher) and this ensures that access to critical section is granted only to a finite number of processes (those which started before) before eventually process i gets access.

But in some places bounded waiting is defined as finite waiting (see one here from CMU) and since deadlock is possible here, bounded waiting is not guaranteed as per that definition.

27 votes -- Arjun Suresh (294k points)

Given question is a wrongly modified version of actual bakery algorithm, used for N-process critical section problem.

Bakery algorithm code goes as follows : (as in William stalling book page 209, 7th edition)

```
Entering[i] = true;
Number[i] = 1 + max(Number[1], ..., Number[NUM_THREADS]);
Entering[i] = false;

for (integer j = 1; j <= NUM_THREADS; j++) {
    // Wait until thread j receives its number:
    while (Entering[j]) {
      /* nothing */
    }

    // Wait until all threads with smaller numbers or with the same
    // number, but with higher priority, finish their work:
    while ((Number[j] != 0) && ((Number[j], j) < (Number[i], i))) {
      /* nothing */
    }
}

    <Critical Section>

    Number[i] = 0;
    /*remainder section */
```

code explanation:

The important point here is that due to lack of atomicity of `max` function multiple processes may calculate the same `Number`.

In that situation to choose between two processes, we prioritize the lower `process_id`.

`(Number[j], j) < (Number[i], i))` this is a tuple comparison and it allows us to correctly select only one process out of `i` and `j`.but not both (when `Number[i] = Number[j]`)

Progress and Deadlock:

The testing condition given in the question is `while (t[j] != 0 && t[j] <=t[i]);` which creates deadlock for both `i` and `j` (and possibly more) processes which have calculated their Numbers as the same value. C and D are wrong.

Bounded waiting :

If the process `i` is waiting and looping inside the for loop. Why is it waiting there ? Two reasons,

1. Its number value is not yet the minimum positive value.
2. Or, its Number value is equal to some other's Number value.

Reason1 does not dissatisfy bounded waiting , because if the process `i` has the Number value = 5 then all processes having less positive `Number` will enter CS first and will exit. Then Process `i` will definitely get a chance to enter into CS.

Reason2 dissatisfy bounded waiting because assume process 3 and 4 are fighting with the equal Number value of 5. whenever one of them (say 4) is scheduled by the short term scheduler to the CPU, it goes on looping on $Number[3] \Leftarrow Number[4]$ .Similarly with process 3 also. But when they are removed from the Running state by the scheduler , other processes may continue normal operation. So for process 3 and 4 although they have requested very early, because of their own reason, other processes are getting a chance of entering into CS. B is wrong.

note : in this all the processes go into deadlock anyway after a while.

How mutual exclusion is satisfied ?

Now we assume all processes calculate their Number value as distinct.

And categorize all concurrent N processes into three groups;

1. Processes which are now testing the while condition inside the for loop.
2. Processes which are now in the reminder section.
3. Processes which are now about to calculate its Number values.

In *Category 1,* assume process `i` wins the testing condition, that means no one else can win the test because `i` has the lowest positive value among the 1st category of processes.

Category 3 processes will calculate Number value more than the Number of `i` using `max` the function.

Same goes with *Category 2* processes if they ever try to re-enter.

---

detail of bakery algorithm Link1 and Link2 and Link3_page53

15 votes -- Debashish Deka (51.4k points)

5.26.2 Resource Allocation: GATE1992_02,xi top

http://gateoverflow.in/568

Selected Answer

Answer: A

For n=3, 2-2-2 combination of resources leads to deadlock.

For n=2, 3 - 3 is the maximum need and that can always be satisfied.

13 votes -- Rajarshi Sarkar (35k points)

5.26.3 Resource Allocation: GATE1993-7.9, UGCNET-Dec2012-III-41 top

http://gateoverflow.in/2297

Selected Answer

13 and 15.

Consider the worst scenario: all processes require one more instance of the resource. So, P1 would have got 2, P2 - 3 and P3 - 5. Now, if one more resource is available at least one of the processes could be finished and all resources allotted to it will be free which will lead to other processes also getting freed. So, 2 + 3 + 5 = 10 would be the maximum value of m so that a deadlock can occur.

17 votes -- Arjun Suresh (294k points)

5.26.4 Resource Allocation: GATE1994_28 top

http://gateoverflow.in/2524

Selected Answer

From the RAG we can make the necessary matrices.

Allocation

	R1	R2	R3
P0	1	0	1
P1	1	1	0
P2	0	1	0
P3	0	1	0

Future Need

	R1	R2	R3
P0	0	1	1
P1	1	0	0
P2	0	0	1
P3	1	2	0

Total=(2 3 2)

Allocated=(2 3 1)

Available=Total -Allocated

=(0 0 1)

P2 s need (0 0 1) can be met

And it releases its held resources after running to completion

A=(0 0 1)+(0 1 0)=(0 1 1)

P0 s need (0 1 1) can be met

and it releases

A=(0 1 1)+(1 0 1)=(1 1 2)

P1 needs can be met (1 0 0)

A=(1 1 2)+(1 0 0)=(2 1 2)

P3 s need can be met

so the safe sequence would be P2 P0 P1 P3.

14 votes -- Sourav Roy (3.6k points)

a) The system is not in deadlock state as there exists a safe sequence.

b) P_2 P_0 P_1 P_3 is a safe sequence.

10 votes -- Hunaif (485 points)

5.26.5 Resource Allocation: GATE1996_22 top

http://gateoverflow.in/2774

Selected Answer

Allocation

	R0	R1	R2
P0	1	0	2
P1	0	3	1
P2	1	0	2

MAX NEED

	R0	R1	R2
P0	4	1	2
P1	1	5	1
P2	1	2	3

Future Need

	R0	R1	R2
P0	3	1	0
P1	1	2	0
P2	0	2	1

Available=(2 2 0)

P1(1 2 0) s needs can be met. P1 executes and completes releases its allocated resources.

A=(2 2 0)+(0 3 1)=(2 5 1)

Further P2 (0 2 1) s needs can be met.

A=(2 5 1)+(1 0 2)=(3 5 3)

next P0 s needs can be met.

Thus safe sequence exists P1 P2 P0.

Next Request P0(0 1 0)

Allocation

	R0	R1	R2
P0	1	0+1=1	2
P1	0	3	1
P2	1	0	2

MAX NEED

	R0	R1	R2
P0	4	1	2
P1	1	5	1
P2	1	2	3

Future Need

Future Need

	R0	R1	R2
P0	3	0	0
P1	1	2	0
P2	0	2	1

Available=(2 2-1=1 0)

Here also not a single request need by any process can be made.

a)System is in safe state.

b)Since request of P0 can not be met,system would delay the request and wait till resources are available.

8 votes -- Sourav Roy (3.6k points)

5.26.6 Resource Allocation: GATE1997_6.7 top http://gateoverflow.in/2263

Selected Answer

Answer: C

(a) 1-1-1 allocation of resources can cause a deadlock.

(c) 2-1-1 is the general resource allocation which will never cause a deadlock as the process getting 2 resources will release its resources after its task is over.

12 votes -- Rajarshi Sarkar (35k points)

5.26.7 Resource Allocation: GATE1997_75 top http://gateoverflow.in/19705

Selected Answer

a) Can Deadlock occur. No, because every time Older Process who wants some resources which are already acquired by some younger process. In this condition Younger will be killed and release its resources which is now taken by now older process. So never more than one process will wait for some resources indefinitely. Timestamp will also be unique.

b) Can a process Starve. No, because every time when Younger process is getting killed, it is restarted with same timestamp which he had at time of killing. So it will act as an elder even after killing for all those who came after it..

There is No starvation .. consider this scenario :

say a process p_{12} with TS 12 and another process p_{11} with timestamp 11 so p_{12} gets killed but again come with **same timestamp**. As timestamp is increasing for newly enter process so at next process p_{13} enter with timestamp 13 which have greater timestamp than p_{12} so p_{12} gets executed ..hence there is no starvation possible.

7 votes -- sonu (2.4k points)

5.26.8 Resource Allocation: GATE1998_1.32 top http://gateoverflow.in/1669

Selected Answer

Each process needs 2 drives

Consider this scenario

P1 P2 P3 P4 P5 P6

1 1 1 1 1 1

This is scenario when a deadlock would happen, as each of the process is waiting for 1 more process to run to completion. And there are no more Resources available as max 6 reached. If we could have provided one more R to any of the process, any of the process could have executed to completion, then released its resources, which further when assigned to other and then other would have broken the deadlock situation.

In case of processes, if there are less than 6 processes, then no deadlock occurs.

Consider the maximum case of 5 processes.

P1 P2 P3 P4 P5

1 1 1 1 1

In this case system has 6 resources max,and hence we still have 1 more R left which can be given to any of the processes, which in turn runs to completion, releases its resources and in turn others can run to completion too.

Ans b) 5

14 votes -- Sourav Roy (3.6k points)

5.26.9 Resource Allocation: GATE2000-2.23 top http://gateoverflow.in/670

Selected Answer

The answer is C.

A is valid. Which dissatisfies Hold and Wait but ends up in starvation.
B is valid. Which is used to dissatisfy circular wait.
C is invalid.
D is valid and is used to dissatisfy Hold and Wait.

19 votes -- Gate Keeda (19.1k points)

5.26.10 Resource Allocation: GATE2001-19 top http://gateoverflow.in/760

Selected Answer

in question program for P2 should be like this:

Program for P2:

Q1: While R1 is busy do no-op
Q2: Set R1 $\leftarrow$ busy
Q3: While (R2 is busy) do no-op;
Q4: Set R2 $\leftarrow$ busy
Q5: Use R1 and R2
Q6: Set R2 $\leftarrow$ free

Q7: Set R2 $\leftarrow$ free

a) Mutual exclusion is not guranteed;

initially both R1=free and R2=free

now cosider the scenario,

P1 will start and check the condition (R1==busy) it will be evaluated as false and P1 will be preempted

then P2 will start and check the condition (R1==busy) it will be evaluated as false and P2 will be preempted

now again P1 will start execution and set R1=busy then preempted again

then P2 will start execution and set R1=busy which was already updated by P1 and now p2 will be preempted

after that P1 will start execution and same scenario happen again with both P1 and P2

both set R2=busy and enter into critical section together.

hence Mutual exclusion is not guranteed.

b)

here deadlock is not possible, because atleast one process is able to proceed and enter into critical section.

c)

if Q1 and Q3 ; Q2 and Q4 will be interchanged then Mutual exclusion is guranteed but deadlock is possible.

here, both process will not be able to enter critical section together.

for deadlock:

if P1 sets R1=busy and then preempted, and P2 sets R2=busy then preempted...

in this scenario no process can proceed further, as both holding the resource that is required by other to enter into CS.

hence deadlock will be there.

10 votes -- jayendra (8.1k points)

5.26.11 Resource Allocation: GATE2004-IT-63 top

http://gateoverflow.in/3706

Selected Answer

Answer is (A)

When the process wakes up again after it has been killed once or twice IT WILL HAVE SAME TIME-STAMP as it had WHEN IT WAS KILLED FIRST TIME. And that time stamp can never be greater than a process that was killed after that or a NEW process that may have arrived.

So every time when the killed process wakes up it MIGHT ALWAYS find a new process that will say "your time stamp is less than me and I take this resource", which of course is as we know, and that process will again be killed.

This may happen indefinitely if processes keep coming and killing that "INNOCENT" process every time it try to access.

So **STARVATION is possible. Deadlock is not possible.**

19 votes -- Sandeep_Uniyal (7.3k points)

5.26.12 Resource Allocation: GATE2005-71 top

http://gateoverflow.in/1394

Selected Answer

to ensure deadlock never happens allocate resource to each process in following manner..
allocation will be (max requirement -1) i.e. S_i-1 for each i..
now $\sum(S_i - 1) + 1$(to prevent deadlock) <= m(available resources)
$\sum S_i - \sum 1 + 1 <= m$
$\sum S_i - n + 1 <= m$

$\sum S_i + 1 <= m + n$
$\sum S_i < m + n$

34 votes -- Digvijay (47k points)

5.26.13 Resource Allocation: GATE2005-IT-62 top http://gateoverflow.in/3823

Selected Answer

The answer is (c)

If R_1 and R_2 are allocated to the Process P1 , then it will complete it's job and release it . After that process P_2 will get both the resources and complete it's Job .

16 votes -- zabiullah shiekh (173 points)

5.26.14 Resource Allocation: GATE2006-66 top http://gateoverflow.in/1844

Selected Answer

B. $x_p + x_q \geq \min_{k \neq p,q} y_k$

The question asks for "necessary" condition to guarantee no deadlock. i.e., without satisfying this condition "no deadlock" is not possible.

Both the processes p and q have no additional requirements and can be finished releasing $x_p + x_q$ resources. Using this we can finish one more process only if condition B is satisfied.

PS: Condition B just ensures that the system can proceed from the current state. it does not guarantee that there won't be a deadlock before all processes are finished.

20 votes -- Arjun Suresh (294k points)

5.26.15 Resource Allocation: GATE2007-57 top http://gateoverflow.in/1255

Selected Answer

The answer is C.

Available Resources

X	Y	Z
0	1	2

Now, P1 will execute first, As it meets the needs.

After completion, The available resources are updated.

Updated Available Resources

X	Y	Z
2	1	3

Now P0 will complete the execution, as it meets the needs.

After completion of P0 the table is updated and then P2 completes the execution.

Thus P2 completes the execution in the last.

12 votes -- Gate Keeda (19.1k points)

5.26.16 Resource Allocation: GATE2008-65 top http://gateoverflow.in/488

Selected Answer

A. In deadlock prevention, we just need to ensure one of the four necessary conditions of deadlock doesn't occur. So, it may be the case that a resource request might be rejected even if the resulting state is safe. (One example, is when we impose a strict ordering for the processes to request resources).

Deadlock avoidance is less restrictive than deadlock prevention. Deadlock avoidance is like a police man and deadlock prevention is like a traffic light. The former is less restrictive and allows more concurrency.

Ref: http://www.cs.jhu.edu/~yairamir/cs418/os4/tsld010.htm

22 votes -- Arjun Suresh (294k points)

Option **A** is answer.
The main difference between deadlock prevention and deadlock avoidance lies in the definition of deadlock itself.
We know Necessary_conditions for deadlock to happen. Means deadlock can be there only if these conditions are satisfied.
But it does not mean that if these conditions are satisfied then deadlock will always be there.

The above definition is the main idea and fine line on that both strategies differ.

Deadlock Prevention says: Let's prevents one of the conditions.
Deadlock Avoidance says: Let me allow all conditions to hold simultaneously (all conditions holds simultaneously doesn't guarantee deadlock) but I will also check any chance of deadlock (i.e system in the safe state if I allocate requested resource.), It allows the four conditions but makes judicious decisions so that the deadlock point is not potentially reached.

Clearly, Deadlock prevention is more restrictive. It decreases throughput also. At the same time we can not use Deadlock avoidance practically as it demands to know uses of all resources in advance.

The analogy is like this:
(Now take an example of protection from viral through the water.)
Deadlock Prevention: Don't use water
Deadlock Avoidance: Use water but first filter out.

14 votes -- Sachin Mittal (7.1k points)

5.26.17 Resource Allocation: GATE2008-IT-54 top http://gateoverflow.in/3364

Selected Answer

Answer: B

Starvation can occur as each time a process requests a resource it has to release all its resources. Now, maybe the process has not used the resources properly yet. This will happen again when the process requests another resource. So, the process starves for proper utilisation of resources.

Deadlock will not occur as it is similar to a deadlock prevention scheme.

14 votes -- Rajarshi Sarkar (35k points)

5.26.18 Resource Allocation: GATE2009-30 top http://gateoverflow.in/1316

Selected Answer

At t = 3, the process P1 has to wait because available R1=1, but P1 needs 2 R1. so P1 is blocked.

similarly, at various times what is happening can be analyzed with table below.

		R1(3)	R2(2)	R3(3)	R4(2)
	t=0	3	0	1	1

	t=1	3	0	0	1
	t=2	1	0	0	0
block P1	t=3	1	0	0	0
	t=4	0	0	0	0
UB P1	t=5	1	1	0	0
	t=6	1	1	1	0
	t=7	1	0	2	0
B P1	t=8	2	0	2	1
UB P1	t=9	2	1	3	0
	t=10				

there are no process in deadlock, hence **A is right choice** :)

14 votes -- Sachin Mittal (7.1k points)

5.26.19 Resource Allocation: GATE2010-46 top

http://gateoverflow.in/2348

Selected Answer

From the resource allocation logic, it's clear that even numbered processes are taking even numbered resources and all even numbered processes share no more than 1 resource. Now, if we make sure that all odd numbered processes take odd numbered resources without a cycle, then deadlock cannot occur. The "else" case of the resource allocation logic, is trying to do that. But, if n is odd, R_{n-i} and R_{n-i-2} will be even and there is possibility of deadlock, when two processes requests the same R_i and R_j. So, only B and D are the possible answers.

Now, in D, we can see that P_0 requests R_0 and R_2, P_2 requests R_2 and R_4, so on until, P_{18} requests R_{18} and R_{20}. At the same time P_1 requests R_{40} and R_{38}, P_3 requests R_{38} and R_{36}, so on until, P_{17} requests R_{24} and R_{22}. i.e.; there are no two processes requesting the same two resources and hence there can't be a cycle of dependencies which means, no deadlock is possible.

But for B, P_8 requests R_8 and R_{10} and P_{11} also requests R_{10} and R_8. Hence, a deadlock is possible. (Suppose P_8 comes first and occupies R_8. Then P_{11} comes and occupies R_{10}. Now, if P_8 requests R_{10} and P_{11} requests R_8, there will be deadlock)

66 votes -- Arjun Suresh (294k points)

5.26.20 Resource Allocation: GATE2013_16 top http://gateoverflow.in/1438

Selected Answer

For deadlock-free invocation, X, Y and Z must access the semaphores in the same order so that there won't be a case where one process is waiting for a semaphore while holding some other semaphore. This is satisfied only by option B.

In option A, X can hold a and wait for c while Z can hold c and wait for a
In option C, X can hold b and wait for c, while Y can hold c and wait for b
In option D, X can hold a and wait for c while Z can hold c and wait for a

So, a deadlock is possible for all choices except B.

http://www.eee.metu.edu.tr/~halici/courses/442/Ch5%20Deadlocks.pdf

18 votes -- Arjun Suresh (294k points)

5.26.21 Resource Allocation: GATE2014-1-31 top http://gateoverflow.in/1800

Selected Answer

This is the current safe state.

AVAILABLEX=3, Y=2, Z=2

	MAX	ALLOCATION
	X Y Z	X Y Z
P0	8 4 3	0 0 1
P1	6 2 0	3 2 0
P2	3 3 3	2 1 1

Now, if the request REQ1 is permitted, the state would become :

AVAILABLEX=3, Y=2, Z=0

	MAX	ALLOCATION	NEED
	X Y Z	X Y Z	X Y Z
P0	8 4 3	0 0 3	8 4 0
P1	6 2 0	3 2 0	3 0 0
P2	3 3 3	2 1 1	1 2 2

Now, with the current availability, we can service the need of P1. The state would become :

AVAILABLEX=6, Y=4, Z=0

	MAX	ALLOCATION	NEED
	X Y Z	X Y Z	X Y Z
P0	8 4 3	0 0 3	8 4 0
P1	6 2 0	3 2 0	0 0 0
P2	3 3 3	2 1 1	1 2 2

With the resulting availability, it would not be possible to service the need of either P0 or P2, owing to lack of Z resource. Therefore, the system would be in a deadlock. ⇒ We cannot permit REQ1. Now, at the given safe state, if we accept REQ2 :

AVAILABLEX=1, Y=2, Z=2

MAX ALLOCATION NEED

	MAX X Y Z	ALLOCATION X Y Z	NEED X Y Z
P0	8 4 3	0 0 1	8 4 2
P1	6 2 0	5 2 0	1 0 0
P2	3 3 3	2 1 1	1 2 2

With this availability, we service P1 (P2 can also be serviced). So, the state is :

AVAILABLE X=7, Y=4, Z=2

	MAX X Y Z	ALLOCATION X Y Z	NEED X Y Z
P0	8 4 3	0 0 1	8 4 2
P1	6 2 0	5 2 0	0 0 0
P2	3 3 3	2 1 1	1 2 2

With the current availability, we service P2. The state becomes :

AVAILABLE X=10, Y=7, Z=5

	MAX X Y Z	ALLOCATION X Y Z	NEED X Y Z
P0	8 4 3	0 0 1	8 4 2
P1	6 2 0	5 2 0	0 0 0
P2	3 3 3	2 1 1	0 0 0

Finally, we service P0. The state now becomes :

AVAILABLE X=18, Y=11, Z=8

	MAX X Y Z	ALLOCATION X Y Z	NEED X Y Z
P0	8 4 3	0 0 1	0 0 0
P1	6 2 0	5 2 0	0 0 0
P2	3 3 3	2 1 1	0 0 0

The state so obtained is a safe state. ⇒ REQ2 can be permitted. So, only REQ2 can be permitted. Hence, B is the correct choice.

1 votes -- Divya Bharti (4k points)

Option B

Request 1 if permitted does not lead to a safe state.

After allowing Req 1,

Allocated : Max : Requirement :

P0 0 0 3 8 4 3 8 4 0

P1 3 2 0 6 2 0 3 0 0

P2 2 1 1 3 3 3 1 2 2

Available : X=3 Y=2 Z=0

Now we can satisfy P1's requirement completely. So Availabe becomes : X=6,Y=4,Z=0.

Since Z is not available now, neither P0 nor P2's requirement can be satisfied. So its an unsafe state.

17 votes -- Poulami Das (117 points)

5.26.22 Resource Allocation: GATE2014-3-31 top

http://gateoverflow.in/2065

Selected Answer

for this types of problems in which every process is making same number of request,use the formula n.(m-1)+1<=r

where n=no. of processes

m=resource request made by processes

r=no. of resources

so above problem can be solved as 3.(3-1)+1<=r i.e. 7<=r

min number of resource required are 7

14 votes -- neha pawar (4.4k points)

5.26.23 Resource Allocation: GATE2015-2_23 top http://gateoverflow.in/8114

Selected Answer

3 * 2 = 6

4 * 2 = 8.

I guess a question can't get easier than this- D choice. (Also, we can simply take the greatest value among choice for this question)

[There are 6 resources and all of them must be in use for deadlock. If the system has no other resource dependence, N=4 cannot lead to a deadlock. But if N=4, the system can be in deadlock in presence of other dependencies.

Why N=3 cannot cause deadlock? It can cause deadlock, only if the system is already in deadlock and so the deadlock is independent of the considered resource. Till N=3, all requests for considered resource will always be satisfied and hence there won't be a waiting and hence no deadlock with respect to the considered resource.]

11 votes -- Arjun Suresh (294k points)

5.26.24 Resource Allocation: GATE2015-3_52 top http://gateoverflow.in/8561

Selected Answer

a deadlock will not occur if any one of the below four conditions are prevented :

1> hold and wait

2> mutual exclusion

3> circular weight

4> no-premption

now

option-1 if implemented violates 1 so deadlock cannot occur.

option-2 if implemented violates circular wait(making the dependency graph acyclic)

option-3 if implemented violates circular wait(making the dependency graph acyclic)

option-4 it is equivalent to the other options 2 and 3

so the correct option is 4 as all of them are methods to avoid deadlock.

http://www.cs.uic.edu/~jbell/CourseNotes/OperatingSystems/7_Deadlocks.html

24 votes -- Tamojit Chatterjee (2.2k points)

5.26.25 Resource Allocation: GATE2017-2-33 top http://gateoverflow.in/118375

Selected Answer

Process	*Current Allocation*	*Max Requirements*	*Need*
P1	3	7	4
P2	1	6	5
P3	3	5	2

Given there are total 9 tape drives,

so according to the above table we can see we have currently allocated (7 tape drive),So**currently Available tape drive=2**

So,P3 can use it and after using it will relase it 3 resources **New Available=5**

then P1 can use it and will relase it 3 resources so **New Available=8**

and lastly P2 so all the process are in **SAFE STATE** and there will be **NO DEADLOCK**

Safe Sequence will be ***P3->P2->P1*, or *P3->P1->P2.***

Answer will be B only.

14 votes -- Abhishek Mitra (313 points)

5.26.26 Resource Allocation: ISI2013-CS-5b top

http://gateoverflow.in/47644

Min value of X whatever system couldnot be in safe state

Here we know Maximum available resources and current allocation

We have to figure out Need Matrix to find safe state

	R1	R2	R3	R4	R5
P1	0	1	0	0	2
P2	0	2	1	0	0
P3	1	0	3	0	0
P4	0	0	1	1	1

Now we think with X=1 P_4 could be executed

and after executing P_4 releases (1,1,1,1,0)

Now available resource **(1, 1, 2, 2, 1)**

which couldnot fulfill resource requirement of P_1,P_2,P_3

for that we need X=2

Now P_3 executed and released its resources (1,1,0,1,0)

Now available resources **(2,2,3,3,1)**

With this P_2 could executed and release (2,0,1,1,0)

Now available resources **(4,2,4,4,1)**

But with this P_1 cannot be executed as, P_1 need (0,1,0,0,2)

So, the Process cannot be in safe state

5 votes -- srestha (58.4k points)

5.27 Runtime Environments(2) top

5.27.1 Runtime Environments: GATE1991-02,iii top http://gateoverflow.in/513

Match the pairs in the following questions by writing the corresponding letters only.

(a)	Buddy system	(p)	Run time type specification
(b)	Interpretation	(q)	Segmentation
(c)	Pointer type	(r)	Memory allocation
(d)	Virtual memory	(s)	Garbage collection

gate1991 operating-system normal match-the-following runtime-environments

Answer

5.27.2 Runtime Environments: GATE1996_2.17 top http://gateoverflow.in/2746

The correct matching for the following pairs is

(A) Activation record	(1) Linking loader
(B) Location counter	(2) Garbage collection
(C) Reference counts	(3) Subroutine call
(D) Address relocation	(4) Assembler

A. A-3 B-4 C-1 D-2
B. A-4 B-3 C-1 D-2
C. A-4 B-3 C-2 D-1
D. A-3 B-4 C-2 D-1

gate1996 operating-system easy runtime-environments

Answer

Answers: Runtime Environments

5.27.1 Runtime Environments: GATE1991-02,iii top http://gateoverflow.in/513

Selected Answer

A-R

B-P

C-S

D-Q

11 votes -- Gate Keeda (19.1k points)

5.27.2 Runtime Environments: GATE1996_2.17 top http://gateoverflow.in/2746

Selected Answer

ans is d

4 votes -- neha pawar (4.4k points)

5.28 Semaphore(7) top

5.28.1 Semaphore: GATE 2016-2-49 top

http://gateoverflow.in/39576

Consider a non-negative counting semaphore S. The operation $P(S)$ decrements S, and $V(S)$ increments S. During an execution, 20 $P(S)$ operations and 12 $V(S)$ operations are issued in some order. The largest initial value of S for which at least one $P(S)$ operation will remain blocked is ________

gate2016-2 operating-system semaphore normal numerical-answers

Answer

5.28.2 Semaphore: GATE1990-1-vii top

http://gateoverflow.in/83851

Fill in the blanks:

Semaphore operations are atomic because they are implemented within the OS __________.

gate1990 operating-system semaphore process-synchronization

Answer

5.28.3 Semaphore: GATE1992-02,x, ISRO2015-35 top

http://gateoverflow.in/564

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

At a particular time of computation the value of a counting semaphore is 7. Then
20
P operations and
15
V operations were completed on this semaphore. The resulting value of the semaphore is :

A. 42
B. 2
C. 7
D. 12

gate1992 operating-system semaphore easy isro2015

Answer

5.28.4 Semaphore: GATE1998_1.31 top

http://gateoverflow.in/1668

A counting semaphore was initialized to 10. Then $6P$ (wait) operations and $4V$ (signal) operations were completed on this semaphore. The resulting value of the semaphore is

A. 0
B. 8
C. 10
D. 12

gate1998 operating-system process-synchronization semaphore easy

Answer

5.28.5 Semaphore: GATE2006-IT-57 top

http://gateoverflow.in/3601

The wait and signal operations of a monitor are implemented using semaphores as follows. In the following,

- x is a condition variable,
- mutex is a semaphore initialized to 1,
- x_sem is a semaphore initialized to 0,
- x_count is the number of processes waiting on semaphore x_sem, initially 0,
- next is a semaphore initialized to 0,
- next_count is the number of processes waiting on semaphore next, initially 0.

The body of each procedure that is visible outside the monitor is replaced with the following:

```
P(mutex);
...
body of procedure
...
if (next_count > 0)
    V(next);
else
    V(mutex);
```

Each occurrence of x.wait is replaced with the following:

```
x_count = x_count + 1;
if (next_count > 0)
    V(next);
else
    V(mutex);
------------------------------------------------------------ E1;
x_count = x_count - 1;
```

Each occurrence of x.signal is replaced with the following:

```
if (x_count > 0)
{
    next_count = next_count + 1;
    ------------------- E2;
    P(next);
    next_count = next_count - 1;
}
```

For correct implementation of the monitor, statements E1 and E2 are, respectively,

A. P(x_sem), V(next)
B. V(next), P(x_sem)
C. P(next), V(x_sem)
D. P(x_sem), V(x_sem)

gate2006-it operating-system process-synchronization semaphore normal

Answer

5.28.6 Semaphore: GATE2008-63 top

http://gateoverflow.in/486

The P and V operations on counting semaphores, where s is a counting semaphore, are defined as follows:

$P(s):$ $s = s - 1;$
If $s < 0$ then wait;

$V(s):$ $s = s + 1;$
If $s <= 0$ then wake up process waiting on s;

Assume that P_b and V_b the wait and signal operations on binary semaphores are provided. Two binary semaphores x_b and y_b are used to implement the semaphore operations $P(s)$ and $V(s)$ as follows:

$P(s): P_b(x_b);\ s = s - 1;\ \text{if } (s < 0)\ \{V_b(x_b);\ P_b(y_b);\ \}\ \text{else } V_b(x_b);$

$V(s): P_b(x_b);\ s = s + 1;\ \text{if } (s <= 0)\ V_b(y_b);\ V_b(x_b);$

The initial values of x_b and y_b are respectively

A. 0 and 0
B. 0 and 1
C. 1 and 0
D. 1 and 1

gate2008 operating-system normal semaphore

Answer

5.28.7 Semaphore: TIFR2012-B-10 top

http://gateoverflow.in/25110

Consider the blocked-set semaphore where the signaling process awakens any one of the suspended process; i.e.,

Wait (S): If $S > 0$ then $S \leftarrow S - 1$, else suspend the execution of this process.

Signal (S): If there are processes that have been suspended on semaphore S, then wake any one of them, else $S \leftarrow S + 1$

Consider the following solution of mutual exclusion problem using blocked-set semaphores.

```
s := 1;
cobegin
P(1)   ||    P(2)     ||     .....    ||      P(N)
coend
```

Where the task body P(i) is

```
begin
while true do
begin
 < non critical section >
 Wait (S)
<critical section>
 Signal (S)
end
end
```

Here N is the number of concurrent processors. Which of the following is true?

a. The program fails to achieve mutual exclusion of critical regions.
b. The program achieves mutual exclusion, but starvation freedom is ensured only for $N \leq 2$
c. The program does not ensure mutual exclusion if $N \geq 3$
d. The program achieves mutual exclusion, but allows starvation for any $N \geq 2$
e. The program achieves mutual exclusion and starvation freedom for any $N \geq 1$

tifr2012 operating-system process-synchronization semaphore

Answer

Answers: Semaphore

5.28.1 Semaphore: GATE 2016-2-49 top

http://gateoverflow.in/39576

Selected Answer

Ans : (7). Take any sequence of 20P and 12V operations, atleast one process will always remain blocked.

14 votes

-- Ashish Deshmukh (1.5k points)

5.28.2 Semaphore: GATE1990-1-vii top

http://gateoverflow.in/83851

The concept of semaphores is used for synchronization.
Semaphore is an integer with a difference. Well, actually a few differences.
You set the value of the integer when you create it, but can never access the value directly after that; you must use one of the semaphore functions to adjust it, and you cannot ask for the current value.
There are semaphore functions to increment or decrement the value of the integer by one.

Decrementing is a (possibly) blocking function. If the resulting semaphore value is negative, the calling thread or process is blocked, and cannot continue until some other thread or process increments it.
Incrementing the semaphore when it is negative causes one (and only one) of the threads blocked by this semaphore to become unblocked and runnable.
Therefore all semaphore operations are atomic. Implemented in kernel

2 votes -- Neeraj7375 (769 points)

5.28.3 Semaphore: GATE1992-02,x, ISRO2015-35 top

http://gateoverflow.in/564

Selected Answer

Ans=option B

currently semaphore is 7 so after 20 P(wait) operation it will come to -12 then for 15 V(signal) operation the value comes to 2.

16 votes -- sanjeev_zerocode (409 points)

5.28.4 Semaphore: GATE1998_1.31 top

http://gateoverflow.in/1668

Selected Answer

answer is option (b)

Initially semaphore is 10 , then 6 down operations are performed means (10-6=4) and 4 up operations means (4+4=8)

so , at last option(b) 8 is correct.

12 votes -- Kalpna Bhargav (3.2k points)

5.28.5 Semaphore: GATE2006-IT-57 top

http://gateoverflow.in/3601

Selected Answer

- x_count is the number of processes waiting on semaphore x_sem, initially 0,

x_count is incremented and decremented in x.wait, which shows that in between them wait(x_sem) must happen which is P(x_sem). Correspondingly V(x_sem) must happen in x.signal. So, D choice.

What is a monitor?

5 votes -- Arjun Suresh (294k points)

5.28.6 Semaphore: GATE2008-63 top

http://gateoverflow.in/486

Selected Answer

Answer is (C) .

Reasoning :-

First let me explain what is counting semaphore & How it works. Counting semaphore gives count, i.e. no of processes that can be in Critical section at same time. Here value of S denotes that count. So suppose S = 3, we need to be able to have 3 processes in Critical section at max. Also when counting semaphore S has negative value we need to have Absolute value of S as no of processes waiting for critical section.

A & B are out of option, because Xb must be 1, otherwise our counting semaphore will get blocked without doing anything. Now consider options C & D.

Option D :-

Yb = 1, Xb = 1

Assume that initial value of S = 2. (At max 2 processes must be in Critical Section.)

We have 4 processes, P1, P2, P3 & P4.

P1 enters critical section , It calls P(s) , S = S - 1 = 1. As S > 1, we do not call Pb(Yb).

P2 enters critical section , It calls P(s) , S = S - 1 = 0. As S >0 we do not call Pb(Yb).

Now P3 comes, it should be blocked but when it calls P(s) , S = S - 1 = 0-1 = -1 As S < 0 ,Now we do call Pb(Yb). Still P3 enters into critical section & We do not get blocked as Yb's Initial value was 1.

This violates property of counting semaphore. S is now -1, & No process is waiting. Also we are allowing 1 more process than what counting semaphore permits.

If Yb would have been 0, P3 would have been blocked here & So Answer is (C).

35 votes -- Akash (43.8k points)

5.28.7 Semaphore: TIFR2012-B-10 top http://gateoverflow.in/25110

I think answer would be option D
since at one time only one process can enter the critical section.
If P1 keep on entering the critical section P2 never get the chance to enter the critical section so starvation can occur for any n>2

4 votes -- Umang Raman (15.2k points)

5.29 System Calls(1) top

5.29.1 System Calls: GATE1999-1.11, UGCNET-Dec2015-II-44 top http://gateoverflow.in/1464

System calls are usually invoked by using

A. a software interrupt
B. polling
C. an indirect jump
D. a privileged instruction

gate1999 operating-system normal ugcnetdec2015ii system-calls

Answer

Answers: System Calls

5.29.1 System Calls: GATE1999-1.11, UGCNET-Dec2015-II-44 top http://gateoverflow.in/1464

Selected Answer

Software interrupt is the answer.

Privileged instruction cannot be the answer as system call is done from user mode and privileged instruction cannot be done from user mode.

14 votes -- Arjun Suresh (294k points)

Ans) A Software interrupt

https://en.wikipedia.org/wiki/System_call#Typical_implementations

12 votes -- Prasanna Ranganathan (4.3k points)

5.30 Threads(7) top

5.30.1 Threads: GATE2004-11 top http://gateoverflow.in/1008

Consider the following statements with respect to user-level threads and kernel-supported threads

I. context switch is faster with kernel-supported threads

II. for user-level threads, a system call can block the entire process

III. Kernel supported threads can be scheduled independently

IV. User level threads are transparent to the kernel

Which of the above statements are true?

A. II, III and IV only
B. II and III only
C. I and III only
D. I and II only

gate2004 operating-system threads normal

Answer

5.30.2 Threads: GATE2004-IT-14 top http://gateoverflow.in/3655

Which one of the following is NOT shared by the threads of the same process ?

A. Stack
B. Address Space
C. File Descriptor Table
D. Message Queue

gate2004-it operating-system easy threads

Answer

5.30.3 Threads: GATE2007-17 top http://gateoverflow.in/1215

Consider the following statements about user level threads and kernel level threads. Which one of the following statements is FALSE?

A. Context switch time is longer for kernel level threads than for user level threads.

B. User level threads do not need any hardware support.

C. Related kernel level threads can be scheduled on different processors in a multi-processor system.

D. Blocking one kernel level thread blocks all related threads.

gate2007 operating-system threads normal

Answer

5.30.4 Threads: GATE2011-16, UGCNET-June2013-III-65 top http://gateoverflow.in/2118

A thread is usually defined as a light weight process because an Operating System (OS) maintains smaller data structure for a thread than for a process. In relation to this, which of the following statement is correct?

A. OS maintains only scheduling and accounting information for each thread
B. OS maintains only CPU registers for each thread
C. OS does not maintain virtual memory state for each thread
D. OS does not maintain a separate stack for each thread

gate2011 operating-system threads normal ugcnetjune2013iii

Answer

5.30.5 Threads: GATE2014-1-20 top http://gateoverflow.in/1787

Which one of the following is **FALSE**?

A. User level threads are not scheduled by the kernel.
B. When a user level thread is blocked, all other threads of its process are blocked.
C. Context switching between user level threads is faster than context switching between kernel level threads.
D. Kernel level threads cannot share the code segment.

gate2014-1 operating-system threads normal

Answer

5.30.6 Threads: GATE2017-1-18 top http://gateoverflow.in/118298

Threads of a process share

(A) global variables but not heap.

(B) heap but not global variables.

(C) neither global variables nor heap.

(D) both heap and global variables.

gate2017-1 operating-system threads

Answer

5.30.7 Threads: GATE2017-2-07 top http://gateoverflow.in/118240

Which of the following is/are shared by all the threads in a process?

I. Program counter
II. Stack
III. Address space
IV. Registers

A. I and II only
B. III only
C. IV only
D. III and IV only

gate2017-2 operating-system threads

Answer

Answers: Threads

5.30.1 Threads: GATE2004-11 top http://gateoverflow.in/1008

Selected Answer

Answer A

I) User level thread switching is faster than kernel level switching. SO I is false.

II) & III) is true.

IV) User level threads are transparent to the kernel

This is little confusing .if you search define transparent on google, you get definations like "(of a material or article) allowing light to pass through so that objects behind can be distinctly seen."->"transparent blue water"", "

easy to perceive or detect."->"the residents will see through any transparent attempt to buy their votes"

This makes it all confusing .Though if go & check more defination

Computing
(of a process or interface) functioning without the user being aware of its presence. So in case of Computing transparent means functioning without being aware. In our case user level threads are functioning without kernel being aware about them. So IV is actually correct. (Even though other defination of transparent disagree to it !)

22 votes -- Akash (43.8k points)

User level threads can switch almost as fast as a procedure call. Kernel supported threads switch much slower. So, I is false.

II, III and IV are TRUE. So A.

"The kernel knows nothing about user-level threads and manages them as if they were single-threaded processes"

Ref: http://stackoverflow.com/questions/15983872/difference-between-user-level-and-kernel-supported-threads

18 votes -- Arjun Suresh (294k points)

5.30.2 Threads: GATE2004-IT-14 top http://gateoverflow.in/3655

Selected Answer

Stack is not shared

15 votes -- Sankaranarayanan P.N (11.2k points)

5.30.3 Threads: GATE2007-17 top http://gateoverflow.in/1215

Selected Answer

Ans -> D

1. Context switch time is longer for kernel level threads than for user level threads. -> This is True, as Kernel level threads are managed by OS and Kernel maintains lot of data structures. There are many overheads involved in Kernel level thread management, which are not present in User level thread management !
2. User level threads do not need any hardware support.-> This is true, as User level threads are implemented by Libraries programmably, Kernel does not sees them.
3. Related kernel level threads can be scheduled on different processors in a multi-processor system.-> This is true.
4. Blocking one kernel level thread blocks all related threads. -> This is false. If it had been user Level threads this would have been true, (In One to one, or many to one model !) Kernel level threads are independent.
5.

18 votes -- Akash (43.8k points)

5.30.4 Threads: GATE2011-16, UGCNET-June2013-III-65 top http://gateoverflow.in/2118

Selected Answer

Answer to this question is (C).

Many of you would not agree at first So here I explain it how.

OS , on per thread basis, maintains ONLY TWO things : CPU Register state and Stack space. It does not maintain anything else for individual thread. Code segment and Global variables are shared. Even TLB and Page Tables are also shared since they belong to same process.

(A) option (A) would have been correct if 'ONLY' word were not there. It NOT only maintains register state BUT stack space also.

(B) option B is obviously FALSE

(C) C is TRUE as it says that OS does not maintain VIRTUAL Memory state for individual thread which isTRUE

(D) This is also FALSE.

35 votes -- Sandeep_Uniyal (7.3k points)

5.30.5 Threads: GATE2014-1-20 top http://gateoverflow.in/1787

Selected Answer

(D) is the answer. Threads can share the Code segments. They have only separate Registers and stack.

User level threads are scheduled by the thread library and kernel knows nothing about it. So, A is TRUE.

When a user level thread is blocked, all other threads of its process are blocked. So, B is TRUE. (With a multi-threaded kernel, user level threads can make non-blocking system calls without getting blocked. But in this option, it is explicitly said 'a thread is blocked'.)

Context switching between user level threads is faster as they actually have no context-switch- nothing is saved and restored while for kernel level thread, Registers, PC and SP must be saved and restored. So, C also TRUE.

Ref: http://www.cs.cornell.edu/courses/cs4410/2008fa/homework/hw1_soln.pdf

13 votes -- Sandeep_Uniyal (7.3k points)

5.30.6 Threads: GATE2017-1-18 top http://gateoverflow.in/118298

Selected Answer

A thread shares with other threads a process’s (to which it belongs to) :

- Code section
- Data section (static + heap)
- Address Space
- Permissions
- Other resources (e.g. files)

Therefore, D is the answer.

7 votes -- Kantikumar (3.5k points)

5.30.7 Threads: GATE2017-2-07 top http://gateoverflow.in/118240

Selected Answer

thread is light weight process, and every thread have its own, stack , register, and PC(one of the register in CPU contain address of next instruction to be executed), so only address space that is shared by all thread for a single process.
so option B is correct ans.

8 votes -- 2018 (5.2k points)

5.31 User Modes(1) top

5.31.1 User Modes: GATE2005-IT-19, UGCNET-June2012-III-57 top http://gateoverflow.in/3764

A user level process in Unix traps the signal sent on a Ctrl-C input, and has a signal handling routine that saves appropriate files before terminating the process. When a Ctrl-C input is given to this process, what is the mode in which the signal handling routine executes?

A. User mode
B. Kernel mode
C. Superuser mode

D. Privileged mode

gate2005-it operating-system user-modes normal ugcnetjune2012iii

Answer

Answers: User Modes

5.31.1 User Modes: GATE2005-IT-19, UGCNET-June2012-III-57 top

http://gateoverflow.in/3764

Selected Answer

- When an user send an input to the process it can not be in privileged mode as it is coming from an user so option D , Privileged mode can not be possible here ..

Now see , kernel mode = Privileged mode

- That means both option B and option D are equal. As option D can not be possible , option B also false.
- There is nothing called superuser mode so option C is clearly wrong .
- Only option A is left , when an user input come like ' ctrl+c' the signal handling routine **executes in user mode only** as **a user level** process in UNIX traps the signal.

Hence option A is correct answer.

4 votes -- Bikram (44.7k points)

5.32 Virtual Memory(37) top

5.32.1 Virtual Memory: GATE 2016-1-47 top

http://gateoverflow.in/39690

Consider a computer system with 40-bit virtual addressing and page size of sixteen kilobytes. If the computer system has a one-level page table per process and each page table entry requires 48 bits, then the size of the per-process page table is __________ megabytes.

gate2016-1 operating-system virtual-memory easy numerical-answers

Answer

5.32.2 Virtual Memory: GATE1989-2-iv top

http://gateoverflow.in/87081

Match the pairs in the following questions:

(A) Virtual memory	(p) Temporal Locality
(B) Shared memory	(q) Spatial Locality
(C) Look-ahead buffer	(r) Address Translation
(D) Look-aside buffer	(s) Mutual Exclusion

match-the-following gate1989 operating-system virtual-memory

Answer

5.32.3 Virtual Memory: GATE1990-1-v top

http://gateoverflow.in/83833

Fill in the blanks:

Under paged memory management scheme, simple lock and key memory protection arrangement may still be required if the __________ processors do not have address mapping hardware.

gate1990 operating-system virtual-memory

Answer

5.32.4 Virtual Memory: GATE1990-7b top

http://gateoverflow.in/85404

In a two-level virtual memory, the memory access time for main memory, $t_M = 10^{-8}$ sec, and the memory access time for the secondary memory, $t_D = 10^{-3}$ sec. What must be the hit ratio, H such that the access efficiency is within 80 percent of its maximum value?

gate1990 descriptive operating-system virtual-memory

Answer

5.32.5 Virtual Memory: GATE1991_03,xi top http://gateoverflow.in/525

Choose the correct alternatives (more than one can be correct) and write the corresponding letters only:

Indicate all the false statements from the statements given below:

(a). The amount of virtual memory available is limited by the availability of the secondary memory

(b). Any implementation of a critical section requires the use of an indivisible machine- instruction ,such as test-and-set.

(c). The use of monitors ensure that no dead-locks will be caused .

(d). The LRU page-replacement policy may cause thrashing for some type of programs.

(e). The best fit techniques for memory allocation ensures that memory will never be fragmented.

gate1991 operating-system virtual-memory normal

Answer

5.32.6 Virtual Memory: GATE1994-1.21 top http://gateoverflow.in/2464

Which one of the following statements is true?

A. Macro definitions cannot appear within other macro definitions in assembly language programs
B. Overlaying is used to run a program which is longer than the address space of a computer
C. Virtual memory can be used to accommodate a program which is longer than the address space of a computer
D. It is not possible to write interrupt service routines in a high level language

gate1994 operating-system normal virtual-memory

Answer

5.32.7 Virtual Memory: GATE1995_1.7 top http://gateoverflow.in/2594

In a paged segmented scheme of memory management, the segment table itself must have a page table because

A. The segment table is often too large to fit in one page
B. Each segment is spread over a number of pages
C. Segment tables point to page tables and not to the physical locations of the segment
D. The processor's description base register points to a page table

gate1995 operating-system virtual-memory normal

Answer

5.32.8 Virtual Memory: GATE1995_2.16 top http://gateoverflow.in/2628

In a virtual memory system the address space specified by the address lines of the CUP must be ______ than the physical memory size and _____ than the secondary storage size.

A. smaller, smaller
B. smaller, larger

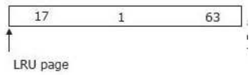
C. larger, smaller
D. larger, larger

gate1995 operating-system virtual-memory normal

Answer

5.32.9 Virtual Memory: GATE1996_7 top http://gateoverflow.in/2759

A demand paged virtual memory system uses 16 bit virtual address, page size of 256 bytes, and has 1 Kbyte of main memory. LRU page replacement is implemented using list, whose current status (page number is decimal) is



For each hexadecimal address in the address sequence given below,

00FF, 010D, 10FF, 11B0

indicate

i. the new status of the list

ii. page faults, if any, and

iii. page replacements, if any.

gate1996 operating-system virtual-memory normal

Answer

5.32.10 Virtual Memory: GATE1999-2.10 top http://gateoverflow.in/1488

A multi-user, multi-processing operating system cannot be implemented on hardware that does not support

A. Address translation
B. DMA for disk transfer
C. At least two modes of CPU execution (privileged and non-privileged)
D. Demand paging

gate1999 operating-system normal virtual-memory

Answer

5.32.11 Virtual Memory: GATE1999_19 top http://gateoverflow.in/1518

A certain computer system has the segmented paging architecture for virtual memory. The memory is byte addressable. Both virtual and physical address spaces contain 2^{16} bytes each. The virtual address space is divided into 8 non-overlapping equal size segments. The memory management unit (MMU) has a hardware segment table, each entry of which contains the physical address of the page table for the segment. Page tables are stored in the main memory and consists of 2 byte page table entries.

a. What is the minimum page size in bytes so that the page table for a segment requires at most one page to store it? Assume that the page size can only be a power of 2.

b. Now suppose that the pages size is 512 bytes. It is proposed to provide a TLB (Transaction look-aside buffer) for speeding up address translation. The proposed TLB will be capable of storing page table entries for 16 recently referenced virtual pages, in a fast cache that will use the direct mapping scheme. What is the number of tag bits that will need to be associated with each cache entry?

c. Assume that each page table entry contains (besides other information) 1 valid bit, 3 bits for page protection and 1 dirty bit. How many bits are available in page table entry for storing the aging information for the page? Assume that the page size is 512 bytes.

gate1999 operating-system virtual-memory normal

Answer

5.32.12 Virtual Memory: GATE1999_2.11 top http://gateoverflow.in/1489

Which of the following is/are advantage(s) of virtual memory?

(a) Faster access to memory on an average.

(b) Processes can be given protected address spaces.

(c) Linker can assign addresses independent of where the program will be loaded in physical memory.

(d) Program larger than the physical memory size can be run.

gate1999 operating-system virtual-memory easy

Answer

5.32.13 Virtual Memory: GATE2001-1.20 top http://gateoverflow.in/713

Where does the swap space reside?

A. RAM
B. Disk
C. ROM
D. On-chip cache

gate2001 operating-system easy virtual-memory

Answer

5.32.14 Virtual Memory: GATE2001-1.21 top http://gateoverflow.in/714

Consider a virtual memory system with FIFO page replacement policy. For an arbitrary page access pattern, increasing the number of page frames in main memory will

A. always decrease the number of page faults
B. always increase the number of page faults
C. sometimes increase the number of page faults
D. never affect the number of page faults

gate2001 operating-system virtual-memory normal

Answer

5.32.15 Virtual Memory: GATE2001-1.8 top http://gateoverflow.in/701

Which of the following statements is false?

A. Virtual memory implements the translation of a program's address space into physical memory address space
B. Virtual memory allows each program to exceed the size of the primary memory
C. Virtual memory increases the degree of multiprogramming
D. Virtual memory reduces the context switching overhead

gate2001 operating-system virtual-memory normal

Answer

5.32.16 Virtual Memory: GATE2001-2.21 top http://gateoverflow.in/739

Consider a machine with 64 MB physical memory and a 32-bit virtual address space. If the page size s 4KB, what is the approximate size of the page table?

A. 16 MB
B. 8 MB
C. 2 MB
D. 24 MB

gate2001 operating-system virtual-memory normal

Answer

5.32.17 Virtual Memory: GATE2002-19 top http://gateoverflow.in/872

A computer uses 32-bit virtual address, and 32-bit physical address. The physical memory is byte addressable, and the page size is 4 kbytes. It is decided to use two level page tables to translate from virtual address to physical address. Equal number of bits should be used for indexing first level and second level page table, and the size of each table entry is 4 bytes.

a. Give a diagram showing how a virtual address would be translated to a physical address.
b. What is the number of page table entries that can be contained in each page?
c. How many bits are available for storing protection and other information in each page table entry?

gate2002 operating-system virtual-memory normal descriptive

Answer

5.32.18 Virtual Memory: GATE2003-26 top http://gateoverflow.in/916

In a system with 32 bit virtual addresses and 1 KB page size, use of one-level page tables for virtual to physical address translation is not practical because of

A. the large amount of internal fragmentation
B. the large amount of external fragmentation
C. the large memory overhead in maintaining page tables
D. the large computation overhead in the translation process

gate2003 operating-system virtual-memory normal

Answer

5.32.19 Virtual Memory: GATE2003-78 top http://gateoverflow.in/788

A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Assuming that no page faults occur, the average time taken to access a virtual address is approximately (to the nearest 0.5 ns)

A. 1.5 ns
B. 2 ns
C. 3 ns
D. 4 ns

gate2003 operating-system normal virtual-memory

Answer

5.32.20 Virtual Memory: GATE2003-79 top http://gateoverflow.in/43578

A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Suppose a process has only the following pages in its virtual address space: two contiguous code pages starting at virtual address 0x00000000, two contiguous data pages starting at virtual address 0x00400000, and a stack page starting at virtual address 0xFFFFF000. The amount of memory required for storing the page tables of this process is

A. 8 KB
B. 12 KB
C. 16 KB
D. 20 KB

gate2003 operating-system normal virtual-memory

Answer

5.32.21 Virtual Memory: GATE2004-IT-66 top http://gateoverflow.in/3709

In a virtual memory system, size of virtual address is 32-bit, size of physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. Which one of the following is the maximum number of bits that can be used for storing protection and other information in each page table entry?

A. 2
B. 10
C. 12
D. 14

gate2004-it operating-system virtual-memory normal

Answer

5.32.22 Virtual Memory: GATE2006-62, ISRO2016-50 top http://gateoverflow.in/1840

A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a translation look-aside buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is:

A. 11 bits
B. 13 bits
C. 15 bits
D. 20 bits

gate2006 operating-system virtual-memory normal isro2016

Answer

5.32.23 Virtual Memory: GATE2006-63, UGCNET-June2012-III-45 top http://gateoverflow.in/1841

A computer system supports 32-bit virtual addresses as well as 32-bit physical addresses. Since the virtual address space is of the same size as the physical address space, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true?

A. Efficient implementation of multi-user support is no longer possible
B. The processor cache organization can be made more efficient now
C. Hardware support for memory management is no longer needed
D. CPU scheduling can be made more efficient now

gate2006 operating-system virtual-memory normal ugcnetjune2012iii

Answer

5.32.24 Virtual Memory: GATE2008-67 top http://gateoverflow.in/490

A processor uses 36 bit physical address and 32 bit virtual addresses, with a page frame size of 4 Kbytes. Each page table entry is of size 4 bytes. A three level page table is used for virtual to physical address translation, where the virtual address is used as follows:

- Bits 30-31 are used to index into the first level page table.
- Bits 21-29 are used to index into the 2nd level page table.
- Bits 12-20 are used to index into the 3rd level page table.
- Bits 0-11 are used as offset within the page.

The number of bits required for addressing the next level page table(or page frame) in the page table entry of the first, second and third level page tables are respectively

A. 20,20,20
B. 24,24,24

C. 24,24,20
D. 25,25,24

gate2008 operating-system virtual-memory normal

Answer

5.32.25 Virtual Memory: GATE2008-IT-16 top http://gateoverflow.in/3276

A paging scheme uses a Translation Look-aside Buffer (TLB). A TLB-access takes 10 ns and a main memory access takes 50 ns. What is the effective access time(in ns) if the TLB hit ratio is 90% and there is no page-fault?

A. 54
B. 60
C. 65
D. 75

gate2008-it operating-system virtual-memory normal

Answer

5.32.26 Virtual Memory: GATE2008-IT-41 top http://gateoverflow.in/3351

Assume that a main memory with only 4 pages, each of 16 bytes, is initially empty. The CPU generates the following sequence of virtual addresses and uses the Least Recently Used (LRU) page replacement policy.

0, 4, 8, 20, 24, 36, 44, 12, 68, 72, 80, 84, 28, 32, 88, 92

How many page faults does this sequence cause? What are the page numbers of the pages present in the main memory at the end of the sequence?

A. 6 and 1, 2, 3, 4
B. 7 and 1, 2, 4, 5
C. 8 and 1, 2, 4, 5
D. 9 and 1, 2, 3, 5

gate2008-it operating-system virtual-memory normal

Answer

5.32.27 Virtual Memory: GATE2008-IT-56 top http://gateoverflow.in/3366

Match the following flag bits used in the context of virtual memory management on the left side with the different purposes on the right side of the table below.

Name of the bit		**Purpose**	
I.	Dirty	a.	Page initialization
II.	R/W	b.	Write-back policy
III.	Reference	c.	Page protection
IV.	Valid	d.	Page replacement policy

A. I-d, II-a, III-b, IV-c
B. I-b, II-c, III-a, IV-d
C. I-c, II-d, III-a, IV-b
D. I-b, II-c, III-d, IV-a

gate2008-it operating-system virtual-memory easy

Answer

5.32.28 Virtual Memory: GATE2009-10 top http://gateoverflow.in/1302

The essential content(s) in each entry of a page table is / are

A. Virtual page number

B. Page frame number

C. Both virtual page number and page frame number

D. Access right information

gate2009 operating-system virtual-memory easy

Answer

5.32.29 Virtual Memory: GATE2009-34 top http://gateoverflow.in/1320

A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because

A. It reduces the memory access time to read or write a memory location.
B. It helps to reduce the size of page table needed to implement the virtual address space of a process
C. It is required by the translation lookaside buffer.
D. It helps to reduce the number of page faults in page replacement algorithms.

gate2009 operating-system virtual-memory easy

Answer

5.32.30 Virtual Memory: GATE2009-9, ISRO2016-52 top http://gateoverflow.in/1301

In which one of the following page replacement policies, Belady's anomaly may occur?

A. FIFO
B. Optimal
C. LRU
D. MRU

gate2009 operating-system virtual-memory normal isro2016

Answer

5.32.31 Virtual Memory: GATE2011-20, UGCNET-June2013-II-48 top http://gateoverflow.in/2122

Let the page fault service time be 10 milliseconds(ms) in a computer with average memory access time being 20 nanoseconds (ns). If one page fault is generated every 10^6 memory accesses, what is the effective access time for memory?

A. 21 ns
B. 30 ns
C. 23 ns
D. 35 ns

gate2011 operating-system virtual-memory normal ugcnetjune2013ii

Answer

5.32.32 Virtual Memory: GATE2013-52 top http://gateoverflow.in/379

A computer uses 46-bit virtual address, 32-bit physical address, and a three–level paged page table organization. The page table base register stores the base address of the first-level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second-level table (T2). Each entry of T2 stores the base address of a page of the third-level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the size of a page in KB in this computer?

A. 2
B. 4
C. 8
D. 16

gate2013 operating-system virtual-memory normal

Answer

5.32.33 Virtual Memory: GATE2013-53 top http://gateoverflow.in/43294

A computer uses 46-bit virtual address, 32-bit physical address, and a three–level paged page table organization. The page table base register stores the base address of the first-level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second-level table (T2). Each entry of T2 stores the base address of a page of the third-level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the minimum number of page colours needed to guarantee that no two synonyms map to different sets in the processor cache of this computer?

A. 2
B. 4
C. 8
D. 16

gate2013 normal operating-system virtual-memory

Answer

5.32.34 Virtual Memory: GATE2014-3-33 top http://gateoverflow.in/2067

Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in milliseconds) is _________.

gate2014-3 operating-system virtual-memory numerical-answers normal

Answer

5.32.35 Virtual Memory: GATE2015-1_12 top http://gateoverflow.in/8186

Consider a system with byte-addressable memory, 32-bit logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in megabytes is_________________.

gate2015-1 operating-system virtual-memory easy numerical-answers

Answer

5.32.36 Virtual Memory: GATE2015-2_25 top http://gateoverflow.in/8120

A computer system implements a 40-bit virtual address, page size of 8 kilobytes, and a 128-entry translation look-aside buffer (TLB) organized into 32 sets each having 4 ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____.

gate2015-2 operating-system virtual-memory easy numerical-answers

Answer

5.32.37 Virtual Memory: GATE2015-2_47 top http://gateoverflow.in/8247

A computer system implements 8 kilobyte pages and a 32-bit physical address space. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the virtual address supported by the system is _______ bits.

gate2015-2 operating-system virtual-memory normal numerical-answers

Answer

Answers: Virtual Memory

5.32.1 Virtual Memory: GATE 2016-1-47 top http://gateoverflow.in/39690

Selected Answer

NO. OF PAGES (N) = 2^26 = NO. OF ENTRIES IN PAGE TABLE

PAGE TABLE ENTRY SIZE (E) = 6 Bytes

So, Page Table Size = n * e = 2^26 x 6 Bytes = 384MB

12 votes -- G VENKATESWARLU (619 points)

384 MB ($2^{20}*2^6*6$ bytes)

17 votes -- Bharani Viswas (671 points)

5.32.2 Virtual Memory: GATE1989-2-iv top http://gateoverflow.in/87081

Selected Answer

(A) Virtual memory (p) Address Translation
(B) Shared memory (q) Mutual Exclusion
(C) Look-ahead buffer (r) Spatial Locality
(D) Look-aside buffer (s) Temporal Locality

http://gateoverflow.in/3304/difference-between-translation-buffer-translation-buffer

9 votes -- Prashant Singh (49.2k points)

5.32.3 Virtual Memory: GATE1990-1-v top http://gateoverflow.in/83833

i/o processors bcz processor will issue address for device controller and if there is no translation hardware then it ain't gonna be peachy.

5 votes -- ashish gusai (359 points)

5.32.4 Virtual Memory: GATE1990-7b top http://gateoverflow.in/85404

Selected Answer

In 2 level virtual memory, for every memory access, we need 2 page table access (TLB is missing in the question) and 1 memory access for data. So, best case memory access time

$= 3 \times 10^{-8}\ s.$

We are given

$$3 \times 10^{-8} = 0.8\left[3 \times 10^{-8} + (1-h) \times 10^{-3}\right]$$

$$\implies 0.6 \times 10^{-8} = 0.8 \times 10^{-3} - 0.8h \times 10^{-3} \implies h = \frac{8 \times 10^{-4} - 6 \times 10^{-9}}{8 \times 10^{-4}} = 1 - 0.75 \times 10^{-5} \approx 99.99\%$$

15 votes -- Arjun Suresh (294k points)

5.32.5 Virtual Memory: GATE1991_03,xi top http://gateoverflow.in/525

Selected Answer

A) A is true.

B) This is false. Example :- Peterson's solution is purely software based solution without use of hardware.

https://en.wikipedia.org/wiki/Peterson's_algorithm

C) False. Reference -> https://en.wikipedia.org/wiki/Monitor_(synchronization)

D) True. This will happend if page getting replaced is immediately refered in next cycle.

E) False.Memory can get fragmented with First fit.

10 votes -- Akash (43.8k points)

5.32.6 Virtual Memory: GATE1994-1.21 top http://gateoverflow.in/2464

Selected Answer

1. Is TRUE.

2. False. Overlaying is used to increase the address space usage when physical memory is limited on systems where virtual memory is absent. But it cannot increase the address space (logical) of a computer.

3. False. Like above is true for physical memory but here it is specified address space which should mean logical address space.

4. Is false. We can write in high level language just that the performance will be bad.

11 votes -- Arjun Suresh (294k points)

5.32.7 Virtual Memory: GATE1995_1.7 top http://gateoverflow.in/2594

Selected Answer

Option B is true for segmented paging(segment size becomes large so paging done on each segment) which is different from paged segmentation(segment table size becomes large and paging done on segment table)

Here option A is true , as segment table are sometimes too large to keep in one pages. So, segment table divided into pages. Thus page table for each Segment Table pages are created.

For reference , read below :

https://stackoverflow.com/questions/16643180/differences-or-similarities-between-segmented-paging-and-paged-segmentation
Differences or similarities between Segmented paging and Paged segmentation scheme.

11 votes -- Anurag Semwal (8k points)

ans is A

segment table is too large therefore paged segmented table is used.

12 votes -- jayendra (8.1k points)

5.32.8 Virtual Memory: GATE1995_2.16 top http://gateoverflow.in/2628

ans is C.

primary memory < virtual memory < secondary memory

we can extend VM upto the size of disk(secondary memory).

8 votes -- jayendra (8.1k points)

5.32.9 Virtual Memory: GATE1996_7 top http://gateoverflow.in/2759

Selected Answer

Given that page size is 256 bytes (2^8) and Main memory (MM) is 1KB (2^{10}).

So total number of pages that can be accommodated in MM = $2^{10}/2^8 = 2^2 = 4$

So essentially, there are 4 frames that can be used for paging (or page replacements).

The current sequence of pages in memory shows 3 pages (17, 1, 63). So there is 1 more empty frame left. It also says that the least recently used page is 17.

Now, since page size given is 8 bits wide (256 B), and virtual memory is of 16 bit, we can say that 8 bits are used for offset. The given address sequence is hexadecimal can be divided accordingly:

Page Number in Hexadecimal	Offset	Page Number in Decimal
00	FF	**0**
01	0D	**1**
10	FF	**16**
11	B0	**17**

We only need the Page numbers, which can be represented in decimal as: 0, 1, 16, 17.

Now, if we apply LRU algo to the existing frame with these incoming pages, we get the following states:

0 | Miss| 17 1 63 **0**

1 | Hit| 17 **1** 63 0

16 | Miss| **16** 1 63 0

17 | Miss| 16 1 **17** 0

i) New status of the list is **16 1 17 0.**

ii) Number of page faults = **3**.

iii) Page replacements are indicated above.

19 votes -- Ashis Kumar Sahoo (823 points)

5.32.10 Virtual Memory: GATE1999-2.10 top http://gateoverflow.in/1488

Selected Answer

Answer should be both A and C (Earlier GATE questions had multiple answers and marks were given only if all correct answers were selected).

Address translation is needed to provide memory protection so that a given process does not interfere with another.

We also need at least 2 modes of execution to ensure user processes share resources properly and OS maintains control. This is not required for a single user OS like early version of MS-DOS.

Demand paging and DMA enhances the performances- not a strict necessity.

Ref: Hardware protection section in Galvin

http://www.examrace.com/d/pdf/f54efd26/GATE-Computer-Science-1999.pdf

19 votes -- Arjun Suresh (294k points)

5.32.11 Virtual Memory: GATE1999_19 top http://gateoverflow.in/1518

Selected Answer

A)

$\text{Size of each segment} = \frac{2^{16}}{8} = 2^{13}$

Let the size of page be 2^k bytes

We need a page table entry for each page. For a segment of size 2^{13}, number of pages required will be

2^{13-k} and so we need 2^{13-k} page table entries. Now, the size of these many entries must be less than or equal to the page size, for the page table of a segment to be requiring at most one page. So,

$2^{13-k} \times 2 = 2^k$ (As a page table entry size is 2 bytes)

$k = 7$ bits

So, $\text{page size} = 2^7 = 128$ bytes

B)

The TLB is placed after the segment table.

Each segment will have $\frac{2^{13}}{2^9} = 2^4$ page table entries

So all page table entries of a segment will reside in the cache and segment number will differentiate between page table entry of each segment in the TLB cache.

$\text{Total segments} = 8$

Therefore 3 bits of tag is required

C)

$\text{Number of Pages for a segment} = \frac{2^{16}}{2^9} = 2^7$

$\text{Bits needed for page identification} = 7 \text{ bits} + 1 \text{ valid bit} + 3 \text{ page protection bits} + 1 \text{ dirty bit} = 12 \text{ bits needed for a pag}$

$\text{Size of each page table entry} = 2$ bytes $= 16$ bits

$\text{Number of bits left for aging} = 16 - 12 = 4$ bits

11 votes -- Danish (3.6k points)

5.32.12 Virtual Memory: GATE1999_2.11 top http://gateoverflow.in/1489

Selected Answer

Virtual memory provides an interface through which processes access the physical memory. So,
(a) Is false as direct access can never be slower.

(b) Is true as without virtual memory it is difficult to give protected address space to processes as they will be accessing physical memory directly. No protection mechanism can be done inside the physical memory as processes are dynamic and number of processes changes from time to time.

(c) Position independent can be produced even without virtual memory support.

(d) This is one primary use of virtual memory. Virtual memory allows a process to run using a virtual address space and as and when memory space is required, pages are swapped in/out from the disk if physical memory gets full.

So, answer is b and d.

18 votes -- Arjun Suresh (294k points)

5.32.13 Virtual Memory: GATE2001-1.20 top http://gateoverflow.in/713

Selected Answer

Option B is correct.

Swap space is the area on a hard disk which is part of the Virtual Memory of your machine, which is a combination of accessible physical memory (RAM) and the swap space. Swap space temporarily holds memory pages that are inactive. Swap space is used when your system decides that it needs physical memory for active processes and there is insufficient unused physical memory available. If the system happens to need more memory resources or space, inactive pages in physical memory are then moved to the swap space therefore freeing up that physical memory for other uses. Note that the access time for swap is slower therefore do not consider it to be a complete replacement for the physical memory. Swap space can be a dedicated swap partition (recommended), a swap file, or a combination of swap partitions and swap files.

👍 19 votes -- Manoj Kumar (37.5k points)

ans is B.

generally swap space is 2*RAM, not compulsorily always but generally. inactive pages of memory are moved to swap memory.

👍 10 votes -- jayendra (8.1k points)

5.32.14 Virtual Memory: GATE2001-1.21 top http://gateoverflow.in/714

Selected Answer

ans is C.

Belady's anomaly.

👍 12 votes -- jayendra (8.1k points)

5.32.15 Virtual Memory: GATE2001-1.8 top http://gateoverflow.in/701

Selected Answer

D should be the answer.

A - MMU does this translation but MMU is part of VM (hardware).

B, C - The main advantage of VM is the increased address space for programs, and independence of address space, which allows more degree of multiprogramming as well as option for process security.

D - VM requires switching of page tables (this is done very fast via switching of pointers) for the new process and thus it is theoretically slower than without VM. In anyway VM doesn't directly decrease the context switching overhead.

👍 21 votes -- Arjun Suresh (294k points)

5.32.16 Virtual Memory: GATE2001-2.21 top http://gateoverflow.in/739

Selected Answer

Number of pages = 2^{32} / 4KB = 2^{20} as we need to map every possible virtual address.

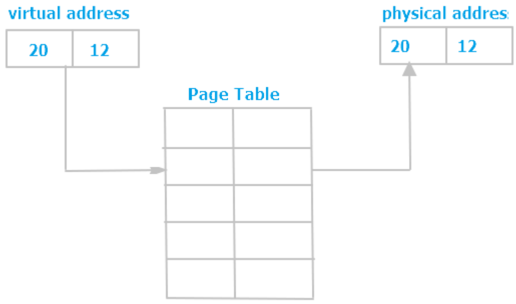
So, we need 2^{20} entries in the page table. Physical memory being 64 MB, a physical address must be 26 bits and a page (of size 4KB) address needs 26-12 = 14 address bits. So, each page table entry must be at least 14 bits.

So, total size of page table = 2^{20} * 14 bits ≈ 2 MB (assuming PTE is 2 bytes)

👍 21 votes -- Arjun Suresh (294k points)

5.32.17 Virtual Memory: GATE2002-19 top http://gateoverflow.in/872

- VA = 32 Bit
- PA = 32 Bit
- Page size = 4 KB = 2^{12} B
- PTE = 4 B



B) No of Page Tables entries possible = Page size / PTE = 2^{12} B/ 4 B = 2^{10}

Equal number of bits should be used for indexing first level and second level page table, is given because one page can contain 2^{10} entries. Then 2^{10} * 2^{10} =2^{20}

C)

Frame no = 32 bit (Physcial Address) - 12 (Offset) = 20

No of BIts available for Storing Protection = 4 * 8 - 20 Bit = 32-20 = 12 Bit

10 votes -- Akash (43.8k points)

5.32.18 Virtual Memory: GATE2003-26 top

http://gateoverflow.in/916

Selected Answer

Option A : Internal fragmentation exists only in the last level of paging.

Option B : There is no External fragmentation in the paging.

Option C : $\frac{2^{32}}{2^{10}} = 2^{22} = 4M$ entries in the page table which is very large. (**Answer**)

Option D : Not much relevant.

18 votes -- Abhishek Singhal (261 points)

5.32.19 Virtual Memory: GATE2003-78 top

http://gateoverflow.in/788

Selected Answer

78. It's given cache is physically addressed. So, address translation is needed for all memory accesses. (I assume page table lookup happens after TLB is missed, and main memory lookup after cache is missed)

```
Average access time = Average address translation time + Average memory access time
= 1ns
(TLB is accessed for all accesses)
+ 2*10*0.04
(2 page tables accessed from main memory in case of TLB miss)
+ Average memory access time
= 1.8ns + Cache access time + Average main memory access time
= 1.8ns + 1 * 0.9 (90% cache hit)
+ 0.1 * (10+1) (main memory is accessed for cache misses only)
= 1.8ns + 0.9 + 1.1
= 3.8ns
```

We assumed that page table is in main memory and not cached. This is given in question also, though they do not explicitly say that page tables are not cached. But in practice this is common as given here. So, in such a system,

```
Average address translation time
= 1ns (TLB is accessed for all accesses)
+ 2*0.04 * [0.9 * 1 + 0.1 * 10]
```

```
(2 page tables accessed in case of TLB miss and they go through cache)
```

= 1 ns + 1.9 * .08

= 1.152 ns

and average memory access time = 1.152 ns + 2 ns = 3.152 ns

> If the same thing is repeated now probably you would get marks for both. 2003 is a long way back -- then page table caching never existed as given in the SE answers. Since it exists now, IIT profs will make this clear in question itself.

39 votes -- gatecse (13.4k points)

0.96(1+(0.9(1) + 0.1(10+1))) + 0.04(1+ 2* (10) + (0.9(1) + 0.1(10+1))) = 3.8 ns..so 4ns

11 votes -- resilientknight (2.3k points)

5.32.20 Virtual Memory: GATE2003-79 top

http://gateoverflow.in/43578

Selected Answer

First level page table is addressed using 10 bits and hence contains 2^{10} entries. Each entry is 4 bytes and hence this table requires 4 KB. Now, the process uses only 3 unique entries from this 1024 possible entries (two code pages starting from 0x00000000 and two data pages starting from 0x00400000 have same first 10 bits). Hence, there are only 3 second level page tables. Each of these second level page tables are also addressed using 10 bits and hence of size 4 KB. So,

```
total page table size of the process
= 4 KB + 3 * 4 KB
= 16 KB
```

17 votes -- Arjun Suresh (294k points)

5.32.21 Virtual Memory: GATE2004-IT-66 top

http://gateoverflow.in/3709

Selected Answer

ans is D

page table entry must contain bits for representing frames and other bits for storing information like dirty bit,reference bit etc

no. of frames (no. of possible pages) = Physical memory size/ Page size = $2^{30}/2^{12} = 2^{18}$

18+x=32   (PT entry size=32 bit)

x =14 bits

15 votes -- neha pawar (4.4k points)

5.32.22 Virtual Memory: GATE2006-62, ISRO2016-50 top

http://gateoverflow.in/1840

Selected Answer

page size of 4KB.. so offset bits are 12 bits..

so remaining bits of virtual address 32 - 12 = 20 bits will be used for indexing...

number of sets = 128/4 = 32 (4-way set) => 5 bits..

so tag bits = 20 - 5 = 15 bits..

so option (C)

18 votes -- Vicky Bajoria (4.9k points)

5.32.23 Virtual Memory: GATE2006-63, UGCNET-June2012-III-45 top http://gateoverflow.in/1841

Selected Answer

A is the best answer here.

Virtual memory provides

1. increased address space for processes
2. memory protection
3. relocation

So, when we don't need more address space, even if we get rid of virtual memory, we need hardware support for the other two. Without hardware support for memory protection and relocation, we can design a system (by either doing them in software or by partitioning the memory for different users) but those are highly inefficient mechanisms. i.e., there we have to divide the physical memory equally among all users and this limits the memory usage per user and also restricts the maximum number of users.

31 votes -- Arjun Suresh (294k points)

5.32.24 Virtual Memory: GATE2008-67 top http://gateoverflow.in/490

Selected Answer

Physical address is 36 bits. So, number of bits to represent page frame $= 36 - 12 = 24\ bits$ (12 offset bits as given in question). So, the third level page table must have 24 bits for addressing the page frames.

since frame size remains same, so does the number of bits require to represent its size, which are $12\ bits$
from the generated Logical Address which is of 32 bits, 12 offset bits that are required to represent frame offset are removed, so we are left with $32 - 12 = 20\ bits$;
these $20\ bits$ will be divided into three partitions so that each partition could represent which i^{th} level page table we are referring to.

Now we need to know how many bits will be required to represent 3^{rd} level page table. To compute that: we have to find the number of possible third level page tables and we need to address each of them in second level page table.

$$\text{Number of third level page tables possible} = \frac{\text{Physical memory size}}{\text{Size of a third level page table}} = \frac{2^{36}}{\text{Number of entries in a single third level page table} \times \text{Size of an entry}}$$

Similarly we need to find the no. of possible second level page tables and we need to address each of them in first level page table.

PS: No. of third level page tables possible means the no. of distinct addresses a page table can have. At any given time, no. of page tables at level j is equal to the no. of entries in the level $j-1$, but here we are considering the possible page table address.

http://www.cs.utexas.edu/~lorenzo/corsi/cs372/06F/hw/3sol.html See Problem 3, second part solution - It clearly says that we should not assume that page tables are page aligned.

So, we need 25 bits in second level page table for addressing the third level page tables.

Now,

$$\text{Number of second level page tables possible} = \frac{\text{Physical memory size}}{\text{Size of a second level page table}} = \frac{2^{36}}{\text{Number of entries in a single second level page table} \times \text{Size of an ent}}$$

So, we need 25 bits for addressing the second level page tables as well.

So, answer is (D).

60 votes -- Arjun Suresh (294k points)

Total no. of physical frames = 2^(36)/2^(12) = 2^24
Therefore, bits needed to address a physical frame = 24 .
Now, A **3rd level PTE[Page table entry]** contains **"bits to address a Physical frame"**[final mapping from virtual to

physical address] **+ valid/Invalid bit + some other bits**[R/w etc.] **.**

But, *question specifically asks for only "bits needed to address the next level page table or page frame".*
So, t**he bits needed to address the page frame** is **24.**

A **2nd level PTE[Page table entry]** contains **"bits to address a Physical frame"*[Physical address where a 3rd level page resides in main memory]*** **+** valid/Invalid bit + some other bits[R/w etc.]
So, **the bits needed to address the page frame/next page table** is **24.**
Similarly,
A **1st level PTE[Page table entry]** contains **"bits to address a Physical frame"*[Physical address where a 2nd level page resides in main memory]*** **+** valid/Invalid bit + some other bits[R/w etc.]
The bits needed to address the page frame/next page table is **24.**

Hence , the answer is B .

See figure 2 here for reference **:** http://www.cs.berkeley.edu/~kamil/teaching/sp04/031104.pdf .

17 votes -- done (769 points)

5.32.25 Virtual Memory: GATE2008-IT-16 top

http://gateoverflow.in/3276

Selected Answer

Effective access time = hit ratio * time during hit + miss ratio * time during miss

In both cases TLB is accessed and assuming page table is accessed from memory only when TLB misses.

= 0.9 * (10+50) + 0.1 *(10 + 50 + 50)

= 54 + 11

= 65

16 votes -- Arjun Suresh (294k points)

5.32.26 Virtual Memory: GATE2008-IT-41 top

http://gateoverflow.in/3351

Selected Answer

We have 4 spaces for a page and there will be a replacement only when a 5th distinct page comes. Lets see what happens for the sequence of memory accesses:

(Each page is of 16 bytes, so say for page 0, it contains virtual addresses from 0-15)

0: Page fault - 1, Pages in memory - 0

4: Page faults - 1, Pages in memory - 0

8: Page faults - 1, Pages in memory - 0

20: Page faults - 2, Pages in memory - 0, 1

24: Page faults - 2, Pages in memory - 0, 1

36: Page faults - 3, Pages in memory - 0, 1, 2

44: Page faults - 3, Pages in memory - 0, 1, 2

12: Page faults - 3, Pages in memory - 1, 2, 0

68: Page faults - 4, Pages in memory - 1, 2, 0, 4

72: Page faults - 4, Pages in memory - 1, 2, 0, 4

80: Page faults - 5, Pages in memory - 2, 0, 4, 5

84: Page faults - 5, Pages in memory - 2, 0, 4, 5

28: Page faults - 6, Pages in memory - 0, 4, 5, 1

32: Page faults - 7, Pages in memory - 4, 5, 1, 2

88: Page faults - 7, Pages in memory - 4, 1, 2, 5

92: Page faults - 7, Pages in memory - 4, 1, 2, 5

So, (B) choice.

20 votes -- Arjun Suresh (294k points)

5.32.27 Virtual Memory: GATE2008-IT-56 top http://gateoverflow.in/3366

Selected Answer

Option (D)..

Dirty and R/W is well known..

Refrence bit is used in a version of FIFO called second chance (SC) policy, in order to avoid replacement of heavily used page.. It is set to one when a page is used heavily and periodically set to 0.. Since it is used in a version FIFO which is a page replacement policy, this bit is come under category of page replacement..

Valid bit is not used for page relacement.. It is not used in any page replacement policy.. it tells the page in the memory is valid or not.. If it is valid it is directly used and if it is not then a fresh page is loaded.. So basically it is page initialization. because we are not replacing, it is initializing, we not knocking out somebody, we are filling empty space... so initialization.. so option (D)

20 votes -- Vicky Bajoria (4.9k points)

5.32.28 Virtual Memory: GATE2009-10 top http://gateoverflow.in/1302

Selected Answer

It is B.

The page table contains the page frame number essentially.

11 votes -- Gate Keeda (19.1k points)

5.32.29 Virtual Memory: GATE2009-34 top http://gateoverflow.in/1320

Selected Answer

B.

Which is a clear reason why we perform paging.

When the page table size increases we perform paging on the page table. Resulting in multi-level page table.

12 votes -- Gate Keeda (19.1k points)

5.32.30 Virtual Memory: GATE2009-9, ISRO2016-52 top http://gateoverflow.in/1301

Selected Answer

It is A.

http://en.wikipedia.org/wiki/B%C3%A9l%C3%A1dy%27s_anomaly

10 votes -- Gate Keeda (19.1k points)

5.32.31 Virtual Memory: GATE2011-20, UGCNET-June2013-II-48 top

http://gateoverflow.in/2122

Selected Answer

open slide 12-13 to check :

web.cs.ucla.edu/~ani/classes/cs111.08w/Notes/Lecture%2016.pdf

$$\begin{aligned}\text{EMAT} &= \frac{1}{10^6} \times 10\,ms + \left(1 - \frac{1}{10^6}\right) \times 20\,ns \\ &= 29.99998\,ns \\ &\approx 30\,ns\end{aligned}$$

answer = **option B**

29 votes -- Amar Vashishth (28.7k points)

Effective memory access time = Memory access time + page fault rate *page fault service time

so here

$\text{EMAT} = 20ns + \frac{1}{10^6} \times 10 \times 10^6 ns$

$= 20 + 10 = 30ns$

Ans is B.

15 votes -- neha pawar (4.4k points)

5.32.32 Virtual Memory: GATE2013-52 top

http://gateoverflow.in/379

Selected Answer

Let the page size be x.

Since virtual address is 46 bits, we have total number of pages $= \frac{2^{46}}{x}$

We should have an entry for each page in last level page table which here is T3. So,

number of entries in T3 (sum of entries across all possible T3 tables) $= \frac{2^{46}}{x}$

Each entry takes 32 bits = 4 bytes. So, total size of T3 tables $= \frac{2^{46}}{x} \times 4 = \frac{2^{48}}{x}$ bytes

Now, no. of T3 tables will be Total size of T3 tables/page table size and for each of these page tables, we must have a T2 entry. Taking T3 size as page size, no. of entries across all T2 tables

$= \frac{\frac{2^{48}}{x}}{x} = \frac{2^{48}}{x^2}$

Now, no. of T2 tables (assuming T2 size as pagesize) = $\frac{2^{48}}{x^2} \times 4$ bytes = $\frac{\frac{2^{50}}{x^2}}{x} = \frac{2^{50}}{x^3}$.

Now, for each of these page table, we must have an entry in T1. So, number of entries in T1

$= \frac{2^{50}}{x^3}$

And size of T1 $= \frac{2^{50}}{x^3} \times 4 = \frac{2^{52}}{x^3}$

Given in question, size of T1 is page size which we took as x. So,

$x = \frac{2^{52}}{x^3}$

$x^4 = 2^{52}$

$x = 2^{13}$

$= 8KB$

46 votes -- Arjun Suresh (294k points)

I already put it as comment, in case if one skipped it.

One other method to find page size-

We know that all levels page tables must be completely full except outermost, the outermost page table may occupy whole page or less. But in question, it is given that Outermost page table occupies whole page.

Now let page size is 2^p Bytes.

Given that PTE = 32 bits = 4 Bytes = 2^2 Bytes.

Number of entries in any page of any pagetable =page size/PTE = $2^p/2^2$ = 2^{p-2}.

Therefore Logical address split is

p-2	p-2	p-2	p

logical address space is 46bits given. Hence equation becomes,

(p-2)+(p-2)+(p-2)+p = 46

⇒p=13.

Therefore page size is 2^{13} Bytes =**8KB**.

22 votes -- Sachin Mittal (7.1k points)

5.32.33 Virtual Memory: GATE2013-53 top

http://gateoverflow.in/43294

Selected Answer

Let the page size be x.

Since virtual address is 46 bits, we have total number of pages $= \frac{2^{46}}{x}$

We should have an entry for each page in last level page table which here is T3. So,

number of entries in T3 (sum of entries across all possible T3 tables) $= \frac{2^{46}}{x}$

Each entry takes 32 bits = 4 bytes. So, total size of T3 tables $= \frac{2^{46}}{x} \times 4 = \frac{2^{48}}{x}$ bytes

Now, no. of T3 tables will be Total size of T3 tables/page table size and for each of these page tables, we must have a T2 entry. Taking T3 size as page size, no. of entries across all T2 tables

$= \frac{\frac{2^{48}}{x}}{x} = \frac{2^{48}}{x^2}$

Now, no. of T2 tables (assuming T2 size as pagesize) = $\frac{2^{48}}{x^2} \times 4$ bytes = $\frac{\frac{2^{50}}{x^2}}{x} = \frac{2^{50}}{x^3}$.

Now, for each of these page table, we must have an entry in T1. So, number of entries in T1

$= \frac{2^{50}}{x^3}$

And size of T1 $= \frac{2^{50}}{x^3} \times 4 = \frac{2^{52}}{x^3}$

Given in question, size of T1 is page size which we took as x. So,

$x = \frac{2^{52}}{x^3}$

$x^4 = 2^{52}$

$x = 2^{13}$

$= 8KB$

Min. no. of page color bits = No. of set index bits + no. of offset bits - no. of page index bits (This ensures no synonym maps to different sets in the cache)

We have 1MB cache and 64B cache block size. So,

number of sets = 1MB/(64B * Number of blocks in each set) = 16K/16 (16 way set associative) = 1K = 2^{10}.

So, we need 10 index bits. Now, each block being 64 (2^6) bytes means we need 6 offset bits.

And we already found page size = 8KB = 2^{13}, so 13 bits to index a page

Thus, no. of page color bits = 10 + 6 - 13 = 3.

With 3 page color bits we need to have 2^3 = 8 different page colors

More Explanation:

A synonym is a physical page having multiple virtual addresses referring to it. So, what we want is no two synonym virtual addresses to map to two different sets, which would mean a physical page could be in two different cache sets. This problem never occurs in a physically indexed cache as indexing happens via physical address bits and so one physical page can never go to two different sets in cache. In virtually indexed cache, we can avoid this problem by ensuring that the bits used for locating a cache block (index+offset) of the virtual and physical addresses are the same.

In our case we have 6 offset bits + 10 bits for indexing. So, we want to make these 16 bits same for both physical and virtual address. One thing is that the page offset bits - 13 bits for 8 KB page, is always the same for physical and virtual addresses as they are never translated. So, we don't need to make these 13 bits same. We have to only make the remaining 10 + 6 - 13 = 3 bits same. Page coloring is a way to do this. Here, all the physical pages are colored and a physical page of one color is mapped to a virtual address by OS in such a way that a set in cache always gets pages of the same color. So, in order to make the 3 bits same, we take all combinations of it (2^3 = 8) and colors the physical pages with 8 colors and a cache set always gets a page of one color only. (In page coloring, it is the job of OS to ensure that the 3 bits are the same).

http://ece.umd.edu/courses/enee646.F2007/Cekleov1.pdf

15 votes -- Arjun Suresh (294k points)

5.32.34 Virtual Memory: GATE2014-3-33 top http://gateoverflow.in/2067

Selected Answer

EMAT=TLB hit*(TLB access time+memory access time)+TLB miss(TLB access time+page table access time+memory access time)

=0.6(10+80)+0.4(10+80+80)

= 54+68

=122msec

20 votes -- neha pawar (4.4k points)

5.32.35 Virtual Memory: GATE2015-1_12 top http://gateoverflow.in/8186

Selected Answer

total no of pages = 2^32 / 2^12 = 2^20

We need a PTE for each page and an entry is 4 bytes. So,
page table size = 4 * 2^20 = 2^22 = 4MB

18 votes -- Anoop Sonkar (4.9k points)

5.32.36 Virtual Memory: GATE2015-2_25 top

http://gateoverflow.in/8120

Selected Answer

Ans 40 - (5+13) = 22 bits

TLB maps a virtual address to the physical address of the page. (The lower bits of page address - offset bits- are not used in TLB as they are the same for virtual as well as physical addresses). Here, for 8 kB page size we require 13 offset bits.

In TLB we have 32 sets and so virtual address space is divided into 32 using 5 set bits. (Associativity doesn't affect the set bits as they just adds extra slots in each set).

So, number of tag bits = 40 - 5 - 13 = 22

18 votes -- Vikrant Singh (13.4k points)

5.32.37 Virtual Memory: GATE2015-2_47 top

http://gateoverflow.in/8247

Selected Answer

8 KB pages means 13 offset bits.
For 32 bit physical address, 32 - 13 = 19 page frame bits must be there in each PTE (Page Table Entry).
We also have 1 valid bit, 1 dirty bit and 3 permission bits.
So, total size of a PTE (Page Table Entry) = 19 + 5 = 24 bits = 3 bytes.

Given in question, maximum page table size = 24 MB
Page table size = No. of PTEs * size of an entry
So, no. of PTEs = 24 MB / 3 B = 8 M

Virtual address supported = No. of PTEs * Page size (As we need a PTE for each page and assuming single-level paging)
= 8 M * 8 KB
= 64 GB = 2^{36} Bytes

So, length of virtual address supported = 36 bits (assuming byte addressing)

26 votes -- Arjun Suresh (294k points)

Ans 36 bits

Assume Virtual Address = x bits

entry size in page table = 19(frame bits)+5(permission bits) = 24 bits = 3 Bytes

2^(x-13)*3 = 24*2^(20)

solving we get x = 36 bits

10 votes -- Vikrant Singh (13.4k points)

5.33 Working Set(1) top

5.33.1 Working Set: GATE2006-IT-12 top

http://gateoverflow.in/3551

In the working-set strategy, which of the following is done by the operating system to prevent thrashing?

I. It initiates another process if there are enough extra frames.

II. It selects a process to suspend if the sum of the sizes of the working-sets exceeds the total number of available frames.

A. I only
B. II only
C. Neither I nor II
D. Both I and II

gate2006-it operating-system process-schedule working-set normal

Answer

Answers: Working Set

5.33.1 Working Set: GATE2006-IT-12 top

http://gateoverflow.in/3551

Selected Answer

Extract from Galvin "*If there are enough extra frames, another process can be initiated. If the sum of the working-set sizes increases, exceeding the total number of available frames,the operating system selects a process to suspend. The process's pages are written out (swapped), and its frames are reallocated to other processes. The suspended process can be restarted later.*"

So Option (D)

16 votes -- Danish (3.6k points)

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