FWC RTL ASSIGNMENT-1

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Main Code

```
`timescale 1ns / 1ps
module down_counter(
   input clk,
   input [7:0]in,
   input latch,
   input dec,
   input div_2,
   output reg[7:0] count,
   output reg z_flag
   );
always @ (posedge clk)
begin
   if ({latch,dec}==2'b10)
   count <= in;               //same as i/p
   else if ({latch,dec}==2'b11)
   count <=in;               //same as i/p since latch is high
   else if({latch,dec}==2'b01)
   begin
    if (count!=0)
    begin
    count<=count-1;          //decrements since dec is high and latch is 0
    z_flag<=0;              // when count !=0 zero flag is low
    end
    else
```

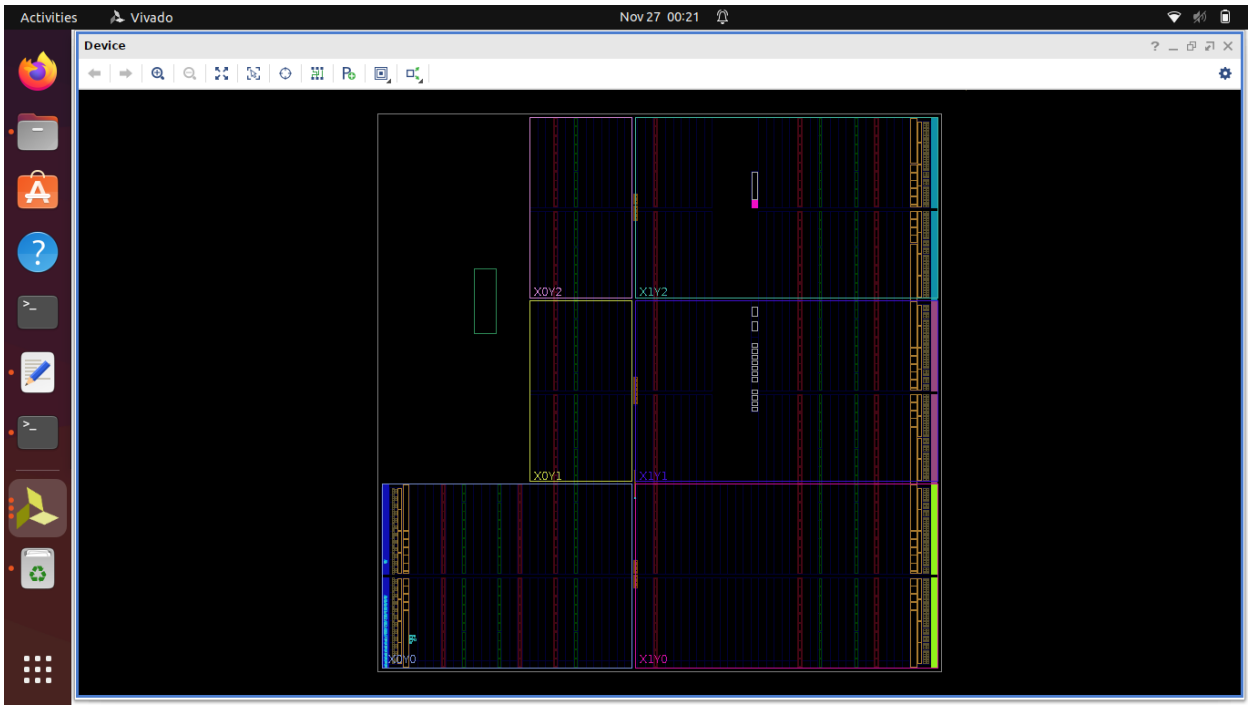
```
    z_flag<=1;              // when count = 0 zero flag is high
   end
  else if({latch,dec}==2'b00 & div_2==1)
  count<=count/2;           //result will be div/2 since div_2 is high
  else
  count<=count;
end
endmodule
```

Test bench

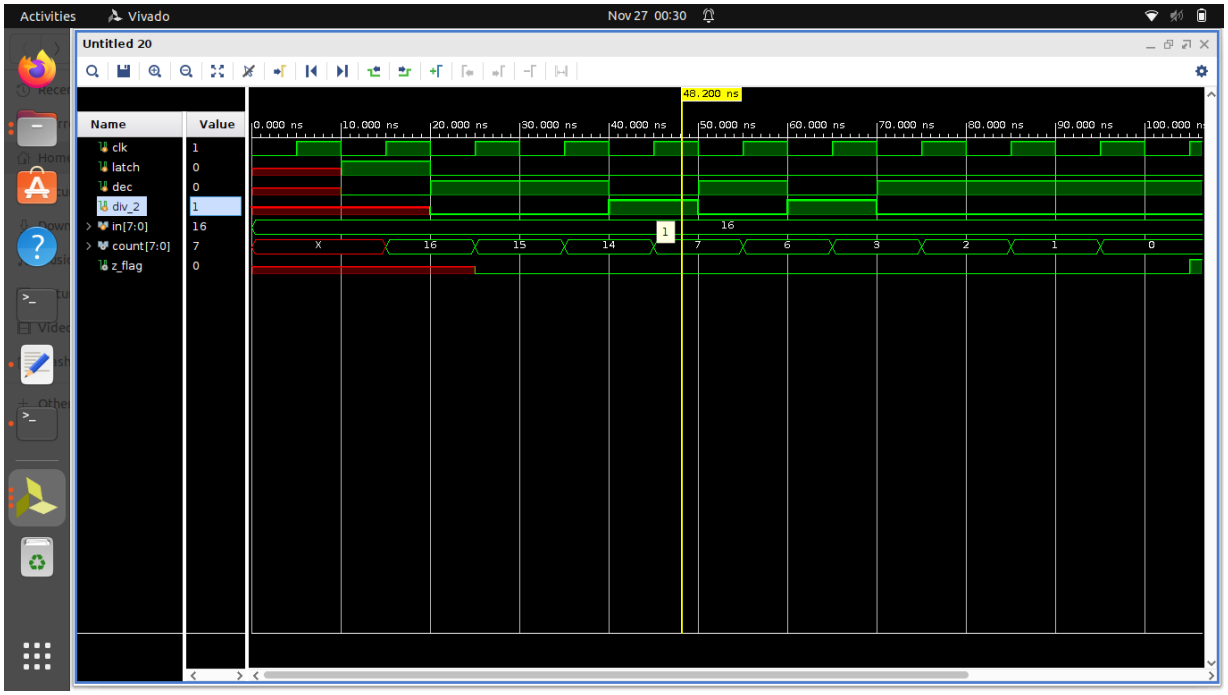
```
`timescale 1ns / 1ps
module down_counter_tb;

reg  clk,latch,dec,div_2;
reg [7:0] in=8'b00010000;

wire [7:0] count;
wire z_flag;

down_counter u1(.clk(clk),.in(in),.latch(latch),
          .dec(dec),.div_2(div_2),.count(count),.z_flag(z_flag));

always #5 clk=~clk;
initial begin
clk<=0;
#10 latch<=1;dec<=0;
#10 latch<=0;dec<=1;div_2=0;
#10 latch<=0;dec<=1;div_2=0;
#10 latch<=0;dec<=0;div_2=1;
```

```
#10 latch<=0;dec<=1;div_2=0;
#10 latch<=0;dec<=0;div_2=1;
#10 latch<=0;dec<=1;div_2=0;
#50 $stop;
end
endmodule
```

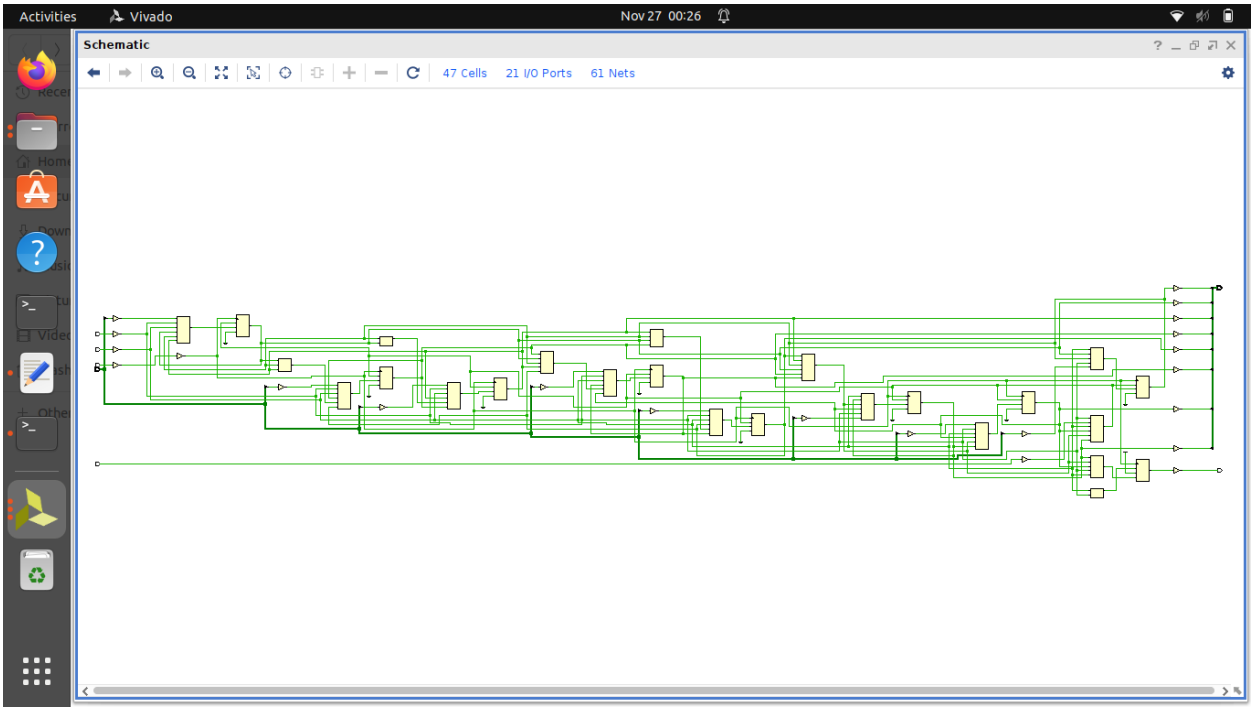
Device Diagram



Timing Diagram



Schematic Diagram



Dataflow Design (netlist)