



## 1. Description

### 1.1. Project

|                 |                           |
|-----------------|---------------------------|
| Project Name    | indipended_watchdog_timer |
| Board Name      | NUCLEO-L496ZG-P           |
| Generated with: | STM32CubeMX 6.8.1         |
| Date            | 07/05/2023                |

### 1.2. MCU

|                |                |
|----------------|----------------|
| MCU Series     | STM32L4        |
| MCU Line       | STM32L4x6      |
| MCU name       | STM32L496ZGTxP |
| MCU Package    | LQFP144        |
| MCU Pin number | 144            |

### 1.3. Core(s) information

|         |               |
|---------|---------------|
| Core(s) | Arm Cortex-M4 |
|---------|---------------|

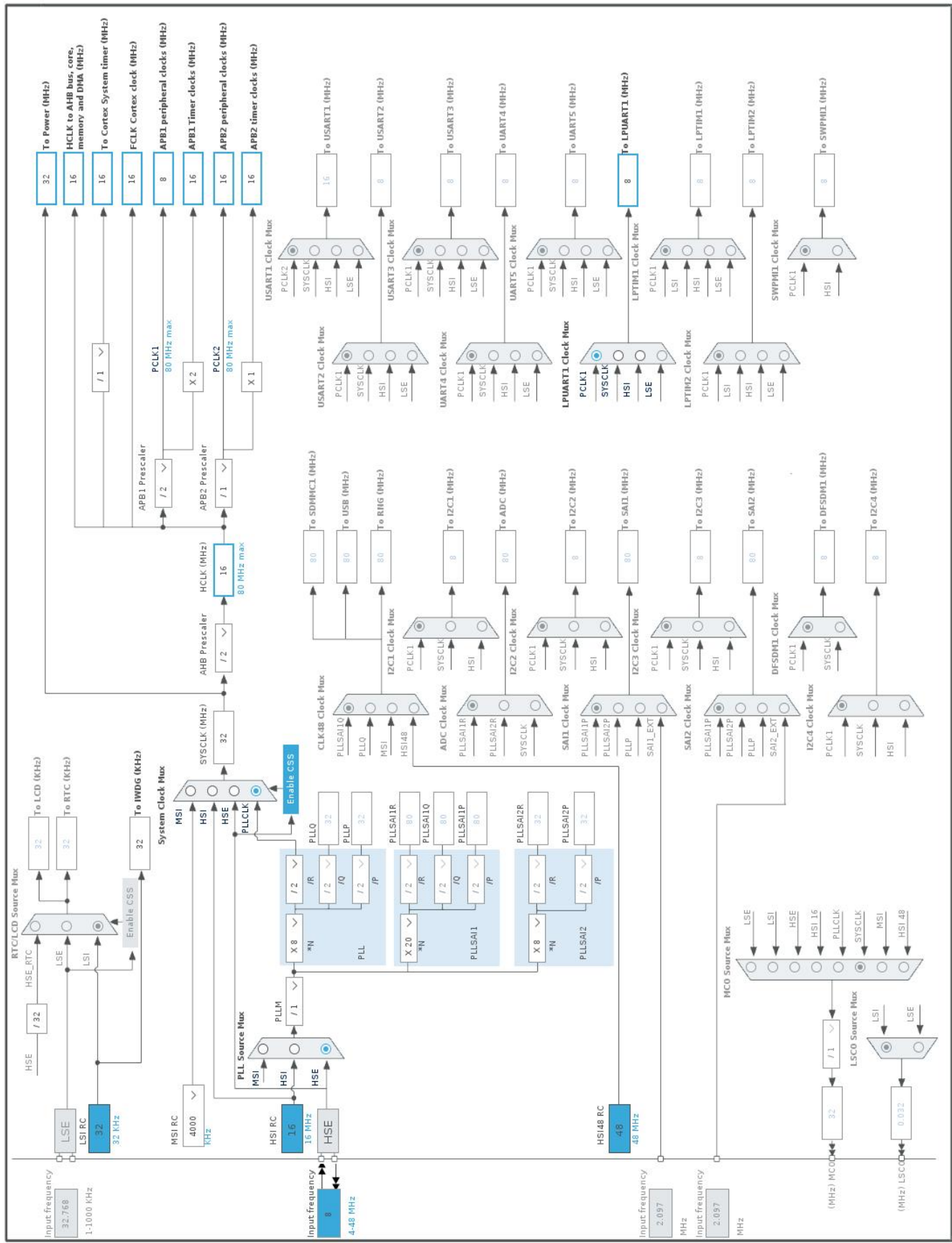


### 3. Pins Configuration

| Pin Number<br>LQFP144 | Pin Name<br>(function after<br>reset) | Pin Type | Alternate<br>Function(s) | Label        |
|-----------------------|---------------------------------------|----------|--------------------------|--------------|
| 6                     | VBAT                                  | Power    |                          |              |
| 16                    | VSS                                   | Power    |                          |              |
| 17                    | VDD                                   | Power    |                          |              |
| 23                    | PH0-OSC_IN (PH0)                      | I/O      | RCC_OSC_IN               |              |
| 24                    | PH1-OSC_OUT (PH1)                     | I/O      | RCC_OSC_OUT              |              |
| 25                    | NRST                                  | Reset    |                          |              |
| 30                    | VSSA                                  | Power    |                          |              |
| 31                    | VREF-                                 | Power    |                          |              |
| 33                    | VDDA                                  | Power    |                          |              |
| 38                    | VSS                                   | Power    |                          |              |
| 39                    | VDD                                   | Power    |                          |              |
| 51                    | VSS                                   | Power    |                          |              |
| 52                    | VDD                                   | Power    |                          |              |
| 61                    | VSS                                   | Power    |                          |              |
| 62                    | VDD                                   | Power    |                          |              |
| 70                    | VDD12                                 | Power    |                          |              |
| 71                    | VSS                                   | Power    |                          |              |
| 72                    | VDD                                   | Power    |                          |              |
| 83                    | VSS                                   | Power    |                          |              |
| 84                    | VDD                                   | Power    |                          |              |
| 92                    | PG7                                   | I/O      | LPUART1_TX               |              |
| 93                    | PG8                                   | I/O      | LPUART1_RX               |              |
| 94                    | VSS                                   | Power    |                          |              |
| 95                    | VDDIO2                                | Power    |                          |              |
| 106                   | VDDUSB                                | Power    |                          |              |
| 107                   | VSS                                   | Power    |                          |              |
| 108                   | VDD                                   | Power    |                          |              |
| 120                   | VSS                                   | Power    |                          |              |
| 121                   | VDD                                   | Power    |                          |              |
| 130                   | VSS                                   | Power    |                          |              |
| 131                   | VDDIO2                                | Power    |                          |              |
| 136                   | PB7 *                                 | I/O      | GPIO_Output              | BSP_LED_BLUE |
| 142                   | VDD12                                 | Power    |                          |              |
| 143                   | VSS                                   | Power    |                          |              |
| 144                   | VDD                                   | Power    |                          |              |

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

| Name                              | Value  |
|-----------------------------------|--|
| Project Name                      | indipended_watchdog_timer  |
| Project Folder                    | /home/dnk066/chirag/STM32/work space/TIMER/indipended_watchdog_timer |
| Toolchain / IDE                   | STM32CubeIDE   |
| Firmware Package Name and Version | STM32Cube FW_L4 V1.17.2  |
| Application Structure             | Advanced   |
| Generate Under Root               | Yes  |
| Do not generate the main()        | No   |
| Minimum Heap Size                 | 0x200  |
| Minimum Stack Size                | 0x400  |

### 5.2. Code Generation Settings

| Name  | Value                                 |
|---|---------------------------------------|
| STM32Cube MCU packages and embedded software                    | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files   | No                                    |
| Backup previously generated files when re-generating            | No                                    |
| Keep User Code when re-generating                               | Yes                                   |
| Delete previously generated files when not re-generated         | Yes                                   |
| Set all free pins as analog (to optimize the power consumption) | No                                    |
| Enable Full Assert  | No                                    |

### 5.3. Advanced Settings - Generated Function Calls

| Rank | Function Name        | Peripheral Instance Name |
|------|----------------------|--------------------------|
| 1    | SystemClock_Config   | RCC                      |
| 2    | MX_GPIO_Init         | GPIO                     |
| 3    | MX_LPUART1_UART_Init | LPUART1                  |
| 4    | MX_IWDG_Init         | IWDG                     |

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

|           |                |
|-----------|----------------|
| Series    | STM32L4        |
| Line      | STM32L4x6      |
| MCU       | STM32L496ZGTxP |
| Datasheet | DS11585_Rev2   |

### 6.2. Parameter Selection

|             |     |
|-------------|-----|
| Temperature | 25  |
| Vdd         | 3.0 |

### 6.3. Battery Selection

|                   |                 |
|-------------------|-----------------|
| Battery           | Li-SOCL2(A3400) |
| Capacity          | 3400.0 mAh      |
| Self Discharge    | 0.08 %/month    |
| Nominal Voltage   | 3.6 V           |
| Max Cont Current  | 100.0 mA        |
| Max Pulse Current | 200.0 mA        |
| Cells in series   | 1               |
| Cells in parallel | 1               |



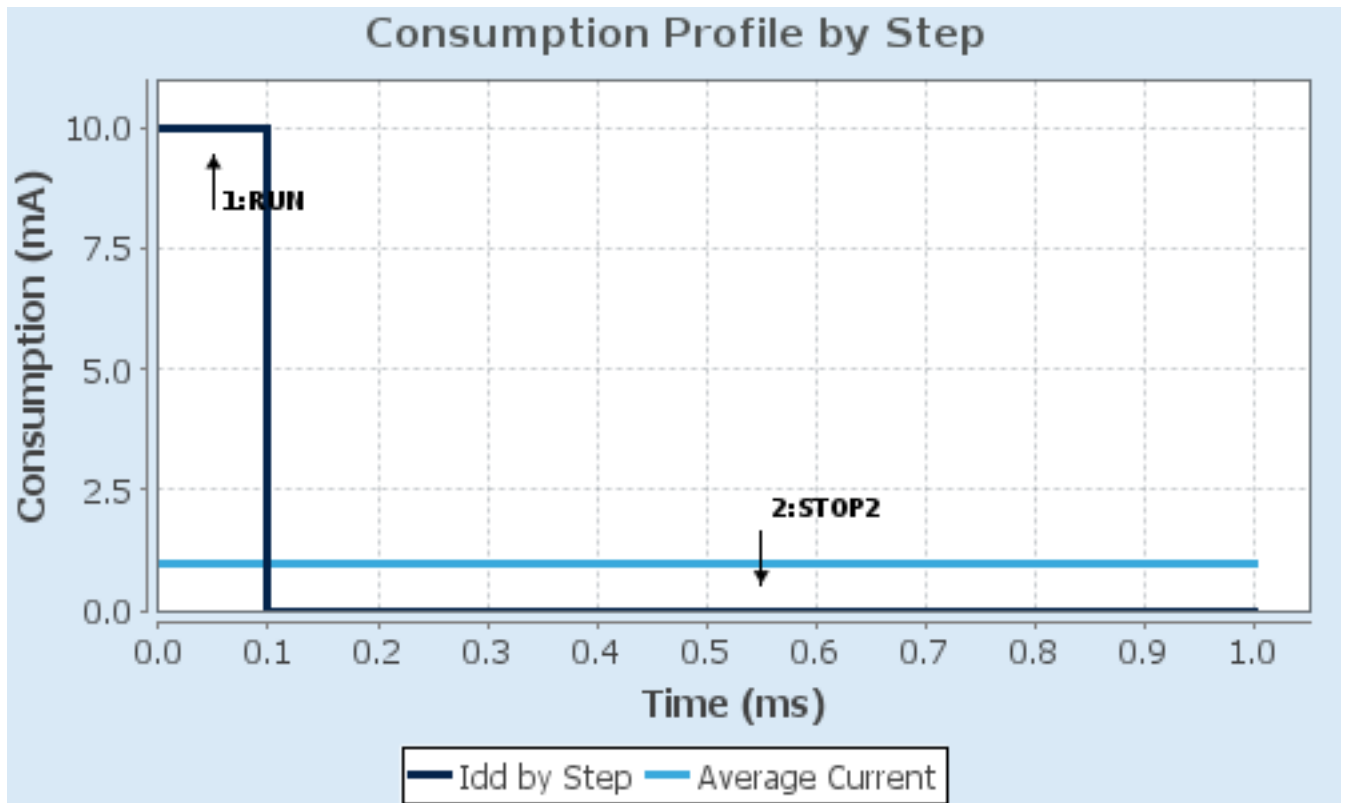
#### 6.4. Sequence

|                               |                      |                |
|-------------------------------|----------------------|----------------|
| <b>Step</b>                   | Step1                | Step2          |
| <b>Mode</b>                   | RUN                  | STOP2          |
| <b>Vdd</b>                    | 3.0                  | 3.0            |
| <b>Voltage Source</b>         | Battery              | Battery        |
| <b>Range</b>                  | Range1-High          | NoRange        |
| <b>Fetch Type</b>             | FLASH                | n/a            |
| <b>CPU Frequency</b>          | 80 MHz               | 0 Hz           |
| <b>Clock Configuration</b>    | HSE BYP PLL Flash-ON | ALL CLOCKS OFF |
| <b>Clock Source Frequency</b> | 4 MHz                | 0 Hz           |
| <b>Peripherals</b>            |                      |                |
| <b>Additional Cons.</b>       | 0 mA                 | 0 mA           |
| <b>Average Current</b>        | 10 mA                | 2.69 $\mu$ A   |
| <b>Duration</b>               | 0.1 ms               | 0.9 ms         |
| <b>DMIPS</b>                  | 100.0                | 0.0            |
| <b>Ta Max</b>                 | 104.04               | 105            |
| <b>Category</b>               | In DS Table          | In DS Table    |

#### 6.5. Results

|               |                            |                 |             |
|---------------|----------------------------|-----------------|-------------|
| Sequence Time | 1 ms                       | Average Current | 1 mA        |
| Battery Life  | 4 months, 19 days, 3 hours | Average DMIPS   | 100.0 DMIPS |

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. IWDG

**mode: Activated**

#### 7.1.1. Parameter Settings:

##### **Watchdog Clocking:**

|                                |             |
|--------------------------------|-------------|
| IWDG counter clock prescaler   | <b>8 *</b>  |
| IWDG window value              | 4095        |
| IWDG down-counter reload value | <b>79 *</b> |

### 7.2. LPUART1

**Mode: Asynchronous**

#### 7.2.1. Parameter Settings:

##### **Basic Parameters:**

|             |                                    |
|-------------|------------------------------------|
| Baud Rate   | <b>115200 *</b>                    |
| Word Length | <b>8 Bits (including Parity) *</b> |
| Parity      | None                               |
| Stop Bits   | 1                                  |

##### **Advanced Parameters:**

|                |                      |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Single Sample  | Disable              |

##### **Advanced Features:**

|                               |         |
|-------------------------------|---------|
| Auto Baudrate Mode            | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion                | Disable |
| TX and RX pins Swapping       | Disable |
| Overrun                       | Enable  |
| DMA on RX Error               | Enable  |
| MSB First                     | Disable |

### 7.3. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

### 7.3.1. Parameter Settings:

#### **System Parameters:**

|                   |                    |
|-------------------|--------------------|
| VDD voltage (V)   | 3.3                |
| Instruction Cache | Enabled            |
| Prefetch Buffer   | Disabled           |
| Data Cache        | Enabled            |
| Flash Latency(WS) | 0 WS (1 CPU cycle) |

#### **RCC Parameters:**

|                                |          |
|--------------------------------|----------|
| HSI Calibration Value          | 64       |
| MSI Calibration Value          | 0        |
| MSI Auto Calibration           | Disabled |
| HSE Startup Timeout Value (ms) | 100      |
| LSE Startup Timeout Value (ms) | 5000     |

#### **Power Parameters:**

|                               |                                 |
|-------------------------------|---------------------------------|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |
|-------------------------------|---------------------------------|

## **7.4. SYS**

**Timebase Source: SysTick**

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

| IP      | Pin               | Signal      | GPIO mode                    | GPIO pull/up pull down      | Max Speed             | User Label   |
|---------|-------------------|-------------|------------------------------|-----------------------------|-----------------------|--------------|
| LPUART1 | PG7               | LPUART1_TX  | Alternate Function Push Pull | No pull-up and no pull-down | <b>Very High</b><br>* |              |
|         | PG8               | LPUART1_RX  | Alternate Function Push Pull | No pull-up and no pull-down | <b>Very High</b><br>* |              |
| RCC     | PH0-OSC_IN (PH0)  | RCC_OSC_IN  | n/a                          | n/a                         | n/a                   |              |
|         | PH1-OSC_OUT (PH1) | RCC_OSC_OUT | n/a                          | n/a                         | n/a                   |              |
| GPIO    | PB7               | GPIO_Output | Output Push Pull             | No pull-up and no pull-down | Low                   | BSP_LED_BLUE |

### 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

#### 8.3.1. NVIC

| Interrupt Table  | Enable | Preenmption Priority | SubPriority |
|--|--------|----------------------|-------------|
| Non maskable interrupt   | true   | 0                    | 0           |
| Hard fault interrupt   | true   | 0                    | 0           |
| Memory management fault  | true   | 0                    | 0           |
| Prefetch fault, memory access fault                                  | true   | 0                    | 0           |
| Undefined instruction or illegal state                               | true   | 0                    | 0           |
| System service call via SWI instruction                              | true   | 0                    | 0           |
| Debug monitor  | true   | 0                    | 0           |
| Pendable request for system service                                  | true   | 0                    | 0           |
| System tick timer  | true   | 0                    | 0           |
| PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38 | unused |                      |             |
| Flash global interrupt   | unused |                      |             |
| RCC global interrupt   | unused |                      |             |
| LPUART1 global interrupt   | unused |                      |             |
| FPU global interrupt   | unused |                      |             |

#### 8.3.2. NVIC Code generation

| Enabled interrupt Table                 | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|-----------------------------------|----------------------|------------------|
| Non maskable interrupt                  | false                             | true                 | false            |
| Hard fault interrupt                    | false                             | true                 | false            |
| Memory management fault                 | false                             | true                 | false            |
| Prefetch fault, memory access fault     | false                             | true                 | false            |
| Undefined instruction or illegal state  | false                             | true                 | false            |
| System service call via SWI instruction | false                             | true                 | false            |
| Debug monitor                           | false                             | true                 | false            |
| Pendable request for system service     | false                             | true                 | false            |
| System tick timer                       | false                             | true                 | true             |

\* User modified value

## 9. System Views

- 9.1. Category view
- 9.1.1. Current

| Middleware  |        |        |              |            |          |           |
|-------------|--------|--------|--------------|------------|----------|-----------|
| System Core | Analog | Timers | Connectivity | Multimedia | Security | Computing |
| DMA         |        |        | LPUART1      |            |          |           |
| GPIO        |        |        |              |            |          |           |
| IWDG        |        |        |              |            |          |           |
| NVIC        |        |        |              |            |          |           |
| RCC         |        |        |              |            |          |           |
| SYS         |        |        |              |            |          |           |

## 10. Docs & Resources

| Type | Link |
|------|------|
|------|------|