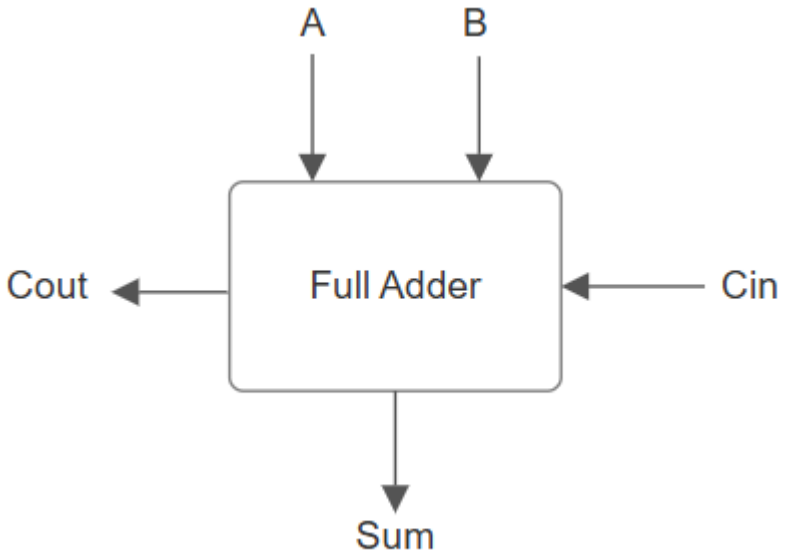
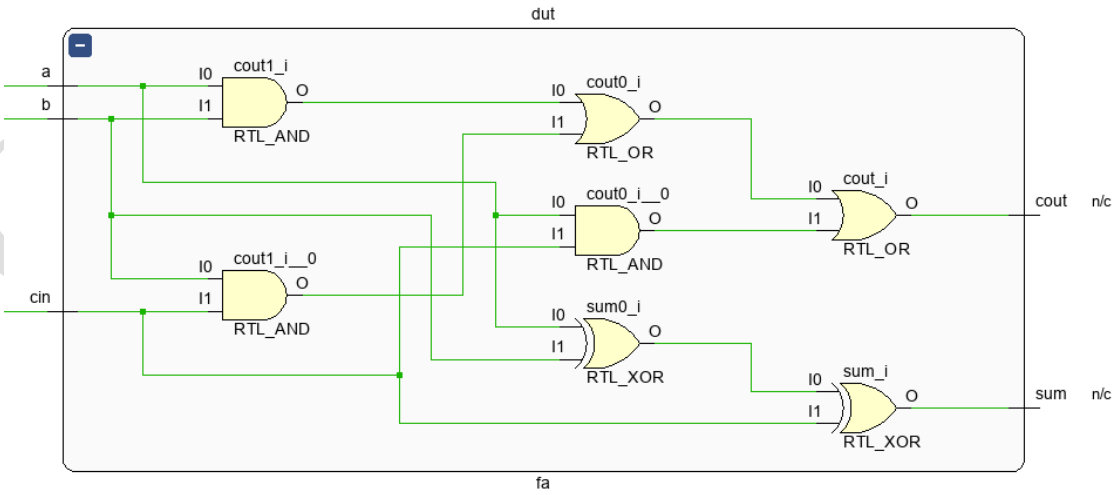
Day – 1

1. Full Adder:



Design:

```
module fa(input a,b,cin, output sum,cout);
assign sum = a^b^cin;
assign cout = a&b|b&cin|a&cin;
endmodule
```

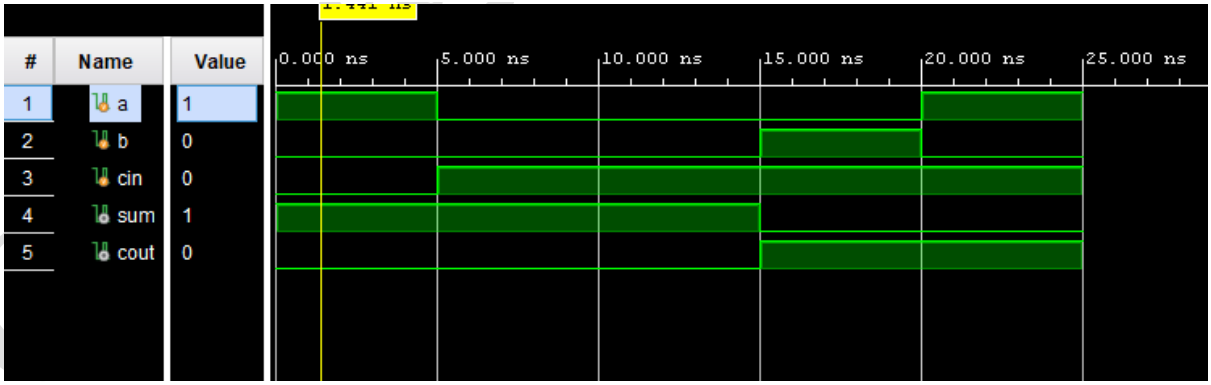


Testbench:

```
module fa_tb();

reg a,b,cin;
wire sum,cout;

fa dut(.a(a),.b(b),.cin(cin),.sum(sum),.cout(cout));

initial begin
$monitor("a=%b, b=%b, cin=%b | sum=%b, cout=%b",a,b,cin,sum,cout);
repeat(10)
begin
{a,b,cin}=$random();
#5;
end
$finish;
end
endmodule
```

Simulation:

```
# run 1000ns
a=1, b=0,cin=0 | sum=1, cout=0
a=0, b=0,cin=1 | sum=1, cout=0
a=0, b=1,cin=1 | sum=0, cout=1
a=1, b=0,cin=1 | sum=0, cout=1
$finish called at time : 25 ns : File "F:/Vivadc
INFO: [USF-XSim-96] XSim completed. Design snaps
```

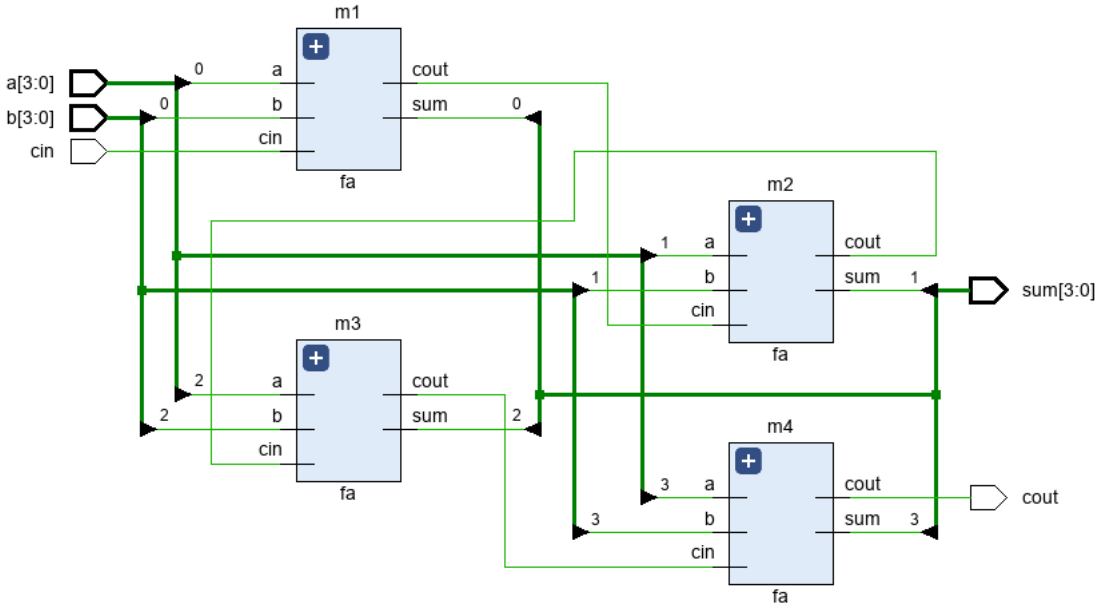


2. Ripple Carry Adder Using the Full Adder:

Design:

```
module rca(input [3:0]a, input [3:0]b, input cin, output [3:0]sum, output cout);
wire [2:0]w;
```

```
fa m1(a[0],b[0],cin,sum[0],w[0]);
fa m2(a[1],b[1],w[0],sum[1],w[1]);
fa m3(a[2],b[2],w[1],sum[2],w[2]);
fa m4(a[3],b[3],w[2],sum[3],cout);

endmodule
```



Testbench:

```
module rca_tb();

reg [3:0]a,b;
reg cin;
wire [3:0] sum;
wire cout;

rca dut(.a(a),.b(b),.cin(cin),.sum(sum),.cout(cout));

initial begin
$monitor("a=%b, b=%b,cin=%b | sum=%b, cout=%b",a,b,cin,sum,cout);
repeat(10)
begin
{a,b,cin}=$random();
#5;
end
$finish;
end
endmodule
```

Simulation:

```
# run 1000ns
a=1001, b=0010,cin=0 | sum=1011, cout=0
a=0100, b=0000,cin=1 | sum=0101, cout=0
a=0000, b=0100,cin=1 | sum=0101, cout=0
a=0011, b=0001,cin=1 | sum=0101, cout=0
a=1000, b=0110,cin=1 | sum=1111, cout=0
a=1100, b=0110,cin=1 | sum=0011, cout=1
a=0011, b=0010,cin=1 | sum=0110, cout=0
a=0000, b=1001,cin=0 | sum=1001, cout=0
a=1000, b=0000,cin=1 | sum=1001, cout=0
a=1000, b=0110,cin=1 | sum=1111, cout=0
$finish called at time : 50 ns : File "F:/Vivado/100DaysofRTL/Day3/Day3.srcs
```