A Review of the Copper Metallization Technology: The Damascene Process and Recent Trends in the Copper Metallization

**Abstract:** This review analyses the copper metallization using damascene process for electroplating and its recent trends. It is a popular method used in the manufacturing of integrated circuits. The paper presents discussion of the various techniques involved in these process. The challenges faced during its implementation, such as defects and voids are presented, and the proposed solutions to overcome these challenges are discussed. The recent advances in copper electroplating and the use of additives and pulse plating to improve the quality of the deposited copper is highlighted. The selective copper metallization for cost reduction and the use of alternative materials for interconnects is also discussed.

1. Introduction

Copper is a good alternative for ever-smaller structures since it offers many advantages over aluminum. It is more power efficient, has less resistance and has far less electromigration than Al. However, the inability of copper to be structured as easily as aluminum in dry etch techniques is one of the main drawbacks in the manufacture of ICs. In copper technology, an additive procedure known as the damascene process must be used rather than a subtractive one.

The damascene processes were developed after the attempts to build a successful Cu-etch process failed. The damascene process' principal goal is to incorporate Cu into integrated circuits (IC) in order to minimize the RC effects of the interconnects.

The damascene process eliminates the complex process of metal etching and it is a sophisticated method of inlaying metal (copper) for interconnection in integrated circuits (ICs). The damascene process is of two types: Single Damascene (SD) and Dual Damascene (DD). The simple dual damascene (DD) process differs from the simple single damascene (SD) approach as one metal deposition step and one CMP step are eliminated in the DD process (as well as the dielectric deposition step). The DD is more desirable than the twin SD process because of the reduction in the processing stages. In DD, the plugs are mostly filled with Cu and sometimes Al is also used. However, in SD process, the via holes are filled using Tungsten (W). The damascene method involves etching a trench in the dielectric layer, filling it with a barrier layer to prevent Cu diffusion, and then depositing the Cu-seed layer as the nucleation site for the electroplated Cu [1][2][3]. Subsequently, Chemical Mechanical Polishing (CMP) is used to remove the overburden metals. Although there are five principal dual damascene approaches being researched, only the key modes of trench first, via first and buried via are currently being used in commercial production.

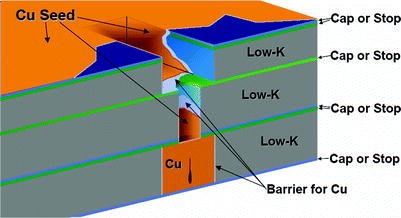


Fig. A dual damascene architecture showing the different materials in the unit structure (Photo courtesy, Peter J. Wolf)

The major advantage of the damascene process is that it has improved device performance (speed) and fine line structure by introducing borderless contact via, which addresses soft plasma processes for either dry etching, cleaning, or material deposition. Copper damascene techniques can actually create Cu-interconnecting lines that are less than 1/1000th the width of a human hair [1]. It also eliminates some of the difficult processing steps such as metal etching, IMD gap-filling and IMD CM. However, it is very expensive and its process is very complex. It is limited in its ability to produce very narrow line widths, as the process requires a minimum width to ensure proper copper deposition and polishing. This can limit the density of components that can be integrated onto a single chip and limit the usage of the process in ever decreasing semiconductor gate technology [4].

1. Past Challenges and Issues in Development

The shift from using aluminium to copper interconnects in semiconductor manufacturing had quickly accelerated over the last 3 decades. The main reasons for this shift are the fact that copper has lower resistance and is increased electromigration resistance than aluminium. There are two processes involved in the fabrication of via and line levels - dual-damascene and single-damascene. The dual-damascene process, which fabricates both levels at the same time, has about 30% fewer steps and is more cost-effective. However, there are still significant obstacles that need to be overcome before copper processing becomes a regular part of manufacturing [5].

First of all, the presence of copper contamination on the wafer's bevel and backside is a significant issue during manufacturing. The best way to address this problem is to ensure that the plating solution does not come into contact with these areas. By using this method in combination with a rinse after plating, it is possible to eliminate copper contamination effectively. Secondly, Despite the fact that many semiconductor process engineers were not familiar with electroplating, they tend to prefer more familiar methods like CVD, directional PVD, and reflow. However, because copper electroplating is less expensive, there has been a strong incentive for engineers to explore it more thoroughly. Therefore, the use of copper electroplating is becoming more widely accepted. [5]

The dual-damascene process presents new challenges for the etching process. The main issue is that the formation of trenches does not have an etch-stop point. In the fabrication of aluminum interconnects, the etching process removes the primary metal or dielectric and stops on an etch-stop material such as TiN, which helps to overcome any unevenness in the etching process within the wafer. However, in the dual-damascene process, trenches are only partially etched into the dielectric layer, and there is no etch-stop material to stop the etching process. This means that any unevenness in the etching process within the wafer directly affects the depth of the trenches, which can result in non-uniformity across the wafer. To address the issue of uneven etching in the dual-damascene process, a layered dielectric can be used. This involves depositing the oxide dielectric in two separate layers, with a thin etch-stop material such as silicon nitride in between. While this method provides a stop for the trench etch, it also increases the cost and complexity of the process. Additionally, it increases the inter-level capacitance of the interconnect stack, which partially offsets the benefits gained by using lower-resistivity copper, such as an increase in clock speed. [5]

The process of dual-damascene poses a significant challenge for lithographers. Creating trench structures over pre-existing topography (from the previous via-etch step) creates issues with resist coating, exposure, and development processes. Lithography problems may ultimately restrict the use of dual-damascene beyond one or two additional device generations, especially at lower interconnect levels where the smallest critical dimensions (CDs) are needed. [5]

Moreover, the damascene etch process becomes more difficult with each new device generation. To achieve the lowest possible inter-level capacitance within the interconnect stack, it is necessary to reduce the width of vias and lines proportionally with the decrease in transistor gate length while maintaining the maximum practical spacing between metal levels. This means that as each new device generation is introduced, the aspect ratio of the vias becomes larger, and the via etch and metal fill processes become increasingly challenging. [5]

According to experimental evidence, it has been found that physical vapour deposition (PVD) techniques, even with better flux directionality, cannot achieve copper deposition without voids. Instead, cusping (as shown in Figure 6.13b) is a common issue observed after the metal is deposited within the trench. However, it has been demonstrated that good trench filling can be achieved through reflow after sputtering.[1][6][7]

The three methods mentioned earlier (trench first, via first, and buried via) for producing damascene structures pose various difficulties. For instance, with the trench first method, it is necessary to apply resist to the trench and then create a pattern for the via within the thick resist layer. It can be challenging to open a pattern through a thick resist layer. Another challenging aspect is determining whether an intermediate etch stop (ES) layer is necessary to define the trench. Without the ES layer, the edges of the trench can be etched quickly, causing them to become rounded. However, it is also difficult to detect the actual endpoint of the process without the ES layer, which can make controlling the critical dimension (CD) and depth of the trench highly problematic. Additionally, most of the materials used for the ES layer have high dielectric constants (K), which can significantly impact the overall effective capacitance of the interconnect stack. [1]

The process of via-self alignment can be quite challenging to achieve accurate alignment between the trench and the via hole in the hard mask. Misalignment can result in the via hole being an incomplete, half-moon shape. Additionally, it is common for different dielectric materials to be used for the via level and the trench level, with the trench dielectric being more critical for capacitance. However, some low-K materials used in the via dielectric contain carbon and hydrogen, which requires adjusting the process to meet selectivity and etch requirements. The transition to the Cu-damascene process with low-K materials requires a significant change in the back-end processing, especially as the industry moves towards larger wafer sizes and smaller device geometries each year. [1]

Advanced microprocessors need multiple wiring levels, usually eight or more, to transmit signals and power between transistors and to the outside world. The dual damascene technique can make these interconnected structures by creating both a wiring level and via level at the same time, reducing the overall number of processing steps. However, the dual damascene method still requires around 20 processing steps to complete wiring. Some industries in the IC field are exploring the replacement of photolithography, which is a significant part of the damascene process, with step and flash imprint lithography (SFIL) [1][6][7].

However, the clock-speed and electromigration advantages of copper provide strong motivation to resolve all these challenges.

1. Current Challenges

Though the damascene process has been a state-of-the-art for copper electroplating, it has some significant challenges to overcome. When dual damascene copper interconnects are being integrated, the low-k materials undergo various procedures like patterning, deposition of barrier metal, and chemical mechanical polishing (CMP) which alter the material's structure and cause damage. These processes lead to an increase in the density of structural defects, alteration of the film's hydrophobicity, accumulation of metal stress and diffusion, and delamination, all of which significantly decrease the performance of dielectric reliability. However, with a stable barrier/metal system, the electrical performance can be insured [8].

One of the primary difficulties in copper damascene plating has been managing plating baths that are large in volume and contain multiple components with composition changes occurring at varying rates. Copper has unique characteristics, such as susceptibility to oxidation under normal conditions, and electroplated copper has unstable grains that require proper thermal stabilization to prevent spontaneous annealing at room temperature. The instability of the electroplated copper film also poses challenges for metrology, as thickness changes near edge contacts, structures, and regions with defects or oxidation can be significant and unpredictable. Additionally, preventing copper contamination in the fab when using common process and metrology tools for both Cu-containing and non-Cu processes is a major concern. In summary, the control of copper damascene electroplating processes has presented ongoing challenges in process control. [9]

Damascene processing has required significant development of Cu CMP. Achieving complete removal of the copper overburden and barrier layer while minimizing dishing and erosion heavily relies on the thickness and overall and local non-uniformity of the electroplated copper. Meeting the CMP requirements for global and local non-uniformity has been a continuous challenge for the copper plating process. Figure 25's surface roughness contour map revealed a clear issue in copper damascene plating - a swirl pattern. The areas with the swirl pattern showed differences in surface roughness that were attributed to trace impurity differences, which were measured using SIMS. The swirl problem was caused by surface wetting of the seed when hot entry was used. However, as depicted in Figure 2670, it was observed that the swirl pattern did not occur when cold entry was employed. [9]

To meet these requirements, quality control methods have been implemented, plater design and operation have been improved, plating electrolytes have been advanced, and new measurement tools and methods have been introduced.

1. Recent Advances

In recent years, there are attempts to reduce the overall cost of the Cu damascene process using selective electroplating. The initial experiment with selective electroplating involved using it in advanced interconnects in a Cu dual damascene integration [11]. In this process, the dielectric layer was first patterned with the desired features, followed by the deposition of the regular barrier metal and thin Cu seed layers using physical vapor deposition (PVD). Then, the surface was selectively treated before proceeding with the regular Cu electroplating process, which prevented deposition in the field areas. This made the deposition process faster and reduced the amount of time needed for CMP polishing. [10]

Adding the SCM layer as a distinct step in the process allows for independent optimization and straightforward integration into the overall process. This can be achieved at a reasonable cost, and the savings in ECD (electrochemical deposition) and CMP (chemical mechanical polishing) processes will offset the cost of including the SCM unit. Additionally, the cost of the SCM unit is expected to be much lower than that of a typical electroplating system [10].

In order to achieve void-free super-filling of high aspect ratio structures in upcoming nanoscale interconnects, it is necessary to develop better additive chemistries. However, for features smaller than 10 nanometers, simply improving the additives chemistries is unlikely to solve the challenges associated with metallizing such aggressive geometries. As technology advances beyond the 10 nanometer node, significant changes will likely be necessary in how feature metallization is approached. [12]

A review is conducted of several emerging and disruptive technologies that have the potential to offer solutions for metallization in future generations.

Direct Cu electroplating on noble liners: Conventional dual-damascene metallization typically involves using PVD Cu seed layers, which often result in overhang, meaning an excessive amount of Cu is deposited during PVD at the feature opening. This can cause uneven seed coverage and may result in pinch-off before the Cu electroplating step. This limitation hinders the feasibility of using PVD Cu seed layers in future metallization schemes. To address this problem, noble metal liners such as ruthenium (Ru) are being explored. Ru is noble, electrically conductive, and doesn't corrode in acid Cu plating baths. [12]

Currently, liners or direct plating are not utilized in semiconductor technology. Nonetheless, several major semiconductor equipment manufacturers are conducting research and development in these technologies. [12]

Electroless deposition: As mentioned earlier, achieving wafer-scale current distribution is a significant challenge in electroplating for wafer metallization. In contrast, electroless plating doesn’t necessitate an external applied current or potential. Electroless deposition involves adding soluble reductants (such as aldehydes) to the plating electrolyte, which enables Cu metal to be deposited onto a catalytically active substrate. Since there is no need for current flow through a resistive seed layer, the deposit distribution is significantly more uniform. As such, electroless deposition is a potential candidate for future 450mm wafer metallization. [12]

1. Conclusion
2. References

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