A Review of the Copper Metallization Technology: The Damascene Process and Recent Trends in the Copper Metallization

**Abstract:** This review analyses the copper damascene process for electroplating and its recent trends. It is a popular method used in the manufacturing of integrated circuits (ICs). The paper presents discussion of the various techniques involved in these process. The challenges faced during its implementation, such as defects, voids, and delamination are presented, and the proposed solutions to overcome these challenges are discussed. The recent advances in copper electroplating and the use of additives and pulse plating to improve the quality of the deposited copper is highlighted. The selective copper metallization for cost reduction and the use of alternative materials for interconnects is also discussed.

1. Introduction

Copper is a good alternative for ever-smaller structures since it offers many advantages over aluminum. It is more power efficient, has less resistance and has far less electromigration than Al. However, the inability of copper to be structured as easily as aluminum in dry etch techniques is one of the main drawbacks in the manufacture of ICs. In copper technology, an additive procedure known as the damascene process must be used rather than a subtractive one.

The damascene processes were developed after the attempts to build a successful Cu-etch process failed. The damascene process' principal goal is to incorporate Cu into integrated circuits (IC) in order to minimize the RC effects of the interconnects.

The damascene process eliminates the complex process of metal etching and it is a sophisticated method of inlaying metal (copper) for interconnection in integrated circuits (ICs). The damascene process is of two types: Single Damascene (SD) and Dual Damascene (DD). The simple dual damascene (DD) process differs from the simple single damascene (SD) approach as one metal deposition step and one CMP step are eliminated in the DD process (as well as the dielectric deposition step). The DD is more desirable than the twin SD process because of the reduction in the processing stages. In DD, the plugs are mostly filled with Cu and sometimes Al is also used. However, in SD process, the via holes are filled using Tungsten (W). The damascene method involves etching a trench in the dielectric layer, filling it with a barrier layer to prevent Cu diffusion, and then depositing the Cu-seed layer as the nucleation site for the electroplated Cu. [1,2,self]. Subsequently, Chemical Mechanical Polishing (CMP) is used to remove the overburden metals. Although there are five principal dual damascene approaches being researched, only the key modes of trench first, via first and buried via are currently being used in commercial production.

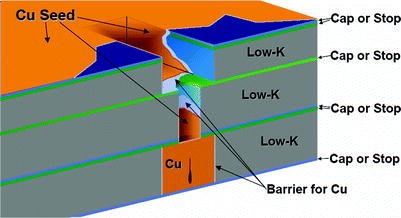


Fig. A dual damascene architecture showing the different materials in the unit structure (Photo courtesy, Peter J. Wolf)

The major advantage of the damascene process is that it has improved device performance (speed) and fine line structure by introducing borderless contact via, which addresses soft plasma processes for either dry etching, cleaning, or material deposition. Copper damascene techniques can actually create Cu-interconnecting lines that are less than 1/1000th the width of a human hair. It also eliminates some of the difficult processing steps such as metal etching, IMD gap-filling and IMD CM. However, it is very expensive and its process is very complex. It is limited in its ability to produce very narrow line widths, as the process requires a minimum width to ensure proper copper deposition and polishing. This can limit the density of components that can be integrated onto a single chip and limit the usage of the process in ever decreasing semiconductor gate technology [https://semiengineering.com/what-will-replace-dual-damascene/].

1. Past Challenges and Issues in Development

Copper is used widely for metal interconnection in ULSI due to its lower resistivity and superior resistance against electro-migration. As copper duel damascene process is complicated and critical in semiconductor wafer processes manufacturing, Cu dual-damascene interconnects with low-k dielectric structure on wafers were investigated in this study by Chun-Jen Weng [defects-1]. As metal interconnect line aspect ration, pattern density, and metal interconnect layers increased, these schemes could be more complicate and challengeable than traditional process on etching and lithography module process infrastructure.