Unit 1 Computer Evolution

Question 1

The Arithmetic and Logic Unit is the core of any_____.

Processor

Adder

Subtractor

Device

Question 2

ALU is needed to transfer data between the various_____.

Processors

Registers

Adder

Bus

Question 3

The _____ of ALU is determined by the way in which its arithmetic instructions are

Efficiency

Flexibility

Complexity

Capacity

Question 4

_____inputs tell the circuit what to do with the data inputs.

Combinational

Sequential

Control

Direct

Question 5

A typical ALU will have_____input ports and _____ result port.

1,1

1,2

2,1

2,2

Question 6

Additional output bits are together called as the _____bits.

Input

Status

Binary

Control

Question 7

The result of the computation is sent to the output labeled____.

ST

DS

SRC

DST

Question 8

_____are the commands given to the computer which tells what operation that computer should do.

Code

Memory

Instruction

Program

Question 9

In _____, the German mathematician and philosopher Gottfried Leibniz constructed a calculator that could perform multiplication and division along with addition and subtraction.

1670

1672

1671

1673

Question 10

In _____, the punch cards were developed to specify the pattern in the technology of weaving

1746

1750

1749

1748

Question 11

_____ is an electronic device that performs calculations on data, presenting the results to humans or other computers in a variety of useful ways.

Computer

Calculator

Modem

Instrument

Question 12

The group of instructions is called_____

Program

Code

Data

Procedure

Question 13

The machine used a _____ of punched paper cards.

Group

Class

Series

Bundle

Question 14

In 1801, _____ made an improvement to the textile loom.

Gottfried Leibniz

B. Pascal.

Charles Babbage

Joseph Marie Jacquard

Question 15

The only arithmetic operation performed by difference engine machine was _____.

Addition

Subtraction

Division

Multiplication

Question 16

The difference engine consist of a number of mechanical _____.

Processors

Devices

Registers

Disks

Question 17

_____ machine was designed to be a general purpose device that is capable of performing any mathematical operation automatically.

Analytical Engine

Differences Engine

Hardwired Engine

Rotational Engie

Question 18

_____is a memory unit comprising sets of counter wheels.

Mill

Store

Punch Cards

Output

Question 19

_____corresponds to a modern Arithmetic Logic Unit.

Store

Punch Cards

Output

Mill

Question 20

_____ is a printer or a card punch device so that output data is either printed on a printer or punched on cards.

Punch Cards

Output

Mill

Store

Question 21

_____constituted a computer program.

Output

Store

Punch Cards

Mill

Question 22

_____ was designed and constructed by at the Moore school of engineering .

ENIAC (Electronic Numerical Integrator and Computer)

ENIAC (Electronic Numerical Inter and Computer)

ENC (Electronic Numerical Computer)

IAC (Integrator and Computer)

Question 23

In the ___ the first two supercomputers were designed specifically for numeric processing in scientific applications.

1942

1950

1952

1960

Question 24

ENIAC was able to perform _____additions or subtractions per second.

2000

3000

5000

7000

Question 25

In _____, Dennis Ritchie developed the C language from the design of the CPL and Thompson's B.

1966

1968

1970

1972

Question 26

The microprocessor that was introduced by Intel was _____ in 1972.

Intel 8000

Intel 8005

Intel 8008

Intel 8009

Question 27

_____refers to the operational units of a computer and their interconnections, and how they implement the architecture of the system.

Organisation

Structure

Function

Computer

Question 28

Fifth generation is based on parallel processing hardware and _____ software.

C++

C

Java

Artificial Intelligence (AI)

Question 29

The smallest machines are called as _____.

Macrocomputers

Computers

Semicomputers

Microcomputers

Question 30

_____ are used for business data processing, when computing and storage capacity is larger than what the minicomputers can handle.

Miniframes

Microframes

Macroframes

Mainframes

Question 31

A _____ is a complex system that contains millions of elementary electronic components.

Computer

Modem

Calculator

Bus

Question 32

_____ defines the way in which the components of a computer are interrelated.

Structure

Function

Organization

Architecture

Question 33

_____refers to those attributes of a computer system which are visible to a programmer.

Structure

Organization

Architecture

Function

Question 34

_____ defines the operation of each individual component as a part of the structure.

Organization

Function

Structure

Architecture

Question 35

_____refers to the operational units of a computer and their interconnections, and how they implement the architecture of the system.

Structure

Architecture

Organization

Functiom

Question 36

The_____ of the bus is the number of wires in the bus.

Capacity

Memory

Size

Length

Question 37

It consists of a _____ on the horizontal line that represents it is a bus that carries more wires.

Slant Dash

Equals

Plus

Dash

Question 38

A bus allows any number of_____to hook up to the bus.

Machines

Devices

Instruments

Instructions

Question 39

____bit address bus for the CPU to specify which address to read or write from or to memory.

4

8

16

32

Question 40

Other kinds of busses that are used primarily for I/O devices like _____.

USB

Memory Device

Hardware device

Software Device

Question 41

For N devices, this requires about _____ connections, which may be too many.

N-1

N

N2

N+1

Question 42

To support two 32-bit busses, both the CPU and memory require _____ pins or

16

28

32

64

Question 43

In _____ control unit determines the address of the next instruction to be executed and loads it into program counter.

Instruction Interpretation

Instruction Sequencing

Data Instruction

Data Interpretation

Question 44

The I/O transfers are controlled by the _____ instructions that identify both the devices involved and the type of transfer.

Hardware

General

Instructional

Software

Question 45

The data transfer between a processor and the_____ is controlled by the control circuits.

Device

Memory

Microprocessor

Hardware

Question 46

The computer accepts information through the_____unit and transfers it to the memory.

Output

Control

Instruction

Input

Question 47

_____ stored in the memory is fetched into arithmetic and logic unit to perform the desired operations.

Information

Program

Data

Hardware

Question 48

Processed information is transferred to the _____unit.

Input

Output

Control

Storage

Question 49

All activities inside the machine are controlled by a _____unit.

Control

Input

Output

Storage

Question 50

ALU stands for _____.

Arithmetic Logic Unit

Arithmetic Local Unit

All Local Unit

All Logic Unit

Question 51

All instructions are stored as_____ values.

Secondary

Decimal

Octal

Binary

Question 52

A _____ is an entity that interacts in some or the other way with its external environment.

Modem

Computer

Processor

Register

Question 53

_____is the computational unit and controls the operations of the computer and performs its data processing functions.

CPU

Computer

Register

Modem

Question 54

_____ is used to store the instructions, data and the result.

Disk

Drive

Memory

I/O Interface

Question 55

_____ is used to move data from the computer and from its external environment.

Modem

Memory

Register

Input/Output Interface

Question 56

The computer system consists of _____ CPU.

Zero

Single

Double

Multi

Question 57

The bulk of the memory is stored in a separate device called RAM usually called_____.

Physical Memory

Secondary Memory

Internal Memory

Primary Memory

Question 58

Information from the secondary memory is accessed indirectly through the I/O programs that transfer the information between the main memory and _____memory.

Primary

Internal

Secondary

Physical

Question 59

Primary memory is also called as_____.

Internal Memory

External Memory

Main Memory

Primary Memory

Question 60

Memory is a large array of _____.

Bits

Bytes

Words

Groups

Question 61

Most of the memory is in _____, which can be thought of as a large array of bytes.

RAM

Hardwired Memory

External Memory

Internal Memory

Question 62

The number of bits in each word is called as _____of the computer.

Word Count

Word Length

Word Variable

Word Memory

Question 63

Addresses are the numbers used to identify _____ locations.

Alternative

Serial

Parallel

Successive

Question 64

All the I/O peripherals are _____ than CPU and RAM.

Slower

Faster

Cheaper

Expensive

Question 65

There are a wide variety of _____ which deliver different amounts of data, run at different speeds and present data in different formats.

Processors

Peripherals

Registers

Drives

Question 66

_____ is electronically connected to the processing part of a computer.

Output Device

Hardware Device

Input Device

Peripheral Device

Question 67

Computer accepts the coded information through the _____ unit.

Control

Transmission

Output

Input

Question 68

_____ unit displays the processed results.

Input

Output

Control

ALU

Question 69

A key characteristic of a bus is that it is a shared_____ medium.

Receiving

Translation

Transmission

Transparent

Question 70

The communication between the external environment and CPU is established through the System _____.

Bus

Memory

RAM

ROM

Question 71

_____ contains an address of an instruction to be fetched.

Instruction Registers

Program Counter

Storage Registers

Instruction Counter

Question 72

MAR stands for _____.

Main Address Registers

Memory Accumulator Register

Memory Address Registers

Memory And Registers

Question 73

_____ memory, which stores both instructions and data.

Main

Secondary

Primary

Internal

Question 74

_____ capable of operating on binary data.

PC

IR

MAR

ALU

Question 75

Input and Output (I/O) equipment operated by the ____ unit.

Storage

Control

Output

Input

Question 76

_____contains a word of data to be written to memory or the word most recently used.

MAR

IR

MBR

PC

Question 77

_____ is a special purpose register designated to hold the result of an operation performed by the ALU.

Program Counter

MAR

MBR

Accumulator

Unit 2 Basic Arithmetic Operations

Question 1

Booths Algorithm invented by _____.

Anil davis Booth

Andrew Donald Booth

Charles Babbage

Michael Booth

Question 2

Booth used _____ that were faster at shifting than adding and created the algorithm to increase their speed.

Scientific Calculators

Mobiles

Desk Calculators

Computers

Question 3

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in _____ complement notation.

Question 3 options:

1's

2's

3's

4's

Question 4

Booth's algorithm examines adjacent pairs of bits of the _____bit multiplier Y in signed two's complement representation.

N-1

N+1

N/2

N

Question 5

_____ point describes a method of representing real numbers in a way that can support a wide range of values.

Floating

Fixed

Decimal

Octal

Question 6

The base for the scaling is normally ___,___ or ____.

2,8,16

2,10,16

2,4,8

2,16,32

Question 7

The first part represents a signed, fixed-point number called the _____.

Exponent

Fraction

Mantissa

Floating Point

Question 8

The second part designates the position of the decimal (or binary) point and is called the _____.

Mantissa

Decimal Point

Fraction

Exponent

Question 9

The _____ and the radix-point position of the mantissa are always assumed.

Mantissa

Exponent

Fraction

Radix

Question 10

A floating-point number is said to be normalized if the most significant digit of the mantissa is _____.

Non-zero

Zero

Positive

Negative

Question 11

_____numbers provide the maximum possible precision for the floating-point number.

Positive

Negative

Normalized

Physical

Question 12

The mantissa is always a number in the range from _____.

1 to 2

1 to 3

1 to 4

1 to 5

Question 13

Floating point arithmetic is a way to represent and handle a large range of real numbers in a _____.

Decimal Form

Octal Form

Binary Form

Hexadecimal Form

Question 14

The exponent is an _____ with some special provisions for handling negative exponents .

Word

Integer

Byte

Bit

Question 15

A real number in the floating point format consists of a mantissa and an integer_____ .

Fraction

Decimal

Binary

Exponent

Question 16

The performance of _____ systems is dramatically affected by how well software designers understand the basic hardware technologies at work in a system.

Hardware

Constant

Software

Computer

Question 17

_____ designers must understand the far reaching effects their design decisions have on software applications.

Software

Computer

Application

Hardware

Question 18

The procedure of division is then repeated with the new sequence, continuing until the digits in the _____ have been exhausted.

Divisor

Dividend

Quotient

Subtrahend

Question 19

The first integrated circuit to implement the draft of what was to become IEEE

Intel 8086

Intel 8087

Intel 8088

Intel 8089

Question 20

In IEEE standards Single precision width is _____.

8 bits

16 bits

32 bits

64 bits

Question 21

In IEEE standards double precision width is _____.

64 bits

84 bits

118 bits

128 bits

Question 22

In IEEE standards single precision range is _____.

$\diamond$1.18$\diamond$10?38to $\diamond$9.2$\diamond$1038

$\diamond$1.18$\diamond$10?38to $\diamond$2.4$\diamond$1038

$\diamond$1.18$\diamond$10?38to $\diamond$8.4$\diamond$1038

$\diamond$1.18$\diamond$10?38to $\diamond$3.4$\diamond$1038

Question 23

A binary digit is called a _____.

Word

Byte

Bit

Octal

Question 24

If the minuend is larger than the subtrahend, the difference is _____.

Positive

Negative

Neutral

Positive or Negative

Question 25

Digital computers use the binary number system, which has two digits_____.

0,0

0,1

1,1

1,8

Question 26

If the minuend is_____ than the subtrahend, the difference is negative.

Larger

Equal

Lesser or equal

Smaller

Question 27

If minuend and subtrahend are equal, the difference is_____.

Positive

Negative

More than zero

Zero

Question 28

Negative of negative is_____.

Positive

Negative

Positive and Negative

Positive or Negative

Question 29

_____ is represented in digital computers in groups of bits.

Data

Instruction

Program

Information

Question 30

A shift register may be _____directional.

Uni or Bi

Uni

Bi

Uni and Bi

Question 31

Two designs for general shift registers, one using _____ and the other using _____.

D-Flip-flop,J-Flip-flop

D-Flip-flop,JK-Flip-flop

SR-Flip-flop,JK-Flip-flop

D-Flip-flop,SR-Flip-flop

Question 32

The _____ may have one or more shift registers in order to implement the different types of shifts.

PC

IR

MAR

ALU

Question 33

In a shift register with _____ input, the bits to be shifted are input one by one.

Parallel

Direct

Serial

Indirect

Question 34

The operation results in a carry if the sum (or difference) has_____ bit.

N+1

N

N-1

N/2

Question 35

_____ Algorithm indicates if the result of a signed 2's complement addition or subtraction is out-of-range.

Carry

Overflow

Shift

Slow Division

Question 36

A system known as ones' complement can be used to represent _____ numbers.

Negative

Positive

Signed

Unsigned

Question 37

The binary division is similar to the _____ division procedure.

Decimal

Octal

Primary

Secondary

Question 38

The problems of multiple representations of 0 and the need for the end-around carry are circumvented by a system called _____complement.

1's

2's

3's

4's

Question 39

Multiplication is first carried out with the LSB of the multiplicand on the multiplier _____ basis.

Word by Word

Bit by Bit

Number by Number

Byte by Byte

Question 40

Negating a number (whether negative or positive) is done by inverting all the bits and then adding_____ to that result.

1

2

3

4

Question 41

Multiplication is first carried out with the _____ of the multiplicand on the multiplier bit by bit basis.

MSB

NSB

LSB

SSB

Question 42

The ones' complement form of a negative binary number is the bitwise_____ applied to it

AND

OR

NOT

NAND

Question 43

While performing the subtraction the 1's complement of the subtrahend is obtained first and then _____to the minuend.

Added

Multiplied

Stored

Complimented

Question 44

1's complement method is useful in the sense subtraction can be carried with adder circuits of_____ of a processor.

Input

ALU

Output

Memory

Question 45

1's complement is added to the minuend, which results in a carry generation known as _____.

End Carry

Next Carry

End-Around Carry

Farward Carry

Question 46

In a computer's _____, an accumulator is a register in which intermediate arithmetic and logic results are stored.

Memory

CPU

Hardware

Screen

Question 47

Modern CPUs are typically _____ machines.

2-operand

3-operand

4-operand

2-operand or 3-operand

Question 48

The accumulator is initially set to _____, then each number in turn is read and added to the value in the accumulator.

Zero

Positive Value

Negative Value

Any value

Question 49

Access to main memory is _____ than access to a register like the accumulator because the technology used for the large main memory is slower (but cheaper) than that used for a register.

Faster

Slower

Cheaper

Expensive

Question 50

_____would add the value read from the memory location at memaddress to the value from the accumulator, placing the result in the accumulator.

Memaddress

ADD address

ADD memaddress

ADD

Question 51

The accumulator is not identified in the instruction by a register number; it is implicit in the instruction and no other register can be specified in the_____.

Instruction

Information

Program

Data

Unit 3: Central Processing Unit and Instructions

Question 1

Programs are normally written in a high-level language, which enables the programmer to use constants, local and global variables, pointers and_____.

String

Pointer

Array

Operand

Question 2

The different ways in which the location of an _____ is specified in an instruction are referred to as addressing modes.

Operation

Opcode

Options

Operand

Question 3

In _____ Addressing Mode ,single memory reference to access data.

Indirect

Register

Direct

Index

Question 4

The operand is in a memory location; the address of this location is given _____ in the instruction.

Explicitly

Implicitly

Directly

Indirectly

Question 5

Processor registers are used as temporary storage locations where the data in a register are accessed using the _____ mode.

Index

Direct

Indirect

Register

Question 6

The register or memory location that contains the address of an operand is called a _____.

Indicator

Index

String

Pointer

Question 7

Programmers use organizations called _____to represent the data used in computations.

Program

Data Structures

Computer Organisation

Data Design

Question 8

The instruction must only specify what is the operation to be performed and which is its second _____.

Operand

Operations

Opcode

Code

Question 9

As the technology allowed to move to wider data paths, it has become also possible to specify more complex _____.

Instruction Code

Instruction Format

Program Instruction

Code Format

Question 10

The main drawback is little_____in choosing the instruction set, most operations have as an operand the content of the accumulator, and this is also the place where the result goes.

Capacity

Efficiency

Flexibility

Security

Question 11

_____ specifies the operation to be performed

Source Code

Instruction Code

Operation Code

Program Code

Question 12

_____ operation may involve one or more source operands, that is operands that are the inputs for the operation.

Source Operand Reference

Result Operand Reference

Next Instruction Reference

Operation Code

Question 13

The instruction set is a programmer's means of implementation of the _____.

CPU

Program

Computer

Instruments

Question 14

CPU contains one or more registers that may be referenced by _____instructions.

CPU

Program

Sequential

Machine

Question 15

Usually the instructions are written in symbolic representations of machine code using English like language called _____.

Program

Code

Data

Mnemonics

Question 16

The address of the next instruction is handled by the _____.

Program Counter

Addressing

Instruction Format

MAR

Question 17

The layout of the instruction is called _____.

Instrction Details

Code Format

Program Format

Instruction Format

Question 18

_____ is concerned with addresses that refer to the memory other than registers.

Address Granularity

Address generation

Address Range

Address Modulation

Question 19

The designer might provide a variety of instruction formats of _____ lengths.

Same

Equal or Unequal

Different

Equal and Unequal

Question 20

A machine must have registers so that the data can be brought into the_____ for processing.

CPU

Printer

Register

Amplifier

Question 21

Each operand may require its own mode indicator or the use of indicator is limited to _____ of the address fields.

Two

Three

Four

One

Question 22

_____format is defined as the layout of bits in an instruction in terms of its constituent parts.

Code

Data

Instruction

Program

Question 23

A related consideration for the instruction length is the _____ transfer rate.

Memory

Data

Code

Program

Question 24

Almost all machines have a set of general purpose registers, with typically _____registers in it.

8

16

32

8 or 16

Question 25

International Reference Alphabet (IRA) is referred to as _____ in the USA.

ASCII

Digits

Words

Elements

Question 26

ASCII ⓒ encoded characters are usually stored and transferred as _____bits per character.

4

8

16

32

Question 27

The _____ bit may be set to 1 or 0 for even parity.

8

16

32

64

Question 28

Logical values are also called as _____ values which are 1 = true, 0 = false.

Physical

Internal

Boolean

External

Question 29

In an N-bit word, the _____ bit holds the magnitude of the numbers.

N

N+1

N-1

N/2

Question 30

In an N-bit word the N-bits holds the _____ of the numbers.

Exponent

Magnitude

Fraction

Decimal

Question 31

All machine language include _____ data types.

Alphabetic

Boolean

Numeric

Fraction

Question 32

_____is the most fundamental type of machine instruction.

Transfer of Control

Data Transfer

System Control

I/O Transfer

Question 33

If the address refers to virtual memory, translate from virtual to _____ memory address.

Actual

Internal

Physical

External

Question 34

Machines also provide a variety of operations for manipulating individual bits of a word often referred to as _____.

Bit Extension

Bit Twiddling

Bit Welding

Bit Translation

Question 35

System control instructions are reserved for the use of _____.

Operating Device

Operating System

Java

Embedded System

Question 36

_____ instructions can only be executed while the processor is in a privileged state, or is executing a program in a special privileged area of memory.

Data Transfer

Bit Extension

Bit Twidding

System Control

Unit 4 Processor Organization

Question 1 (1 point)

_____ is the portion of a machine instruction which references a peripheral device o+A90r data.

- Operation
- **Operand**
- Opcode
- Option

Question 2 (1 point)

The position of an operand value in memory space is known as the_____.

- Opcode Address
- Data Address
- Extra Address
- **Effective Address**

Question 3 (1 point)

_____ mode stresses on a rule for changing or interpreting the address field of the instruction prior to the actual reference of the operand.

- **Addressing**

- Implied
- Immediate Mode
- Relative Mode

Question 4 (1 point)

The process by which the operands are selected during program _____ is depended upon the addressing mode of the instruction.

- Fetching
- **Execution**
- Decoding
- Storing

Question 5 (1 point)

The address part in the instruction is actually the displacement needed from the instruction to the_____.

- Instruction
- Code
- **Data**
- Information

Question 6 (1 point)

The instruction (IR) contains the _____ without referring to memory.

- **Operand**
- Operation
- Opcode
- Option

Question 7 (1 point)

The_____ register's content is combined with the address portion of the instruction to acquire the EA in this mode.

- Relative
- Direct
- Register
- **Index**

Question 8 (1 point)

The Intel 8086 is a _____bit microprocessor developed by Intel.

- **16**
- 32

- 64
- 128

Question 9 (1 point)

Intel 8086 consists of_____ bit address bus.

- 18
- **20**
- 32
- 64

Question 10 (1 point)

Intel 8086 utilises _____bit data transfer bus.

- 4
- 8
- **16**
- 32

Question 11 (1 point)

Address bus carries the address of the instruction to be executed by the _____.

- Data Transfer Bus
- Address Bus
- Register
- **Processor**

Question 12 (1 point)

In order to add hardware or microcode-based floating point performance, the _____ can be connected to a mathematical coprocessor.

- 8086
- 8088
- 8089
- **8086 or 8088**

Question 13 (1 point)

The _____ CPU was the first Intel CPU to include an on-chip FPU.

- **80486**
- 80490
- 80494
- 80496

Question 14 (1 point)

_____is a coprocessor used for 8086 processor.

- 8080
- 8086
- **8087**
- 8088

Question 15 (1 point)

The _____ is a special-purpose register which is utilised by the processor to contain the address of the subsequent instruction to be implemented.

- Memory Address Register
- **Program Counter**
- Memory Data Register
- Instruction Register

Question 16 (1 point)

_____ is a two-way register which contains data accessed from memory or data awaiting storage in memory.

- Memory Address Register
- Instructional Registers
- **Memory Data Register**
- Program Counter

Question 17 (1 point)

_____ the instruction to be implemented is included in the first phase of an instruction cycle.

- **Fetching**
- Decoding
- Executing
- Reading

Question 18 (1 point)

The Control Unit of CPU forwards the decoded information in the form of a sequence of control signals to the applicable _____units of the CPU.

- Processing
- Fetching
- **Functional**
- Executing

Question 19 (1 point)

The decoder interprets the instruction when the _____has been obtained.

- Data
- **Instruction**
- Information
- Details

Question 20 (1 point)

_____register stores the instruction presently being executed.

- Data
- Segment
- **Instruction**
- General

Question 21 (1 point)

Instructional cycle process carries on, till a _____instruction comes across.

- WAIT
- STOP
- DELETE
- **HALT**

Question 22 (1 point)

Mode selection is acquired by the way the _____ is hard-wired in the circuit.

- Components
- **Chip**
- Processor
- Pointer

Question 23 (1 point)

The _____ mode is utilised for a single processor system, where 8086/8088 directly produces all the essential control signals.

- Maximum
- Medium
- **Minimum**
- Any

Question 24 (1 point)

A single microprocessor is present in the _____ mode system.

- Maximum
- **Minimum**

- Medium
- Any

Question 25 (1 point)

Transceivers are the ____directional buffers.

- Uni
- **Bi**
- Tri
- Multi

Question 26 (1 point)

The maximum mode is planned for multiprocessor systems, where an extra_____ IC is needed to produce the control signals.

- 8086
- 8088
- **Bus Controller**
- 8089

Question 27 (1 point)

Maximum mode operation is new and specially designed for the operation of the _____ arithmetic coprocessor.

- 8082
- **8086**
- 8088
- 8089

Question 28 (1 point)

Maximum mode requires an _____ bus-controller, _____ bus-controller like the 8086 arithmetic coprocessor.

- Internal,8289
- Internal,8288
- External,8289
- **External,8288**

Question 29 (1 point)

Most PCs use one microprocessor for every calculation, performing ____ instruction after another.

- **One**
- Two

- Three
- Four

Question 30 (1 point)

The parallelism technology involves _____ microprocessors cooperating simultaneously to accomplish one task.

- One
- Two
- Three
- **Multiple**

Question 31 (1 point)

Parallelism can increase the operating time of battery-powered computers by _____ the power consumption.

- Increasing
- **Decreasing**
- Same
- Different

Question 32 (1 point)

_____ in many computer applications critically dependent on the speed of arithmetic operations.

- Efficiency
- Function
- Data
- **Performance**

Question 33 (1 point)

Computer arithmetic covers methods of representing integers and real values in _____systems and effective algorithms for controlling such numbers by way of software or hardware circuits.

- Analog
- Positive
- Negative
- **Digital**

Question 34 (1 point)

Floating point numbers are approximations of real numbers, and because arithmetic has limited precision, floating point addition is_____.

- **Non-Associative**
- Commutative
- Associative
- Non-Commutative

Question 35 (1 point)

The field that deals with such issues is called _____ analysis.

- Alphabetical
- Stastical
- Logical
- **Numerical**

Question 36 (1 point)

_____ is the most visible component of the CPU.

- **Register Set**
- Memory Space
- Flag
- Pointer

Question 37 (1 point)

General purpose registers can be _____ order.

- Smaller and Bigger
- **Lower and Higher**
- Positive and Negative
- Zero

Question 38 (1 point)

The _____ chips have a set of on-board powerful set of registers.

- **80x86**
- 80x88
- 86x88
- 86x89

Question 39 (1 point)

The 8086 processor utilises the segment registers to retrieve blocks of memory known as _____.

- Blocks
- Groups
- **Segments**

- Columns

Question 40 (1 point)

The _____ registers SI and DI are used for offset storage in certain types of addressing modes.

- General
- Program
- **Index**
- Segment

Question 41 (1 point)

The flags register is a _____bit register called EFLAGS.

- 16
- **32**
- 64
- 128

Question 42 (1 point)

The flags operate particular operations and depict the _____ of the 80386.

- Value
- Code
- **Status**
- Method

Question 43 (1 point)

Read Cycle is Data Transfer from Memory or Input/Output to _____.

- **CPU**
- External Device
- Internal Device
- Memory

Question 44 (1 point)

The processor starts a read bus cycle by floating the address of the memory location on the _____ lines.

- Control
- Data
- **Address**
- Input

Question 45 (1 point)

The _____subsystem decodes the address and puts the data on the data lines.

- Address
- **Memory**
- Data
- Control

Question 46 (1 point)

The processor cancels out the _____, giving a signal that the data is not valid anymore.

- Data address
- Data Signal
- Data Pin
- **Data Strobe**

Question 47 (1 point)

The processor sets the Read/Write signal to low for a _____ operation.

- Read
- Execute
- **Write**
- Decode

Question 48 (1 point)

The processor sets the Read/Write signal to high for a _____ operation.

- **Read**
- Write
- Decode
- Execute

Question 49 (1 point)

_____ also cancels out the address strobe signal.

- CPU
- Register
- Decoder
- **Processor**

Question 50 (1 point)

How many general purpose registers are there in 8086?

- **8**
- 12

- 16
- 24

Question 51 (1 point)

There are two special purpose registers on the 8086 CPU, the _____ register and the _____ pointer .

- Base,Instruction
- Segment, Flag
- Code ,Base
- **Flag, Instruction**

Question 52 (1 point)

8086 processor consists of eight _____ bit general purpose registers which are named as:ax, bx, cx, dx, si, di, bp, and sp

- 8
- **16**
- 32
- 64

Question 53 (1 point)

The _____ register is known as the accumulator.

- BX
- **AX**
- **AX**
- **AX**

Question 54 (1 point)

The sp register stands for the_____ Pointer.

- String
- Segment
- **Stack**
- State

Question 55 (1 point)

_____is utilised for on-chip debugging.

- Sign Flag
- Overflow Flag
- Auxiliary Flag
- **Trap Flag**

Unit 5 Control Unit Design

Question 1

_____ are used to move data between the registers and ALU.

Control Unit

External Data Path

Internal Data Path

Any Data Path

Question 2

The control unit uses _____ to maintain the timings.

Cycle

Clock

Flag

Parity

Question 3

_____ are needed by the control unit to determine the status of the CPU.

Clock

Cycle

Flags

Parity

Question 4

The control unit must have the logic required to perform _____ and execution functions.

Decoding

Storing

Fetching

Sequencing

Question 5

The control unit causes _____ micro-instruction per clock cycle.

Zero

Negative

Positive

One

Question 6

Control signals to logic that adds _____ to the contents of the PC and stores the result back in the PC.

1

2

3

4

Question 7

_____ is the control unit controls the internal flow of data.

Control Paths

Address Paths

Data Paths

Information Paths

Question 8

MAR and MDR registers communicate with main memory through address bus and_____bus.

Data

Control

Information

Direct

Question 9

Registers ____ and _____are used only by the CPU for temporary storage during execution of some instructions.

Si,Di

Ax,Bx

Y,Z

Cx,Dx

Question 10

The transfer mechanism where one device initiates the transfer and waits until the other device responds is called _____ transfer.

Asynchronous

Synchronous

Direct

Indirect

Question 11

A memory operation can be completed in _____ clock cycle.

Zero

Negative

One

Two

Question 12

The signals for the corresponding speed names are set to ____, for the signal corresponding to that step, and all other signals are inactive.

-1

0

1

2

Question 13

The _____ designs enable faster data transfers than the open controller approach.

One State

Three State

Four State

Five State

Question 14

If open controller arrangement is used, the three state output gate is replaced by an open controller _____ gate.

NAND

OR

AND

XOR

Question 15

_____ is achieved by replacing the current contents of the PC by the branch address.

Coding

Dividing

Branching

Encoding

Question 16

An alternative arrangement for the single bus organization is the _____.

Three bus

Single bus

Two bus

Multiple bus

Question 17

The time or clock for execution of a single instruction is called an _____ .

Instruction Cycle

Instruction Register

Instruction Code

Information Cycle

Question 18

_____holds last instruction fetched.

Instruction Code

Instruction Cycle

Information Cycle

Instruction Register

Question 19

Each smaller cycles involves a series of steps called _____.

Flow Chart

Micro Operation

Macro Operation

Mini Operations

Question 20

_____ holds address of next instruction to be fetched.

Instruction Counter

Instruction Cycle

Instruction Register

Program Counter

Question 21

The_____ field of the instruction is transferred to the MAR.

Data

Control

Register

Address

Question 22

The flow chart of all the sequence of _____ operations is tied up together.

Micro

Macro

Equal

Maximum

Question 23

ICC code for execute state is _____.

10

0

1

11

Question 24

The CPU must generate the control signals in the _____.

Improper Sequence

Proper Sequence

Processor Sequences

Improper Order

Question 25

In a hardwired implementation, the control unit is essentially a _____ circuit.

Sequential

Combinatorial

Combinational

Ordered

Question 26

The key inputs to the control unit are IR, clock, Flags, and _____bus.

Address

Data

Control

Single

Question 27

_____ issues repetitive sequence of pulses.

Cycle

Clock

Flag

Control

Question 28

_____program memory is a special memory in which the micro routines corresponding to the instruction set of a computer are stored.

Macro

Medium

Micro

Mini

Question 29

The control signals are loaded into various parts of the_____in the correct sequence.

Memory

CPU

Register

Processor

Question 30

The micro program defines the_____set of a computer.

Program

Data

Information

Instruction

Unit 6 Memory Organization

Question 1

The CPU requires its own local memory in the form of _____.

Registers

Processors

Array

String

Question 2

Data are generally stored in units called _____.

Blocks

Groups

Rows

Records

Question 3

In _____ memory information decays naturally or is lost when electrical power is switched off.

Non-Volatile

Volatile

External

Internal

Question 4

Capacity is one of the important aspects of the _____.

Register

Processor

CPU

Memory

Question 5

_____ is the natural unit of organisation of memory.

Word Count

Word Length

Word Block

Word Size

Question 6

A block may contain a _____ of data.

Group

Block

Unit

Portion

Question 7

Cycle time is applied to ____.

ROM

Read Memory

Write Memory

RAM

Question 8

_____ requires periodic refreshing.

DRAM

PROM

ROM

SRAM

Question 9

In which memory organisation, the bits of a particular word, are spread across multiple chips?

2 D

2 1/2 D

3 D

4 D

Question 10

The minimum time delay between two successive memory operations is called _____.

Internal Memory Time

External Memory Time

Memory Cycle Time

External Cycle Time

Question 11

A DRAM memory cell uses a single transistor and a _____ to store a bit of data.

Register

LED

Processor

Capacitor

Question 12

The bulk of a modern processor's memory is composed of _____chips.

SRAM

RAM

ROM

DRAM

Question 13

To write information into the cell, a voltage signal is applied to the _____ line.

Data

Address

Control

Register

Question 14

Dynamic nature of the chips are completely invisible to the user; such chips are known as_____

Pseudo Dynamic

Static State

Pseudo Static

Dynamic State

Question 15

_____memories are used only when the very fast operation is required.

Unipolar

Bipolar

Tripolar

Non-Polar

Question 16

If memory access requests are made for consecutive addresses, then the access will be made for _____ modules.

Same

Similar

Different

New

Question 17

When an instruction FETCH is issued by the processor, a memory access circuit creates four consecutive addresses and places them in _____ MARs.

Two

Four

Six

Eight

Question 18

One may combine interleaving and cache to reduce the speed mismatch between the _____ memory and main memory

Primary

Cache

Secondary

Tritary

Question 19

When a cache miss occurs, the block that contains the desired word must be copied from the_____ memory into the cache.

Secondary

Tritary

Main

Primary

Question 20

If a single memory is used, then the time needed to load the desired block into the cache is _____cycles.

28

38

42

46

Question 21

The memory is built with DRAM chips that allow the first word to be accessed in 8 clock cycles, but subsequent words of the block are accessed in _____ clock cycles per word.

1

2

3

4

Question 22

To perform a Write operation, the information at the data input DI is given to the _____.

Column Decoder

Column Encoder

Row Decoder

Row Encoder

Question 23

The main purpose of the refresh circuit is to maintain the integrity of the stored contents of the _____.

Block

Cell

Row

Group

Question 24

A single static memory chip has a control input called _____.

Static Select

Dynamic Select

Chip Select

Normal Select

Question 25

The R / W inputs are given to all chips which provide common Read / Write_____.

Lines

Components

Control

Blocks

Question 26

The main purpose of the refresh circuit is to maintain the_____ of the stored information.

Density

Integrity

Storage

Flexibility

Question 27

Application of a _____address causes cells on the corresponding row to be read and refreshed during both reading and writing operations.

Column

Line

Row

Block

Question 28

_____program memory is a special memory in which the micro routines corresponding to the instruction set of a computer are stored.

Macro

Medium

Micro

Mini

Question 29

The control signals are loaded into various parts of the_____in the correct sequence.

Memory

CPU

Register

Processor

Question 30

The micro program defines the_____set of a computer.

Program

Data

Information

Instruction

Unit 7 High Speed Memories

Question 1

The rate at which the CPU can execute instructions is limited by the _____.

Memory Cycle Time

Processor Cycle Time

Register Cycle Time

Cycle Time

Question 2

The collections of tags which are currently assigned to the cache are stored in a special memory, called the cache _____.

Main Memory

Primary Memory

System Memory

Tag Memory

Question 3

The solution is to exploit the principle of the locality by providing a small, fast memory between the CPU and the main memory. This memory is known as _____memory.

Primary

Secondary

Tritary

Cache

Question 4

The number of lines (C) of cache is _____than the number of main memory blocks (M).

Greater

Little Lesser

little greater

Less

Question 5

The correspondence between the main memory and CPU are specified by a _____.

Instruction

Mapping Function

Macro Operation

Program Operations

Question 6

In _____ technique block K of the main memory maps onto block K modulo 128 of the cache.

Indirect Mapping

Associative Mapping

Block Set Associative mapping

Direct Mapping

Typical block size is ____ to _____ words.

2, 18

32, 64

24, 32

4, 16

Question 8

The purpose of reading a block from main memory is that it is likely that future references will be to other words in the _____.

Block

Cell

Group

Row

Question 9

The main memory address can be divided into three fields such as___, _____ and _____.

FIELD, TAG and WORD

TAG, BLOCK and CELL

TAG, GROUP and CELL

TAG, BLOCK and WORD

Question 10

Data is stored in block regions which is an angular part of a track and is referred as a _____.

Sector

Track

Platter

Head

Question 11

_____ is the time required to move the disk arm (head) to the required track.

Access Time

Seek Time

Transfer Time

Rotational Delay

Question 12

_____ is a set of physical disk drives viewed by the operating system as a single logical drive

RAM

ROM

RAID

PROM

Question 13

_____are recorded on and later retrieved from the disk via a conducting coil named the head.

Attribute

Element

Instruction

Data

Question 14

_____is time required to rotate the disk to get wanted sector beneath the head.

Transfer Time

Access Time

Seek Time

Rotational Delay

Question 15

Data are distributed across the physical drives of an _____.

Array

Register

String

Processor

Question 16

Redundant disk capacity is used to _____parity information, which guarantees data recoverability in case of a disk failure.

Fetch

Decode

Store

Execute

Question 17

In a _____environment each user will have a separate user space with a separate page table.

Singleuser

Multiuser

Nonuser

System user

Question 18

In virtual memory concept we assumed that _____ large program is being executed.

No

More Than One

Only One

Two

Question 19

Management routines are the parts of the_____ of the computer.

Hardware

Operating System

Software

Memory

Question 20

The _____ main memory is thus shared by the active pages of the system space and several user spaces.

Logical

Physical

Virtual

Processor

Question 21

Virtual address space is divided into two parts system space and _____space.

Memory

Client

User

Server

Question 22

Paging is more efficient than _____.

Virtualisation

Partitioning

Framing

Processing

Question 23

Programs are divided to "logical" chunks known as "pages", assigned to available chunks of memory known as _____.

Page Table

Page Selection

Page Layout

Page Frames

Question 24

A set of virtual addresses constitute the _____.

Virtual Address Space

Physical Address Space

Local Address Space

Logicall Address Space

Question 25

The simplest method of translation assumes that all programs and data are composed of fixed length units called _____.

Memory

Pages

Segment

Layout

Question 26

Page normally ranges from 1K to _____ bytes in length.

8K

80K

800K

8000K

Question 27

Information about the disk or the main memory is kept in a_____in the main memory.

Page Counter

Page Layout

Page Table

Page Address

Question 28

The starting address of the table is kept in a page table _____ register.

Code

Segment

Base

Index

Question 29

One _____ bit indicates whether the page has been modified when it was in the main memory.

Address

Control

Data

Clock

Question 30

Virtual memory _____ the effective size of the main memory.

Decreases

Maintains

Increases

Changes

Unit 8 Secondary Memory

Question 1 (1 point)

First Digital Audio Tape (DAT) introduced in _____Year.

- 1987
- 1988
- 1990
- 1992

Question 2 (1 point)

DDS stand for_____.

- Dual Data Storage
- Digital Data Storage
- Digital Device Storage
- Digital Data Schema

Question 3 (1 point)

Computer data storage medium is a sequential-access medium and is commonly used for _____.

- Storage
- Data Accessing
- Backups
- Analysing

Question 4 (1 point)

DAT _____ remained relatively expensive, and commercial recordings were not made available on the format.

- Devices
- Element
- Components
- Recorders

Question 5 (1 point)

DAT _____are capable of reading the audio data from a DAT cassette.

- Object
- Device
- Records
- Drive

Question 6 (1 point)

The format saw moderate success in professional markets and as a computer_____ medium.

- Storage
- Backup
- Analysis
- Primary

Question 7 (1 point)

DAT has the ability to record at higher, equal or lower sampling rates than a CD at ____bits quantisation.

- 8
- 12
- 16
- 20

Question 8 (1 point)

A device that stores computer data on magnetic tape is a _____.

- Drive
- Device
- Object
- Component

Question 9 (1 point)

Magnetic tape was first used to record computer data in _____.

- 1921

- 1930
- 1943
- 1951

Question 10 (1 point)

Devices that record and play back audio and video using magnetic tape are tape recorders and _____tape recorders.

- Audio
- Video
- Macro
- Mini

Question 11 (1 point)

A major difference is that video signals use _____bandwidth than audio signals.

- Less
- Same
- Zero
- More

Question 12 (1 point)

Recording density was 128 characters per inch on _____ tracks.

- Five
- Six
- Seven
- Eight

Question 13 (1 point)

Tape remains a viable alternative to disk in some situations due to its lower cost per _____.

- Bit
- Byte
- Group
- Word

Question 14 (1 point)

The tape has historically offered enough advantage in _____over disk storage to make it a viable product, particularly for backup, where media removability is necessary.

- Efficiency
- Performances
- Speed

- Cost

Question 15 (1 point)

CD ◆ Rom stands for_____.

- Compact Drive Read-Only Memory
- Compact Disk Read-Only Memory
- Compact Disk Refer-Only Memory
- Compact Disk Read-Of Memory

Question 16 (1 point)

DVD stands for _____.

- Drive Verse Disk
- Drive Versatile Disk
- Digital Versatile Disk
- Drive Verse Data

Question 17 (1 point)

Can be written to and erased multiple times with _____.

- CD Read
- CD Rewritable
- DVD Rewritable
- CD Refer

Question 18 (1 point)

Spiral spacing on a DVD _____distance between pits _____.

- 0.64um, 0.4um
- 0.74um, 0.4um
- 0.84um, 0.4um
- 0.74um, 0.2um

Question 19 (1 point)

_____ were selected by using the deflection coils in the CRT to pull the beam into position in front of the cell, lighting up the front of the tube in that location.

- Blocks
- Units
- Cells
- Groups

Question 20 (1 point)

Spiral spacing on a CD is _____, distance between pits is _____.

- 1.2um, 0.84um
- 1.6um, 0.834um
- 1.9um, 0.8um
- 1.9um, 0.2um

Question 21 (1 point)

Blank recordable DVD discs can be recorded once using a DVD recorder and then function as a _____.

- DVD-RAM
- DVD-PROM
- CD-ROM
- DVD-ROM

Question 22 (1 point)

RAID stand for _____.

- Redundant Array of Independent Disks
- Recall Array of Independent Disks
- Redundant Array of Independent Drives
- Redundant Array in Disks

Question 23 (1 point)

SNIA stands for_____.

- Secured Networking Industry Association
- Storage Networking Industry Association
- Segment Networking Industry Association
- Storage Networking Industry Authority

Question 24 (1 point)

Block-level striping with dedicated parity _____.

- RAID 4
- RAID 5
- RAID 6
- RAID 7

Question 25 (1 point)

Block-level striping with distributed parity_____.

- RAID 3
- RAID 4
- RAID 5
- RAID 6

Question 26 (1 point)

Block-level striping with double distributed parity_____.

- RAID 4
- RAID 5
- RAID 6
- RAID 7

Question 27 (1 point)

_____ is calculated across corresponding bytes and stored on a dedicated parity drive.

- Address
- Parity
- Analysis
- Capacity

Question 28 (1 point)

Each drive operates independently, allowing I/O requests to be performed _____.

- Serial
- Equally
- Parallel
- Differently

Question 29 (1 point)

One _____ bit indicates whether the page has been modified when it was in the main memory.

- Address
- Control
- Data
- Clock

Question 30 (1 point)

Virtual memory _____ the effective size of the main memory.

- Decreases
- Maintains
- Increases
- Changes

Unit 9 IO Organization

Question 1

I/O operations are accomplished through a wide assortment of external devices that provide a means of exchanging data between the _____ environment and the computer.

External

Internal

Explicit

Implicit

Question 2

The link is used to exchange control, _____and data between the I/O module and the external device.

Address

Status

Link

Memory

Question 3

_____readable is suitable for communicating with the computer user.

Machine

Device

Human

Any

Question 4

_____readable is suitable for communicating with equipments.

Human

Component

Device

Machine

Question 5

The _____ converts the data forms from electrical signals into other forms of energy or vice versa.

Transmitter

Transformer

Translator

Transducer

Question 6

_____ logic associated with the device controls the device operation in response to the direction from the I/O module.

Control

Alphabetic

Arithmetic

Machine

Question 7

A_____ is associated with the transducer to temporarily hold the data being transferred between the I/O module and external devices.

Peripherals

Processor

Buffer

Register

Question 8

I/O memory must have an interface to CPU and _____.

Memory

External Device

Internal Device

Register

Question 9

I/O module gets _____from device.

Memory

Data

Attribute

Code

Question 10

_____ are exchanged between the CPU and the I/O module over the data bus.

Data

Communication

Processor

Registers

Question 11

I/O module can report with the status signals. Commonly used status signals are _____.

STOP or WAIT

READY or WAIT

BUSY or READY

WAIT or BUSY

Question 12

I/O module must be recognised with a_____address for each peripheral it controls.

Different

Related

Unique

Unrelated

Question 13

A program monitors SIN, and when SIN is set to _____, the processor reads the contents of DATAIN.

0

1

2

Negative

Question 14

The buffer registers DATAIN, and DATAOUT and the status flag SIN and SOUT are part of circuitry commonly known as a _____interface.

Drive

Disk

Device

Component

Question 15

The buffer registers DATAIN, and DATAOUT and the status flags SIN and SOUT are part of circuitry commonly known as a _____.

Drive interface

Data interface

Device interface

Disk interface

Question 16

Priorities may be used to control the nesting of _____.

Information

Interrupts

Data

Attributes

Question 17

The _____ checks periodically to determine if an interrupt signal is pending.

Hardware

Software

CPU

Processor

Question 18

The concept of interrupts is useful in operating systems and in many control applications where processing of certain routines has to be accurately timed about the _____events.

Internal

Implicit

External

Explicit

Question 19

When one acknowledges_____ that it originated the interrupt, then that device is serviced.

Negatively

Positively

Equally

Zero

Question 20

_____ are assigned to device interfaces on the basis of any of several factors.

Parity

Process

Peripheral

Priorities

Question 21

The CPU pushes the program counter and the Program Status Word onto the _____.

Stack

Array

String

Process

Question 22

_____ of this instruction results in the same actions as when a hardware interrupt request is received.

Fetching

Decoding

Storing

Execution

Question 23

There are wide varieties of peripherals with a variety of operation _____.

Methods

Structures

Types

Classes

Question 24

The need of I/O Module is impractical to incorporate the necessary logic within the _____ to control a range of devices.

Hardware

Software

Processor

CPU

Question 25

The data transfer rate of peripherals is often much_____ than that of the memory or CPU.

Faster

Slower

Wider

Different

Question 26

Peripherals often use different data formats and word_____ than the computer system to which they are attached.

Count

Format

Cell

Length

Question 27

Interface to the CPU and memory via the _____or central switch.

System Switch

Central System

Switch Bus

System Bus

Question 28

Interface to one or more peripheral devices by tailored _____ links.

Data

Control

Address

Switch

Question 29

The I/O module does not take any further action to_____ CPU that is it does not interrupt CPU.

Wait

Alert

Read

Write

Question 30

A _____ command causes the I/O module to obtain an item of data from the peripheral and place it in an internal buffer.

Write

Wait

Read

Alert

Question 31

A _____command causes the I/O module to take an item of data from the data bus and subsequently transmit the data item to the peripheral.

Read

Write

Alert

Wait

Question 32

Data is read in one _____ at a time.

Byte

Word

Bit

Hexa

Question 33

The _____ operation is usually implemented by two machine instructions.

Interrupt

Data

Branch

Parity

Question 34

The _____instruction tests the state of one bit in the destination location, where the bit position to be tested is indicated by the first operand.

Out Status

Test Bit

Data Out

Data In

Question 35

The first instruction tests the_____ and the second performs the branch.

Internal Flag

External Flag

Parity Flag

Status Flag

Unit 10 IO - Data Transfer

Question 1

A bus is asynchronous when data transfer on the bus depends upon the _____ of the data and not on a clock signal.

Quality

Accessibility

Range

Amount

Question 2

Synchronous buses are simple and are also easy to_____.

Modify

Execute

Implement

Understand

Question 3

In asynchronous bus data transfer on the bus is monitored by a bus _____.

Cycle

Clock

Parity

Signal

Question 4

Control buses are used to transmit _____.

Analog Signal

Control Signal

Digital Signal

Address Signal

Question 5

_____ bus transmit the memory address.

Power

Data

Address

Control

Question 6

_____ buses transmit the power-supply/ground voltage.

Data

Power

Address

Control

Question 7

Data buses are used to ____ data.

Internal Flag

External Flag

Parity Flag

Transmit

Question 8

The I/O handling procedure will require some status information from the _____device

I/O

Input

Output

External

Question 9

The word _____ is often used to refer to the buffer itself.

Pin

Port

I/O pin

I/O Port

Question 10

Program controlled I/O is often used for simple operations which must be performed _____.

Combinationally

Seperatly

Sequentially

Alternatively

Question 11

The main disadvantage of program-controlled I/O is that a great deal of time may be spent testing the status inputs of the I/O devices when the devices do not need _____.

Changes

Modification

Conectivity

Servicing

Question 12

It is relatively easy to add or delete _____.

Options

Disks

Devices

Drives

Question 13

A_____is the name given to a connection to an I/O device.

Link

Port

Connection

I/O Connection

Question 14

The key concept in I/O software designing is_____ achieved by using uniform naming.

Device Independence

Device Dependence

Drive Independence

Drive Dependence

Question 15

Data transfer between the I/O devices and the central computer may be tackled in_____ modes.

No

Single

Double

Several

Question 16

Few modes utilise the CPU as an intermediate path, while others transfer the data straight to and from the memory unit, with no intervention of CPU just as in _____.

IOP

DMA

IMA

Direct Access

Question 17

The CPU implements programs that begin, direct and end a _____operation.

Input

Output

Deleting

I/O

Question 18

In both programmed I/O as well as interrupt driven I/O, CPU is in charge of reading data from the_____as well as writing data into the_____.

Memory,Device

Drive,Memory

Drive,Drive

Memory,Memory

Question 19

The I/O module is able to _____ data from/in the memory.

Store

Retrieve

Store or Retrieve

Copy

Question 20

Data transfer to and from peripherals can be performed in _____ modes.

3

4

5

6

Question 21

When a large quantity of data is to be transferred from CPU, a _____ can be utilised.

DMA Module

DMA Page

DMA Design

DMA Method

Question 22

In both Programmed and Interrupt driven I/O, the CPU is busy in implementing_____ instructions.

Input

Input/Output

Output

Read

Question 23

In majority mini- and main-frame computer systems, a great deal of input and output happens between the _____ and the disk system.

Drive

Device

Processor

Memory

Question 24

I/O performed in such a manner is generally called _____.

Indirect Memory Access

Indirect Media Access

Direct Media Access

Direct Memory Access

Question 25

_____the DMA controller maintains control of the bus till the entire data has been moved to (from) memory from (to) the peripheral device.

On

Off

Burst Mode

Single Cycle Mode

Question 26

In _____ (cycle stealing), the DMA controller gives up the bus following every transfer of single data word.

Single Cycle Mode

Burst Mode

Arithmetic

Machine

Question 27

If the data to be transferred is in bulk then _____ technique is the best choice as it increases the data transfer speed.

Direct Access

IOP

DMA

Memory Access

Question 28

In case varied data_____ happen to be exchanged, the interface should be able to transform serial data to parallel form as well as vice-versa.

Information

Interrupts

Data

Attributes

Question 29

The reason behind the communication link is to solve the differences which exist between every peripheral and the _____computer.

Super

Mini

Central

Mainframe

Question 30

Peripherals linked to a computer need special communication connections for interfacing them along with the _____.

CPU

Disk

Drive

Hardware

Question 31

In all general-purpose computers, the terminal, magnetic disk and _____ are utilised.

Keyboard

Mouse

Drive

Printer

Question 32

The magnetic _____ is used for backup storage in computers.

Disk

Drive

Tape

Device

Question 33

We release a _____ command to make the peripheral active.

Status

Control

Data Input

Data Output

Question 34

We utilise a _____ command to check several status conditions in the peripheral and the interface.

Control

Data Input

Data Output

Status

Question 35

The 8237 is a DMA Controller that provides the memory as well as I/O with memory address information and control signals at the time of the _____.

DMA Transfer

DMA Request

DMA Response

DMA Process

Question 36

PCI bus was initially created as a local bus expansion for the _____ bus.

ISA/ESA

ISA/EISA

ISA/EIS

EIS/ISA

Question 37

ISA stands for _____

Indian Standard Architecture

Industry Set Architecture

Industry Standard Architecture

Industry Secured Architecture

Question 38

The initial version of the PCI bus performed at _____ with a 32-bit bus (133MBps).

20MHz

24MHz

30MHz

33MHz

Question 39

The PCI bus performs either asynchronously or synchronously along with the motherboard _____ rate.

Clock

Cycle

Noise

Period

Question 40

PCI will permit a bus master to move data at the _____ allowable rate.

Minimum

Maximum

Zero

Normal

Question 41

The PCI bus utilises its personal internal interrupt system for handling the_____ from the cards on the bus.

Response

Argument

Request

Statement

Question 42

PCI gives support to full device_____mastering.

Peripheral

Register

Processor

Bus

Question 43

_____should be present at the very ends of the bus, subsequent to all the real devices on the chain.

Terminators

Transmitters

Enders

Transducers

Question 44

Reflected signals intrude with the "real" data on the bus and cause data corruption and _____.

Noise Corruption

Signal Corruption

Signal Loss

Noise Loss

Question 45

In the initial SCSI arrangement, synchronous communication permitted speeds till_____.

2Mb/sec

3Mb/sec

4Mb/sec

5 Mb/sec

Question 46

SCSI utilises a 3-bit addressing scheme, in which every device is designated an address varying from_____.

0 to 5

0 to 7

0 to 9

0 to 12

Question 47

Terminators can be either _____ terminators or _____ terminators.

InternaI, External

Implicit,Explicit

Farward, Backward

Positive , Negative

Question 48

The host computer is normally designated to be _____.

Device 3

Device 5

Device 7

Device 9

Question 49

ANSI X3.131 – 1986 is the official name of the_____ standard.

ANSI

SCSI

ASCII

PCI

Question 50

Serial I/O 8251 contains_____ duplex double buffered system.

Half

More than half

Full

Overflow

Question 51

_____communication is mostly used while transmitting the data over a long distance.

Serial

Parallel

Alternative

Direct

Question 52

Serial I/O 8251 one bit at one time over a_____ line.

Zero

Single

Double

Multiple

Question 53

Serial I/O 8251 is also called _____ chip.

Universal Synchronous Asynchronous Receiver Transducer(USART)

Universal Synchronous Asynchronous Recorder Transmitter (USART)

Uniform Synchronous Asynchronous Receiver Transmitter (USART)

Universal Synchronous Asynchronous Receiver Transmitter (USART)

Question 54

Synchronous baud rate of serial I/O 8251 is _____ baud .

0-16k

0-32k

0-64k

0-128k

Question 55

Asynchronous baud rate of serial I/O 8251 is _____ baud.

0-19k

0-18k

0-18.2k

0-19.2k

Question 56

Serial I/O 8251 has_____DIP package.

16pin

28pin

32pin

36pin

Question 57

0

Electrical Indian Association

Electronic Industries Association

Electrical Industries Association

Electronic Indian Association

Question 58

A wire exists for every signal, along with the _____signal.

Ground

Analog

Digital

Positive

Question 59

Very high data rate is possible by use of _____ signalling.

Similar

Positive

Differential

Negative

Question 60

The differential signalling uses very small amount of _____ which saves power.

Current

Noise

Amplitude

Voltage

Question 61

A signal resting on a single line is not possible to screen efficiently for _____.

Noise

Current

Voltage

Amplitude

Question 62

_____ levels with relation to ground signify the RS-232 signals.

Current

Voltage

Amplification

Serial

Question 63

The _____ ports on the majority of the computers utilise a subset of the RS- 232C standard.

Parallel

Alternative

Serial

Combinational

Question 64

Majority of the operations and actions which occur in computers are carefully controlled and happen at particular_____and_____.

Time and Cycle

Time and Interval

Interval and Version

Version and Cycle

Question 65

In synchronous data transmission, data is transmitted though a bit-stream, that transmits a group of characters in a _____ stream.

Single

Double

Multiple

Zero

Question 66

Data transfer, the transmission speed is synchronised at both the sender and receiver by the help of _____ signal, at the time of transfer.

Analog

Digital

Clock

Data

Question 67

The word asynchronous is normally used to portray communications in which data can to be transmitted irregularly instead of in a_____ stream.

Single

Multiple

Zero

Steady

Question 68

The _____must decide the clocking of the signal itself.

Transmitter

Transducer

Recorder

Receiver

Question 69

Asynchronous communication is at times known as _____ transmission.

Sychronous

Start-Stop

Asynchronous Start-Stop

Normal

Question 70

The trouble with asynchronous communications is that the receiver should have a method to differentiate between _____ and valid data.

Noise

Input

Output

Sound

Unit 11 Peripherals

Question 1 (1 point)

A bus is asynchronous when data transfer on the bus depends upon the _____ of the data and not on a clock signal.

- Quality
- Accessibility
- Range
- Amount

Question 2 (1 point)

Synchronous buses are simple and are also easy to_____.

- Modify
- Execute
- Implement
- Understand

Question 3 (1 point)

In asynchronous bus data transfer on the bus is monitored by a bus _____.

- Cycle
- Clock
- Parity
- Signal

Question 4 (1 point)

Control buses are used to transmit _____.

- Analog Signal
- Control Signal
- Digital Signal
- Address Signal

Question 5 (1 point)

_____ bus transmit the memory address.

- Power
- Data
- Address
- Control

Question 6 (1 point)

_____ buses transmit the power-supply/ground voltage.

- Data

- Power
- Address
- Control

Question 7 (1 point)

Data buses are used to ____ data.

- Internal Flag
- External Flag
- Parity Flag
- Transmit

Question 8 (1 point)

The I/O handling procedure will require some status information from the _____device

- I/O
- Input
- Output
- External

Question 9 (1 point)

The word _____ is often used to refer to the buffer itself.

- Pin
- Port
- I/O pin
- I/O Port

Question 10 (1 point)

Program controlled I/O is often used for simple operations which must be performed _____.

- Combinationally
- Seperatly
- Sequentially
- Alternatively

Question 11 (1 point)

The main disadvantage of program-controlled I/O is that a great deal of time may be spent testing the status inputs of the I/O devices when the devices do not need _____.

- Changes
- Modification
- Connectivity
- Servicing

Question 12 (1 point)

It is relatively easy to add or delete _____.

- Options
- Disks
- Devices
- Drives

Question 13 (1 point)

A_____is the name given to a connection to an I/O device.

- Link
- Port
- Connection
- I/O Connection

Question 14 (1 point)

The key concept in I/O software designing is_____ achieved by using uniform naming.

- Device Independence
- Device Dependence
- Drive Independence
- Drive Dependence

Question 15 (1 point)

Data transfer between the I/O devices and the central computer may be tackled in_____ modes.

- No
- Single
- Double
- Several

Question 16 (1 point)

Few modes utilise the CPU as an intermediate path, while others transfer the data straight to and from the memory unit, with no intervention of CPU just as in _____.

- IOP
- DMA
- IMA
- Direct Access

Question 17 (1 point)

The CPU implements programs that begin, direct and end a _____operation.

- Input
- Ottput
- Deleting
- I/O

Question 18 (1 point)

In both programmed I/O as well as interrupt driven I/O, CPU is in charge of reading data from the_____as well as writing data into the_____.

- Memory,Device
- Drive,Memory
- Drive,Drive
- Memory,Memory

Question 19 (1 point)

The I/O module is able to _____ data from/in the memory.

- Store
- Retrieve
- Store or Retrieve
- Copy

Question 20 (1 point)

Data transfer to and from peripherals can be performed in _____ modes.

- 3
- 4
- 5
- 6

Question 21 (1 point)

When a large quantity of data is to be transferred from CPU, a _____ can be utilised.

- DMA Module
- DMA Page
- DMA Design
- DMA Method

Question 22 (1 point)

In both Programmed and Interrupt driven I/O, the CPU is busy in implementing_____ instructions.

- Input
- Input/Output
- Output

- Read

Question 23 (1 point)

In majority mini- and main-frame computer systems, a great deal of input and output happens between the _____ and the disk system.

- Drive
- Device
- Processor
- Memory

Question 24 (1 point)

I/O performed in such a manner is generally called _____.

- Indirect Memory Access
- Indirect Media Access
- Direct Media Access
- Direct Memory Access

Question 25 (1 point)

_____the DMA controller maintains control of the bus till the entire data has been moved to (from) memory from (to) the peripheral device.

- On
- Off
- Burst Mode
- Single Cycle Mode

Question 26 (1 point)

In _____ (cycle stealing), the DMA controller gives up the bus following every transfer of single data word.

- Single Cycle Mode
- Burst Mode
- Arithmetic
- Machine

Question 27 (1 point)

If the data to be transferred is in bulk then _____ technique is the best choice as it increases the data transfer speed.

- Direct Access
- IOP
- DMA
- Memory Access

Question 28 (1 point)

In case varied data_____ happen to be exchanged, the interface should be able to transform serial data to parallel form as well as vice-versa.

- Information
- Interrupts
- Data
- Attributes

Question 29 (1 point)

The reason behind the communication link is to solve the differences which exist between every peripheral and the _____computer.

- Super
- Mini
- Central
- Mainframe

Question 30 (1 point)

Peripherals linked to a computer need special communication connections for interfacing them along with the _____.

- CPU
- Disk
- Drive
- Hardware

Question 31 (1 point)

In all general-purpose computers, the terminal, magnetic disk and _____ are utilised.

- Keyboard
- Mouse
- Drive
- Printer

Question 32 (1 point)

The magnetic _____ is used for backup storage in computers.

- Disk
- Drive
- Tape
- Device

Question 33 (1 point)

We release a _____ command to make the peripheral active.

- Status
- Control
- Data Input
- Data Output

Question 34 (1 point)

We utilise a _____ command to check several status conditions in the peripheral and the interface.

- Control
- Data Input
- Data Output
- Status

Question 35 (1 point)

The 8237 is a DMA Controller that provides the memory as well as I/O with memory address information and control signals at the time of the _____.

- DMA Transfer
- DMA Request
- DMA Response
- DMA Process

Question 36 (1 point)

The 8237 is, in reality, a special-purpose _____ which has the job of high-speed data transfer between the I/O devices and memory.

- Microprogram
- Microprocessor
- Macroprocessor
- Macroprogram

Question 37 (1 point)

Intel 8237 was utilised like a DMA controller in the earliest ____ and _____.

- IBM XT ,IBM PC
- IBM XT ,IBM XT
- IBM PC ,IBM PC
- IBM XT ,IBM

Question 38 (1 point)

Intel 8237 has_____ independent DMA channel.

- 2
- 3
- 4
- 5

Question 39 (1 point)

Intel 8237 supports the software DMA _____.

- HTTP Response
- Response
- Requests
- HTTP Request

Question 40 (1 point)

Every channel can address _____ address with word count capabilities.

- 32k
- 64k
- 128k
- 254k

Question 41 (1 point)

Maximum data transfer rate is _____MB/Sec.

- 1.2
- 1.4
- 1.6
- 1.8

Question 42 (1 point)

PPI stands for ___ Programmable Peripheral Interface_____.

- Programmable
- Process
- Programmable
- Programmable

Question 43 (1 point)

PPI is a_____ device that can be programmed by the programmer.

- Singlepart
- Multipart

- Dualpart
- Triplepart

Question 44 (1 point)

The Intel 8255 is a Programmable Peripheral Interface (PPI) chip which was initially created for the Intel _____ microprocessor.

- 8080
- 8082
- 8085
- 8088

Question 45 (1 point)

Intel 8255 is made in DIP___and PLCC _____pins encapsulated versions.

- 40,41
- 40,42
- 40,43
- 40,44

Question 46 (1 point)

Mode 1 supports _____

- Encapsulating
- Handshaking
- Directioning
- Programming

Question 47 (1 point)

Mode 2 is used for _____ handshaking data transfer.

- Uni-directional
- Bi-directional
- Tri-directional
- Any-directional

Question 48 (1 point)

The individual bits of port C has the ability to set or reset by conveying the signal _____ instruction to the control register.

- IN
- EXE
- OUT
- WAIT

Question 49 (1 point)

PCI bus was initially created as a local bus expansion for the _____ bus.

- ISA/ESA
- ISA/EISA
- ISA/EIS
- EIS/ISA

Question 50 (1 point)

ISA stands for _____

- Indian Standard Architecture
- Industry Set Architecture
- Industry Standard Architecture
- Industry Secured Architecture

Question 51 (1 point)

The initial version of the PCI bus performed at _____ with a 32-bit bus (133MBps).

- 20MHz
- 24MHz
- 30MHz
- 33MHz

Question 52 (1 point)

The PCI bus performs either asynchronously or synchronously along with the motherboard _____ rate.

- Clock
- Cycle
- Noise
- Period

Question 53 (1 point)

PCI will permit a bus master to move data at the _____ allowable rate.

- Minimum
- Maximum
- Zero
- Normal

Question 54 (1 point)

The PCI bus utilises its personal internal interrupt system for handling the_____ from the cards on the bus.

- Response
- Argument
- Request
- Statement

Question 55 (1 point)

PCI gives support to full device_____mastering.

- Peripheral
- Register
- Processor
- Bus

Question 56 (1 point)

_____should be present at the very ends of the bus, subsequent to all the real devices on the chain.

- Terminators
- Transmitters
- Enders
- Transducers

Question 57 (1 point)

Reflected signals intrude with the "real" data on the bus and cause data corruption and _____.

- Noise Corruption
- Signal Corruption
- Signal Loss
- Noise Loss

Question 58 (1 point)

In the initial SCSI arrangement, synchronous communication permitted speeds till_____.

- 2Mb/sec
- 3Mb/sec
- 4Mb/sec
- 5 Mb/sec

Question 59 (1 point)

SCSI utilises a 3-bit addressing scheme, in which every device is designated an address varying from_____.

- 0 to 5
- 0 to 7

- 0 to 9
- 0 to 12

Question 60 (1 point)

Terminators can be either _____ terminators or _____ terminators.

- InternaI, External
- Implicit,Explicit
- Farward, Backward
- Positive , Negative

Question 61 (1 point)

The host computer is normally designated to be _____.

- Device 3
- Device 5
- Device 7
- Device 9

Question 62 (1 point)

ANSI X3.131 – 1986 is the official name of the_____ standard.

- ANSI
- SCSI
- ASCII
- PCI

Question 63 (1 point)

Serial I/O 8251 contains_____ duplex double buffered system.

- Half
- More than half
- Full
- Overflow

Question 64 (1 point)

_____communication is mostly used while transmitting the data over a long distance.

- Serial
- Parallel
- Alternative
- Direct

Question 65 (1 point)

Serial I/O 8251 one bit at one time over a_____ line.

- Zero
- Single
- Double
- Multiple

Question 66 (1 point)

Serial I/O 8251 is also called _____ chip.

- Universal Synchronous Asynchronous Receiver Transducer(USART)
- Universal Synchronous Asynchronous Recorder Transmitter (USART)
- Uniform Synchronous Asynchronous Receiver Transmitter (USART)
- Universal Synchronous Asynchronous Receiver Transmitter (USART)

Question 67 (1 point)

Synchronous baud rate of serial I/O 8251 is _____ baud .

- 0-16k
- 0-32k
- 0-64k
- 0-128k

Question 68 (1 point)

Asynchronous baud rate of serial I/O 8251 is _____ baud.

- 0-19k
- 0-18k
- 0-18.2k
- 0-19.2k

Question 69 (1 point)

Serial I/O 8251 has_____DIP package.

- 16pin
- 28pin
- 32pin
- 36pin

Question 70 (1 point)

0

- Electrical Indian Association
- Electronic Industries Association
- Electrical Industries Association

- Electronic Indian Association

Question 71 (1 point)

A wire exists for every signal, along with the _____signal.

- Ground
- Analog
- Digital
- Positive

Question 72 (1 point)

Very high data rate is possible by use of _____ signalling.

- Similar
- Positive
- Differential
- Negative

Question 73 (1 point)

The differential signalling uses very small amount of _____ which saves power.

- Current
- Noise
- Amplitude
- Voltage

Question 74 (1 point)

A signal resting on a single line is not possible to screen efficiently for _____.

- Noise
- Current
- Voltage
- Amplitude

Question 75 (1 point)

_____ levels with relation to ground signify the RS-232 signals.

- Current
- Voltage
- Amplification
- Serial

Question 76 (1 point)

The _____ ports on the majority of the computers utilise a subset of the RS- 232C standard.

- Parallel
- Alternative
- Serial
- Combinational

Question 77 (1 point)

Majority of the operations and actions which occur in computers are carefully controlled and happen at particular_____and_____.

- Time and Cycle
- Time and Interval
- Interval and Version
- Version and Cycle

Question 78 (1 point)

In synchronous data transmission, data is transmitted though a bit-stream, that transmits a group of characters in a _____ stream.

- Single
- Double
- Multiple
- Zero

Question 79 (1 point)

Data transfer, the transmission speed is synchronised at both the sender and receiver by the help of _____ signal, at the time of transfer.

- Analog
- Digital
- Clock
- Data

Question 80 (1 point)

The word asynchronous is normally used to portray communications in which data can to be transmitted irregularly instead of in a_____ stream.

- Single
- Multiple
- Zero
- Steady

Question 81 (1 point)

The _____must decide the clocking of the signal itself.

- Transmitter

- Transducer
- Recorder
- Receiver

Question 82 (1 point)

Asynchronous communication is at times known as _____ transmission.

- Sychronous
- Start-Stop
- Asynchronous Start-Stop
- Normal

Question 83 (1 point)

The trouble with asynchronous communications is that the receiver should have a method to differentiate between _____ and valid data.

- Noise
- Input
- Output
- Sound

Unit 12

Question 1 (1 point)

_____ is the most commonly used input device.

- Keyboard
- Mouse
- Printer
- Display Unit

Question 2 (1 point)

The signal from the keyboard is monitored by the keyboard controller in the computer which is an_____ circuit that processes all of the data that comes from the keyboard and forwards it to the operating system for further processing.

- Sequential
- Integrated
- Combinational
- Electric

Question 3 (1 point)

_____ input device is used to directly draw the figures on the screen of the monitor.

- Mouse

- Keyboard
- Light Pen
- Printer

Question 4 (1 point)

Digital cameras are used to bring in live_____ onto the screen, where some changes can also be made thereon.

- Texts
- Audios
- Videos
- Images

Question 5 (1 point)

_____ is a conversion process used by scanners.

- Translating
- Monitoring
- Normalising
- Digitising

Question 6 (1 point)

In 1995, when the manufacturers saw that the users are reluctant to the use of scanners, they reduced the price of the small paper scanners by _____%.

- 40-50
- 50-60
- 60-70
- 70-80

Question 7 (1 point)

Drum Scanners are capable of resolutions up to _____PPI.

- 21000
- 22000
- 24000
- 28000

Question 8 (1 point)

Users cannot understand results represented in the form of _____signals.

- Electronic
- Digital
- Physical
- Continous

Question 9 (1 point)

_____devices convert the machine-readable output into human-readable form.

- Input
- Output
- Hardware
- Software

Question 10 (1 point)

_____ the picture elements more improved is the resolution of the image.

- Higher
- Lower
- Smaller
- Larger

Question 11 (1 point)

Flat-panel displays have a _____ weight and consume _____ electricity as compared to CRTs.

- More, Less
- Less, More
- Less, Less
- More,More

Question 12 (1 point)

A clearer and more detailed image is provided by the higher resolution, containing _____ pixels.

- Zero
- Less
- More
- Infinite

Question 13 (1 point)

Two monitors having the same pixel configuration may show a variation in sharpness in its view due to a difference in _____.

- Line Pitch
- Dot Pitch
- Parallel Pitch
- Any Pitch

Question 14 (1 point)

_____ printers are available in a variety of sizes, usually the bigger and quicker the printer, the more costly it is.

- Inkjet
- Doy Matrix
- Laser
- Monochrome

Question 15 (1 point)

The secondary storage units of a computer, as well as the input/output (I/O) devices are called _____.

- Peripheral
- Input
- Output
- Processor

Question 16 (1 point)

The peripheral devices are add-on hardware to expand computer's abilities or improve its_____.

- Efficiency
- Speed
- Capacity
- Performaces

Question 17 (1 point)

Peripherals that offer _____ storage for the system are magnetic disks.

- Primary
- Secondary
- Teritary
- Memory

Question 18 (1 point)

A peripheral is linked to a host computer however, it is not a part of the _____computer and just relies on it.

- Client
- Server
- Primary
- Host

Question 19 (1 point)

A computer may perform various tasks considerably, given its default_____ configuration.

- Computer
- Server
- Hardware
- Software

Question 20 (1 point)

The most common _____ are keyboards, mouse, display units and printers.

- Peripheral
- Devices
- Instruments
- Components

Unit 13

Question 1 (1 point)

The multiprocessor operating systems are complex in comparison to multiprograms on a _____processor operating system because multiprocessor executes tasks concurrently.

- Uni
- Bi
- Tri
- Zero

Question 2 (1 point)

In separate supervisor system each process behaves_____.

- Dependently
- Independently
- Similarly
- Differently

Question 3 (1 point)

The access protection is maintained, between processor, by using some synchronisation mechanism like _____.

- Kernal
- Operating System
- Semaphores
- Thread

Question 4 (1 point)

The master processor is dedicated to executing the_____.

- Operating Device
- Snchronisation System
- Operating System
- Synchronisation Device

Question 5 (1 point)

In symmetric organisation all processors configuration are _____.

- Different
- Dependent
- Independent
- Identical

Question 6 (1 point)

The simplest way to achieve this is to treat the entire operating system as critical section and allow only one processor to execute the operating system at_____ time.

- One
- Two
- Three
- Four

Question 7 (1 point)

Limited _____ is the main limitation of this system, because the master processor become a bottleneck and will consequently fail to fully utilise slave processors.

- Durability
- Scalability
- Performances
- Processing

Question 8 (1 point)

There are mainly _____.

- 3
- 4
- 5
- 6

Question 9 (1 point)

A shared memory multiprocessor system develops the problem of contention due to memory_____.

- Combining
- Sharing
- Splitting
- Managing

Question 10 (1 point)

Communication contention occurs when various processors are unable to complete their access because of the interconnection_____ limitations.

- Network
- Physical
- Transport
- Datalink Layer

Question 11 (1 point)

Communication contention may also occur in a situation when the processors request access to different memory_____.

- Block
- Component
- Module
- Unit

Question 12 (1 point)

_____ is another common type of contention problem in a multiprocessor system.

- Bluetooth
- Wifi
- Hot Spot
- Network

Question 13 (1 point)

_____ technique is utilised to resolve performance degradation problem caused due to hot spot contention.

- Sequencing
- Combining
- Managing
- Marketing

Question 14 (1 point)

Proper allocation of _____must be done by the compiler.

- Drive Structure
- Data System
- Data Structure
- Operating System

Question 15 (1 point)

A coprocessor is also known as a_____processor.

- Alphabetical
- Numeric
- Dual Core
- Quad Core

Question 16 (1 point)

With the help of _____, the multiprocessor is offloaded of its work.

- Processor
- Mini Multiprocessor
- Coprocessor
- Modified Processor

Question 17 (1 point)

Coprocessor is a relatively new concept in the area of _____.

- Multiprogramming
- Multiprocessing
- Programming
- Processing

Question 18 (1 point)

The _____ assigns some of the work to the coprocessor, which otherwise would have been assigned to the multiprocessor.

- Hard Disc
- Motherboard
- Hardware
- Software

Question 19 (1 point)

Coprocessors allow a line of computers to be customised so that customers who do not need the extra_____ need not pay for it.

- Efficiency
- Speed
- Performance

- Capacity

Question 20 (1 point)

SMP refers to _____.

- Symmetric Multiprocessing
- Symmetric Multiprogramming
- Systematic Multiprocessing
- Systematic Multiprogramming

Question 21 (1 point)

A Loosely-coupled multiprocessor system is often referred to as _____.

- Couple
- Clusters
- Group
- Channels

Question 22 (1 point)

_____ is one of the common examples of a loosely-coupled system.

- Unix Cluster
- Unix Beowulf cluster
- Linux Beowulf cluster
- Any Linux cluster

Question 23 (1 point)

Closely or tightly-coupled multiprocessor systems contain _____ CPUs.

- No
- One
- Two
- Multiple

Question 24 (1 point)

A tightly-coupled multiprocessor system consists of _____ CPUs, and these CPUs are linked jointly at the bus level.

- One
- Two
- Three
- Multiple

Question 25 (1 point)

_____bit Ethernet is one of the most common high-speed communication systems.

- Giga
- Mega
- Macro
- Mini

Question 26 (1 point)

Multiple standalone duals or single processor commodity computers unified through a _____communication system form the basis of loosely-coupled multiprocessors.

- Normal Speed
- Low Speed
- High Speed
- High Velocity

Question 27 (1 point)

A system may assimilate one or more external_____and assign them the duty of direct communication with all I/O devices.

- Devices
- Processor
- Registers
- Componepts

Question 28 (1 point)

With relation to a _____ which requires being set up completely by the CPU, the IOP is able to fetch and execute its personal instructions.

- IOP Decoder
- IOP Controller
- DMA Controller
- DMA Decoder

Question 29 (1 point)

The CPU is in possession of _____ required in the solution of computational jobs.

- Processing Data
- Processing Array
- Processing String
- Controlling Data

Question 30 (1 point)

The data _____of CPU data and memory are dissimilar to the data _____ of peripheral devices.

- Device,Device

- Device,Format
- Format,Device
- Format,Format

Question 31 (1 point)

The computer system might have numerous channels, and every channel is allocated a _____.

- Format
- Outline
- Address
- Description

Question 32 (1 point)

The initial word causes a byte to move into a magnetic tape from memory beginning at address _____.

- 2000
- 4000
- 6000
- 8000

Question 33 (1 point)

The first flag is fixed at 1 in the first command word to indicate _____.

- Data Changing
- Data Linking
- Data Formating
- Data Chaining

Question 34 (1 point)

A huge _____memory is needed for holding together the complicated operating system as well as several programs of users.

- Main
- Primary
- Secondary
- Cache

Question 35 (1 point)

The routine operation and maintenance of such systems is also _____.

- Cheap
- Cheaper
- Very Expensive

- Expensive

Question 36 (1 point)

_____ coherence refers to the consistency of data stored in local caches of a shared resource.

- Memory
- Cache
- Switch
- Bus

Question 37 (1 point)

A _____ consistency model determines in which order processes get notice of memory accesses by other processes.

- Cache
- Switch
- Bus
- Memory

Question 38 (1 point)

Besides the CPUs, multiprocessing also makes possible _____efficiency in the utilisation of every other device of the computer system.

- Constant
- Zero
- Decreased
- Increased

Question 39 (1 point)

Multiprocessing makes the functioning of computer systems better by permitting parallel processing of _____ segments.

- Code
- Base
- Program
- Bus

Question 40 (1 point)

_____ is the interleaved execution of more than two processes by a sole CPU computer system.

- Multiprocessing
- Multiprogrammming
- Singleprocessing

- Singleprogramming

Unit 14: Parallel Organization

Question 1 (1 point)

_____ processors have larger instruction sets that often include some particular complex instructions.

- **CISC**
- RISC
- Parity
- Couple

Question 2 (1 point)

The RISC architecture involves an attempt to reduce execution time by simplifying the instruction set of the computer.

- Fetching
- **Simplifying**
- Decoding
- Executing

Question 3 (1 point)

In CISC a large variety of addressing modes , typically from _____different modes.

- 5 to 10
- 5 to 12
- **5 to 20**
- 5 to 30

Question 4 (1 point)

_____ is defined as the amount of work that the processor can do in a given period.

- Efficiency
- Capacity
- Speed
- **Performance**

Question 5 (1 point)

RISC stands for _____.

- Redundancy Instruction Set Computer
- Reduced Instruction Structure Computer
- **Reduced Information Set Computer**
- Reduced Instruction Set Computer

Question 6 (1 point)

CISC stands for _____.

- **Complex Instruction Set Computer**
- Complex Instruction Structure Computer
- Component Instruction Set Computer
- Complex Information Set Computer

Question 7 (1 point)

In RISC all operations are done within the_____ of the CPU.

- Processors
- IC Chips
- **Registers**
- Disks

Question 8 (1 point)

A parallel processing organisation looks for a grosser level of parallelism, one that enables work to be done in _____, and cooperatively, by multiple processors.

- **Parallel**
- Serial
- One by One
- Alternatively

Question 9 (1 point)

A single processor executes a single instruction stream to operate on data stored in a single memory this is called as_____.

- MISD
- MIMD
- SIMD
- **SISD**

Question 10 (1 point)

A sequence of data is transmitted to a set of processors, each of which executes a different instruction sequence this is called as_____.

- SISD
- MISD
- **MIMD**
- SIMD

Question 11 (1 point)

A more recent development is the _____ organization

- Uniform Memory Access (UMA)
- Memory Access (MA)
- Static Memory Access (SMA)
- **Non Uniform Memory Access (NUMA)**

Question 12 (1 point)

The term _____ refers to a computer hardware architecture and also to the operating system behaviour that reflects that architecture.

- UMA
- NUMA
- MA
- **SMP**

Question 13 (1 point)

_____is a shared memory architecture used in parallel computers.

- NUMA
- SMP
- **UMA**
- MA

Question 14 (1 point)

_____ is a computer memory design used in multiprocessing, where the memory access time depends on the memory location relative to a processor.

- **NUMA**
- UMA
- SMP
- MA

Question 15 (1 point)

Superscalar instruction issue can favourably be discussed within the framework of its design _____.

- **Issue**
- Space
- Link
- File

Question 16 (1 point)

The _____, specifies the maximum number of instructions a superscalar processor is able to issue in each cycle.

- Data Rate
- Transfer Rate
- **Issue Rate**
- Execution Rate

Question 17 (1 point)

The third aspect of issue policy concerns the_____, an efficient technique to avoid issue blockages.

- **Use of Shelving**
- Use of Storing
- Use of Designing
- Use of Repairing

Question 18 (1 point)

_____may be blocked in both cases, with or without shelving.

- Design Issue
- Structure Issue
- Storage Issue
- **Instruction issue**

Question 19 (1 point)

The simplest, most often used policy is the _____.

- Superscalar Issue Policy
- Straightforward Superscalar Issue with Renaming
- Straightforward Aligned Superscalar Issue
- **Straightforward Superscalar Issue Policy**

Question 20 (1 point)

The final policy commonly used is the_____.

- Straightforward Aligned Superscalar Issue
- Advanced Superscalar Issue Policy
- **Straightforward Superscalar Issue with Renaming**
- Straightforward Superscalar Issue Policy

Question 21 (1 point)

Register renaming, is a standard technique for removing false data dependencies, that is, _____ dependencies, among register data.

- WAN and WAR
- WAN and WAW
- WAR and WAT
- **WAR and WAW**

Question 22 (1 point)

In Super Scalar Processors,_____ instructions are issued per cycle and multiple results are generated per cycle.

- Single
- **Multiple**
- Dual
- Input

Question 23 (1 point)

Owing to their higher complexity, superscalar_____appeared on the market after a considerable delay.

- RISC processors
- CISC Program
- **CISC processors**
- RISC Program

Question 24 (1 point)

The Pentium and the _____ are examples of the first superscalar CISC machines, which have been available since 1993.

- MC 68020
- MC 68040
- **MC 68060**
- MC 68080

Question 25 (1 point)

The _____ and the Am 29000 superscalar processors are typically intended for high-performance desktop and workstation market.

- Intel 560
- **Intel 960**
- Intel 970
- Intel 980

Question 26 (1 point)

Super scalar processors have to issue multiple instructions per cycle, the first task necessarily is parallel _____.

- **Fetching**
- Decoding
- Executing
- Storing

Question 27 (1 point)

An increasingly common method of enhancement is _____.

- Decoding
- **Predecoding**
- Postdecoding
- Encoding

Question 28 (1 point)

The instruction issue policy used becomes crucial for achieving higher, _____ performance.

- IC
- Register
- **Processor**
- Disk

Question 29 (1 point)

The _____algorithm is more suitable for pipelining because the machine can merge two ordered vectors in one pass.

- **Merge-Sort**
- Merge-Algorithm
- Insertion-Sort
- Insertion-Algorithm

Question 30 (1 point)

The degree of _____ refers to the number of independent operations that can be performed.

- Sorting
- **Parallelism**
- Vectorization
- Insertion

Question 31 (1 point)

The process to replace a block of sequential code by vector instructions is called _____.

- **Vectorization**
- Insertion
- Parallelism
- Segmentation

Question 32 (1 point)

The system software, which does this regeneration of parallelism, is called a_____.

- Vectorizing Computer
- Vectorizing Address
- **Vectorizing Compiler**
- Vectorizing Content

Question 33 (1 point)

The main memory is often interleaved to minimise the_____ of vector operands.

- Complexity Time
- Rotational Time
- **Access Time**
- Execution Time

Question 34 (1 point)

The _____ fetches and decodes scalar and vector instructions.

- **Control Processing Unit (CPU)**
- Instruction Processing Unit (IPU)
- Information Processing Unit (IPU)
- Computer Processing Unit (CPU)

Question 35 (1 point)

An increase in system overhead may be incurred with vector _____.

- Fragmentations
- **Vectorization**
- Segmentations
- Parallelization