VHDL CODE WITH CHISELTESTER

A LOOK INTO USING VHDL WITH VERILOG-ONLY TOOLS

WHY?

- Open-source tools
- Verilog only tools
 - VHDL is more difficult to parse
- Chisel with legacy code
 - Only when using Verilator

HOW?

- Open-source tools
- GHDL
 - Open-source VHDL simulator
 - Full support for 1987, 1993, 2002
 - Partial support for 2008
- Yosys Yosys Open SYnthesis Suite
 - Open-source RTL synthesis tools
 - Verilog-2005 only
- Combined
 - Ghdl-yosys-plugin

GETTING STARTED

- Run natively on Linux
 - https://github.com/chisel-uvm/vhdl2verilog
- Run through Docker
 - https://github.com/chisel-uvm/Docker
 - Both vhdl2Verilog and Chisel

CONVERSION

- yosys -m ghdl -p 'ghdl --std=08 src/accualu.vhd -e accualu; write_verilog synth_accualu.v'
 - --std=08 for VHDL 2008 support
 - Files required
 - Needs to be in order
 - -e is the entity
 - Generates a file called synth_accualu.v
 - Support for generics

BLACKBOX IN CHISEL

- Same as for Verilog
- Blackbox

```
"AluAccuGenerated" should "pass" in {
  test(new AluAccuGenerated(32)).withAnnotations(Seq
    (VerilatorBackendAnnotation)) { dut => testFun(dut) }
}
```

```
class accualu extends BlackBox with HasBlackBoxResource {
 val io = IO(new Bundle {
   val clock = Input(Clock())
   val reset = Input(Reset())
   val op = Input(UInt(3.W))
   val din = Input(UInt(32.W))
   val ena = Input(Bool())
   val accu = Output(UInt(32.W))
 setResource("/accualu converted.v")
class AluAccuGenerated(size: Int) extends AluAccu(size) {
 val AluAccu = Module(new accualu())
 //Needs to be done with explicit clock and reset
 // because blackbox does not have this defined.
 AluAccu.io.op := io.op
 AluAccu.io.din := io.din
 AluAccu.io.ena := io.ena
 io.accu := AluAccu.io.accu
 AluAccu.io.clock := clock
 AluAccu.io.reset := reset
```

DEMO AND FUTURE

- Currently used for converting old files
- Should be called within Chisel
- Support for generics on the fly
 - -gBIT_WIDTH=12