High-Level Design and Verification of Digital Systems

Martin Schoeberl

Technical University of Denmark

Program

- Introduction, Martin Schoeberl
- UVM - How, why, and is it even necessary?, Kasper Hesse
- Code coverage at Scala level, Hans Jakob Damsgaard
- Code Coverage at FIRRTL Level, Andrew Dobis
- Property Based Testing, Zhoulai Fu
- Cover Points, Andrew Dobis
- Break, bring your own coffee
- C Integration in SystemVerilog and Scala, Kasper Hesse
- VHDL Code with Chisel Tester, Simon Thye Andersen
- Constraint random Verification, Enrico Tolotto
- Sorting Use Case, Tjark Petersen
- Teaching Activities on Verification at DTU, Martin Schoeberl
- Summarize and Outlook, Martin Schoeberl

InfinIT Project

- High-Level Design and Verification of Digital Systems
- June – October
- DTU, ITU, AU
- Microchip, WS Audiology, Synopsys, Syosil
- Several student researchers
- Kickoff project for larger research project

Topics

- Increase productivity in digital design and verification
- UVM and SystemVerilog
- Chisel and Scala
- Mixing of languages and technologies
- What is missing in Chisel/Scala world?
  - Get inspired by SystemVerilog and UVM
  - We started prototype implementations

State of the Art

- Most HW designs are in VHDL or Verilog
  - Quite old languages
- Modern concepts such as OO and FP missing
- SystemVerilog adds OO for verification
  - Code coverage and constraint random generators
  - OO not usable for design description
- Universal Verification Method (UVM)

UVM

- Open-source SystemVerilog classes
  - Industry standard
  - Adaption?
- A blueprint to define tests
  - Make tests reusable
- Main approach to compare DUT against a reference model
- Uses SV constraint random test vector generation
- Uses SV coverage metrics

Chisel and ChiselTest

- Chisel is a hardware construction language
- Embedded in Scala, which runs on a JVM
- Many Scala and Java libraries are available
- Generates Verilog for synthesis
- OO and FP usable for hardware description
- ChiselTest is a testing framework for Chisel
  - Basic setting of inputs and reading outputs of a DUT

What is Missing in Chisel?

- A UVM ‘like’ verification framework
- Mixed language support (VHDL)
- Constraint random generation
- Coverage measurements
- Library of test components
  - E.g., bus functional models

First Experiments

- Using Chisel and UVM on a small test circuit
- An ALU with an accumulator
- Written in Chisel and in VHDL
- Tested with Chisel and UVM
- Using Yosys to convert VHDL to Verilog
  - Test the VHDL implementation with Chisel
  - Same tester as the one for the Chisel test
- Show it

Results in Open-Source

- https://github.com/chisel-uvm