

Teaching and Summary

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Teaching

- In Digital Electronics 2
 - Just simple test benches
 - Using waveforms for debugging
 - No further verification
- This fall a new course on: “Verification of Digital Designs”
 - Special course with 5 students
 - First half lecture, including guest lectures
 - Second half project based

Teaching Continued

- Lecture and lab topics
 - Mainly Chisel, some UVM
 - Testbenches with checking
 - Selecting input vectors, randomization
 - Regression tests
- Project topics see:
 - <https://github.com/chisel-uvm/class2020>
- Teaching material and projects in open source

A Paper

- Describing first results
 - <https://woset-workshop.github.io/WOSET2020.html#article-2>
- Extend it
 - Including all the work presented so far
 - Technical report published by DTU
 - Compress it to a conference/journal article

Funding Application

- Software Defined Hardware
- DFF application (submitted end of September)
- Two PhD positions + student researchers
- DTU and ITU
- Industry partners:
 - Microchip
 - Comcores
 - Syosil
 - Synopsys
 - Napatech
 - Teledyne
 - Widex

Future Work

- Continue with the open-source project
- Have some master and bachelor projects
- Link it to the Chisel developer community
 - There is a verification meeting every two weeks
- Hopefully with the DFF funded project

Conclusion

- We aim for an open-source digital design and verification framework
- Start is the Chisel HW construction language
- First steps explored with Scala, Verilator, and Yosys
- On-going project
- See: <https://github.com/chisel-uvm>
- Joining the effort is very welcome