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Letter of Interest

We at Teledyne Reson would like to show our interest in the Software-Defined Hardware project. As a company, we work with system integration and development of components and subsystems. Therefore we need well-defined tests at all levels (components/module, integration, subsystem and system). One of the component types are FPGA. It is especially for the FPGA type of component, we would be interested in new test- and verification capabilities as the current practices are to use either hardware in the loop testing or very low-level simulation verification which both have severe but different shortfalls. For the former, testing can only be done very late in the development and this poses both a technical risk but also a schedule risk. For the latter the validation at low simulation level is very time consuming. There is a need for higher abstraction level simulation and verification for firmware like VHDL and Verilog.

Therefore we recognize the potential for the use of Chisel for both development and testing, which would require compatibility with both VHDL and Verilog. Furthermore, an interest lies in open-source tools that can be used to assist external CAD tools such as ModelSim, when doing simulations of systems or components.

What we can contribute is thoughts and ideas around our need for test and development systems. We have large digital designs that run tests for extended periods. These designs could be used for testing the created verification systems for seeing the capabilities in real-life applications.

With kind regards



Morten Rytter
RD Director
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