```verilog
operand1 <= 16'h0000;
operand2 <= 16'h0000;
if (op1 == 1'b1) begin
    operand1 <= c;
end
if (op2 == 1'b1) begin
    operand2 <= c;
end
next_c <= operand1 + operand2;
```
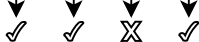
✓ ✓ ✗ ✓

```verilog
operand1 <= 16'h0000;
operand2 <= c;
if (op1 == 1'b1 || op2 == 1'b1) begin
    operand1 <= 16'h0001;
end
next_c <= operand1 + operand2;
```

✗ ✓ ✓