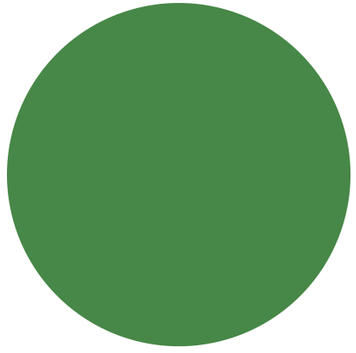
ChiselVerify

Run completed in 3 seconds, 911 milliseconds.
Total number of tests run: 8
Suites: completed 5, aborted 0
Tests: succeeded 8, failed 0, canceled 0, ignored 0, pending 0



Succeeded	8	(100%)
Failed	0	(0%)
Canceled	0	(0%)
Ignored	0	(0%)
Pending	0	(0%)

☑ Succeeded ☑ Failed ☑ Canceled ☑ Ignored ☑ Pending

Suite	Duration (ms.)	Succeeded	Failed	Canceled	Ignored	Pending	Total
Adder4BitTest	2604	3	0	0	0	0	3
AluTest	1499	1	0	0	0	0	1
AluTestVerilator	3695	1	0	0	0	0	1
TestCoverageInformations	69	2	0	0	0	0	2
TestResources	66	1	0	0	0	0	1

Verilator - code coverage report

Current view : top level - chisel.AluTestVerilator - Alu.v
Test : output.info
Date : 2021-02-04

	Hit	Total	Coverage
Lines :	6	6	100.0%

Line	Hits	Source code
1		`module Alu(`
2	5	`input clock,`
3	2	`input reset,`
4	2	`input [1:0] io_fn,`
5	2	`input [3:0] io_a,`
6	2	`input [3:0] io_b,`
7	4	`output [3:0] io_result`
8		`);`
9		`wire _T = 2'h0 == io_fn; // @[Conditional.scala 37:30]`
10		`wire [3:0] _T_2 = io_a + io_b; // @[Alu.scala 18:30]`
11		`wire _T_3 = 2'h1 == io_fn; // @[Conditional.scala 37:30]`
12		`wire [3:0] _T_5 = io_a - io_b; // @[Alu.scala 19:30]`
13		`wire _T_6 = 2'h2 == io_fn; // @[Conditional.scala 37:30]`
14		`wire [3:0] _T_7 = io_a | io_b; // @[Alu.scala 20:30]`
15		`wire _T_8 = 2'h3 == io_fn; // @[Conditional.scala 37:30]`
16		`wire [3:0] _T_9 = io_a&io_b; // @[Alu.scala 21:30]`
17		`wire [3:0] _GEN_0 = _T_8 ? _T_9 : 4'h0; // @[Conditional.scala 39:67 Alu.scala 21:2`
18		`wire [3:0] _GEN_1 = _T_6 ? _T_7 : _GEN_0; // @[Conditional.scala 39:67 Alu.scala 20`
19		`ire[30]GEN2T3?T5GEN1//@[Conditionalscala3967Alscala19`