resume

name：Chi Suhua (池素华)

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Highlights:

* 15+ years of experience in GPU Hardware&Software including Power/Performance Profiling, GPU modeling, Heterogeneous computing, AI Software Stack.
* Familiar Various GPGPU model: gem5/multi2sim
* Good Knowledge on GPU/GPGPU architecture.
* Familiar with Cuda/OpenCL programming
* Good at programming : cuda/OpenCL/C++/C/python,bash,linux kernel,...

Interest area

* Architecture exploring in GPGPU/AI domain.
* Hardware/architecture level modeling developer.

Work experience:

Dec 2019 - Present: Senior Software engineer

* AI core library developer: write AI operator in asm and run in ISS simulator.

March 2018 - Dec 2019: Senior Software engineer

* Developing GEMM asm kernel
* Wrote GPGPU SIMT simulator and use LLVM JIT engine to execute LLVM-IR format kernel code.
* Involved in AI Chip Linux UMD/KMD driver discussion and setup

August 2006 - Feb 2018: Worked in AMD for 12 years, and have many significant achievement:

* Work in dGPU Performance team
* 3D game trace draw snapshot/playback tool development
* AMD GPU 3D performance analysis
* AMD AI Stack(ROCM) Performance Profiling
* Proposal on AI feature architecture improvement, matrix preload/broadcast feature
* dGPU modeling development
  + Work in dGPU Power team
* Build up SOC DesignForPower team
* Write AMD GPU PowerVirus which can burn GPU in highest power.
* DiDt Controller/CAC power architecture
* Write GPU Kernel microbench for GPU Power Analysis and Modeling
  + Work in dGPU Design Verification team
* OpenGL like library development
* Enable OpenGL test case with Power Gating feature
  + Work in dGPU SOC CAD team
* Build up Shanghai SOC CAD team
* Develop SOC Front-end synthesis flow, and the flow is also used NA AMD site.

Dec 2005 - Aug 2006: IC designer in Navasic:

* Work as RTL designer.

April 2002 - April 2005: IC designer in IPcore Shanghai technology:

* CAD engineer on writing script to develop ASIC integration flow.
* ASIC front-end engineer to synthesis and timing analysis on various project.

Prior to IPCore technology, worked in (1998~2002)

Work as PCB board level hardware engineer

* **埃迪恩(上海)信息技术有限公司: 硬件工程师**(2000/11~2002/3)
* **福州宽信科技有限公司: 硬件工程师** (1999/10~2000/10)
* **上海贝尔: 硬件工程师** (1998/7~1999/10)

Education 1994~1998 Bachelor :

* BSEE, FuDan University, micro-electronic major

Contribution/Paper/Technical report(AMD internal)

1. Paralleled tile synthesis flow
2. SOC Netlist editor script, easy diff for eco
3. PowerGating insertion flow
4. DiDt control - AATC12/13 poster(AATC is AMD Aasic Technical conference)
5. GPU Draw snapshot/playback - AATC16 poster
6. Power Virus and Power-Modeling
7. GPGPU simulator which can run simple cuda c code.