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Unit - 4

Digital CMOS Circuits

* MOS Transistors :-

- A metal oxide semiconductor (MOS) structure is created by superimposing several structures or layers of conducting and insulating material.
- These structures are manufactured using series of chemical processes like -
 - ① Oxidation of silicon
 - ② Introduction of dopant
 - ③ Deposition and etching of metal wires and contacts.
- CMOS technology provides two types of transistors
 - A] n-type transistor (nMOS)
 - B] p-type transistor (pMOS)
- Transistor operations are controlled by electric field ∴ called as Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
- n_t and p_t indicates heavily doped and n- and p- indicates lightly doped.

construction :-

NMOS construction and symbol :-

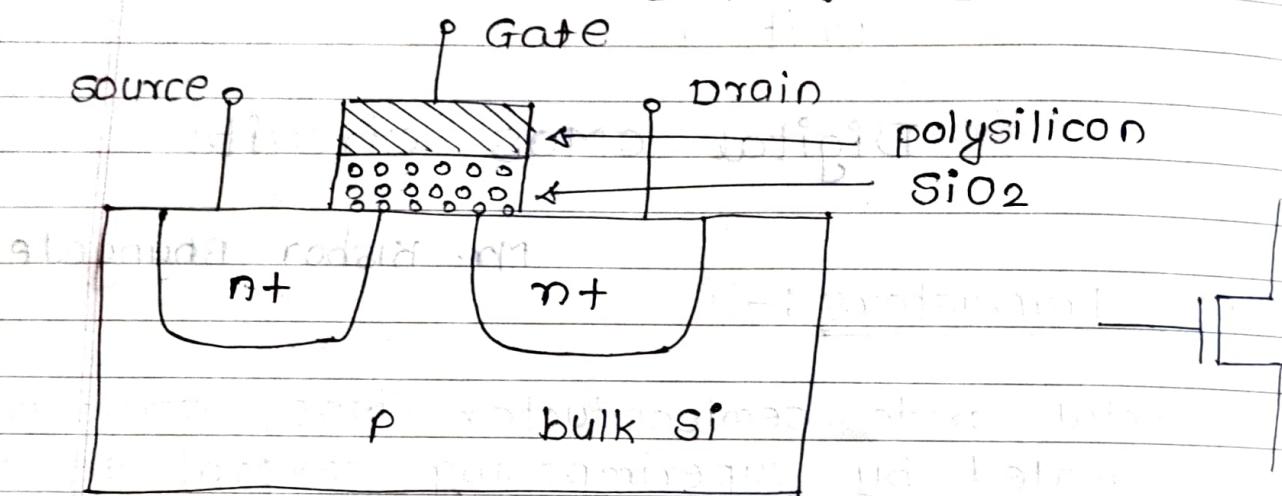


fig. NMOS transistor symbol

PMOS construction and symbol

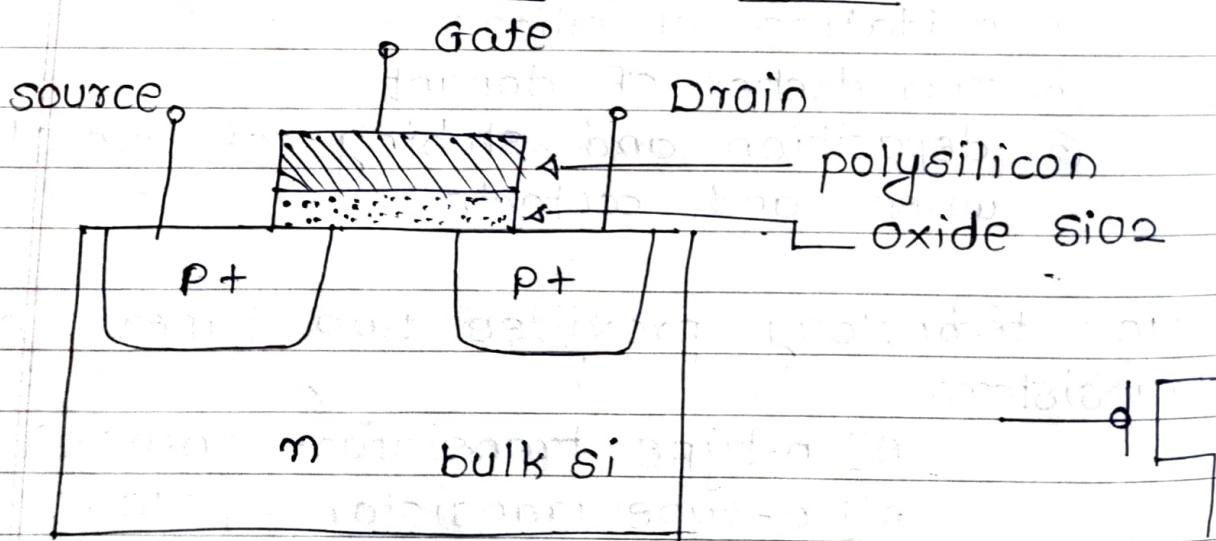


fig. PMOS transistor symbol

- Each transistor consists of stack of wafer or bulk or body or substrate, Silicon dioxide and conducting gate.
∴ transistors are called as metal oxide semiconductor.

\Rightarrow An nmos transistor have p type body and two heavily doped nt region adjacent to gate called as source and drain.

The body is typically grounded.

\Rightarrow P-mos construction is opposite to that of nmos which has p type source and drain and ntype body.

\Rightarrow Region under the gate is called as channel.

Working :-

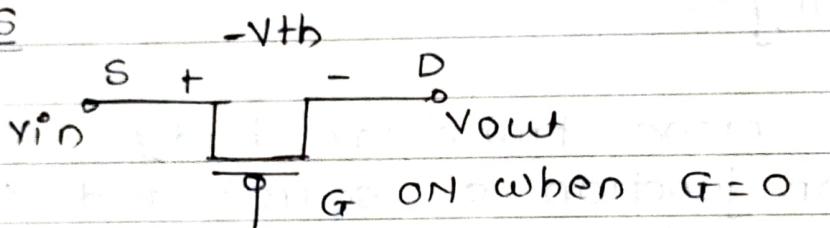
- for nmos transistor body is grounded.
 \therefore pn junction of source and drains are in reverse bias.
- If the gate is also grounded ie. $I_G = 0$ then no current flows through reverse biased junction and x'stor is said to be off.
- When gate voltage is increased, electron starts flowing through channel from source to drain. and we say that x'stor is ON.
- In pmos transistor body has positive voltage. When a gate voltage is also positive, source and drain are in reverse bias and no current flows \therefore pmos remains OFF.
- When the gate voltage is lowered, now

gate voltage inverts the channel and current flows due to holes from source to drain. \therefore PMOS is ON.

- ie when gate signal is high ie VDD, NMOS is ON and when gate signal is low NMOS is OFF.

when gate signal is low ie Gnd, PMOS is ON and when gate signal is high ie. VDD, PMOS is OFF.

for PMOS



when $G=0$ and $Vin = VDD$,

$$Vout = Vin - (-Vth)$$

$$= VDD + Vth$$

= strong 1

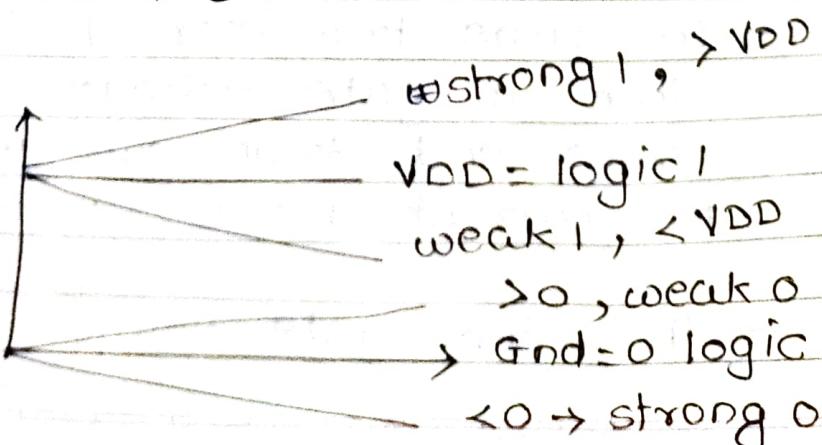
when $G=0$ and $Vin = Gnd = 0$

$$Vout = Vin - (-Vth)$$

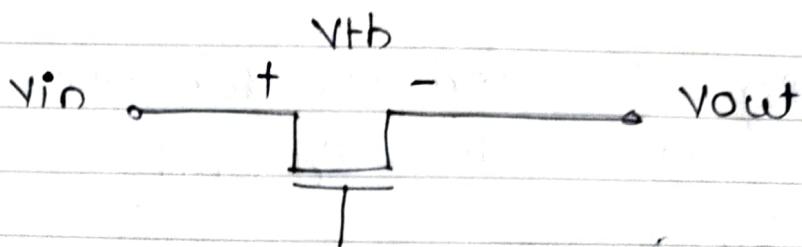
$$= 0 + Vth$$

= weak 0

logic level



for nmos



G ON when $G = V_{DD} = 1$

when $G = 1$ and $V_{in} = V_{DD}$,

$$\begin{aligned}V_{out} &= V_{in} - V_{th} \\&= V_{DD} - V_{th} \\&= \text{Weak 1}\end{aligned}$$

when $G = 1$ and $V_{in} = Gnd = 0$,

$$\begin{aligned}V_{out} &= V_{in} - V_{th} \\&= 0 - V_{th} \\&= -V_{th} \\&= \text{Strong 0}\end{aligned}$$

\therefore we can say that, pmos gives strong 1 for input 1 and weak 0 when input is 0,
 \therefore it is always connected to V_{DD} in CMOS logic.

NMOS gives strong 0 when input is 0 & weak 1 when input is 1, \therefore it is always connected to Ground in CMOS logic design.

-NMOS and PMOS has two types -

- ① Depletion layer MOSFET - physical channel present
- ② Enhancement layer MOSFET - physical channel absent.

* Transfer characteristics of nmos and pmos :-

Transfer characteristics for nmos and pmos are shown in following fig.

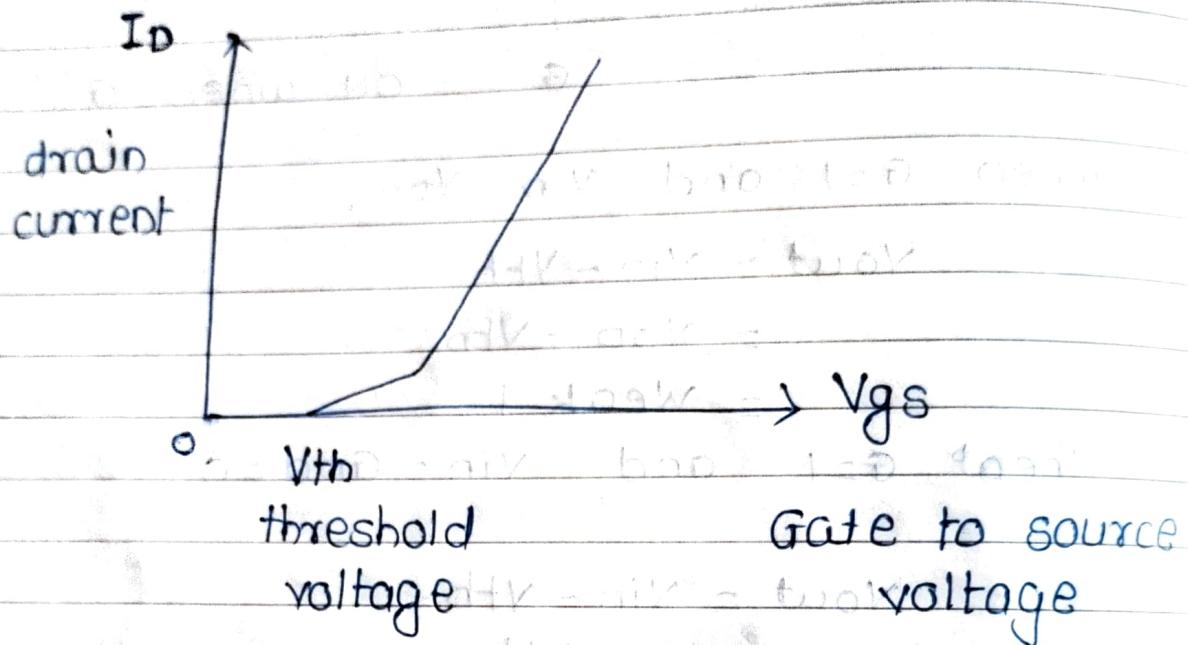


Fig. transfer chara. of nmos

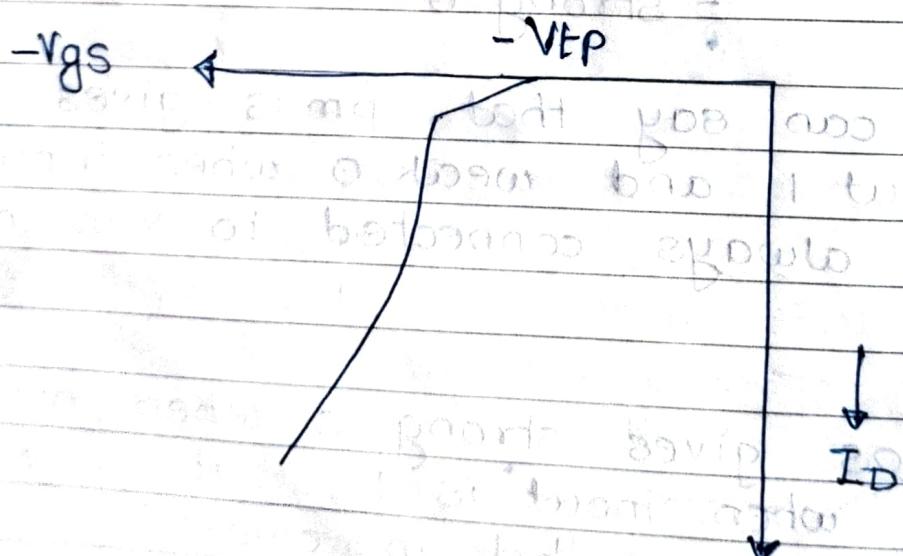


Fig. transfer chara of pmos

The graph of input voltage V_{gs} vs output current I_D is called as transfer chara.

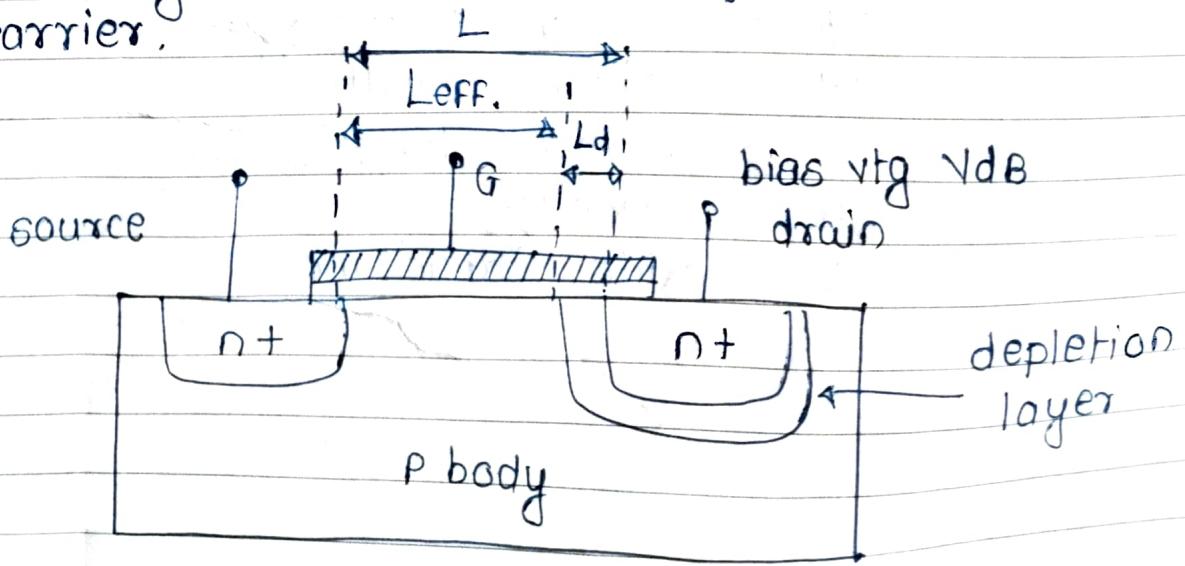
* Non ideal IV Effects :-

The CMOS transistor has following non ideal IV Effects.

- a) channel length modulation
- b) Body Effect
- c) Mobility degradation
- d) Velocity saturation
- e) Drain induced barrier lowering
- f) gate leakage
- g) junction leakage

a) Channel Length Modulation :-

- channel length modulation is shortening of length of channel region when drain bias voltage is increased.
- When drain voltage is increased, reversed biased pn junction between n drain and p body forms depletion layer with no carrier.



- Effective channel length is given by,

$$L_{eff} = L - L_d$$

- Resistance is directly proportional to length; when channel length decreases, resistance also decreases.

- This decrease in resistance causes increase in drain current which further causes decrease in channel length.

- Ideal equation for drain current is given as,

$$I_D = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} (1 + \lambda \cdot V_{ds}) (V_{gs} - V_t)^2$$

$$I_D = \frac{B}{2} \cdot (1 + \lambda \cdot V_{ds}) (V_{gs} - V_t)^2$$

where,

I_D = drain current

V_{ds} = drain to source voltage

V_{gs} = gate to source voltage

V_t = threshold voltage

W = channel width

L = channel length

μ = mobility

C_{ox} = oxide capacitance

b) Body Effect :-

- All MOS devices are made up of common substrate. Due to this substrate voltage for all devices should be equal.
- But when we connect the devices in series to perform required gate function, this substrate voltage changes as shown in following figure.

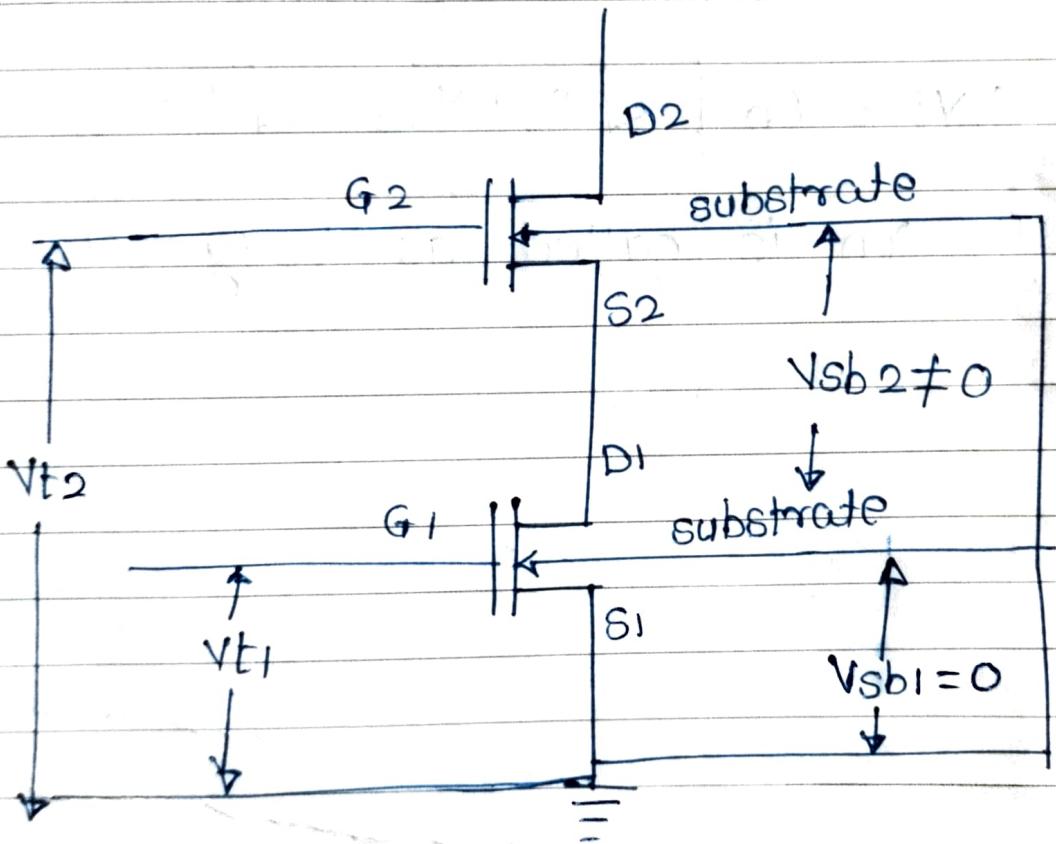


Fig. body Effect.

- For transistor 1, source to substrate voltage $V_{sb1} = 0$ but for x'stor 2, source to substrate voltage is not zero.
ie. $V_{sb2} \neq 0$

- This variation of source to substrate voltage results in variation of threshold voltage V_{th} .

$$\text{ie. } V_{t2} > V_{t1}$$

- The variation in threshold voltage due to changes in source to substrate V_{tg} is called as body effect.

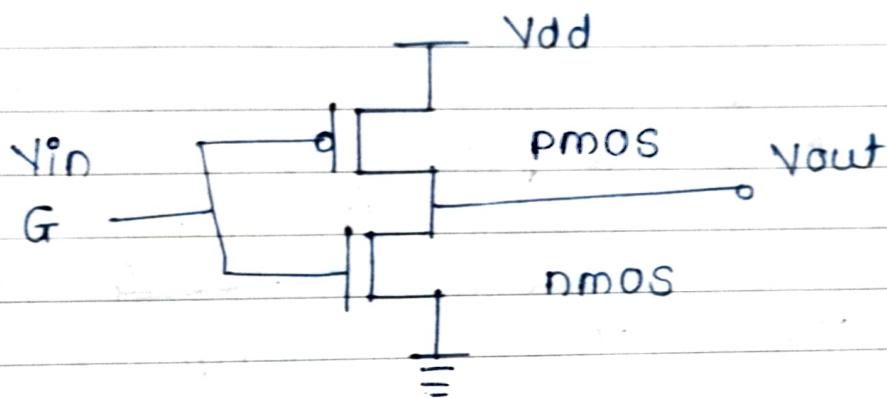
- The amount by which threshold voltage is increased is given by,

$$\Delta V_t = \gamma_n \cdot [\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}]$$

where γ_n is called as body effect factor.

* CMOS Inverter :-

- for CMOS inverter, when we provide input to circuit output is complement of input signal.
- CMOS inverter consists of PMOS connected to pull up side and NMOS connected to pull down side which act as load.



Working :-

when $V_{in} = 0$, PMOS turns ON and NMOS turn OFF, $\therefore V_{out} = V_{dd}$

when $V_{in} = V_{dd}$ ie logic 1, PMOS turns OFF and NMOS turns ON, $\therefore V_{out} = 0$

Input (V_{in})
logic 1 ie V_{dd}

logic 0 ie. 0

Output V_{out}
logic 0 ie. 0

logic 1 ie. V_{dd}

for inverter substrate of NMOS is connected to ground and that of PMOS is connected to V_{dd} .

Operation of inverter :-

operation of inverter can be divided in to five regions as shown in following fig.

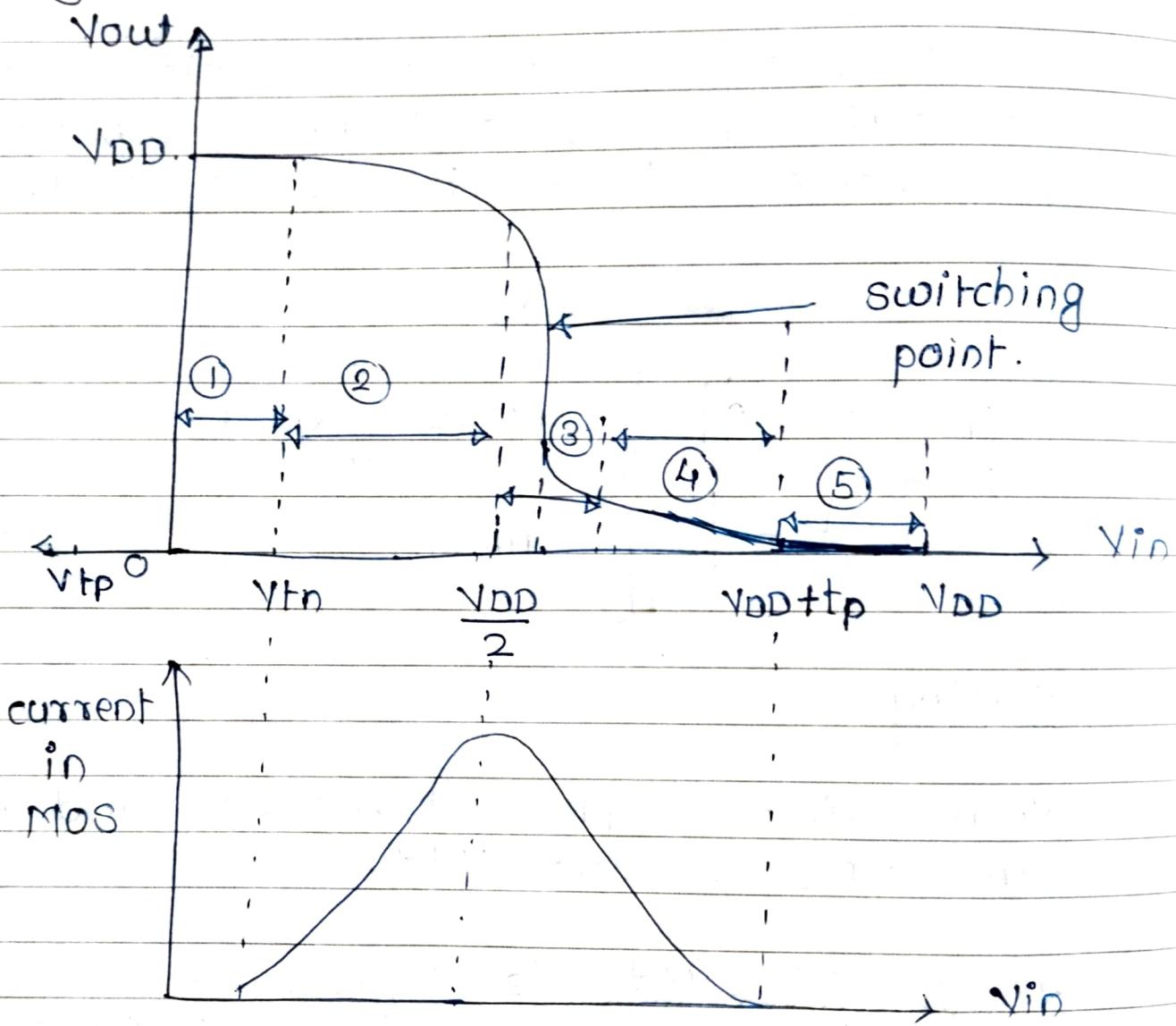


Fig. transfer chara. and current in CMOS inverter.

- CMOS transfer chara. is graph of input voltage V_{in} vs output voltage V_{out} .
- Switching of inverter takes place at $V_{DD}/2$.

Region 1 ($0 \leq V_{in} \leq V_{tn}$)

- For region 1 V_{in} is, $0 \leq V_{in} \leq V_{tn}$
- nmos is in cut off region and pmos is in linear region.
- output voltage is given by,
$$V_{out} = V_{DD}$$
.

Region 2 ($V_{tn} \leq V_{in} \leq V_{DD}/2$)

- nmos is in saturation region
- pmos is in non saturation region
- output voltage is given by,

$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - 2(V_{in} - \frac{V_{DD}}{2} - V_{tp})V_{DD} - \frac{B_n}{B_p}(V_{in} - V_{tn})^2}$$

B_n and B_p are gain factors of nmos & pmos.

Region 3

- nmos saturation
- pmos saturation
- $V_{in} = V_{DD}/2$

Region 4 $V_{DD}/2 \leq V_{in} \leq V_{DD} + V_{tp}$

- nmos nonsaturation
- pmos saturation

- output voltage is,

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 \frac{B_P}{B_N} (V_{in} - V_{DD} - V_{tp})}$$

Region 5 ($V_{in} \geq V_{DD} + V_{tp}$)

- nmos linear mode

- pmos cut off

- output voltage is,

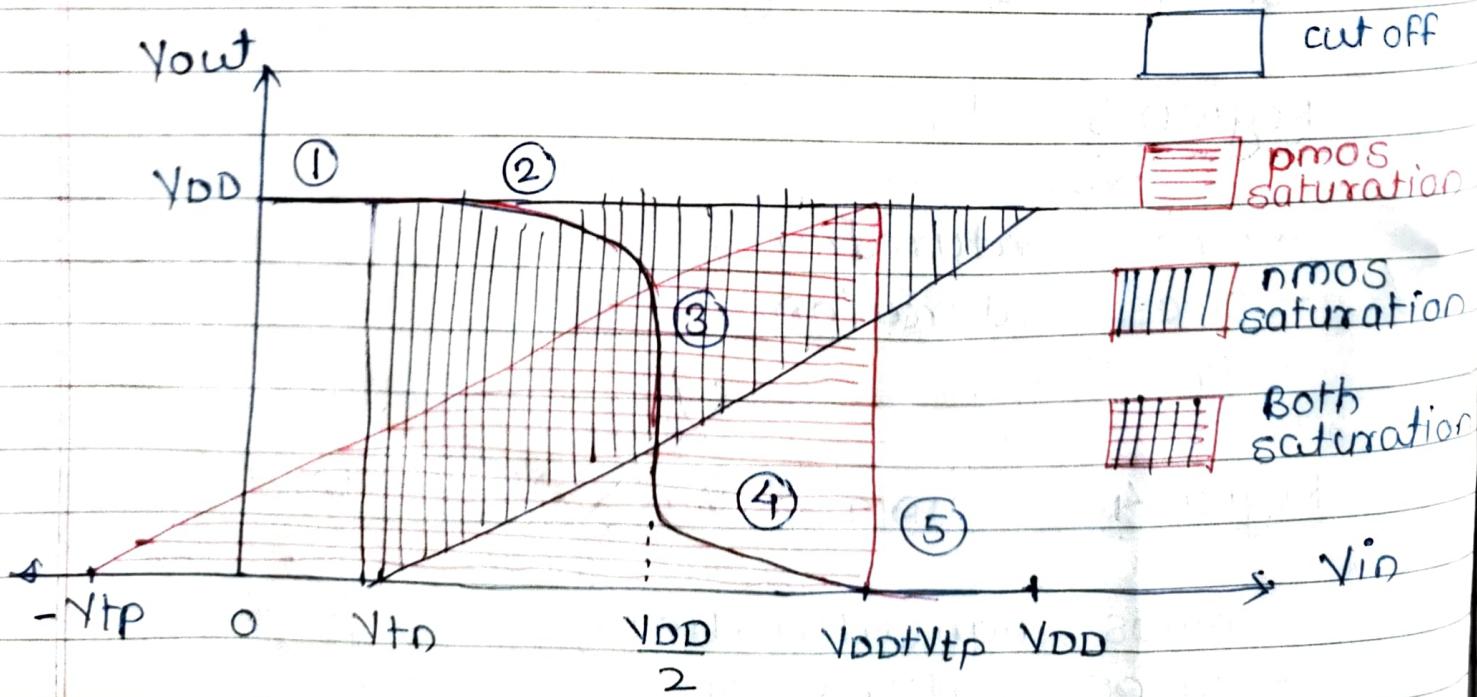
$$V_{out} = 0$$

Inverter symbol :-



inverter

Voltage transfer curve :-



Region

nmos

pmos

1	cutoff	Linear
2	saturation	linear
3	saturation	saturation
4	Linear	saturation
5	Linear	cut off

Advantages of inverter :-

- ① Low power dissipation
- ② ideal voltage level for high logic and low logic .
ie. strong high and strong 0 output
- ③ sharp transition betⁿ states which increases noise margin

cost efficient and do not require external bias

* Power Dissipation in CMOS :-

Power delivered to a gate of CMOS from the power supply is called power dissipation.

CMOS has three types of power dissipation

- ① static power dissipation

- ② dynamic power dissipation

- ③ short circuit power dissipation

Normally, power dissipⁿ is product of supply v_{tg} and current drawn from power

supply.

$$\text{ie. } P_D = V_{DD} \times I_{DC}$$

power dissipation

↓
static diss?
↓
CMOS OFF

↓
Dynamic diss?
↓
CMOS ON

↓
Short ckt
power diss?

power diss?
due to leakage
current

capacitor
charging of
CMOS results
in to power
dissipation

① static power dissipation:-

- ① In CMOS inverter, one of the transistor is always off i.e. no current flows through the device.
- ② But small amount of leakage current is present between diffusion region & body. This reverse bias leakage current is very small, therefore power dissipation is also very small.
- ③ If the temperature of junction increases, leakage current increases which results in increase in power diss?.

$$P_{\text{static}} = \text{Leakage current} \times \text{Supply voltage}$$

$$P_{\text{static}} = I_{\text{leakage}} \times V_{\text{DD}}$$

② Dynamic Power Dissipation :-

In CMOS inverter, during the transition from 0 to 1 and 1 to 0, both transistors are ON for short duration.

Due to this small current flows from V_{DD} to V_{SS} which charges and discharges the load capacitor C .

Load capacitor charged through PMOS and its voltage rises from 0 to V_{DD} .

$$P_{\text{dynamic}} = C \cdot V_{\text{DD}}^2 \cdot F_p$$

$$P_{\text{dynamic}} = C \cdot V_{\text{DD}}^2 \cdot F_p$$

where,

P_{dynamic} = Dynamic power dissipation

V_{DD} = V_{DD} Supply voltage

F_p = switching frequency

C = capacitance of load

If we increase the switching freq then dynamic power dissipation also increases.

③ Short ckt power dissipation :-

During the switching of 0 to 1 and 1 to 0 in inverter which is unloaded, some amount of short ckt current flows from V_{DD} to V_{SS} .

This short ckt current results in the power dissipation in CMOS.

$$P_{SC} = \frac{K}{12} (V_{DD} - 2V_T) \cdot \frac{3t_r}{t_p}$$

t_r = rise time = t_f = fall time

t_p = peak time

V_T = threshold voltage of the

$K = Kn = K_P$ band gap reference voltage

P_{SC} = short ckt power dissipation

V_{DD} = supply voltage

Slow rise time increases P_{SC} rapidly.

Total power dissipation can be obtained from the sum of all three dissipation.

$$P_{total} = P_{static} + P_{dynamic} + P_{SC}$$

e.g. A CMOS logic is operating at 10 MHz and 3V with the load of 100 pF. Static power dissipation is 100 μW. calc. total power dissipation if freq is increased to 100 MHz.

⇒

$$C = 100 \text{ pF} = 100 \times 10^{-12} \text{ F}$$

$$f_p = 100 \text{ MHz}$$

$$V_{DD} = 3V$$

$$P_{static} = 100 \mu\text{W}$$

$$P_{dynamic} = ?$$

$$P_{\text{dynamic}} = C \cdot V_{\text{DD}}^2 F_p$$

$$= 100 \times 10^{-12} \times 3^2 \times 100 \times 10^6$$

$$P_{\text{dynamic}} = 80 \text{ mW}$$

$$P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}}$$

$$= 100 \times 10^{-6} + 80 \times 10^{-3}$$

$$\boxed{P_{\text{total}} = 80.1 \text{ mW}}$$

* Power Delay Product :-

- Power delay product is product of power consumption and duration of switching event.
- Power delay product measures the energy of gate.

i.e. $PDP = P_{\text{avg}} \times t_p$

PDP = power delay product

t_p = switching duration

P_{avg} = average power

- PDP stands for average energy consumed per switching events.
- It is used to determine the quality of digital gate.
- PDP also known as switching energy.

- when the gate is switched as its maximum possible rate f_{max} ,

$$P_{avg} \times f_{max} = \frac{t_{HOL} + t_{PLH}}{2 t_p}$$

$$t_p = (t_{PHL} + t_{PLH}) / 2$$

$$PDP = P_{avg} \times f_{max} = I_{load}^2$$

$$= I_{load}^2 \cdot 2 \cdot f_{max} \cdot \rho_{load}$$

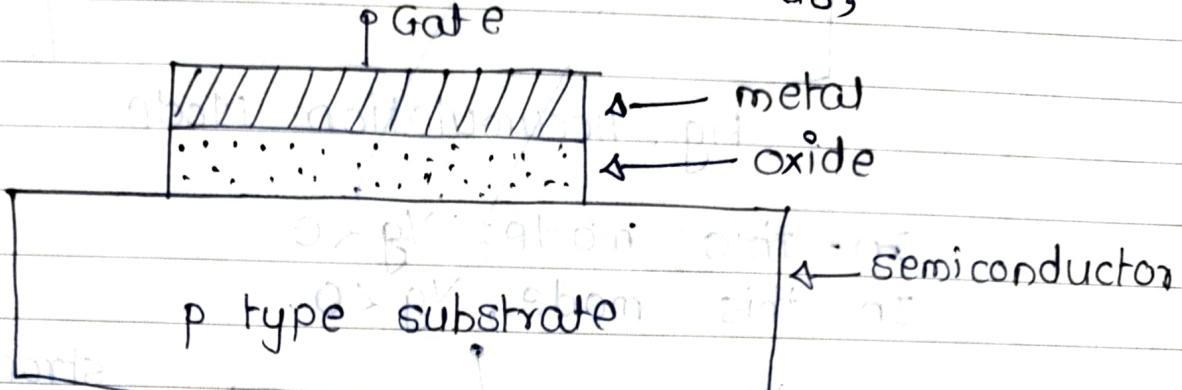
but $t_p = \frac{2C}{K \cdot V_{DD}}$

$$\therefore PDP = \frac{2 \cdot V_{DD} \cdot C^2 \cdot F}{K \cdot V_{DD}}$$

- In VLSI, design goal is to minimize the PDP, in order to get minimum power at high frequencies.
- Thus to decrease PDP, it is important to decrease V_{DD} as well as load capacitor (C) value.
- At high frequencies, power dissipation is dominated by load capacitance.

* MOS capacitor :-

General MOS structure is shown as,



In MOS oxide layer is present between metal and semiconductor. Since oxide is very good insulator, it forms oxide capacitance in the circuit.

operation :-

Depending upon value of gate voltage applied, MOS capacitor works in three modes

- a) Accumulation
- b) Depletion
- c) Strong inversion

MOS capacitance changes its value with the variation in gate voltage.

a) Accumulation Mode :-

In this mode there is accumulation of holes (assuming n-MOS) at the Si-SiO₂ interface. All the field lines originating from gate terminates on this layer giving dielectric thickness as oxide thickness. as shown in fig.

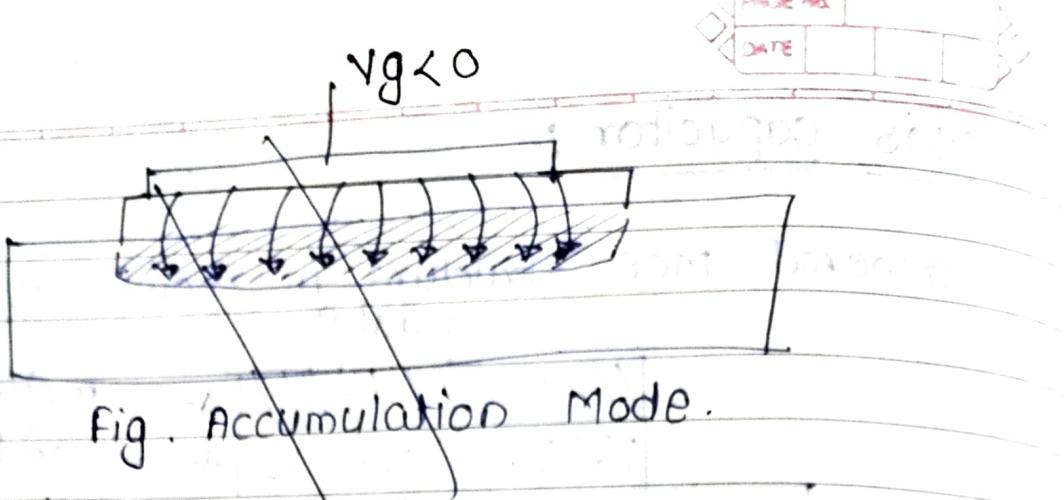


Fig. Accumulation Mode.

In this mode, $V_g < 0$.

In this mode, $V_g < 0$.

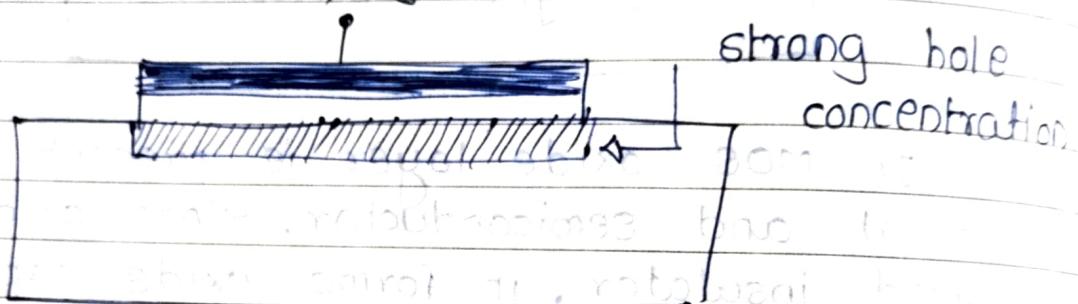


fig. a. Accumulation layer.

b) Depletion Mode :-

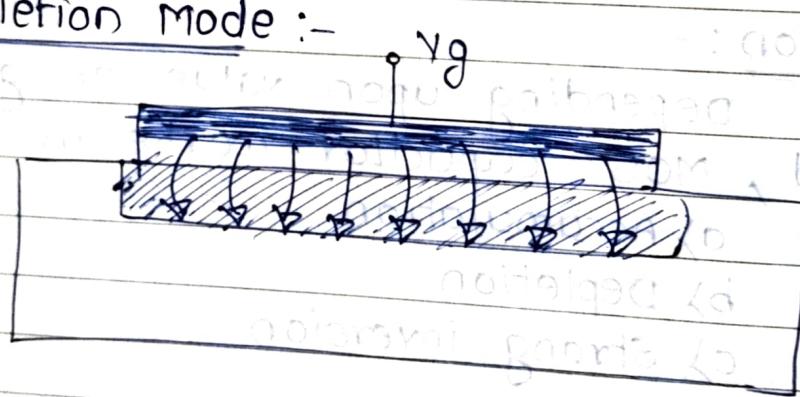


fig.b
depletion mode

As we move from negative voltage to positive voltage, the holes at the interface are repelled and push back in to bulk leaving a depletion layer.

This layer counters a positive charge on gate and keep increasing till the gate voltage is below threshold voltage. as shown in fig. b.

c) Strong inversion :-

When V_{GS} crosses threshold voltage, the increase in depletion region width stops and charge on layer is countered by mobile electrons at Si-SiO₂ interface. This is called inversion because mobile charges are opposite to the types of charges found in substrate. In this mode the inversion layer is formed by electrons. Thus it reduces dielectric thickness as shown in fig c.

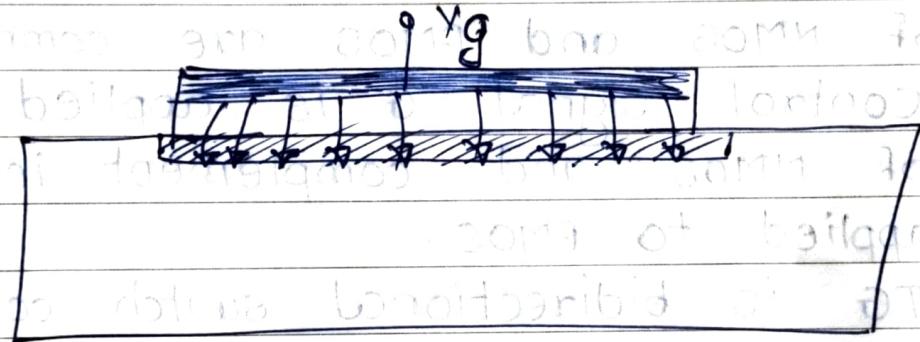


Fig.c Strong inversion mode.

Oxide capacitance can be given as,

$$C_{ox} = \frac{\epsilon_0}{t_{ox}}$$

where,

C_{ox} = oxide capacitance

ϵ_0 = dielectric constant of oxide

t_{ox} = thickness of oxide

* Transmission Gate :-

Transmission gate (TG) is also called as pass gate which gives strong 1 for 1 input and strong 0 for 0 input.

construction :-

- IF TG, NMOS and PMOS are connected such that source and drain terminals of NMOS and PMOS are common.
- control signal G is applied to gate of NMOS and complement ie. \bar{G} is applied to PMOS.
- TG is bidirectional switch controlled by gate signal G.

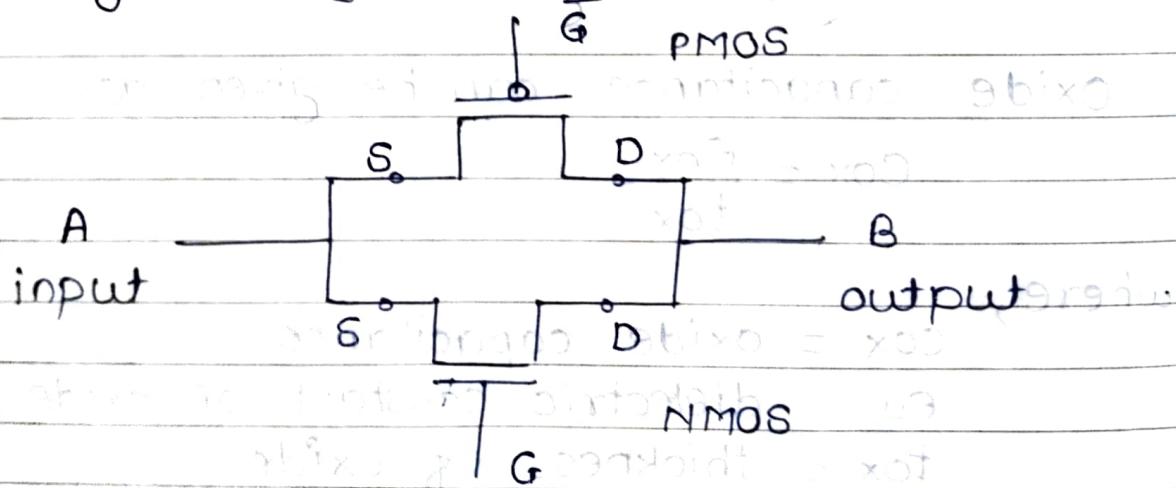
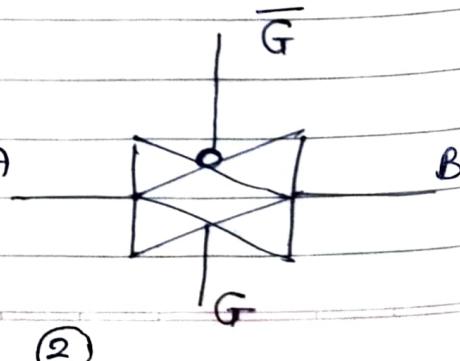
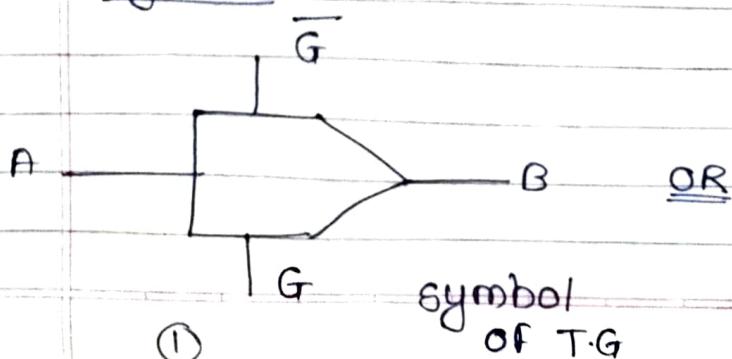
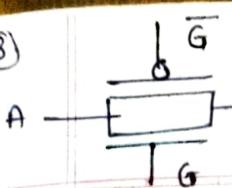


Fig. construction of TG.

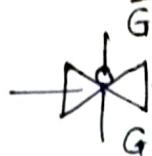
symbol



③



OR



symbol

Working :-When $G=1 = V_{dd} = \text{High} \Rightarrow$ ie. $\bar{G}=0$ PMOS \rightarrow gate 0 \rightarrow ONNMOS \rightarrow gate 1 \rightarrow ONPMOS \rightarrow gate 1 \rightarrow OFFNMOS \rightarrow gate 0 \rightarrow OFF

- When $G=1$, NMOS is ON and PMOS is also ON.
- Both transistors are ON and provide low resistance path between node A and B.
- \therefore input provided at A will be available at B.

When $G=0 = Gnd = \text{Low} \Rightarrow$ ie. $\bar{G}=\Phi$ \rightarrow NMOS is OFF as $G=0$ \rightarrow PMOS is OFF as $\bar{G}=1$ \rightarrow Both transistor act as open ckt and provide high impedance path betⁿ A & B. \rightarrow No o/p will be available at B for i/p at BApplications :-

- Electronics switches
- Analog multiplexers
- logic circuits
- Analog to digital converter