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**UNI-VLSI-V1**

# VLSI Development Board User Manual

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## Chapter 1: Introduction

Thank you for purchasing the Xilinx Spartan™-3E based VLSI Development Board (**UNI-VLSI-V1**). You will find it useful in developing your Spartan-3E FPGA application. The board provides easy to use development platform for implementing digital designs.

### *Key Components and Features:*

The key features of the VLSI Development board are:

- Spartan-3E XC3S250E FPGA
  - Up to 172 user-I/O pins
  - 208-pin FBGA package
  - Over 5,000 logic cells
- 2-line, 16-character LCD screen
- Two 9-pin RS-232 ports (DTE- and DCE-style)
- 32 discrete LEDs and DIP switches
- PS/2 mouse or keyboard port
- Separate VGA display port
- Expansion connectors (32 free user I/O arranged in 10 pin FRC)
- Dual, 8 bit DAC
- 8 bit, 8 channel ADC
- USB interface(type B)
- 8 pushbuttons for trigger, input
- 6 common anode 7-segment LED display
- Xilinx 2 Mbit Platform Flash configuration PROM

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## Chapter 2: LCD 16x2 Interface

The **UNI-VLSI-V1** board includes 2 lines by 16 characters LCD (liquid crystal display) Module. The dot matrix LCD displays alphanumeric characters, numbers and symbols. For displaying characters, numbers and symbol, user needs to send 8 bit ASCII value on data pins (Data0-Data8). The user can control the LCD display by controlling control lines (RS, EN) and sending command codes on data pins.

All the functions required for controlling LCD backlight are provided internally on board. Internal refresh is provided by the controller. The Interface details of the LCD display are as shown in figure 2.1.

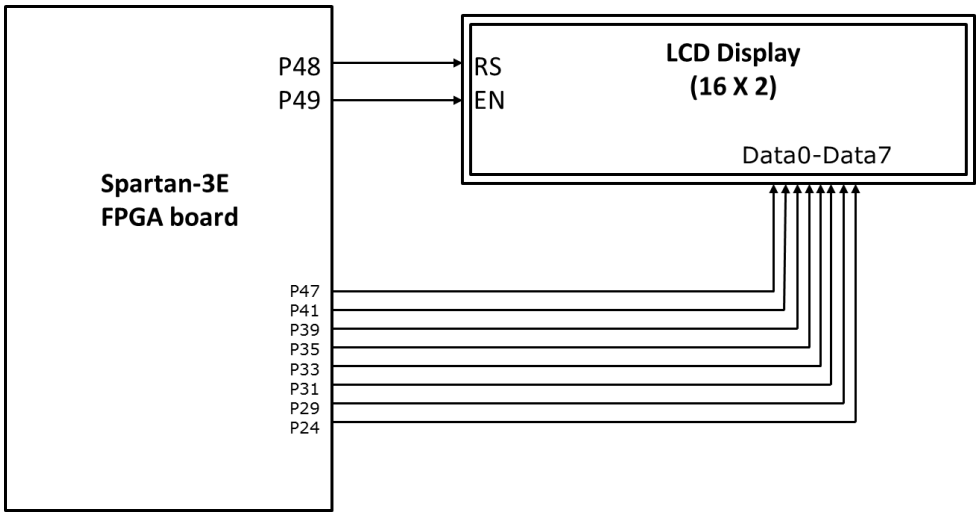


Figure 2.1: Interfacing of LCD with FPGA

**Pin Assignment (UCF Location) for LCD:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| LCD_RS | P48 | P74 |
| LCD_EN | P49 | P72 |
| LCD_Data0 | P47 | NC |
| LCD_Data1 | P41 | NC |
| LCD_Data2 | P39 | NC |
| LCD_Data3 | P35 | NC |
| LCD_Data4 | P33 | P66 |
| LCD_Data5 | P31 | P61 |
| LCD_Data6 | P29 | P59 |
| LCD_Data7 | P24 | P58 |

Table 2.1: Pin Assignmnet (UCF) for LCD

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## Chapter 3: Multiplexed Seven Segment LED Interface

The **UNI-VLSI-V1** board has a six common anode seven segment LED display arranged in time multiplexed manner and controlled by FPGA user-I/O pins as shown in figure 3.1.

To display all six digits, each display is selected sequentially one after another in time division multiplexed manner above a minimum rate to get flicker free display. If each digit is scanned more than 30 times per second, a flicker free display is obtained.

Each display is selected by lowering its enable signal. All displays shares eight common control signals to turn ON the LED segments corresponding to enabled display. The display data inputs, A through G and DP, drive the individual segments that comprise the character. A Low value lights the individual segment, a High turns off the segment.

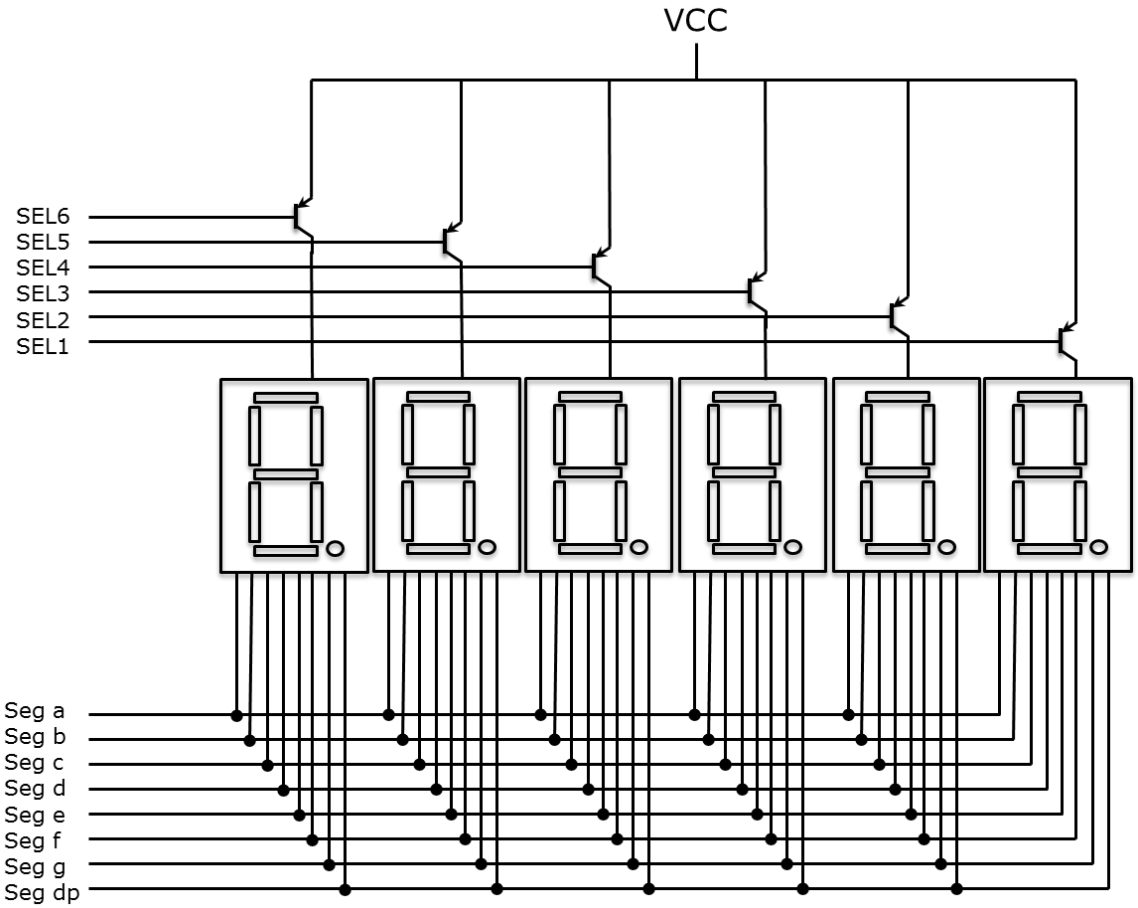


Figure 3.1: Multiplexed six seven segment displays

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**Pin Assignment (UCF Location) for 7-Segment Display:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| Sel_DIS1 | P23 | P57 |
| Sel_DIS2 | P18 | P50 |
| Sel_DIS3 | P15 | P47 |
| Sel_DIS4 | P4 | P35 |
| Sel_DIS5 | P9 | P45 |
| Sel_DIS6 | P12 | P43 |
| Segment_a | P8 | P56 |
| Segment_b | P16 | P51 |
| Segment_c | P3 | P44 |
| Segment_d | P2 | P33 |
| Segment_e | P11 | P34 |
| Segment_f | P19 | P48 |
| Segment_g | P22 | P41 |
| Segment_dp | P5 | P40 |

Table 3.1: Pin Assignment (UCF) for 7-Segment LED Display

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## Chapter 4: LED's and DIP Switches Interface

The **UNI-VLSI-V1** board has 32 individual bidirectional I/O's. Each I/O is connected with a surface-mount LED and a DIP switch. A LED is assigned to each I/O to indicate its data status when I/O is configured as input. DIP switch is used to provide digital input (i.e. logic 0 and logic 1) to the FPGA.

The LED can display the output data value of I/O by configuring it as output and keeping its corresponding DIP switch at 0 positions.

The LEDs are divided in four groups of 8 LED based on 8-pin DIP switches I/O's are labeled as TL1 to TL32. (SW1:TL1-TL8, SW2:TL9-TL16, SW3:TL17-TL-24, SW4:TL25-TL32).

**Pin Assignment (UCF Location) for IOs:**

| DIP Switch | Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 | DIP Switch | Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|---|---|---|---|---|
| SW1 | TL1 | P205 | P29 | SW3 | TL17 | P179 | NC |
| | TL2 | P206 | P30 | | TL18 | P180 | NC |
| | TL3 | P203 | P26 | | TL19 | P177 | NC |
| | TL4 | P200 | P23 | | TL20 | P178 | NC |
| | TL5 | P202 | P24 | | TL21 | P152 | NC |
| | TL6 | P197 | P21 | | TL22 | P168 | NC |
| | TL7 | P199 | P22 | | TL23 | P171 | NC |
| | TL8 | P196 | P17 | | TL24 | P172 | NC |
| SW2 | TL9 | P192 | P11 | SW4 | TL25 | P165 | NC |
| | TL10 | P193 | P12 | | TL26 | P167 | NC |
| | TL11 | P189 | P9 | | TL27 | P163 | NC |
| | TL12 | P190 | P10 | | TL28 | P164 | NC |
| | TL13 | P186 | P144 | | TL29 | P161 | NC |
| | TL14 | P187 | P2 | | TL30 | P162 | NC |
| | TL15 | P185 | P5 | | TL31 | P160 | NC |
| | TL16 | P181 | P6 | | TL32 | P153 | NC |

Table 4.1: Pin Assignment (UCF) for LED's and DIP switches

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## Chapter 5: Pushbuttons Interface

The **UNI-VLSI-V1** board has 8 individual pushbuttons for input purpose. The pushbuttons are read as 0 when pushed. They are read as 1 in normal (unpressed) condition. Pushbuttons are labeled as K0 to K7.

### Pin Assignment (UCF Location) for Pushbuttons:

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| K0 | P204 | P27 |
| K1 | P194 | P16 |
| K2 | P184 | P15 |
| K3 | P183 | P14 |
| K4 | P174 | P7 |
| K5 | P175 | P8 |
| K6 | P169 | NC |
| K7 | P159 | NC |

Table 5.1: Pin Assignment (UCF) for Pushbuttons

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## Chapter 6: ADC Interface

The **UNI-VLSI-V1** board includes a ADC 0808. The ADC has 8 analog input channels. The channels are selected by setting the address pins of ADC. Among the eight channels, input to channel 6 and 7 is given by molex connecter, another molex connector dedicated for the GND beside them. The analog input to channel 5 to 2 is given by external circuit through relimate pins. The variable analog input to channels 0 and channel 1 is given through 10k pot. The other controlling signals of ADC are interfaced with FPGA board as shown in figure 3.

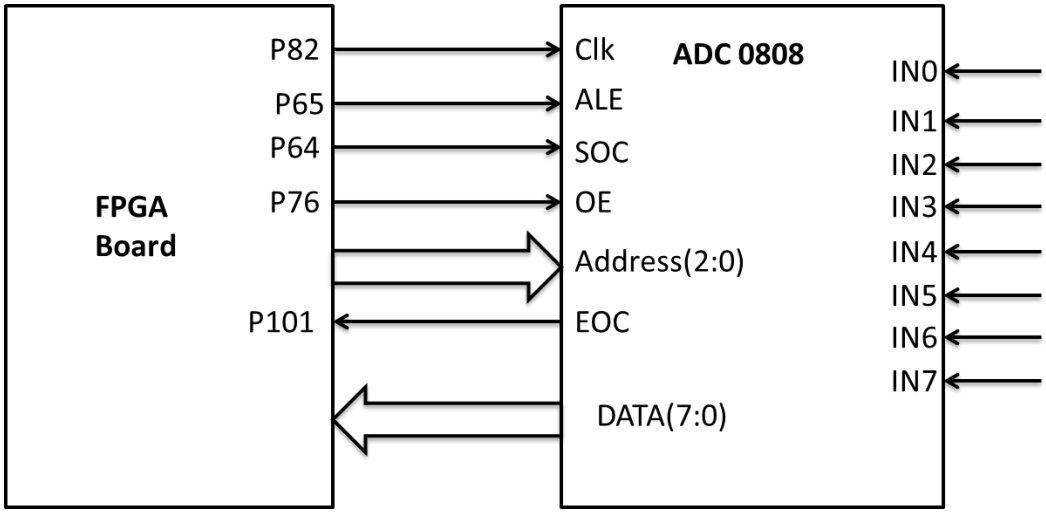


Figure 6.1: Interfacing of ADC with FPGA

**Pin assignment (UCF Location) for ADC 0808:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| ADC_DATA 0 | P71 | P87 |
| ADC_DATA 1 | P72 | P88 |
| ADC_DATA 2 | P54 | P79 |
| ADC_DATA 3 | P51 | P78 |
| ADC_DATA 4 | P89 | P95 |
| ADC_DATA 5 | P91 | P97 |
| ADC_DATA 6 | P57 | P80 |
| ADC_DATA 7 | P58 | P81 |
| ADC_EOC | P101 | P98 |
| ADC_ADD 0 | P69 | P85 |
| ADC_ADD 1 | P68 | P84 |
| ADC_ADD 2 | P74 | P92 |

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| | | |
|---|---|---|
| ADC_SOC | P64 | P82 |
| ADC_ALE | P65 | P83 |
| ADC_CLK | P82 | P94 |
| ADC_OE | P76 | P93 |

Table 6.1: Pin assignment (UCF) for ADC

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## Chapter 7: DAC Interface

The **UNI-VLSI-V1** board includes a dual, 8-bit, digital-to-analog converter (DACs). TLC7528 has separate on-chip data latches. Data are transferred to either of the two DAC data latches through a common, 8-bit, input port. Control input DACA/B determines which DAC is to be loaded. Low on DACA/B selects ADC A. TLC7528 allows easy interface to most popular microprocessor buses and output ports. DAC works on 5V. The figure 4 shows the interfacing diagram of DAC with FPGA Board.

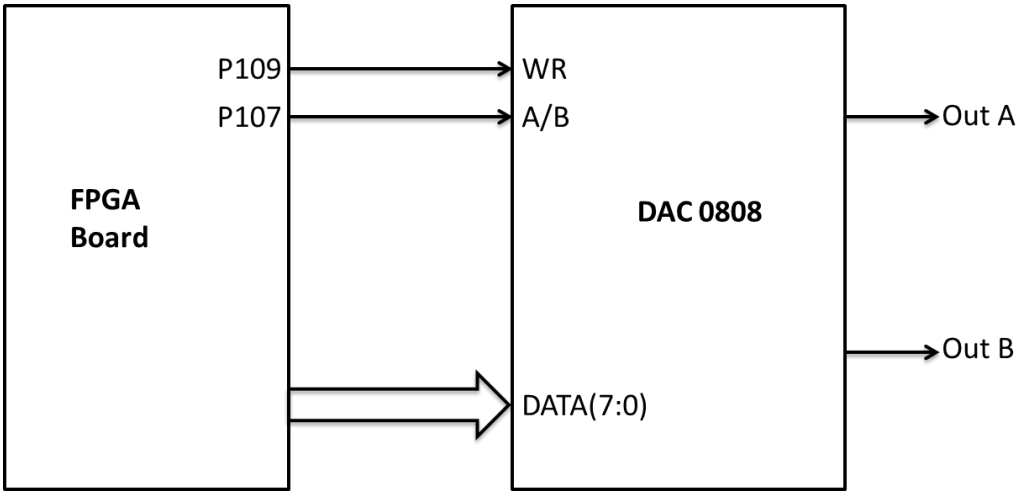


Figure 7.1: Interfacing diagram of DAC with FPGA

**Pin Assignment (UCF Location) DAC TLC7528:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| DAC_DATA 0 | P116 | P114 |
| DAC_DATA 1 | P119 | P116 |
| DAC_DATA 2 | P120 | P115 |
| DAC_DATA 3 | P122 | P117 |
| DAC_DATA 4 | P115 | P111 |
| DAC_DATA 5 | P113 | P112 |
| DAC_DATA 6 | P112 | P105 |
| DAC_DATA 7 | P108 | P104 |
| DAC_WR | P109 | P102 |
| DAC_A_B | P107 | P101 |

Table 7.1: Pin Assignment (UCF) for DAC

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## Chapter 8: PS/2 Mouse/Keyboard Port

The **UNI-VLSI-V1** board includes a PS/2 interface for keyboard and mouse connection using a standard 6 pin PS/2 connector as shown in figure 8.1.

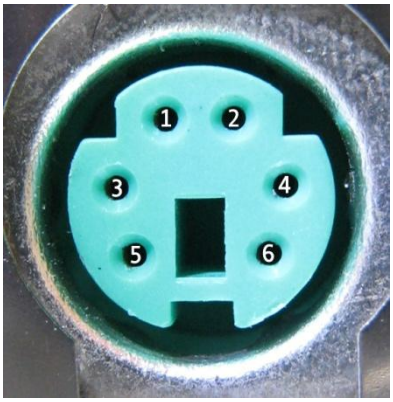


Figure 8.1: PS/2 Connector

Both a PC mouse and keyboard use the two-wire PS/2 serial bus to communicate with a host device, the SPARTAN -3E FPGA in this case. The PS/2 bus includes both clock and data. Both a mouse and keyboard drive the bus with identical signal timings and both use 11-bit words that include a start, stop and odd parity bit. However, the data packets are organized differently for a mouse and keyboard. Furthermore, the keyboard interface allows bidirectional data transfers.

| PS/2 Connector Pin | Signal |
|---|---|
| 1 | DATA(PS2D) |
| 2 | Reserved |
| 3 | GND |
| 4 | Voltage Supply |
| 5 | CLK(PS2C) |
| 6 | Reserved |

Table 8.1: PS/2 Connector Details

The PS/2 bus timing appears in Table 8.2 and Figure 8.2. The clock and data signals are only driven when data transfers occur, and otherwise they are held at logic High - in the idle state. The timings define signal requirements for

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mouse-to-host communications and bidirectional keyboard communications. As shown in Figure 11, the attached keyboard or mouse writes a bit on the data line when the clock signal is high, and the host reads the data line when the clock signal is low.

| Symbol | Parameter | Min | Max |
|---|---|---|---|
| $T_{CK}$ | Clock high or low time | 30µs | 50µs |
| $T_{SU}$ | Data to clock setup time | 5µs | 25µs |
| $T_{HLD}$ | Clock to data hold time | 5µs | 25µs |

Table 8.2: PS/2 Bus Timing

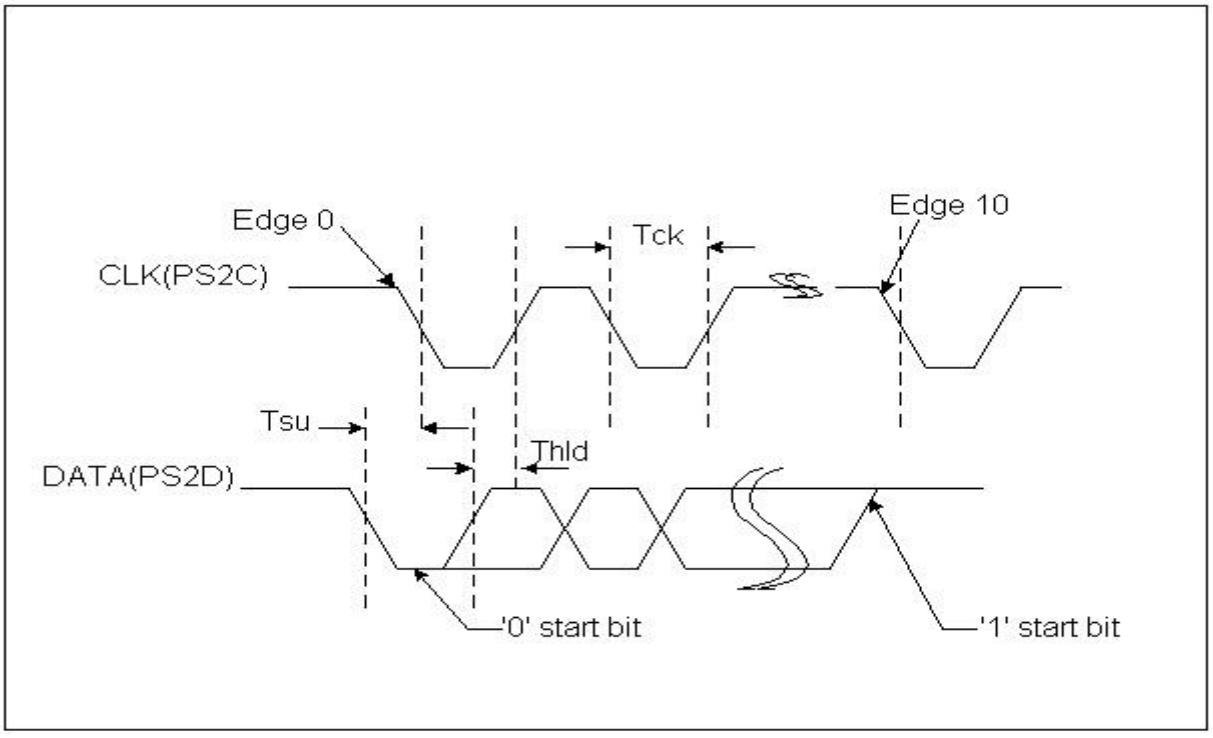


Figure 8.2: PS/2 Timing Diagram

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### *PS/2 Keyboard Commands*

The most commonly used commands for PS/2 keyboard are as follows

| Command | Description |
|---|---|
| ED | Turn on/off Num Lock, Caps Lock, and Scroll Lock LEDs. The keyboard acknowledges receipt of an "ED" command by replying with an "FA", after which the host sends another byte to set LED status. The bit positions for the keyboard LEDs appear in Table 13. Write a '1' to the specific bit to illuminate the associated keyboard LED. |
| EE | Upon receiving an echo command, the keyboard replies with the same scan code "EE". |
| FE | Resend. Upon receiving a resend command, the keyboard resends the last scan code sent. |
| FF | Reset. Resets the keyboard. |
| F3 | Set scan code repeat rate. The keyboard acknowledges receipt of an "F3" by returning an "FA" after which the host sends a second byte to set the repeat rate. |

Table 8.3: Common PS/2 Keyboard Commands

The keyboard sends data to the host only when both the data and clock lines are High, the idle state.
Because the host is the "bus master", the keyboard checks whether the host is sending data before driving the bus. The clock line can be used as a "clear to send" signal. If the host pulls the clock line Low, the keyboard must not send any data until the clock is released. The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by eight bits of scan code (LSB first), followed by an odd parity bit and terminated with a '1' stop bit. When the keyboard sends data, it generates 11 clock transitions at around 20 to 30 kHz, and data is valid on the falling edge of the clock as shown in Figure 8.2.

**Pin Assignment (UCF Location) for PS/2 Connector**

Only pin 1 and pin 5 of connector are connected to FPGA board.

| Signal Name | XC3S250E-PQ208 |
|---|---|
| PS2_CLK | P25 |
| PS2_DATA | P26 |

Table 8.4: Pin Assignment (UCF) for PS/2 Connector

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## Chapter 9: VGA Display Port

The **UNI-VLSI-V1** board includes a VGA display port via a DB15 connector. Connect this port directly to most PC monitors or flat-panel LCDs using a standard monitor cable.

The Spartan-3E FPGA directly drives the five VGA signals via resistors. Each color line has a series resistor, with one bit each for VGA_RED, VGA_GREEN, and VGA_BLUE. The series resistor, in combination with the termination resistance built into the VGA cable, ensures that the color signals remain in the VGA-specified 0V to 0.7V range. The interfacing diagram of DB15 with FPGA board is shown in figure 9.1.

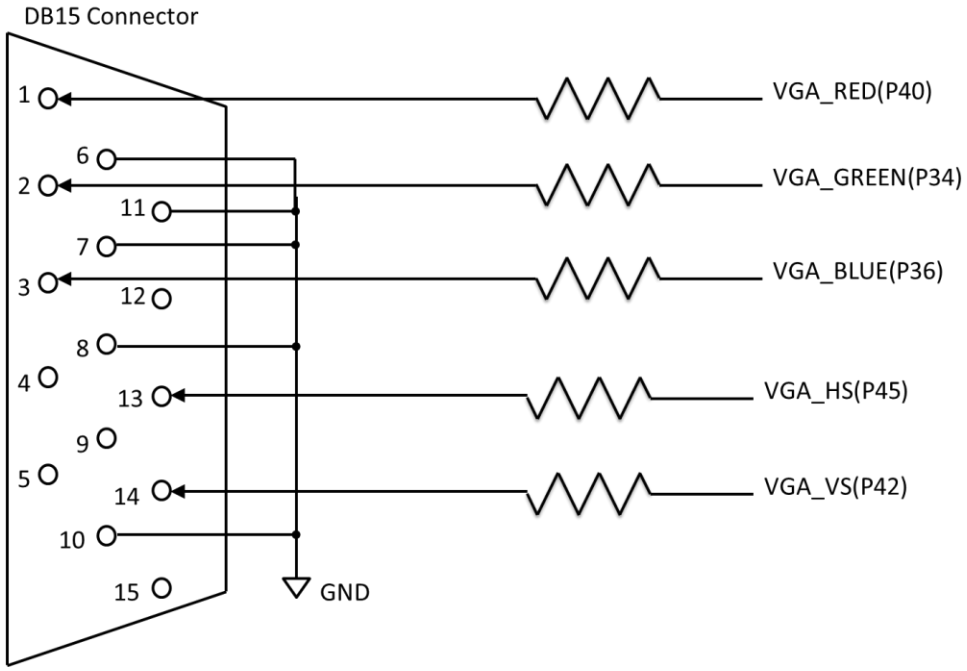


Figure 9.1: Interfacing diagram of VGA connector with FPGA

The VGA_HSYNC and VGA_VSYNC signals using LVTTL or LVCMOS33 I/O standard drive levels. Drive the VGA_RED, VGA_GREEN, and VGA_BLUE signals High or Low to generate the eight colors shown in table 9.1.

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| VGA_RED | VGA_GREEN | VGA_BLUE | Color |
|---|---|---|---|
| 0 | 0 | 0 | Black |
| 0 | 0 | 1 | Blue |
| 0 | 1 | 0 | Green |
| 0 | 1 | 1 | Cyan |
| 1 | 0 | 0 | Red |
| 1 | 0 | 1 | Magenta |
| 1 | 1 | 0 | Yellow |
| 1 | 1 | 1 | White |

Table 9.1: 3 bit Display Color Codes

**Pin Assignment (UCF location) for VGA Display Port:**

| Pin Description | XC3S250E-PQ208 |
|---|---|
| VGA_RED | P40 |
| VGA_GREEN | P34 |
| VGA_BLUE | P36 |
| VGA_HS | P45 |
| VGA_VS | P42 |

Table 9.2: Pin Assignment (UCF) for VGA Display

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## Chapter 10: RS232 Serial Port

The **UNI-VLSI-V1** board has two RS-232 serial ports:

- A female DB9 DCE connector
- A male DB9 DTE connector

The DCE-style port connects directly to the serial port connector available on most personal computers and Workstations via a standard straight-through serial cable.

The FPGA supplies serial output data using LVTTL or LVCMOS levels to the RS-232 voltage converter which converts the logic value provided by FPGA Board to the appropriate RS-232 voltage level and vice-versa. MAX 3232 is used as voltage converter which has as 3.3V as logic high.

The connection between the FPGA and the DB9 connectors is shown in figure 10.1. Hardware flow control is not supported on the connector. The port's DCD, DTR, and DSR signals connect together. Similarly, the port's RTS and CTS signals connect together.

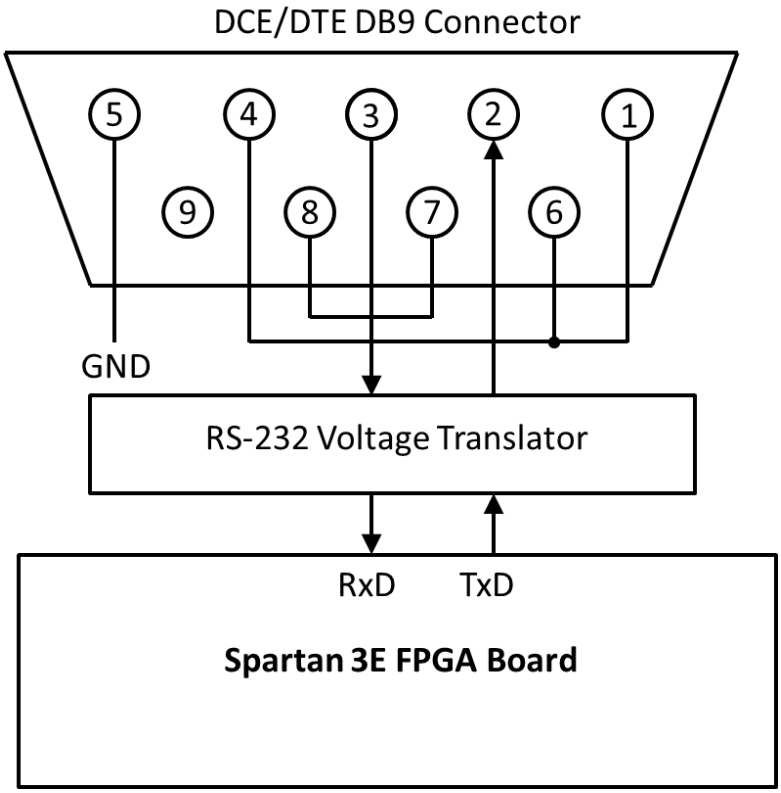


Figure 10.1: Interfacing of DCE or DTE DB9 connector with FPGA

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**Pin Assignment (UCF Location) for RS232 Serial Ports:**

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| TxD_F | P30 | P67 |
| RxD_F | P43 | P62 |

Table 10.1: Pin Assignment (UCF) for Female DB9 DCE Connector

| Signal Name | XC3S250E-PQ208 |
|---|---|
| TxD_M | P28 |
| RxD_M | P32 |

Table 10.2: Pin Assignment (UCF) for Male DB9 DTE Connector

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## Chapter 11: USB Interface

The **UNI-VLSI-V1** board has USB interface using device FT232HL from FTDI. This act as USB to UART converter so that Communication with FPGA can accomplished by USB port. The Chip also generates the different clocks which can be used as the clock source for FPGA (See Chapter 12).

### Pin Assignment (UCF Location) for USB interface:

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| USB_Rx | P106 | P99 |
| USB_TX | P100 | P100 |

Table 11.1: Pin Assignment (UCF) for USB

## Chapter 12: Clock Sources

The **UNI-VLSI-V1** board supports multiple clock input sources which are listed below.

- The board includes an on-board 12 MHz clock oscillator
- Three Clock outputs form USB to UART IC FT232HL.
  - 7.5 MHz, 15 MHz, 30MHz
- 32 KHz Clock output from RTC IC3231.
- Variable Clock using IC555. The Clock is varied using potentiometer PR1.

### Pin Assignment (UCF Location) for Clock Sources:

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| RESET | -- | P32 |
| Clock_12MHz | P80 | P55 |
| Clock_7.5MHz | P78 | NC |
| Clock_15MHz | P77 | NC |
| Clock_30MHz | P83 | NC |
| Clock_32kHz | P75 | NC |
| Clock_555 | P132 | P120 |

Table 12.1: Pin Assignment (UCF) for Clock sources

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## Chapter 13: RTC Interface

The **UNI-VLSI-V1** board has a RTC for time keeping purpose. The RTC used is DS3231 which is an extremely accurate I2C real time clock (RTC) with an integrated temperature compensated crystal oscillator (TCXO) and crystal. RTC operates on a battery input of 3.3V, and maintains accurate timekeeping when main power to the device is interrupted.

The RTC maintains seconds, minutes, hours, day, date, month, and year information with Leap Year Compensation Valid Up to 2100. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Address and data are transferred serially through an I2C bidirectional bus.

### Pin Assignment (UCF Location) for RTC:

| Signal Name | XC3S250E-PQ208 |
|---|---|
| RTC_SDA | P61 |
| RTC_SCL | P62 |

Table 13.1: Pin Assignment (UCF) for RTC

## Chapter 14: Buzzer Interface

The **UNI-VLSI-V1** board has a buzzer for audio indication of a signal. The buzzer will turn ON by making high the buzzer pin on FPGA board, configuring it as output. The interfacing of buzzer with FPGA board is as shown in figure 14.1. Buzzer section the development board is shown in figure 15.1 (see Chapter 15).

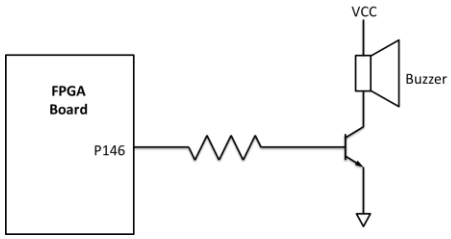


Figure 14.1: Interfacing of Buzzer with FPGA

### Pin Assignment (UCF Location) for Buzzer:

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| Buzzer | P146 | P139 |

Table 14.1: Pin Assignment (UCF) for Buzzer

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## Chapter 15: RGB LED Interface

The **UNI-VLSI-V1** board has a RGB LED. The LED has 4 terminals - Red, Green, Blue and Ground. Logic high is applied to R/G/B terminals to generate a chromatic signal corresponding to R, G and B signals. The LED can be used to observe the PWM signal.

### Pin Assignment (UCF Location) for RGB LED:

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| LED_Red | P151 | P140 |
| LED_Green | P150 | P142 |
| LED_Blue | P147 | P143 |

Table 15.1: Pin Assignment (UCF) for RGB LED

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## Chapter 16: Expansion Connectors

The **UNI-VLSI-V1** board provides expansion connectors for easy interface flexibility to other off-board components. Total 32 bidirectional I/O's (Some are dedicated input pins, see pin assignment) are available to the user through FRC expansion headers. The bidirectional I/O can be configured as input or output. The board includes the four 10-pin FRC I/O expansion headers. Each 10-pin FRC consists 8 I/Os along with VCC and GND.
The expansion I/O's can be interfaced with external circuitry for data input/output purpose such as controlling ON/OFF of relay, motors, square wave of various frequency, etc.

**Pin Assignment (UCF Location) for Expansion Connectors:**

| Pin number (FRC J10) | FPGA Pin/ Location | Direction/ Purpose |
|---|---|---|
| 1 | 102 | inout |
| 2 | 98 | Inout |
| 3 | 99 | Inout |
| 4 | 96 | Inout |
| 5 | 97 | Inout |
| 6 | 93 | Inout |
| 7 | 94 | Inout |
| 8 | 90 | Inout |
| 9 | +3.3v | Supply |
| 10 | Gnd | Gnd |

Table 16.1: Pin Assignment (UCF) for FRC Connector **J10**

| Pin number (FRC J12) | FPGA Pin/ Location | Direction/ Purpose |
|---|---|---|
| 1 | 118 | input |
| 2 | 110 | input |
| 3 | 123 | Inout |
| 4 | NC | NC |
| 5 | 124 | Input |

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| | | |
|---|---|---|
| 6 | 126 | Inout |
| 7 | 127 | Inout |
| 8 | 128 | Inout |
| 9 | +3.3v | Supply |
| 10 | Gnd | Gnd |

Table 16.2: Pin Assignment (UCF) for FRC Connector **J12**

| Pin number (FRC J14) | XC3S250E-PQ208 | Direction/ Purpose | XC6SLX9-TQG144 | Direction/ Purpose |
|---|---|---|---|---|
| 1 | 138 | Inout | P119 | I/O |
| 2 | 142 | input | P118 | I/O |
| 3 | 140 | Inout | P123 | I/O |
| 4 | 145 | Inout | P121 | I/O |
| 5 | 144 | Input | P126 | I/O |
| 6 | 148 | input | P124 | I/O |
| 7 | 154 | input | P132 | I/O |
| 8 | 14 | input | P127 | I/O |
| 9 | +3.3v | Supply | +3.3v | Supply |
| 10 | Gnd | Gnd | Gnd | Gnd |

Table 16.3: Pin Assignment (UCF) for FRC Connector **J14**

| Pin number (FRC J15) | XC3S250E-PQ208 | Direction/ Purpose | XC6SLX9-TQG144 | Direction/ Purpose |
|---|---|---|---|---|
| 1 | 130 | input | P131 | I/O |
| 2 | 129 | Inout | P134 | I/O |
| 3 | 134 | Inout | P133 | I/O |
| 4 | 133 | Inout | P138 | I/O |
| 5 | 136 | Input | P137 | I/O |
| 6 | 135 | Inout | P141 | I/O |

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| | | | | |
|---|---|---|---|---|
| 7 | 139 | Inout | P1 | I/O |
| 8 | 137 | Inout | P46 | I/O |
| 9 | +3.3v | Supply | +3.3v | Supply |
| 10 | Gnd | Gnd | Gnd | Gnd |

Table 16.4: Pin Assignment (UCF) for FRC Connector **J15**

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## Chapter 17: Configuration Options

The **UNI-VLSI-V1** board supports a two FPGA configuration options:

1. Boundary Scan Mode
2. Master Serial Mode

The configuration mode jumpers determine which configuration mode the FPGA uses when power is first applied, or whenever the **CONFIG RST** button is pressed. The DONE pin LED lights when the FPGA successfully finishes configuration. Pressing the CONFIG RST button forces the FPGA to restart its configuration process.

### *Boundary Scan Mode*

In boundary scan mode of configuration the SPARTAN-3 FPGA is directly configured via a on board JTAG port using the dedicated configuration pins TCK, TMS, TDI and TDO. The on-board JTAG port also provides in-system programming for the on-board Platform Flash PROM.

The jumper setting for selection of boundary scan mode is discussed in configuration jumper settings section.

### *Master Serial Mode*

In master serial mode first Program the on-board 2 Mbit Xilinx XCF02S serial Platform Flash PROM, then PROM will configure the FPGA from the image stored in the Platform Flash PROM.

In Master Serial mode, the FPGA automatically loads the configuration bit stream in bit-serial form from configuration flash synchronized by the configuration clock (CCLK) generatedby the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master Serial configuration mode. Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN). The serial Bit stream data must be set up at the FPGA’s DIN input pin a short time before each rising edge of the FPGA's internally generated CCLK signal.

The jumper setting for selection of Master Serial Mode is discussed in configuration jumper setting section.

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### *Configuration Jumper Settings*

- **Mode Selection Jumpers:** M0, M1, M2 are the mode selection jumpers used to select the configuration mode either Boundary Scan or Master Serial Mode.

| Configuration Mode | 1 | 2 | |
|---|---|---|---|
| MODE0 (M0) | ● | ● | • Connecting 1-2 selects Logic –0,<br>• Disconnecting 1-2 selects Logic- 1 |
| MODE1 (M1) | ● | ● | |
| MODE2 (M2) | ● | ● | |

Table 17.1: Mode Selection Jumper Settings

| Configuration Mode | MODE0 | MODE1 | MODE2 |
|---|---|---|---|
| Boundary Scan Mode | 1 | 0 | 1 |
| Master Serial Mode | 0 | 0 | 0 |

Table 17.2: Mode Selection Table

### *JTAG Header:*

An on board JTAG connector (6 pin male - **JTAG**) is provided for configuring the FPGA through parallel port of PC via a parallel III cable. The details of this connector are as shown in figure 17.1.

| Pin number (JTAG) | FPGA Pin/ Location |
|---|---|
| 1 | +3.3V |
| 2 | GND |
| 3 | TCK |
| 4 | TDO |
| 5 | TDI |
| 6 | TMS |

Figure 17.2: JTAG Connector Details

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## Appendix A: Consolidated Pin Assignment (UCF Location)

### Pin Assignment (UCF Location) for LCD:

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| LCD_RS | P48 | P74 |
| LCD_EN | P49 | P72 |
| LCD_Data0 | P47 | NC |
| LCD_Data1 | P41 | NC |
| LCD_Data2 | P39 | NC |
| LCD_Data3 | P35 | NC |
| LCD_Data4 | P33 | P66 |
| LCD_Data5 | P31 | P61 |
| LCD_Data6 | P29 | P59 |
| LCD_Data7 | P24 | P58 |

### Pin Assignment (UCF Location) for 7-Segment Display:

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| Sel_DIS1 | P23 | P57 |
| Sel_DIS2 | P18 | P50 |
| Sel_DIS3 | P15 | P47 |
| Sel_DIS4 | P4 | P35 |
| Sel_DIS5 | P9 | P45 |
| Sel_DIS6 | P12 | P43 |
| Segment_a | P8 | P56 |
| Segment_b | P16 | P51 |
| Segment_c | P3 | P44 |
| Segment_d | P2 | P33 |
| Segment_e | P11 | P34 |
| Segment_f | P19 | P48 |
| Segment_g | P22 | P41 |
| Segment_dp | P5 | P40 |

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**Pin Assignment (UCF Location) for IOs:**

| DIP Switch | Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 | DIP Switch | Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|---|---|---|---|---|
| SW1 | TL1 | P205 | P29 | SW3 | TL17 | P179 | NC |
| | TL2 | P206 | P30 | | TL18 | P180 | NC |
| | TL3 | P203 | P26 | | TL19 | P177 | NC |
| | TL4 | P200 | P23 | | TL20 | P178 | NC |
| | TL5 | P202 | P24 | | TL21 | P152 | NC |
| | TL6 | P197 | P21 | | TL22 | P168 | NC |
| | TL7 | P199 | P22 | | TL23 | P171 | NC |
| | TL8 | P196 | P17 | | TL24 | P172 | NC |
| SW2 | TL9 | P192 | P11 | SW4 | TL25 | P165 | NC |
| | TL10 | P193 | P12 | | TL26 | P167 | NC |
| | TL11 | P189 | P9 | | TL27 | P163 | NC |
| | TL12 | P190 | P10 | | TL28 | P164 | NC |
| | TL13 | P186 | P144 | | TL29 | P161 | NC |
| | TL14 | P187 | P2 | | TL30 | P162 | NC |
| | TL15 | P185 | P5 | | TL31 | P160 | NC |
| | TL16 | P181 | P6 | | TL32 | P153 | NC |

**Pin Assignment (UCF Location) for Pushbuttons:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| K0 | P204 | P27 |
| K1 | P194 | P16 |
| K2 | P184 | P15 |
| K3 | P183 | P14 |
| K4 | P174 | P7 |
| K5 | P175 | P8 |
| K6 | P169 | NC |
| K7 | P159 | NC |

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**Pin assignment (UCF Location) for ADC 0808:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| ADC_DATA 0 | P71 | P87 |
| ADC_DATA 1 | P72 | P88 |
| ADC_DATA 2 | P54 | P79 |
| ADC_DATA 3 | P51 | P78 |
| ADC_DATA 4 | P89 | P95 |
| ADC_DATA 5 | P91 | P97 |
| ADC_DATA 6 | P57 | P80 |
| ADC_DATA 7 | P58 | P81 |
| ADC_EOC | P101 | P98 |
| ADC_ADD 0 | P69 | P85 |
| ADC_ADD 1 | P68 | P84 |
| ADC_ADD 2 | P74 | P92 |
| ADC_SOC | P64 | P82 |
| ADC_ALE | P65 | P83 |
| ADC_CLK | P82 | P94 |
| ADC_OE | P76 | P93 |

**Pin Assignment (UCF Location) DAC TLC7528:**

| Signal Name | XC3S250E-PQ208 | XCS6LX9-TQG144 |
|---|---|---|
| DAC_DATA 0 | P116 | P114 |
| DAC_DATA 1 | P119 | P116 |
| DAC_DATA 2 | P120 | P115 |
| DAC_DATA 3 | P122 | P117 |
| DAC_DATA 4 | P115 | P111 |
| DAC_DATA 5 | P113 | P112 |
| DAC_DATA 6 | P112 | P105 |
| DAC_DATA 7 | P108 | P104 |
| DAC_WR | P109 | P102 |
| DAC_A_B | P107 | P101 |

**Pin Assignment (UCF Location) for PS/2 Connector**

| Signal Name | FPGA Pin |
|---|---|
| PS2_CLK | P25 |
| PS2_DATA | P26 |

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**Pin Assignment (UCF location) for VGA Display Port:**

| Pin Description | Location |
|---|---|
| VGA_RED | P40 |
| VGA_GREEN | P34 |
| VGA_BLUE | P36 |
| VGA_HS | P45 |
| VGA_VS | P42 |

**Pin Assignment (UCF Location) for RS232 Serial Ports:**

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| TxD_F | P30 | P67 |
| RxD_F | P43 | P62 |

Pin Assignment (UCF) for Female DB9 DCE Connector

| Pin Description | Location |
|---|---|
| TxD_M | P28 |
| RxD_M | P32 |

Pin Assignment (UCF) for Male DB9 DTE Connector

**Pin Assignment (UCF Location) for USB interface:**

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| USB_Rx | P106 | P99 |
| USB_TX | P100 | P100 |

**Pin Assignment (UCF Location) for Clock Sources:**

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| RESET | -- | P32 |
| Clock_12MHz | P80 | P55 |
| Clock_7.5MHz | P78 | NC |
| Clock_15MHz | P77 | NC |
| Clock_30MHz | P83 | NC |
| Clock_32kHz | P75 | NC |
| Clock_555 | P132 | P120 |

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**Pin Assignment (UCF Location) for RTC:**

| Signal Name | FPGA Pin |
|---|---|
| RTC_SDA | P61 |
| RTC_SCL | P62 |

**Pin Assignment (UCF Location) for Buzzer:**

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| Buzzer | P146 | P139 |

**Pin Assignment (UCF Location) for RGB LED:**

| Signal Name | XC3S250E-PQ208 | XC6SLX9-TQG144 |
|---|---|---|
| LED_Red | P151 | P140 |
| LED_Green | P150 | P142 |
| LED_Blue | P147 | P143 |

**Pin Assignment (UCF Location) for Expansion Connectors:**

| Pin number (FRC J10) | FPGA Pin/ Location | Direction/ Purpose |
|---|---|---|
| 1 | 102 | inout |
| 2 | 98 | Inout |
| 3 | 99 | Inout |
| 4 | 96 | Inout |
| 5 | 97 | Inout |
| 6 | 93 | Inout |
| 7 | 94 | Inout |
| 8 | 90 | Inout |
| 9 | +3.3v | Supply |
| 10 | Gnd | Gnd |

Pin Assignment (UCF) for FRC Connector **J10**

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| Pin number (FRC J12) | FPGA Pin/ Location | Direction/ Purpose |
|---|---|---|
| 1 | 118 | input |
| 2 | 110 | input |
| 3 | 123 | Inout |
| 4 | NC | NC |
| 5 | 124 | Input |
| 6 | 126 | Inout |
| 7 | 127 | Inout |
| 8 | 128 | Inout |
| 9 | +3.3v | Supply |
| 10 | Gnd | Gnd |

Pin Assignment (UCF) for FRC Connector **J12**

| Pin number (FRC J14) | XC3S250E-PQ208 | Direction/ Purpose | XC6SLX9-TQG144 | Direction/ Purpose |
|---|---|---|---|---|
| 1 | 138 | Inout | P119 | I/O |
| 2 | 142 | input | P118 | I/O |
| 3 | 140 | Inout | P123 | I/O |
| 4 | 145 | Inout | P121 | I/O |
| 5 | 144 | Input | P126 | I/O |
| 6 | 148 | input | P124 | I/O |
| 7 | 154 | input | P132 | I/O |
| 8 | 14 | input | P127 | I/O |
| 9 | +3.3v | Supply | +3.3v | Supply |
| 10 | Gnd | Gnd | Gnd | Gnd |

Pin Assignment (UCF) for FRC Connector **J14**

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| Pin number (FRC J15) | XC3S250E-PQ208 | Direction/ Purpose | XC6SLX9-TQG144 | Direction/ Purpose |
|---|---|---|---|---|
| 1 | 130 | input | P131 | I/O |
| 2 | 129 | Inout | P134 | I/O |
| 3 | 134 | Inout | P133 | I/O |
| 4 | 133 | Inout | P138 | I/O |
| 5 | 136 | Input | P137 | I/O |
| 6 | 135 | Inout | P141 | I/O |
| 7 | 139 | Inout | P1 | I/O |
| 8 | 137 | Inout | P46 | I/O |
| 9 | +3.3v | Supply | +3.3v | Supply |
| 10 | Gnd | Gnd | Gnd | Gnd |

Pin Assignment (UCF) for FRC Connector **J15**