

eg. ① Implement 2:1 mux using T.G



Truth table

sel	Y	I <sub>0</sub>	I <sub>1</sub>
0	I <sub>0</sub>	I <sub>0</sub>	0
1	I <sub>1</sub>	0	I <sub>1</sub>

$$\therefore Y = \overline{\text{sel}} \cdot I_0 + \text{sel} \cdot I_1$$

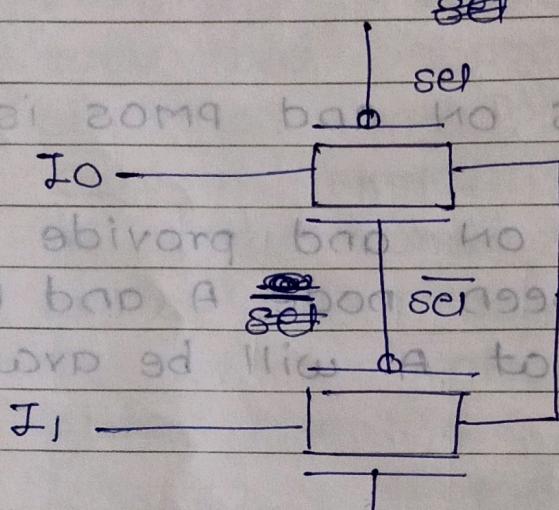


Fig. 2x1 mux using T.G

② Design 4x1 mux using T.G.

⇒ Truth table

For 4x1 mux, we need 2 select lines.

0 0	I <sub>0</sub>
0 1	I <sub>1</sub>
1 0	I <sub>2</sub>
1 1	I <sub>3</sub>

$$Y = \bar{s}_0 s_1 I_0 + \bar{s}_1 s_0 I_1 + s_1 \bar{s}_0 I_2 + s_1 s_0 I_3$$

$$Y = (\bar{s}_0 \cdot I_0 + s_0 I_1) \bar{s}_1 + (\bar{s}_0 I_2 + s_0 I_3) s_1$$

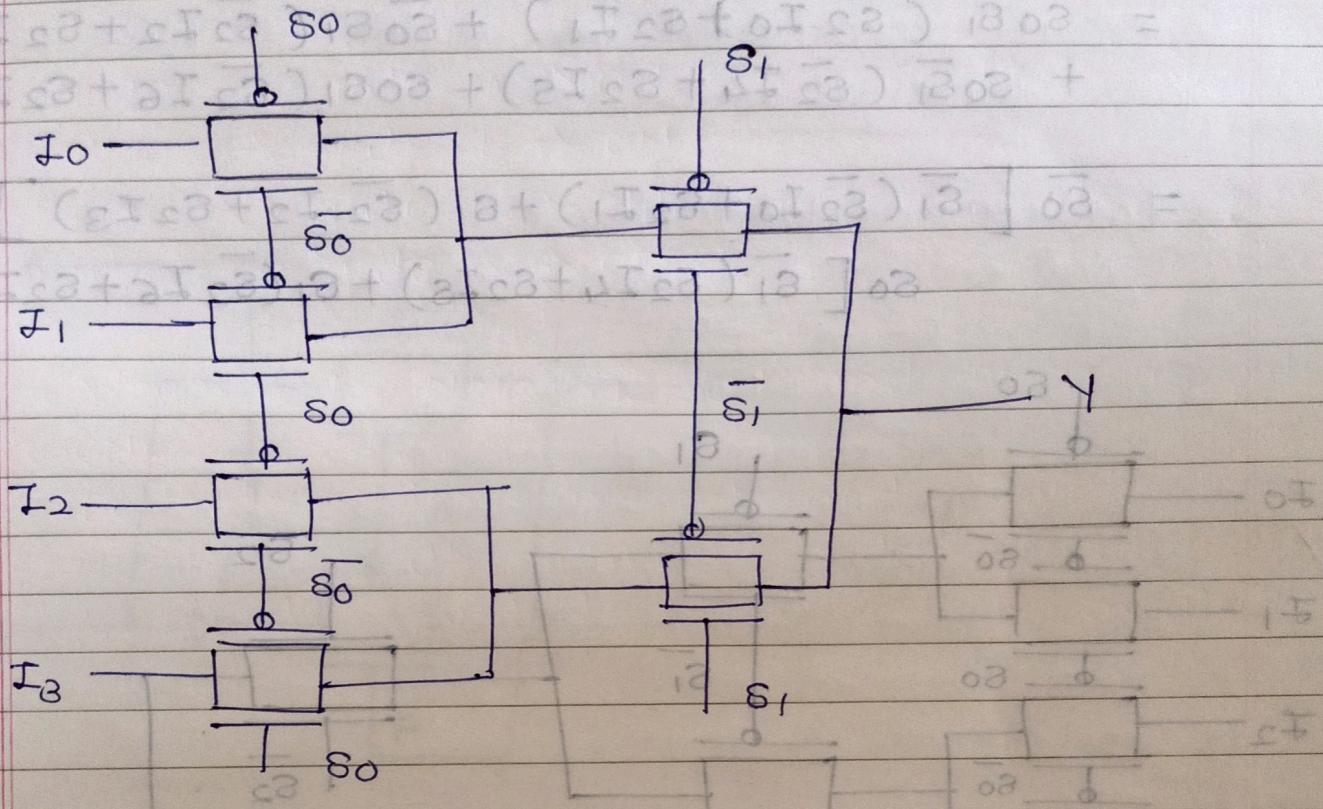


Fig. 4:1 mux using T.G.

③ Design 8:1 Mux using T-G

$\Rightarrow$  Truth table :- select lines =  $n=3$

$$2^n = 8 \quad 2^3 = 8$$

$s_0$	$s_1$	$s_2$	$Y$
0	0	0	$I_0$
0	0	1	$I_1$
0	1	0	$I_2$
0	1	1	$I_3$
1	0	0	$I_4$
1	0	1	$I_5$
1	1	0	$I_6$
1	1	1	$I_7$

$$\gamma = \bar{s}_0 \cdot \bar{s}_1 \cdot \bar{s}_2 \cdot I_0 + \bar{s}_0 \cdot s_1 \cdot s_2 \cdot I_1 + s_0 \cdot s_1 \cdot \bar{s}_2 \cdot I_2 \\ + \bar{s}_0 \cdot s_1 \cdot s_2 \cdot I_3 + s_0 \cdot \bar{s}_1 \cdot \bar{s}_2 \cdot I_4 + s_0 \cdot \bar{s}_1 \cdot s_2 \cdot I_5 \\ + s_0 \cdot s_1 \cdot \bar{s}_2 \cdot I_6 + s_0 \cdot s_1 \cdot s_2 \cdot I_7$$

$$= \bar{s}_0 \bar{s}_1 (\bar{s}_2 I_0 + s_2 I_1) + \bar{s}_0 s_1 (\bar{s}_2 I_2 + s_2 I_3) \\ + s_0 \bar{s}_1 (\bar{s}_2 I_4 + s_2 I_5) + s_0 s_1 (\bar{s}_2 I_6 + s_2 I_7)$$

$$= \bar{s}_0 [ \bar{s}_1 (\bar{s}_2 I_0 + s_2 I_1) + s_1 (\bar{s}_2 I_2 + s_2 I_3) ] + \\ s_0 [ \bar{s}_1 (\bar{s}_2 I_4 + s_2 I_5) + s_1 (\bar{s}_2 I_6 + s_2 I_7) ]$$

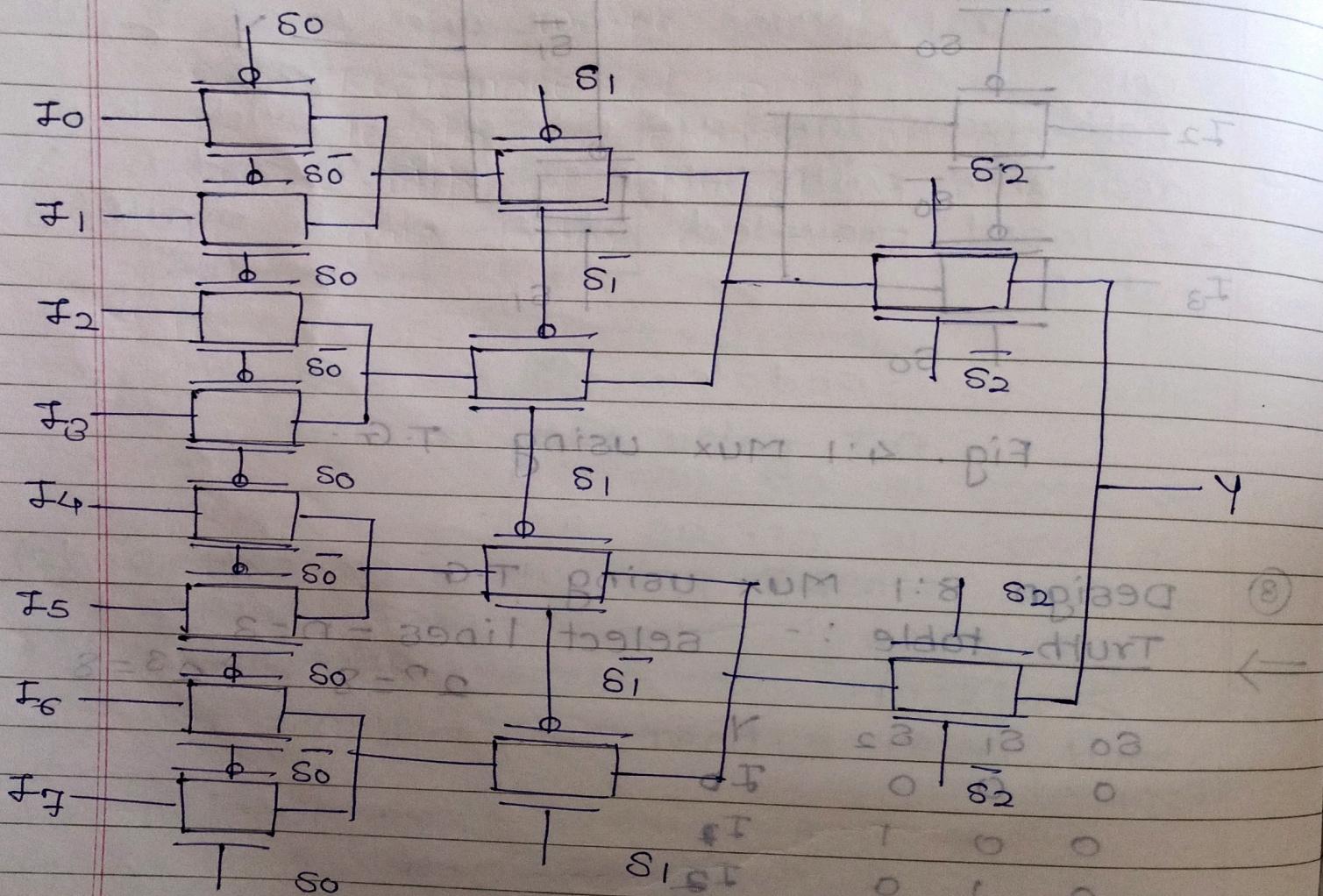


Fig. 8x1 MUX using T.G

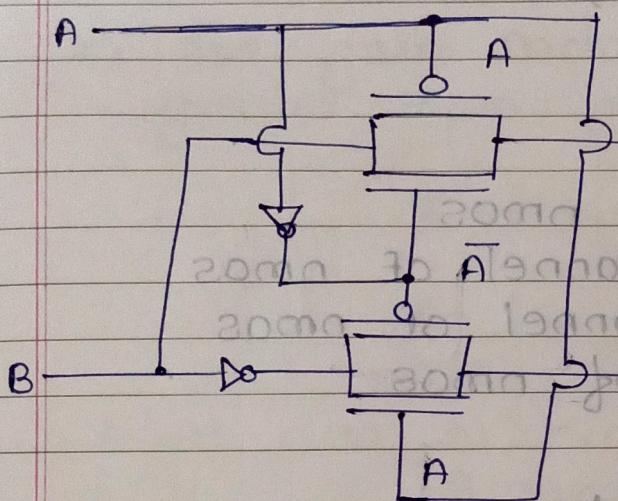
④ Design XOR gate using TG.

⇒ Truth table.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$Y = \bar{A}B + \bar{A} \cdot B$$

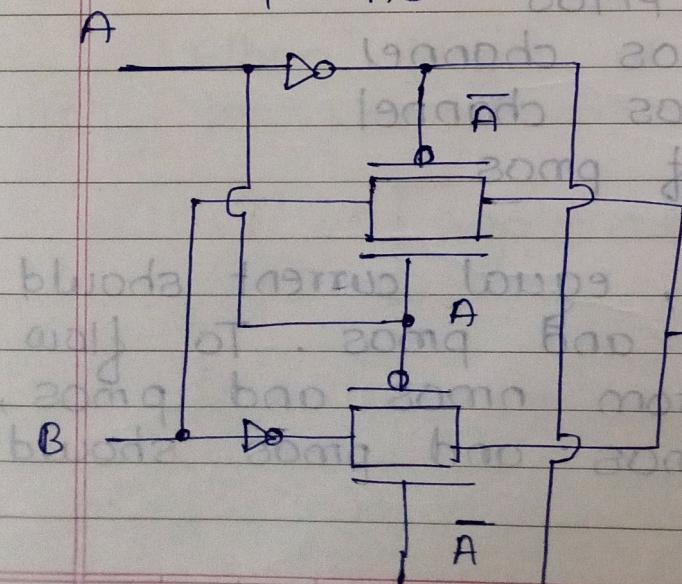
$$Y = \bar{A}B + A \cdot \bar{B}$$



⑤ Design XNOR gate using TG.

⇒

$$Y = AB + \bar{A} \cdot \bar{B}$$



\* Show that  $(W/L)_P \approx 2.5 \left(\frac{W}{L}\right)_N$

⇒ The resistance of CMOS gate is directly proportional to length of channel and inversely proportional to width of channel & gain factor.

⇒ For NMOS transistor,

$$R_N \propto \frac{L_N}{W_N \cdot B_N}$$

$R_N$  = Resistance of NMOS

$L_N$  = length of channel of NMOS

$W_N$  = width of channel of NMOS

$B_N$  = gain factor of NMOS

⇒ For PMOS transistor,

$$R_P \propto \frac{L_P}{W_P \cdot B_P}$$

where,

$R_P$  = Resistance of PMOS

$L_P$  = length of PMOS channel

$W_P$  = width of PMOS channel

$B_P$  = gain factor of PMOS

⇒ For CMOS inverter, equal current should flow from NMOS and PMOS. To flow equal current from NMOS and PMOS, resistance of NMOS and PMOS should be equal.

ie.

$$R_D = R_P$$

$$\frac{L_D}{W_D} = \frac{B_D}{B_P} \cdot \frac{L_P}{W_P}$$

$$\frac{L_D}{W_D} = \frac{B_D}{B_P} \cdot \frac{L_P}{W_P}$$

$\Rightarrow$  But gain factor of nmos is 2.5 times greater than gain factor of pmos.

$$B_D \approx 2.5 B_P$$

$$\frac{L_D}{W_D} = \frac{2.5 B_P}{B_P} \cdot \frac{L_P}{W_P}$$

$$\frac{L_D}{W_D} = 2.5 \frac{L_P}{W_P}$$

$$\boxed{\frac{W_P}{L_P} = 2.5 \frac{W_D}{L_D}}$$

When length of nmos and pmos is same  
ie.  $L_P = L_D$

$$\boxed{W_P \approx 2.5 W_D}$$

Hence proved.

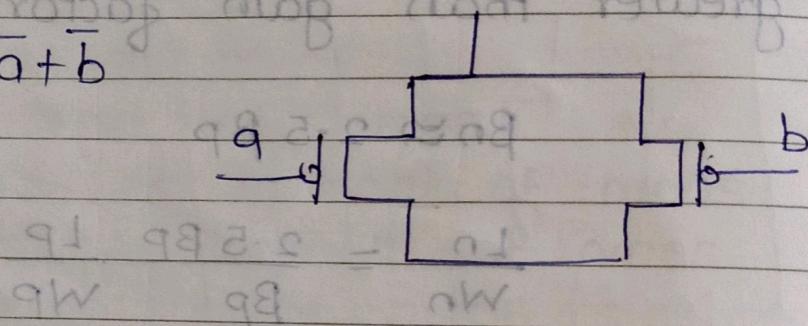
## \* Design of CMOS logic

⇒ For any expression to be designed using CMOS logic, it should be complement form.

$$\text{ie. } y = \overline{\bar{a} + b \cdot c + d}$$

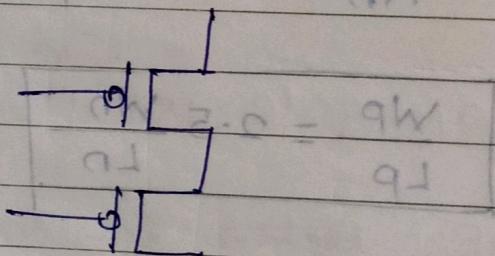
⇒ When variables are in OR ie. +, connect the gates in parallel.

$$\text{ie. } y = \overline{\bar{a}} + \overline{b}$$



⇒ When the variables are in AND ie. \*, connect the gates in series.

$$\text{ie. } y = \bar{a} \cdot \bar{b}$$



⇒ NMOS logic is complement of PMOS logic.

⇒ Always connect PMOS logic to pull up side that is Vdd.

⇒ Always connect NMOS to pull down side  
ie. Ground

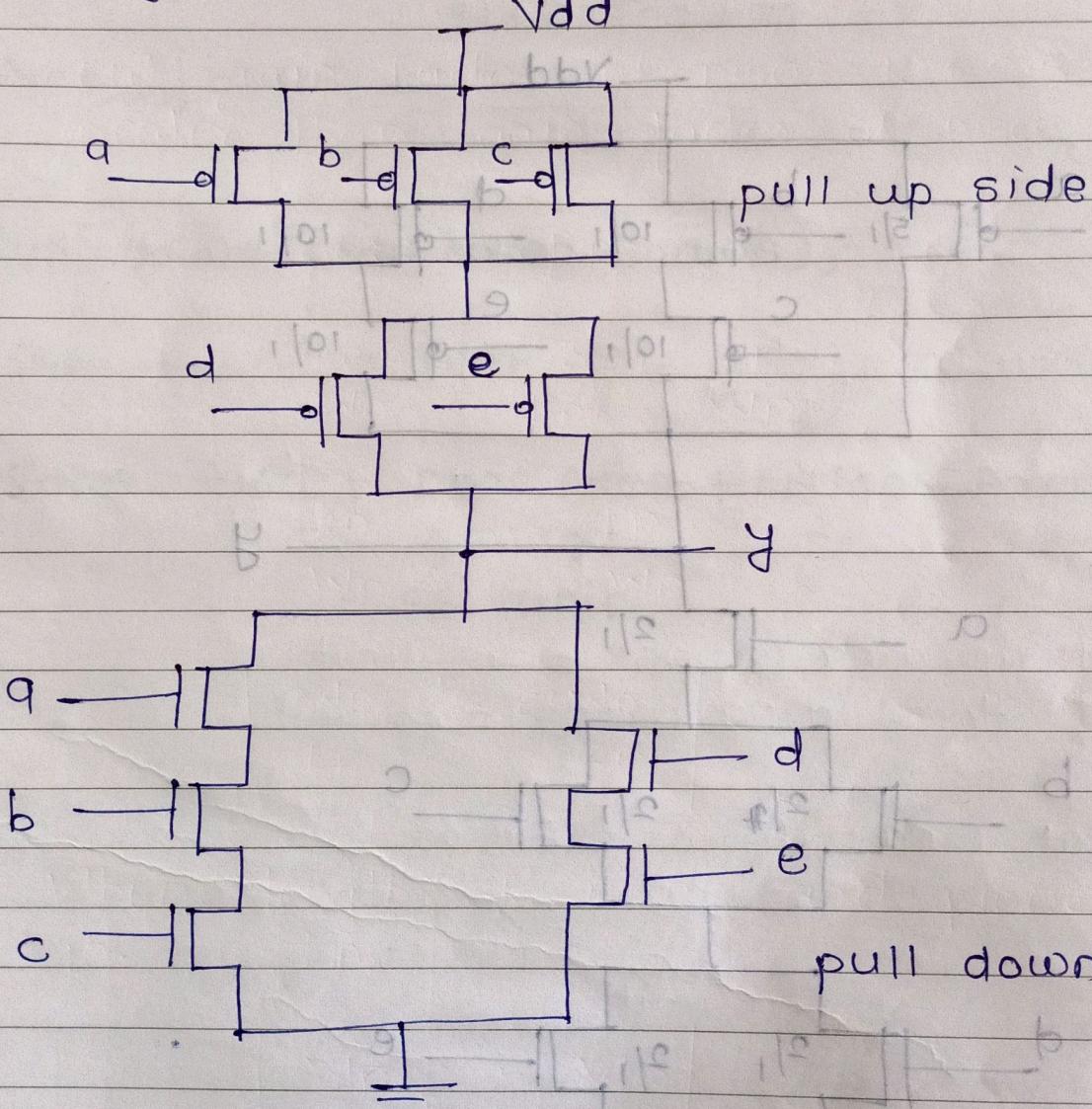
⇒ Make expression in complement form by using inverters at output if not given.

① Implement  $y = \overline{abc + de}$  using CMOS.

$\Rightarrow$  By DeMorgan's theorem,

$$y = \overline{\overline{abc} \cdot \overline{de}}$$

$$y = (\overline{a} + \overline{b} + \overline{c}) \cdot (\overline{d} + \overline{e})$$



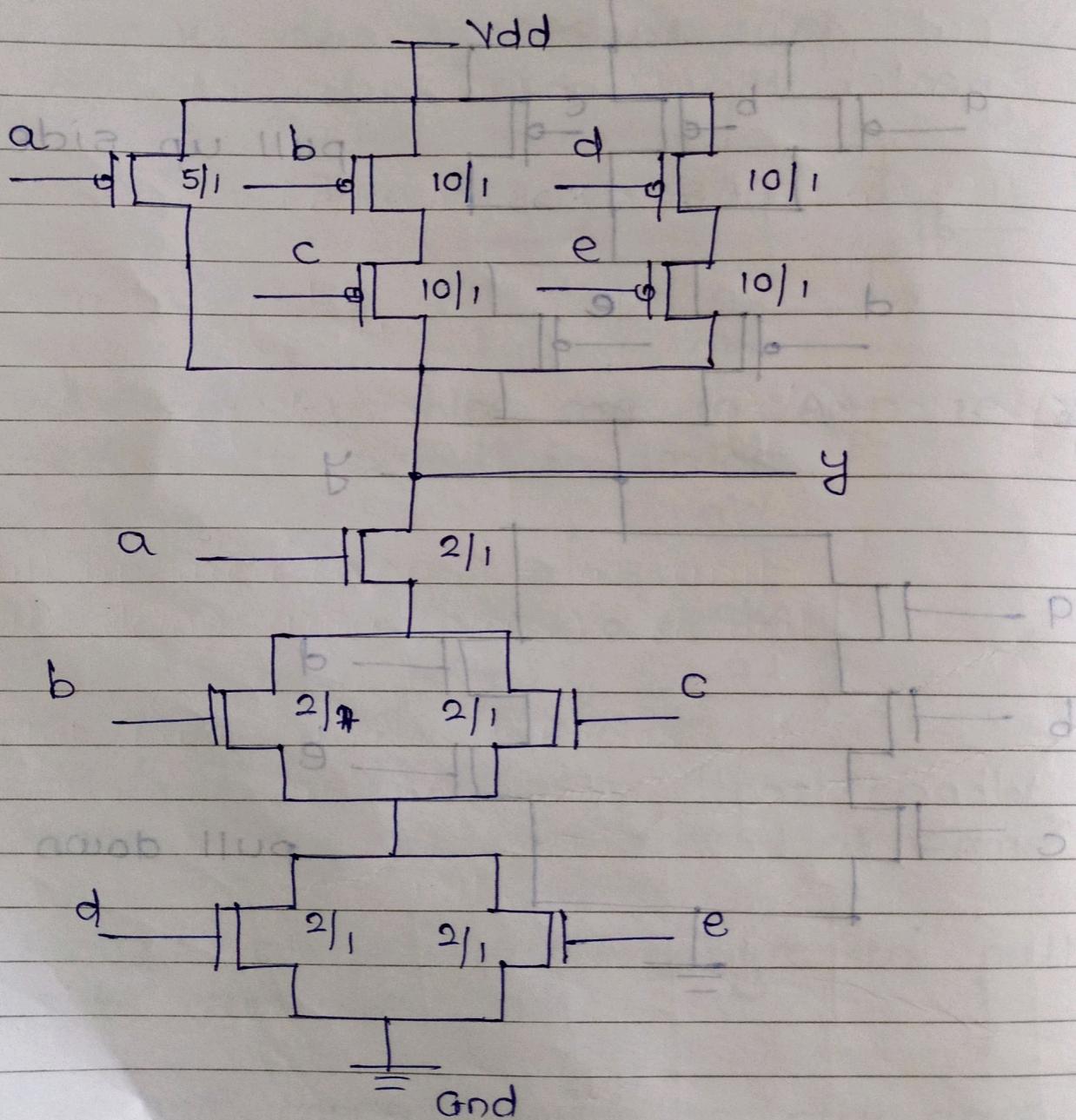
\*

Design the circuit using CMOS logic and calculate area.

$$y = \overline{a(b+c)(d+e)}$$

$\Rightarrow$

$$\begin{aligned} y &= \overline{a(b+c)(d+e)} \\ &= \overline{a} + \overline{(b+c)} + \overline{(d+e)} \\ &= \overline{a} + \overline{b} \cdot \overline{c} + \overline{d} \cdot \overline{e} \end{aligned}$$



consider,  $(\frac{W}{L})_N = \frac{Q}{I}$

$$\text{but } \left(\frac{W}{L}\right)_P = 2.5 \left(\frac{W}{L}\right)_N$$

$$\therefore \left(\frac{W}{L}\right)_P = \frac{5}{1}$$

Pull up side area (pmos),

$$\text{Area}_{\text{pmos}} = \text{sum of all } \left(\frac{W}{L}\right)_P$$

$$\text{Area}_{\text{pmos}} = 45 \text{ unit}$$

Pull down side area (nmos),

$$\text{Area}_{\text{nmos}} = 10 \text{ unit}$$

Total Area = PMOS Area + NMOS Area

$$= 45 + 10$$

$$= 55 \text{ unit.}$$

\* Design CMOS logic for  $y = AB + CDEFG + H$ .  
also compute area on chip.

=>

$$y = AB + CDEFG + H$$

Invert the  $y$  twice to implement using CMOS.

$$y = \overline{AB + CDEFG + H}$$

$$y = \overline{\overline{AB} \cdot \overline{CDEFG} \cdot \overline{H}}$$

$$y = \overline{(\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G}) \cdot \overline{H}}$$

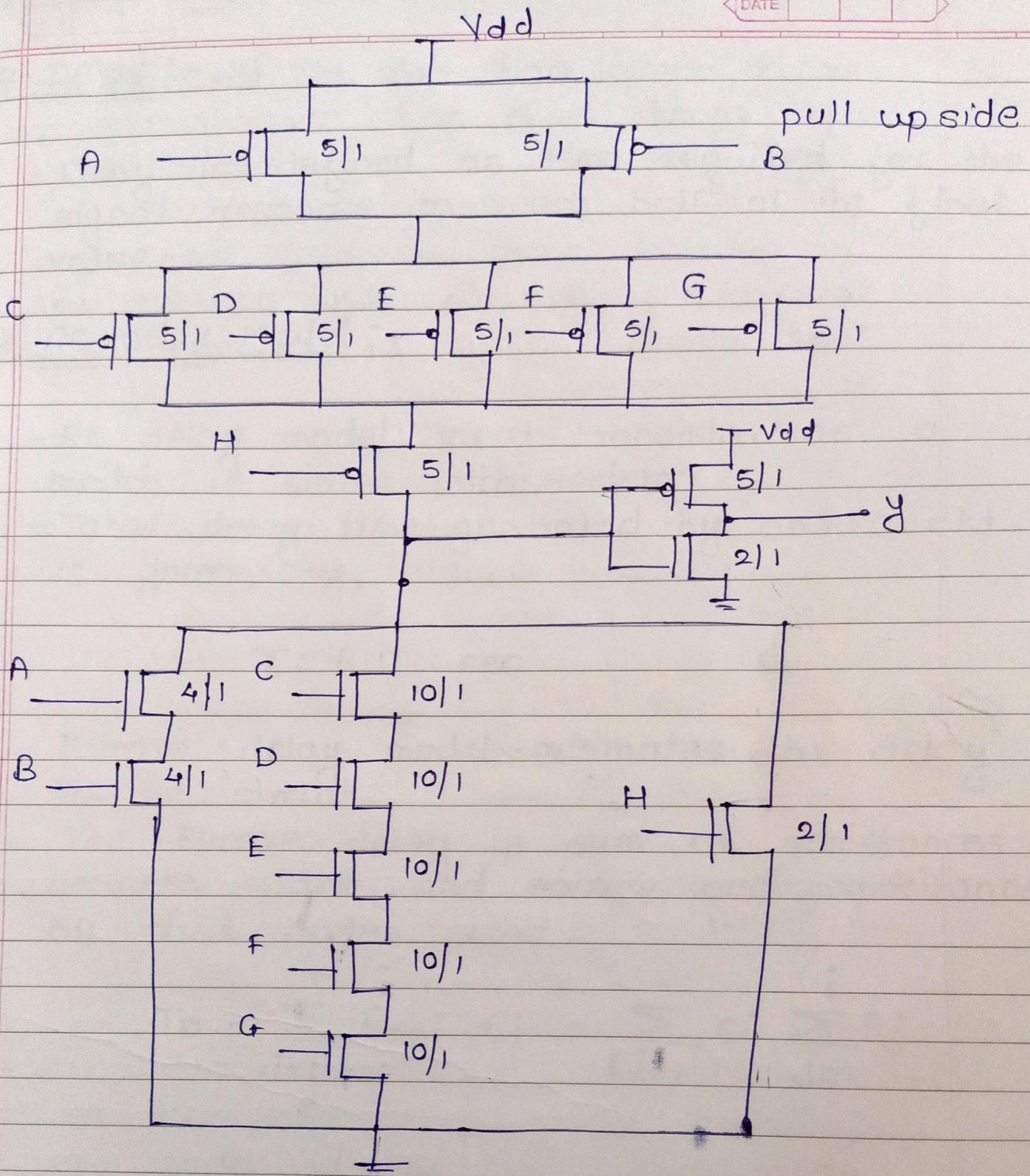
Assume  $\left(\frac{W}{L}\right)_N = \frac{2}{1}$

$$\left(\frac{W}{L}\right)_P = \frac{5}{1} \text{ as } \left(\frac{W}{L}\right)_P = 2.5 \times \left(\frac{W}{L}\right)_N$$

Pull up area (PMOS) = 45 unit  
pull down area (NMOS) = 60 unit

$$\begin{aligned} \text{Total Area} &= A_{PMOS} + A_{NMOS} \\ &= 45 + 60 \end{aligned}$$

$$= 105 \text{ unit.}$$



\* Delay :- adt no ana batudirrait a xal -  
grn 222antingan ban ia ot loupe am

Delay is defined as time required for the signal response to reach half of its final value.

\* RC Delay Model :-

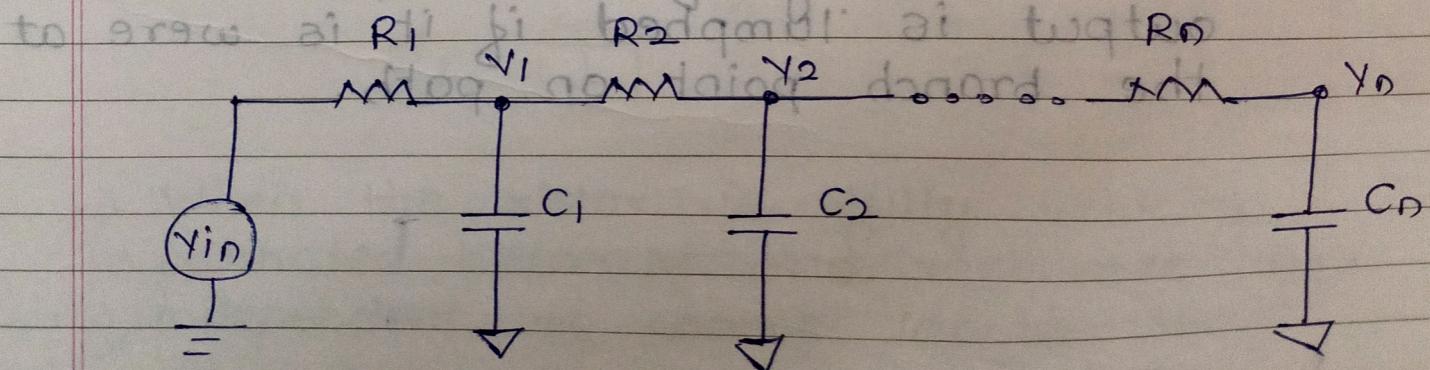
- RC delay model treat transistor as a switch in series with resistor.
- Total delay time generated by an RC ckt is given by,

$$\tau = R \cdot C \text{ sec.}$$

- Elmore delay model estimates the delay in RC circuit.

The Elmore delay is sum of resistances between nodes and source and capacitances on that node.

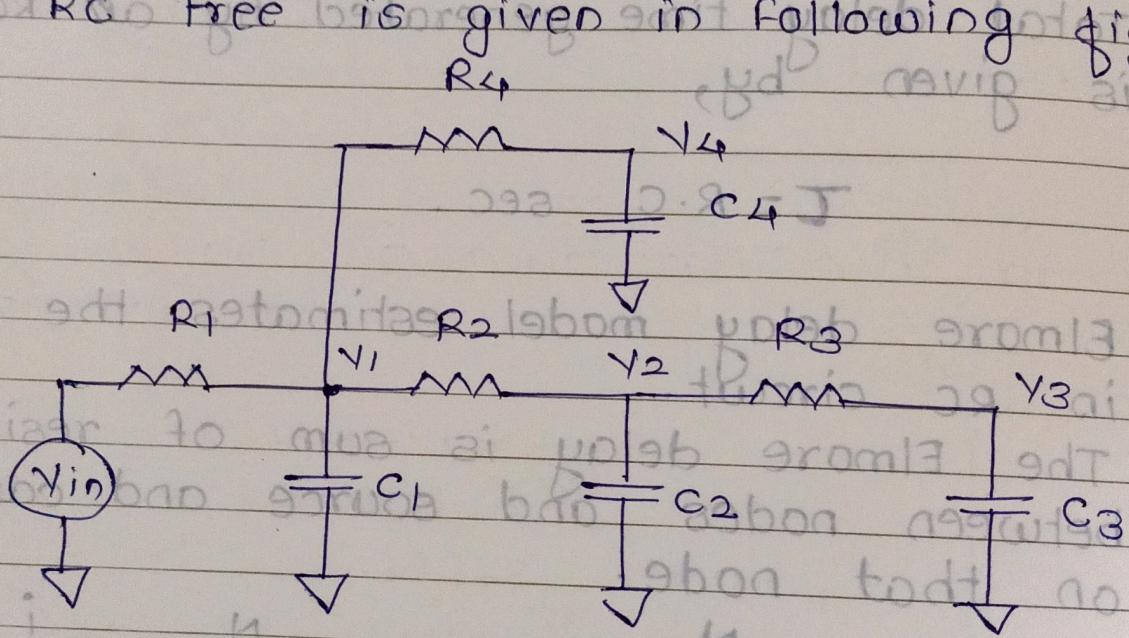
$$T_D = \sum_{i=1}^N R_{0+i} \cdot C_i = \sum_{i=1}^N C_i \sum_{j=1}^i R_j$$



- For a distributed line all the resistances are equal to  $R_1$  and capacitances are equal to  $C_1$ .
- In general wire branching into many destinations are modeled as RC tree. The Elmore delay of RC tree is given as,

$$T_D = \sum_{k=1}^N R_{ki} C_k$$

The RC tree is given in following fig.



- In RC tree, the capacitance on the branches away from the path to the output is lumped if it is at the branch point on path.

### \* Effective Resistance :-

→ RC model treats transistor as a switch in series with resistor.

The effective resistance is ratio of  $V_{ds}$  and  $I_{ds}$  averaged across the switching interval.

$$R_{eff} = \frac{V_{ds}}{I_{ds}}$$

→ A unit NMOS transistor has effective resistance of  $R$ .

→ A NMOS transistor of  $k$  times unit width has resistance of  $R/k$  because it delivers  $k$  times as much current.

→ A unit PMOS has greater resistance in the range of  $2R - 3R$  because of its lower mobility.

→ According to long channel model, current decreases linearly with channel length and hence resistance is proportional to  $L$ .

$$R \propto L$$

→ When theistor is fully velocity saturated, current and resistance are independent of channel length.

→ Real transistors operate between these two extremes.  
Due to this resistance of transistor in series is lower than sum of resistances, because series x'stors has smaller Vds and are less velocity saturated.

### \* Linear Delay Model :-

- The RC delay model showed that delay is linear function of fanout of gate.  
→ In generalised normalised delay of gate is can be expressed as,

$$d = f + p \quad \text{where}$$

$d$  = normalized delay  
 $f$  = Effort delay  
 $p$  = parasitic delay

→ The effort delay depends upon complexity and fanout of gate.

$$f = g \cdot h$$

→ Complexity is represented by logical efforts g. Inverter has logical efforts equal to 1.

⇒  $b$  is fanout or electrical efforts of gate.  
 If the load does not contain identical copies of gate, the electrical efforts can be calculated as,

$$b = \frac{C_{out}}{C_{in}}$$

where,

$C_{out}$  = capacitance of external load

$C_{in}$  = input capacitance of gate

#### \* Logical Efforts :-

⇒ Logical efforts of the gate is defined as ratio of input capacitance of gate to the input capacitance of an inverter that can deliver same output current.

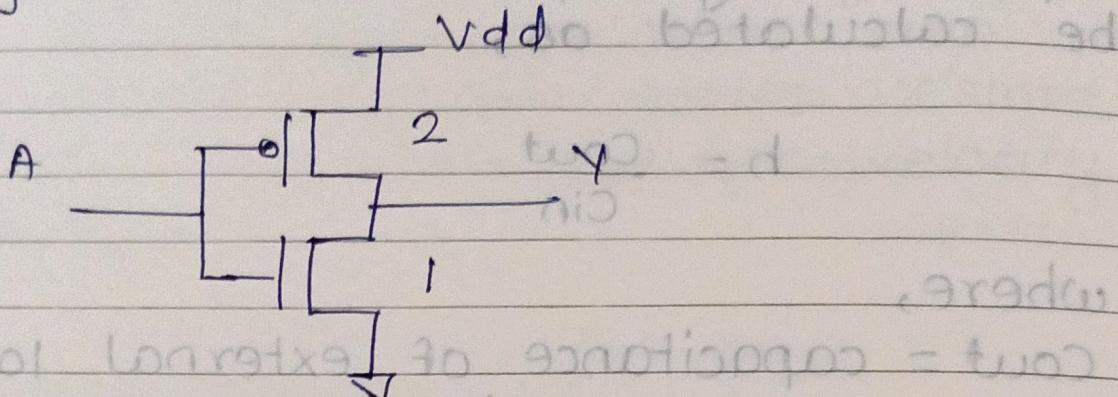
⇒ Logical efforts indicates how much worse a gate is producing output current as compared to an inverter.

⇒ Logical efforts can be measured in simulation from delay vs fanout plots as the ratio of the slope of delay of gate to delay of an inverter.

⇒  $g = \text{logic efforts} = \frac{\text{gate i/p capacitance}}{\text{inverter i/p capacitance}}$

→ PMOS has twice resistance than NMOS.

### ① Logical Efforts of inverter :-



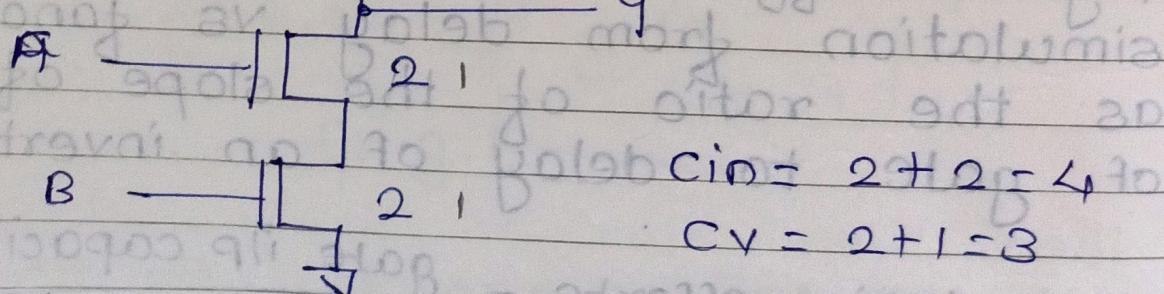
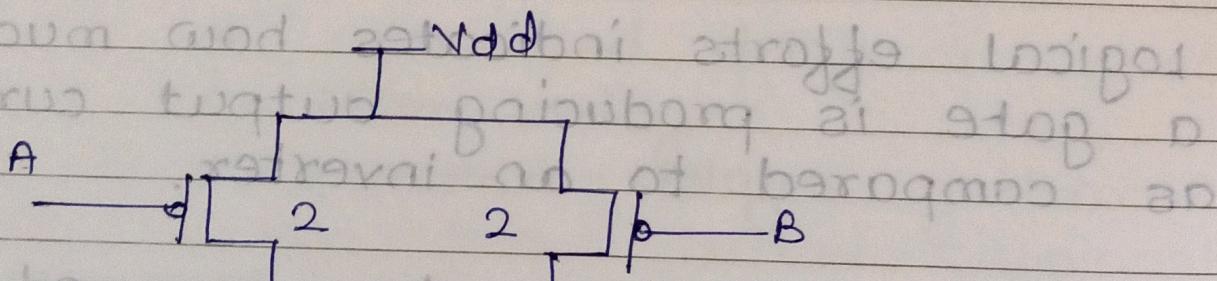
$$\text{input capacitance} = C_{in} = 2 + 1 = 3$$

$$\text{inverter i/p capacitance} = C_V = 2 + 1 = 3$$

$$\text{logical efforts, } g = \frac{C_{in}}{C_V} = \frac{3}{3} = 1$$

### ② Logical Efforts for 2 input NAND gate

$$y = \overline{a \cdot b} = \overline{a} + \overline{b}$$



$$C_{in} = 2 + 2 - 1 = 3$$

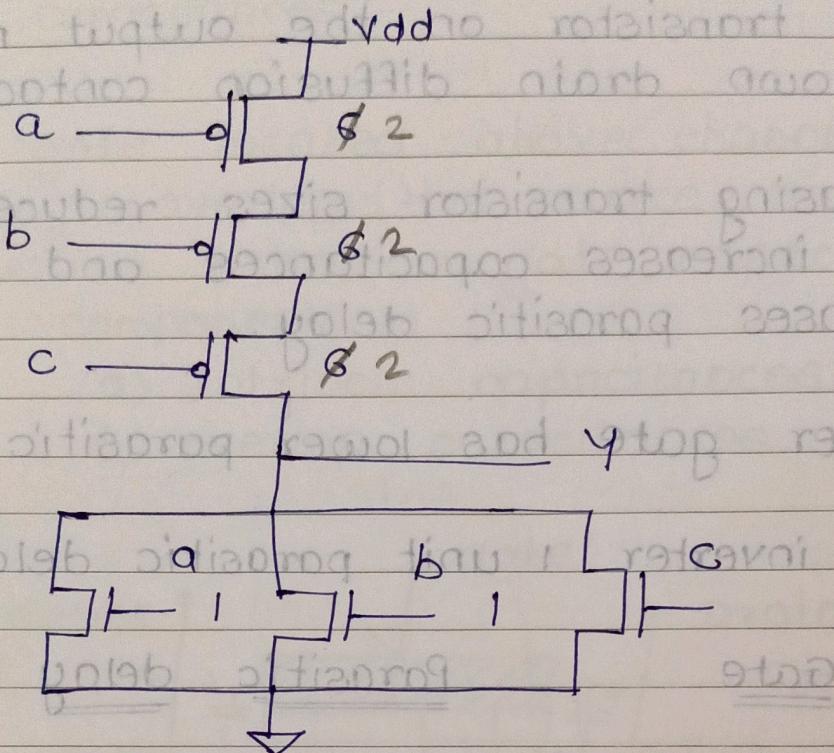
$$C_V = 2 + 1 = 3$$

$$g = 1/3$$

logical Efforts for

③ Three input NOR gate

$$y = \overline{a+b+c} = \overline{a} \cdot \overline{b} \cdot \overline{c}$$



$$C_{in} = 6 + 1 = 7$$

$$C_V = 2 + 1 = 3$$

$$g = \frac{C_{in}}{C_V} = \frac{7}{3}$$

### \* Parasitic Delay :-

⇒ Parasitic delay of gate is the delay of gate when it drives zero load.

⇒ It can be estimated with RC delay model. for manual calculation of the parasitic delay count only the

diffusion capacitance on output node.

- ⇒ Each transistor on the output node has its own drain diffusion contact.
- ⇒ Increasing transistor sizes reduces resistances but increases capacitances and hence increases parasitic delay.
- ⇒ Larger gate has lower parasitic delay.
- ⇒ For inverter 1 unit parasitic delay occurs.

Gate

inverter

n input NAND

n input NOR

n way mux

Parasitic delay

$$P_{inv} = 1$$

$$n \cdot P_{inv}$$

$$n \cdot P_{inv}$$

$$2n \cdot P_{inv}$$

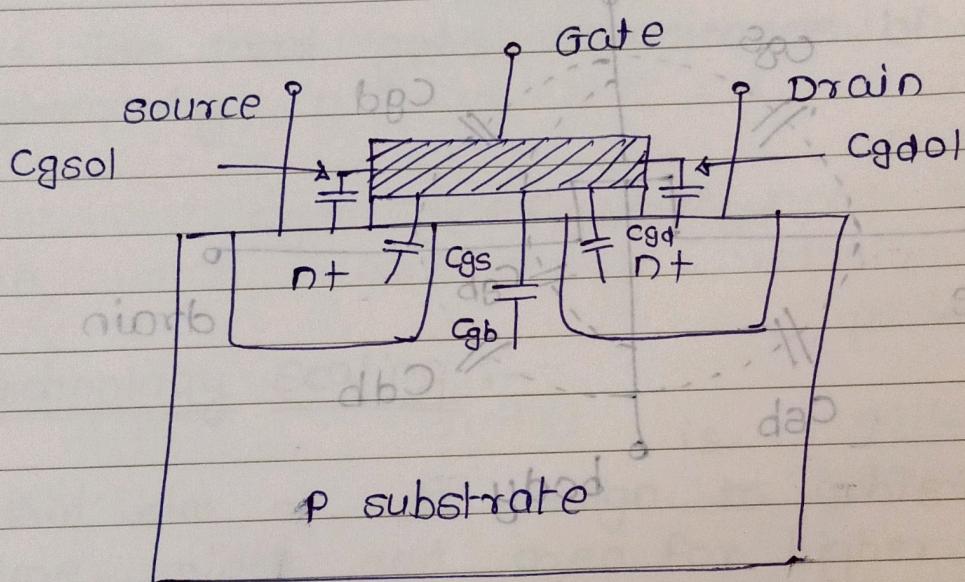
$$C_A = \frac{C_D}{2}$$

\* Gate and diffusion capacitances :-

⇒ A) Gate capacitances :-

→ MOS gate located above channel and partially overlap the source and drain diffusion areas. ∴ gate capacitances has two components -  
 a) Intrinsic capacitances  
 b) overlap capacitances

⇒



$C_{gs0}$  ⇒ overlap capacitance bet<sup>n</sup> gate to source

$C_{gd0}$  ⇒ overlap capacitance bet<sup>n</sup> drain to gate

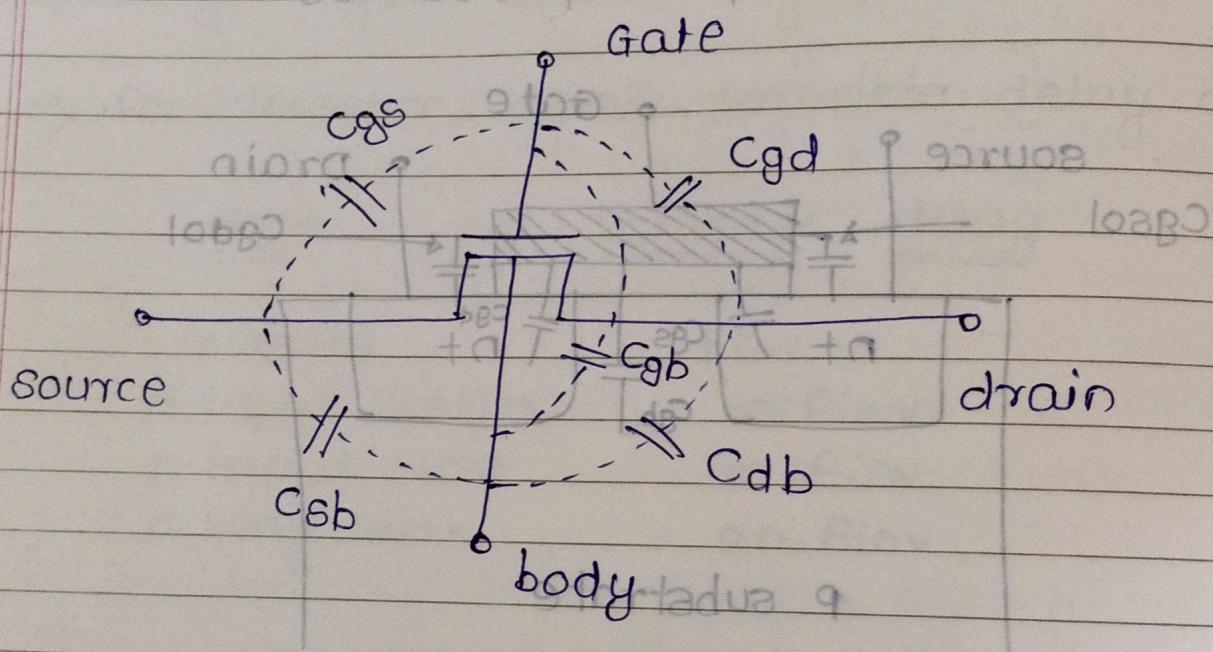
⇒ overlap capacitances are proportional to width of transistors.

⇒ Intrinsic capacitances are formed bet<sup>n</sup>

gate and source, gate and drain  
of gate and body. It has three  
components -

- ①  $C_{GS}$   $\Rightarrow$  gate to source capacitance
- ②  $C_{GD}$   $\Rightarrow$  gate to drain capacitance
- ③  $C_{GB}$   $\Rightarrow$  gate to body capacitance.

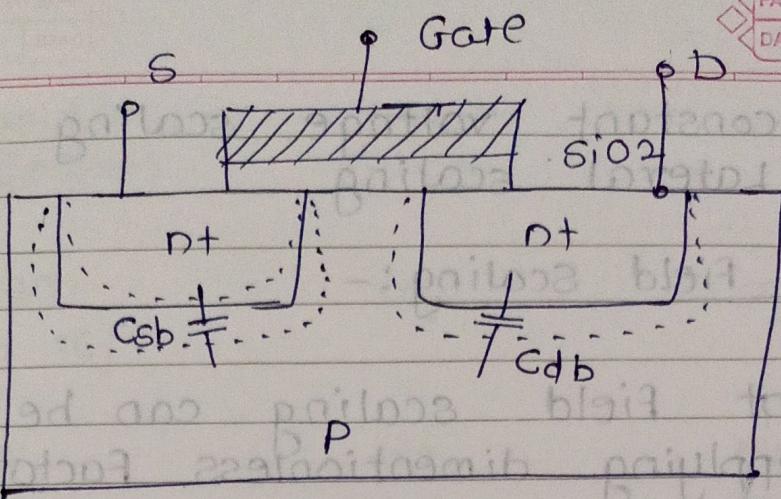
$\Rightarrow$  capacitances of MOS are shown in  
following dia.



### B] Diffusion Capacitances:-

$\Rightarrow$  PN junction bet<sup>n</sup> source diffusion and  
body contribute parasitic capacitances  
across depletion region.

$\Rightarrow$  Two semiconductor materials acts as  
metal part and depletion layer  
act as dielectric bet<sup>n</sup> them.



$C_{sb} \Rightarrow$  source to body diffusion capacitance

$C_{db} \Rightarrow$  drain to body diffusion capacitance

The total gate capacitance of MOS is given by,

$$C_g = C_{gs} + C_{gb} + C_{gd}$$

### \* Technology Scaling :-

⇒ Main aim of VLSI design to achieve smaller time width and area for higher package density.

⇒ scaling is used to achieve -

- a) Maximum count of gate on chip
- b) Minimum size of device
- c) Minimum power dissipation
- d) Maximum frequency of operation

⇒ Scaling has three types

- i) constant Field scaling

- ii) constant voltage scaling
- iii) Lateral scaling
- i) constant field scaling :-

⇒ constant field scaling can be obtained by applying dimensionless factor  $\propto$  to dimension.

⇒ In constant field scaling, device is scaled down by factor  $s$  to preserve magnitude of internal electric field constant for this scaling potential.

⇒ The parameters which are independent on electric field remains same after scaling.

<u>Scaling parameter</u>	<u>Before scaling</u>	<u>After scaling</u>
channel Length ( $L$ )	$L$	$L' = L/s$
channel Width ( $w$ )	$w$	$w' = w/s$
channel area ( $A$ )	$A = w \cdot L$	$w' = \frac{w}{s}, L' = \frac{L}{s} \Rightarrow A' = \frac{w}{s} \cdot \frac{L}{s} = \frac{wL}{s^2}$
Supply voltage ( $V_{DD}$ )	$V_{DD}$	$V_{DD}' = \frac{V_{DD}}{s}$

Threshold voltage ( $V_T$ )

$$V_T$$

$$V_T' = \frac{V_T}{S}$$

Junction depth  $\alpha_j$

$$\alpha_j$$

$$\alpha_j' = \frac{\alpha_j}{S}$$

doping densities

$$N_A$$

$$N_A' = S \cdot N_A$$

$$N_D$$

$$N_D' = S \cdot N_D$$

oxide -  $C_OX$   
capacitance  
 $C_OX$

$$C_{OX}$$

$$C_{OX}' = S \cdot C_{OX}$$

drain current  $I_D$

$$I_D$$

$$I_D' = S \cdot I_D / S$$

power dissipation  
 $P_d$

$$P_d = V_{DD} \cdot I_d$$

$$P_d' = \frac{V_{DD}}{S} \cdot \frac{I_d}{S}$$

$$= \frac{V_{DD} \cdot I_d}{S^2}$$

### ii) Constant voltage scaling :-

⇒ In constant voltage scaling, all dimensions of MOS are reduced by scaling factor  $S$  by keeping their supply voltage & other terminal voltages constant.

⇒ Parameter independent on supply voltage remains same after scaling.

### Scaling parameter

channel length  $L$

### Before scaling

$L$

### After scaling

$$L' = L/S$$

channel width  $w$

$w$

$$w' = w/S$$

channel Area

$$A = w \cdot L$$

$$A' = \frac{w \cdot L}{S^2}$$

Supply voltage  $V_{DD}$

$V_{DD}$

$$V_{DD}' = V_{DD}/S$$

threshold

voltage  $V_T$

$$V_T$$

Junction depth  $x_j$

$$x_j$$

$$x_j' = \frac{x_j}{S}$$

doping densities

$$N_A$$

$$N_A' = S^2 N_A$$

$$N_D$$

$$N_D' = S^2 N_D$$

oxide capacitance

$$C_{ox}$$

$$C_{ox}' = S \cdot C_{ox}$$

drain current

$$I_D$$

$$I_D' = S \cdot I_D$$

power dissipation

$$P_d = V_{DD} \cdot I_d$$

$$P_d' = V_{DD} \cdot S \cdot I_d \\ = S \cdot P_d$$

### iii) Lateral scaling :-

In lateral scaling only gate length is scaled. Lateral scaling is easy to implement

### Advantages of scaling :-

- High chip density ie. more no. of gate on chip
- Improved chip performance
- improved device characteristics
- reduced chip cost
- reduced power dissipation
- reduced parasitic capacitance

### Disadvantages of scaling :-

- Power consumption per unit area increases. Hence device get heated during operation.
- Due to scaling carrier mobility decreases which reduces gain of device
- Reduced conductor size reduces current carrying capacity
- Forced cooling is needed to avoid heating.