

VLSI - Very large scale Integration.

- Design using HDL - Hardware description language
- HDL - standard language which could be used by all digital designers to have uniformity in design.
- Therefore, companies designed VHDL language known as VHDL-93 or IEEE STD 1076.
- VHDL cannot model digital system expressed on transistor level.
- VHDL is modelling?
- Define all signals through which our will interact with real world. \Rightarrow Input and output
- Defining the logical relationship between input and output signals.

Type:-

1. Structural Description:- The circuit is described as interconnection of known components.
2. Behavioural Description:- The behaviour of circuit is described by mean set of sequential instructions.
3. Dataflow Description:- The behaviour of circuit is described by mean of boolean equations.

VHDL model:-

It contain following building blocks:-

1. Library section. (LS)

2. Entity Declaration (ED)

3. Architecture Block. (AB)

4. Configuration Declaration (CD)

5. Package. . (P)

(1), (2), (3) are compulsory blocks, (4) and (5) are optional.

- VHDL model for smallest possible digital system
i.e. NOT gate must have LS, ED, AB.

Syntax for LS:-

```
library IEEE;
```

```
use library_name. package-name. function-name;
```

```
use IEEE.std_logic_1164.all;
```

```
use IEEE.std_logic_unsigned.all;
```

* Entity Declaration:

- ED is like a wrapper for architecture, hiding the details of what is inside it.

Syntax:-

```
ENTITY entity-name is port (
```

```
    signal-name1 : signal-mode signal-type;
```

```
    ;
```

```
);
```

```
END entity-name;
```

- Entity declaration starts with name of entity. It lists the set of interface ports ports are signals through which entity communicates.

e.g. Entity and2_gate is

Port(

A, B : * in BIT ;

C : out BIT ;

);

End and2_gate ;

'in' and 'out' are signal direction.

in - input port

out - output port.

The entity and2_gate has two inputs port A and B and one output port C.

* Architecture Block:-

- It defines what actually circuit does.
- It describes the actual function of circuit.
- Syntax :-

Architecture arch-name of entity-name

Begin

$c \leftarrow A \text{ AND } B \}$ → logic statement.

end ~~Arch~~ arch-name ;

- A higher level architecture may use lower level entity many times and multiple top-level architecture may use the same lower level one.
- VHDL also allows defining multiple architectures for single entity and it provides configuration management facility that allows you to specify which to use.

* Data ~~types~~^{objects} :-

- Three basic types of objects in VHDL:-
Signal, constant, variable.
- Data object associated with its type and value.
- The value that an object can take will depend on the definition of type used for that object.
- Scope :-
 1. Object declared in package → available to all VHDL descriptions that use that package
 2. Object declared in entity → available to all architectures associated with entity.
 3. Object declared in architecture → available to all statements in that architecture
 4. Object declared in process → available only within that process

1. Constants:-

- Constants are objects that are assigned a single value of that type.
- Once assigned cannot be changed during simulation.
- It can declared as follows:-

Constant constant_name : type_name [:= value];

- e.g.

constant DELAY1 : time := 4ns ;

- For use in architecture we can declare constant at the start of architecture
- For global use of constant , we can declare package.

2. Variables:-

- Variables are objects used to store a single value and can be updated using variable assignment statements.
- Variables in VHDL similar to variables in programming language

- The variable declaration is as follows-


```
variable variable-name : type-name [:= value];
```
- e.g.


```
variable A : bit := 0;
variable SUM : integer range 0 to 256 := 16;
```
- It can be updated using variable assignment statement such as-


```
variable-name := expression.
```
- Updation of variable is without any delay.

3. Signals:-

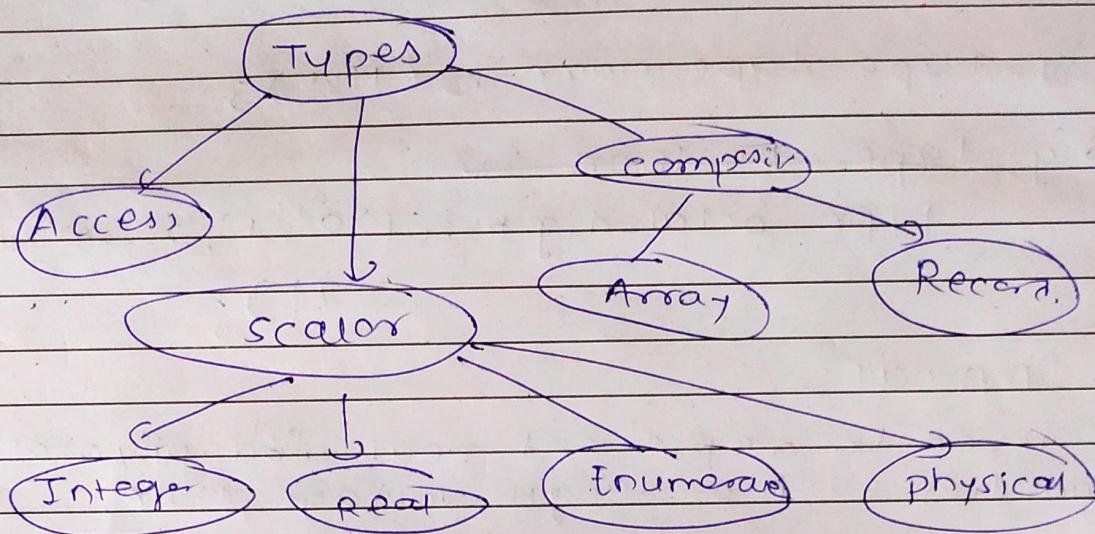
- Used for communication b/w VHDL components.
- Signals can be considered as wires that can have current value and future values.
- As wires are used to connect components on circuit board, signals are used to connect concurrent elements.
- Syntax,-


```
signal signal-name : signal-type [:= value];
```
- signal sum, carry : std_logic;


```
signal a : bit;
```
- Signal declared in external package is global otherwise declared in architecture are locally used within architecture.

* Datatypes:-

- All data objects in VHDL must have type
- The data type specifies the range or set of values that the object can take.



1. Scalar :-

- Scalar types represent single value.

1. Integer:-

- Type integer defined as range of integers including at least the range $-2^{31} + 1$ to $2^{31} - 1$

- Syntax:-

Variable a: Integer;

2. Real :-

- For real the range of values it can take is -1.0×10^{38} to 1.0×10^{38} .
- Variable a: REAL;

3. Enumerated:-

- Used to describe own unique data types.
- User specifies list of possible values

e.g. type type-name is (list);

e.g. type boolean is

type octal-digit is ('0','1','2','3','4','5','6','7');

4. Physical :-

- used to represent real world physical quantities such as length, voltage, time.

- type resistance is range 0 to 100,00,000

Units

ohm;

Kohm = 1000 ohm;

Mohm = 1000 Kohm;

END Units;

Arrays:-

- used to group elements of same type into single object

- type byte is array (0 to 31) of bit;

type reg-type is array (15 DownTo 0) of bit;

- variable x : reg-type; Variable Y: BIT;
Y := x(4); \leftarrow Y gets value of element at index 4

1 -

QCA -

Package:-

- A package represents a program unit that contains group of logically related declaration.
- User defined constructs declared inside architecture and entities are not visible to other VHDL component.
- std_logic is defined in package ieee.std_logic_1164 in ieee library
In order to use std_logic it is required to specify library and package.

```
library IEEE;  
use IEEE.std_logic_1164.all;
```

- Syntax of package declaration:-

```
Package package-name is  
    Declaration are written here;  
End package-name;
```

- Once it is declared, it can be used by any VHDL entity by using two statements

```
Library WORK;  
use WORK.package-name.all;
```

Attributes:-

- Attributes provide information about certain items in VHDL.
- Attributes consist of quote mark 's followed by name of attribute.

1. Signal_name event:- It returns boolean value true if an event on signal occurred, otherwise gives a false

e.g. if (clock'event and clock='1') — rising edge clk

2. Range kind attributes:- It return range.

3. ~~Value is~~