* Unit 5: Application Specific Integrated Circuits

- Cell design specifications, Design Flow:
  - Spice simulation:
    - AC and DC analysis
    - Transfer characteristics
    - Transient responses
    - Noise analysis
  - Design Rule:
    - Lambda rule
    - micron rule.
  - Design Issues:
    - Antenna Effect
    - Electro Migration Effect
    - cross talk and Drain punch through
    - Timing analysis.

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* Antenna Effect:

- plasma induced damage.
- Antenna effect refers to accmulation of charge on conducter connected to gate during the fabriccation process.
- The wire connected to gate acts as antenna. The diodes formed by drain and source diffusion layer can conduct significant amount of cur
- This effect may cause gate failures or deteriorate IV characters

Techniques to reduce effect

1) Reduce the build up charge by optimizing the processing steps.

2) Embedding protection diode

3) Break signal wires and route to upper metal layer by jumper section.

* Electromigration:

- Electromigration is physical design issue.
- Electromigration is movement of atoms based on current flow through the material.
- If current density is high, the heat dissipated within the material will repeatedly break the atoms from structure and move them.
- Electromigration can cause shorts and voids in the interconnect leading to failure of interconnect.

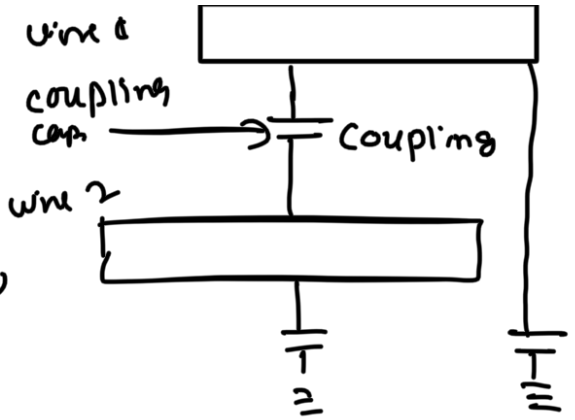
- As technology nodes getting smaller, EM is becoming physical roadblock in scaling of interconnect.

- Techniques to prevent electromigration:
  1. Increase in metal width to reduce current density.
  2. Lower the supply voltage.
  3. Shorten wire length
  4. Reduce the frequency.

* Cross talk:

- Unwanted transfer of signal from one place to another through coupling capacitors is called Cross talk.

- Wire 1 → C_1 → V_1
  Wire 2 → C_2 → V_2



- If each wire were isolated,
  $Q_1 = C_1 V_1$
  $Q_2 = C_2 V_2$

- Two wires coupled by coupling capacitance.
  $\therefore Q_1 = C_1 V_1 + C_{coupling} V_2$
  $Q_2 = C_2 V_2 + C_{coupling} V_1$

- Differentiating we get.

$$i_1 = \frac{dQ_1}{dt} = C_1 \frac{dV_1}{dt} + C_{coupling} \frac{dV_2}{dt} \quad -(1)$$

$$i_2 = \frac{dQ_2}{dt} = C_2 \frac{dV_2}{dt} + C_{coupling} \frac{dV_1}{dt} \quad -(2)$$

eq. (1) and (2) shows that whenever voltage of one line changes, it result in charge in both 1, and in current.

- Two effects: (1) crosstalk noise (2) crosstalk delay

Techniqun to reduce:
(1) increase spacing between wires will reduce crosstalk
(2) Plate ground lines or VDD between signal lines.

* Drain Punch Through:-

- When a drain is at high voltage, w.r. source, the depletion region around the drain may extend to source, causing current to flow irrespective of gate voltage. This is known as drain punch through condition. and punch through voltage

V_{PT} is given by,

$$V_{PT} = \frac{q_b \cdot N_a \cdot L^2}{2\epsilon}$$

q_b = charge, N_a = dopin concenration,
L^2 = channel length

- Channel length (L) (↓) ⇒ V_{PT} ∝ (↓).

- Punch through voltage highly depends on drain voltage and on source drain junction depths.

- This effect is undesirable as it increases output conductance and limit max. operating voltage of device.

- How to Reduce?
  - increase overall bulk doping level.
  - avoided using
    a) delta doping
    b) halo implant
    c) packet implant.

* Timing Analysis:

- Timing Analysis is used to verify whether ckt meets all its timing requirements.
- Three types:- 1. time, 2. power, 3. area of design constraint
- Two types of timing analysis:

1. Static timing analysis: cheks static delay requirements of circuit without i/p or o/p.
2. Dynamic timing analysis: verify functionality of design by applying i/p vector and checking

correct o/p vector.

- Basis of all timing analysis is clock and seq. components. i.e Flip flop, Latches.

- Clock should be glitch free.

- When passing data from one clock to other, ensure that worst case duty cycle is used for calculation.

* Design Rule Check :