

Unit-2

Digital Design of Issues

SOC

System on chip is packaging of all necessary electronics components required for system on single integrated circuit.
eg.

Mobile phones, digital camera

=> SOC for mobile phones consists of audio receiver, transmitter, analog to digital converter, processor, SRAM and display etc.

=> SOC design uses intellectual property blocks - (IP)-blocks which is predefined component that can be used in larger designs.

=> IP blocks has two types -

IP blocks

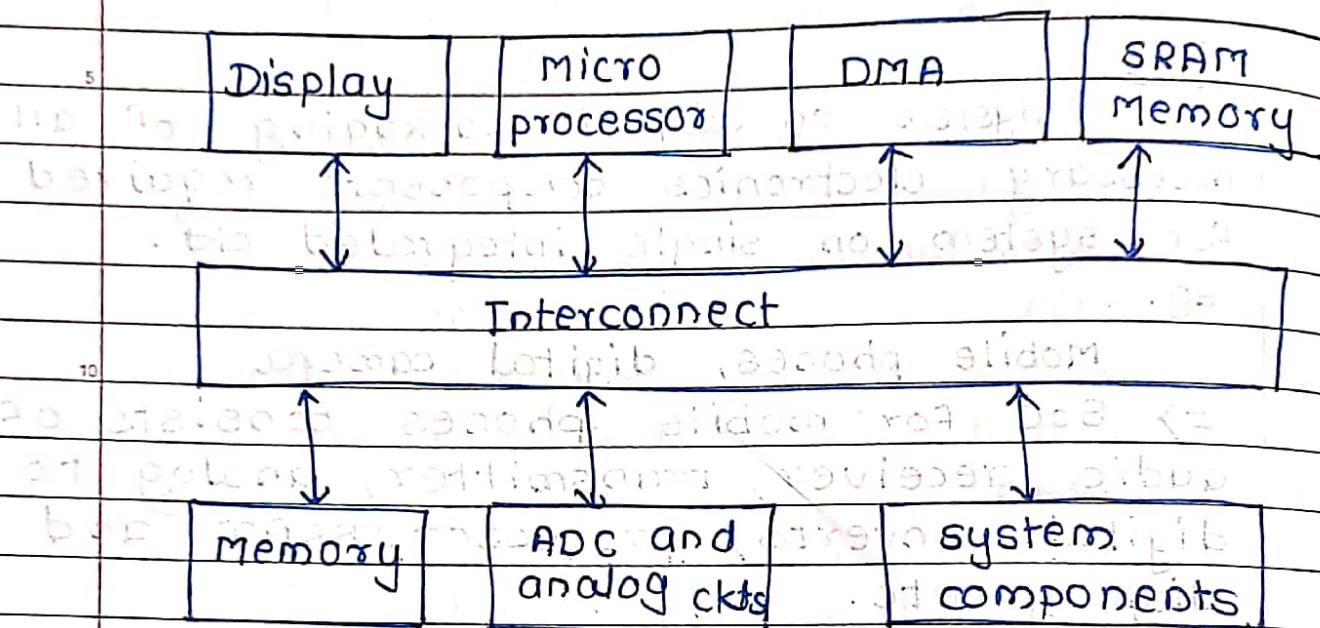
ot additional field RF band
radio and other functions

Hard IP

SOFT IP

- predefined layout
- full layout is available
- block size, power consumption & performance can be measured accurately.
- It can be easily targeted to new technology
- large size and not fast.
- synthesizable model
- in hardware description language.

⇒ Basic SOC system model is as shown,



⇒ While designing SOC, ensure that all IP blocks work properly ie.

all types of functions such as arithmetic, logical, functions, performance, power consumption and testability must be verified.

⇒ Each IP block must be able to communicate with each other.

⇒ Many sysm uses embedded software. Many SOC uses windows CE, Linux and palm os to provide networking and management.

⇒ Advantages of SOC over system on board

- less power consumption
- less size

- performance is better
- low cost
- Interfacing is easier bet' n diff blocks.

* Clock skew :-

In every VLSI system, some of the storage elements are needed for state storage. This storage elements are operated by clock. i.e. all synchronous

\Rightarrow Clock skew is phenomenon of in synchronous ckt in which same sourced clock signal arrives at different components like latches and flip flop at different times.

\Rightarrow This can be caused by,

- wire interconnect length
- temperature variation
- variation in intermediate devices
- capacitive coupling
- material imperfections
- diff. bet two input capacitances of clock input.

\Rightarrow As clock rate increases, timing becomes more critical and less variation can be tolerated in ckt.

\Rightarrow Clock skew has two types

① positive skew

② negative skew

① Positive skew :-

Positive skew occurs when transmitting register receives clock tick earlier than receiving register.

② Negative skew :-

Negative skew occurs when receiver register receives clock tick earlier than transmitting register.

Zero clock skew refers to arrival of clock signal simultaneously at a transmitter register and register of receiver.

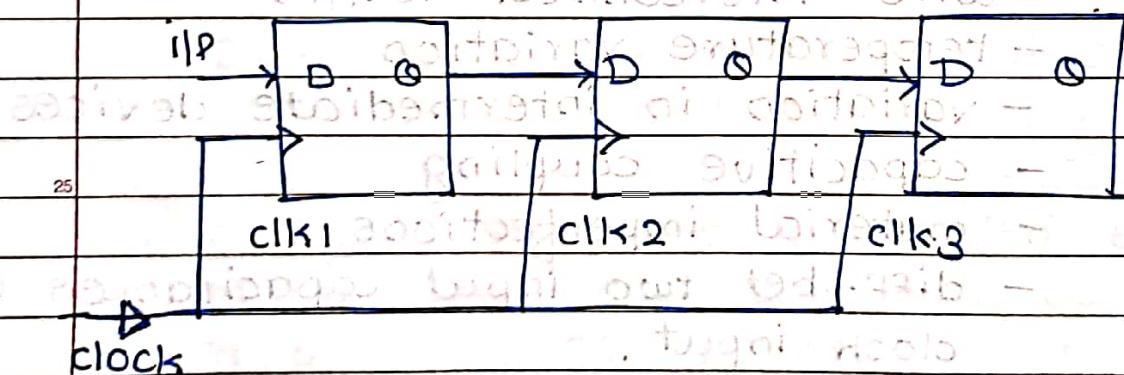
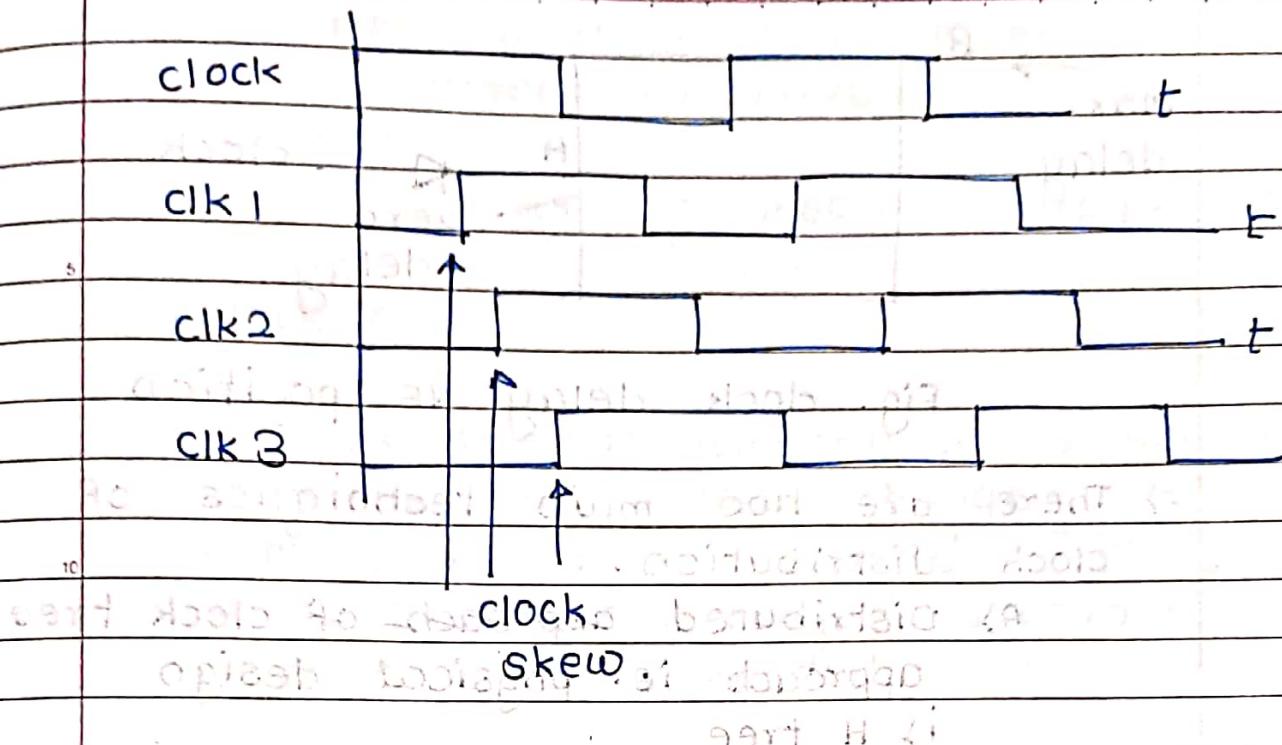


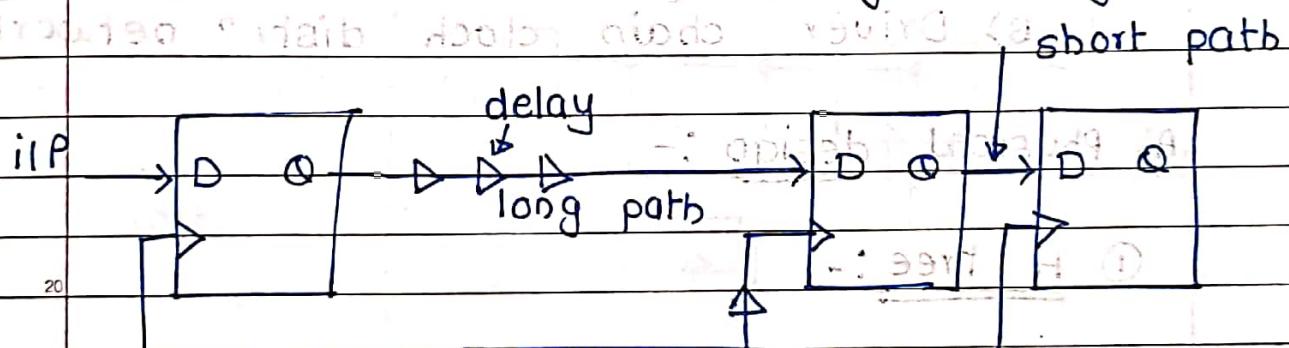
Fig. sequential registers with

clock skew.

We have applied clock to three sequential registers, but it will reach at diff. times at each register.



⇒ To avoid long path clock skew, we can add small amount of delay in long path.



* Clock Distribution Techniques :-

clock distribution in VLSI system is challenging due to large capacitive load. clock distribution comes under floor planning because clock delay varies with position of block on chip.

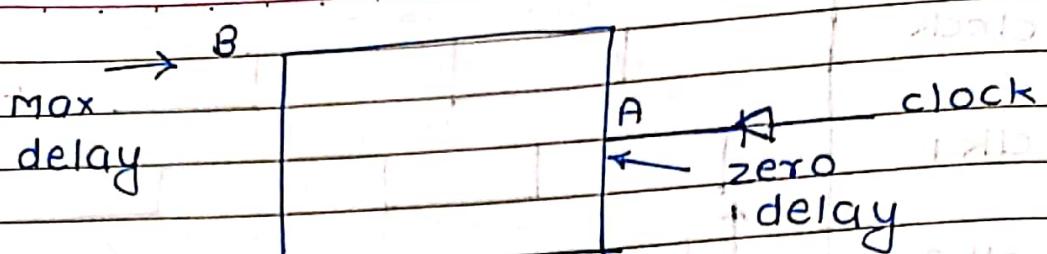


Fig. clock delay vs position

=> There are two main techniques of clock distribution.

A) Distributed approach of clock tree approach ie. physical design

i) H tree

ii) balanced tree

iii) clock grid

B) Driver chain clock distr? network.

A) Physical design :-

① H tree :-

for H structure, four smaller H structures are attached at four endpoints of H.

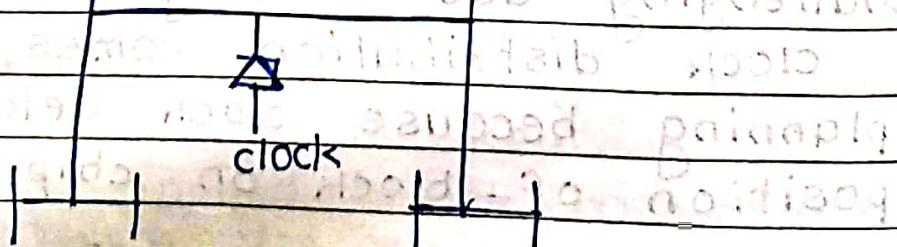
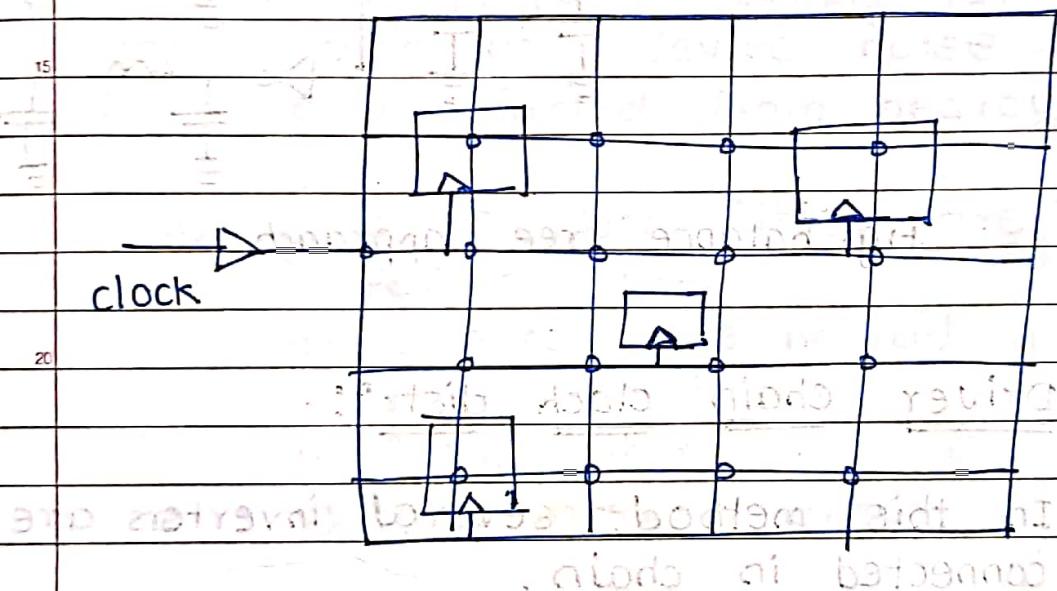


Fig. H-tree approach

- H tree approach has low skew
- It requires big driver ∴ lots of power.
- lots of routing resources required.

② Clock Grid

- clock grid implementation is simple.
- insensitive to load changes.
- More power is required.
- drivers are arranged in parallel.
- More area is needed.



3) Balance Tree:-

- Most common topology for high performance chips.
- Usually heavy use of automated tool
- Place buffer first and cluster FF around them!
- must match interconnect RC delay.

- It takes 3-4 metal layers to implement.
- Uses small metal
- low c load
- small buffer

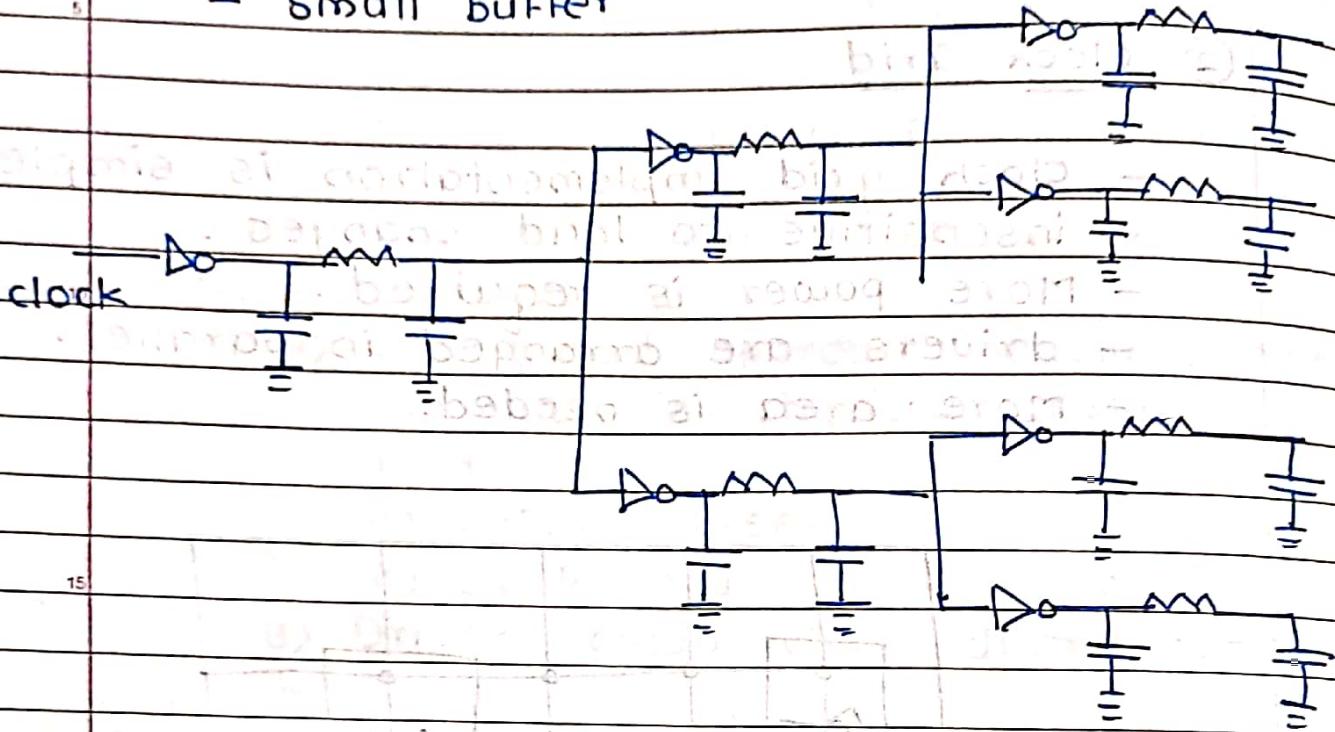


Fig: balance tree approach.

B) Driver chain clock distr'.:-

In this method, several inverters are connected in chain.

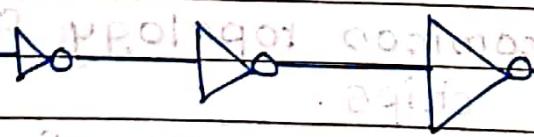


fig. driver chain

In this, logic delay increases if capacitance attached to logic ckf becomes larger.

- Thus can not be used for high capacitance clk.
- In each inverter current is \propto times more than previous inverter.

* Clock Jitter :-

clock jitter is timing variations of a set of signal edges from their ideal values.

\Rightarrow jitter in clock are caused by noise or other disturbances in system, thermal noise, power supply variations, loading conditions, device noise and interference coupled from nearby cks.

\Rightarrow Types of clock jitter are.

i) Period jitter

ii) cycle to cycle period jitter

iii) long term jitter

iv) Phase jitter

v) time interval error.

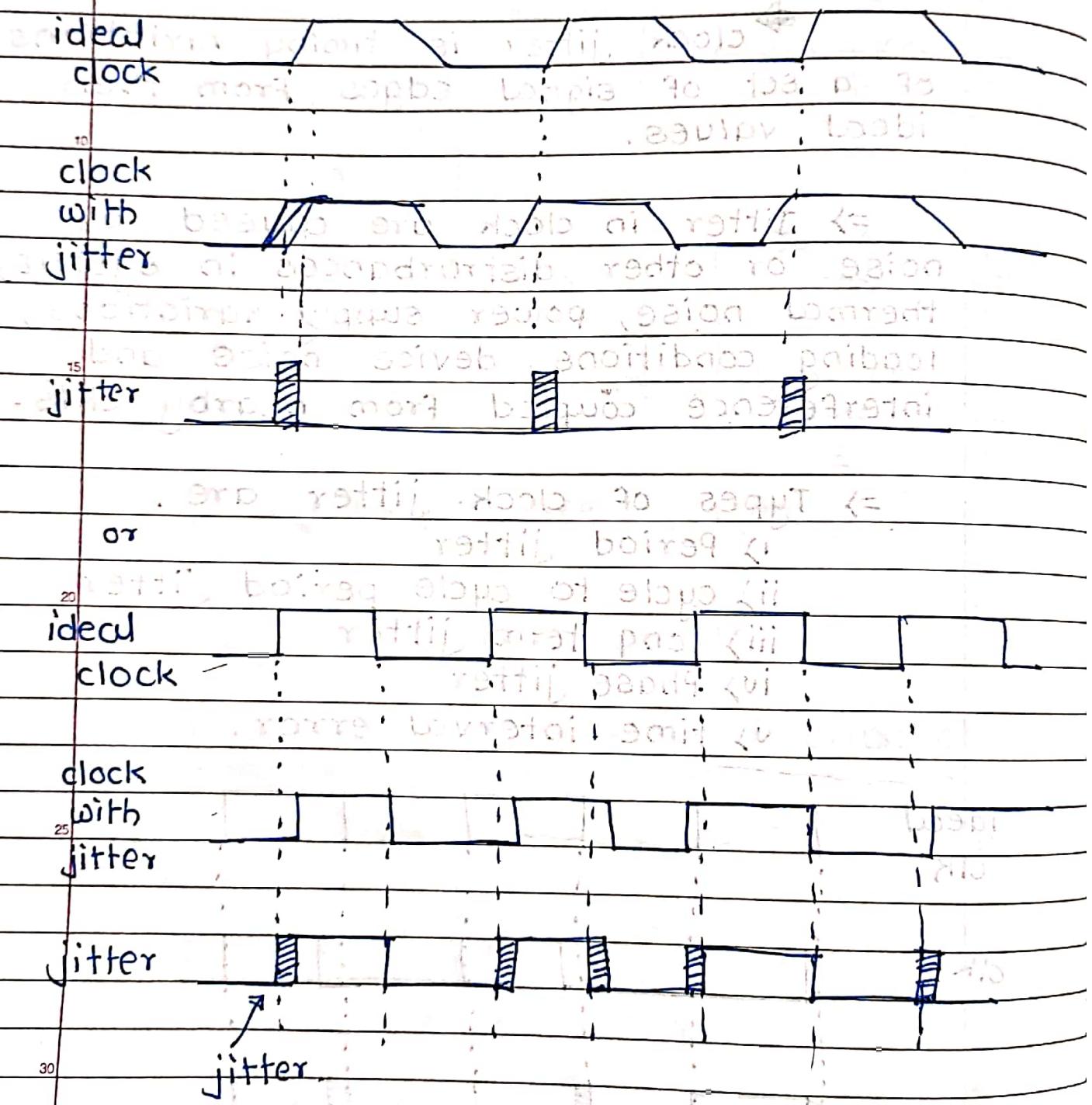
ideal

clk

clk

jitter

\Rightarrow Period jitter is deviation of cycle time of clock to the ideal period.
 Period jitter can also be defined as measured clock period and ideal clock period.

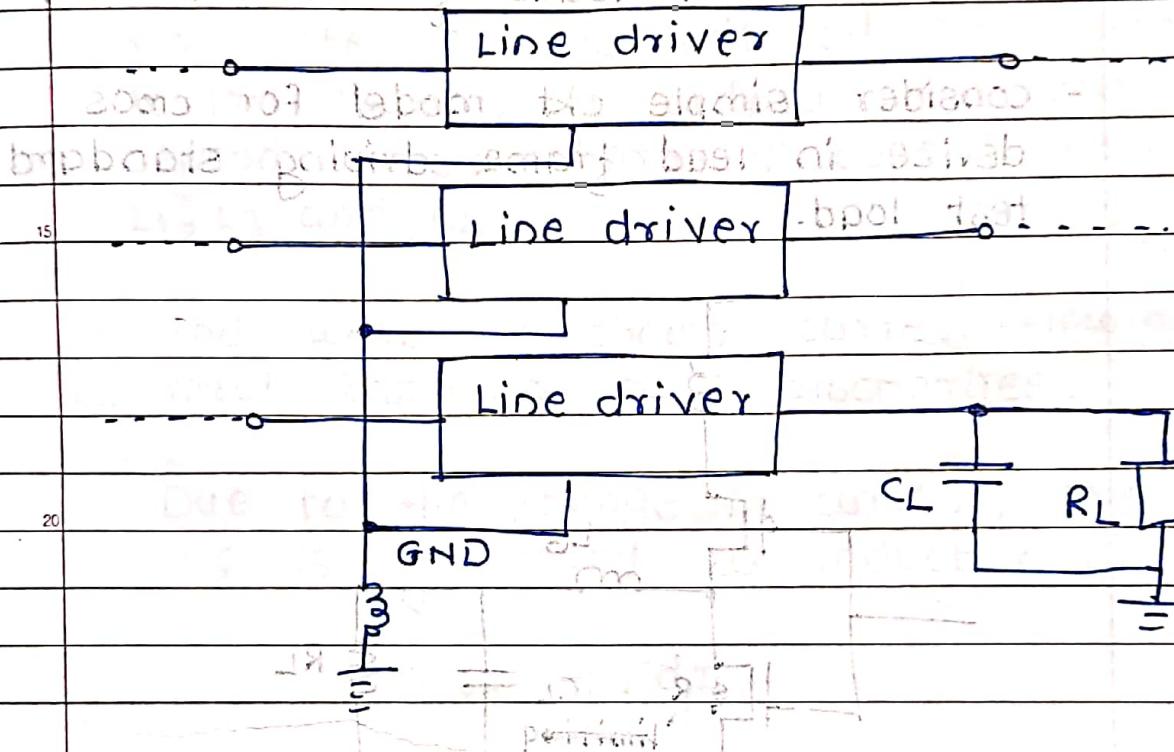


* Ground Bound :-

Ground bounce is a phenomenon associated with transistor switching where the gate voltage can appear to be less than the local ground potential causing unstable operation of logic gate.

Set of sub example will show how ground bounce occurs.

Let's consider about the ground bounce.



- Ground bound takes place in VLSI ckt's when supply to logic gate has low resistance connection with ground.

When a gate is turned on, current flows through source to drain. Due to this silicon vicinity of source is pulled high above local ground.

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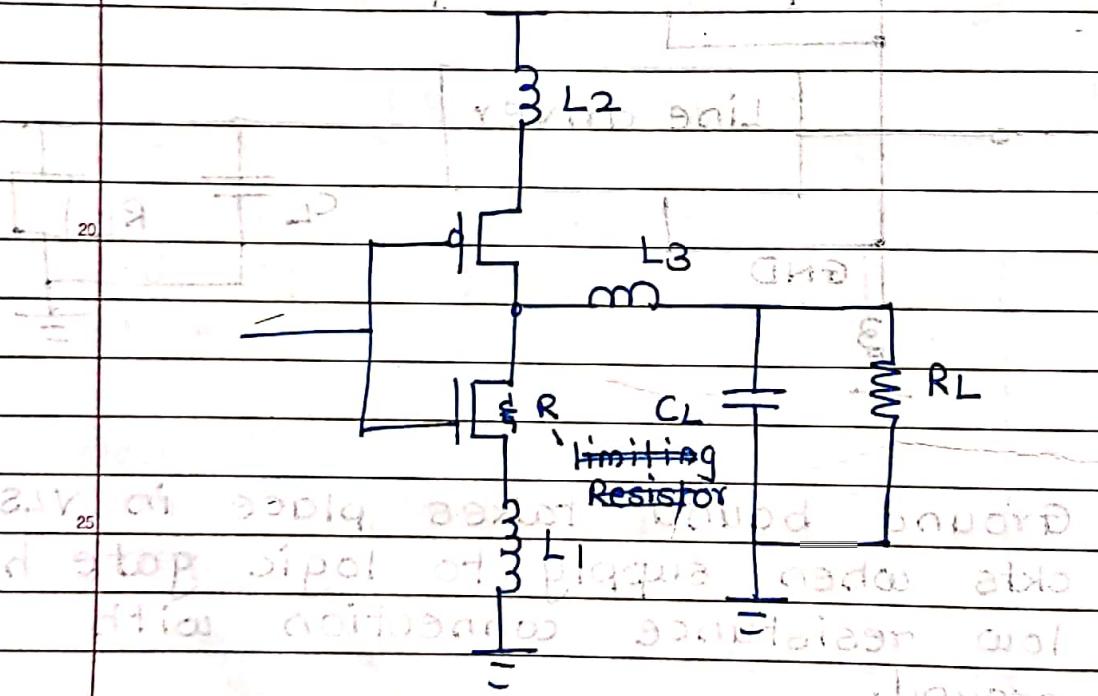
Flows through source to drain. Due to this silicon vicinity of source is pulled high above local ground.

- Relative to this voltage gate v_{tg} can go negative thus shutting OFF the transistor.

- when the local charge dissipates, the xistor turn back ON causing repeat of phenomenon causes

* \Rightarrow Ground bound may occurs due to the intrinsic electrical chara. ie. inductance found in all leads frame material.

- consider simple ckt model for cmos device in lead frame driving standard test load.

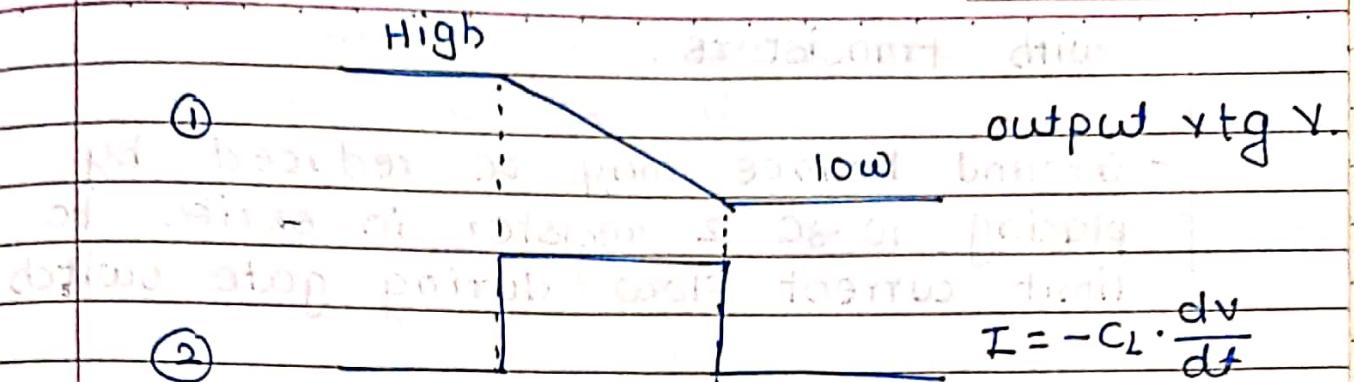


L_1 = intrinsic inductor in ground leads

L_2 = intrinsic inductor of power leads

L_3 = intrinsic inductance of output leads

$C_L \& R_L$ = standard test load.



$$(3) \quad V_{GB} = L \cdot \frac{dI}{dt}$$

- due to change in output voltage \Rightarrow $V_{GB} = L \cdot \frac{dI}{dt}$

- higher voltage leads to more current

- when the load is switched from high to low logic, the output slew rate depends upon characteristics of output x'stor, L_1, L_2 and C_{OL} . Due to dI/dt , there is a

- 1st waveform shows current flowing

out through capacitor when it discharges.

- 2nd waveform

- Due to other changes in current, the vtg is generated at inductor L_1 .

$$V_{GB} = L \cdot \frac{dI}{dt}$$

- when this voltage is greater than

gate vtg, x'stors are unable to switch ON.

* \Rightarrow Ground bound may also be generated during low to high transition.

\Rightarrow Ground bound may be generated due to large gate capacitances associated

with transistors.

- Ground bounce may be reduced by placing 10-20 Ω resistor in series to limit current flow during gate switch.

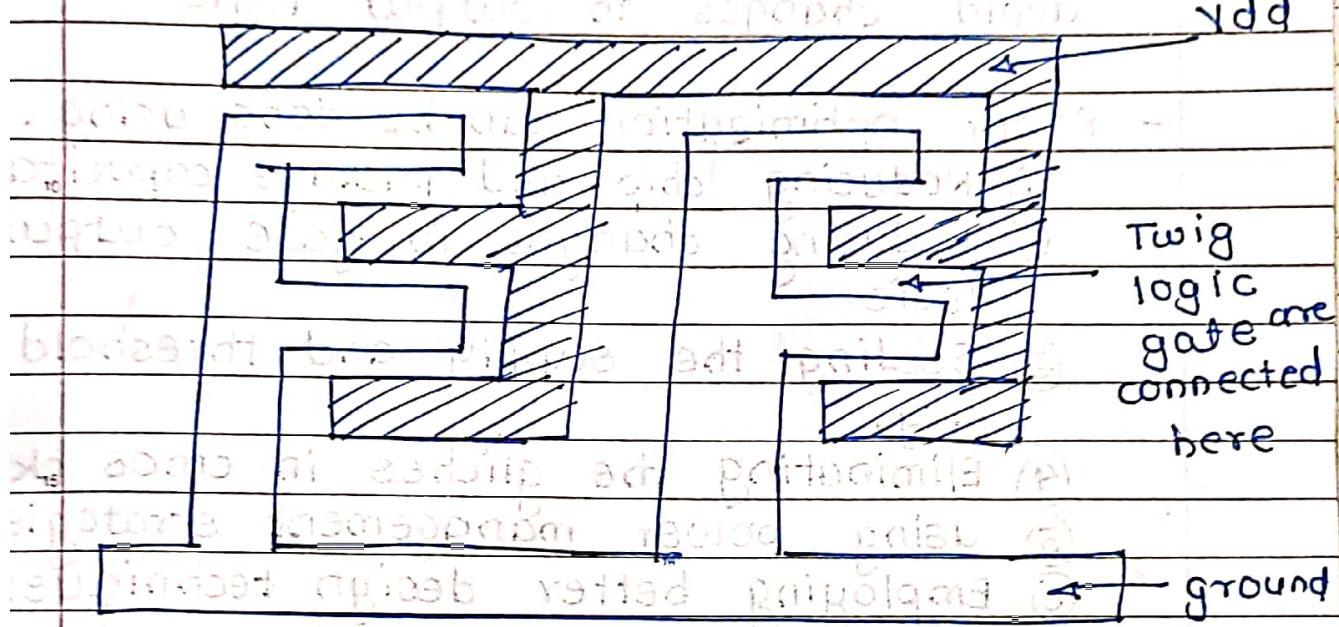
* Power distribution techniques :-

- Power distribution is important in VLSI design to ensure that required power is delivered without being destroyed.
- While designing global power distribution network, VDD and GND both should run entirely in metal.
- The functions of power distribution networks are -

- ① carry currents from pads to stores on chip.
- ② maintain stable voltage with low noise
- ③ provide average and peak power demand
- ④ provide current return path to signal inputs and outputs
- ⑤ avoid electromagnetism and self heating wearout.

- consume little area and wire.
- easy to lay out.

\Rightarrow Power and ground tree structure for power distribution.



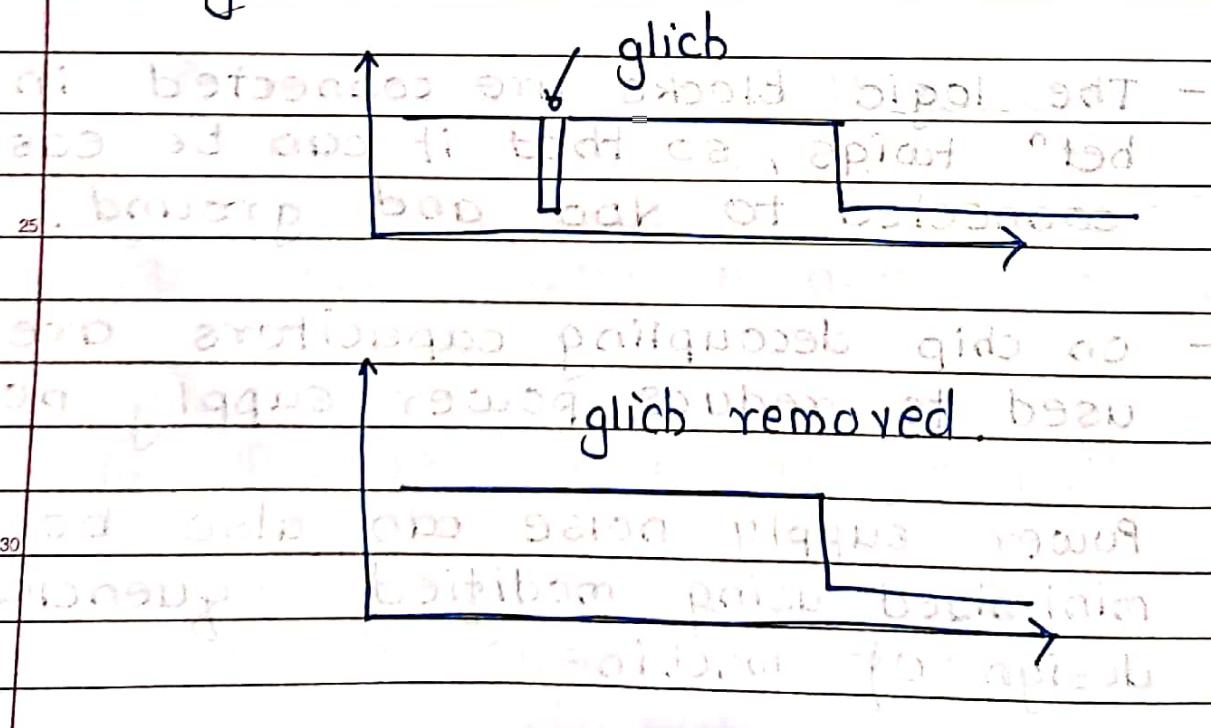
positions to bring in uniform data -
 Fig. shows power and ground tree
 for uniform power distribution.

- The logic blocks are connected in betw twigs, so that it can be easily connected to Vdd and ground.
- On chip decoupling capacitors are used to reduce power supply noise.
- Power supply noise can also be minimized using modified sequential design of machine.

* Power optimisation :-

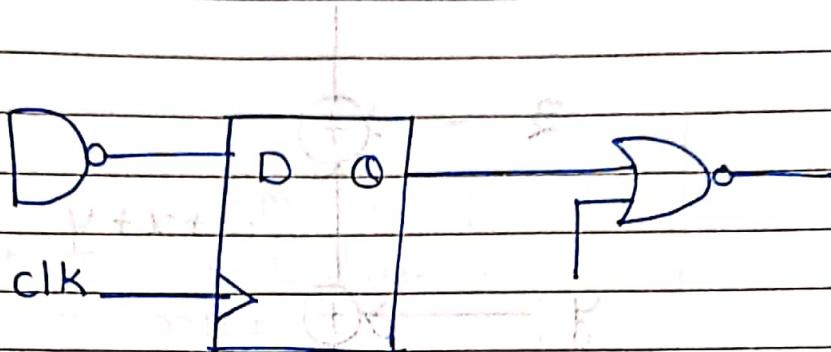
- Power consumption of gate is reduced if its output changes few times.
- We need to design logic networks which avoid changes in output logic.
- Power optimisation can be done using -
 - ① Reducing chip and package capacitance
 - ② Reducing changes in gate output logic
 - ③ Scaling the supply and threshold voltage.
 - ④ Eliminating the glices in cmos ckts
 - ⑤ using power management strategies
 - ⑥ Employing better design techniques.

- Glich reduction is applied efficiently to sequential logic than combinational logic.



- Glich is unwanted change in output logic.

- Glices can be avoided by using flip flops.



clk

Glich

- As shown in above figure, D flip flop changes its output only for positive edge of clock.

- If any glich occurs after positive edge of clock, it will not affect the output of flip flop.

- There is possibility of glices in long chain of gates.

eg. suppose we need to implement the function $x + y + z + w$

Then in long chain network, the implementation can be as follow,

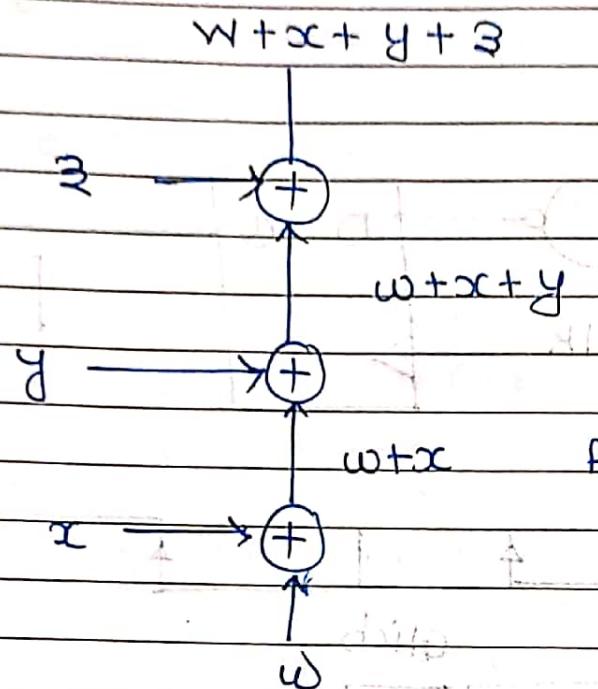


Fig. long chain

- In long chain signal arrives at each gate at diff. times, which causes glitches.

- This can be eliminated by using the balance tree structure, in which all gates signal reaches at same time.

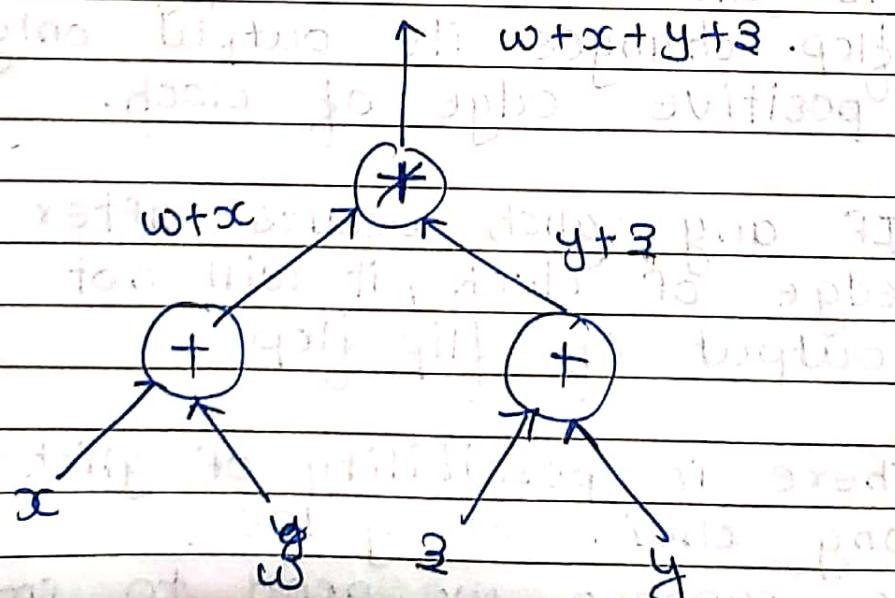
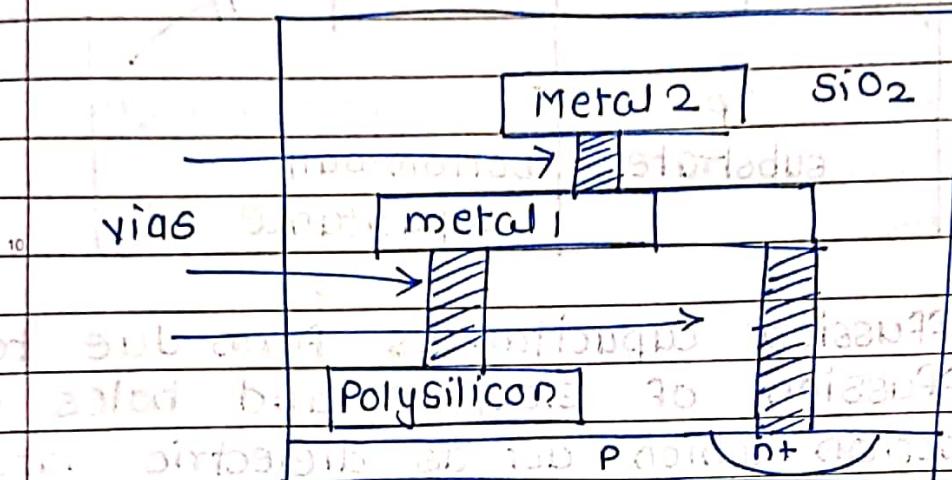


Fig. balance tree.

* Wire Parasitics :-

→ Parasitics elements are introduced due to wire, vias and x'stor in to ckts.



→ Vias are cuts in insulating SiO_2 , the metal thro' cut to make connection on desired layer.

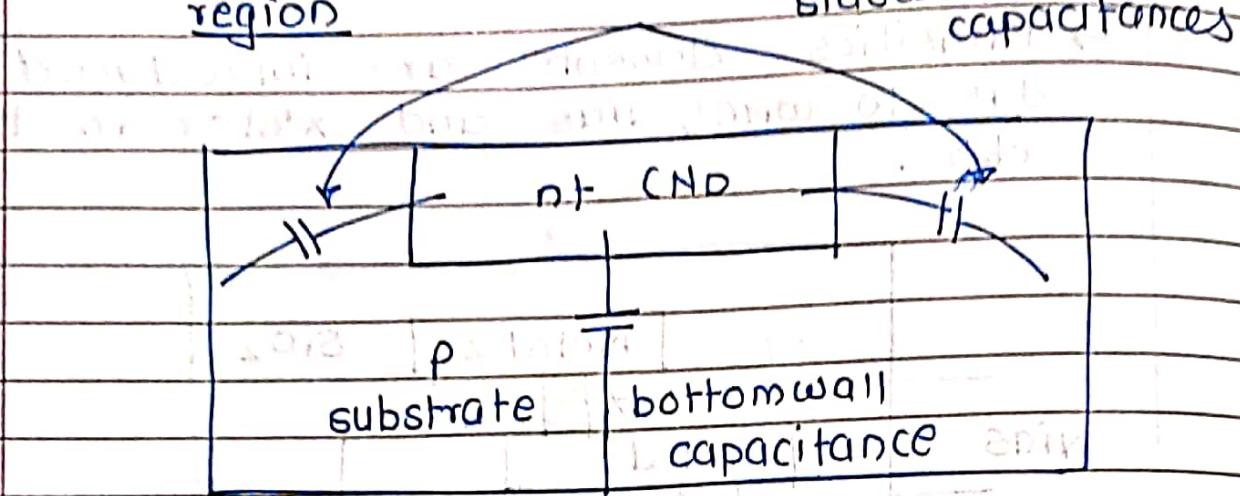
→ Wire has two types of parasitics.
 a) wire capacitances
 b) wire resistances.

a) Wire capacitances

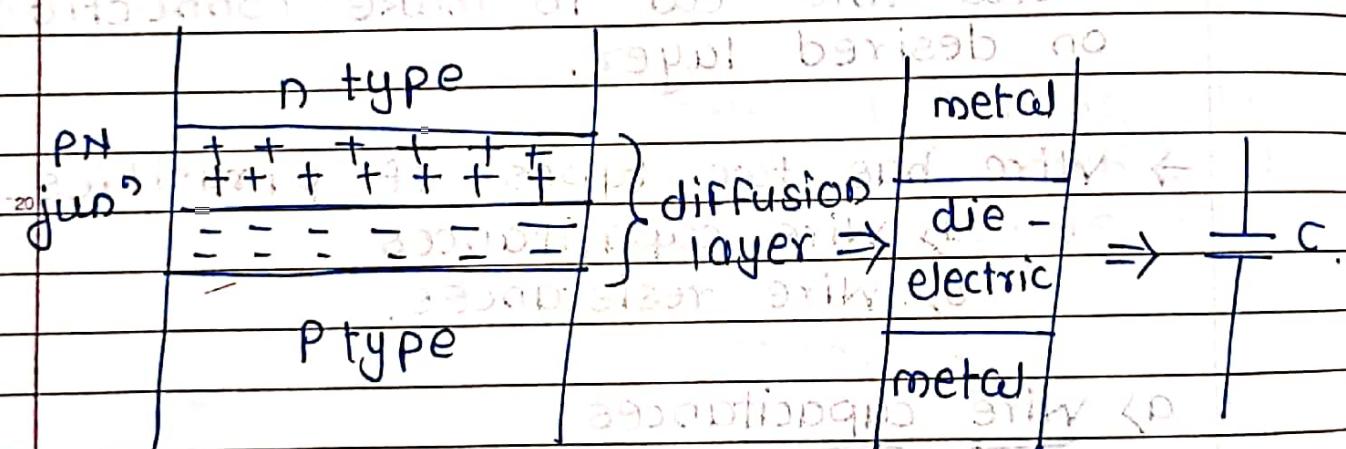
Wire has three types of capacitances.

- ① diffusion wire capacitance in ends of diffusion region
- ② capacitance due to poly & metal wire
- ③ capacitance due to different layers and wires.

i) Diffusion wire capacitances in diffusion region



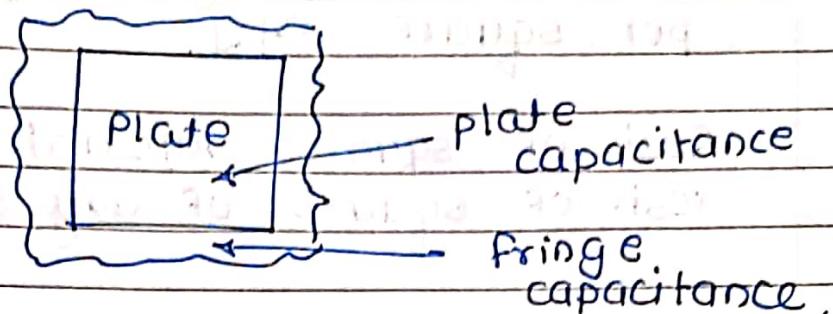
Diffusion capacitances form due to diffusion of electron and holes at P-N junction which act as dielectric material and P and N region as metal contact which performs capacitor structure.



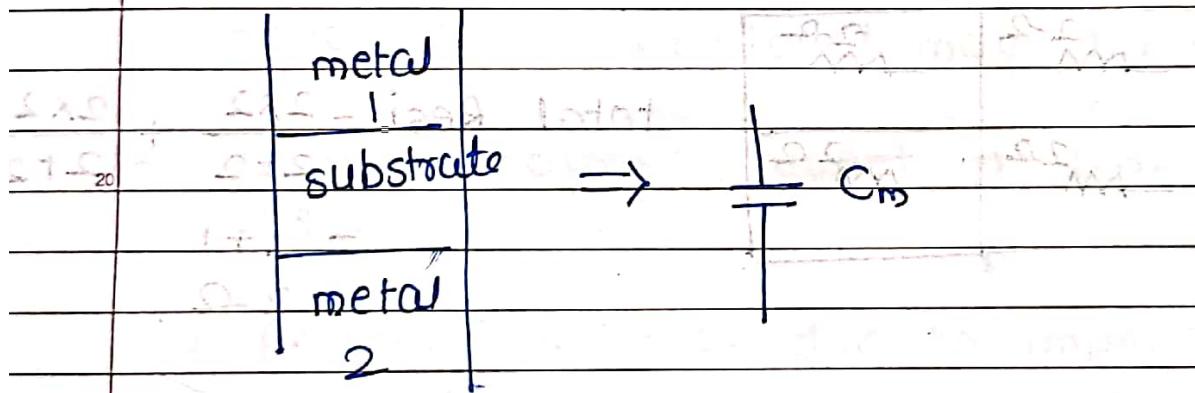
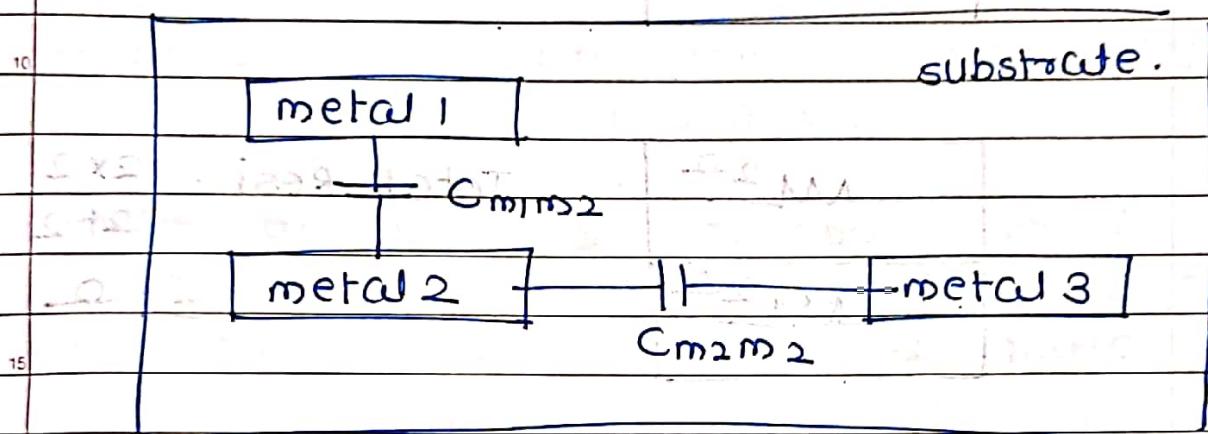
ii) capacitance due to poly and metal wire

capacitance is formed due to changes in electric field at the edges of metal plate, these are called as plate or fringe capacitances.

area of overlap of metal 1 & 2



iii) capacitance bet' diff layers of metal



As the total number of metal layers increases and capacitances of substrate decreases.

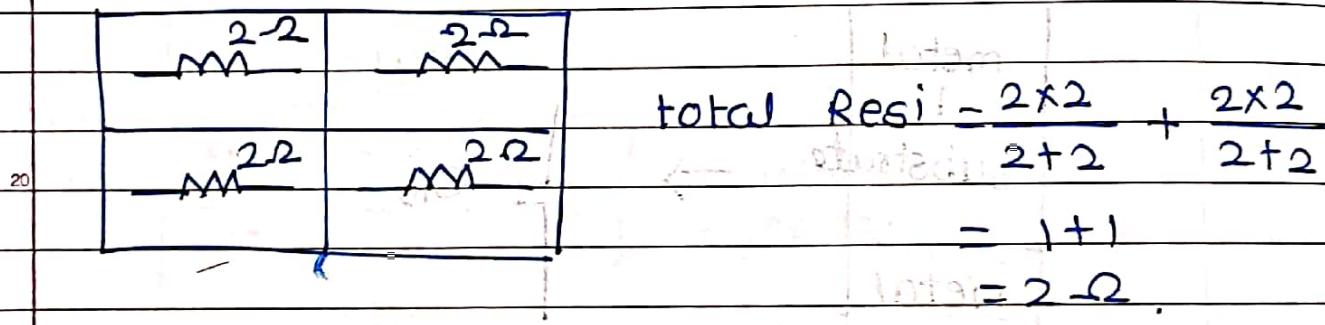
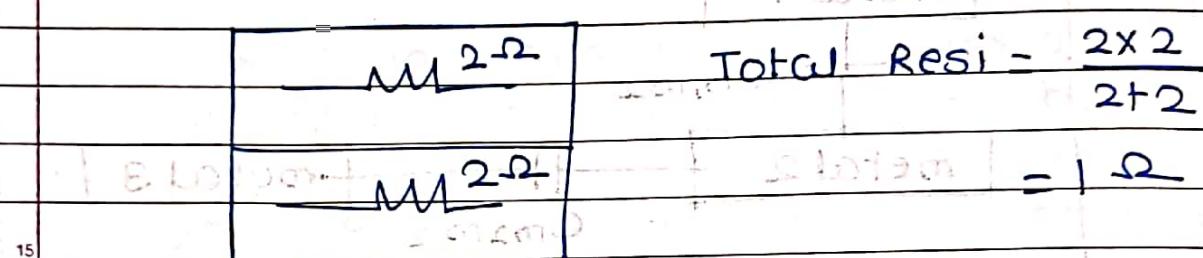
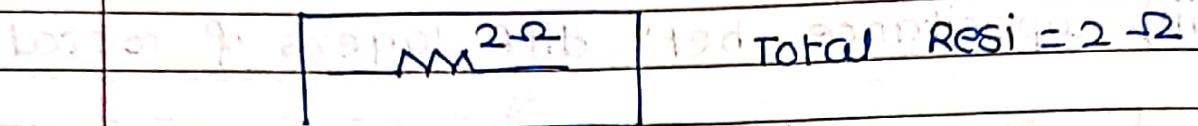
b) Wire Resistances :-

After calculating the layout

Wire resistance is calculated by measuring size of wire on the layout.

- Unit of resistivity is given by ohms per square $\Omega \square$.

- Resi. of square material is same as resi. of square of any size.

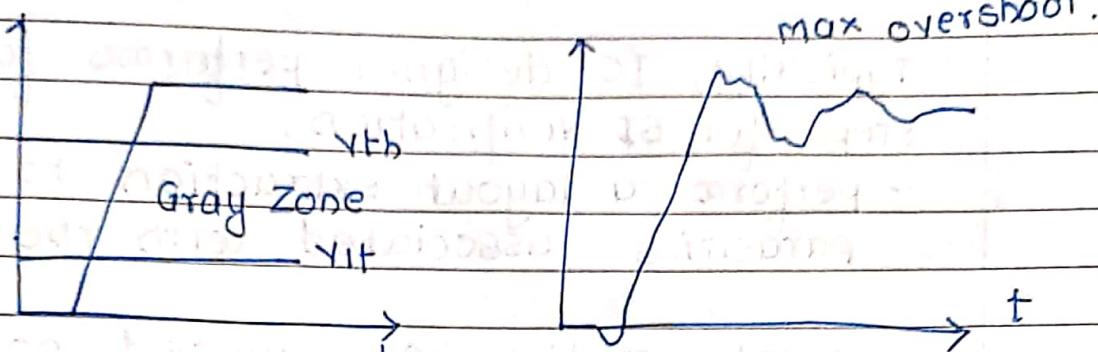


* Signal Integrity Issues

signal integrity is set of measure of quality of an electrical signal.

Digital signals are fundamentally analog in nature and subject to effect as noise, distortion, crosstalk & loss.

v_{tg}



- For digital systems, signal is transmitted in the form of 1 and 0.

For digital ckt's, v_{tg} above V_H is considered as logic high while voltage below V_L is considered as logic low.

- If signal value switches into gray zone, then logic level may change.

Common noises at present in VLSI ckt's are -

a) Reflection noise :- due to impedance mismatch, stubs, vias, and other interconnect discontinuities.

b) Crosstalk :- due to electromagnetic coupling bet' signal traces & vias.

c) Power / Ground noise :-

Due to parasitics of ground & supply leads. such as ground bounce & supply bounce.

SI verification

Typically, IC designer performs following steps for SI verification.

- perform a layout extraction to get parasitics associated with the layout.
- create a list of expected noise events, including diff. types of noises such as coupling and discharge sharing.
- create a model for each noise event.
- create a SPICE netlist or another simulation model that represents the desired expectation.
- run spice model. Analyze simulation results and decide whether redesign is required.

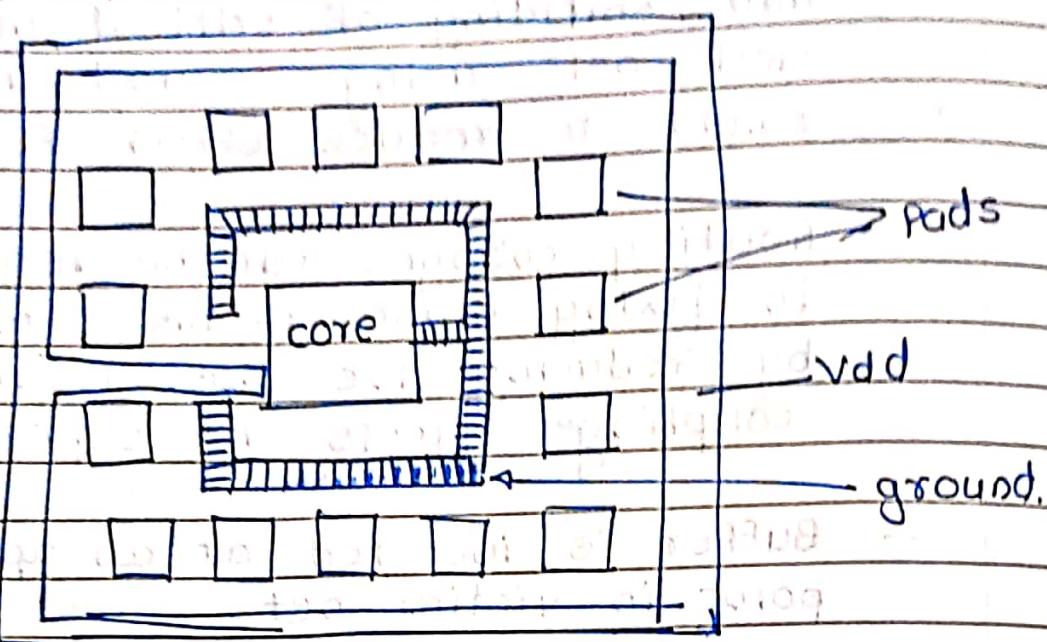
Solutions to SI problems:

- Remove impedance discontinuities. finding places where significant shift in impedance exists and adjusting the geometry of path to shift impedance to better match.
- Driver optimization.

- Add shielding of critical nets or clock nets using ground and VDD shields to reduce effect of crosstalk.
- 5 - Routing changes can be very effective in fixing noise problem mainly by reducing the most troublesome coupling effects via separation.
- 10 - Buffer is inserted at an appropriate point in victim net.
- 15 - Increase transition time of the attacking net by reducing driver strength.

* IO Architecture :-

- Pads are used to connect internal circuitry of IC to external input and outputs.
- 20 - Normally pads are distributed around the edges of chip.
- 25 - The pad must have enough area so that wire bond can be soldered to it.
- 30 - Each pad has standard width & height.
- IO arch* is shown as follow which consists of IO pads, core, VDD and Gnd tree.



3. In Middle position of pads there is chip core. So Do not do short circuit.

— The wires connected to pads should not be cross to avoid short circuit.

— The pads are arranged in some specific order.

— Routing and electrical noise can be generally determined by the order of pins on the package.

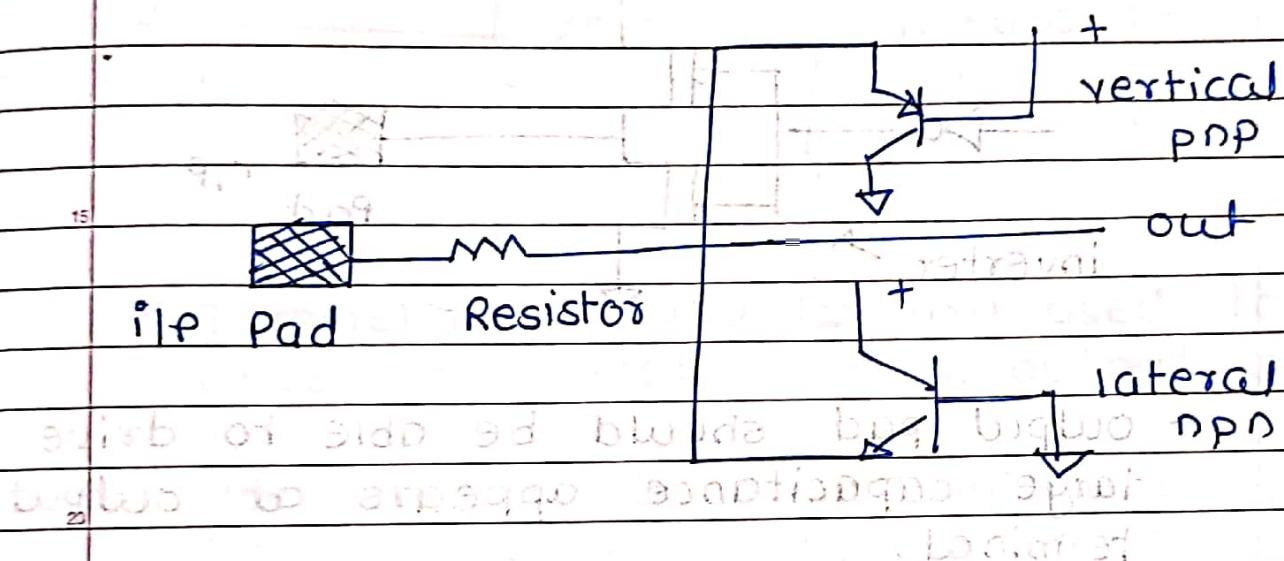
— As Vdd and Vss carry large current, it requires large pads.

— Multiple power pins are used to limit inductive voltage drop.

* Pad Design :- (IO Arch?)

a) Input Pad design

- Main job of input pads is to protect chips internal ckt from static electricity which may damage chip.
- CMOS ckt are sensitive to static discharge because of thin oxide layer used in CMOS.



- At gate input the SiO_2 oxide layer is very thin so we need protective ckt bet "Pad" and "gate" of $\text{X}'\text{stor}$.

- To protect ckt from electro static discharge the ckt is shown above.

- The resistors limits the current caused by vtg spikes.

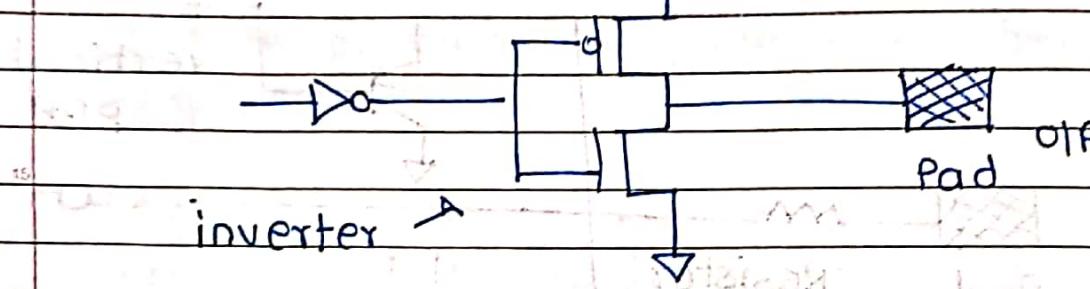
- The vertical p-n-p x'stor is used to protect chip from high +ve voltage

which appear to input pad.

- Similarly, lateral npp x'istor used to protect x'istor from -ve high voltage appears at input pad.

b) Output Pad Design :-

Output pad circuit is shown as,



- Output pad should be able to drive large capacitance appears at output terminal.

- Output pad circuitry consists of chain of inverters to drive up to large off chip load.

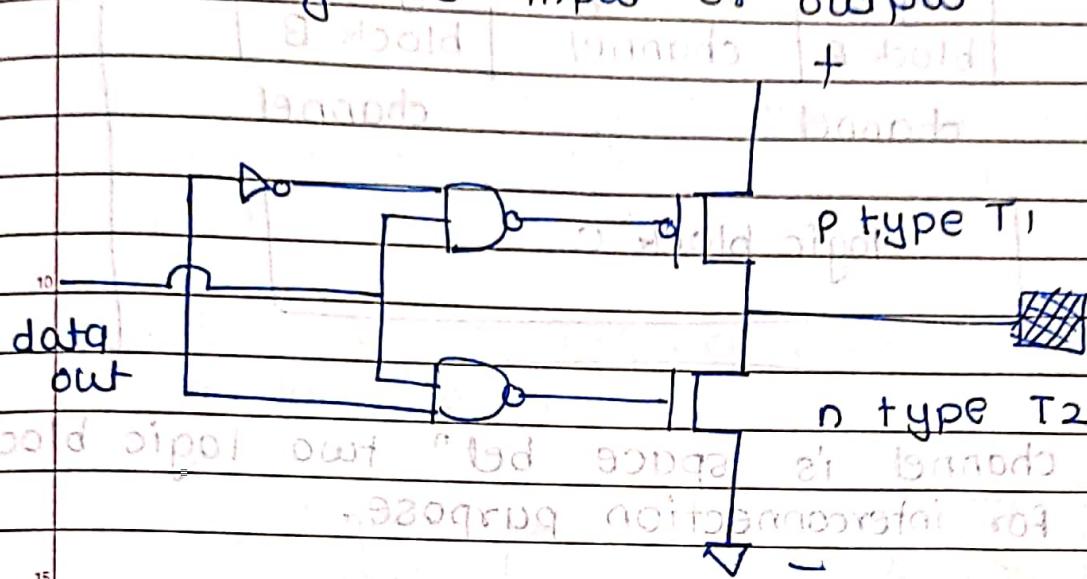
- Output pad circuitry transistors are large in size.

c) Three state Pad design :-

These pad are used as input as well as output pads.

- These pads are used to solve problem of pin count.

- We can not use same pad simultaneously as input or output.



Transistors T_1 and T_2 are used to drive three state pad in output mode.

- when both output transistors are off, the pad can be used as input pad.

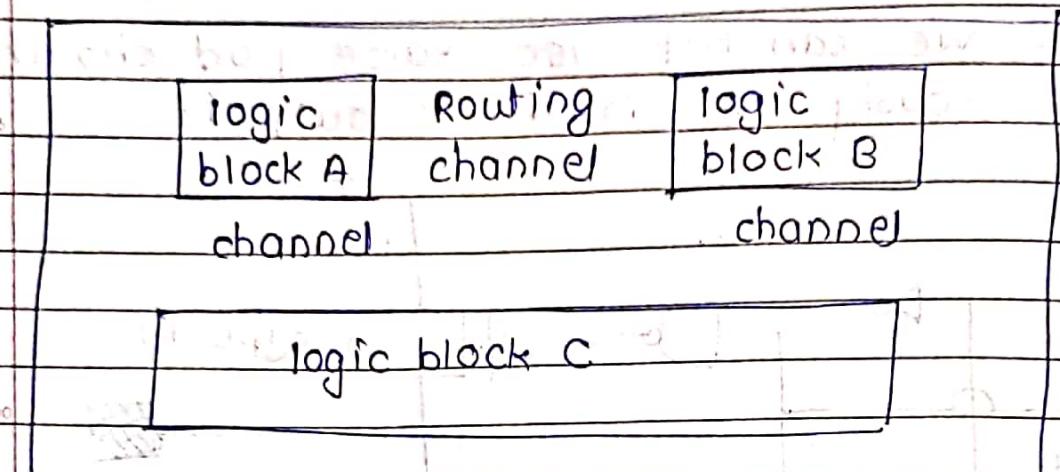
* Interconnect Routing Techniques

Routing makes connection between logic cells

- Global routing determines location of all interconnects and minimized interconnect area.

- Detailed routing completely routes all the interconnects on the chip. It minimizes total interconnect length used.

- local routing joints the cells with interconnects.



- channel is space bet' two logic blocks for interconnection purpose.

- Interconnection routing must be efficient so that it needs low chip area, low interconnect length, or low delay setup time (see more after switchbox routing).

- There are two popular interconnect methods
 - ① Global Routing
 - ② Switchbox Routing.

1) * Global Routing

- Global routing is used for minimization of total interconnect area.

- Optimal routing of single net is much easier than optimal routing of sequence of net.
- for global routing maze routing algo".

is used.

- Maze routing algm find the shortest path for single wire between set of points, if any path exists.
- Points on the grid are iteratively labelled with their distance from source point.

All points at distance 1 from source are labelled with 1.

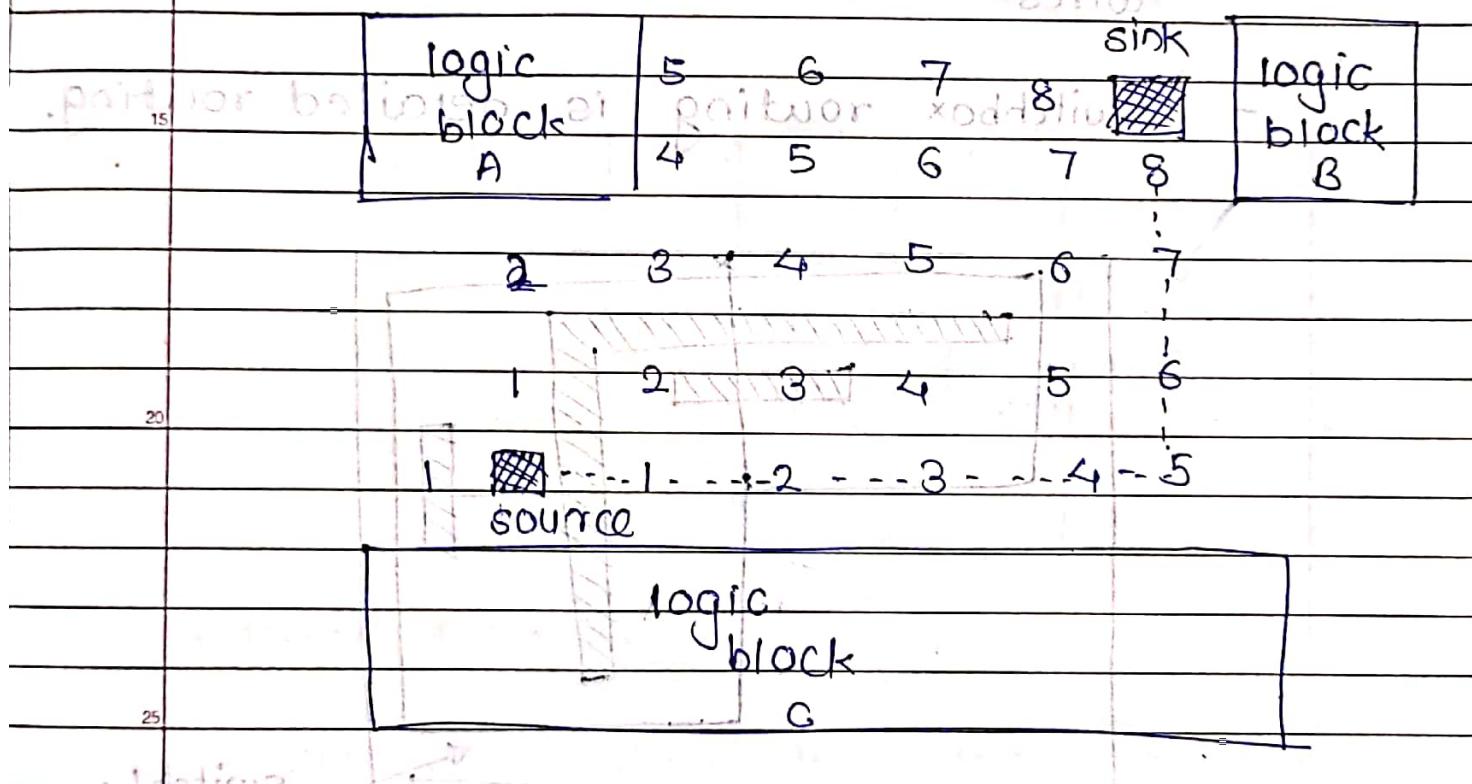


Fig. Maze Routing algm.

In second step all adjacent points to it are labelled as 2 and so on.

- The labeling stops when sink or net to be routed is found.

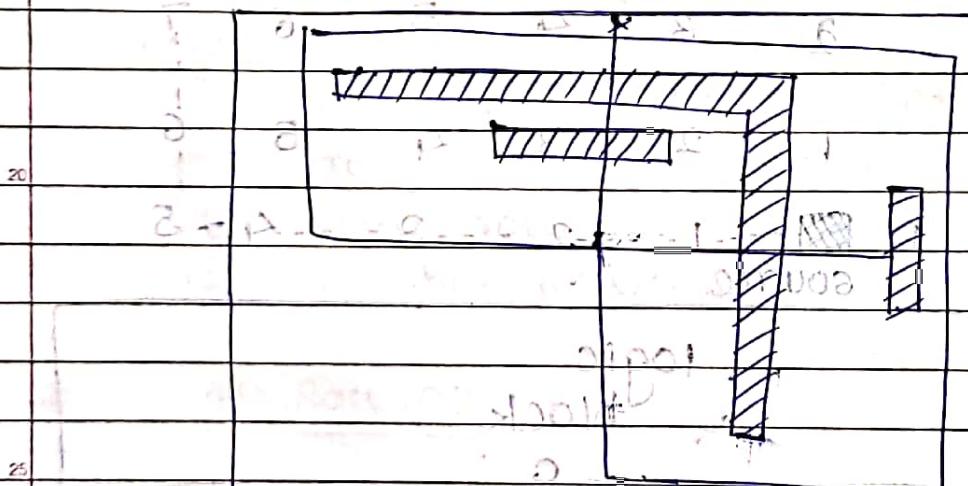
- After that route is traced back from sink to source.

→ Thus the shortest path is found out for net routing.

(2) Switchbox Routing :-

- switchbox routing is harder than channel; because we cannot expand switchbox to make space for more wires.

~~switchbox routing is detailed routing.~~



switchbox formed at intersection of two channels.

→ switchbox is used to route wires betw two intersecting channels.

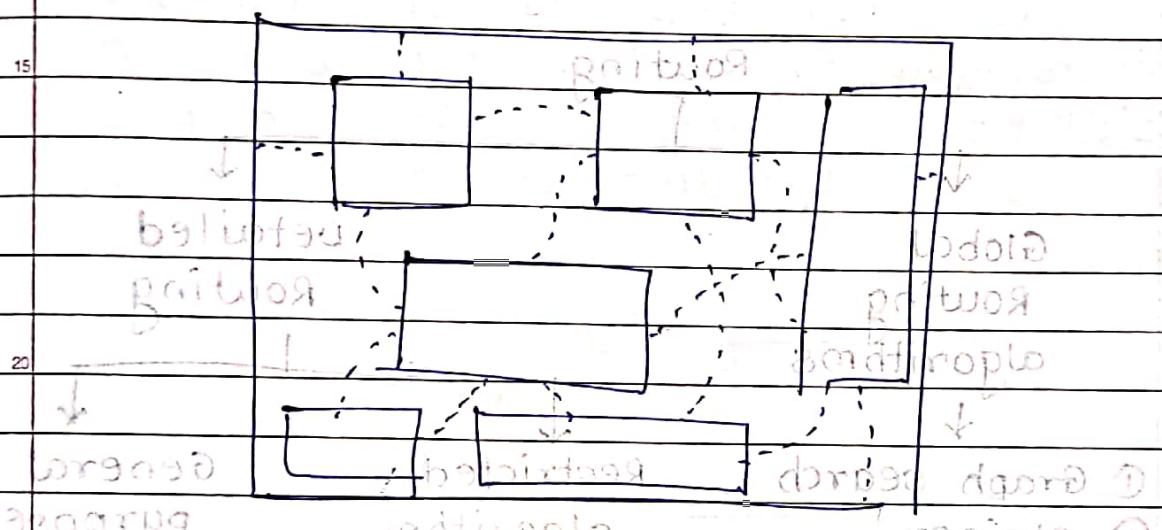
- channel is splitted into two channel,

then route one channel first and route second as switchbox.

- switchbox routing may fail due to added constraints.

* Global Routing

- Global routing has detailed placement with exact terminal locations.
- It determines routing region for each net separately before global routing.
- It minimizes area and time.



* Detailed Routing :-

- Detailed routing determines exact route (and) layers for each net.

- Detailed routing completely routes the interconnects on chip.

- It should have minimum chip area, minimum vias and power.

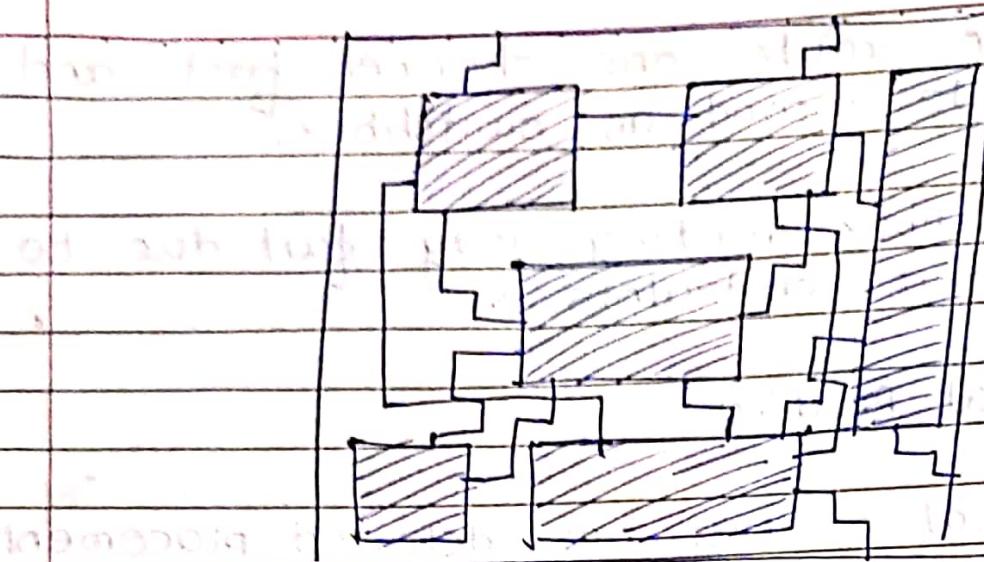
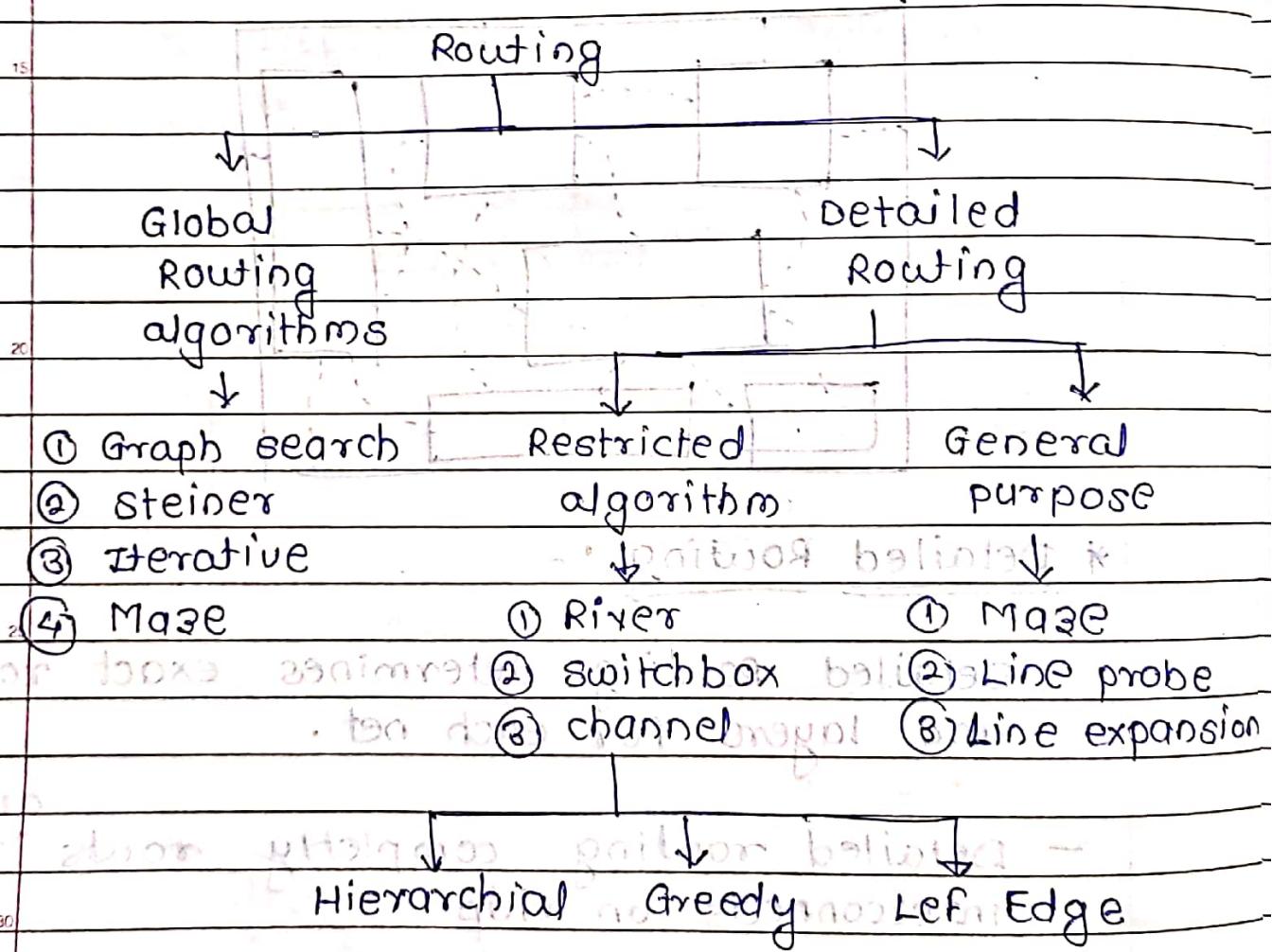


Fig. Detailed Routing

Different types of algorithms are used for routing, no need of algorithm



* Metastability :-

⇒ Metastability is ability of system to persist for an unbounded time in an unequilibrium unstable state or metastable state.

⇒ In metastable state, ckt is unable to switch in to stable 0 or 1 logic level within a time required for circuit operation.

⇒ Example:

Consider SR latch, when both inputs S and R are high i.e. $S=1$ and $R=1$, then Q and \bar{Q} are true state of flip flop/stuck to only one of two stable stages. This condition is called as metastability.

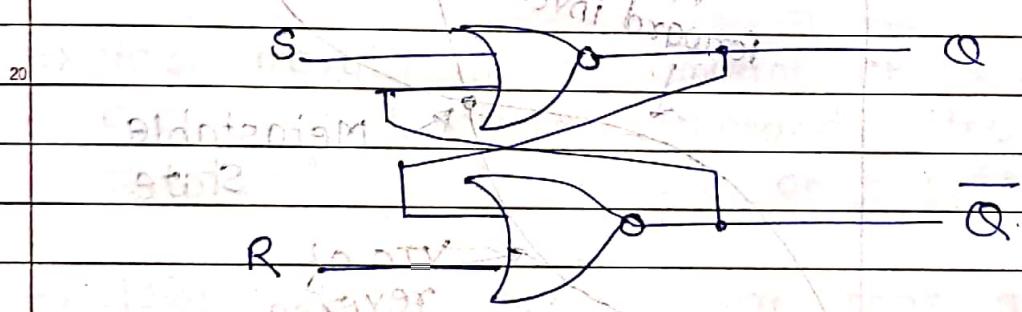


fig. SR flip flop

causes :-

- (1) Metastability may occurs due to violation of set-up and hold time of flip flop
- (2) It may occur due to clock skew resulting due to different path length of clock signal.

③ Slower operating frequency of the peripherals.

④ Asynchronous or rapidly changing inputs.

⇒ Metastable condition in D latch with two inverter.

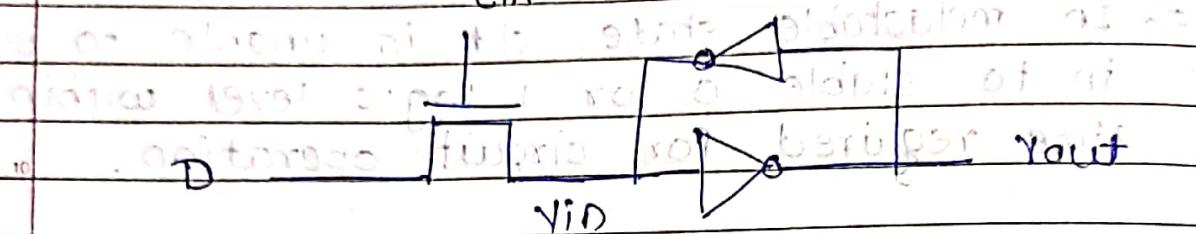
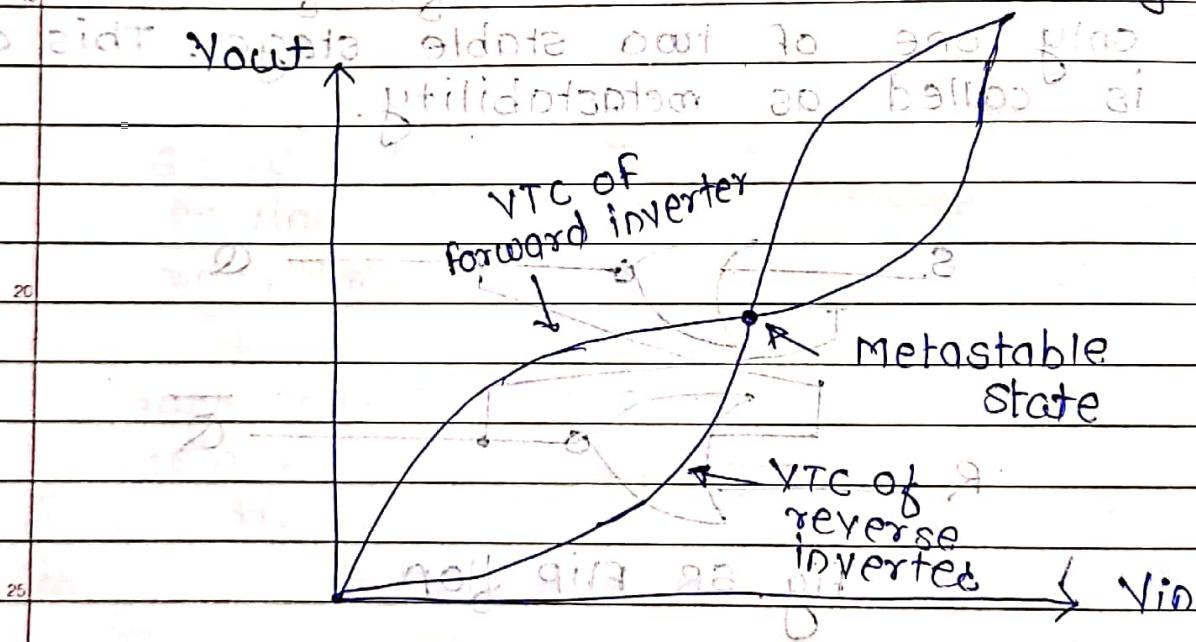


fig. simple D latch.

qui need to be called VTC

voltage transfer characteristic of forward and reverse inverter are shown in fig.



⇒ probability of flip flop being metastable

is less than latches as flip flops are edge sensitive and latches are level sensitive.

At the transition of sub threshold

transition state to normal

⇒ Metastability in digital system occurs when two asynchronous signals combines in such a way that their resulting output goes to an intermediate state.

* Metastability Reduction :-

Metastability can be reduced by,

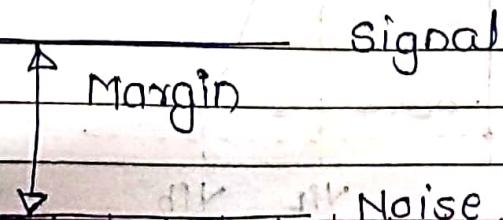
- ① using synchronizers
- ② using fast flip flops
- ③ cascading flip flops in synchronizers
- ④ reducing sampling rates
- ⑤ Avoiding input with low dv/dt
- ⑥ Avoid asynchronous inputs
- ⑦ Reducing clock skew

* Noise Margin :-

⇒ Noise margin is the amount of noise that a CMOS circuit could withstand without compressing the output of circuit.

⇒ Noise margin makes sure that any signal with logic 1 with finite logic noise added to it, is still recognized as logic 1 not 0.

⇒ Noise margin is basically difference between signal value and noise value.



\Rightarrow Noise margin is closely related to input output voltage characteristics. This parameter allows us to determine the allowable noise voltage on input of gate so that output will not be affected.

\Rightarrow There are two types of noise margin,

- ① Low noise margin
- ② High noise margin

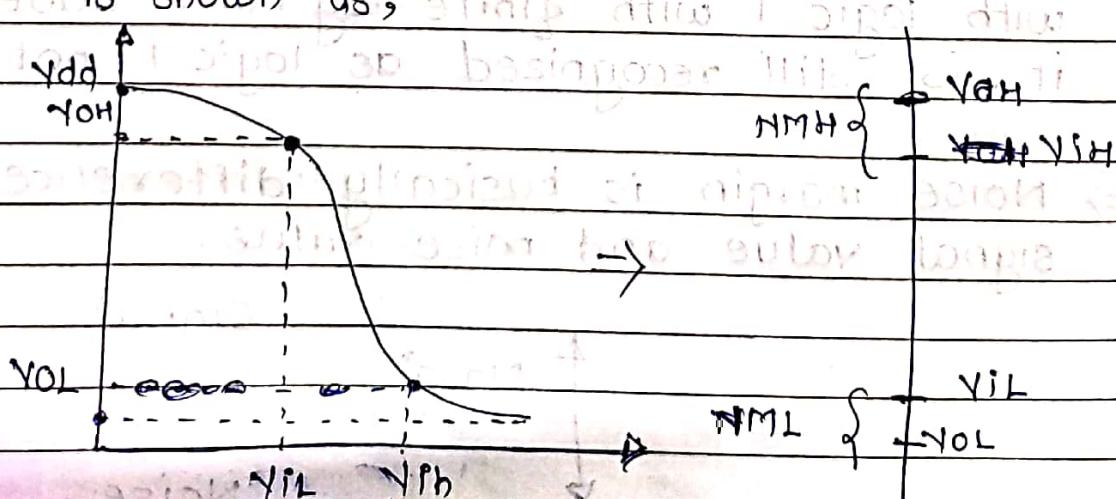
\Rightarrow Low noise margin (NML) is diff bet max low output voltage of driving gate and minimum input low voltage used to drive gate.

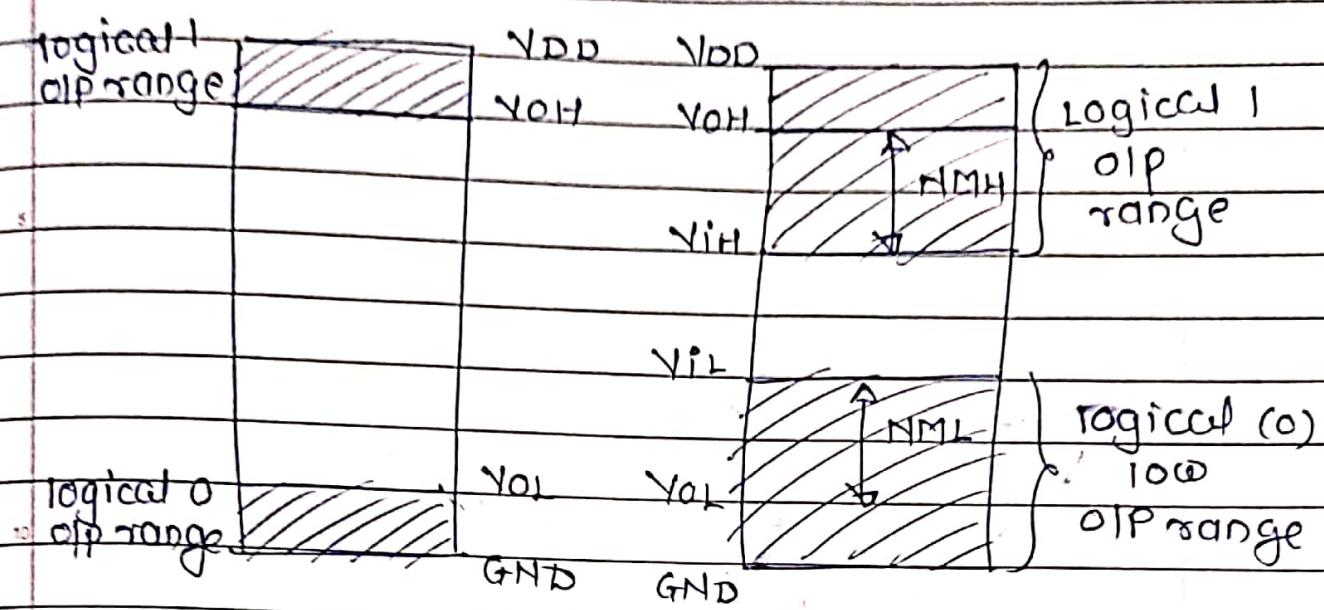
$$NML = V_{IL} - V_{OL}$$

\Rightarrow High noise margin (NMH) is diff bet minimum high output voltage of driving gate and minimum input high voltage used to drive gate.

$$NMH = V_{OH} - V_{IH}$$

\Rightarrow Output characteristic of inverter with noise margin





output characteristics

fig. 1010 and high noise margins.