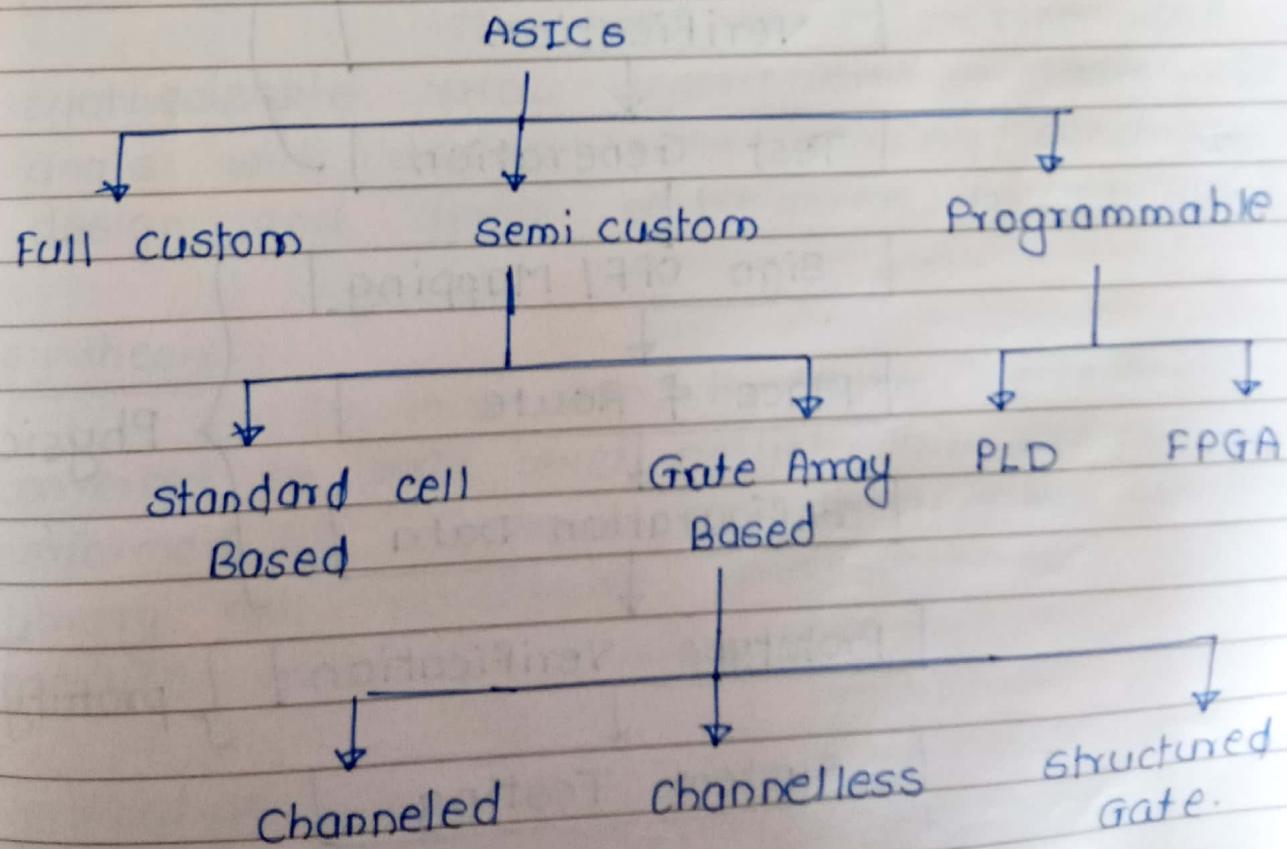


Unit 4: Application Specific Integrated Circuits

Any IC other than general purpose IC which contain functionality of thousands of gates is usually called as Application specific Integrated Circuits.

ASIC are designed to fit certain application. An ASIC is digital or mixed signal circuit designed to meet specification set by specific project.

The classification of ASIC is shown below



* ASIC Design Flow :-

ASIC design flow is given as,

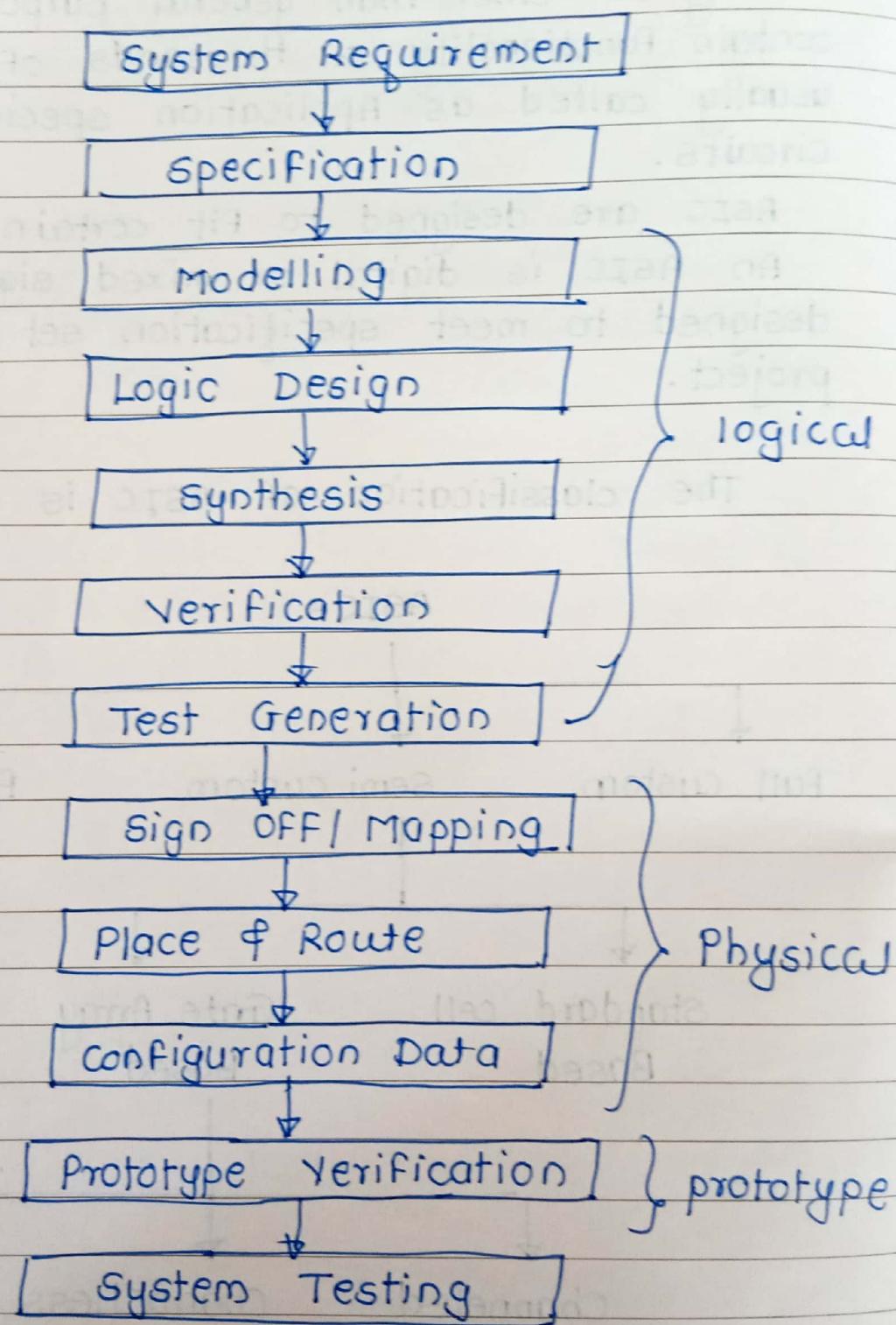


Fig. ASIC design flow

ASIC specification :-

The goal of ASIC specification is to specify functional requirements for design and define the external interfaces to related designs.

ASIC Modelling :-

The goal is to build simulatable VHDL model corresponding to specification. The function of model is verified using VHDL test bench.

Logic Design :-

The goal is to write the synthesizable VHDL description of design. It deals with design rules, reusing, synchronous design and design partitioning in RTL block.

Synthesis :-

In this step, hardware description is converted to gate level netlist. This process is performed by synthesis tool that takes standard library cell, constraint and RTL code and produce gatelevel netlist.

Verification :-

In this step, test benches and run simulations to verify functionality. This gives assertion based verification and automated test bench generation.

Test Generation :-

It consists of insertion of various designs for testability (DFT) to perform device testing using automated test equipment and system level test. Automatic test pattern generator tool generates test vector to perform logic and parameter testing. This consists of built-in self test and boundary scan module.

Place and Route :-

Manually place major modules in chip depending on connection with other modules. Standard cell rows are defined next and gates are placed. Timing driven placement tries to minimize delay on critical path.

Prototype verification :-

Final verification is done with engineering samples.

Physical measurements done in prototype testing are -

- parametric DC test
- parametric AC test
- functional test
- power consumption
- Thermal Test

* Cell Design Specification :-

- ⇒ An electronics functional unit normally defined in terms of its layout on silicon.
- ⇒ Similar to PCB components, ASIC vendors have libraries build of core cells of specific technology ie. 0.5 μ, 0.25 μ or 0.18 μ
- Each cell in ASIC cell library must contain following,
 - ① A physical layout
 - ② A behavioral model
 - ③ A verilog / VHDL model
 - ④ detailed timing model
 - ⑤ Test strategy
 - ⑥ circuit schematic
 - ⑦ cell icon
 - ⑧ wire load model
 - ⑨ routing model
- cell design specification must consist of following aspects
 - ① The cell used in hard IP or in soft IP
 - ② Function of cell
 - ③ Performance of cell
 - ④ Power consumption
 - ⑤ process features
- Physical design of cell is considered by placement and routing.
- cell design is mainly created to automate the design of ASIC.

- The cost of cell design if exceed that of cost of cell manufacturing then design trade off between area and lower design cost is considered.

* SPICE Simulation :-

- Simulation program in integrated circuit emphasis (SPICE) is general purpose, open source analog electronics circuit simulator.
- It is a program used in integrated circuit and board level design to check integrity of circuit design and predict the circuit behaviour.
- Using SPICE we can do following analysis ,
 - ① AC analysis
 - ② DC analysis
 - ③ DC transfer curve analysis
 - ④ Noise analysis
 - ⑤ Transfer function analysis
 - ⑥ Transient analysis
- SPICE simulation uses SPICE model and netlist.
- Netlist defines how pins are connected in your schematic.
- Model contain text descriptor of component values which can be used for the SPICE simulation.

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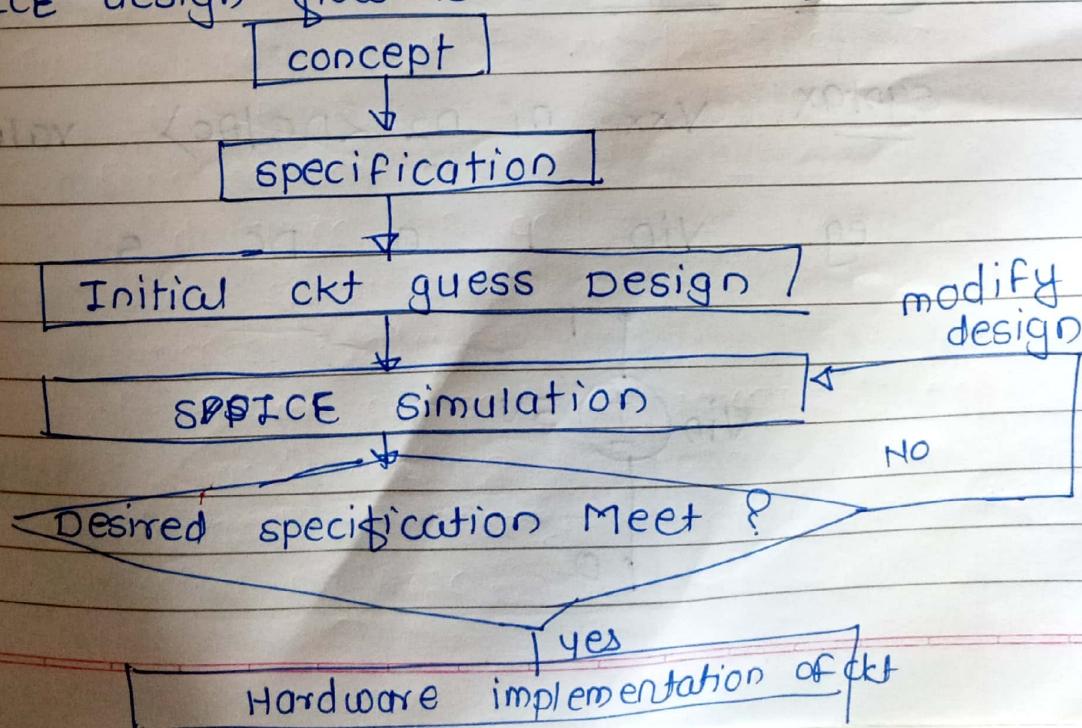
- Different circuit elements used in SPICE program are

- ① Resistor
- ② capacitors
- ③ Inductors
- ④ Dependent current & voltage sources
- ⑤ Independent current & voltage sources
- ⑥ switches
- ⑦ Active devices such as diodes, BJT, JFET, MOSFET etc.

- SPICE program file consists of

- ① title
- ② Parameter
- ③ circuit description
- ④ Inputs
- ⑤ Analysis
- ⑥ output
- ⑦ model

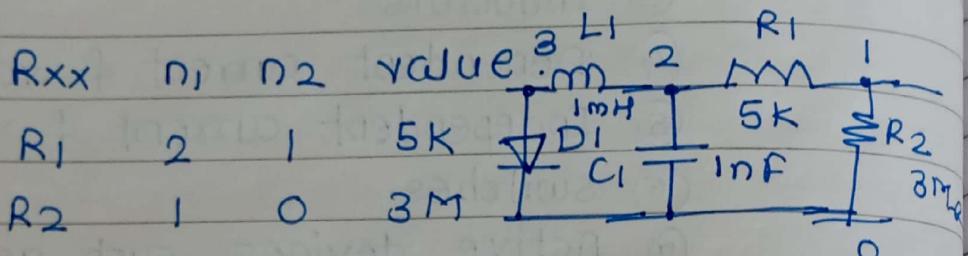
- SPICE design flow is shown as,



* syntax of circuit Elements in SPICE :-

① Resistor

syntax



② capacitor

syntax :- C_{xx} n₁ n₂ value

eg. C₁ 2 0 10

③ Inductor

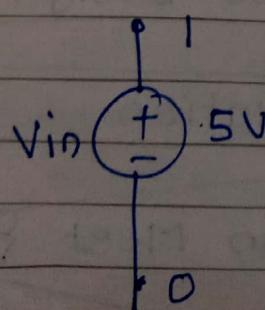
syntax : L_{xx} n₁ n₂ value

eg. L₁ 3 2 1m

④ Voltage source

syntax V_{xx} n₁ n₂ <DC/Ac> value

eg. Vin 1 0 DC 5



current source

syntax :- $I_{xx} \ n_1 \ n_2 \ \langle DC/AC \rangle \ value$

voltage controlled voltage source :-

VCVS: $E_{xx} \ n_1 \ n_2 \ n_{c1} \ n_{c2} \ value$

voltage controlled current source

VCCS: $G_{xx} \ n_1 \ n_2 \ n_{c1} \ n_{c2} \ value$

current controlled current source

CCCS: $F_{xx} \ n_1 \ n_2 \ n_{c1} \ n_{c2} \ value$

current controlled current source

CCVS: $H_{xx} \ n_1 \ n_2 \ n_{c1} \ n_{c2} \ value$

Diode

D_{xx} $n_1 \ n_2 \ \langle Model\ Name \rangle$

BJT

Q_{xx} $n_c \ n_b \ n_e \ \langle Model\ Name \rangle$

MOSFET

M_{xx} $n_d, n_g, n_s \ n_b \ \langle Model\ Name \rangle$

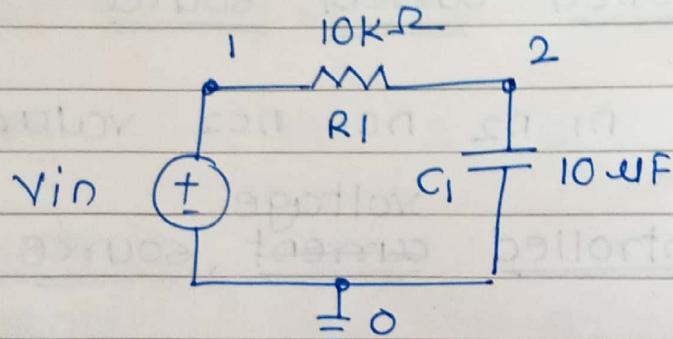
output

- print type OY₁ OY₂
- plot type OY₁ OY₂

* AC Analysis:-

AC analysis is used to calculate small signal response of circuit. In ac analysis, DC operating points are first calculated to obtain linear, small signal model of all non-linear components. Then the equivalent circuit is analyzed from start to stop frequency. The result of AC analysis is displayed in two parts a) gain vs frequency
b) phase vs frequency

eg.



SPICE code

```

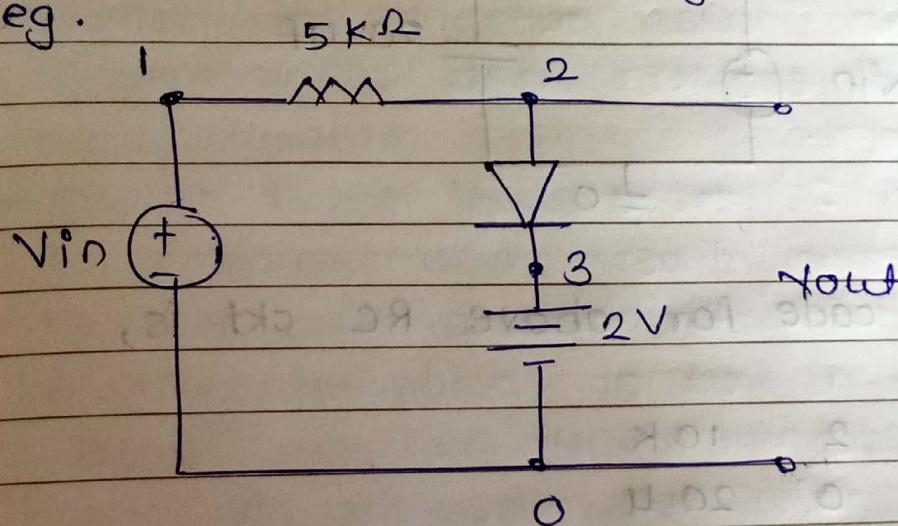
R1 1 2 10K
C1 2 0 10u
Vin 1 0 dc 0 ac 1
  ac dec 10 1 1meg
  control
  run
  plot v1b(2) xlog
  endc
  end
    
```

* DC Analysis :-

DC analysis of SPICE finds dc operating points of circuit.

DC operating point analysis calculates the behaviour of circuit when dc voltage or current is applied to it. The result of this analysis is generally referred as the bias points or quiescent points. In most cases DC analysis results are intermediate values for further analysis.

e.g.



SPICE code for dc analysis of above ckt is,

```

 $\Rightarrow$  RI 1 2 5K
DI 2 3
Vdc 3 0 dc 2
ViD 1 0 dc
•dc Vin -5 5 0.01

```

•control

•run

plot $V(2)$ vs $V(1)$

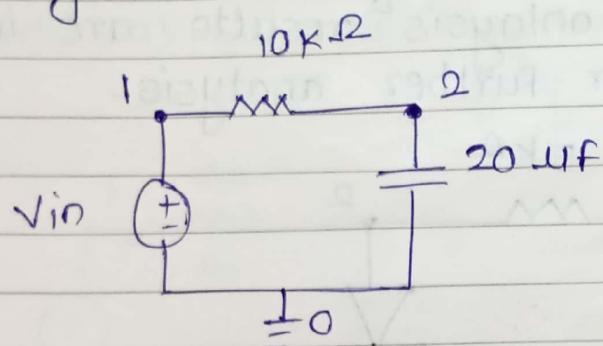
•endc

•end

* Transient Analysis :-

In transient analysis, PSIM computes the circuit response as function of time. This analysis divides the time into segments and calculate the voltage and current levels for each given interval. Finally the results voltage vs time are presented graphically.

e.g.



SPICE code for above RC ckt is,

R1 1 2 10K

C1 2 0 20uF

Vin 1 0 Pwl(0 0 1ms 0 2ms 5V 10ms 5V)

- trans 0.01ms 10ms

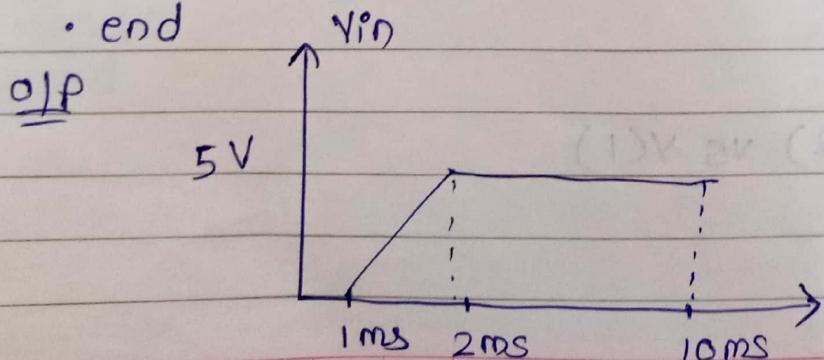
- control

- run

- plot V(1) V(2)

- end c

- end



* Noise Analysis :-

Noise analysis calculates the noise contribution from each resistor and semiconductor devices at a specified output node.

This analysis computes the input noise of circuit equivalent to output referred noise.

* Design Rule check (DRC)

- The design rule checks that all polygons & layers from the layout database meet all the manufacturing process rule.

- Design rules defines the limit of a manufacturable design.
- Design rules tends to differ from company to company and from process to process due to this porting of different technologies & existing technology is time consuming task.
- There are two types of design rules.

- ① λ based rules
- ② micron rules

- Lambda rules are scalable rules and function of single parameter i.e. λ .
- As circuit density is prime goal in industry most semiconductor industries uses micron rules.
- for given process λ is set to specific value and all design dimensions are translated in to absolute numbers.
- In micron design rule scaling & porting design betw diff technologies can be done using CAD tools.

* Need of Layout Design Rules:-

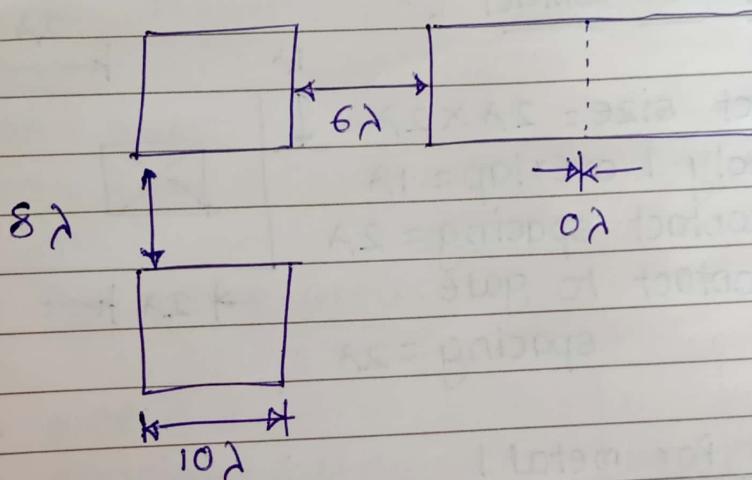
- ① Layout design rules provides necessary guidelines for constructing various masks needed for fabrication process.
- ② It provides guidelines about minimum width, length and minimum spacing requirements betⁿ diff. objects.
- ③ Layout design rules are used to translate a circuit concept in to an actual geometry in silicon.
- ④ Design rules are media between the circuit engineer and IC fabrication engineer.
- ⑤ For an IC process λ is set to value and design dimensions are converted in the forms of numbers.
- ⑥ Scaling is easier and function of single parameter λ .
- ⑦ Design rules are necessary to avoid -
 - a) crosstalk
 - b) noise
 - c) clock skew
 - d) clock jitter
 - e) power optimization
 - f) timing optimization
- ⑧ Design rules also avoid following problems -
 - a) photo resist shrinkage & tearing.
 - b) variation in material deposition, temperature and oxide thickness.
 - c) Impurities
 - d) variations across wafers.

λ Rules :- (Lambda Rules)

* λ Rules are scalable design rules.

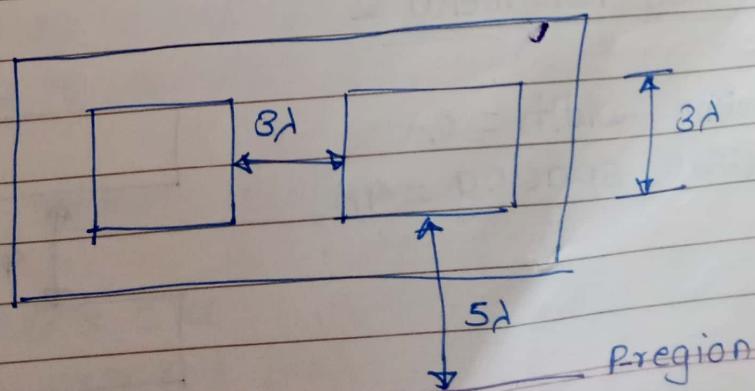
A] Rules for N-well

- ① Maximum width = 10λ
- ② Spacing between well of same potential = 6λ
- ③ Well of different types, spacing = 8λ
- ④ Wells at same potential with spacing = 6λ



B] Rules for Active Area

- ① Max width = 3λ
- ② Max spacing = 3λ
- ③ source/drain active to well edge = 5λ
- ④ substrate/well contact to well edge = 3λ



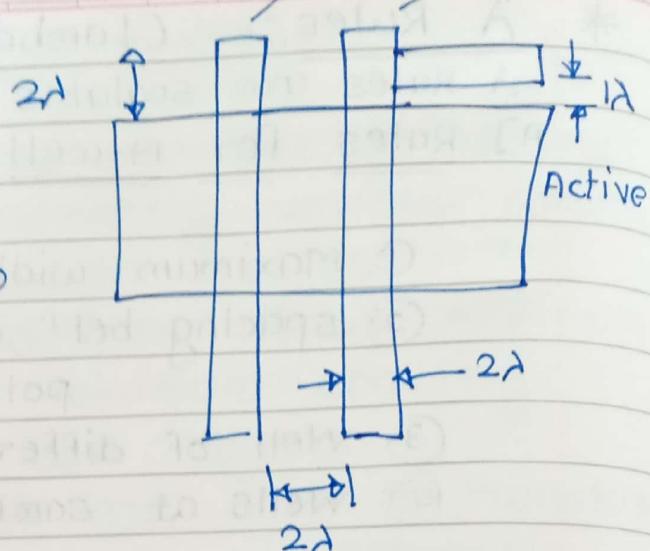
③ Rules for poly1 :-

Max width = 2λ

Min spacing = 2λ

Min gate extension to active = 2λ

Min field poly to active = 1λ



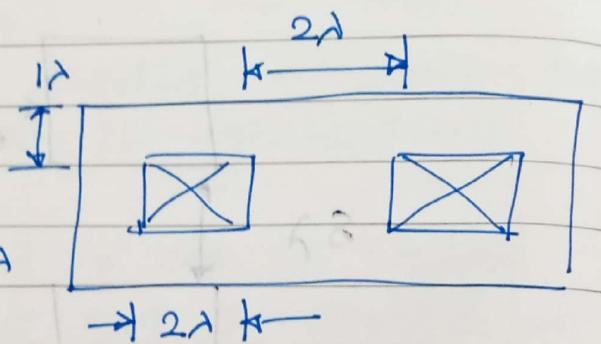
④ Rules for contact :-

Contact size = $2\lambda \times 2\lambda$

Min poly1 overlap = 1λ

Min contact spacing = 2λ

Min contact to gate spacing = 2λ



⑤ Rules for metal1

Min width = 3λ

Min spacing = 3λ

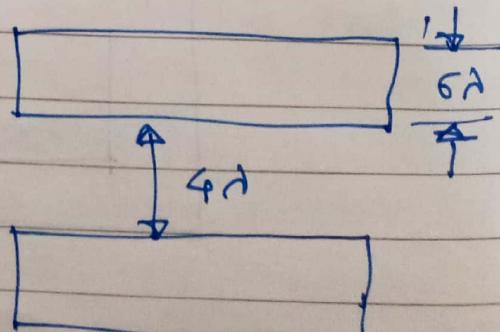
Min overlap to poly contact = 1λ

Min overlap to active contact = 1λ

⑥ Rules for metal2

Min width = 6λ

Min spacing = 4λ



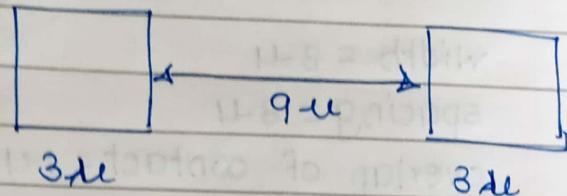
* Micron Rules:

- Micron rules are stated at micron resolution.
- Micron rule consider absolute dimensions.
- All min sizes and spacing are specified in micron.
- Rules don't have to be multiple of λ .
- Can result in 50% reduction in area over λ based rules. \therefore standard in industry.

① Rules for N well

Width = 3- μ

space = 9- μ

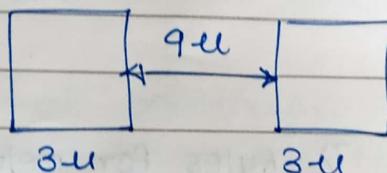


② Rules for active area

Min size = 3- μ

Min spacing = 3- μ

N+ active to N well = 7- μ



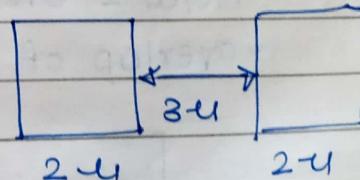
③ Rules for polysilicon

width = 2- μ

spacing = 3- μ

Gate overlap to active = 2- μ

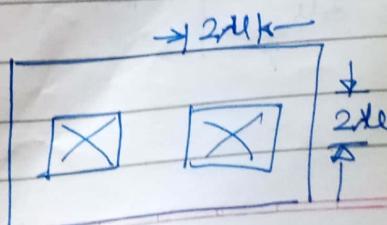
Field poly to active = 1- μ



④ Rules for contact to poly

size = 2- μ x 2- μ

Min poly overlap = 1- μ



Min contact spacing = 2-u

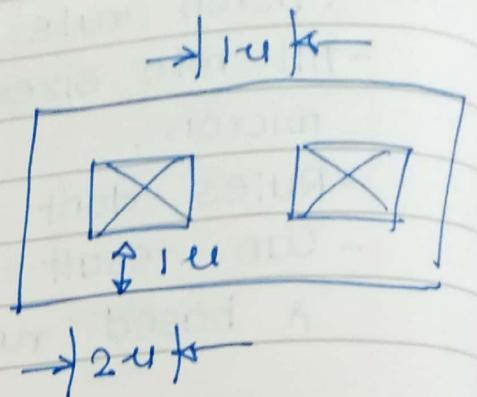
5) Rules for contact to active

contact size = $2\text{-u} \times 2\text{-u}$

Min active overlap = 1-u

Min contact spacing = 2-u

Min spacing to gate = 2-u



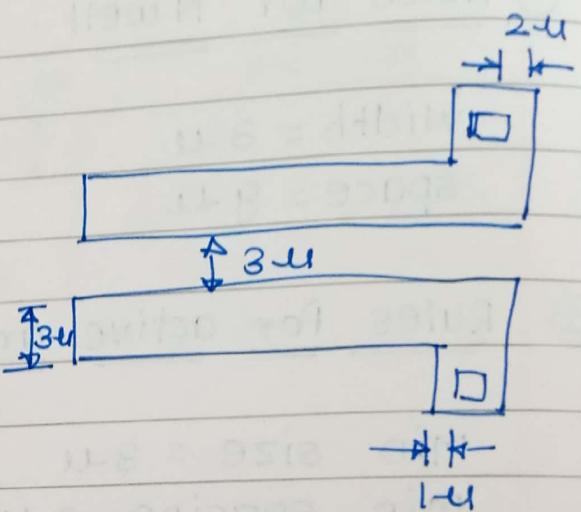
6) Rules for metal 1

width = 3-u

spacing = 3-u

overlap of contact = 1-u

overlap of via = 2-u



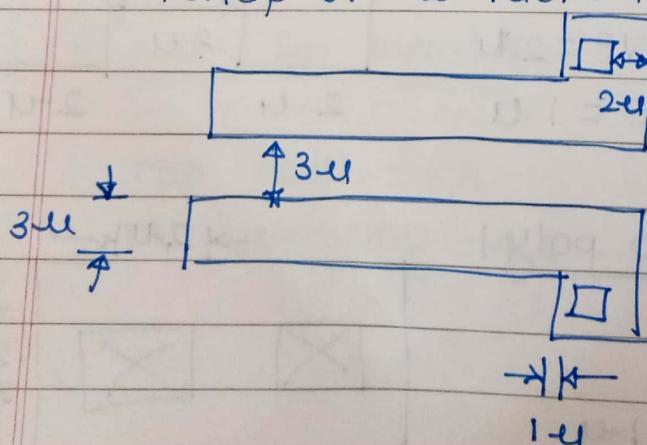
7) Rules for metal 2

width = 3-u

space = 3-u

Metal 2 overlap via = 2-u

overlap of contact = 1-u



* stick diagram for cell layout

In cell layout major steps consists of -

- ① wire planning before cell layout
 - assign direction to each layer
 - group pmos and nmos
 - fix input and output port location
 - power, ground, clock wire must be wide
- ② cell pitch determination
 - height of tallest cell
 - No of over the cells
 - wire length

Stick diagram

- VLSI design aims to translate circuit concept on silicon.
- Stick diagram are means of capturing topography and layer information using the simple diagram.
- Stick diagram convey "layer info" through color code or monochrome encoding.
- Stick diagram act as interface b/w the symbolic circuit and actual layout.
- It shows all component / vias.
- It shows relative placement of component.
- It helps to plan layout and routing.
- A stick diagram is a cartoon of a layout.

- Stick diagram does not show
 - exact placement of component
 - transistor sizing
 - wire length, wire width, tub boundaries
 - parasitics information.

stick diagram notation

Metal 1

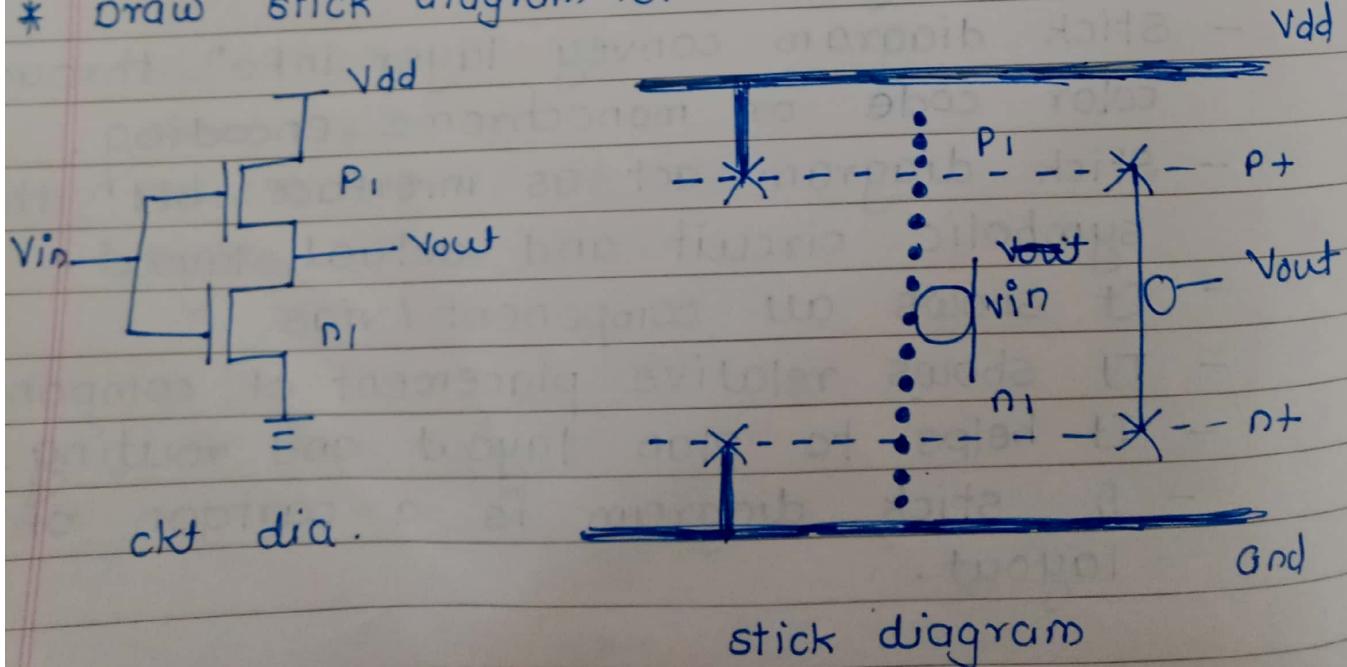
 metal 2

 - - - - - Active pt or nt
 poly

X contact

O via

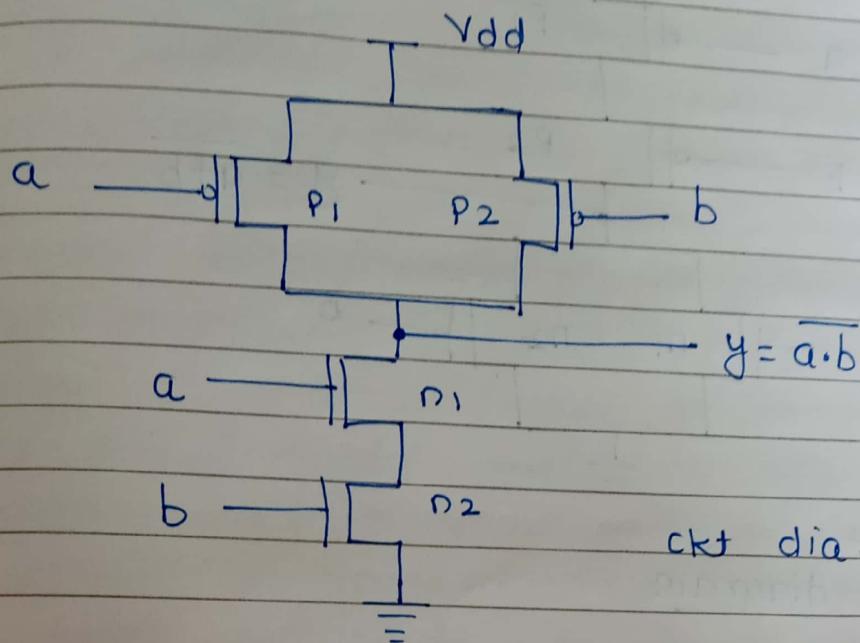
* Draw stick diagram for inverter.



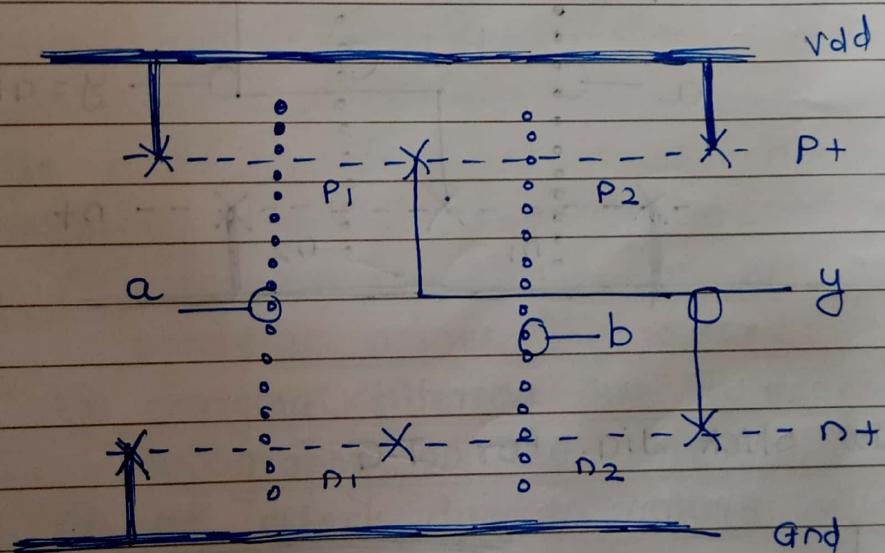
* Draw stick diagram for 2 i/p NAND gate.

$$y = \overline{a \cdot b} = \overline{a} + \overline{b}$$

\Rightarrow



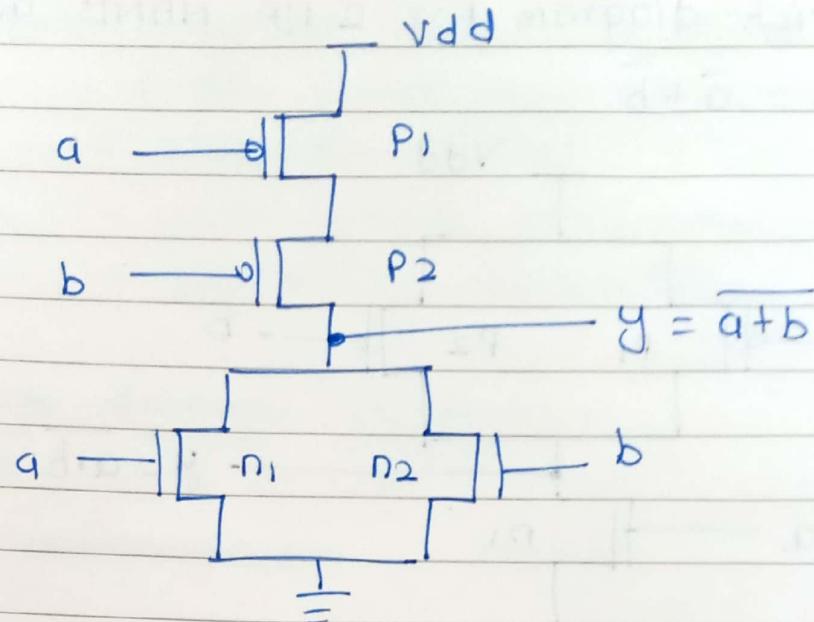
stick diagram



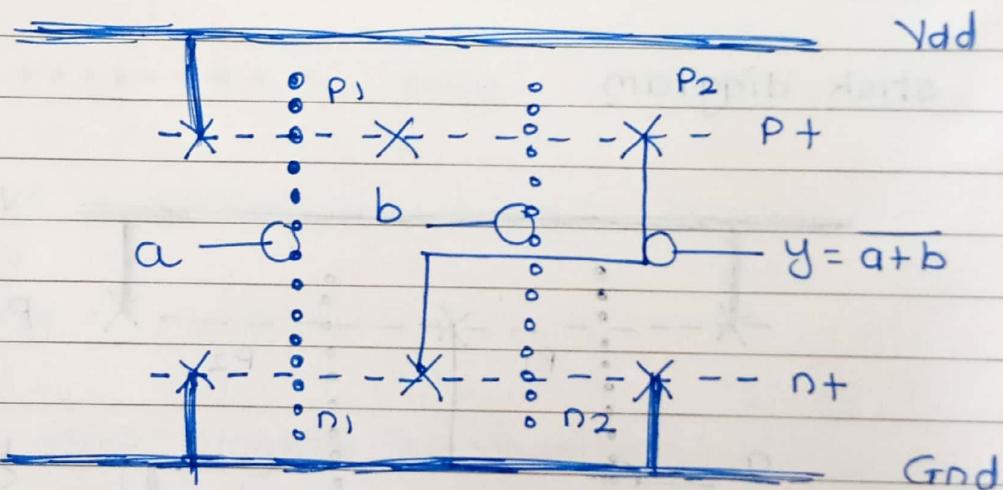
* Draw stick dia. for 2 i/p NOR gate.

$$y = \overline{a+b}$$

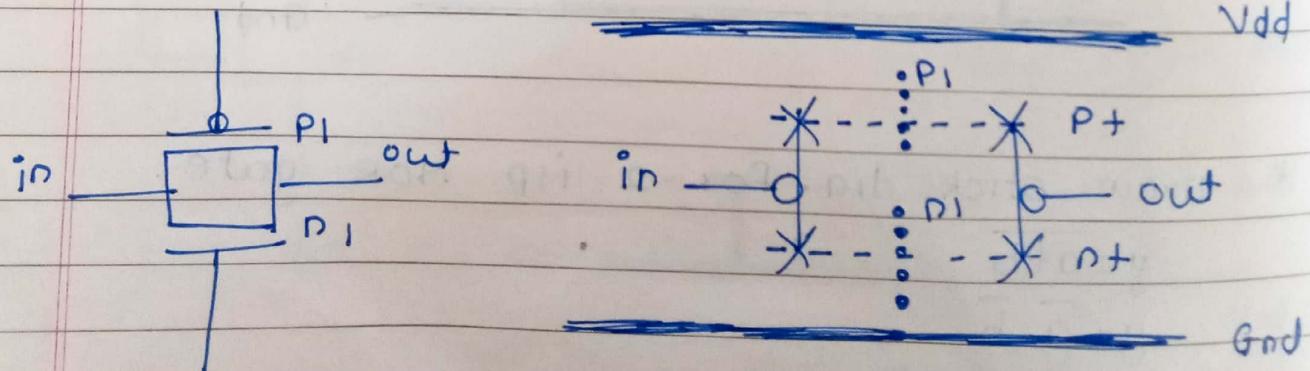
$$y = \overline{\overline{a} \cdot \overline{b}}$$



Stick diagram



* Draw stick dia. for T-G



* Draw stick dia for 3 input NAND and NOR gate.

* Design Issues *

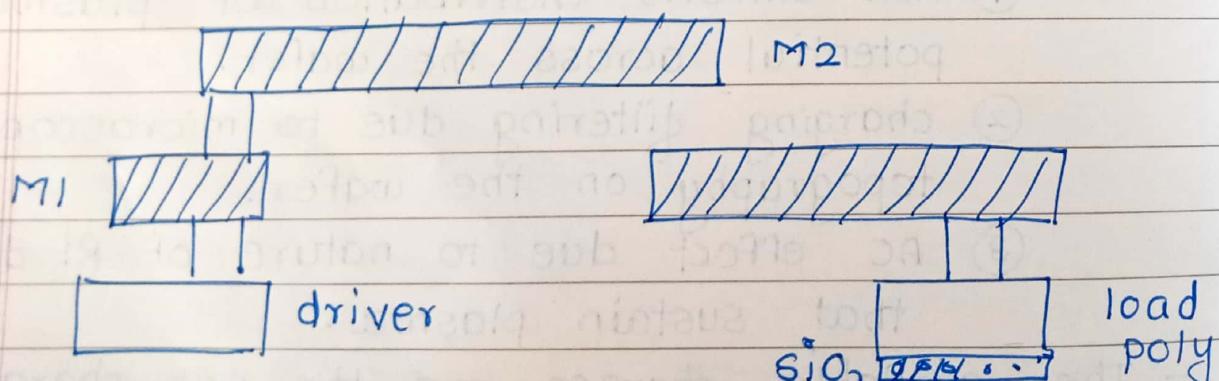
(1) Antenna Effect :-

- Modern wafer processing uses plasma etch. Plasma is an ionized gas used to etch.
- It allows super control of pattern and several chemical reactions that are not possible in traditional wet etch. Also plasma consists of charging damage which is unwanted.
- Plasma charging refers to unintended high field stressing of gate oxide in MOSFET during plasma processing.
- The stress voltage that develops across the gate and substrate of MOSFET during plasma processing mainly comes from -
 - (1) Non uniform distribution of plasma potential across the wafer.
 - (2) charging filtering due to microscopic topography on the wafer.
 - (3) AC effect due to nature of RF discharge that sustain plasma.
- The available charges are the net charges collected from plasma by exposed conductor with connection to gate or substrate.
- size of conductor exposed to plasma plays a role in determining the magnitude of

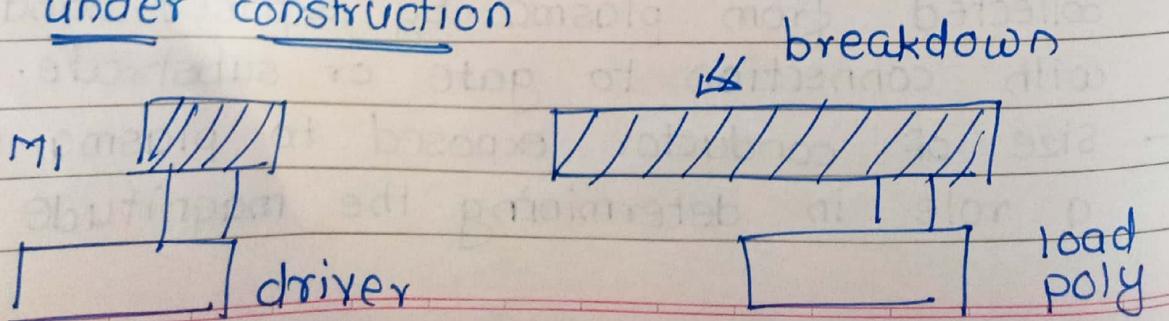
net charge collection rate and therefore tunneling current. This is called as antenna effect.

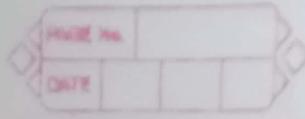
- The area ratio of conductor to oxide under gate is antenna ratio.
- Antenna effect occurs during manufacturing process. During metallization some wires connected to polysilicon gate of 'stor can be left floating until the upper metal layers are deposited.
- Such long floating interconnects act as temporary capacitors, collecting charges during fabrication process, such as plasma etching.
- If the energy built up on floating node is suddenly discharged, the logic gate might suffer permanent damage due to transistor gate oxide breakdown.

After completion



under construction





Reduction of Antenna effect :-

- ① change the order of routing layers. If the gate immediately connect to highest metal layer, no antenna violation will normally occur.
- ② Add vias near the gate, to connect the gate to highest layer used. This add more vias, but involves fewer changes to rest of the net.
- ③ connect diodes to those layers with antenna violations.

* Electro-Migration Effect :-

- Electromigration is gradual displacement of metal atoms in semiconductor.
- It occurs when current density is high enough to cause the drift of metal ions in the direction of electron flow and is characterized by ion flux density.
- This density depends upon magnitude of forces that tends to hold the ions in place ie. the nature of conductor, crystal size, interface and grain boundary chemistry and the magnitude of forces including current density, temperature & mechanical stresses.
- Excessive current density within interconnect which if not effectively mitigated causes electromigration.

- Electromigration is physical design issue.
- Due to high electric fields, fast moving electron knocks off ion forming the metallic interconnect thereby eroding the interconnect.
- As technology nodes keeps getting smaller, EM is becoming a physical roadblock in scaling of interconnect.

Reduction of EM

- 1) Increasing the metal width to reduce current density is typically solution.
- 2) For a via EM violation, you can increase the no of vias to fix potential EM issue.
- 3) Additional straps for current density.
- 4) Layer switching is another option, typically upper layers in technology have higher current driving capacity.

* Crosstalk :-

"switching of signal in one net can interface neighbouring net due to cross coupling capacitance is called as crosstalk."

- crosstalk may lead setup & hold violation.
- crosstalk is shown as,

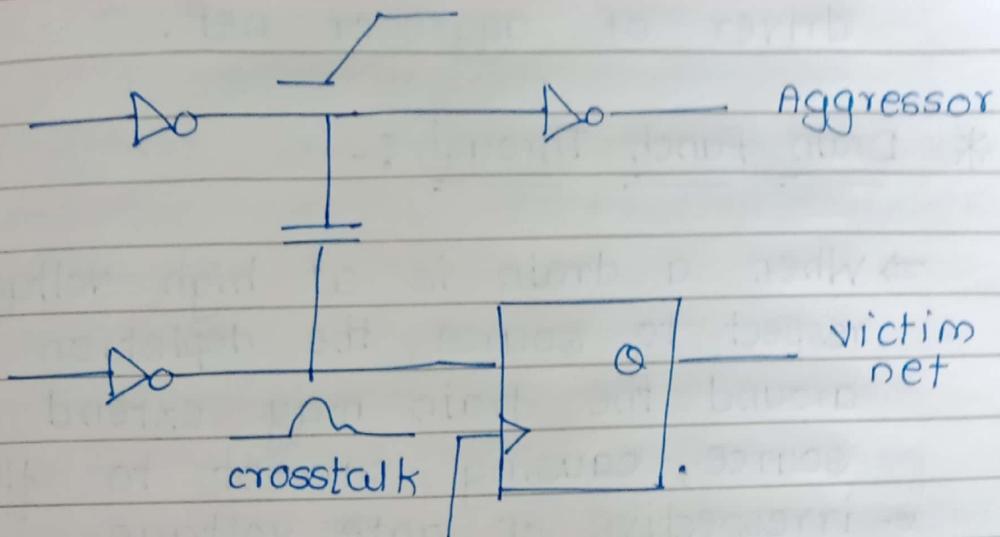


Fig. crosstalk

- Due to process, technology scaling, the spaces betⁿ adjacent interconnect wires keeps shrinking, which leads to an increase in the amount of coupling capacitances betⁿ interconnect wires.
- Crosstalk has two effects
 - ① crosstalk delay
 - ② crosstalk noise
- IF two adjacent wires are switching in opposite direction it will slow down signal hence violating set up times.
- IF two nets are switching in same direction it will aid timing, this is called as crosstalk delay.

Minimizing crosstalk :-

- 1) shielding of victim net by VDD/VSS line.
- 2) Add buffer on victim net.
- 3) increase spacing betⁿ two nets.
- 4) Upsize driver of victim net or downsize

driver of aggressor net.

* Drain Punch Through :-

⇒ When a drain is at high voltage with respect to source, the depletion region around the drain may extend to the source, causing current to flow

→ irrespective of gate voltage.

i.e. even if gate voltage is zero.

This is known as drain punch through condition and the punch through voltage V_{PT} is given by,

$$V_{PT} = \frac{q \cdot N_a \cdot L^2}{2\epsilon}$$

where,

L = channel length

N_a = doping concentration

q = charge

⇒ When channel length L decreases, punch through voltage V_{PT} rapidly decreases.

⇒ Simple way to reduce punchthrough effect is to increase overall bulk doping level. As a result drain and source depletion region will becomes smaller and will not establish a parasitic current path.

⇒ Drain punchthrough can be avoided using
a) delta doping

b) halo implant

c) pocket implant

⇒ The actual amount of current depends mainly on potential distributions under the channel.

⇒ Punchthrough voltage highly depends on applied drain voltage and on the source drain junction depths.

⇒ Punchthrough effect is highly undesirable as it increases output conductance and limit the maximum operating voltage of device.

* Timing Analysis :-

- Timing analysis is used to verify whether ckt meets all its timing requirements.
- There are three types of design constraint
 - ① time
 - ② power
 - ③ area
- During designing there is trade off betⁿ speed, area, power and time according to constraint set by designer.
- We want to make sure that circuit is properly designed and can work properly for all combinations of component over the entire specified operating environment every time.
- Timing analysis is integral part of VLSI design.

- There are two types of timing analysis.

a) Static timing analysis :-

It checks static delay requirements of circuit without any input or output vector.

b) Dynamic timing analysis :-

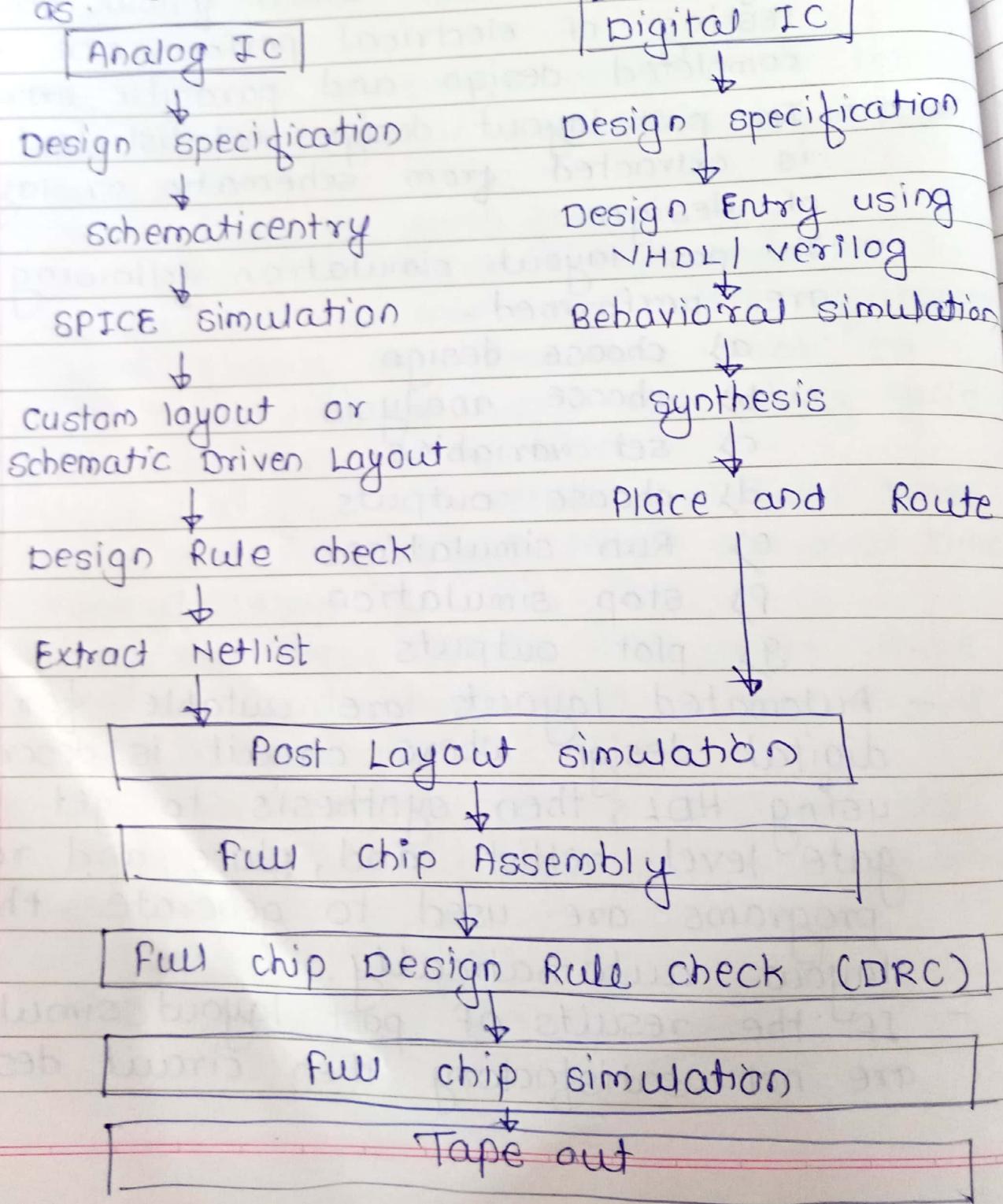
It verify functionality of design by applying input vector and checking for correct output vector.

- The basis of all timing analysis is the clock and sequential components ie. flip flop, Latches.
- clock should be glitch free.
- The clock must, for both high and low phases, meet minimum pulse width requirement.
- When passing data from one clock to other, ensure that worst case duty cycle is used for calculation.
- For flip flop all setup and hold times are met for earliest/latest arrival times for the clock.
- For asynchronous presets and clears, there are two basic parameters ie. recovery & removal must be met.
- To make simplified timing analysis, the designers use single worst case delay which shows maximum T_{PLH} and L_{PHL} .
- In order to carry out timing analysis CAD tools are used.

* Post Layout simulation and parasitic Extraction

- IN ASIC there are two types of simulation first stage of simulation is used for transistor level design to check performance and functionality.
- second stage of simulation is post layout simulation which follows accurately testing of electrical performance of completed design and parasitic extraction
- In post layout design net list text file is extracted from schematic or layout of design.
- In post layout simulation following steps are performed -
 - a) choose design
 - b) choose analysis
 - c) set variables
 - d) choose outputs
 - e) Run simulations
 - f) stop simulation
 - g) plot outputs
- Automated layouts are suitable for digital design where circuit is described using HDL, then synthesis to get the gate level netlist and, place and route programs are used to generate the layout automatically.
- IF the results of post layout simulation are not satisfactory then circuit designer

- can change transistor dimensions.
- The parasitic extraction step is used to identify realistic condition of the system design on given layout.
- Most of the parasitic extraction models used in design tools have numerical limitations.
- Analog and digital IC tapeout is shown as:



* Layout vs Schematic :- (LVS)

⇒ The layout vs schematic is a class of Electronics design automation (EDA) software tool that determines whether a particular integrated circuit layout corresponds to original schematic or circuit diagram of design.

⇒ Layout vs schematic checking software recognizes the drawn shape of layout that represent the electrical components of circuit, as well as connection b/w them. The software then compares them with the schematic or circuit diagram.

⇒ Layout vs schematic checking involves following 3 steps.

- a) Extraction
- b) Reduction
- c) Comparison

a) Extraction :-

The software program takes the database file containing all the layers drawn to represent the circuit during layout. It then runs the database through many logic operations to determine the semiconductor components represented in drawing by their layers of construction. It then examines the various drawn metal layers and finds

how each of these components connects to others.

b) Reduction :-

During reduction the software combines the extracted components in to series and parallel combination if possible and generates netlist representation of layout database.

c) comparison :-

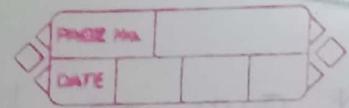
The extracted layout netlist is then compared to netlist taken from circuit schematic.

If the two netlist match, then the circuit passes LVS check. At this point it is said to be LVS clean.

In most cases the layout will not pass LVS first time then layout engineer examines the LVS report and make changes to layout.

⇒ Typical errors encountered during LVS are -

- ① short circuit
- ② Open circuit
- ③ component mismatch
- ④ Missing components.



* Electrical Rule Check (ERC) :-

- Electrical rule check involves checking a design for all wells and substrate areas for proper contact and spacing to ensure correct power and ground connection.

- ERC can also check unconnected inputs and shorted outputs.

- ERC rule checks for things such as,

① Floating gates

② Wrong transistor connections - source and drain connected together for instance

③ Floating interconnect, metal, poly

④ Shorted drain and source of MOS

⑤ No substrate or poly contact or well contact.

⑥ Different contact of substrate / well are connected to different nets.

⑦ Distance of MOS to next substrate / well contact too large.

⑧ Any floating N wells

⑨ Any floating substrate

⑩ Is N well tap connected to ground.

(N well tap always connected to VDD)

⑪ Is p substrate tap connected to Vdd.

(P substrate tap always connected to VSS)

- Design rule checking does syntax analysis on layout whereas electrical rule check does syntax analysis on the network.

* Que. on fabrication methods

- ① Explain fabrication process for NMOS.
- ② Explain fabrication process for PMOS.
- ③ Explain fabrication process for CMOS.
- ④ Explain fabrication process for pwell.
- ⑤ Explain fabrication process for nwell.
- ⑥ Explain fabrication process for dual well or twin tub.

1 Question.