Wearable Microwave Energy Harvesting Circuit to Charge a Cellular Phone

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***Abstract*—In this paper, we will discuss the design, simulation and physical testing of a 2.45 GHz Microwave Energy Harvesting circuit. The circuit consists of a microstip patch antenna with a matching network and rectifier component. We will discuss our metrics of success and our process for verifying the circuit's functionality. We will also discuss the design challenges we encountered during the project, and how we would improve the design in the future. Finally, we will discuss the implications this energy harvesting technology has for the world's social, economic, and environmental systems, and how we factored these into our design.**

I. Introduction

Wireless systems radiate electromagnetic energy through free space. This ambient energy can potentially be captured and converted to DC power. We built an RF energy harvesting circuit to accomplish this task. In our design, an antenna captures radio frequency waves being transmitted through free space. We designed a Printed Circuit Board (PCB) which connected the antenna to a circuit consisting of a matching network and rectifier/DC amplifier. The matching network was used to increase efficiency by matching the impedance of the antenna and load circuit[1].

The antenna was designed to allow frequencies from 2.2 GHz to 2.6 GHz to be transmitted to the rest of the circuit. A rectifier then converted the AC signal to a DC signal and increased the voltage at the output. We utilized a Cockcroft-Walton voltage multiplier to increase the small AC input to a higher DC output. Our initial intention was to use this DC voltage to induce a current across the output load which could be stored in a battery. We sought to use this stored energy to charge a smartphone. However, due to various project constraints, we were forced to abandon this goal. We instead sought to verify the functionality of our RF energy harvesting circuit in producing an output voltage in the near-field and far-field transmission ranges. We performed testing simulations using the Keysight Advanced Design System (ADS) software as well as ANSYS HFSS. Physical testing was performed by utilizing a Voltage Controlled Oscillator to apply input to the circuit and by using a multimeter to measure voltage at the output.

II. Design Process

A. Patch Antenna

We selected a patch antenna since it is simple to design, low-cost, and has relatively good performance. We researched and simulated multiple microstrip patch antennas designed to operate at 2.45 GHz and built the final design on an FR-4 PCB board. Our original design was a patch antenna with a 50 Ohm microstrip feedline. The microstrip feedline is used to feed the antenna and 50 ohms was selected because it is compatible with different types of lab equipment.

The antenna was designed to maximize directivity and gain via a high return loss factor. The design specifications are given below:

Substrate FR-4	Dielectric Constant Er	4.4
	Height	1.6 mm
Conducting Patch	Width	38.532 mm
	Length	28.165 mm
	VSWR at f = 2.45 GHz	1
	Feedline Length	4.5 mm
	Feedline Width	3.5 mm
Ground Plane	Width	47.177 mm
	Length	36.435 mm

Fig. 1. Design specifications of patch antenna

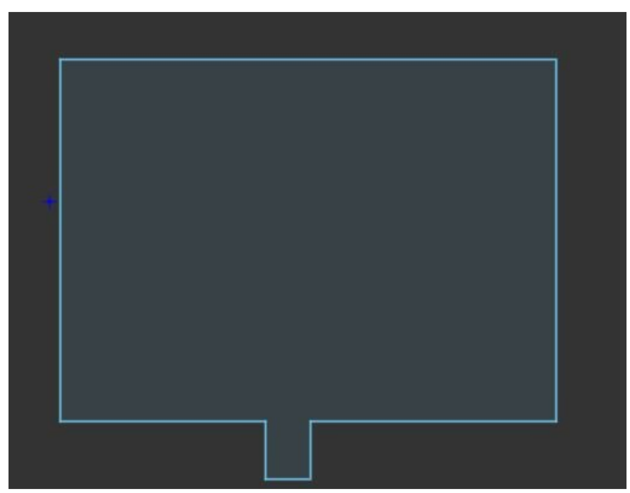

Fig. 2. Patch antenna design from Fusion 360

1) Reasons for Design Specifications: FR-4 was chosen for the substrate because it has a low dielectric constant (Er = 4.4) and is also inexpensive and readily available from manufacturers. The typical dimension for FR-4 is 1.6 mm thickness. This thickness works for our design because the height should be smaller than the wavelength or else the formulas used in our design will be incorrect. These characteristics make it desirable for us to use FR-4 as the substrate in our design.

The dimensions of the patch antenna were selected to allow for operation at a frequency of 2.4 GHz. We chose 2.4 GHz as our resonant frequency because it is a common frequency used in wireless applications. Knowing our desired resonant frequency to be 2.4GHz, we found a corresponding wavelength of lambda = 12.5 cm (lambda = c/f).

$$W = \frac{C_0}{2f_r}\sqrt{\frac{2}{\varepsilon_r+1}} \quad (1)$$

$$\varepsilon_{r-eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\frac{1}{\sqrt{1+12\frac{h}{w}}} \quad (2)$$

Once the substrate material and height were decided, we determined the width of the antenna using the formula one[7]. The width of the antenna has little effect on the resonance frequency, but will influence the bandwidth and input impedance of the antenna. Knowing the width of the antenna we found the effective permittivity of the substrate. This parameter is used to account for the change in permittivity due to the width of the patch and height of the substrate. This parameter is used to calculate the length of the patch to improve the accuracy of the calculation. The length of the antenna was determined by equation 3 and is approximately a quarter wavelength of the resonant frequency to be absorbed by the antenna. However, due to fringing electric fields(3) on the edges of the patch, the effective length is larger than the actual length of the patch antenna. When we calculate L using equation 4, we account for these fringing effects. This is why we have a length smaller than 31.25 mm (one quarter of wifi's wavelength) [7]. This length is what allows for the power to be absorbed and for current to flow resulting in the patch antenna's ability to radiate [6].

$$\Delta L = 0.412h\frac{(\varepsilon_{r-eff}+.3)(\frac{W}{h}+.264)}{(\varepsilon_{r-eff}-.258)(\frac{W}{h}+.8)} \quad (3)$$

$$L = \frac{C_0}{2f_r\sqrt{\varepsilon_{r-eff}}} - 2\Delta L \quad (4)$$

The size of the ground plane was calculated based on the formulas below. We used this equation because it is considered the minimum size allowable for the ground plane [10]. We chose this method to limit the size of the antenna.

$$W_g = 6h + W \quad (5)$$

$$L_g = 6h + L \quad (6)$$

Finally, the feed line allows for the captured electromagnetic waves to travel to the rectifier circuit. The feed line was designed to have an input impedance of 50 Ohms. We used LineCalc to determine the width of the feedline needed to achieve 50 Ohms. We chose 50 ohms as our target because laboratory equipment often requires 50 Ohm feedlines.

After viewing the simulation results shown in section four, we decided that the antenna must be modified because the simulation results did not meet our required goals. So we worked on redesigning the antenna to improve its performance. The same formulas shown above were used except we decided to use 2.45 GHz as the resonating frequency instead of 2.4 GHz because 2.45 GHz is a more accurate representation of wifi frequency. We also added a quarter-wave transformer to the patch antenna to match the impedance of the patch with that of the feedline. The new dimensions are shown below:

Substrate FR4	Dielectric Constant Er	4.4
	Height	1.6 mm
Conducting Patch	Width	38.532 mm
	Length	28.165 mm
	50 Ohm Feedline Width	3 mm
	50 Ohm Feedline Length	32.5 mm
Quarter Wave Transformer	Length	10.5 mm
	Width	1 mm
Ground Plane	Width	47.9 mm
	Length	80.1 mm

Fig. 3. Design specifications of patch antenna for final design

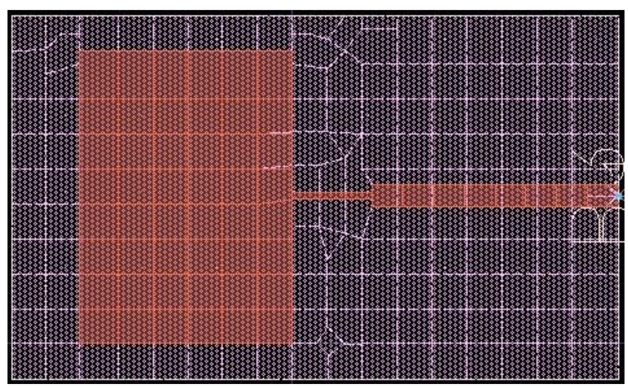

Fig. 4. Final Patch Antenna Design in ADS

For the design of the feedline we used the formula below to determine the width and length of the quarter wave transformer and adjusted it until we obtained the proper results.

$$Z_1 = \sqrt{Z_0 Z_{in}} \quad (7)$$

We were able to compute the value of Z1 by using the transmission line impedance of 50 Ohms (Z0) and the impedance of the edge of the microstrip line that was found to be 243 Ohms. Once finding Z1we used LineCalc to determine the width required to achieve this impedance. We then tuned these values until our antenna obtained the proper requirements.

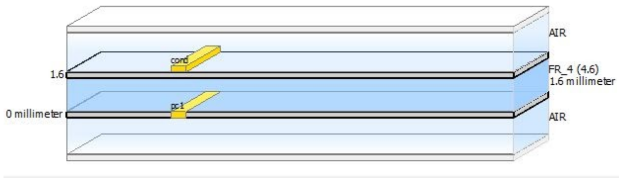

Fig. 5. Substrate used in ADS Simulation

Once we determined a design for our simulation in ADS we also needed to build a substrate model. This model has air on each side of the antenna with a top conducting layer which is the patch antenna and a bottom conducting layer which is the ground plane. The thickness of each copper layer was set to 0.5 oz copper. The FR-4 substrate is placed in between the two conducting layers and has a thickness of 1.6 mm. Once this was setup we could begin simulation in ADS.

We designed the antenna to ensure that the system was capable of resonating at the desired frequency and ensuring that we capture as much power as possible from the surrounding environment.

B. *Voltage Multiplier and Rectifier*

The rectifier design was implemented in ADS to operate at 2.45 GHz. It was simulated using S-parameter Analysis and Harmonic Balance. For the rectifier design, we used a Cockcroft-Walton voltage multiplier which contains diodes, a load resistor, a stage capacitor, a load capacitor and an impedance matching network. The matching network allows for minimum reflection of power from the load. Using just the diodes and capacitors, the voltage multiplier can step up relatively low voltages to high values. This is because the capacitors before the diode store the negative wave cycle that the diode cuts off and then combines it with the negative cycle resulting in double the voltage. We used SMS 7630 Schottky diodes in the rectifying part of the circuit, with a 100k-ohm load resistor used during simulation for maximum output voltage. We also used 3.3nF and 100nF stage and load capacitors respectively. The 3.3 nF capacitors were chosen because they maximized the output voltage of the 3-stage voltage multiplier when tuned in ADS [1].

1) Reasons for Design Specifications: The diode specifics are extremely crucial to a rectifier. A rectifying diode prevents backflow of current and helps in conversion of AC to DC. The SMS 7630 Schottky diodes were used because of their low forward voltage drop of 350 mV and reduced power losses due to conduction and switching. The number of stages in a Cockroft-Walton voltage multiplier has great significance. The reason for choosing a 3-stage voltage multiplier was because of the high output voltage obtained due to the number of stages. If a lower number of stages is used, it will result in a low output voltage, which would in turn restrict the amount of energy that we will be able to obtain from the prototype. If a four-stage voltage multiplier is used, the output voltage obtained as a result of it is almost comparable to the 3-stage multiplier. Moreover, increasing the number of stages over a certain limit causes parasitic effects of capacitors and load

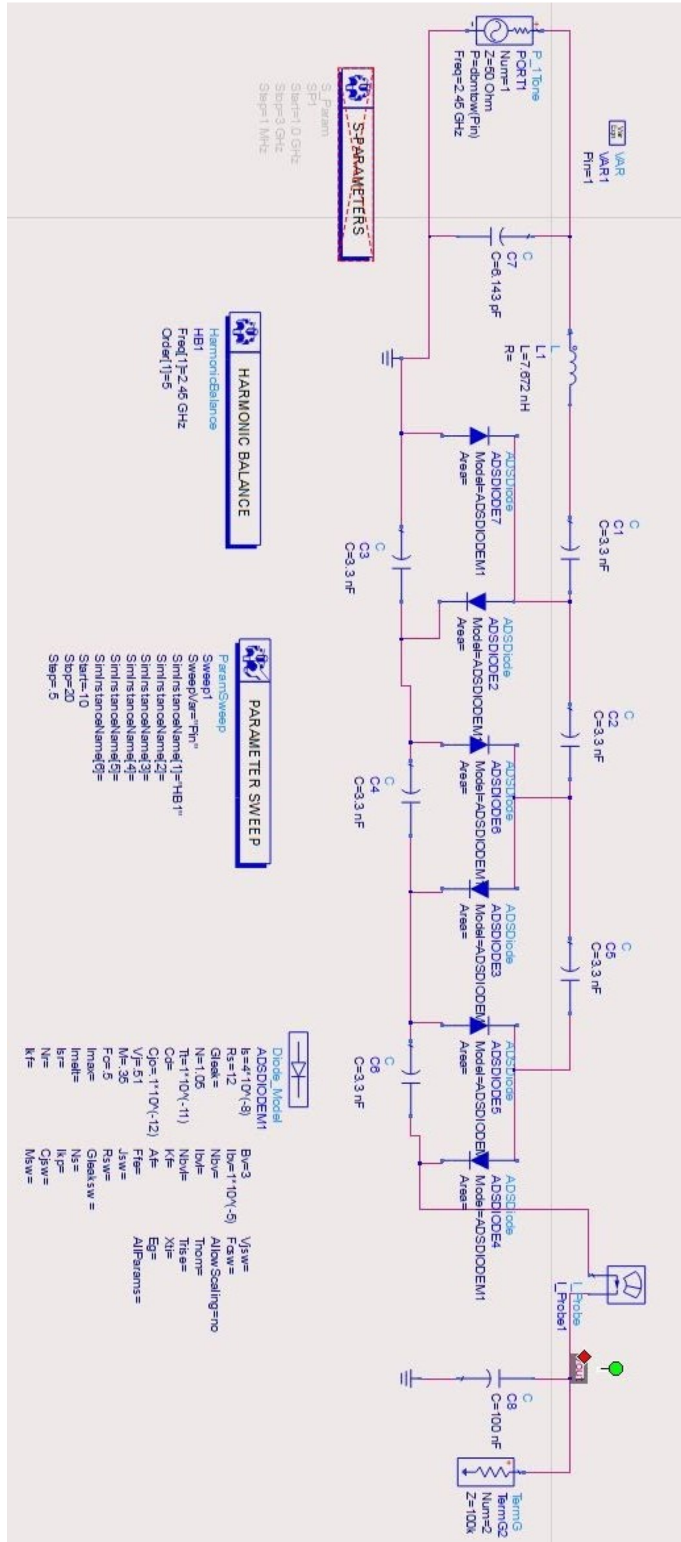

Fig. 6. 3-Stage Cockroft-Walton voltage multiplier simulation in ADS

impedances [1]. In order to prevent this, the number of stages was limited to three.

C. *Prototype Assembly*

The design was sent out to Express PCB who manufactured the antenna and rectifier on a single PCB. We ordered our parts from Digikey.com. Our order contained a range of value for parts we would need and we ordered extra parts. Once the parts were received we built the rectennas by soldering on the ordered parts (it should be noted that the parts we ordered were too small to be soldered with an iron and had to be soldered on with a heat gun). We ended up with two boards, one with a 6.2nH inductor and 7.8 pF capacitor and the other with a 6.1nH and a 7.7pF capacitor for their matching circuits (all other parts other than the matching circuit are identical). Jumper wires were then attached to the outputs to make measuring the voltage across easier.

III. Bill of Materials

Part Name	Part Number	Price Per Unit $	Quantity
CAP CER 0805 3.3NF 1000V X7R 10%	C0805C332KDRACAUTO	0.33	20
CAP CER 6.2PF 50V C0G/NP0 0201	GRM0335C1H6R2BA01D	0.1	4
FIXED IND 7.8NH 1.7A 50 MOHM	LQW15AN7N8J8ZD	0.25	4
RF DIODE SCHOTTKY 1V 75MW SC79	863-1125-1-ND	0.498	20
CAP CER 6.1PF 50V C0G/NP0 0201	587-5349-1-ND	0.036	10
CAP CER 0.1UF 6.3V X6S 0201	GRM033C80J104KE15D	0.018	10
FIXED IND 7.7NH 1.7A 50 MOHM	LQW15AN7N7G8ZD	0.25	4
FIXED IND 7.7NH 1.7A 50 MOHM	LQW15AN7N7G8ZD	0.25	4
FIXED IND 7.9NH 1.7A 50 MOHM	LQW15AN7N9J8ZD	0.25	4
2 Layer - 2 Day StandardPlus (No Mask) Tin Lead Service	EP00014346	29.53	3
	Total Cost= $110.04		

Fig. 7. Bill of Materials

The total cost of our design is $110.04.

IV. Simulation Results

A. Antenna Simulations

The first antenna parameter tested was the S(1,1) parameter also referred to as return loss. This value represents the amount of power reflected by the antenna. An S(1,1) parameter of 0 dB means that all power is reflected from the antenna and is not radiated by the antenna. Usually an S(1,1) parameter below -10 dB implies that more power is being absorbed by the antenna rather than reflected.

The simulated patch antenna shows favorable results with an S(1,1) parameter of -25 dBs at 2.45 GHz. This indicates that the power is being absorbed but it does not indicate if the absorbed power is being radiated by the antenna or if the power is being lost.

Next, we looked at other simulation results such as gain and directivity of the patch antenna. The gain of the antenna shows how well the antenna converts the surrounding RF

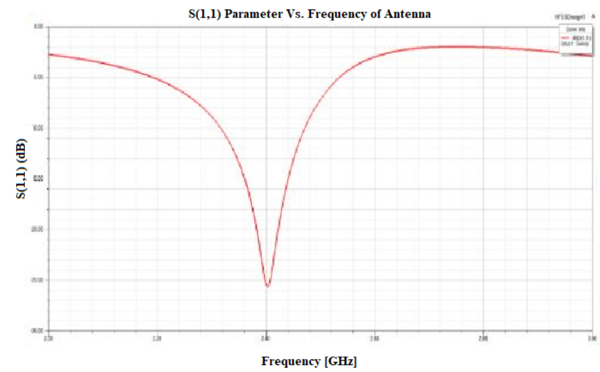

Fig. 8. S(1,1) Parameter of designed patch antenna

	Freq [GHz]	Gain (dB)	Radiation Efficiency
1	2.400000	-3.547762	0.700440

Fig. 9. Gain of Initial Patch Antenna

power around it into electrical power. In our case, we want to achieve high gain since our goal is to capture that energy and make it usable.

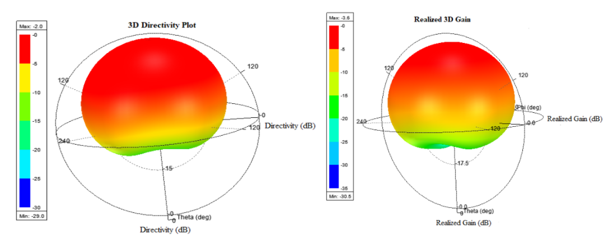

Fig. 10. 3D plots of the gain and directivity of the patch antenna

The results above show that the max gain is -3.54 dBi.Obviously this indicates that the patch antenna is not working properly because its gain and directivity should not be a negative value. Ideally a high gain for a patch antenna is about 8 to 9 dBi. Since we were not getting the results we wanted we decided to create a new patch antenna design, this time using a quarter-wavelength transformer to improve the performance of the antenna.

For the new design we evaluated the same criteria in simulation such as S(1,1), gain, and directivity.

For our final antenna design we were able to obtain a return loss of -21 dB which is lower than our initial design return loss but is higher than the -10 dB threshold that indicates a quality return loss. Although the return loss is not as good, the underlying metrics shown below greatly exceed the previous design and achieve a maximum gain of 5.028 dBi.

We felt that these simulation results were successful and met our design criteria in regards to being able to convert RF energy into electrical energy so we used this antenna design as our final antenna design.

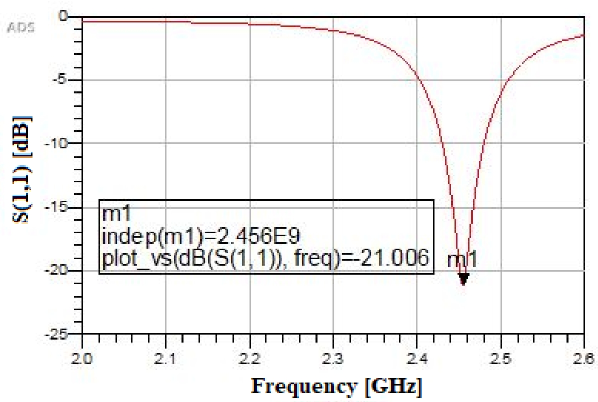

Fig. 11. Return Loss of Final Patch Antenna

Directivity(dBi)	7.52524
Gain (dBi)	5.02888
Radiation efficiency (%)	56.2814

Fig. 12. Antenna Parameters of Final Patch Antenna

B. Cockroft-Walton Voltage Multiplier

The first task of simulating our design was simulating the S(1,1) parameter of the rectifier circuit to obtain the return loss. Return loss describes the amount of power being reflected from the load. This value will be minimized at the desired frequency of 2.45 GHz through the use of a matching impedance network. This was accomplished through an S Parameter sweep from 1 to 3 GHz.

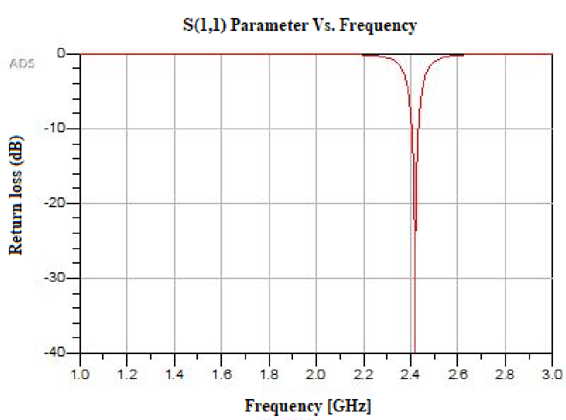

Fig. 13. S(1,1) Parameter of Multiplier Circuit

The results show that the circuit is effectively matched at the desired frequency of 2.45 GHz resulting in maximum power at the load. Once the circuit was effectively matched, we performed simulations using the Harmonic Balance feature in ADS while sweeping the parameter for the power into the multiplier circuit. The harmonic balance feature in ADS allows us to determine node voltages which are used for calculating the RF to DC conversion efficiency of a rectifier. [1] We measured the voltage and current at the load versus the input power of the circuit, as well as the output voltage versus the input power of the circuit. From the graphs, it can be said that increasing the input power from the antenna increases the output voltage up to a certain point after which it gets saturated and remains constant. The same trend is observed for the output current; it increases steadily until it reaches the saturation point after which it remains constant.

The load used in the multiplier design was to determine the output voltage obtained from the simulations. For the prototype, we switched the load to an LED, which would potentially give similar results once an output voltage is obtained. The simulations show the correct operation of the circuit, while the current and voltage values may differ based on the load. The simulation results allow us to gauge the ability to generate a higher voltage and current even though the load in the simulations differs from that used in our final prototype.

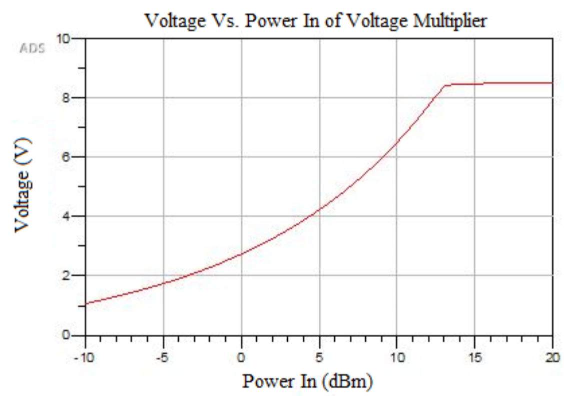

Fig. 14. Output voltage of multiplier Vs. power input

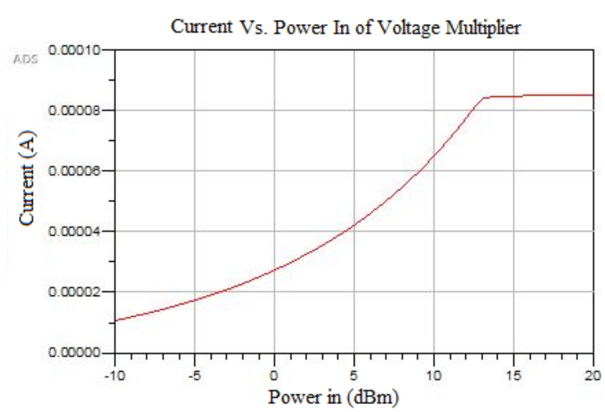

Fig. 15. Current of Load Vs. Power in

C. Finalized Rectenna

As the last step of our simulation process, we designed and built an antenna and rectifier model on ExpressPCB. Using the specifications from the ADS simulations, the diodes and capacitors were placed in the rectifier part of the circuit. These components were also placed very close to one another, thereby closing any big gap between each component of the rectifier. This was done so that any discrepancies in the lengths of the transmission lines between the circuit components can be eliminated.

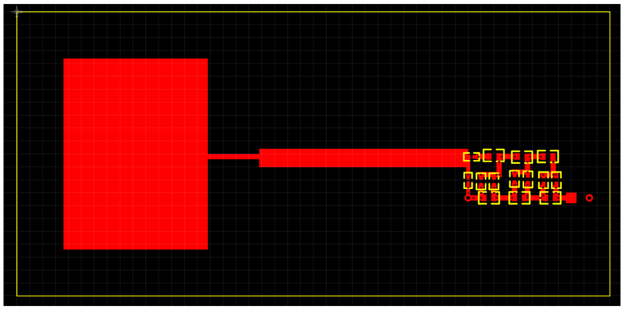

Fig. 16. Rectenna Model designed on ExpressPCB

V. Metric of Success

A. Antenna

1) Simulate a patch antenna in ADS and demonstrate 2.45 GHz operation and proper S11 parameters. (Success)
2) Fabricate a functioning antenna based on the simulated design (Success)
3) Measure S11 parameters, gain, and frequency of operation via network analyzer. Our antenna would be considered successful if it has a S11 parameter of -15dB, a gain of -5dB, and an operating frequency of 2.45 GHz. (We were unable to use a network analyzer during this project)
4) Demonstrate functionality of the antenna by utilizing a VCO to provide input power and a multimeter to measure voltage at the output of the circuit. (Success)

From our initial metrics of success for the patch antenna we were able to properly simulate a patch antenna in ADS and get an S(1,1) parameter of -21 dB at 2.45 GHz which is better than the design goal of -10dB. We then successfully fabricated the antenna using ExpressPCB and were able to get results that indicated the antenna was working. However, we were not able to get specific readings about the actual S(1,1) parameter and gain of our fabricated antenna due to lack of lab equipment.

B. Rectifier and Voltage Multiplier

1) Simulate the functionality of a Cockcroft-Walton Voltage Multiplier. Simulate S11 parameters and harmonic balance analysis. (Success)
2) Fabricate a functioning Cockcroft-Walton Voltage Multiplier on an FR-4 or PCB board. (Success)
3) Have the rectifier successfully convert AC power from our antenna into DC power that can be used to charge or power a load. (Success converting, failed to charge or power a load).

When performing the S(1,1) analysis and harmonic balance in simulation, our rectifier circuit showed proper operation at 2.45 GHz. It achieved an S(1,1) value of -40 dB and a max DC voltage of 8.3 V when a power of 20 dBm was applied. We considered our design successful in simulation. We were also able to fabricate the rectifier circuit onto the PCB board. When testing, we were able to get a DC voltage output reading which implies that the circuit did convert AC into a DC voltage like intended. However, it was not a high enough voltage to power anything meaningful, as it was only able to produce about 100 mV consistently.

C. Load

1) Illuminate an LED solely from power harvested and converted via our antenna and rectifier. (Failed)
2) Charge a battery (any variety) solely from power harvested and converted via our antenna and rectifier. (Failed)
3) Charge an AA battery (starting at no stored charge) enough that the battery can be used in a phone charging circuit to charge a cellular phone (1 percent phone charge increase). (Failed)

Ultimately we were not able to meet any of these metrics for success because the voltage output we were getting was considerably lower than expected.

VI. Alternatives

A. Antenna Alternatives

1) Dipole antenna: This was an alternative we considered, since the antenna can receive power from a greater range of direction compared to a patch antenna. The downside and reason we did not choose a dipole antenna is because the gain was far too low for our project application [8].
2) Array of patch antennas: An array of patch antennas would be preferred for our application due to the increase in power that would be harvested (due to larger surface area being covered), and the increased directionality the array could provide (theoretically we could have each individual antenna facing a different direction) [4]. While attempting to make an array of patch antennas, we faced time constraints and production limitations, thereby making this alternative difficult for us during the design process.

B. Voltage Multiplier/Rectifier Alternatives

1) Buck boost converter: The buck boost converter converts a dc voltage to a higher or lower dc voltage depending on its setup. However the voltage coming into the circuit is an ac signal so the voltage would need to be rectified. This would make the circuit more complicated than the voltage multiplier since the voltage multiplier already acts as a rectifier circuit. Moreover, a high gain is not achievable due to the poor efficiency of a buck boost converter [9].
2) Operational amplifier circuit: We briefly considered an operational amplifier to increase the gain of our rectified signal before it reached our load. This idea was abandoned due to the operational amplifier needing a power source to operate.

C. Load Alternatives

1) Smartphone: While our testing involved the use of an LED, our initial plans involved charging a battery, that would allow us to charge a smartphone. However, this idea was abandoned due to time constraints and production limitations, and verifying this load would require more resources and development to our prototype design. Although this load idea was discarded, it may potentially be used in future applications of the prototype that we built.
2) Peltier Plates: Another alternative we had looked into was thermo cooling plates that use the Peltier effect. These plates have the ability to make one side hot and one side cold when power is put through the device. In the future, our project may be used to power one or more of these devices for different applications. These plates could then be integrated into clothing to allow the users to heat or cool themselves as they wish.

VII. Testing

For testing, we first attempted to use a commercial Wi-Fi router to produce a 2.45GHz signal that would power our antenna and rectifying circuit. Unfortunately, the router was not a reliable source for a 2.45GHz signal. We then used a voltage controlled oscillator (VCO) to test our antenna design. The VCO we were using had an emitter and a power supply which we set to 9.9V and 0.1A for Vtune to produce an emitted signal of 2.45GHz (note that we did adjust these values to look at the effect of other frequencies on the antenna, but the effects were difficult to interpret). We then placed the antennas we built at various distances from the emitter and measured the voltage across the outputs using soldered on jumper wires and a multimeter. We found voltage values for distances between 1cm and 10cm for the two rectennas we built.

VIII. Results

For our results we found that we are currently incapable of charging an LED with just a single rectenna. Our voltages and currents were far too low. We also would be unable to charge a battery with our current design, but an array of antennas may be able to light an LED or charge a battery.

IX. Future Design Improvements

The primary design challenge we faced was a limitation on input power and consequently, the amount of power that could be retrieved at output. In the future, we would attempt to modify the input side of the circuit from a single microstrip patch antenna to a matched array of antennas. Additionally, our antenna suffered from poor directivity during testing. The output power dropped off rapidly when the antenna was slightly rotated. We would perform more thorough trial-and-error testing of the receiving antenna via the lab equipment and microwave horn antenna in the future. Ideally, we would improve the design to have omni-directionality in its reception in order to maximize the amount of ambient energy being utilized.

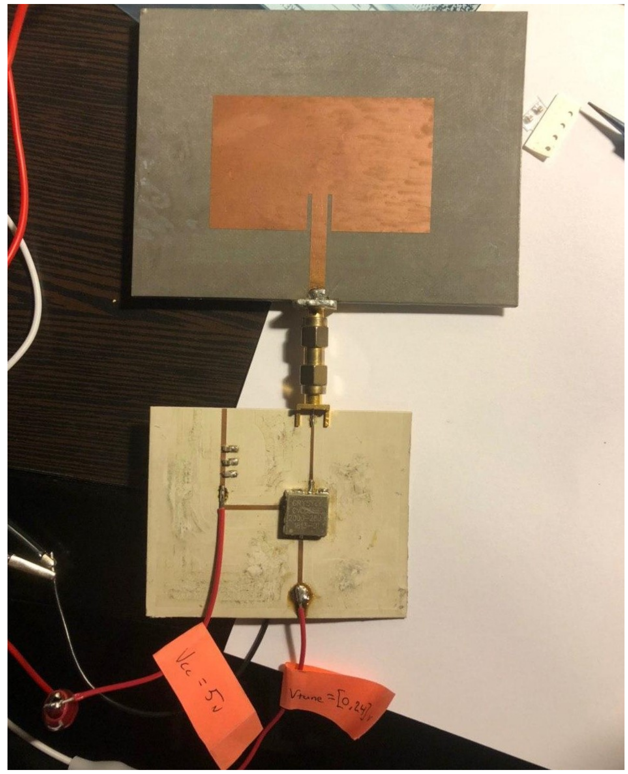

Fig. 17. VCO emitter patch antenna

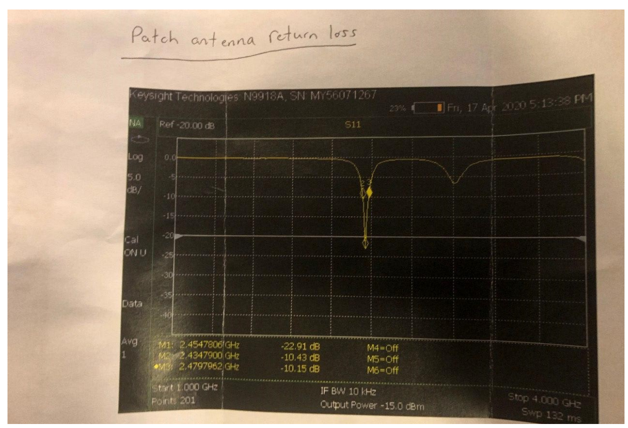

Fig. 18. VCO patch antenna return loss

After obtaining higher output power, we would begin testing different output loads. We would first need to be successful in lighting the LED, obtaining an output voltage of approximately 1.7 Volts. Once we achieve these higher output voltages, we could begin pursuing our original goal of connecting a battery at the load to accumulate charge.

X. Societal Impact

Our prototype utilizes low cost materials and is conservational in its very concept. Our initial design goal envisioned a cost-effective way in which one could carry one of these harvesting devices and improve their personal energy efficiency. The ability to harvest RF energy from free space has massive implications for society because it allows us to make use of

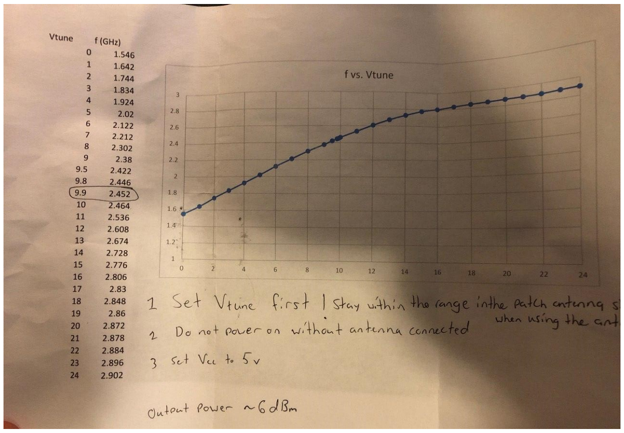

Fig. 19. VCO emitter data

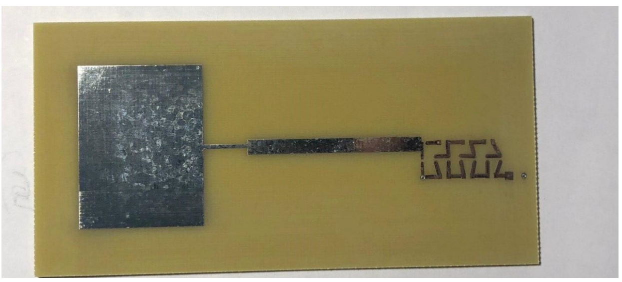

Fig. 20. Board recieved from ExpressPCB

energy that may otherwise be wasted. Developments in this technology can lead to improved energy efficiency, a reduction in battery usage and thus a reduction in waste materials, and reduction in the amount of electricity consumed. The significance of wireless energy harvesting in the progression of environmental causes and societal development has been a major motivating factor in our research and study as engineers.

XI. Conclusion

After having researched, designed, and simulated a patch antenna and rectifier, we built our final rectenna prototype. This prototype primarily works as an energy harvesting device that utilizes Wi-Fi signals in the environment and converts it into DC voltage that could potentially be used to power a device. After testing, we obtained an output voltage that verifies the working of our prototype. Although the output voltage would need to be increased to light up an LED, we have been able to get a result for the output to attest to the functionality of the prototype. Moving forward with research and additional developments to the design could result in a bigger device being charged, with multiple applications. With an array of antennas, our prototype can be used as a portable charger to charge a smartphone. The prototype can also cater to other wireless charging applications, especially in healthcare, such as charging an insulin pump and moving away from the use of batteries.

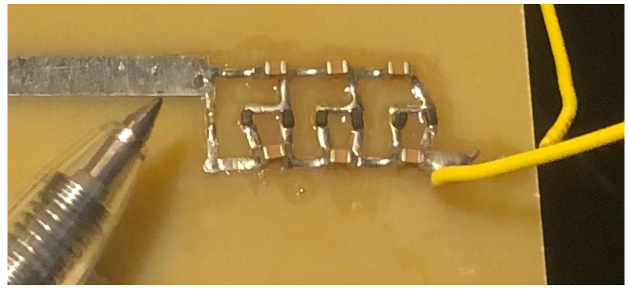

Fig. 21. Soldered rectenna circuit

(7.8nH and 6.2pF)	Vout	Iout
@10cm	.008V	NA
@7cm	.017V	NA
@5cm	.024V	NA
@2.5cm	.047V	0.001mA
@1cm	.107V	0.002mA

(7.7nH and 6.1pF)	Vout	Iout
@10cm	.005V	NA
@7cm	.011V	NA
@5cm	.021V	NA
@2.5cm	.082V	0.001mA
@1cm	.348V	0.002mA

Fig. 22. Measured results from rectennas

XII. References

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