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TOPIC:

Introduction Flip-Flops and Its Types

(Lecture 2)

Types of Digital Circuits

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1. Combinational Circuits
2. Sequential Circuits

Combinational Circuits

- The outputs of the combinational circuit depend only on the present inputs.
- The feedback path is not present in the combinational circuit.
- In combinational circuits, memory elements are not required.
- The clock signal is not required for combinational circuits.
- The combinational circuit is simple to design.

Combinational Circuits are

1. Half and full Adder
2. Half and full subtractor
3. Binary Adder-subtractor
4. Decimal to BCD converter.

Sequential Circuits

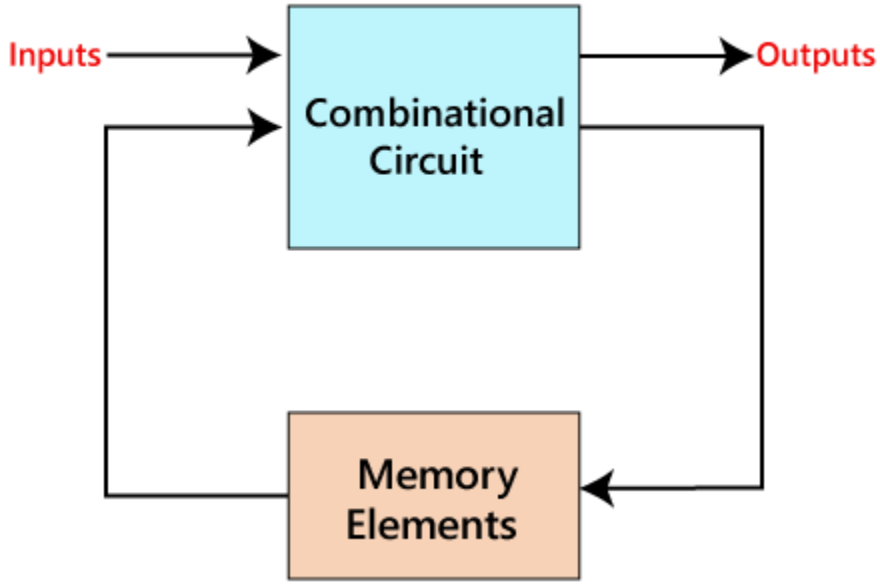
- The outputs of the sequential circuits depend on both present inputs and present state(previous output).
- The feedback path is present in the sequential circuits.
- In the sequential circuit, memory elements play an important role and require.
- The clock signal is required for sequential circuits.
- It is not simple to design a sequential circuit.

Sequential Circuits are

Flip Flops
Registers
Counters
Latches etc.

Sequential Circuits

The sequential circuit is a special type of circuit that has a series of inputs and outputs. The outputs of the sequential circuits depend on both the combination of present inputs and previous outputs. The previous output is treated as the present state. So, the sequential circuit contains the combinational circuit and its memory storage elements. A sequential circuit doesn't need to always contain a combinational circuit. So, the sequential circuit can contain only the memory element.



Introduction

- There are two types of sequential circuits:
  - *synchronous*: outputs change only at specific time
  - *asynchronous*: outputs change at any time
- Bistable logic devices: *latches* and *flip-flops*.
- Latches and flip-flops differ in the method used for changing their state.

Types of Sequential Circuits

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Asynchronous sequential circuits:

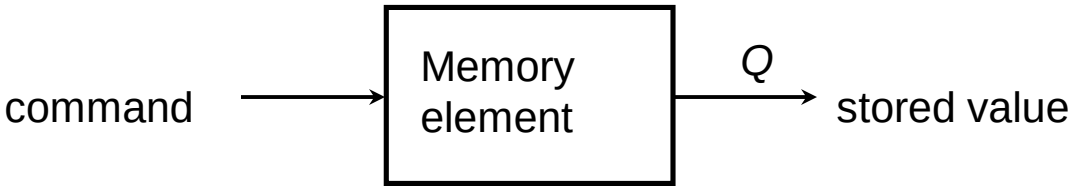
The clock signals are not used by the **Asynchronous sequential circuits**. The asynchronous circuit is operated through the pulses. So, the changes in the input can change the state of the circuit. The asynchronous circuits do not use clock pulses. The internal state is changed when the input variable is changed. The un-clocked flip-flops or time-delayed are the memory elements of asynchronous sequential circuits. The asynchronous sequential circuit is similar to the combinational circuits with feedback.

Synchronous sequential circuits:

In synchronous sequential circuits, synchronization of the memory element's state is done by the clock signal. The output is stored in either flip-flops or latches(memory devices). The synchronization of the outputs is done with either only negative edges of the clock signal or only positive edges.

Memory Elements

- **Memory element**: a device which can remember value indefinitely, or change value on command from its inputs.



- Characteristic table:

Command (at time *t*)	*Q(t)*	*Q(t+1)*
Set	X	1
Reset	X	0
Memorise / No Change	0	0
	1	1

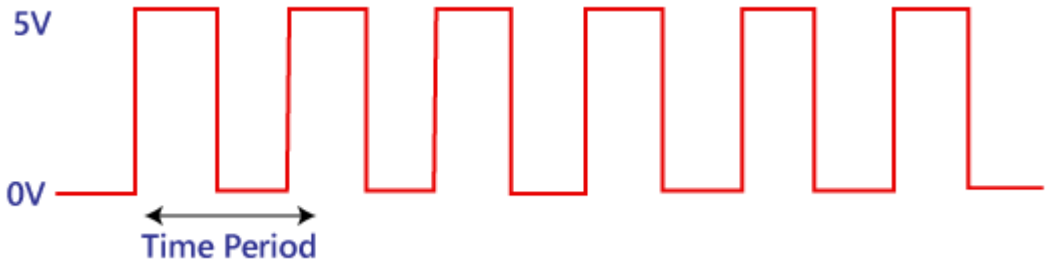
Q(t): current state

Q(t+1) or Q^+: next state

Clock Signal and Triggering

Clock signal

- A clock signal is a periodic signal in which ON time and OFF time need not be the same. When ON time and OFF time of the clock signal are the same, a square wave is used to represent the clock signal. Below is a diagram which represents the clock signal:
- A clock signal is considered as the square wave. Sometimes, the signal stays at logic, either high 5V or low 0V, to an equal amount of time. It repeats with a certain time period, which will be equal to twice the 'ON time' or 'OFF time'.



Memory Elements

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- Two types of triggering/activation:
  - pulse-triggered
  - edge-triggered
- Pulse-triggered
  - latches
  - ON = 1, OFF = 0
- Edge-triggered
  - flip-flops
  - positive edge-triggered (ON = from 0 to 1; OFF = other time)
  - negative edge-triggered (ON = from 1 to 0; OFF = other time)

Types of Triggering

These are two types of triggering in sequential circuits:

1. **Level triggering**

- Positive level triggering
- Negative level triggering

Fig: 1.4 Positive Level Triggering

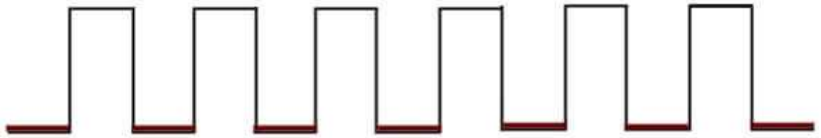


Fig: 1.5 Negative Level Triggering

2. **Edge triggering**

- Positive edge triggering
- Negative edge triggering

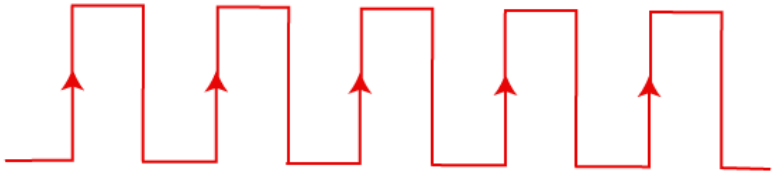


Fig: 1.6 Positive Edge Triggering

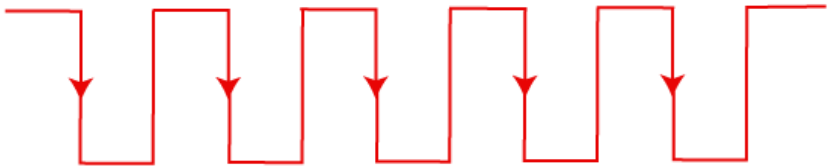


Fig: 1.7 Negative Level Triggering

S-R Latch

- *Complementary* outputs: *Q* and *Q′*.
- When *Q* is HIGH, the latch is in *SET* state.
- When *Q* is LOW, the latch is in *RESET* state.
- For *active-HIGH input* S-R latch (also known as NOR gate latch),

  R=HIGH (and *S*=LOW) RESET state

  S=HIGH (and *R*=LOW) SET state

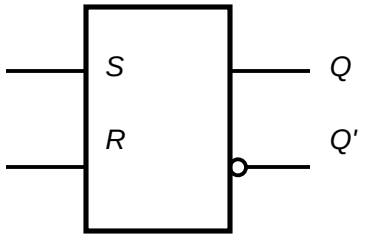
  both inputs LOW no change

  both inputs HIGH *Q* and *Q′* both LOW (invalid)!

S-R Latch

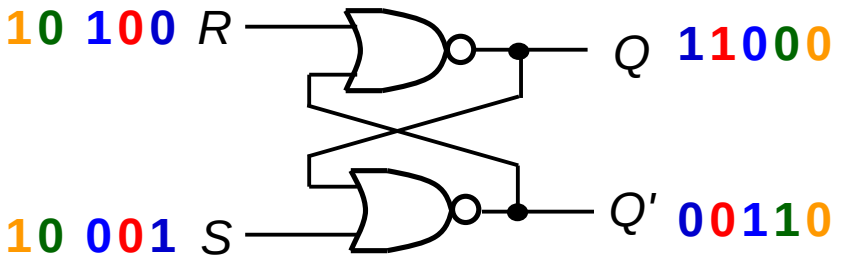
- Characteristics table for active-high input S-R latch:

S	R	Q	Q'	
0	0	NC	NC	No change. Latch remained in present state.
1	0	1	0	Latch SET.
0	1	0	1	Latch RESET.
1	1	0	0	Invalid condition.



S-R Latch

- Active-HIGH input S-R latch



S	R	Q	Q′	
1	0	1	0	initial
0	0	1	0	(afer S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	invalid!

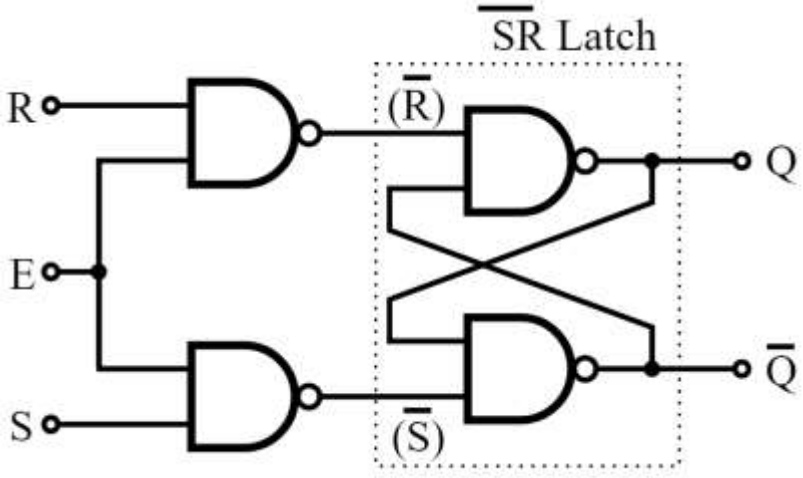
Basics of Flip Flop

A circuit that has two stable states is treated as a **flip flop**. These stable states are used to store binary data that can be changed by applying varying inputs. The flip flops are the fundamental building blocks of the digital system. Flip flops and latches are examples of data storage elements. In the sequential logical circuit, the flip flop is the basic storage element. The latches and flip flops are the basic storage elements but different in working. There are the following types of flip flops:

1. SR Flip Flop
2. J-K Flip-flop
3. D Flip Flop
4. T Flip Flop

SR Flip Flop

It is a Flip Flop with two inputs, one is S and other is R. **S** here stands for Set and **R** here stands for Reset. Set basically indicates set the flip flop which means output 1 and reset indicates resetting the flip flop which means output 0. Here clock pulse is supplied to operate this flip flop, hence it is clocked flip flop.



Truth Table:

S	R	Qn+1	State
0	0	Qn	Hold
0	1	0	Reset
1	0	1	Set
1	1	X	Invalid

Working of SR Flip Flop

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Case 1: Let's say, **S=0** and **R=0**, then output of both AND gates will be 0 and the value of Q and Q' will be same as their previous value, i.e, Hold state.

Case 2: Let's say, **S=0 and R=1**, then output of both AND gates will be 1 and 0, correspondingly the value of Q will be 0 as one of input is 1 and it is a NOR gate so it will ultimately gives 0, hence Q gets 0 value, similarly Q' will be 1.

Case 3: Let's say, **S=1 and R=0**, then output of both AND gates will be 0 and 1, correspondingly the value of Q' will be 0 as one of input to NOR gate is 1, so output will be 0 ultimately and this 0 value will go as input to upper NOR gate, and hence Q will become 1.

Case 4: Let's say, **S=1 and R=1**, then output of both AND gates will be 1 and 1 which is invalid, as the outputs should be complement of each other.

Characteristic Table of SR Flip Flop

S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid

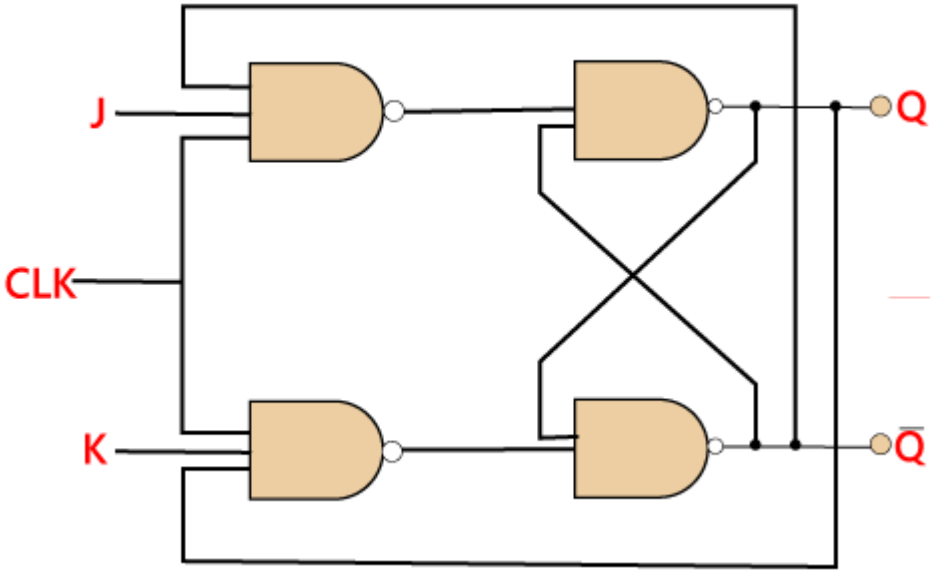
Excitation Table

•Excitation Table basically tells about the excitation which is required by flip flop to go from current state to next state.

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

J-K Flip-flop

- The JK flip flop is used to remove the drawback of the S-R flip flop, i.e., undefined states. The JK flip flop is formed by doing modification in the SR flip flop. The S-R flip flop is improved in order to construct the J-K flip flop. When S and R input is set to true, the SR flip flop gives an inaccurate result. But in the case of JK flip flop, it gives the correct output.
- In J-K flip flop, if both of its inputs are different, the value of J at the next clock edge is taken by the output Y. If both of its input is low, then no change occurs, and if high at the clock edge, then from one state to the other, the output will be toggled. The JK Flip Flop is a Set or Reset Flip flop in the digital system.



Truth Table:

J	K	Qn+1
0	0	hold
0	1	0
1	0	1
1	1	Toggle(Qn)

Characteristic Table

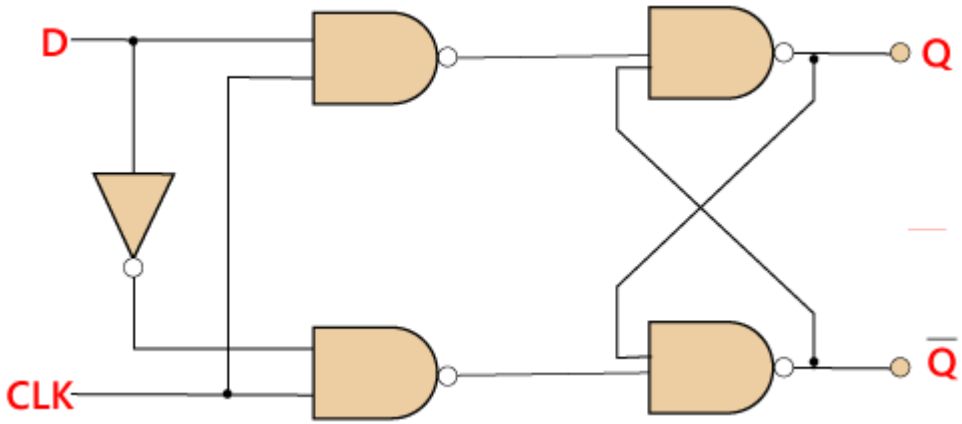
J	K	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

Qn	Qn+1	J	K
0	0	0	x
0	1	1	x
1	0	X	1
1	1	X	0

D Flip Flop

D flip flop is a widely used flip flop in digital systems. The D flip flop is mostly used in shift-registers, counters, and input synchronization.

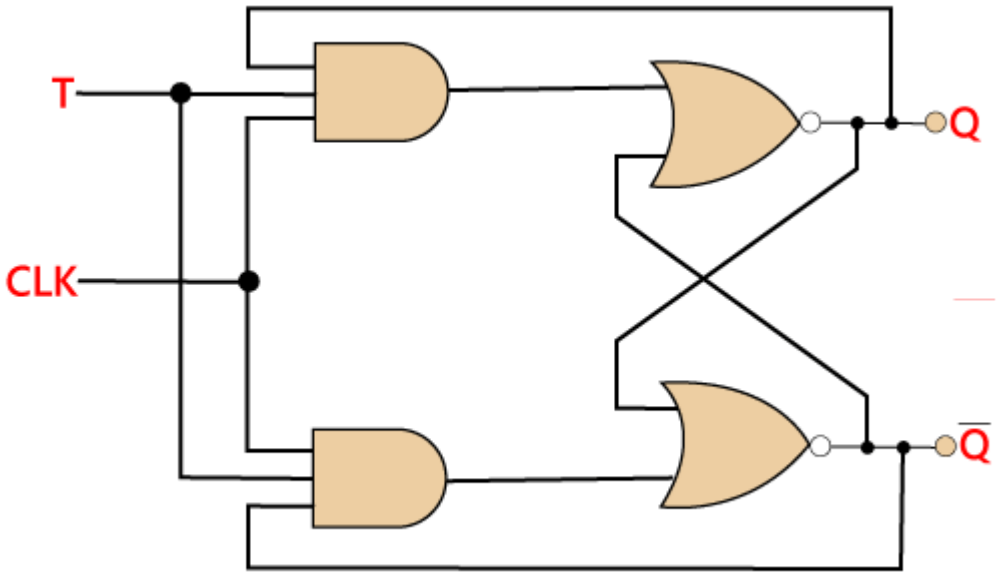


Truth Table:

D	Qn+1
0	1
0	1

T Flip Flop

- Just like JK flip-flop, T flip flop is used. Unlike JK flip flop, in T flip flop, there is only single input with the clock input. The T flip flop is constructed by connecting both of the inputs of JK flip flop together as a single input. The T flip flop is also known as **Toggle flip-flop**. These T flip-flops are able to find the complement of its state.



Truth Table:

T	Y	Y(t+1)
0	0	0
1	0	1
0	1	1
1	1	0