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Design of Synchronous (mod-n) counters.

(Lecture 8-10)

Counter

Definition:

A Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit.

Types of Counter

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Asynchronous Counters:

- Only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop.
- Asynchronous counters are slower than synchronous counters because of the delay in the transmission of the pulses from flip-flop to flip-flop.
- Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops.

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Synchronous Counters:

- All flip-flops are clocked simultaneously by an external clock.
- Synchronous counters are faster than asynchronous counters because of the simultaneous clocking.
- Synchronous counters are an example of state machine design because they have a set of states and a set of transition rules for moving between those states after each clocked event

Design Mod – N synchronous Counter

- The value of N can be different from power of 2. Also, the counting sequence may be random for example some cyclic code (8421, 2423 etc). The following method is applied for designing for mod N and any counting sequence.

- Design for Mod-N counter :

  The steps for the design are:

Step 1

Step 1 :Decision for number of flip-flops

- Example : If we are designing mod N counter and n number of flip-flops are required then n can be found out by this equation.
- $$N \leq 2^n$$
- Here we are designing Mod-10 counter Therefore, N= 10 and number of Flip flops(n) required is

  For n =3, 10<=8, which is false.

  For n= 4,10<=16, which is true.

Therefore number of FF required is 4 for Mod-10 counter.

Step 2

- **Step 2 : Write excitation table of Flip flops.**

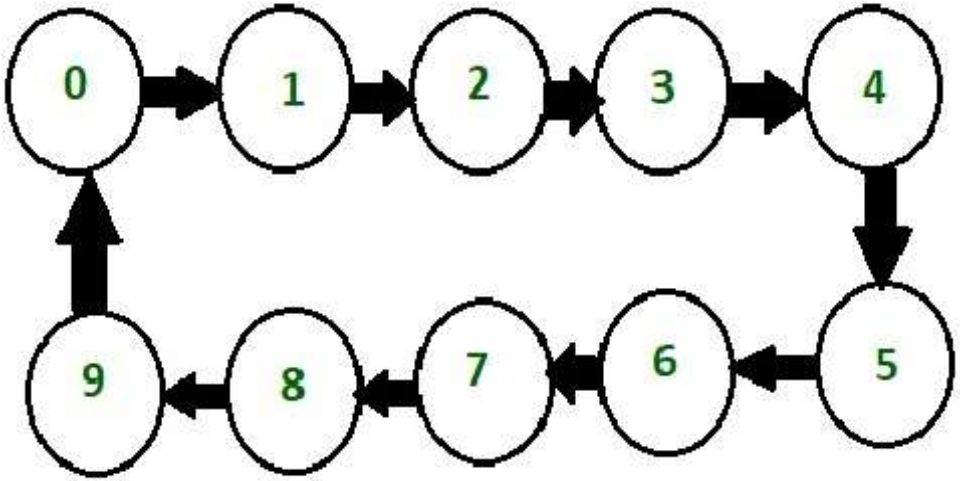
  Here T FF is used.

Previous state(Q_n)	Next state(Q_{n+1})	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T FF.

Step 3

- Step 3 : Draw state diagram and circuit excitation table.



Counting Sequence of Decade counter

A decade counter is called as mod -10 or divide by 10 counter. It counts from 0 to 9 and again reset to 0. It counts in natural binary sequence. Here 4 T Flip flops are used. It resets after Q3 Q2 Q1 Q0 = 1001.

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Circuit excitation table:

- Here Q_3 Q_2 Q_1 Q_0 are present states of four flip-flops and Q^*_3 Q^*_2 Q^*_1 Q^*_0 are next counting state of 4 Flip flops. If there is a transition in current state i.e if Q3 value changes from 0 to 1 or 1 to 0 then there's corresponding T(toggle) bit is written as 1 otherwise 0.

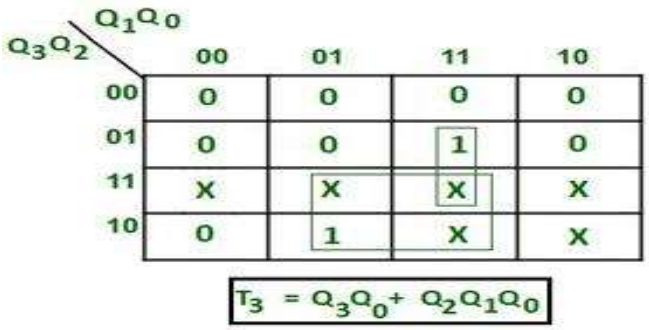
Continue…

Q_3	Q_2	Q_1	Q_0	Q^+_3	Q^+_2	Q^+_1	Q^+_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

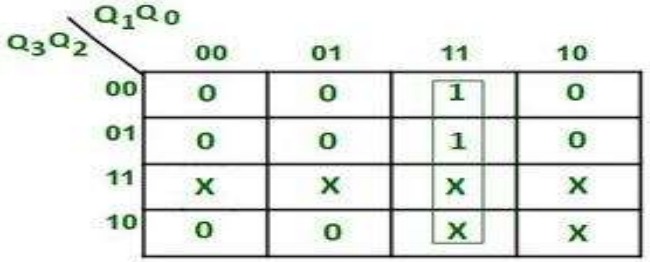
Step 4

Step 4 : Create Karnaugh map for each FF input in terms of flip-flop outputs as the input variable.

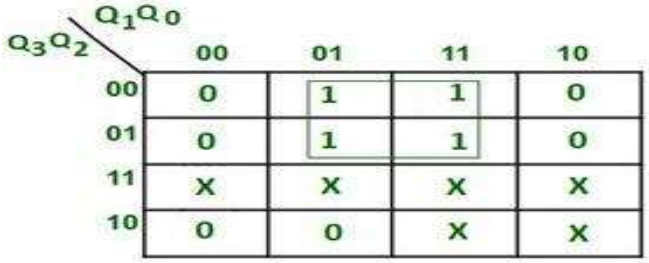
Simplify the K map –



$T_3 = Q_3Q_0 + Q_2Q_1Q_0$



$T_2 = Q_1Q_0$



$T_1 = Q_3'Q_0$

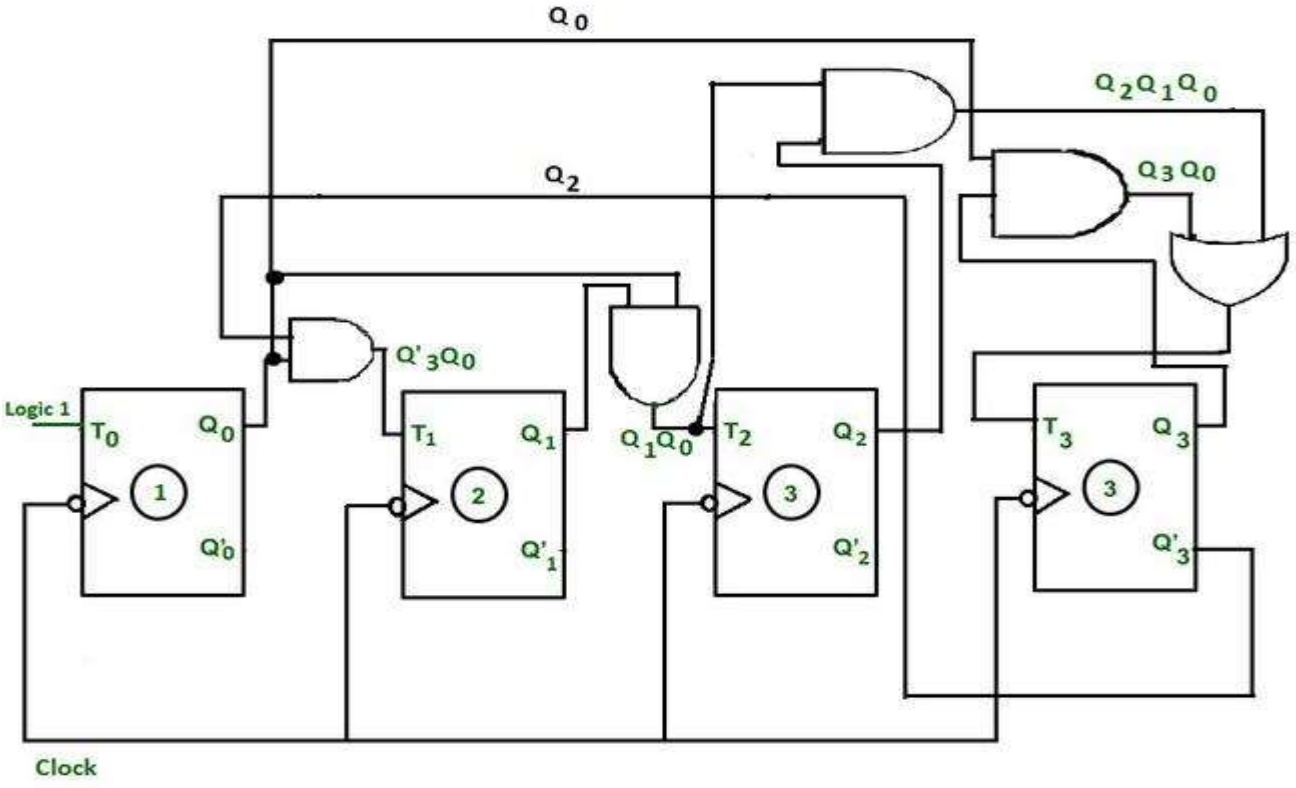
$T_0 = 1$

Step 5

- **Step 5 : Create circuit diagram**

Here negative edge triggered clock is used for toggling purpose. The clock is provided to every Flip flop at same instant of time. The toggle(T) input is provided to every Flip flop according to the simplified equation of K map.

Continue…

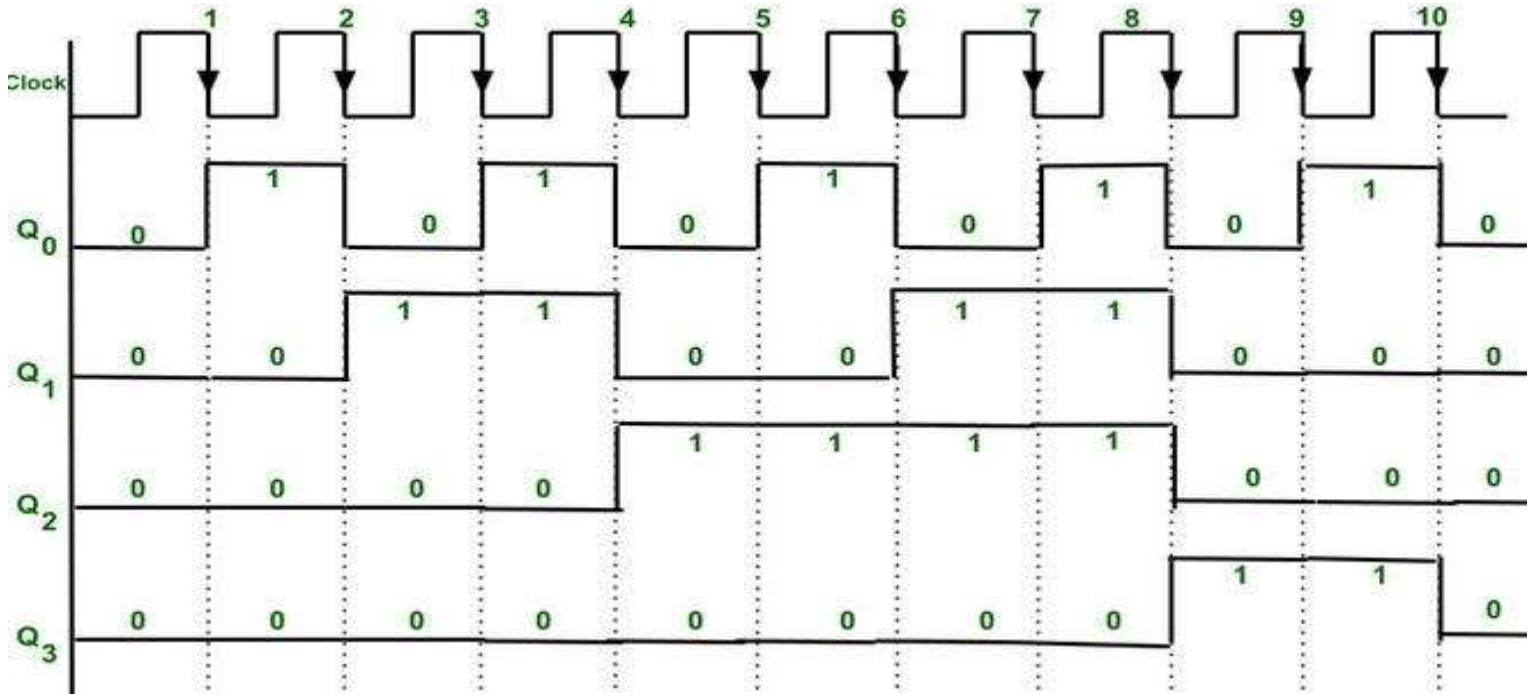

Q0
Q2
Q2Q1Q0
Q3Q0
Q'3Q0
Q1Q0
Logic 1
T0
Q0
Q'0
1
T1
Q1
Q'1
2
T2
Q2
Q'2
3
T3
Q3
Q'3
3
Clock

Timing diagram : Here toggling is used.

Previous state(Q_n)	T	Next state(Q_{n+1})
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic table of T FF.

- The state of a FF will change only when toggle input(T) of a FF is 1.



Timing diagram of synchronous Decade counter

Explanation :

- Initially Q3 Q2 Q1 Q0 are 0 0 0 0.
- The sequence of counter can be verified from the timing diagram. At every falling edge of the clock output Q_0 toggles because T_0 is connected to logic 1.
- T_1 becomes 1 only when expression T1 = Q'_3Q_0 becomes 1 also if clock falling edge occurs(because there is negative edge triggering) then the output state of T_1 i.e Q_1 will change.
- T_2 becomes 1 only when expression T2 = Q_1Q_0 becomes 1 also if clock falling edge occurs then the output state Q2 will change.

Continue…

- T_3 becomes 1 only when expression T1 = Q_3Q_0 + $Q_2Q_1Q_0$ resultant becomes 1 also if clock falling edge occurs(because there is negative edge triggering) then the state of Q3 will change.
- We get Output as Q_3(MSB) Q_2 Q_1 Q_0(LSB).
- After 10th falling edge the output state of all the FFs again becomes 0 0 0 0.