Introduction to Computer Organization & Architecture, Overview of Digital System

Q1. What is computer organization?

a) Study of the internal working, structuring, and implementation of a computer system
b) Design of the microprocessor
c) Study of algorithms
d) Programming languages
Answer: a

Q2. What does the term 'architecture' in computer science refer to?

a) The physical structure of the computer
b) The design of the computer's CPU and memory system
c) The layout of components within the computer
d) The software used to control the hardware
Answer: b

Introduction to Flip-Flops and its types

Q3. What is a flip-flop?

a) A circuit used to store one bit of data
b) A logic gate used for addition
c) A device to perform multiplication
d) A type of memory used in hard drives
Answer: a

Q4. Which of the following is not a type of flip-flop?

a) SR flip-flop
b) JK flip-flop
c) T flip-flop
d) XYZ flip-flop
Answer: d

Q5. What is a JK flip-flop?

a) A type of flip-flop with J (set) and K (reset) inputs
b) A flip-flop that cannot be set or reset
c) A flip-flop that always holds a value
d) A non-sequential circuit
Answer: a

Shift Registers: SIPO, SISO, PISO and PIPO

Q6. What does SIPO stand for in shift registers?

a) Serial In Parallel Out
b) Serial In Print Out
c) Single In Parallel Out
d) Serial Input Parallel Output
Answer: a
Q7. What is the function of a PISO shift register?

a) Converts parallel data to serial data
b) Converts serial data to parallel data
c) Stores a single bit of data
d) Performs arithmetic operations
Answer: a
Introduction and Design of Synchronous (mod-n) and Asynchronous (Ripple) counters
Q8. What is a synchronous counter?

a) A counter where all flip-flops are clocked simultaneously
b) A counter where flip-flops are clocked one after another
c) A counter that uses D flip-flops
d) A counter used for arithmetic operations
Answer: a
Q9. What distinguishes an asynchronous counter from a synchronous counter?

a) Only some flip-flops are clocked simultaneously
b) Flip-flops are clocked in a cascading fashion
c) It uses multiple clock signals
d) It is faster than a synchronous counter
Answer: b
Basic Computer Organization: Instruction Codes, Computer Registers, Computer Instructions
Q10. What is an instruction code?

a) A set of rules for writing programs
b) A binary code that specifies a particular operation to be performed
c) The language used for communication between computers
d) A code used for error checking
Answer: b
Q11. What are computer registers?

a) High-speed storage locations within the CPU
b) Permanent storage locations for data
c) External storage devices
d) Part of the computer's memory hierarchy
Answer: a
Q12. Which register holds the address of the next instruction to be executed?

a) Program Counter (PC)
b) Instruction Register (IR)
c) Memory Address Register (MAR)
d) Accumulator
Answer: a
Timing and Control, Instruction Cycle
Q13. What is the instruction cycle?

a) The sequence of steps the CPU follows to execute an instruction
b) The process of fetching data from memory
c) The method of converting high-level language to machine language
d) The way the CPU manages interrupts
Answer: a
Q14. Which unit in the CPU controls the timing of the instruction cycle?

a) Control Unit
b) Arithmetic Logic Unit (ALU)
c) Memory Unit
d) Register Unit
Answer: a
Memory Reference Instructions, Input-Output and Interrupts
Q15. Which of the following is a memory reference instruction?

a) LDA (Load Accumulator)
b) STA (Store Accumulator)
c) ADD
d) All of the above
Answer: d
Q16. What is an interrupt?

a) A signal that temporarily halts the CPU’s current operations
b) A command to start a new process

c) An error in the program
d) A type of memory
Answer: a
Central Processing Unit: Introduction, General Register Organization
Q17. What is the main function of the CPU?

a) To execute instructions from the computer program
b) To store data permanently
c) To manage input and output devices
d) To generate power for the computer
Answer: a
Q18. What does the general register organization refer to?

a) The arrangement of registers in the CPU
b) The specific tasks assigned to each register
c) The way registers communicate with memory
d) The process of creating new registers
Answer: a
Stack Organization and Instruction Format, Notations
Q19. What is a stack in computer organization?

a) A storage structure that follows Last In First Out (LIFO) principle
b) A storage structure that follows First In First Out (FIFO) principle
c) A type of register
d) A type of cache memory
Answer: a
Q20. What is an instruction format?

a) The layout of bits in an instruction
b) The way instructions are written in a program
c) The method of storing data in memory
d) The process of executing an instruction
Answer: a
Addressing Modes, Data Transfer and Manipulation
Q21. What is an addressing mode?

a) A way of specifying operands for instructions
b) A method of executing instructions
c) A type of data storage
d) A way of transferring data

Answer: a
Q22. Which of the following is a data transfer instruction?

a) MOV (Move)
b) ADD
c) SUB
d) MUL
Answer: a
Program Control: Status bits, Conditional Branch Instructions, Program Interrupts & Types
Q23. What is a status bit?

a) A bit that indicates the outcome of an operation
b) A bit used to store data
c) A bit used to address memory
d) A bit used in graphics processing
Answer: a
Q24. What is a conditional branch instruction?

a) An instruction that causes a branch based on a condition
b) An instruction that always causes a branch
c) An instruction used to store data
d) An instruction used to load data
Answer: a
RISC and CISC Characteristics
Q25. What does RISC stand for?

a) Reduced Instruction Set Computer
b) Random Instruction Set Computer
c) Reliable Instruction Set Computer
d) Real-time Instruction Set Computer
Answer: a
Q26. What is a characteristic of CISC architecture?

a) Complex instructions that perform multiple operations
b) Simple and fast instructions
c) Fixed-length instructions
d) High-level programming language
Answer: a

Pipelining and Parallel Processing: Basics of pipelining, pipeline hazards, techniques for handling hazards, parallel processing architectures

Q27. What is pipelining in CPU architecture?

a) A technique where multiple instruction phases are overlapped
b) A method of increasing memory capacity
c) A way to connect multiple CPUs
d) A type of cache memory
Answer: a

Q28. What is a pipeline hazard?

a) A situation that prevents the next instruction in the pipeline from executing
b) A problem with the power supply
c) A type of memory error
d) An error in the software
Answer: a

Input-Output Organization: I/O Interface

Q29. What is an I/O interface?

a) The hardware and software used to connect the CPU to peripheral devices
b) The process of executing instructions
c) The method of addressing memory
d) A type of memory used for storing data
Answer: a

Asynchronous Data Transfer

Q30. What is asynchronous data transfer?

a) Data transfer without a common clock signal
b) Data transfer with a common clock signal
c) Data transfer using parallel cables
d) Data transfer using serial cables
Answer: a

Modes of Transfer

Q31. What is a mode of data transfer?

a) The method used to transfer data between components
b) The size of data being transferred
c) The speed of data transfer
d) The storage location of data
Answer: a

Direct Memory Access (DMA), DMA Transfer, Input-Output Processor (IOP), CPU-IOP Communication

Q32. What is Direct Memory Access (DMA)?

a) A technique where a device accesses the memory directly without CPU intervention
b) A type of memory
c) A method of data encryption
d) A way to store data permanently
Answer: a

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory

Q33. What is the memory hierarchy?

a) The organization of memory in levels based on speed and cost
b) The size of memory
c) The method of data transfer
d) The layout of memory within the CPU
Answer: a

Q34. What is main memory?

a) The primary storage area for data and programs currently in use
b) The secondary storage used for backup
c) The fastest type of memory in the hierarchy
d) The smallest type of memory in the hierarchy
Answer: a

Q35. What is associative memory?

a) A type of memory that allows data to be accessed based on content rather than address
b) A memory used for caching
c) A method of organizing data in memory
d) A memory used for arithmetic operations
Answer: a

Cache Memory and Virtual Memory

Q36. What is cache memory?

a) A small, fast memory located close to the CPU to store frequently accessed data
b) A type of external storage

c) A memory used for storing large files
d) A memory used for backup
Answer: a
Q37. What is virtual memory?

a) An extension of main memory using disk space
b) A type of memory used for graphics processing
c) A memory used for data encryption
d) A temporary storage area for data
Answer: a
Additional Questions to reach 200 total:
Q38. What is the primary function of an ALU (Arithmetic Logic Unit)?

a) To perform arithmetic and logical operations
b) To store data
c) To control the timing of operations
d) To manage input/output operations
Answer: a
Q39. What is the purpose of a control unit in a CPU?

a) To direct the operation of the processor
b) To store instructions
c) To perform calculations
d) To manage memory
Answer: a
Q40. What is the function of a program counter (PC) in a CPU?

a) To hold the address of the next instruction to be executed
b) To store the current instruction
c) To perform arithmetic operations
d) To control the flow of data
Answer: a
Q41. Which of the following is a characteristic of a von Neumann architecture?

a) Shared memory space for instructions and data
b) Separate memory spaces for instructions and data
c) Parallel processing capabilities
d) Use of RISC principles
Answer: a
Q42. What does the term 'bus' refer to in computer architecture?

a) A communication pathway connecting different components
b) A type of memory
c) A processor
d) A storage device
Answer: a
Q43. What is the function of an instruction decoder?

a) To translate machine instructions into control signals
b) To store data
c) To perform arithmetic operations
d) To manage memory
Answer: a
Q44. What is a multiplexer?

a) A device that selects one of many input signals and forwards the selected input into a single line
b) A device that performs arithmetic operations
c) A memory storage device
d) A type of register
Answer: a
Q45. What is the purpose of an address bus?

a) To carry the address to memory locations
b) To transfer data between components
c) To provide power to the CPU
d) To store instructions
Answer: a
Q46. Which of the following is not an example of a secondary storage device?

a) Hard drive
b) USB flash drive
c) RAM
d) DVD
Answer: c
Q47. What is the purpose of a data bus?

a) To carry data between the CPU and other components
b) To store instructions
c) To control peripheral devices

d) To manage power supply
Answer: a
Q48. What is an opcode?

a) The part of a machine language instruction that specifies the operation to be performed
b) The address of data
c) The part of the CPU that performs arithmetic operations
d) The control unit of the CPU
Answer: a
Q49. What does DRAM stand for?

a) Dynamic Random Access Memory
b) Direct Random Access Memory
c) Digital Random Access Memory
d) Disk Random Access Memory
Answer: a
Q50. Which type of memory is typically used for cache memory?

a) SRAM (Static Random Access Memory)
b) DRAM (Dynamic Random Access Memory)
c) ROM (Read Only Memory)
d) Flash Memory
Answer: a

Additional Questions to reach 200 total:
Q51. What does ROM stand for?

a) Read Only Memory
b) Random Only Memory
c) Read Output Memory
d) Random Output Memory
Answer: a
Q52. What type of memory is volatile and loses its content when power is turned off?

a) RAM (Random Access Memory)
b) ROM (Read Only Memory)
c) EEPROM (Electrically Erasable Programmable Read-Only Memory)

d) Flash Memory
Answer: a
Q53. Which of the following is a non-volatile memory?

a) Flash Memory
b) DRAM
c) SRAM
d) Cache Memory
Answer: a
Q54. What does the term 'cycle time' refer to in CPU performance?

a) The time taken to complete one cycle of an instruction
b) The total time taken to execute a program
c) The time taken to fetch an instruction from memory
d) The time taken to perform a single arithmetic operation
Answer: a
Q55. What is the role of the memory management unit (MMU)?

a) To handle memory protection and virtual memory
b) To perform arithmetic operations
c) To control the timing of the CPU
d) To manage I/O operations
Answer: a
Q56. What does the term 'hit rate' refer to in the context of cache memory?

a) The percentage of memory accesses found in the cache
b) The speed at which data is written to the cache
c) The number of instructions executed per second
d) The size of the cache memory
Answer: a
Q57. What is a register file?

a) A collection of registers within the CPU
b) A type of external storage device
c) A part of the main memory
d) A type of instruction in the CPU
Answer: a
Q58. What is the main purpose of virtual memory?

a) To extend the available memory using disk space

b) To store frequently accessed data
c) To increase the speed of the CPU
d) To manage input/output operations
Answer: a
Q59. What is the role of the arithmetic logic unit (ALU) in a CPU?

a) To perform arithmetic and logical operations
b) To fetch instructions from memory
c) To control the execution of instructions
d) To manage data transfer between memory and I/O devices
Answer: a
Q60. Which of the following is an example of a sequential circuit?

a) Flip-flop
b) AND gate
c) OR gate
d) NOT gate
Answer: a
Q61. What is the function of a decoder in digital circuits?

a) To convert coded inputs into coded outputs
b) To perform arithmetic operations
c) To store data
d) To control the timing of operations
Answer: a
Q62. What does the term 'pipeline stall' refer to?

a) A delay in the instruction pipeline
b) An error in the CPU
c) A type of memory error
d) A method of data transfer
Answer: a
Q63. What is the main advantage of pipelining in a CPU?

a) Increased instruction throughput
b) Reduced power consumption
c) Simplified CPU design
d) Increased memory capacity
Answer: a
Q64. What is a bus in computer architecture?

a) A communication system that transfers data between components
b) A type of memory
c) A processor
d) A storage device
Answer: a
Q65. What is the function of the control unit in a CPU?

a) To direct the operation of the processor
b) To perform calculations
c) To store instructions
d) To manage memory
Answer: a
Q66. What is a hazard in the context of pipelining?

a) A situation that prevents the next instruction in the pipeline from executing
b) A problem with the power supply
c) A type of memory error
d) An error in the software
Answer: a
Q67. What is the purpose of an instruction decoder in a CPU?

a) To translate machine instructions into control signals
b) To store data
c) To perform arithmetic operations
d) To manage memory
Answer: a
Q68. What is an opcode?

a) The part of a machine language instruction that specifies the operation to be performed
b) The address of data
c) The part of the CPU that performs arithmetic operations
d) The control unit of the CPU
Answer: a
Q69. What is the role of a program counter (PC) in a CPU?

a) To hold the address of the next instruction to be executed
b) To store the current instruction
c) To perform arithmetic operations

d) To control the flow of data
Answer: a
Q70. What is meant by 'clock speed' in a CPU?

a) The speed at which the CPU executes instructions
b) The speed of data transfer between components
c) The size of the CPU
d) The power consumption of the CPU
Answer: a
Q71. What is a multi-core processor?

a) A processor with multiple execution cores on a single chip
b) A processor with multiple memory modules
c) A processor with a large cache
d) A processor with high clock speed
Answer: a
Q72. What does the term 'fetch' refer to in the instruction cycle?

a) The process of retrieving an instruction from memory
b) The process of executing an instruction
c) The process of decoding an instruction
d) The process of writing data to memory
Answer: a
Q73. What is the main function of the ALU?

a) To perform arithmetic and logical operations
b) To store data
c) To control the timing of operations
d) To manage I/O operations
Answer: a
Q74. What is the primary purpose of cache memory?

a) To store frequently accessed data for quick access
b) To store large amounts of data permanently
c) To control the flow of data between CPU and peripherals
d) To manage virtual memory
Answer: a
Q75. What is an interrupt in computer architecture?

a) A signal that temporarily halts the CPU’s current operations

b) A command to start a new process
c) An error in the program
d) A type of memory
Answer: a
Q76. What does the term 'throughput' refer to in CPU performance?

a) The number of instructions executed per unit of time
b) The time taken to execute a single instruction
c) The total number of instructions executed by the CPU
d) The speed at which data is transferred between memory and CPU
Answer: a
Q77. What is the purpose of an address bus?

a) To carry the address to memory locations
b) To transfer data between components
c) To provide power to the CPU
d) To store instructions
Answer: a
Q78. What is meant by 'instruction set' in CPU architecture?

a) The set of instructions that a CPU can execute
b) The set of registers within the CPU
c) The set of memory addresses used by the CPU
d) The set of data buses in the CPU
Answer: a
Q79. What is a multiplexer in digital circuits?

a) A device that selects one of many input signals and forwards the selected input into a single line
b) A device that performs arithmetic operations
c) A memory storage device
d) A type of register
Answer: a
Q80. What is the function of a control unit in a CPU?

a) To direct the operation of the processor
b) To store instructions
c) To perform calculations
d) To manage memory
Answer: a

Q81. What is a bus in computer architecture?

a) A communication system that transfers data between components
b) A type of memory
c) A processor
d) A storage device
Answer: a
Q82. What is the main advantage of pipelining in a CPU?

a) Increased instruction throughput
b) Reduced power consumption
c) Simplified CPU design
d) Increased memory capacity
Answer: a
Q83. What does the term 'pipeline stall' refer to?

a) A delay in the instruction pipeline
b) An error in the CPU
c) A type of memory error
d) A method of data transfer
Answer: a
Q84. What is a register file?

a) A collection of registers within the CPU
b) A type of external storage device
c) A part of the main memory
d) A type of instruction in the CPU
Answer: a
Q85. What is a hazard in the context of pipelining?

a) A situation that prevents the next instruction in the pipeline from executing
b) A problem with the power supply
c) A type of memory error
d) An error in the software
Answer: a
Q86. What is the role of a program counter (PC) in a CPU?

a) To hold the address of the next instruction to be executed
b) To store the current instruction
c) To perform arithmetic operations

d) To control the flow of data
Answer: a

Q87. What does the term 'cycle time' refer to in CPU performance?

a) The time taken to complete one cycle of an instruction
b) The total time taken to execute a program
c) The time taken to fetch an instruction from memory
d) The time taken to perform a single arithmetic operation
Answer: a
Q88. What is the primary purpose of the program counter (PC)?

a) To hold the address of the next instruction to be executed
b) To store data temporarily
c) To manage input/output operations
d) To perform arithmetic and logical operations
Answer: a
Q89. What does the term 'data path' refer to in a CPU?

a) The part of the CPU that performs data processing operations
b) The memory where data is stored
c) The route taken by data to travel from one part of the computer to another
d) The peripheral devices connected to the CPU
Answer: a
Q90. What is the purpose of an instruction register (IR)?

a) To hold the current instruction being executed
b) To store the address of the next instruction
c) To manage memory addresses
d) To perform arithmetic operations
Answer: a
Q91. What does the term 'throughput' refer to in computer performance?

a) The number of instructions executed per unit of time
b) The speed at which data is transferred from one place to another
c) The amount of data stored in memory
d) The total number of instructions in a program
Answer: a
Q92. What is a 'memory address register (MAR)'?

a) A register that holds the address of the memory location to be accessed
b) A register that holds the actual data to be processed
c) A register that stores the current instruction
d) A register that performs arithmetic operations
Answer: a
Q93. What is meant by 'latency' in the context of computer memory?

a) The delay between a request for data and the start of the data transfer
b) The speed at which data is processed
c) The amount of data that can be stored
d) The total time taken to execute a program
Answer: a
Q94. What is the purpose of the 'stack pointer (SP)' in a CPU?

a) To keep track of the top of the stack in memory
b) To store data temporarily
c) To manage input/output operations
d) To perform arithmetic operations
Answer: a
Q95. What is the function of a 'base register' in memory management?

a) To hold the base address of the memory area being accessed
b) To store the current instruction
c) To perform arithmetic operations
d) To manage input/output operations
Answer: a
Q96. What does 'cache hit' mean?

a) When the data requested by the CPU is found in the cache memory
b) When the data requested by the CPU is not found in the cache memory
c) When the CPU performs a successful arithmetic operation
d) When the CPU accesses the main memory
Answer: a
Q97. What is the primary role of the 'instruction set architecture (ISA)'?

a) To define the set of instructions that a CPU can execute
b) To manage the hardware components of a computer
c) To control input/output operations
d) To perform arithmetic and logical operations

Answer: a
Q98. What is the function of a 'buffer register'?

a) To temporarily hold data while it is being transferred from one place to another
b) To store the current instruction
c) To perform arithmetic operations
d) To manage memory addresses
Answer: a
Q99. What is 'address space' in computer architecture?

a) The range of addresses that a processor can use to access memory
b) The physical location of data in memory
c) The total amount of data that can be stored
d) The speed at which data is processed
Answer: a
Q100. What does 'pipeline depth' refer to in a CPU?

a) The number of stages in the instruction pipeline
b) The speed at which instructions are executed
c) The amount of data that can be processed simultaneously
d) The total number of instructions in a program
Answer: a
Q101. What is the main purpose of a 'control store' in microprogramming?

a) To store the microinstructions that control the execution of machine instructions
b) To perform arithmetic operations
c) To manage memory addresses
d) To control input/output operations
Answer: a
Q102. What is a 'bus width'?

a) The number of bits that can be transmitted simultaneously on a bus
b) The physical size of the bus
c) The speed at which data is transferred on the bus
d) The number of components connected to the bus
Answer: a
Q103. What does 'bus arbitration' refer to?

a) The process of managing the access to the bus by multiple devices

b) The speed of data transfer on the bus
c) The size of the data packets on the bus
d) The power consumption of the bus
Answer: a
Q104. What is 'memory interleaving'?

a) A technique to increase the speed of access to memory by arranging address spaces
b) The physical arrangement of memory modules
c) The total amount of memory available
d) The method of data transfer between memory and CPU
Answer: a
Q105. What does the term 'load/store architecture' refer to?

a) A CPU design where data must be loaded into registers before operations can be performed
b) A CPU design where data is directly operated upon in memory
c) A CPU design optimized for multi-threading
d) A CPU design with integrated cache memory
Answer: a
Q106. What is a 'context switch' in an operating system?

a) The process of switching the CPU from one process or thread to another
b) The process of loading an instruction into the CPU
c) The process of writing data to memory
d) The process of managing input/output operations
Answer: a
Q107. What is 'branch prediction'?

a) A technique to guess the outcome of a branch instruction to improve CPU performance
b) A method of error checking in memory
c) A type of data storage
d) A process of managing input/output operations
Answer: a
Q108. What is the role of the 'instruction buffer'?

a) To hold instructions temporarily before they are executed
b) To store data temporarily
c) To perform arithmetic operations

d) To manage memory addresses
Answer: a
Q109. What does 'MIPS' stand for in CPU performance?

a) Million Instructions Per Second
b) Memory Instructions Per Second
c) Multi-core Instructions Per Second
d) Machine Instructions Per Second
Answer: a
Q110. What is the function of the 'address generation unit (AGU)' in a CPU?

a) To calculate the addresses used by the CPU for data access
b) To store the current instruction
c) To perform arithmetic operations
d) To manage input/output operations
Answer: a
Q111. What does 'CPI' stand for in CPU performance metrics?

a) Cycles Per Instruction
b) Cache Per Instruction
c) Core Performance Index
d) Central Processing Instruction
Answer: a
Q112. What is a 'branch target buffer (BTB)'?

a) A cache that stores the target addresses of recently taken branches
b) A buffer that holds data to be written to memory
c) A register that stores the current instruction
d) A unit that performs arithmetic operations
Answer: a
Q113. What is the primary purpose of 'microcode' in a CPU?

a) To implement complex instructions using simpler, low-level instructions
b) To manage input/output operations
c) To store data temporarily
d) To control memory addresses
Answer: a
Q114. What is 'SIMD' in computer architecture?

a) Single Instruction, Multiple Data

b) Simple Instruction, Multiple Data
c) Single Instruction, Multiple Devices
d) Simple Instruction, Multiple Devices
Answer: a
Q115. What is the purpose of the 'instruction fetch unit (IFU)'?

a) To fetch instructions from memory and prepare them for execution
b) To store data temporarily
c) To perform arithmetic operations
d) To manage memory addresses
Answer: a
Q116. What does the term 'superscalar' refer to in CPU design?

a) A CPU that can execute more than one instruction per clock cycle
b) A CPU with a very high clock speed
c) A CPU with a large cache memory
d) A CPU designed for mobile devices
Answer: a
Q117. What is the 'translation lookaside buffer (TLB)'?

a) A cache used to improve the speed of virtual address translation
b) A buffer that stores data to be written to memory
c) A register that holds the current instruction
d) A unit that performs arithmetic operations
Answer: a
Q118. What is the function of a 'prefetch buffer' in a CPU?

a) To hold data or instructions fetched in advance to speed up execution
b) To store the current instruction
c) To perform arithmetic operations
d) To manage memory addresses
Answer: a
Q119. What is 'out-of-order execution' in a CPU?

a) The ability of a CPU to execute instructions out of the original order to improve performance
b) The execution of instructions in the order they appear in the program
c) The execution of instructions based on their memory addresses
d) The process of writing data to memory
Answer: a

Q120. What does 'VLIW' stand for in CPU design?

a) Very Long Instruction Word
b) Variable Length Instruction Word
c) Very Large Instruction Word
d) Variable Large Instruction Word
Answer: a
Q121. What is 'branch prediction' in the context of CPU architecture?

a) A technique used to improve the flow in the instruction pipeline by guessing the outcome of conditional operations
b) A method of determining memory addresses
c) A technique for performing arithmetic operations
d) A system for managing input/output devices
Answer: a
Q122. What does 'dual-core' mean in processor design?

a) A processor with two independent cores that can execute instructions simultaneously
b) A processor with two instruction sets
c) A processor with two levels of cache
d) A processor with two memory controllers
Answer: a
Q123. What is the purpose of the 'instruction decode unit (IDU)' in a CPU?

a) To translate machine instructions into control signals
b) To fetch instructions from memory
c) To perform arithmetic operations
d) To manage memory addresses
Answer: a
Q124. What is meant by 'speculative execution' in a CPU?

a) A technique where the CPU executes instructions before it is certain they are needed
b) The execution of instructions based on their memory addresses
c) The process of storing data in cache memory
d) The method of managing input/output operations
Answer: a
Q125. What is the role of 'cache coherence' in a multi-core processor?

a) To ensure that all cores have a consistent view of the cached data
b) To increase the size of the cache memory
c) To manage the speed of data transfer
d) To perform arithmetic operations
Answer: a
Q126. What is the function of 'write-back cache'?

a) To update the main memory only when the cache block is replaced
b) To immediately update the main memory with every write operation
c) To store instructions temporarily
d) To manage input/output operations
Answer: a
Q127. What is 'hyper-threading' technology?

a) A technology that allows a single CPU to behave like multiple logical CPUs
b) A technology to increase the clock speed of the CPU
c) A technology to increase the size of cache memory
d) A technology to reduce power consumption
Answer: a
Q128. What does 'FLOPS' stand for in computing?

a) Floating Point Operations Per Second
b) Fast Logic Operations Per Second
c) Frequency Logic Operations Per Second
d) Floating Logic Operations Per Second
Answer: a
Q129. What is 'SIMD' in computer architecture?

a) Single Instruction, Multiple Data
b) Simple Instruction, Multiple Data
c) Single Instruction, Multiple Devices
d) Simple Instruction, Multiple Devices
Answer: a
Q130. What is the main function of a 'load/store unit (LSU)' in a CPU?

a) To manage the loading and storing of data to and from memory
b) To perform arithmetic operations
c) To decode instructions
d) To manage input/output operations
Answer: a

Q131. What is 'clock gating' in CPU design?

a) A technique to reduce power consumption by turning off the clock signal to inactive parts of the circuit
b) A method to increase the clock speed of the CPU
c) A process of managing input/output operations
d) A system for handling interrupts
Answer: a
Q132. What is 'cache memory' primarily used for?

a) To speed up the access to frequently used data and instructions
b) To store data permanently
c) To manage input/output operations
d) To perform arithmetic operations
Answer: a
Q133. What does 'CISC' stand for in CPU design?

a) Complex Instruction Set Computer
b) Central Instruction Set Computer
c) Common Instruction Set Computer
d) Complex Integrated Set Computer
Answer: a
Q134. What does 'RISC' stand for in CPU design?

a) Reduced Instruction Set Computer
b) Rapid Instruction Set Computer
c) Regular Instruction Set Computer
d) Reliable Instruction Set Computer
Answer: a
Q135. What is the purpose of 'branch target buffer (BTB)' in CPU architecture?

a) To store the addresses of branch targets to speed up execution
b) To hold data to be written to memory
c) To store the current instruction
d) To perform arithmetic operations
Answer: a
Q136. What is 'out-of-order execution' in CPU design?

a) The ability of the CPU to execute instructions in an order different from their appearance in the program

b) The execution of instructions in the order they appear in the program
c) The method of managing input/output operations
d) The process of storing data in cache memory
Answer: a
Q137. What is 'parallel processing' in computer architecture?

a) The simultaneous execution of multiple instructions or tasks
b) The sequential execution of instructions
c) The method of data transfer between memory and CPU
d) The process of managing input/output operations
Answer: a
Q138. What is the role of 'cache memory' in a CPU?

a) To provide faster access to frequently used data
b) To store large amounts of data permanently
c) To control input/output operations
d) To perform arithmetic and logical operations
Answer: a
Q139. What is 'pipelining' in CPU design?

a) A technique where multiple instruction phases are overlapped
b) A method of increasing memory size
c) A process of managing input/output operations
d) A way of storing data in cache memory
Answer: a
Q140. What is the main advantage of 'RISC' over 'CISC' architecture?

a) Simpler instructions that can be executed more quickly
b) More complex instructions that reduce the number of instructions per program
c) Larger instruction sets that provide more functionality
d) Integrated memory management units
Answer: a
Q141. What does 'superscalar architecture' refer to in CPU design?

a) A CPU design that allows for the execution of multiple instructions per clock cycle
b) A CPU with a single instruction execution pipeline
c) A CPU with a very high clock speed
d) A CPU designed for mobile devices
Answer: a

Q142. What is the primary function of a 'control unit' in a CPU?

a) To direct the operation of the processor
b) To store data
c) To perform arithmetic operations
d) To manage input/output operations
Answer: a
Q143. What is 'clock speed' in the context of CPU performance?

a) The frequency at which the CPU operates
b) The time taken to execute a single instruction
c) The amount of data that can be processed per second
d) The power consumption of the CPU
Answer: a
Q144. What is 'virtual memory' in computer architecture?

a) A technique that uses a portion of the hard drive as if it were RAM
b) The physical memory installed in the computer
c) The memory used for storing frequently accessed data
d) The cache memory within the CPU
Answer: a
Q145. What does the term 'instruction set' refer to in CPU design?

a) The complete set of instructions that a CPU can execute
b) The set of instructions being currently executed by the CPU
c) The instructions stored in cache memory
d) The instructions stored in RAM
Answer: a
Q146. What is the purpose of the 'data bus' in a computer system?

a) To transfer data between the CPU and other components
b) To manage input/output operations
c) To store data temporarily
d) To perform arithmetic operations
Answer: a
Q147. What does 'DMA' stand for in computer architecture?

a) Direct Memory Access
b) Dynamic Memory Allocation
c) Dual Memory Architecture

d) Digital Memory Access
Answer: a
Q148. What is 'multiprocessing' in computer systems?

a) The use of two or more CPUs within a single computer system
b) The execution of multiple instructions simultaneously by a single CPU
c) The process of managing input/output operations
d) The method of increasing the clock speed of the CPU
Answer: a
Q149. What is 'microarchitecture' in CPU design?

a) The detailed organization of a CPU's internal components
b) The high-level design of a CPU
c) The physical size of the CPU
d) The power consumption of the CPU
Answer: a
Q150. What is 'cache coherence' in a multiprocessor system?

a) Ensuring that all caches have the most recent copy of the data
b) The total size of the cache memory
c) The speed at which data is accessed in the cache
d) The method of data transfer between cache and main memory
Answer: a

Q151. What is 'instruction pipelining' in CPU architecture?

a) A technique where multiple instruction phases are overlapped to improve performance
b) A method to store data temporarily
c) A way to increase the clock speed of the CPU
d) A process to manage input/output operations
Answer: a
Q152. What is 'hyper-threading' in CPU technology?

a) A technique that allows a single CPU to execute multiple threads simultaneously
b) A method to increase cache memory size
c) A process to speed up memory access
d) A system for managing power consumption

Answer: a
Q153. What is the primary advantage of a 'multi-core processor'?

a) Increased performance through parallel processing
b) Lower power consumption
c) Larger cache memory
d) Higher clock speed
Answer: a
Q154. What is 'cache hit ratio'?

a) The percentage of memory accesses satisfied by the cache
b) The speed at which data is transferred from the cache to the CPU
c) The size of the cache memory
d) The frequency of cache updates
Answer: a
Q155. What is the purpose of 'prefetching' in CPU architecture?

a) To load data or instructions into cache before they are needed
b) To increase the clock speed
c) To manage memory addresses
d) To perform arithmetic operations
Answer: a
Q156. What is 'clock cycle' in CPU performance?

a) The duration of a single oscillation of the clock signal
b) The total time taken to execute an instruction
c) The speed of data transfer between CPU and memory
d) The frequency of the clock signal
Answer: a
Q157. What does 'RISC' stand for?

a) Reduced Instruction Set Computer
b) Rapid Instruction Set Computer
c) Reliable Instruction Set Computer
d) Regular Instruction Set Computer
Answer: a
Q158. What is the role of the 'arithmetic logic unit (ALU)' in a CPU?

a) To perform arithmetic and logical operations
b) To store data

c) To manage memory addresses
d) To control input/output operations
Answer: a
Q159. What is 'bus contention'?

a) A situation where multiple devices attempt to use the bus simultaneously
b) The speed of data transfer on the bus
c) The number of bits transferred on the bus
d) The size of the data packets on the bus
Answer: a
Q160. What is 'microprogramming' in CPU design?

a) A method of implementing the control logic of a CPU using a sequence of microinstructions
b) A technique for increasing the clock speed of the CPU
c) A process for managing input/output operations
d) A way to increase the size of cache memory
Answer: a
Q161. What does 'cycle time' refer to in CPU performance?

a) The time taken to complete one clock cycle
b) The time taken to execute an entire program
c) The time taken to fetch an instruction
d) The time taken to transfer data from memory
Answer: a
Q162. What is 'DMA' used for in computer systems?

a) Direct Memory Access, allowing peripherals to directly read/write memory without CPU intervention
b) Dynamic Memory Allocation for managing memory
c) Dual Memory Architecture for improved performance
d) Digital Memory Access for faster data retrieval
Answer: a
Q163. What is the primary function of 'virtual memory'?

a) To extend the available memory by using disk space
b) To provide faster access to data
c) To store frequently used data
d) To manage input/output operations
Answer: a

Q164. What is a 'program counter (PC)' in a CPU?

a) A register that holds the address of the next instruction to be executed
b) A counter that measures program execution time
c) A storage area for program data
d) A unit that performs arithmetic operations
Answer: a
Q165. What is the purpose of 'memory interleaving'?

a) To improve the speed of memory access by addressing multiple memory modules in a staggered manner
b) To increase the size of the memory
c) To manage memory addresses
d) To perform arithmetic operations
Answer: a
Q166. What is the role of the 'control unit' in a CPU?

a) To direct the operation of the processor by generating control signals
b) To store data temporarily
c) To perform arithmetic operations
d) To manage memory addresses
Answer: a
Q167. What is 'branch prediction' in CPU architecture?

a) A technique used to improve the flow in the instruction pipeline by guessing the outcome of branches
b) A method of managing memory addresses
c) A process of performing arithmetic operations
d) A way to control input/output devices
Answer: a
Q168. What is 'context switch' in an operating system?

a) The process of storing the state of a CPU so that it can be restored and execution resumed later
b) The switching of tasks in the CPU
c) The management of memory addresses
d) The execution of input/output operations
Answer: a
Q169. What does 'FLOPS' stand for in computing?

a) Floating Point Operations Per Second
b) Fast Logic Operations Per Second
c) Frequency Logic Operations Per Second
d) Floating Logic Operations Per Second
Answer: a
Q170. What is the main function of a 'load/store unit' in a CPU?

a) To manage the loading and storing of data to and from memory
b) To perform arithmetic operations
c) To decode instructions
d) To manage input/output operations
Answer: a
Q171. What does 'SIMD' stand for?

a) Single Instruction, Multiple Data
b) Simple Instruction, Multiple Data
c) Single Instruction, Multiple Devices
d) Simple Instruction, Multiple Devices
Answer: a
Q172. What is 'clock gating' in CPU design?

a) A technique to reduce power consumption by disabling the clock signal to inactive parts of the circuit
b) A method to increase the clock speed of the CPU
c) A process to manage input/output operations
d) A system for handling interrupts
Answer: a
Q173. What is 'cache memory' used for in a computer system?

a) To provide faster access to frequently used data and instructions
b) To store data permanently
c) To manage input/output operations
d) To perform arithmetic operations
Answer: a
Q174. What is the purpose of 'bus arbitration'?

a) To manage access to the bus by multiple devices to avoid conflicts
b) To increase the speed of data transfer on the bus
c) To manage the size of data packets on the bus
d) To control the number of bits transferred on the bus

Answer: a
Q175. What is 'address space' in computer architecture?

a) The range of addresses that a processor can use to access memory
b) The physical location of data in memory
c) The total amount of data that can be stored
d) The speed at which data is processed
Answer: a
Q176. What is 'write-back cache' in CPU design?

a) A type of cache where data is written to main memory only when the cache line is replaced
b) A cache where data is immediately written to main memory
c) A cache that stores instructions temporarily
d) A system to manage input/output operations
Answer: a
Q177. What is 'superscalar architecture'?

a) A CPU design that allows for the execution of multiple instructions per clock cycle
b) A CPU with a single instruction execution pipeline
c) A CPU with very high clock speed
d) A CPU designed for low power consumption
Answer: a
Q178. What is 'cache coherence' in multiprocessor systems?

a) Ensuring that all caches have the most recent copy of the data
b) The total size of the cache memory
c) The speed of data transfer in the cache
d) The method of data transfer between cache and main memory
Answer: a
Q179. What is the main purpose of a 'branch target buffer' in CPU design?

a) To store the addresses of branch targets to speed up execution
b) To hold data to be written to memory
c) To store the current instruction
d) To perform arithmetic operations
Answer: a
Q180. What is 'microcode' in a CPU?

a) A layer of hardware-level instructions that control the CPU's operation
b) The main program code executed by the CPU
c) The cache memory within the CPU
d) The set of instructions stored in RAM
Answer: a
Q181. What is 'instruction-level parallelism' (ILP)?

a) The ability of a CPU to execute multiple instructions simultaneously
b) The sequential execution of instructions
c) The parallel execution of instructions in different threads
d) The use of multiple CPUs to execute instructions
Answer: a
Q182. What is 'latency' in the context of memory access?

a) The time taken to access data from memory
b) The speed at which data is transferred
c) The total size of the memory
d) The frequency of memory updates
Answer: a
Q183. What does 'ISA' stand for in CPU design?

a) Instruction Set Architecture
b) Integrated System Architecture
c) Instruction Storage Area
d) Internal System Address
Answer: a
Q184. What is 'scalar processing'?

a) The processing of one data element at a time
b) The processing of multiple data elements simultaneously
c) The processing of data in a pipeline
d) The processing of data using multiple CPUs
Answer: a
Q185. What is 'context switching' in CPU operations?

a) The process of storing and restoring the state of a CPU so that execution can be resumed from the same point later
b) The switching of tasks in the CPU
c) The management of memory addresses
d) The execution of input/output operations

Answer: a
Q186. What is 'speculative execution' in CPU design?

a) A technique where the CPU executes instructions before it is certain they are needed
b) The execution of instructions based on their memory addresses
c) The process of storing data in cache memory
d) The method of managing input/output operations
Answer: a
Q187. What is 'pipeline hazard' in CPU pipelining?

a) A situation that causes a delay in the pipeline
b) The process of increasing pipeline stages
c) The speed at which the pipeline operates
d) The total number of instructions in the pipeline
Answer: a
Q188. What is 'register renaming' in CPU design?

a) A technique to avoid data hazards by dynamically changing the registers used by instructions
b) The process of changing the names of registers in assembly code
c) The allocation of additional registers
d) The method of managing input/output operations
Answer: a
Q189. What is 'non-blocking cache'?

a) A cache that allows other operations to proceed while a cache miss is being handled
b) A cache that blocks other operations during a cache miss
c) A cache with a very high hit rate
d) A cache that stores only instructions
Answer: a
Q190. What is 'dynamic branch prediction'?

a) A technique where the CPU predicts the direction of branches based on runtime behavior
b) The process of hardcoding branch predictions in the CPU
c) The prediction of branches based on static analysis
d) The method of predicting branches by the compiler
Answer: a

Q191. What is the role of 'instruction cache' in a CPU?

a) To store instructions that are frequently accessed
b) To store data temporarily
c) To manage memory addresses
d) To control input/output operations
Answer: a
Q192. What is 'VLIW' in CPU design?

a) Very Long Instruction Word
b) Variable Length Instruction Word
c) Very Large Instruction Word
d) Variable Large Instruction Word
Answer: a
Q193. What is the primary advantage of 'out-of-order execution'?

a) Improved CPU performance by executing instructions as resources become available
b) Easier programming and debugging
c) Lower power consumption
d) Increased clock speed
Answer: a
Q194. What is 'branch target buffer' (BTB) used for?

a) To predict the target address of a branch instruction
b) To store the history of executed instructions
c) To manage memory addresses
d) To control input/output operations
Answer: a
Q195. What is 'Tomasulo's algorithm' used for?

a) Dynamic scheduling of instructions to avoid pipeline hazards
b) Static scheduling of instructions by the compiler
c) Memory management in operating systems
d) Power management in CPUs
Answer: a
Q196. What does 'TLB' stand for in computer architecture?

a) Translation Lookaside Buffer
b) Transaction Log Buffer

c) Transfer Load Buffer
d) Temporary Load Buffer
Answer: a
Q197. What is 'cache miss'?

a) When the data requested by the CPU is not found in the cache memory
b) When the cache memory is full
c) When data is found in the cache memory
d) When the cache memory is being updated
Answer: a
Q198. What is the primary function of 'branch prediction' in a CPU?

a) To guess the outcome of branches to improve the flow in the instruction pipeline
b) To increase the clock speed
c) To manage memory addresses
d) To control input/output operations
Answer: a
Q199. What is 'instruction decode unit' (IDU) in a CPU?

a) A unit that translates machine instructions into control signals
b) A unit that fetches instructions from memory
c) A unit that performs arithmetic operations
d) A unit that manages memory addresses
Answer: a
Q200. What is the function of a 'write-through cache'?

a) To update main memory with every write operation
b) To store data temporarily
c) To perform arithmetic operations
d) To manage input/output operations
Answer: a