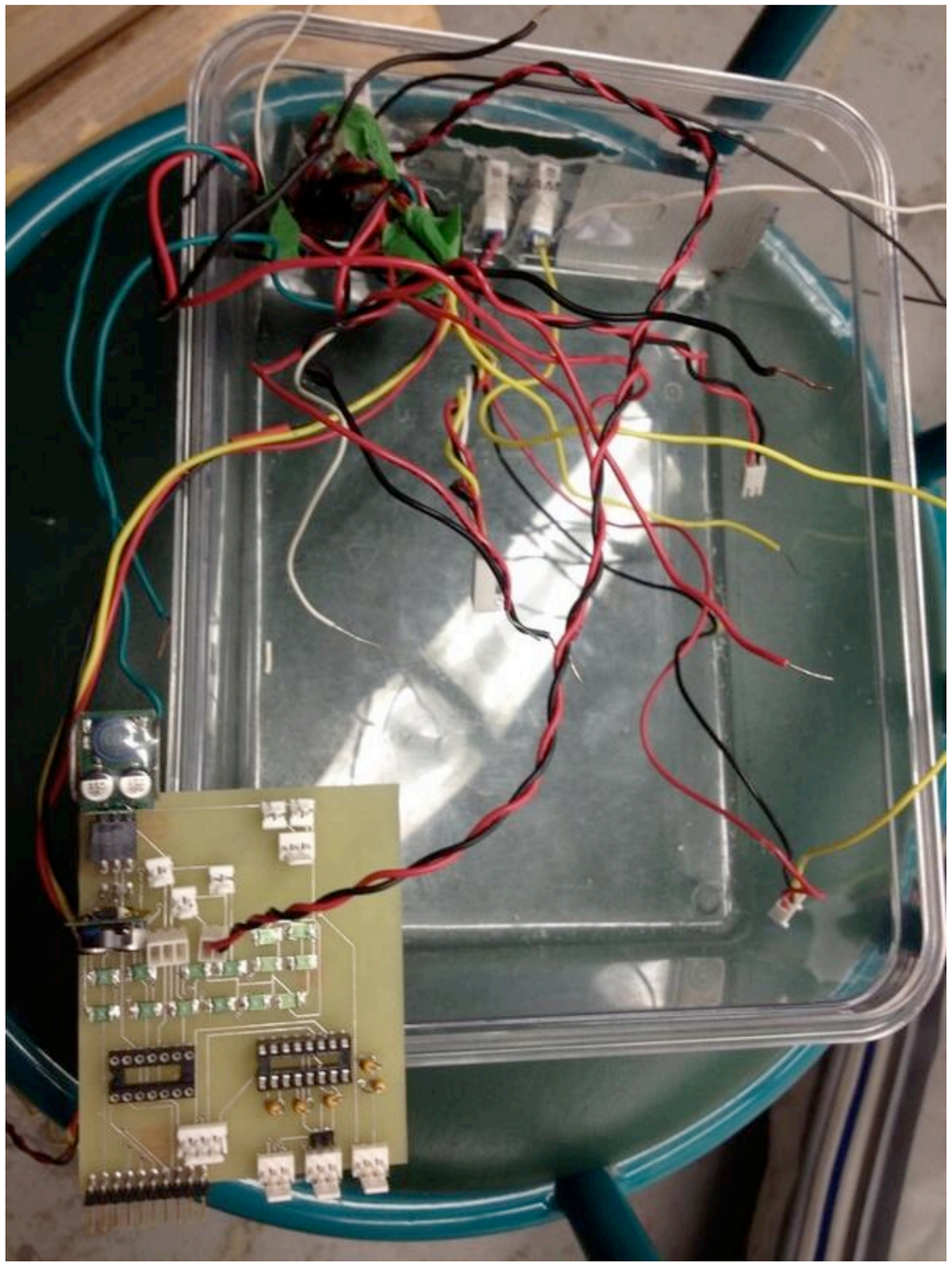
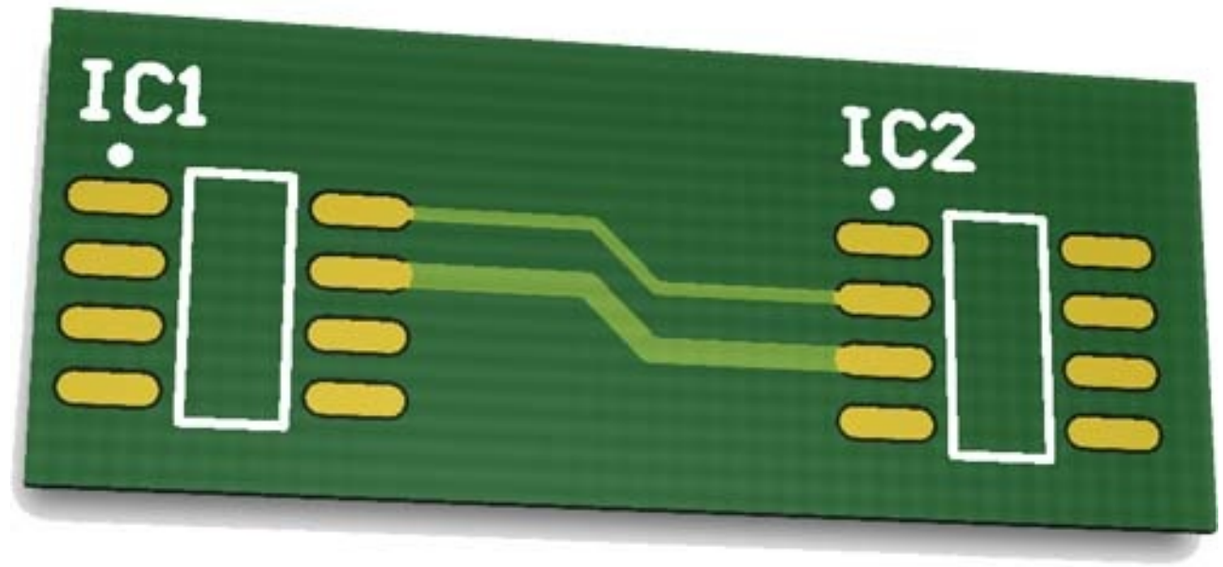
Electronic design - some practicalities

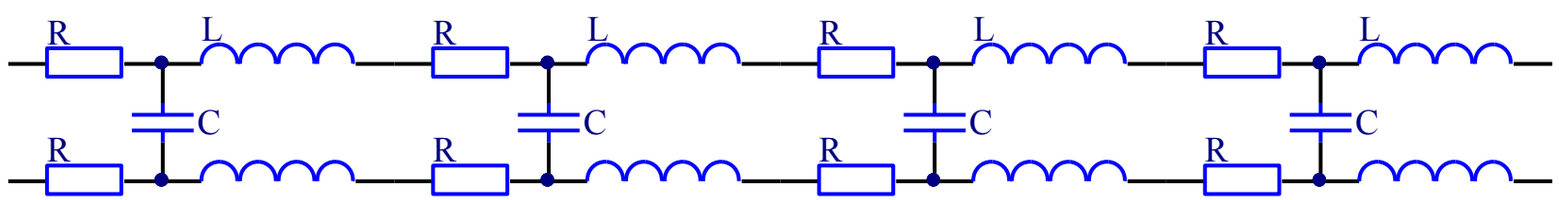
- R, L, C & PCBs - non-ideal behaviour
- opamps
- power management
- I2C
- packages
- DACs
- loading
- spectrum analyser
- bypass C, filters



PCB tracks & layout

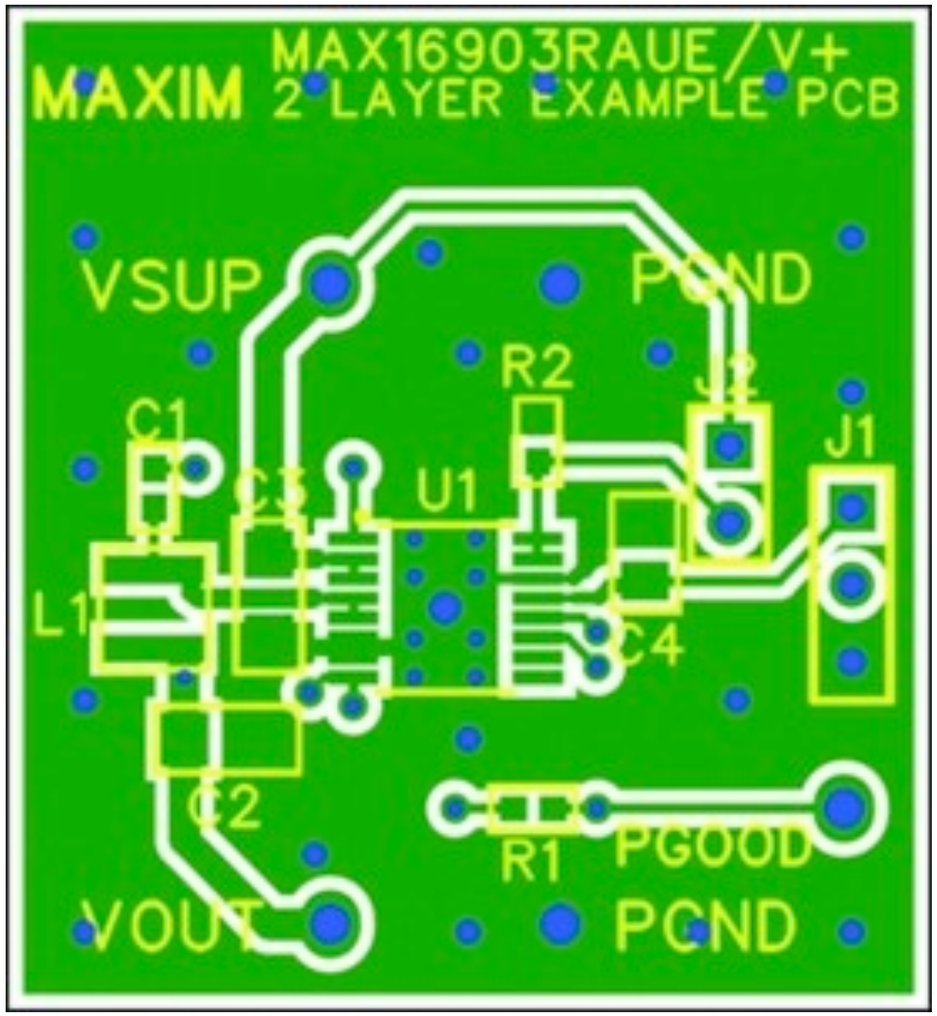
- not zero Ohms, zero Farads, zero Henrys





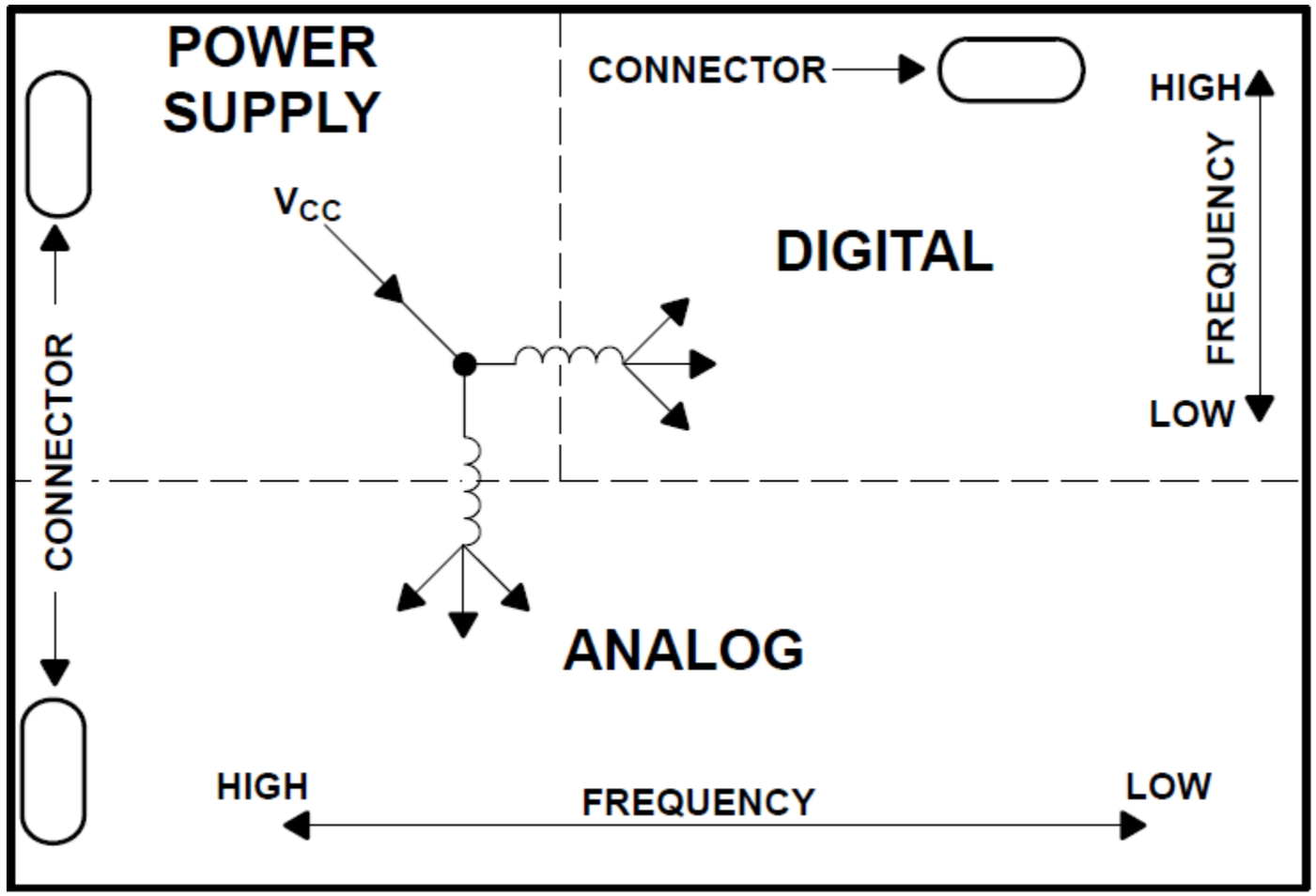
PCB tracks & layout

- So,
- generous track width
- route power intelligently
- close to ground, away from data, small signal
- use groundplanes - sustainability, EMI, EMR

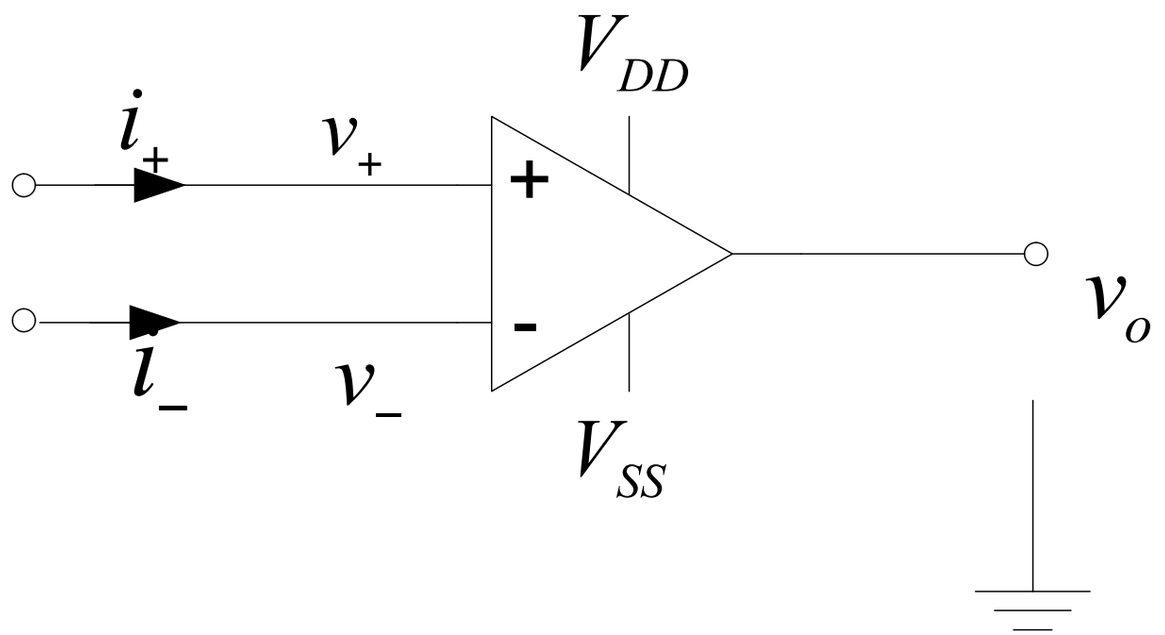


PCB tracks & layout

- Cluster functional elements
- ‘Star’ grounding avoids ground loops



Ideal Op Amp



$$V_{SS} < v_0 < +V_{DD}$$

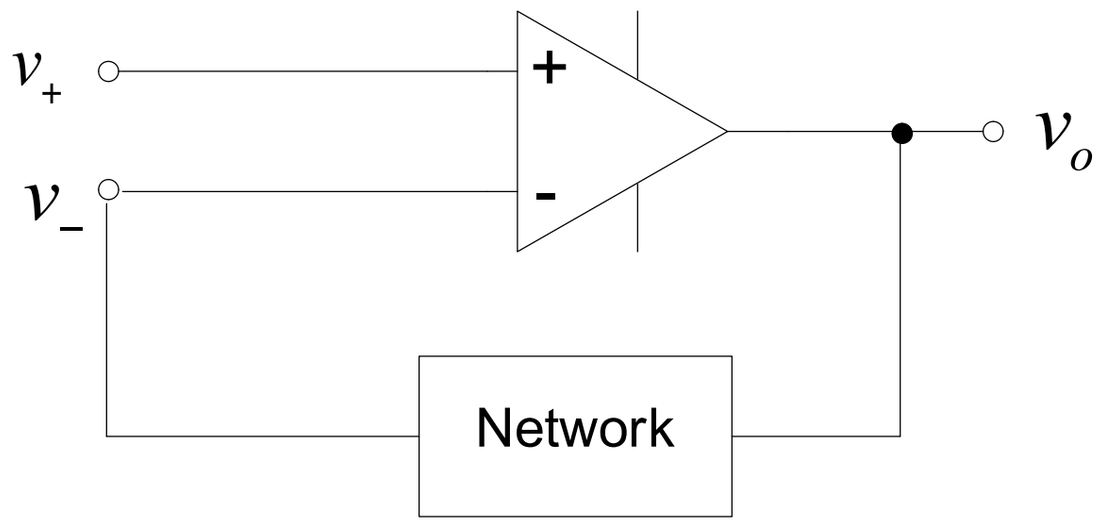
1) $v_0 = A_v \left(v_+ - v_- \right)$

The open-loop gain, A_v, is very large, approaching infinity.

2) $i_+ = i_- = 0$

The current into the inputs are zero.

Ideal Op Amp with Negative Feedback

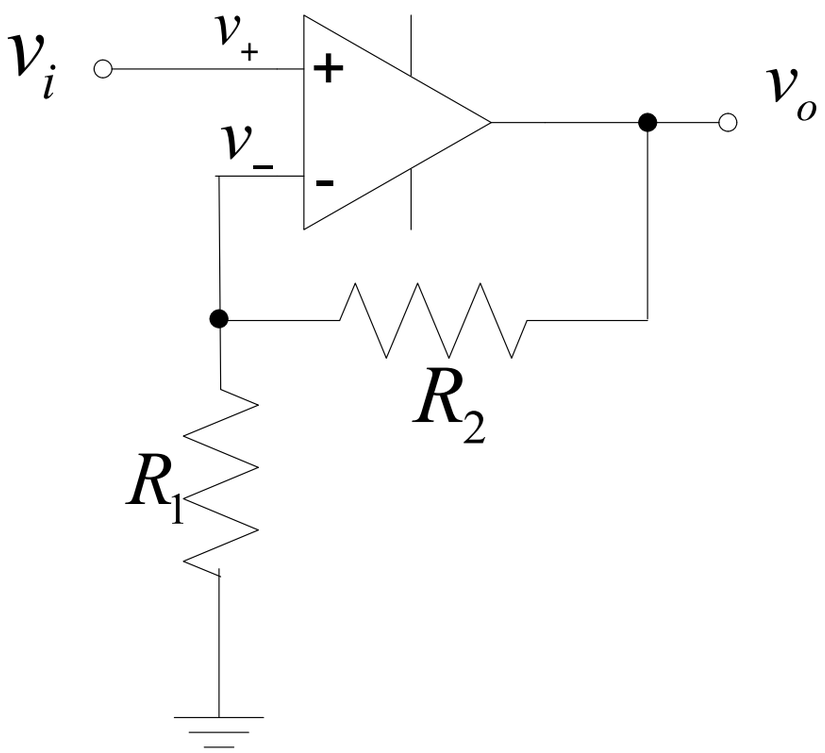


Golden Rules of Op Amps:

1. The output attempts to do whatever is necessary to make the voltage difference between the inputs zero.

2. The inputs draw no current.

Non-inverting Amplifier



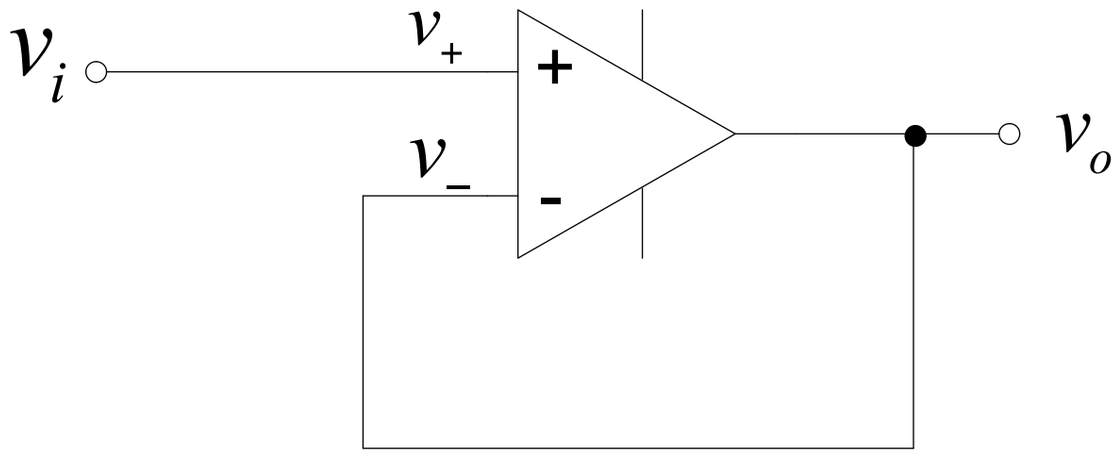
Closed-loop voltage gain

$$A_F = \frac{v_o}{v_i}$$

$$v_i = v_+ = v_- = \frac{R_1}{R_1 + R_2} v_o$$

$$A_F = \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1}$$

Unity-Gain Buffer



Closed-loop voltage gain

$$A_F = \frac{v_o}{v_i}$$

$$v_i = v_+ = v_- = v_o$$

$$A_F = \frac{v_o}{v_i} = 1$$

Used as a "line driver" that transforms a high input impedance (resistance) to a low output impedance. Can provide substantial current gain.

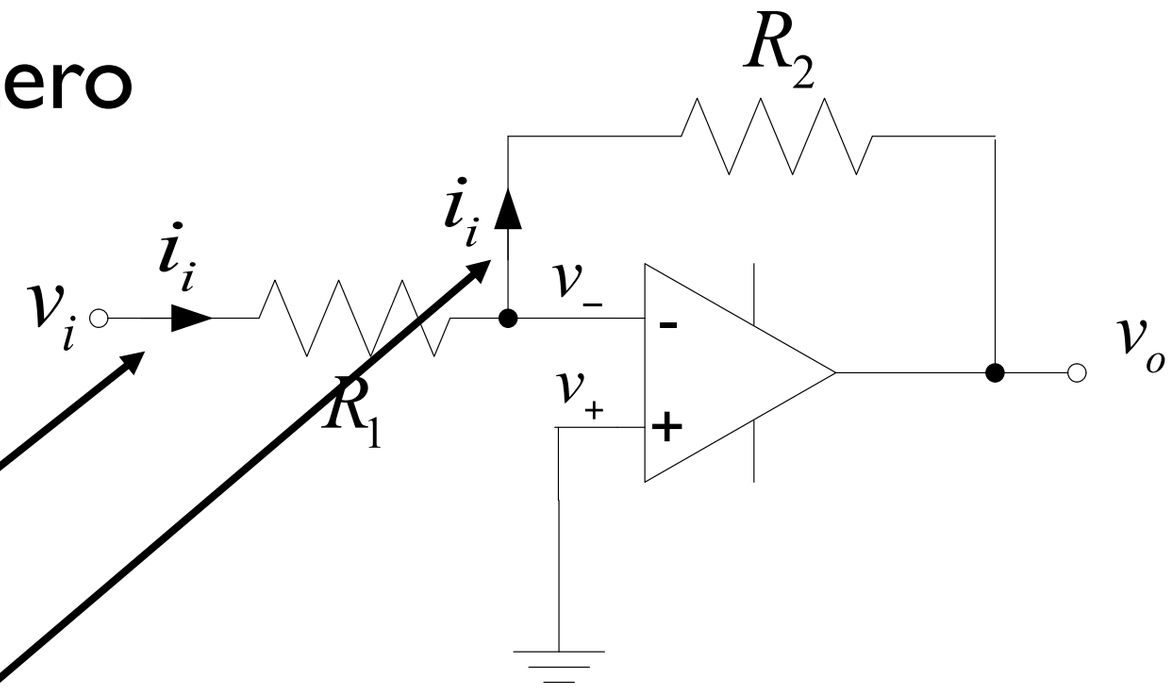
Inverting Amplifier

Current into op amp is zero

$$v_- = v_+ = 0$$

$$i_i = \frac{v_i - 0}{R_1} = \frac{v_i}{R_1}$$

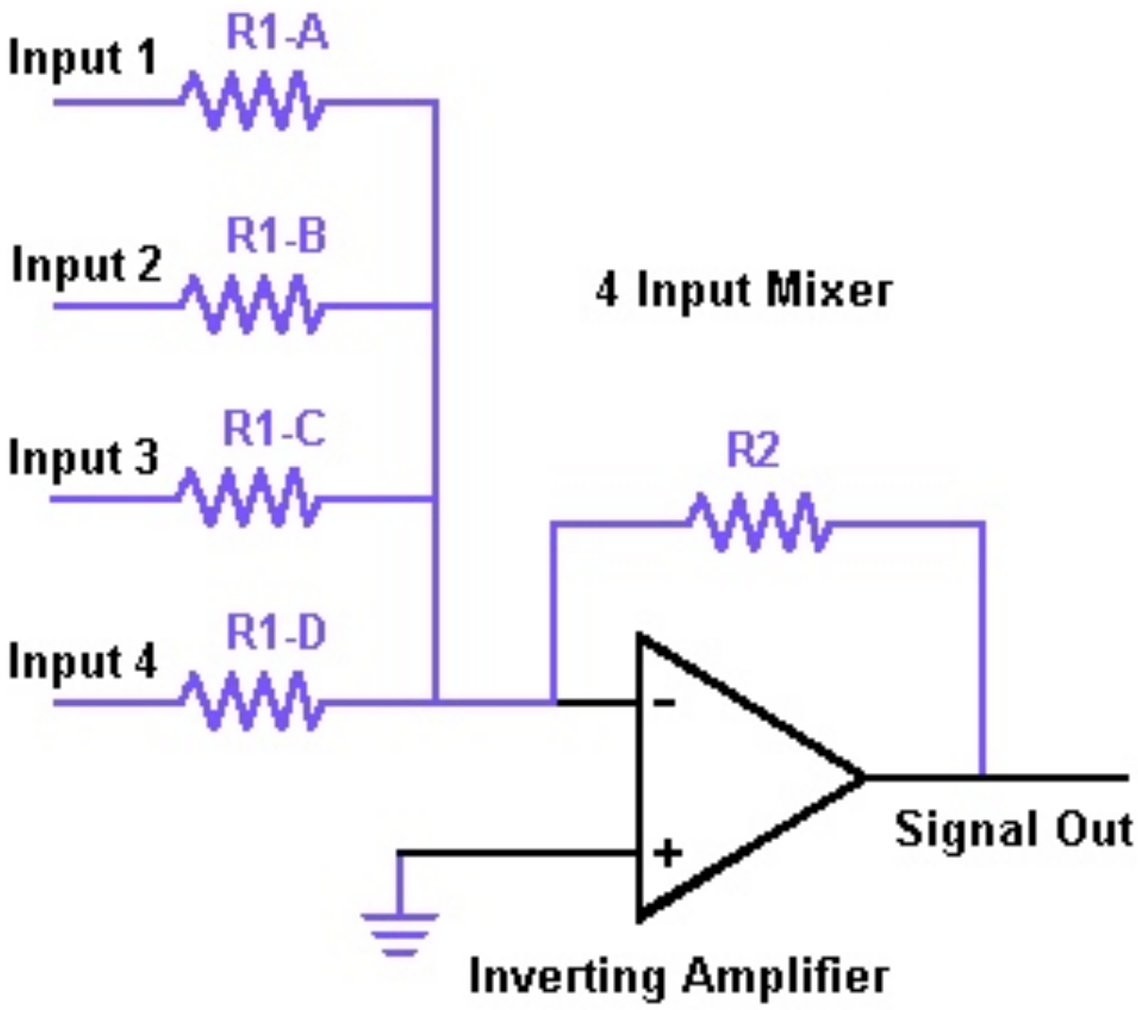
$$i_i = \frac{0 - v_0}{R_2} = \frac{-v_0}{R_2}$$



$$\frac{v_i}{R_1} = \frac{-v_0}{R_2}$$

$$A_F = \frac{v_o}{v_i} = -\frac{R_2}{R_1}$$

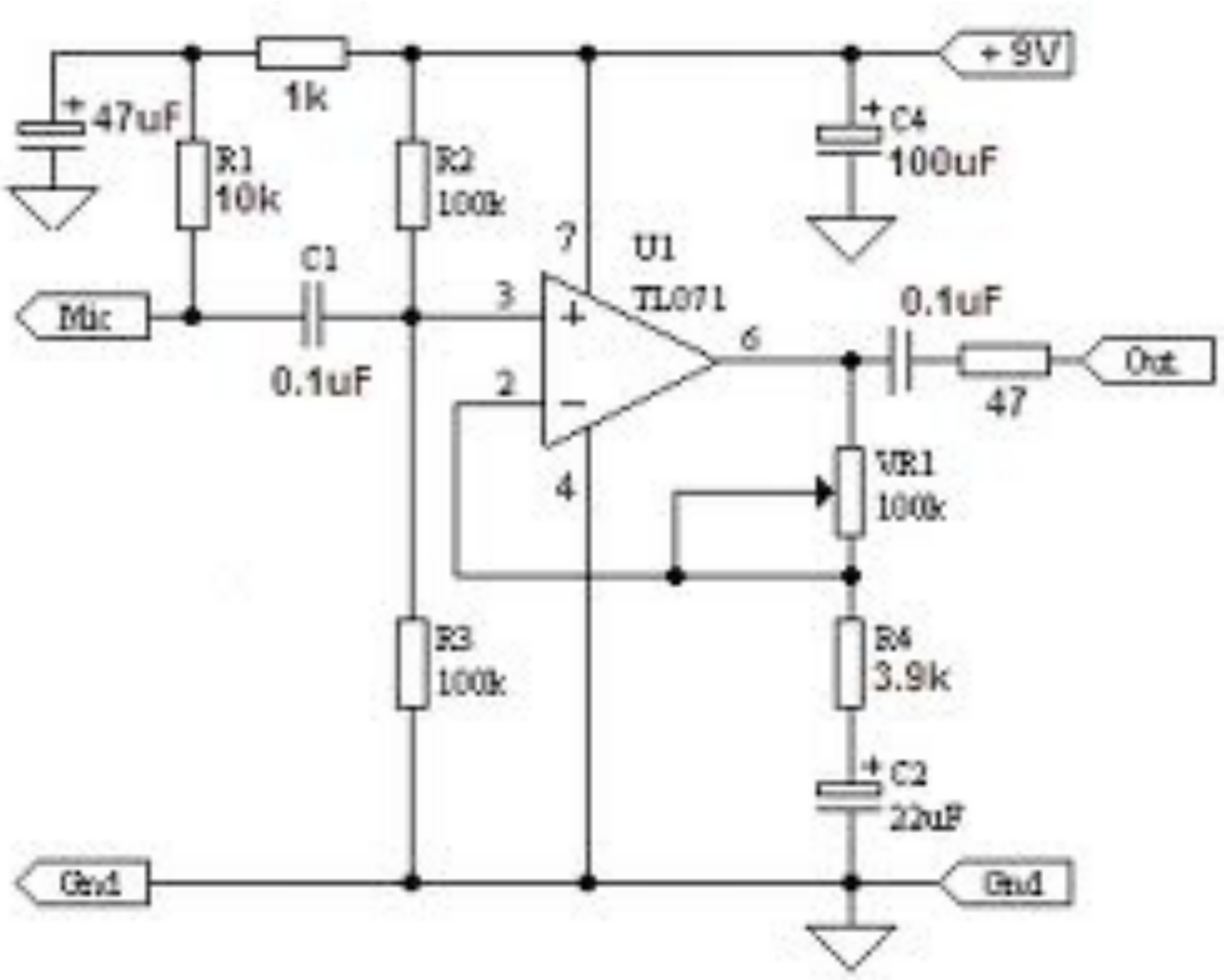
Mixing Amplifier



Consider

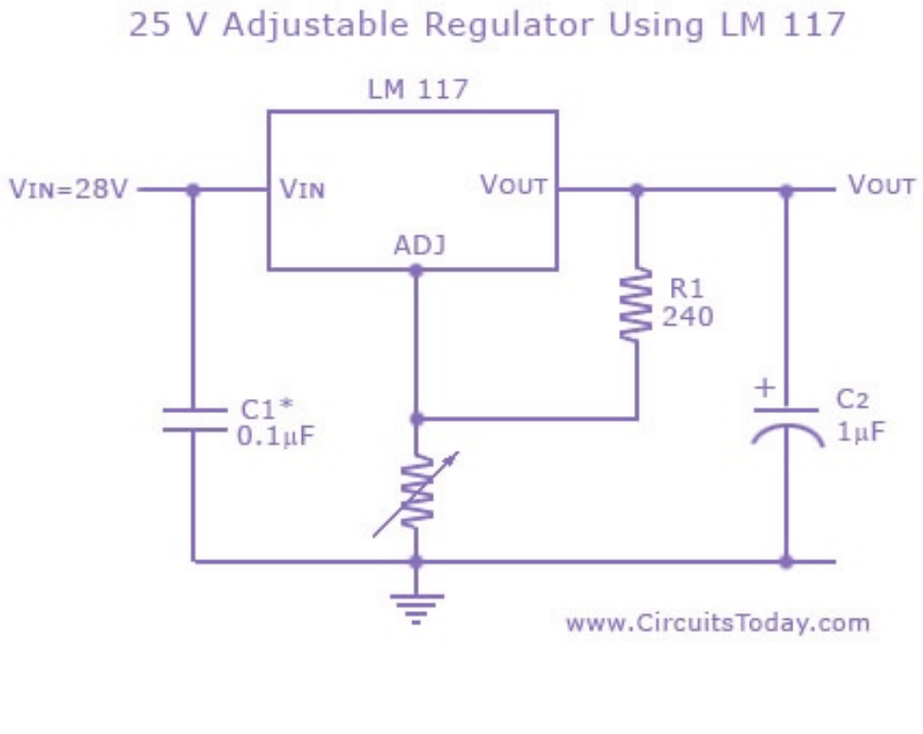
- equal values of R1
- Inverting Amplifier (or not)
- handle the output 'swing'

Practical circuit



- NOTE
- single supply
- bias
- decoupling
- power line filter cap
- AC coupling

Power management

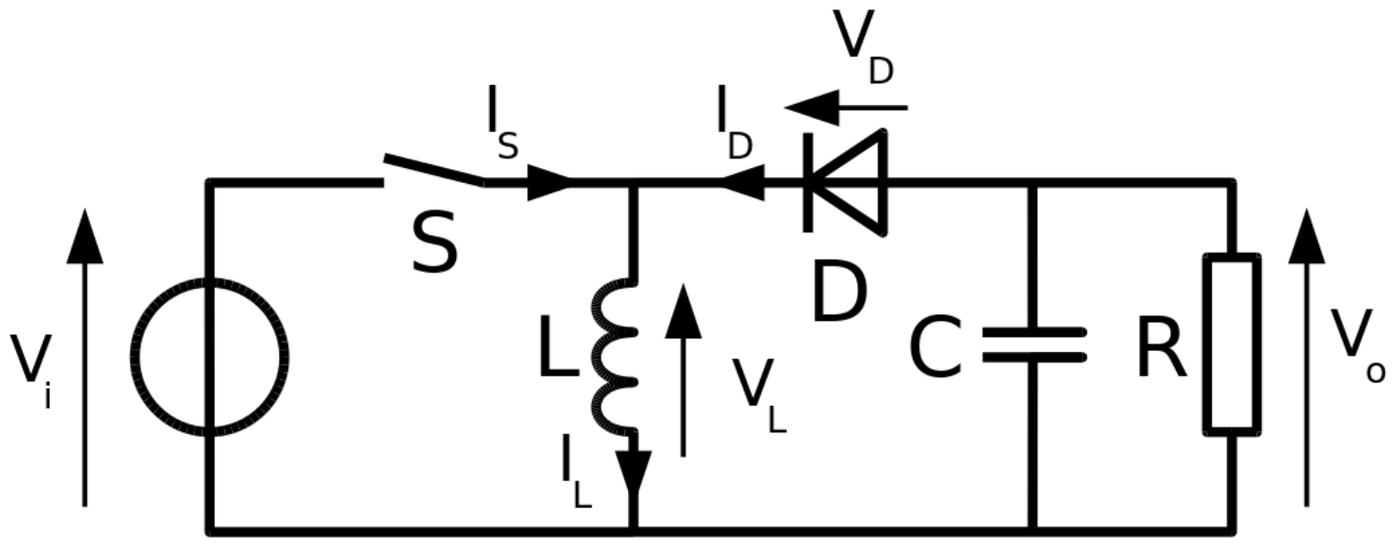


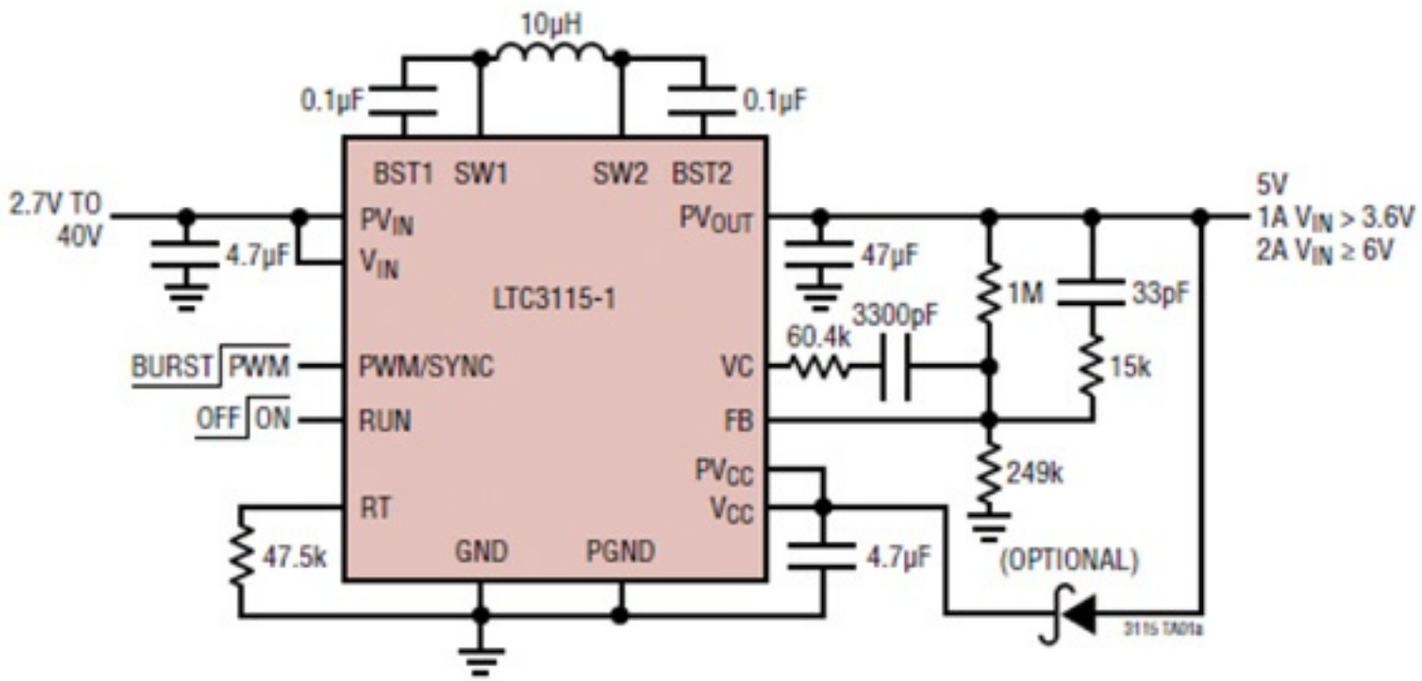
- Linear
- 3 terminal regulators
- 7805, 7905
- LDO types
- EFFICIENCY

Consider:
9 volt battery, 5 volt rail, 100mA draw, 7805 device

4 volt drop @ 100 mA = 400mW loss as HEAT

Power management





- SMPS
- efficiency at what voltages/currents?
- many types!
- C and L
- tailor Vout

Why?

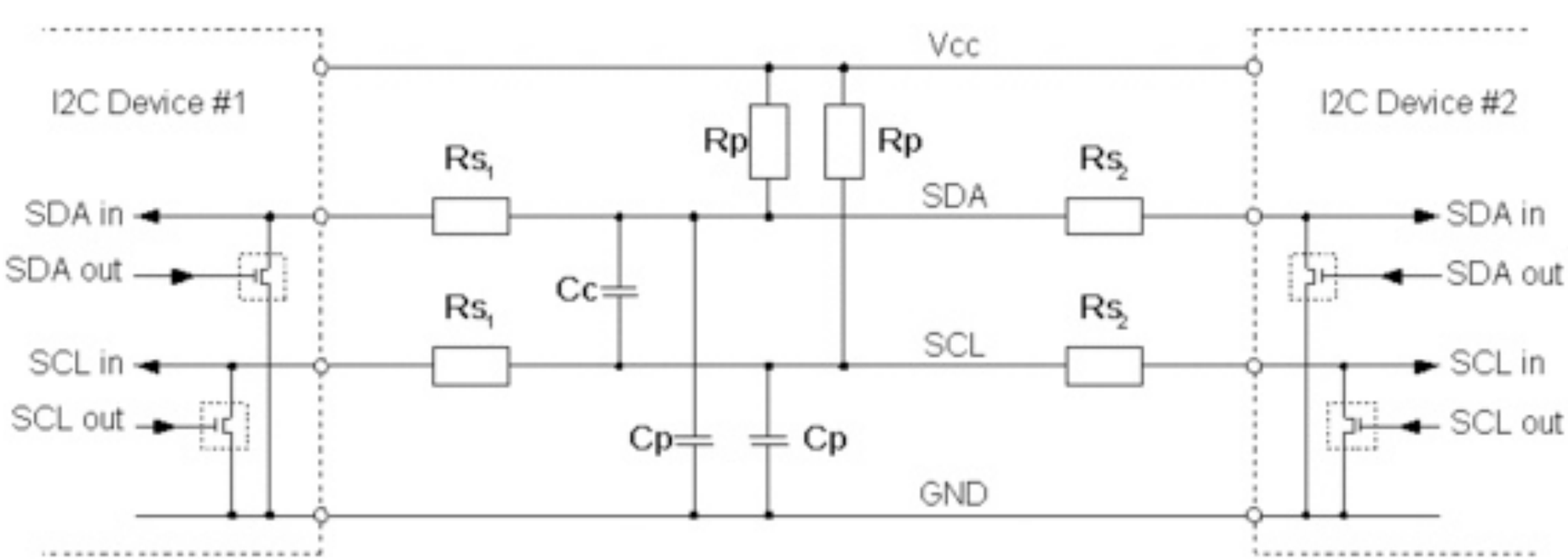
- Parallel bus alternatives failing
- Commercial imperatives

What?

- Inter IC Communications (I2C, “I squared C”)
- “Two Wire”, TWI
- Philips Semiconductors (now NXP)
- Defined in **UM10204** **I2C-bus specification and user manual**

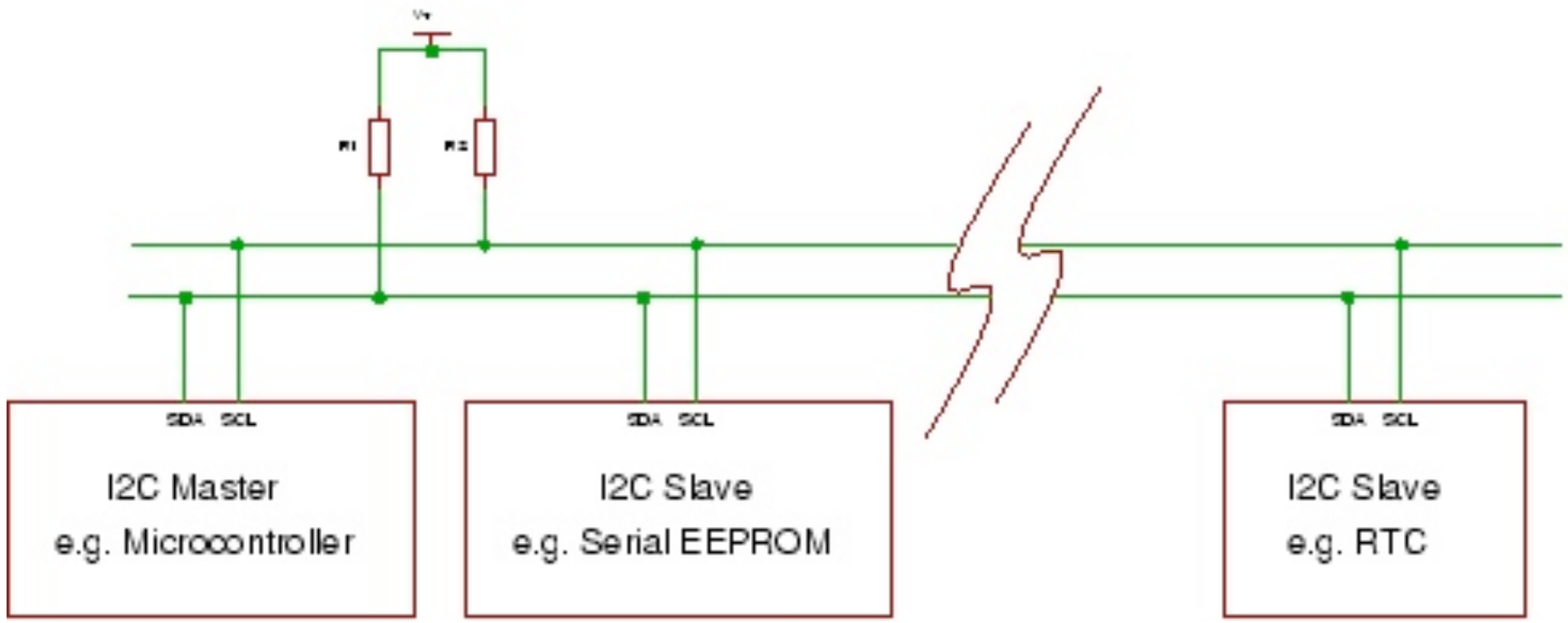
How?

- Two wires - data and clock (SDA, SCL)
- Defined ICs have a fixed (8 bit) address



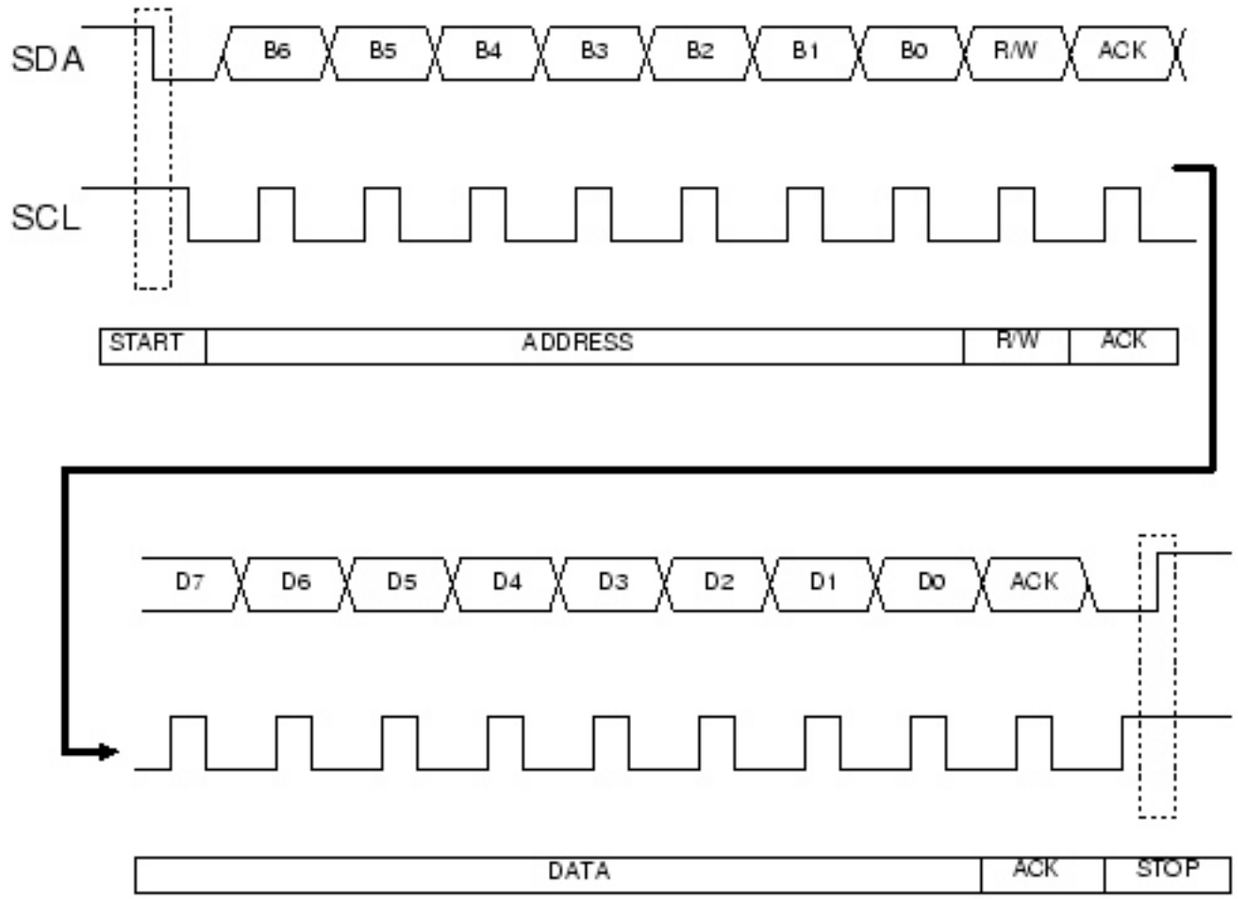
How?

- Master & (multiple) slaves



Basic Command Structure

1. Send the START bit (S).
- 2. Send the slave address (ADDR).
- 3. Send the Read(R)-1 / Write(W)-0 bit.
- 4. Wait for/Send an acknowledge bit (A).
- 5. Send/Receive the data byte (8 bits) (DATA).
- 6. Expect/Send acknowledge bit (A).
- 7. Send the STOP bit (P).



What is the correct address?

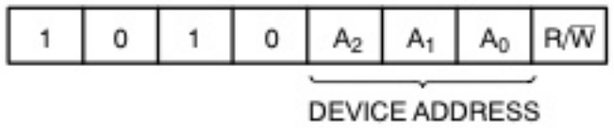


Figure 3. Slave Address Bits

- selectable address for this IC
- NB: READ/WRITE bit
- data read (or written) in 8 bit packets with the clock.

CAT24C512

512 kb I²C CMOS Serial EEPROM

Description

The CAT24C512 is a 512 kb Serial CMOS EEPROM, internally organized as 65,536 words of 8 bits each.

It features a 128−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to eight CAT24C512 devices on the same bus.

Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 128−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8−pin PDIP, SOIC, TSSOP, MSOP and 8−pad UDFN Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

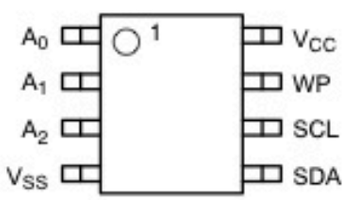
ON Semiconductor®

http://onsemi.com

SOIC−8 W SUFFIX CASE 751BD | UDFN−8 HU5 SUFFIX CASE 517BU | SOIC−8 X SUFFIX CASE 751BE

PDIP−8 L SUFFIX CASE 646AA | TSSOP−8 Y SUFFIX CASE 948AL | MSOP−8 Z SUFFIX CASE 846AD

PIN CONFIGURATION



(Top View)

Basics of using an I2C IC (EEPROM)

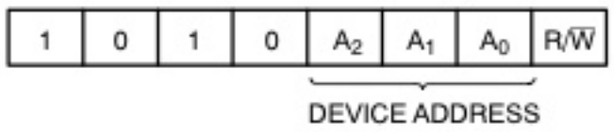


Figure 3. Slave Address Bits

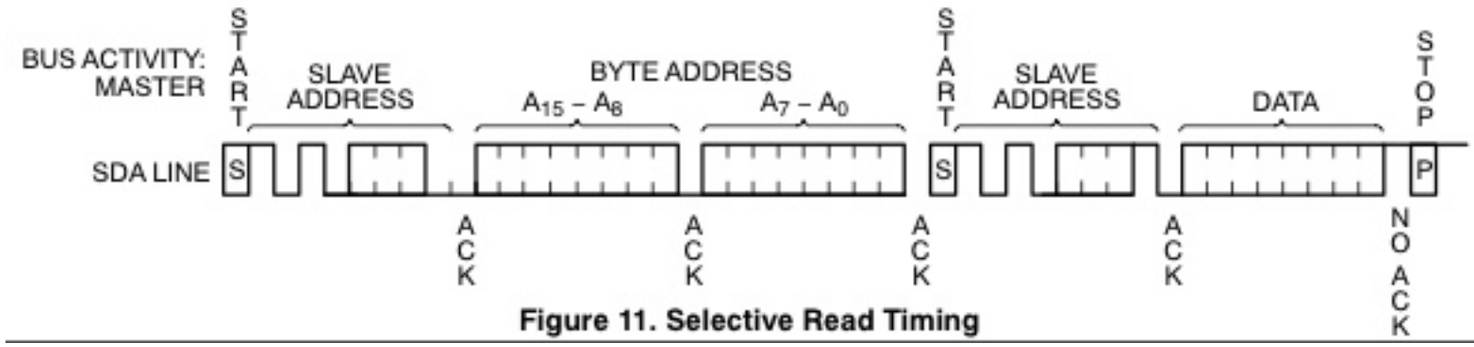


Figure 11. Selective Read Timing

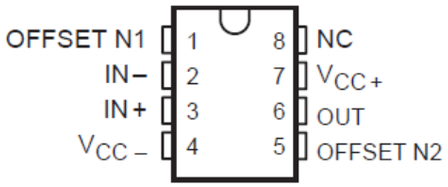
example above is for reading back one byte only.

Component packages

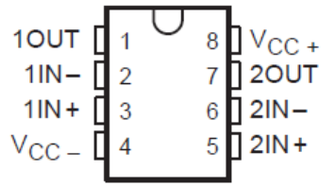
TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080D – SEPTEMBER 1978 – REVISED AUGUST 1996

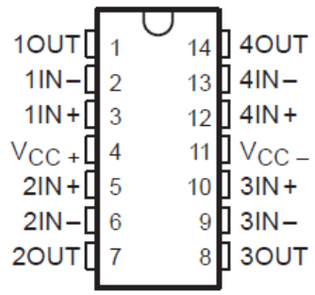
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



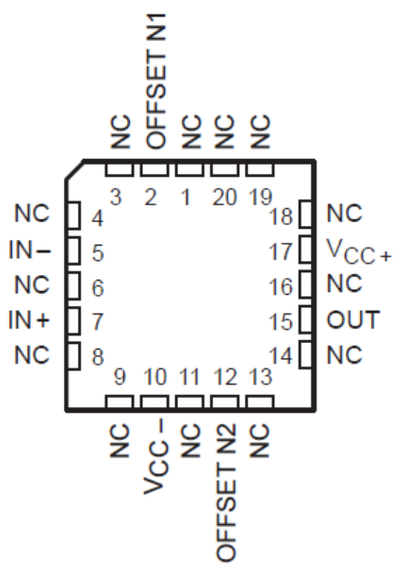
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



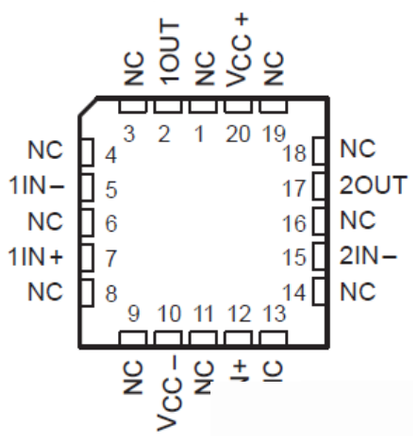
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



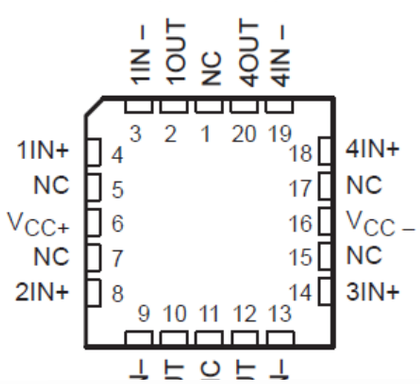
TL071
FK PACKAGE
(TOP VIEW)

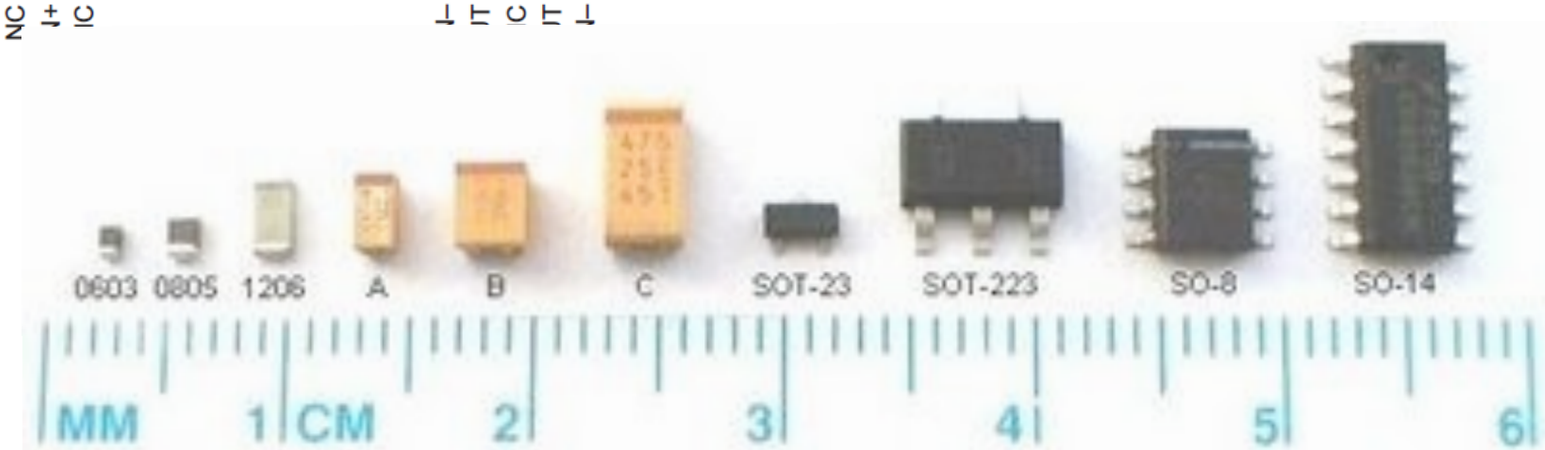


TL072
FK PACKAGE
(TOP VIEW)

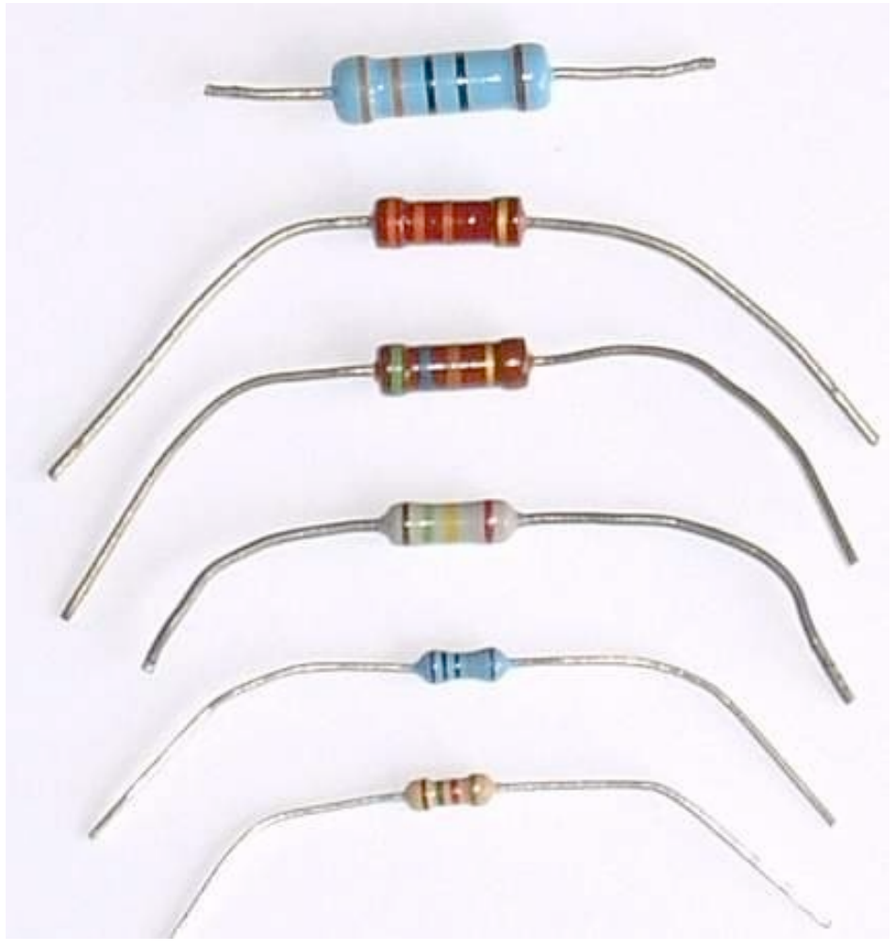


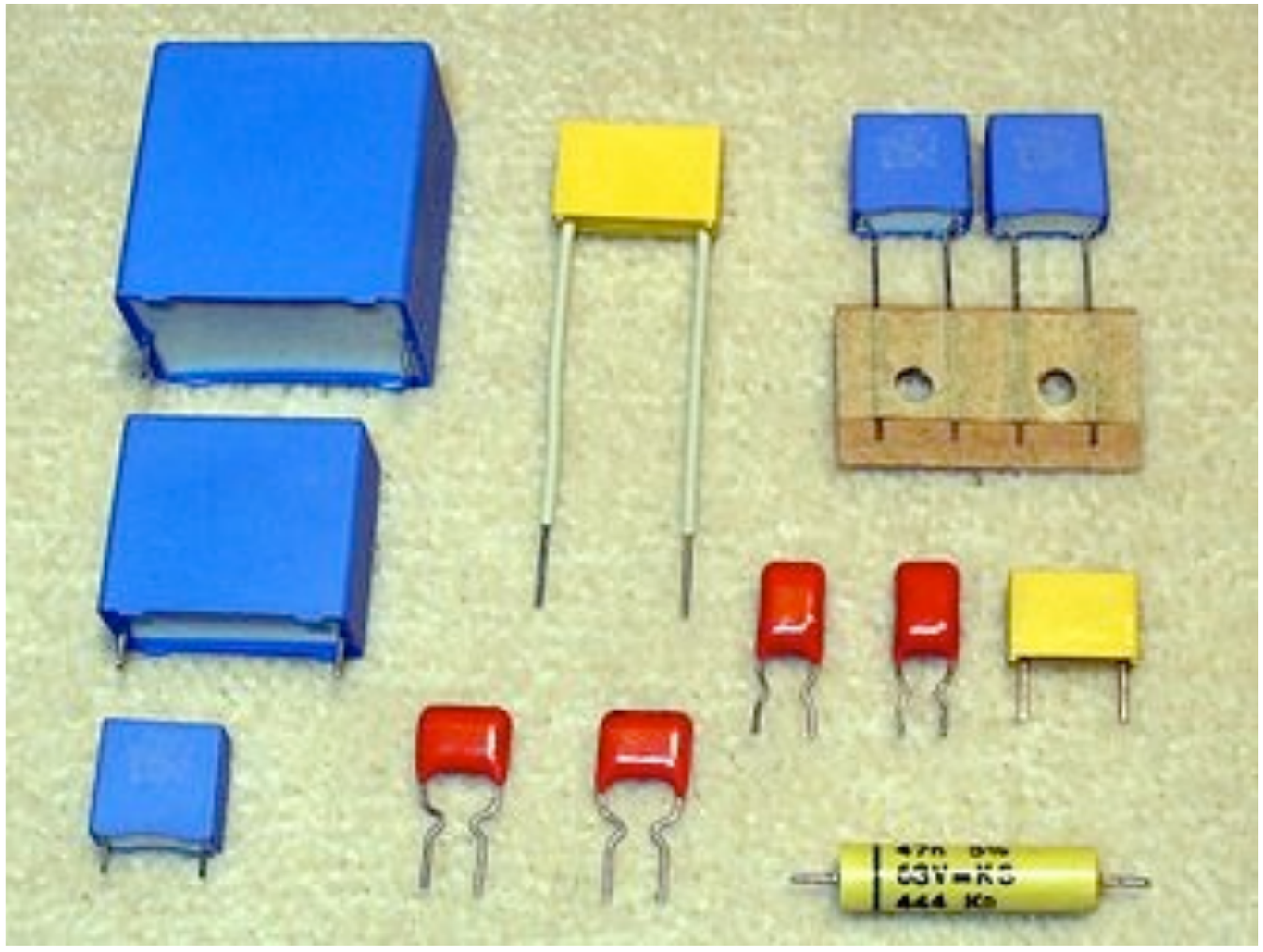
TL074
FK PACKAGE
(TOP VIEW)





Component packages





Resistors - axial, 600 mW, 0.4 inch, 400 mils

Capacitors - axial or radial, 0.1 inch, 100 mils - >400 mils - CHECK FIRST