CSE 291 Assignment 1: Matrix Multiplication IP Core Design on an FPGA

Due date: 04/13/2017

Instructions

Matrix multiplication is a core building block of many algorithms including convolutional neural networks. In this assignment, you will design and optimize matrix multiplication algorithm on an FPGA using Vivado High-level synthesis. You are given two folders (matmul_int and matmul_binary) and you have two tasks as follows:

Task 1: 40% of Assignment 1

Design a 32-bit integer matrix multiplication core where inputs are 32-bit integers. Use files inside matmul_int folder to design and implement 128x128 matrix multiplication. This folder contains following files:

- matmul.cpp
- matmul.h
- matmul_test.cpp
- script.tcl ==> Use this script to run the vivado hls. Do not change contents of this file!

Task 2: 60% of Assignment 1

Design and implement a matrix multiplication core where the inputs are restricted to be +1 and -1. Use matmul_binary folder and files inside this folder for this task.

Submission

- Create a bitbucket repo with lastname1_lastname2_cse291 where lastname1 and lastname2 are lastnames of team members. Share your repo with instructors. (Ali Irturk and Janarbek Matai)
- Create a folder named Assignment1, Assignment2, Assignment3 and Final_Project inside your repo. Use Assignment1 folder for this assignment
- You must submit all necessary source code (matmul_int and matmul_binary folders)
- You must create a wiki (no more than 2 pages) for Assignment 1. Your wiki must contain followings:
    - Hardware architecture diagram for Task 1

- Hardware architecture diagram for Task 2
- Performance and area utilization results corresponding to the architectures
- If you have done any specific optimization which requires changing the code, please explain the optimization and its impact on the hardware performance and area. (Hint: You must change the code for Task 2).