MEC4126F: Integrated Embedded Systems

Prac 7
08 May 2025

Total marks: 51

Instructions to students

1. This template file contains space for the answers to the written questions of Prac 7.
2. Ensure that you copy-paste your answers inside the space allocated for each question.
3. Provide your numerical answers to **TWO (2)** significant decimal points, unless stated otherwise.

PeopleSoft ID: 1932268

Plagiarism Declaration

By demonstrating and submitting this practical I agree that:

- I know that plagiarism is a serious form of academic dishonesty.
- I have read the document about avoiding plagiarism, am familiar with its contents and have avoided all forms of plagiarism mentioned there.
- Where I have used the words of others, I have indicated this by the use of quotation marks.
- I have referenced all quotations and other ideas borrowed from others.
- I have not and shall not allow others to plagiarise my work.
- I have not used an AI language model to generate the code or answers submitted here.

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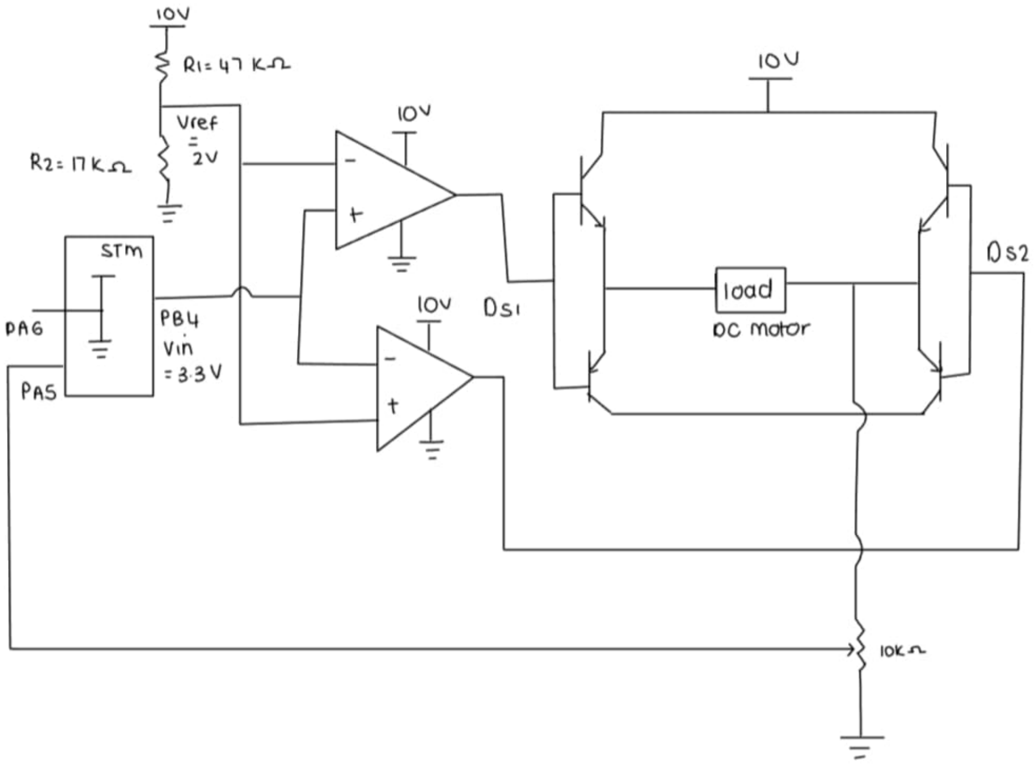
Question 1 (6 marks)



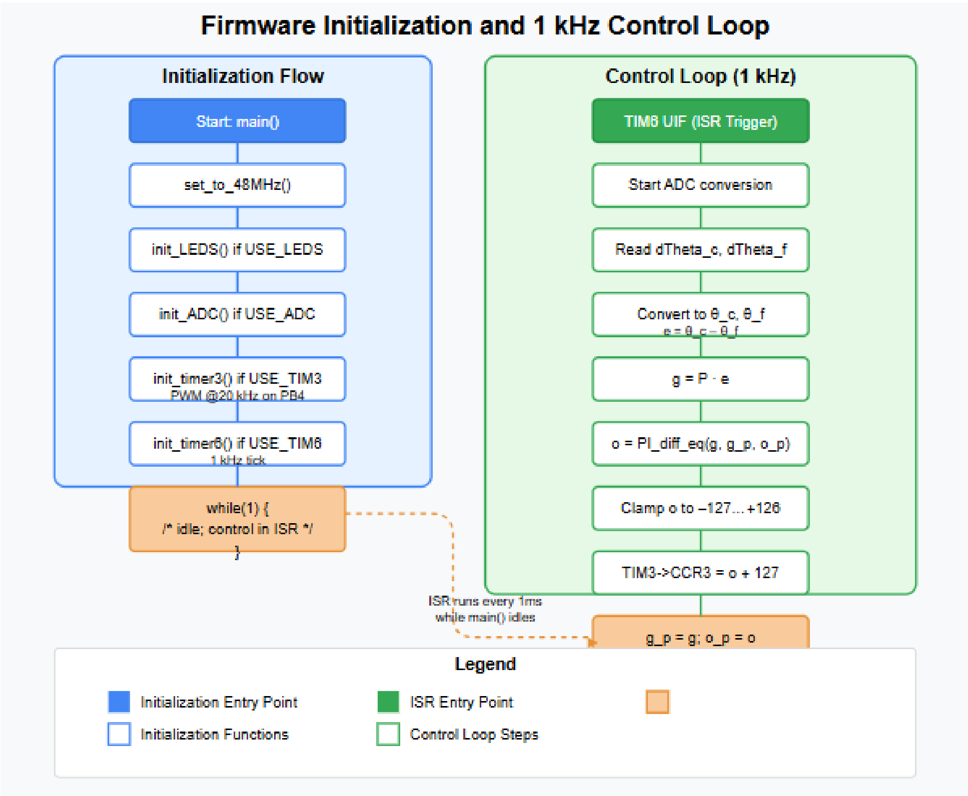
Question 2 (3 marks)

Input PWM (V)	V_ref (V)	Op Amp 1 Output (V)	Op Amp 2 Output (V)	DS1 (V)	DS2 (V)
0	2	0.5	8.16	0.5	8.16
3.3	2	8.16	0.6	8.3	0.6

Question 3 (3 marks)

DS1 (V)	DS2 (V)	Switch A	Switch B	Switch C	Switch D	V_load (V)
8.16	0	ON	OFF	OFF	ON	5.16
0	8.2	OFF	ON	ON	OFF	5.2

Question 4 (14 marks)



Question 5 (6 marks)

The proportional gain, K_p, chiefly determines how aggressively the motor responds to an error: increasing K_p speeds up the rise time and improves disturbance rejection, but if it becomes too large the system turns under-damped, leading to overshoot, oscillation and amplified sensor noise. The integral action, governed by K_i (or equivalently by the integral time constant I), continually accumulates any residual error to drive the steady state offset to zero. In practice, a stronger integral term will eliminate steady-state error and bolster low-frequency disturbance rejection, but if it is excessive it can wind up during large setpoint steps and cause significant overshoot or sustained oscillations unless anti-windup measures are employed.

Choosing the controller's sample time, T_s, involves a trade-off between faithfully approximating the continuous-time PI behaviour and imposing computational and measurement constraints. A shorter sample time (e.g. 1 ms for a 1 kHz update rate) reduces phase lag and more closely emulates an ideal PI controller, yielding faster, more stable responses - but at the cost of higher CPU load, increased susceptibility to ADC noise and potential timing jitter. Conversely, a longer sample period introduces additional discrete-time lag, which can slow the response, increase tracking error, and even destabilise the loop if it approaches the system's dominant time constants. Thus, K_p and K_i must be balanced to shape the transient and steady-state performance, while T_s must be chosen small enough to capture the motor's dynamics yet large enough to allow reliable measurements and processing.

Question 6 (10 marks)

Using the LM358's slew rate limit and the requirement that the level-change time be under 1% of the PWM period:

- Signal swing: 10 V
- Slew rate: 0.3 V/μs
- Signal level change time: 10 V / (0.3 V/μs) = 33.33 μs

To keep this under 1% of the PWM period, the period must be ≥ 33.33 μs / 0.01 = 3333 μs, so the maximum PWM frequency is 1 / 3333 μs ≈ 300 Hz.

With a 48 MHz system clock and a 10-bit PWM resolution (ARR = 1023), the timer prescaler (PSC) is computed by:

PSC ≈ (System Clock / (PWM Frequency × (ARR + 1))) - 1

PSC ≈ (48,000,000 / (300 × 1024)) - 1 ≈ 155.