EE 382M-1 VLSI Testing, Project 2

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1. BIST Design

The BIST block consists of a data path and a controller. As shown in Fig. 1, the data path uses two 16-bit LFSRs for pattern generation and response compression, respectively. The primitive polynomial of the LFSRs is $x^{16}+x^{5}+x^{4}+x^{3}+1$. The modular architecture is used. Each LFSR has a control signal to enable shifting, which is given by the controller. A 16-bit register is used to store the fault-free signature of the CUT. A loading signal given by the controller controls the value update of the register.

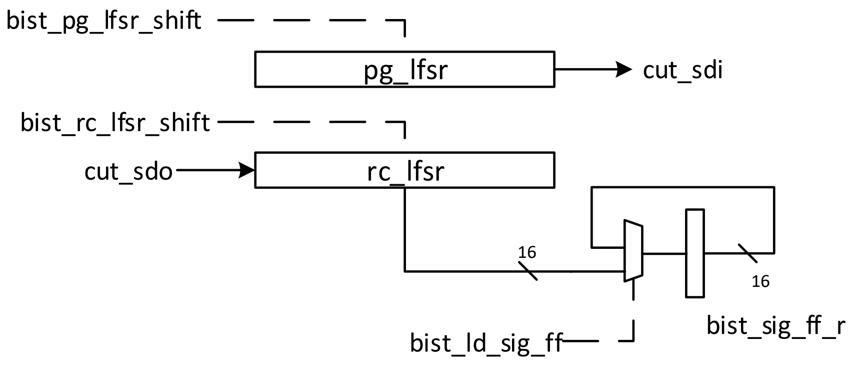


Figure 1 – Data path

The controller consists of two finite state machines (the main state machine and the fault-free controller state machine) and two counters (the scan shifting counter and the test pattern counter). The main state machine controls the general process of the BIST, as shown in Tab. 1. It controls the LFSRs to make them behave correctly according to which step the current test is in. Note we make the shifting-in of the next pattern overlap with the shifting-out of the previous pattern to save test time.

The fault-free controller state machine determines whether the current test is the fault-free case, and controls the update of the fault-free signature register. The register is updated with the signature coming from the response compression LFSR only when the fault-free test, i.e. the first one, is completed.

The scan shifting counter determines when a shifting-in or shifting-out is completed. It counts from 0 to 266 (8 bits) and then wraps around when a pattern is being shifted in or out. (The number of scan cells in the CUT is 277). The test pattern counter counts the number of test patterns that has been applied. It counts from 0 to 1999 (11 bits), where all 2000 patterns have been applied, and signals the main state machine to end the test.

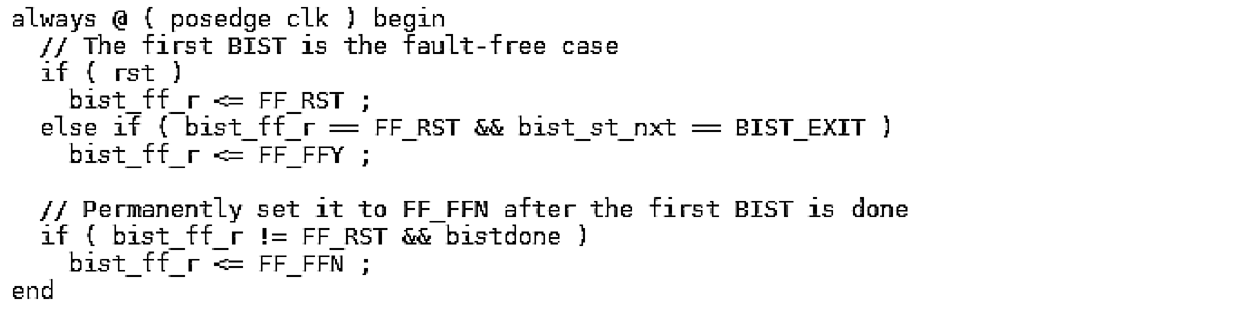
State name	Data path control	Next state
`BIST_IDLE`	Disable both LFSRs and de-assert `cut_scanmode`	Go to `BIST_APLY` when `rst` and `bistmode` are asserted at the same time
`BIST_APLY`	Shift in a test pattern by enabling the pattern generation LFSR and asserting `cut_scanmode`	Go to `BIST_CAPT` when the scan shift counter reaches 226
`BIST_CAPT`	Capture cycle; disable both LFSRs and de-assert `cut_scanmode`	Go to `BIST_CHCK`
`BIST_CHCK`	Shift out the response of the previous pattern and shift in a new pattern at the same time; enable both LFSRs and assert `cut_scanmode`	Go to `BIST_EXIT` if all 2000 patterns have been applied (i.e., the test pattern counter reaches 1999); go back to `BIST_CAPT` otherwise
`BIST_EXIT`	Assert `bistdone`; assert `bistpass` if the current test is the fault-free one or the output of the response compression LFSR is the same with the fault-free signature; register the fault-free signature if the current test is the fault-free one	Go back to `BIST_IDLE`

Table 1 – Main state machine

2. Design Challenge

The main challenge we face is to control the fault-free signature register so that it knows when to update its value and when to keep its value unchanged. We use the state machine shown in Fig. 2 to solve the problem.

The state machine resets to the FF_RST state, and then goes to FF_FFY state before the first test is done. Then it goes to the FF_FFN state and remains there permanently. The fault-free register is updated in the FF_FFY state. (By specification, the first test is always fault free).



```
always @ ( posedge clk ) begin
  // The first BIST is the fault-free case
  if ( rst )
    bist_ff_r <= FF_RST ;
  else if ( bist_ff_r == FF_RST && bist_st_nxt == BIST_EXIT )
    bist_ff_r <= FF_FFY ;

  // Permanently set it to FF_FFN after the first BIST is done
  if ( bist_ff_r != FF_RST && bistdone )
    bist_ff_r <= FF_FFN ;
end
```

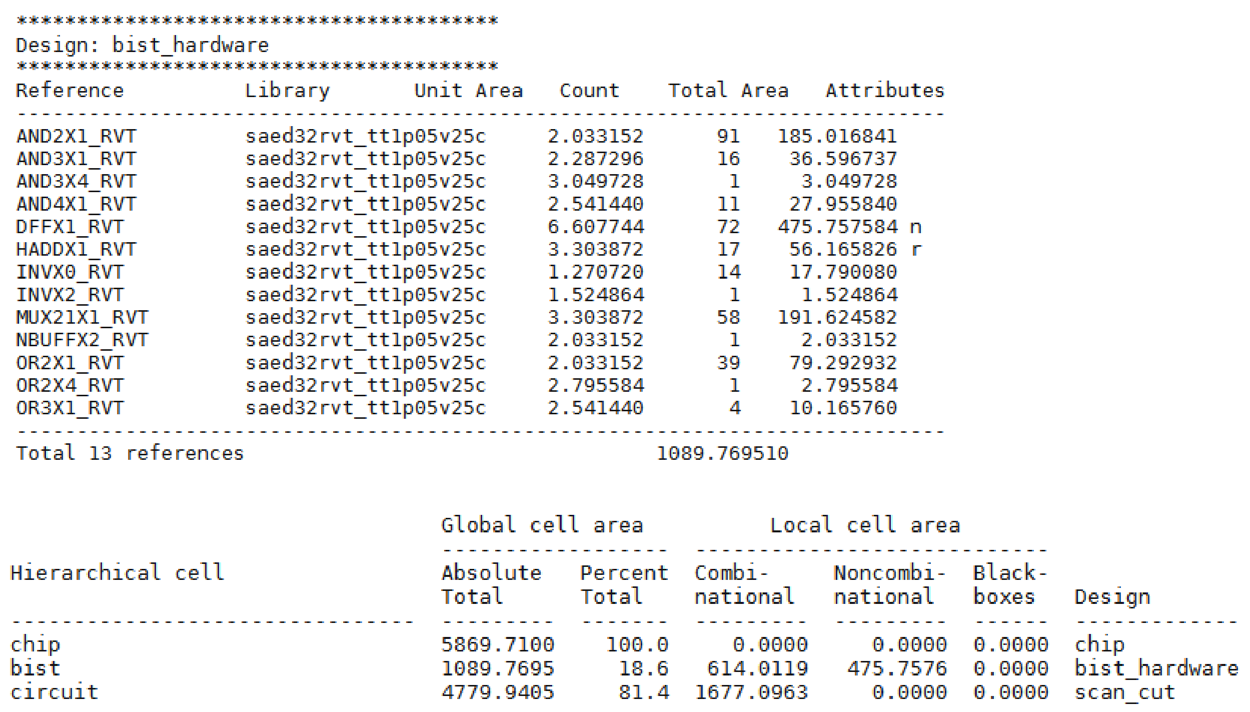
Figure 2 – Fault-free controller state machine

Such an implementation works perfectly in functional simulation; however, it will not work if it is synthesized and put on silicon. The system asserts reset every time a new test is initiated. As a result, since all states are unknown (which can be resolved to any state on silicon) before the first reset, you can never rely on any states to determine whether a reset corresponds to the first, i.e., fault-free, test. But for this project, the state machine shown in Fig. 2 works well since the simulator considers the unknown state different from any other states.

3. Hardware Resources

As described in section 1, our design requires two 16-bit LFSRs, a 16-bit fault-free signature register, a 5-state state machine, a 3-state state machine, an 8-bit counter and an 11-bit counter. To sum them up, we need 72 flip-flops plus combination logic that includes an 8-bit incrementer, an 11-bit incrementer, and some small multiplexers and comparators.

The design is synthesized using the SAED 32/28nm library. The results show that the number of flip-flops is 72, which is consistent with our design intent. The total standard cell area is 1090 microns, which consists of 476 microns' sequential logic (flip-flops) and 614 microns' combinational logic.



```
****************************************
Design: bist_hardware
****************************************
Reference          Library       Unit Area   Count    Total Area   Attributes
-----------------------------------------------------------------------------
AND2X1_RVT         saed32rvt_tt1p05v25c     2.033152      91   185.016841
AND3X1_RVT         saed32rvt_tt1p05v25c     2.287296      16    36.596737
AND3X4_RVT         saed32rvt_tt1p05v25c     3.049728       1     3.049728
AND4X1_RVT         saed32rvt_tt1p05v25c     2.541440      11    27.955840
DFFX1_RVT          saed32rvt_tt1p05v25c     6.607744      72   475.757584 n
HADDX1_RVT         saed32rvt_tt1p05v25c     3.303872      17    56.165826 r
INVX0_RVT          saed32rvt_tt1p05v25c     1.270720      14    17.790080
INVX2_RVT          saed32rvt_tt1p05v25c     1.524864       1     1.524864
MUX21X1_RVT        saed32rvt_tt1p05v25c     3.303872      58   191.624582
NBUFFX2_RVT        saed32rvt_tt1p05v25c     2.033152       1     2.033152
OR2X1_RVT          saed32rvt_tt1p05v25c     2.033152      39    79.292932
OR2X4_RVT          saed32rvt_tt1p05v25c     2.795584       1     2.795584
OR3X1_RVT          saed32rvt_tt1p05v25c     2.541440       4    10.165760
-----------------------------------------------------------------------------
Total 13 references                                   1089.769510


                                   Global cell area          Local cell area
                                   ------------------  ----------------------------
Hierarchical cell                  Absolute   Percent  Combi-     Noncombi-  Black-
                                   Total      Total    national   national   boxes   Design
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chip                               5869.7100    100.0     0.0000     0.0000  0.0000  chip
bist                               1089.7695     18.6   614.0119   475.7576  0.0000  bist_hardware
circuit                            4779.9405     81.4  1677.0963     0.0000  0.0000  scan_cut
```

Figure 3 – Synthesis results