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Electron beam metrology for advanced technology nodes

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The critical dimension scanning electron microscope (CD-SEM) is one of the main tools used to estimate critical dimension (CD) in semiconductor manufacturing nowadays, but, as all metrology tools, it will face considerable challenges to keep up with the requirements of the future technology nodes. The root causes of these challenges are not uniquely related to the shrinking CD values, as one might expect, but to the increase in complexity of the devices in of morphology and chemical composition as well. In fact, complicated three-dimensional device architectures, high aspect ratio features, and wide variety of materials are some of the unavoidable characteristics of the future metrology nodes. In this paper, we report on the development of advanced CD-SEM metrology at imec on a variety of device platforms and processes, for both logics and memories. The large variety of results reported here a clear indication of the on-going creative effort needed to ensure that the critical potential of CD-SEM metrology tools is fully enabled for the 5 nm node and beyond.

1. Introduction

As the semiconductor industry moves toward advanced technology nodes, it is more and more clear that the metrology landscape will have to change. For many years, two very separate approaches coexisted peacefully. On one side, process control tools, ultimately aimed to closely monitor yield. On the other side, research tools, focused on debugging issues and developing new approaches. Metrology tools for process monitoring are characterized by high throughput and fully automated procedures. Research tools, by contrast, are usually characterized by low throughput and marginal levels of automation. With the coming of age of complex device architectures and new materials, the gap between these two different ways of doing metrology is shrinking fast, as the request of performing disruptive types of new metrology grows.[1–3] Consequently, research tools are moving to the fab floor and we now see fully automated transmission electron microscopes (TEM).[4] Similarly, we see classical process control tools expanding their application domain to include new complex types of metrology, covering both process set-up and process control. This paper will specifically focus on this latter trend.

In this paper, we report on the development of advanced critical dimension scanning electron microscope (CD-SEM) metrology at imec on a variety of device platforms and processes, for both logic and memory. We discuss newly developed approaches for silicon, III–V, and germanium Fin field effect transistors (FinFETs), for lateral and vertical nanowires (NW),[5–8] three-dimensional NAND (3D NAND),[9] spin transfer torque random-access memory (STT-RAM),[10,11] and resistive random-access memory (ReRAM).[12] Applications for both front-end of line and back-end of line are developed. In terms of process, source drain epitaxy (S/D Epi), self-aligned quadruple patterning, directed self-assembly, and extreme ultraviolet lithography have been used. The work reported here has been performed on Hitachi CG5000, CG6300, and CV5000 CD SEMs.

In terms of logic, we discuss here the S/D epi defect classification, the metrology optimization for shallow trench isolation (STI) Ge FinFETs, the defectivity of III–V STI FinFETs, and the metrology for vertical and horizontal NWs. With respect to memory, we investigate STT-RAM statistical CD analysis and its electrical performance, ReRAM metrology for vacancy-modulated conductive oxide (VMCO) is compared to electrical performance, and 3D NAND oxide nitride oxide (ONO) thickness measurements. In addition, we report on 3D morphological reconstruction using CD SEM in conjunction with focused ion beam (FIB), on optimized best known methods development methodologies, and on CD SEM overlay.

The standard landing energy used here 500 eV for resist wafers and of 800 eV for etched wafers. Pixel size is in the order of 0.8 nm. Beam current is 8pA. The dynamic measurement reproducibility is of 0.15 nm (3σ).

The large variety of results reported here gives a clear overview of the creative effort put in place to ensure that the critical potential of CD SEM metrology tools is fully enabled for the 5 nm node and beyond.

2. Results and discussion

2.1. SEM-based overlay measurement between resist and buried patterns

With the continuous shrink in pattern size and increased density, overlay and edge-placement[13–17] control has become one of the most critical issues in semiconductor manufacturing. In particular, there is a clear need for SEM-based overlay measurements of after develop inspection (ADI) wafers, to serve as reference for optical overlay and make the necessary corrections before etching. Furthermore, to ensure that these corrections are as accurate as possible, actual device-like feature dimensions need to be measured ADI, in device. The capability of measuring device-scale features is a unique feature of CD SEM overlay targets. In addition, the overall size of these targets is relatively small ($2 \times 2\,\mu$m or less), thus allowing their in-chip placement.[13,14]

In Fig. 1, we report SEM-based overlay measurements obtained using high voltage SEM. In this case, the under layer is reveled using backscattered electrons (BSE), while the surface pattern is investigated using secondary electrons (SE). The size of the targets is less than 1 μm, thus allowing

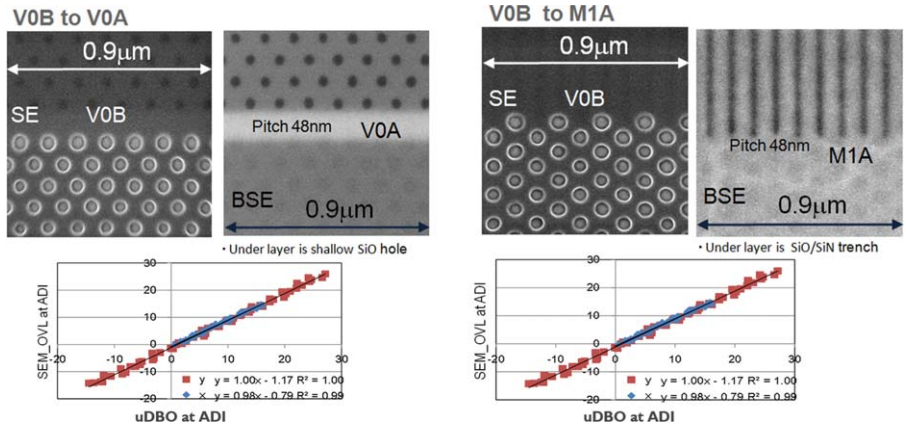

Fig. 1. (Color online) (Left) SEM-based overlay V0B to V0A; (Right) SEM-based overlay V0B to M1A.

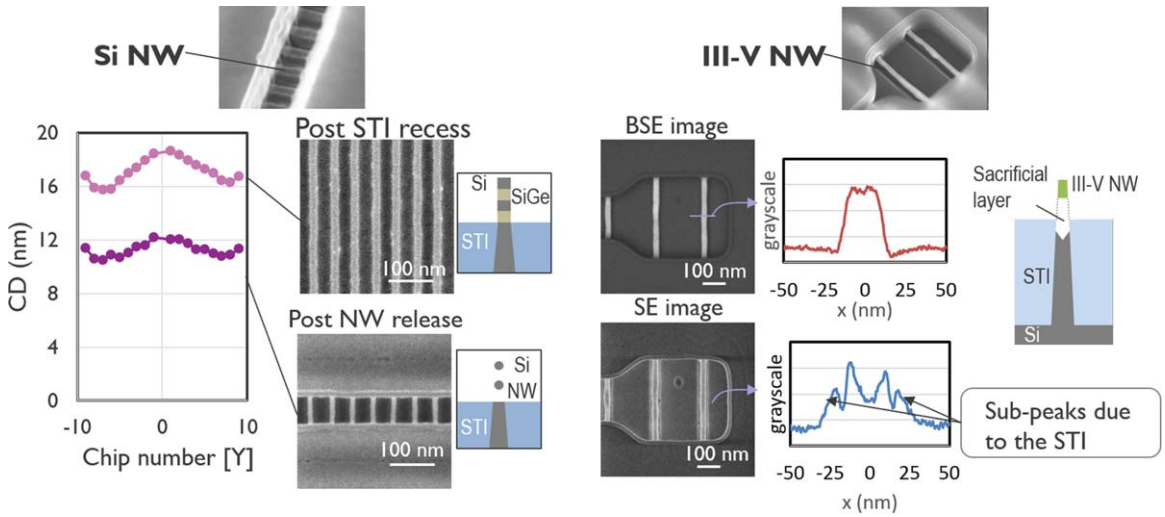

Fig. 2. (Color online) (Left) Metrology of Si lateral NW; (Right) metrology of III–V lateral NW.

in-chip overlay characterization near the device structures for high order corrections. The comparison of SEM-based overlay with diffraction-based overlay (Fig. 1, bottom) indicates the very good quality of the CD SEM results, obtained by using the high voltage CD SEM CV5000.

2.2. NW metrology

Gate-all-around NW transistor is regarded to be a key device to overcome the short channel effect, as an extension of triple-gate finFET. The metrology of NW structures presents a variety of issues that need to be addressed. We report here results for both lateral and vertical NW. The basic requirement of NW metrology lays in the ability to perform consistent CD evaluation. In Fig. 2 (Left), we compare the across wafer signature of silicon fins (post STI recess) and NW (post NW release). The signature, beside an expected offset in CD, is clearly comparable in the two cases, thus indicating that the NW metrology is indeed reliable and provide meaningful information.

In Fig. 2 (Right), we report metrology results on III–V lateral NW. The SE image clearly indicates the presence of spurious sub-peaks in the electronic signal, caused by the STI structure. They would negatively affect the NW metrology results in terms of both repeatability and accuracy. However, these spurious peaks can be avoided if BSE signal is used, as shown in Fig. 2 (Right), thus solving such a metrology issue on III–V NW. These results were obtained on CG6300 CD SEM.

Beside the standard CD metrology qualification of NW, there is a growing interest in investigating defectivity for both vertical and lateral NW. In Fig. 3 we show the results of a defectivity investigation aimed to detect the level of failures in standing vertical NW. The results clearly indicate the possibility to use standard CD SEM (CG6300 in this case) to estimate the success rate in the construction of vertical NW.

2.3. Contrast inspection of Si NW with SEM voltage contrast (VC)

The NW release step is the critical step in the NW FET fabrication. The released NWs are suspended over the gate trench. It is supported only by narrow contacts between NW and source/drain (SD), as shown in Fig. 4. This means that the mechanical stress at the contact region or the undergrowth of the SD easily results in the electrical defect. The inspection of NW-SD contacts is therefore important. However, inspection of physical defects at the NW-SD interface is difficult by top-down inspection because the interface is concealed by the spacer above it. Alternatively, electrical defect inspection would be an option.

An electrical defect inspection method utilizing SEM VC is well-established as a non-destructive inline method. VC is a kind of SEM signal contrast which is caused by the surface

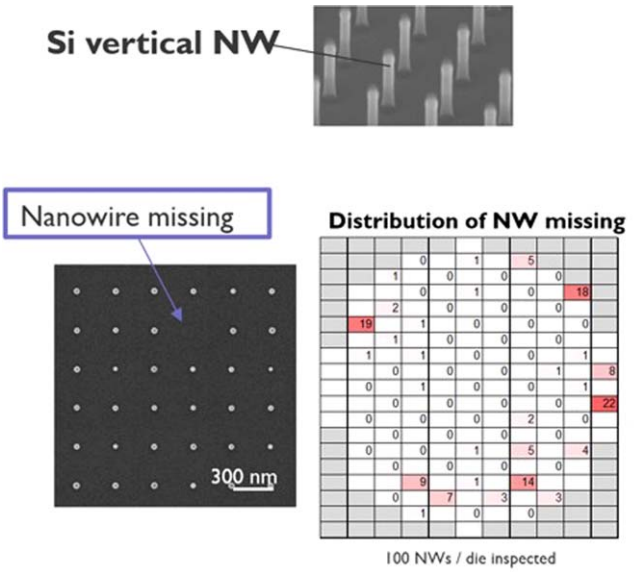

Fig. 3. (Color online) Defectivity of vertical NW.

potential difference. Electrical defects cause the electron beam (EB) -induced charging which is appeared as VC. The mechanism of VC is shown in Fig. 5. Figure 5(a) is a typical energy spectrum of SEs. If the sample surface is not charged, all SEs can be detected. On the other hand, if the sample is charged positively, SEs are decelerated by the surface potential [Fig. 5(b)]. It means that low-energy electrons cannot be detected because they are unable to escape from the surface potential and trapped back into the sample. The obtained SEM signal is therefore decreased by surface charging. Electrical defects can be inspected by means of detecting this signal decrease.

A powerful technique to enhance VC is energy filtering of SEs. With energy filtering, only SEs whose energy is higher than the threshold energy can be detected through the energy filter, as shown in Figs. 5(c) and 5(d). The SE energy spectrum has a peak below 50 eV in general. Thus, the decrease of the detected SEs due to surface potential is enhanced by setting the threshold energy at around the peak of the SE spectrum.

VC-based inspection is already established for local contact and DRAM capacitor.[18–20] The method should be applicable to NW-SD contact inspection, although there is no experimental verification yet. The first one of the two purposes of this study is to verify the validity of the VC-based NW-SD contact inspection.[21,22]

Furthermore, it would be valuable if parasitic resistance and capacitance can be measured. It is already reported that rough estimation of parasitic resistance is possible by evaluating VC.[23] Pulsed irradiation of EB by a special apparatus has been applied to analyze the charging dynamics which gives information of both of resistance and capacitance.[24] However, estimation of resistance and capacitance has not been realized by a conventional SEM with continuous EB irradiation. We propose alternative approach to investigate and quantify the charging dynamics by continuous EB irradiation. Changing the scan speed of EB is equivalent to changing the duration of continuous EB irradiation on single NW. The transient behavior should be observed in case that the duration time is comparable to the charging relaxation time. Thus, a quantitative analysis on the VC images acquired with different scan speeds would enable the parasitic resistance and capacitance estimation. The second purpose of this study is to investigate the feasibility of resistance and capacitance measurement of NW FETs.

2.3.1. NW-SD contact inspection result by VC. Figure 6 shows typical SEM images acquired with and without energy filtering of SEs. One of the NWs is clearly appeared darker than other NWs with energy filtering [Fig. 6(a)], though the gray level of all NWs is almost the same without energy filtering [Fig. 6(b)]. It means that gray level decrease is VC caused by the charging of the NW, namely, there is an electrical contact issue in the dark NW. This result suggests that VC is effective for the contact inspection of NW FETs.

Figure 7(a) shows the histogram of mean gray level of each NW in the image taken with energy filtering (hereafter called "VC image"). Clearly, there are two peaks in the histogram. They should correspond to the NWs with electrical defect (darker NWs) and normal NWs (bright NWs). A dashed line in Fig. 7(a) should be a good criterion to separate the defect NWs and the normal NWs. The ratio of the defect NWs in the inspected NWs for each die is shown as a wafer map in Fig. 7(b). This inspection revealed that the electrical defects are more frequent at wafer edge than at wafer center. Such data should be valuable for process monitoring and failure analysis of the contact issue.

2.3.2. Verification of inspection results with TEM. The obtained cross-sectional TEM images are shown in Fig. 8, together with the VC images of the same NWs. The epitaxial

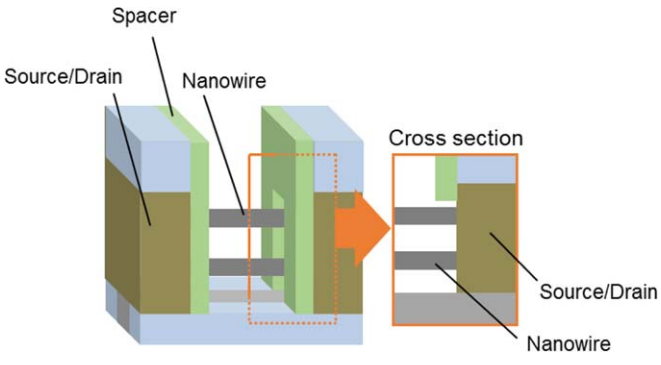

Fig. 4. (Color online) Schematic configuration of NW FET and its cross-section parallel to the NW.

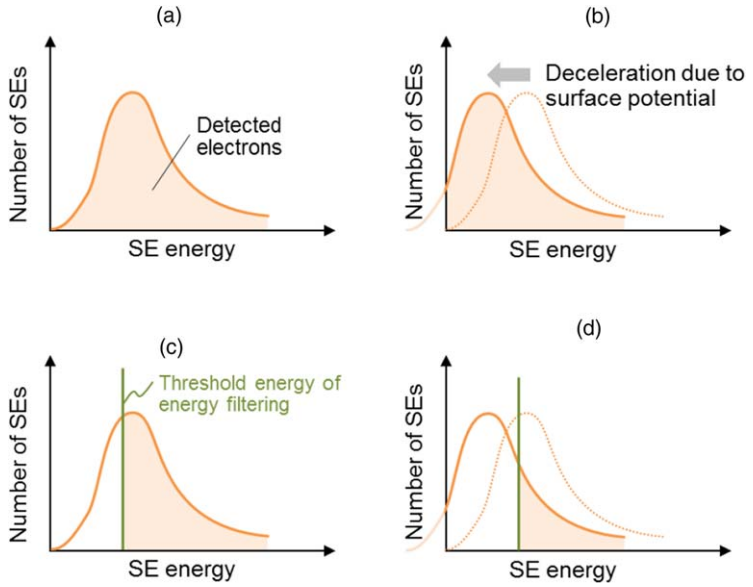

Fig. 5. (Color online) Typical energy spectrum of secondary electrons. (a) Not charged surface without energy filtering of secondary electron, (b) positively charged surface without energy filtering, (c) not charged surface with energy filtering, and (d) charged surface with energy filtering. The colored area corresponds to the detected electrons. The vertical bold line is the threshold energy of energy filtering.

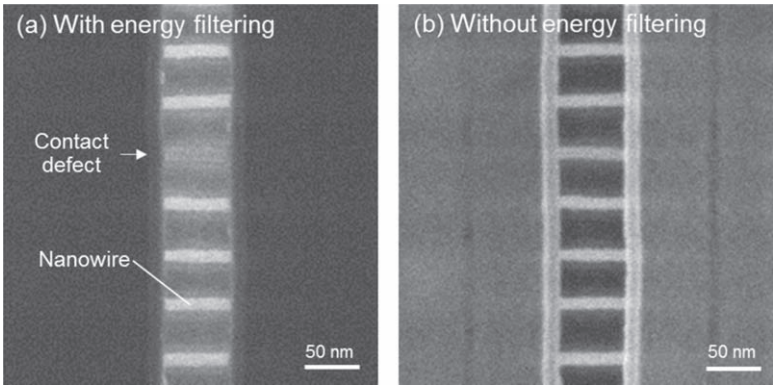

Fig. 6. (a) A typical SEM image acquired with energy filtering of secondary electrons. (b) A SEM image acquired without energy filtering at the same field of view. Voltage contrast is clearly observed by energy filtering.

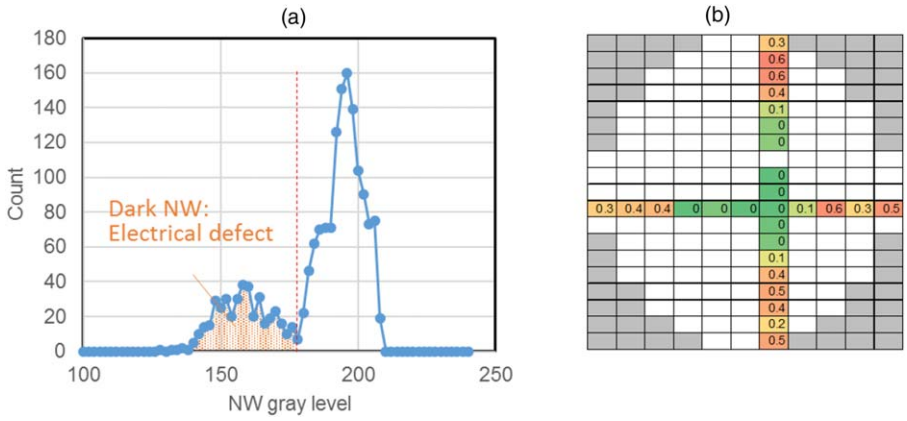

Fig. 7. (Color online) (a) Gray level histogram of 1680 nanowires. The dashed line is a criterion between dark NWs and bright NWs. The dark NWs should correspond to the electrical defects. (b) Intra-wafer map of the ratio of defect NWs. Electrical defects are more frequent at wafer edge.

growth of SD is insufficient, so that contacts between upper NWs and the SD region are not formed well. In some cases, there is a connection with narrow SD path (labeled by "C" in Fig. 8). In other cases, the NW is not connected to SD region (labeled by "NC" in Fig. 8). Comparison between the TEM images and the VC images clarifies that the dark NWs in VC images are floating NWs which are not connected to SD at either end. Such correspondence is confirmed in all tested NWs. This result verifies the validity of the VC-based contact inspection.

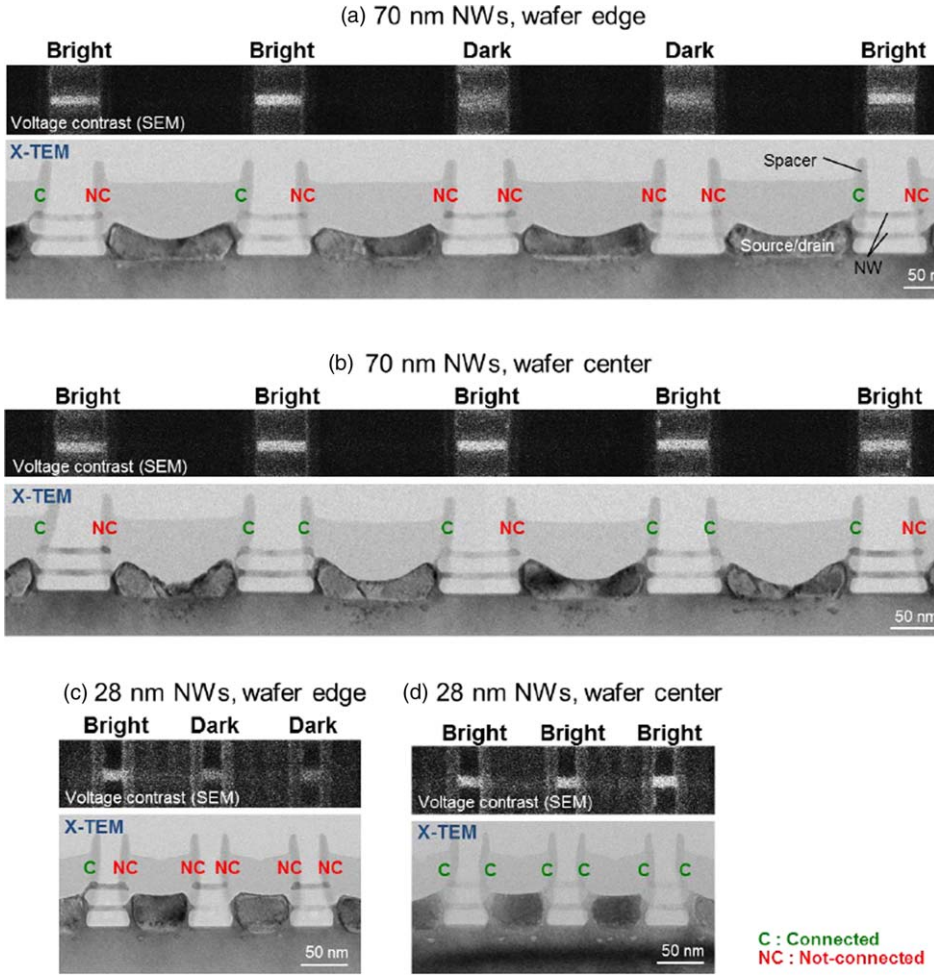

Fig. 8. (Color online) Comparison between SEM voltage contrast images and cross-sectional TEM images of the NWs. (a) 70 nm long NWs at wafer edge, (b) 70 nm long NWs at wafer center, (c) 28 nm long NWs at wafer edge, and (d) 28 nm long NWs at wafer center. "C" and "NC" indicate connected and not connected interface between NW and SD. It is confirmed that dark NWs in the voltage contrast image are not connected to SD region at either end.

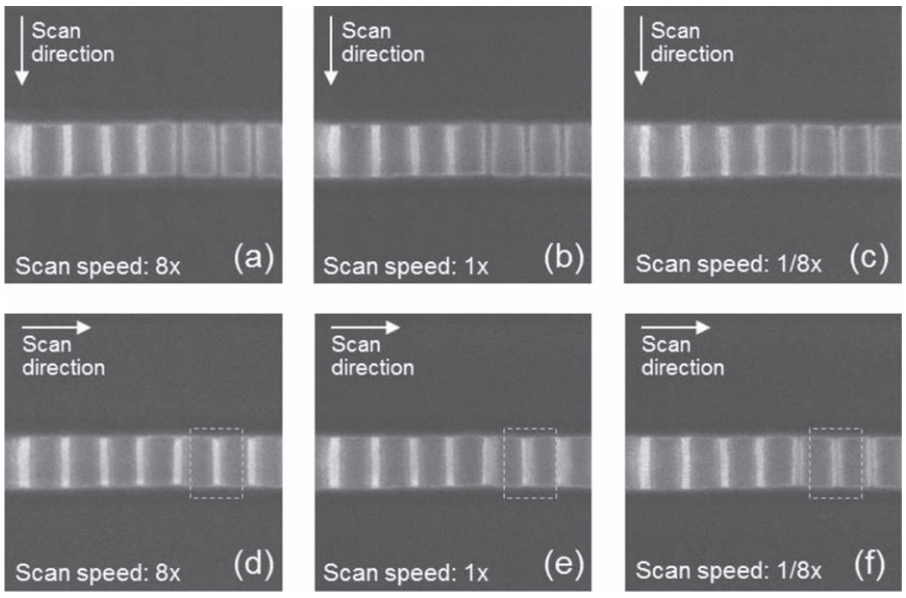

Fig. 9. Voltage contrast images with different scan speeds and directions. (a), (b) (c) Scan parallel to NWs with 8×, 1×, and 1/8× scan speeds, respectively. (d), (e), (f) Scan across NWs with 8×, 1×, and 1/8× scan speeds, respectively.

2.3.3. Resistance and capacitance estimation. The SEM images shown in the previous sections were taken by scanning EB parallel to NWs. In these images, VC due to electrical defects was clearly observed. However, VC was suppressed when EB scans across NWs. Figure 9 shows the VC images taken at the same field of view with different scan speeds and directions. VC was clearly observed regardless to the scan speed in case of scanning parallel to NWs. In

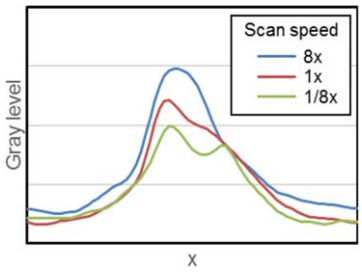

Fig. 10. (Color online) VC profiles of the NW indicated by dashed boxes in Fig. 9.

contrast, VC was less significant for faster scan in case of scanning across NWs. This tendency can be interpreted by considering the duration of continuous EB irradiation on single NW. It becomes shorter for faster scan, resulting the lower NW potential due to EB-induced charging.

For detailed analysis, VC profiles of the NW were extracted from dashed boxes in Figs. 9(d)–9(f), as shown in Fig. 10. They were taken from the same NW with different scan speed. One important feature in the VC profiles is that SEM signal is suppressed by charging particularly at around the top of the peak. This is because that the injected current is high when EB scans the center of NW. On the other hand. the NW potential would be too low to make significant decrease of the SEM signal when EB scans around the side of the NW. Another remarkable feature is that the suppressed profiles are asymmetric. This is due to the charging dynamics. Charing phenomena has its relaxation time which can be approximated by RC if a simple RC circuit is assumed. It means that the charging potential increases during the scan across the NW if relaxation time is longer than or comparable to the scan duration. The SEM signal from right half (latter haft) of NW is, therefore, more affected by charging. These features imply that a quantitative evaluation of these VC profiles would enable the estimation of parasitic resistance and capacitance.

Parasitic resistance and capacitance were estimated by finding the best-fit parameters in the proposed VC model to reproduce the experimentally obtained VC profiles. Figure 11 shows the results of systematic model calculation. 16 combinations of resistance, R, (100, 200, 400, and 800 GΩ) and capacitance, C, (1, 2, 4, and 8 aF) were used as input parameters of the model calculation. Other model conditions, such as accelerating voltage, probe current, scan speed, were set the same as the experimental conditions. The characteristic features discussed in the previous paragraph, namely, the signal decrease at the center and the asymmetric profile, were reproduced by the model calculation. It suggests that the proposed model adequately describes the charging dynamics. Among the calculated series of profiles, the result with $R = 200$ GΩ and $C = 2$ aF matches the experimental results (Fig. 10) most similarly. This matching should be reliable because it is based not only on the shape similarity of each profile, but also on the trend similarity of scan speed dependence. Therefore, the resistance and capacitance were estimated to be 200 GΩ and 2 aF, respectively. Such quantitative evaluation should be valuable for more accurate inspection.

In addition, the capacitance measurement gives the information on the defect point where the electrical connection is hindered. The capacitance between the upper NW and the lower NW can be calculated by the following analytical formula

$$C = \frac{l\pi\varepsilon_0}{\log\left(\frac{h}{a} + \sqrt{\left(\frac{h}{a}\right)^2 - 1}\right)},$$

where a is the wire diameter, h is the distance between two stacked NWs' center, and l is the NW length. By approximating $a = 10$ nm, $h = 20$ nm, and $l = 70$ nm according to the actual NW dimension, the capacitance between stacked NWs is found to be about 3 aF. The value is consistent with the measured capacitance. It suggests that upper NW is electrically disconnected from the lower one. Thus, most probable defect point is the interface between the upper NW and SD. Such presumption is possible by measuring the parasitic capacitance without performing the physical analysis, such as cross-sectional TEM.

2.4. Correlation with electrical performance for STT-MRAM

Emerging non-volatile memory devices are being studied extensively in order to close the access-time gap between memory and storage. Among them, STT-MRAM is considered one of the promising candidates, owing to its low power consumption, low latency, and excellent endurance. The memory element of a STT-MRAM device is a magnetic tunnel junction (MTJ) pillar, which consists of an ultrathin MgO layer sandwiched by two ferromagnetic layers (Fig. 12, Left). The MgO layer will have a high or low tunneling resistance, depending on the magnetization polarity of the ferromagnetic layers. This resistance difference is used as a memory bit. One disadvantage of STT-MRAM is its narrow resistance window. As a consequence, cell-to-cell resistance uniformity is critical to ensure reliability for these devices. Since the resistance of the MgO layer is ideally inversely proportional to its area, physical area control is essential. It is equally important to evaluate the area-independent variability of the resistance, caused by various additional process variations, as it affects the operable memory window. For these reasons, correlation study between area and resistance of STT-MRAM cells was performed.[25)]

The physical area of the memory element was measured by CD-SEM. However, a direct measurement of the MTJ pillars after etching was not possible because in situ encapsulation is required to avoid damage to the MTJ. Thus, measurements were performed after hard mask etching and after encapsulation (Fig. 12, Right). The area difference due to the step difference was corrected by utilizing the results of a dummy wafer which was measured at all steps, namely, after hard mask etching, after MTJ etching, and after encapsulation. The offset between physical dimension of the MgO layer and measured value was also calibrated. 852 pillars with different sizes (60–100 nm in design) were tested for statistical analysis. The calibrated area was compared with the conductance of the same pillar, which is the inverse of the measured resistance at low-resistance state. The variation of MgO thickness across a wafer due to in-process variations was taken into consideration in the analysis.

The conductance of the measured pillars showed obvious linear correlation to their area, besides the case of shorted pillars (Fig. 13, Left, lower plot). This indicates that the

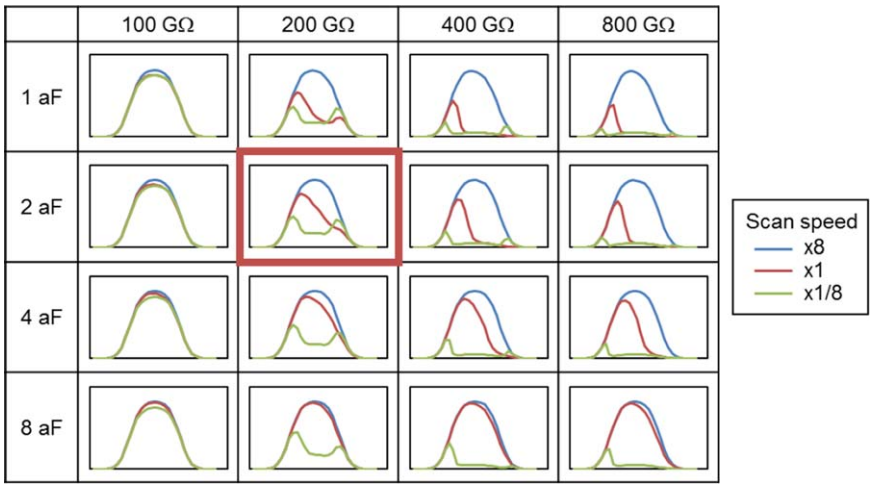

Fig. 11. (Color online) VC profiles calculated by the proposed VC model. 16 combinations of resistance ($R = 100$, 200, 400, and 800 GΩ) and capacitance ($C = 1$, 2, 4, and 8 aF) were used as input parameters of the model. Among these series of VC profiles, the result with $R = 200$ GΩ and $C = 2$ aF is most similar to the experimental result.

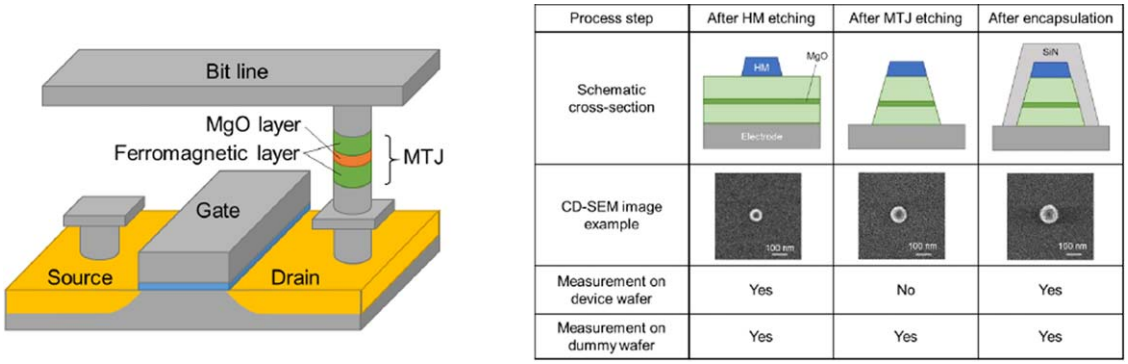

Fig. 12. (Color online) (Left) Typical configuration of STT-MRAM; (Right) schematic cross-sections of a memory pillar and typical CD-SEM images at each process step.

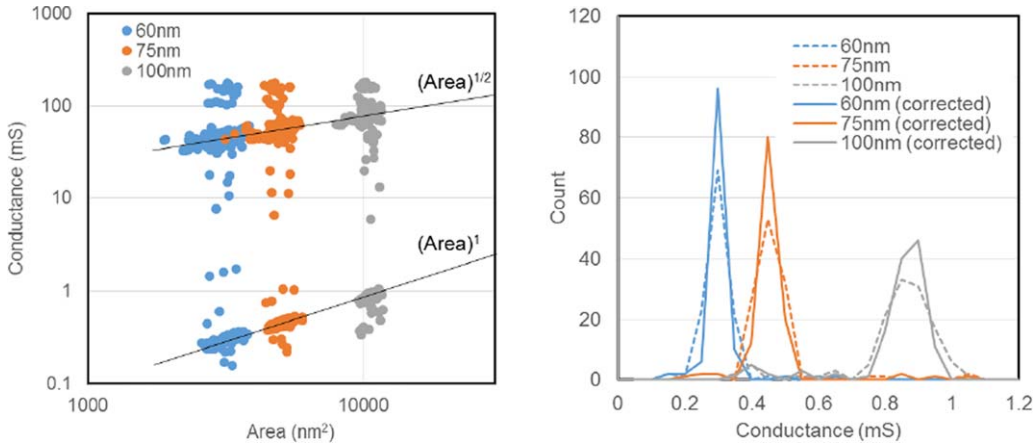

Fig. 13. (Color online) (Left) Correlation plot of area and low-resistance-state conductance of the memory pillars; (Right) histograms of conductance without and with the correction of the area-induced variability.

conductance is affected by the area variability of MTJ pillars, as expected. Efficient size control should be then effective in improving cell-to-cell conductance uniformity. Meanwhile, the conductance of the shorted pillars was observed to be proportional to the square root of the area (Fig. 13, Left, upper plot). This suggests that leakage occurred along the sidewalls of the pillar.

Area-independent conductance variability can be quantified by correcting for the size dependence. The conductance spread of the normal pillars, defined by the interquartile range, was observed to be 14% of the median conductance when the area-induced variability was not corrected, while the spread was down to 9% when it was corrected (Fig. 13, Right). This indicate that the variability of the investigated devices is not only related to size variations, but to process variation as well. Such an analysis provides then useful information when investigating the root causes of variability.

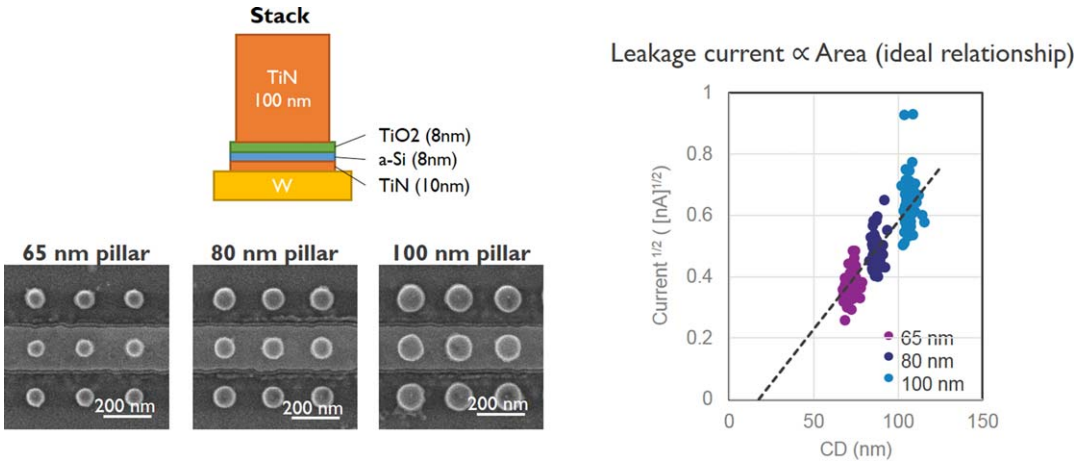

Fig. 14. (Color online) (Left) ReRAM VMCO schematic structure and CD SEM images of the pillars. (Right) Correlation between CD and square root of current.

In summary, correlation analysis between physical size and resistance of STT-MRAM pillars was performed. The result indicates that the resistance variability can be reduced by size control. It was also concluded that this approach is useful for the failure analysis and the quantification of the size-independent resistance variability.

2.5. Correlation with electrical performance for ReRAM VMCO

Another promising candidate of emerging memories is ReRAM whose resistance window is sufficiently large. In Fig. 14 (Left), we report the schematic structure of an ReRAM VMCO memory device. In our case, pillar of 65, 80, and 100 nm were characterized. The electrode below the central row is clearly visible in the pictures. Figure 14 (Right) confirms the correlation between CD and square root of current. The large spread observed indicates the presence of other contributors beside CD to electrical variability.

2.6. 3D NAND ONO (oxide nitride oxide) thickness measurements

A conventional planar NAND device consists of a stack of tunnel oxide—floating gate—inter gate dielectric films [Fig. 15(a)]. On the other hand, a 3D-NAND device has a memory hole which is filled with a vertical channel surrounded by the tunnel oxide–nitride—blocking oxide film, namely the ONO film [Fig. 15(b)]. The thickness of the ONO film stack needs to be controlled precisely since it is directly related to the memory performance. The threshold voltage depends on the thickness ratio among the tunnel oxide, nitride, and blocking oxide films. Data retention is affected by the tunnel oxide thickness.

Currently, instead of measuring the ONO film thickness on the sidewall, the one on a flat surface of the patterned wafer or an unpatterned dummy wafer is measured by conventional ellipsometry. However, the measured thickness is different from that of the vertical film in the actual device at the hole sidewall. Furthermore, hole-to-hole thickness variation cannot be captured. Thus, a local thickness measurement method of the film deposited on the hole sidewall is needed.

A TEM is one of the possible solutions.[26] However, it is a destructive method which cannot be applicable to the inline monitoring. Moreover, a precise measurement is difficult because the sample preparation procedure easily affects the results. The thickness margin of the ONO film would be 1 nm since its typical thickness is about 10 nm. With this assumption, a measurement with 0.1 nm precision is required. It is quite difficult to achieve by TEM. There is no established method to measure the thickness of a vertical film with such high precision.

We propose a CD-SEM as a suitable tool for the thickness measurement of a vertical film.[27,28] It seems possible for the top-down observation tool in principle. However, sufficiently high precision (~0.1 nm) would be challenging. It is also to be examined if the result of the top-down measurement can be regarded as the typical thickness of the film covering from hole bottom to hole top. In this study, two different approaches for the ONO film thickness measurement were examined. Their precision and validity were evaluated by comparing with the results of a TEM and ellipsometry.

2.6.1. ONO process. The structures used in this experiment are memory holes in 3D-NAND test wafers. Figure 16 shows the schematic process flow of the ONO film deposition and etching.[9] After the first etching [Fig. 16(a)], the memory hole receives the deposition of the blocking oxide film [Fig. 16(b)], the nitride film [Fig. 16(c)], the tunnel oxide film [Fig. 16(d)], and the amorphous Si (a-Si) film [Fig. 16(e)] sequentially, followed by the ONO etching [Fig. 16(f)] to remove the ONO film at the hole bottom. The a-Si film protects the ONO film on the sidewall during the ONO etching.

After the ONO process, the memory hole is filled with a-Si or covered with a-Si thin layer which is afterwards annealed to form the poly Si channel (not shown in Fig. 2). A TEM cross-section of a tested memory hole after ONO etching is shown in Fig. 17.

2.6.2. Thickness measurement methods with CD-SEM. Figure 18 shows typical CD-SEM images acquired at each process step with CG5000 (Hitachi). The hole size decreases step by step in the deposition process. After ONO etching, double rings can be observed clearly. By utilizing these images, two different methods are possible to measure the film thickness as shown in Fig. 19. The first method (method 1) is defining the film thickness as the hole size difference caused by film deposition on the memory hole. The hole diameter should decrease by twice the deposited file thickness. The second method (method 2) is measuring the film thickness by the spacing between the outer and the inner

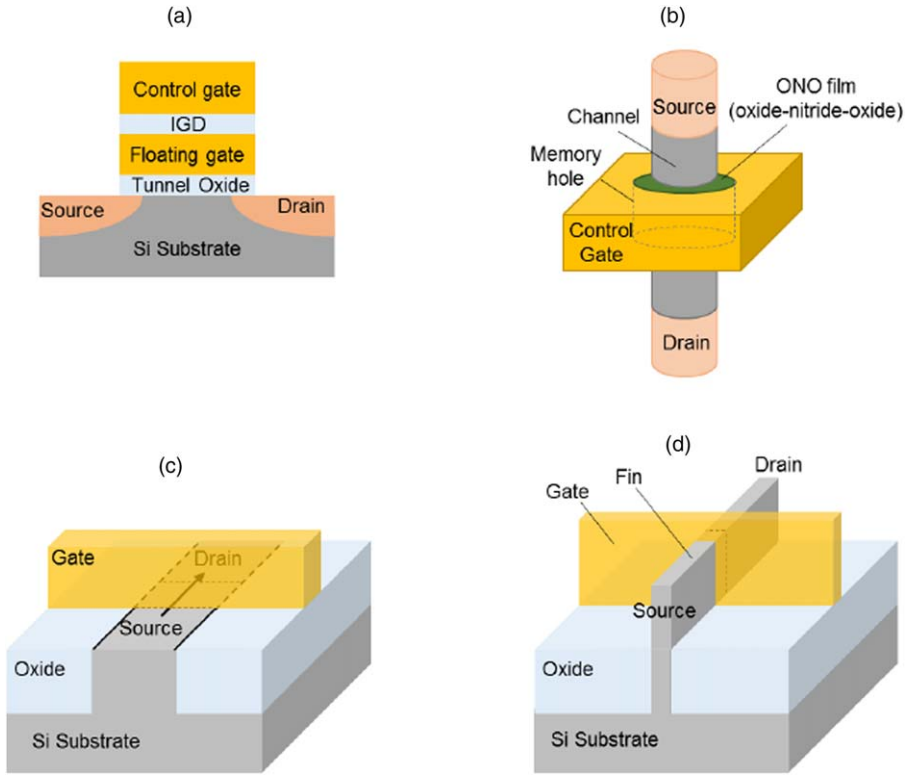

Fig. 15. (Color online) Schematic structures of (a) a planar NAND flash, (b) a 3D-NAND flash, (c) a planar FET and (d) a fin-FET device.

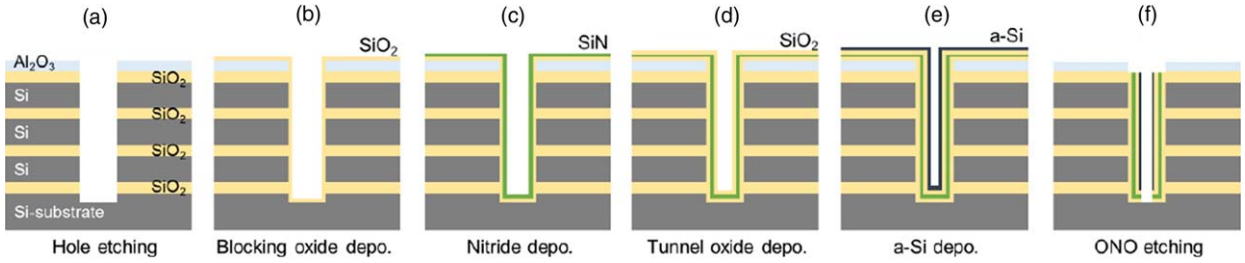

Fig. 16. (Color online) Schematic process flow of the ONO film deposition and etching. (a) Hole etching, (b) blocking oxide deposition, (c) nitride deposition, (d) tunnel oxide deposition, (e) amorphous Si deposition and (f) ONO etching.

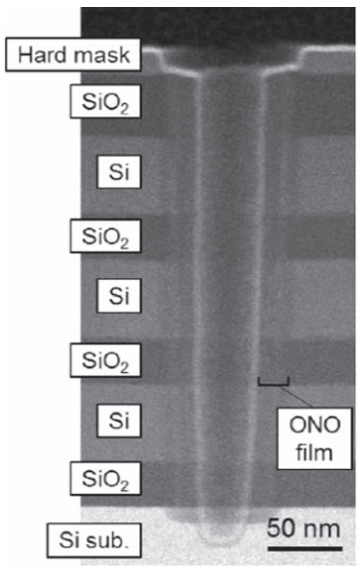

Fig. 17. A typical cross-section of the memory hole observed by a TEM after the ONO etching.

rings of the double rings. In both methods, the thickness can be expressed as follows

$$t = (d1 - d2)/2,$$

where, t is the thickness of the film, $d1$ and $d2$ are the hole diameters before and after deposition for the method 1 and the diameters of outer and inner rings for the methods 2. The method 1 was applied to the ONO deposition steps [Figs. 18(a)–18(d)] and the method 2 is applicable to the ONO etching step [Fig. 18(f)].

2.6.3. Precision and validity. The precision was evaluated by repeating identical measurements twice on a spot. The results of the first and the second measurements on each hole should be same in ideal. Namely, the difference between them is the measurement error. The measurement precision can be evaluated by the variability of this difference. It is corresponding to the data spread around the ideal line in the correlation plot between the first and the second measurement results (Fig. 20). Quantitatively, 3σ precision of the measurement was defined by $3/\sqrt{2}$ of the standard deviation of the

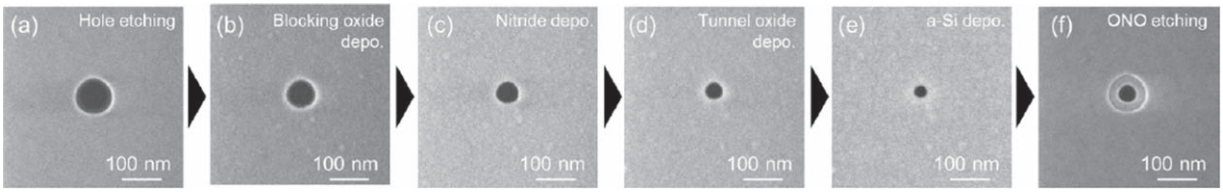

Fig. 18. CD-SEM images obtained at (a) hole etching, (b) blocking oxide deposition, (c) nitride deposition, (d) tunnel oxide deposition, (e) amorphous Si deposition and (f) ONO etching steps.

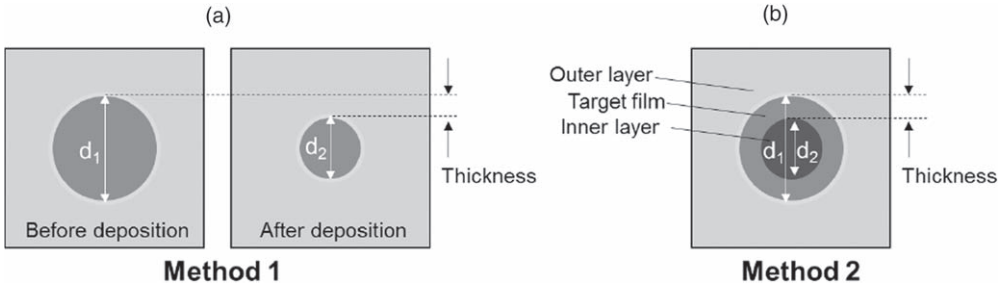

Fig. 19. Two methods for the thickness measurement. (a) A method defining the film thickness by the hole size difference between before and after the film deposition on the hole [Figs. 18(a)–18(d)]. (b) A method measuring the film thickness directly from the spacing of the double rings [Fig. 18(f)].

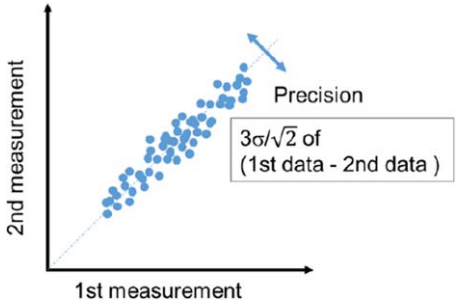

Fig. 20. (Color online) Evaluation method of measurement precision.

first-to-second difference. The thickness precision and the hole diameter precision were calculated with this procedure for both methods 1 and 2.

The validity of the methods was examined by comparing with reference results obtained by a planar TEM. A typical planar TEM image of a lamella cut out from the middle of the memory hole is shown in Fig. 21(a). The schematic diagram of the stack information is shown in Fig. 21(b). The thickness of the ONO film was measured from the TEM images. 8 targets were measured in total. The measured thickness was averaged over 5 holes which were selected within 2 μm distance from the CD-SEM measurement location. Thus, the averaged thickness of the TEM-measured holes should be a representative thickness of the CD-SEM-measured holes.

Another reference was conventional ellipsometry. It can capture the intra-wafer trend which is difficult to obtain by time-consuming TEM measurement. Although the ellipsometry result is different from the thickness of the vertical film, the relative trend across a wafer should serve as a reference. The ellipsometry was performed on an unpatterned test wafer which had received the same film deposition process. The thickness variation over the wafer was compared with the CD-SEM result.

2.6.4. Precision results. The precisions of thickness measurements with several threshold conditions are shown by the solid lines in Fig. 22. The best precision was found to be 0.10 nm and 0.07 nm for the method 1 and 2, respectively. Both methods satisfy the precision requirement (0.1 nm) for the reliable measurement of the ONO film thickness.

The dashed lines in Fig. 22 represent the precision estimated from the precision of hole diameter (method 1) or ring diameter (method 2) by the following equation

$$\text{Thickness precision} = \sqrt{\left(\frac{\text{Precision of } d_1}{2}\right)^2 + \left(\frac{\text{Precision of } d_2}{2}\right)^2}.$$

This equation is valid if the measurement errors of $d1$ and $d2$ are independent of each other. The actual and the estimated precisions are consistent in the method 1 as shown in

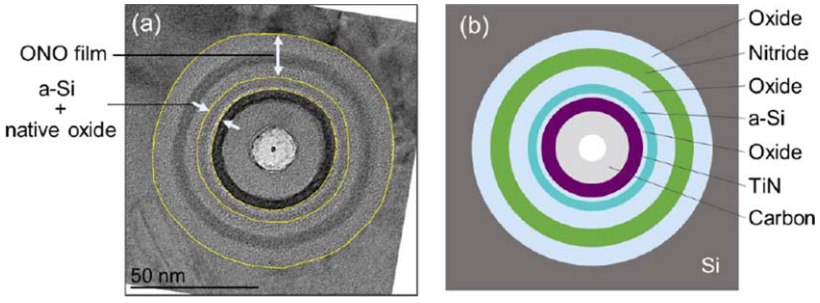

Fig. 21. (Color online) (a) A typical planar TEM image obtained at the middle height of the hole after ONO etching. (b) A schematic diagram of the film stack.

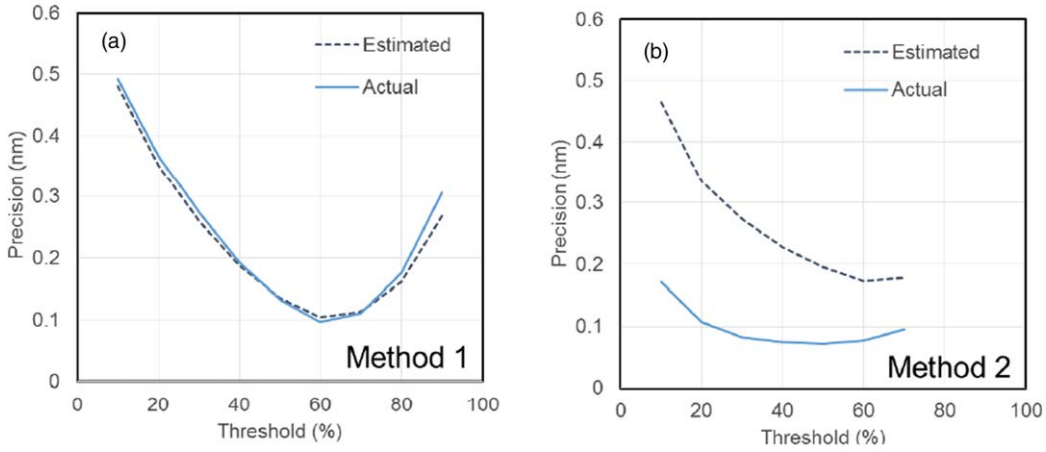

Fig. 22. (Color online) The evaluated thickness measurement precision of (a) the method 1 and (b) the method 2. The bold lines are the experimentally obtained precision. The dashed lines are the estimated precision from the combination of the precision of the hole or ring diameter measurements.

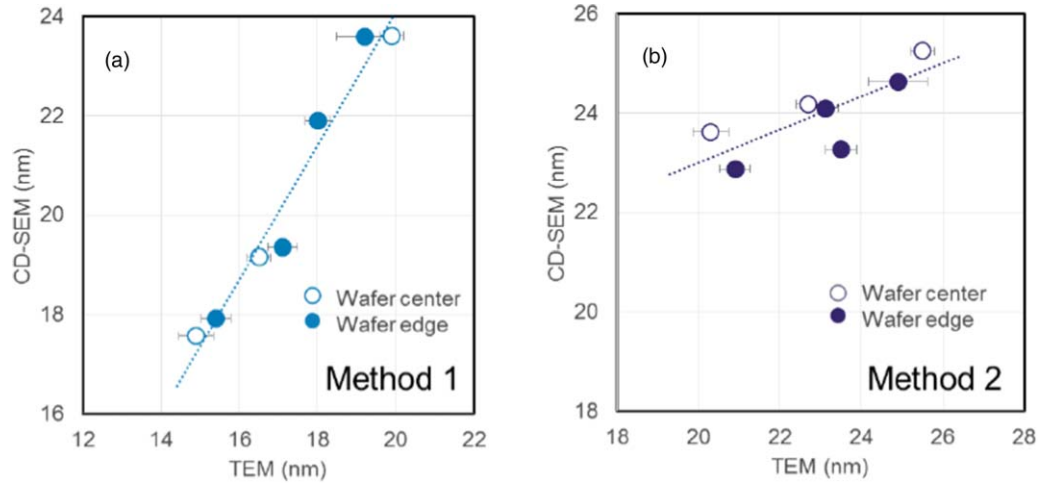

Fig. 23. (Color online) 10 Comparison between TEM results and the CD-SEM results of (a) the method 1 and (b) method 2. The method 1 provides more consistent results with the TEM results.

Fig. 22(a). On the other hand, the actual precision is much better (i.e., the value is smaller) than the estimation in the method 2 as shown in Fig. 22(b). It means that the considerable part of the measurement error of each ring diameter is not independent but correlated. Thus, it can be canceled out by subtracting one from the other. This is the reason of the better precision observed in the method 2.

2.6.5. Validity results. Comparison between CD-SEM and planar TEM results was shown in Fig. 23. Among 8 targets, one target resulted in unclear edges in TEM images due to the sample preparation issue. Thus, data of the 7 targets was plotted. The thickness of the ONO film was used in the comparison of the method 1 and the total thickness of the ONO film and the residual a-Si film was used in the method 2. Each data point represents the averaged thickness over 5 holes. The error bar was defined by the standard deviation of the result of 5 holes. The error bars of the CD-SEM results are not visible in the plot because they are shorter than 0.2 nm.

First, the measurement uncertainty of CD-SEM methods and TEM is discussed. The error bar length in Fig. 23 can be regarded as the combination of the local thickness uniformity and the measurement uncertainty. The short error bars of the CD-SEM results indicated that the local thickness uniformity is less than 0.2 nm. It means that the longer error bars (∼1 nm) of the TEM results are caused by their large measurement uncertainty. Less reproducible lamella preparation would be one of the degradation factors of TEM measurement. Consequently, CD-SEM is more suitable to evaluate the local uniformity.

Next, the sensitivity of the CD-SEM methods 1 and 2 is examined. The Fig. 23 clearly shows that slope of the regression line is steeper for the method 1. Quantitatively, the slope is 1.3 and 0.3 for the method 1 and 2, respectively. This means that the method 1 is more sensitive to the physical dimension difference.

Finally, the accuracy of the measurement result is addressed. The data deviation from the regression line is smaller for the method 1. This means that the method 1 is more accurate. A possible reason of the large deviation in the method 2 is the variation of step-like profile of the hole rim (Fig. 17). The data at the wafer center and the wafer edge is plotted by the open circle and the filled circle in Fig. 23(b). These two kinds of the data seem to align on the different trend lines. This could be due to the difference of the hole rim shape which is caused by the intra-wafer etching variation. Together with the better sensitivity, it is concluded the method 1 provided the more consistent results with the reference.

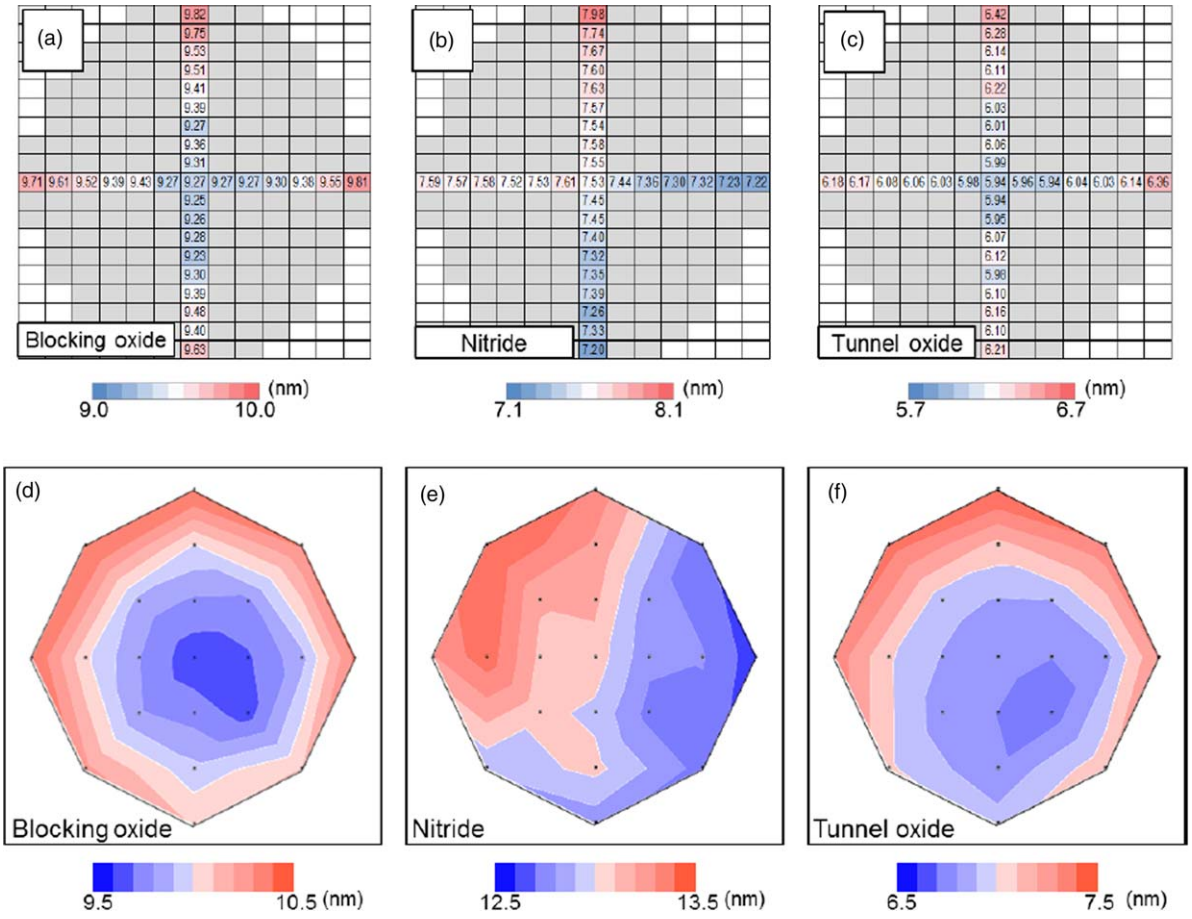

Fig. 24. (Color online) 11 Intra-wafer thickness trend of each film on the wafer 1 measured by (a)–(c) the CD-SEM (method 1) and (d)–(f) the ellipsometry 15.

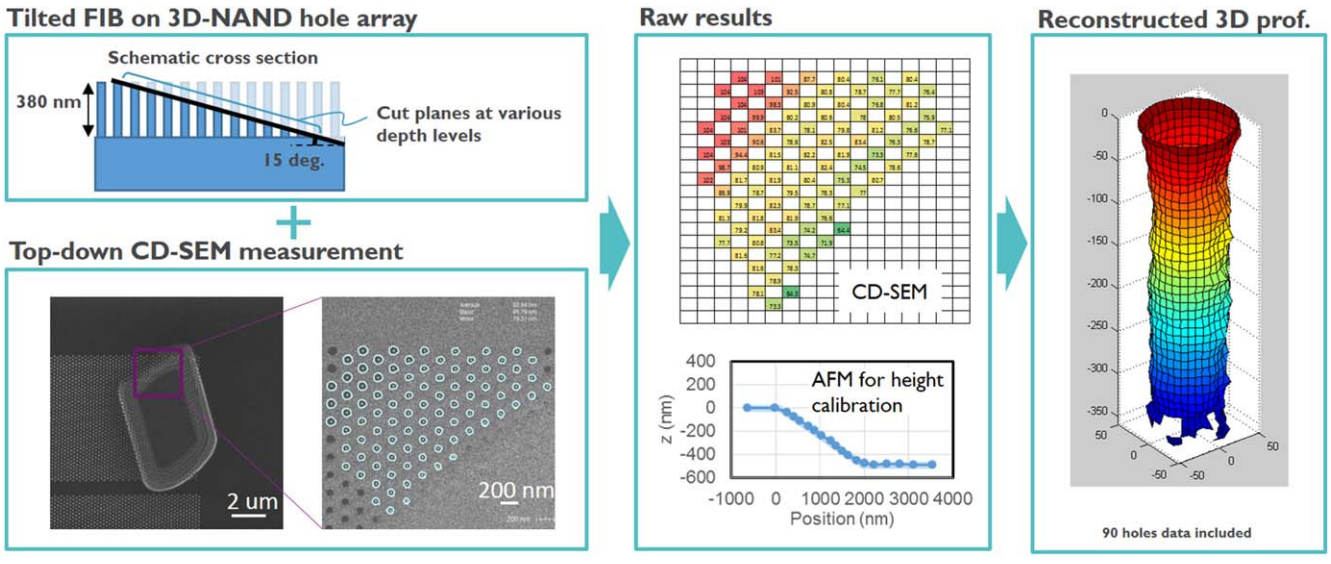

Fig. 25. (Color online) (Left) After a tilt FIB, the holes are measured in the sloped area; (Center) the measured CD is then correlated to the depth, as measured by AFM; (Right) CD as a function of the depth is extracted, thus providing a full 3D reconstruction of the average memory hole.

Figure 24 shows the thickness of each film in the wafer 1 measured by the CD-SEM (method 1) and the ellipsometry. The CD-SEM result shows the similar intra-wafer trend of the ellipsometry result although the measured value is smaller for the CD-SEM results. The thickness difference between the flat film on the blanket wafer and the vertical film on the hole sidewall is due to the limited supply of the source gas into the holes during deposition. These results also confirm the validity of the method 1.

2.7. 3D qualification of 3D NAND memory hole

The measurement of the three-dimensional shape of the high aspect ratio memory hole is a critical issue as well. CD SEM can be used in combination with FIB in order to extract high quality 3D information. The technique was already discussed

in a previous publication.[29–31] Here we apply this approach in order to reconstruct a 3D NAND memory hole. As shown in Fig. 25 (Top Left), the sample is subjected to a tilted FIB at a relatively shallow angle. A measurement of the CH array at all different depths is then executed by CD SEM, as shown in Fig. 25 (Bottom Left). In order to accurately anchor the depth of the measured holes sections, a reference AFM is performed, as shown in Fig. 25, (Center). Using these data, it is possible to obtain a full 3D reconstruction of the average hole, as shown in Fig. 25 (Right).

3. Conclusions

Our results cover a large variety of CD SEM applications. They indicate the central role that CDSEM will have in the development and quality control of the devices for advanced nodes. The investigation reported here shows how the CD SEM is evolving from being a reliable but basic tool for process monitoring, becoming a more flexible instrument, capable of investigating new inspection-type sort of application, as well as englobing novel monitoring strategies of advanced structures.

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