Inspection of 32nm imprinted patterns with an advanced e-beam inspection system

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Abstract

We used electron beam (e-beam) inspection (EBI) systems to inspect nano imprint lithography (NIL) resist wafers with programmed defects. EBI with 10nm pixel sizes has been demonstrated and capability of capturing program defects sized as small as 4nm has been proven. Repeating defects have been captured by the EBI in multiple die inspections to identify the possible mask defects. This study demonstrated the feasibility of EBI as the NIL defect inspection solution of 32nm and beyond.

Key words: NIL, J-FIL, EBI, program defects, repeating defects, 32nm

Introduction

As the feature sizes continue to shrink to nanoscale dimensions, optical lithography starts to run out of steam in resolution. Lithography scientists and engineers figured out many tricks such as immersion lithography and double patterning to enhance resolution and extend the lifetime of the optical lithography. The tricks come at the price of process complexity and cost of ownership. Alternative lithography solutions have been investigated for many years. Besides extreme ultra violet (EUV) lithography and electron beam (e-beam) direct write (EBDW) lithography, nano imprint lithography (NIL) is one of the candidates of alternative lithography solution for deep nanometer integrated circuit (IC) manufacturing. [1] Jet and Flash Imprint Lithography (J-FIL^{TM}) is a particularly interesting imprint approach. This novel technique involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. Because it is a room temperature process, it is also possible to address common integrated circuit manufacturing concerns such as throughput and overlay. Defect inspection solutions for both the imprint mask and NIL printed wafers are one of the major challenges of the NIL development, especially the NIL mask defect inspection, because of the small feature size due to its 1X nature. In comparison, EUV mask and optical lithography masks are 4X.

Because short wavelength and small beam spot, scanning electron microscope (SEM) could achieve much higher resolution than that of optical microscope, which resolution is limited by the diffraction effect of the longer optical wavelength. Although the resolutions of optical defect inspection system

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are not as high as EBI systems, their throughput and signal-to-noise (S/N) ratio are significantly higher, due to the large amount of photons the optical systems can focus on the inspection pixels. On the contrary, there are less than 1000 electrons an EBI system can focus on an inspection pixel with a high resolution beam condition in one scan, such as a scan rate at 100MHz, with an accompanying beam current of 10nA. Lower e-beam current is necessary to reduce the expelling interaction between electrons to achieve high-resolution, however, it causes significantly lower S/N ratio that contributes to shot noise of the SEM image and lower EBI throughput than its optical counterpart. Therefore, as long as the optical inspection system is capable of catching all the defects of interest (DOI), they will continue to be used for defect inspection applications. However, if some DOI cannot be captured by optical inspection systems because of resolution limitations, EBI systems can step in and play an important complementary role. It should also be noted that the electrical nature of defects, such as open circuit or short circuit underneath the surface layer, is beyond the capability of optical systems and EBI again can provide extremely useful information. Because of the small feature size, a combination of mask EBI and wafer EBI is the most likely solution for NIL defectivity for 32nm technology node and beyond.

Experiment Sample

In this study, a NIL mask with 48nm, 40nm and 32nm patterns and programmed defects was fabricated. The location and pattern of the program defects are shown in Figure 1 and the design of the different types of the program defects are illustrated in Figure 2.

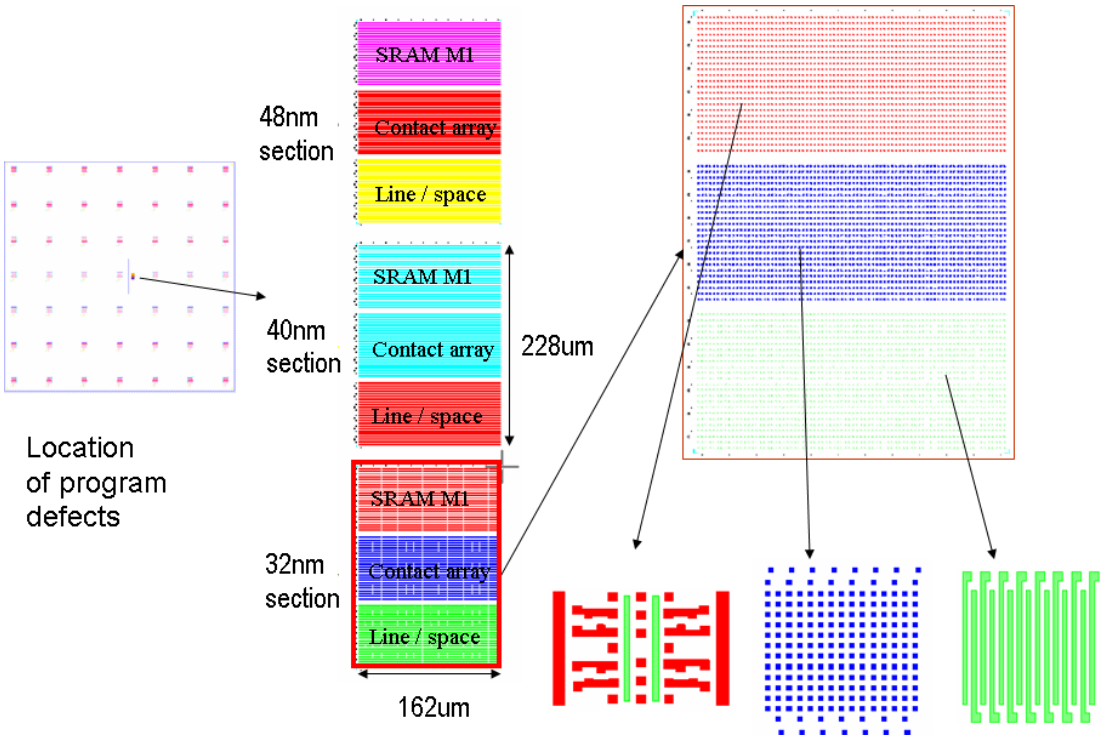

Figure 1. Location of the program defects and pattern layout.

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The designed size of program defect ranges from 4 nm to 48 nm, with an increment of 4nm. The patterns were transferred to NIL resist on a wafer using the Jet and Flash Imprint Lithography (J-FIL) process developed by Molecular Imprints, Inc. [2] NIL resist patterns on the wafer surface consisted of a static random access memory (SRAM) Metal 1 (M1) pattern, dense line space pattern in both horizontal and vertical directions, and dense arrays of pillars. [3] SEM images of the program defects on the mask and on a wafer are shown in Figures 3 and 4, respectively. In Figures 3 and 4, the defect size 1 to 6 indicates the designed program defect size, from 4 nm to 24nm with increments of 4nm.

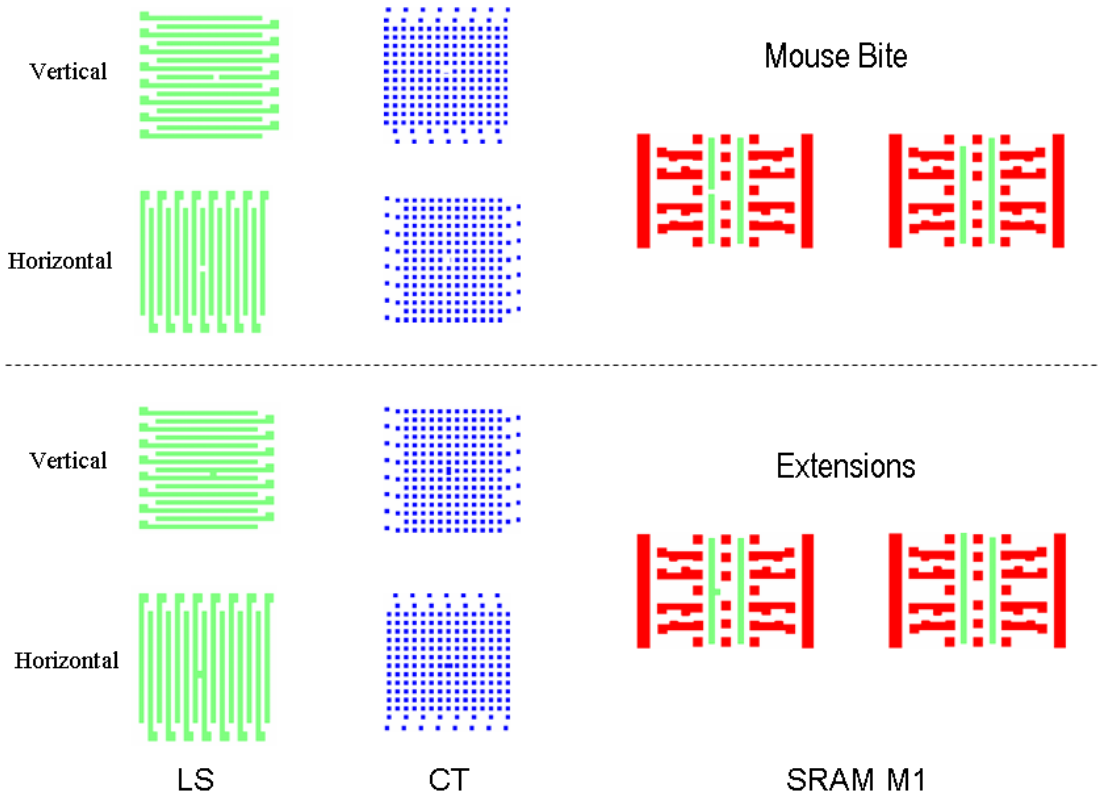

Figure 2. Illustration of different types of program defects. Both extensions and mousebite defects are included in the Metal1, line/space and pillar array patterns.

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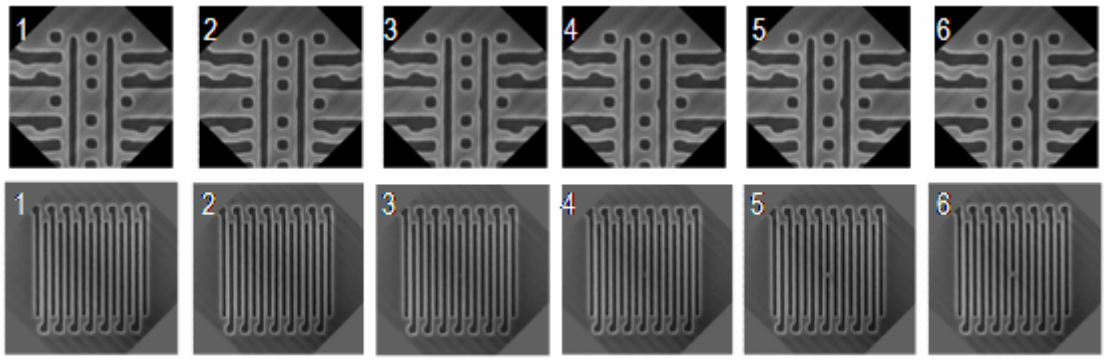

Figure 3. SEM images of the mask patterns for the Metal1 and line/space features. Programmed defects in the patterns ranged from 4nm (picture 1) to 24nm (picture 6).

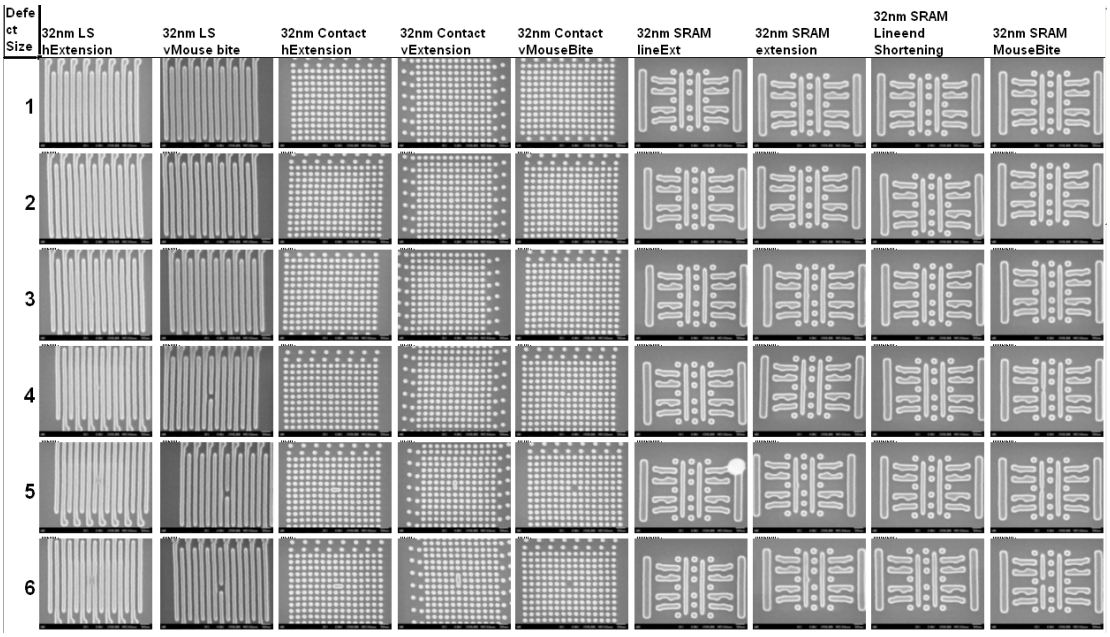

Figure 4. SEM images of imprinted features, including some program defects.

Experimental Equipment

In this study, we used an EBI system developed by Hermes Microvision, Inc. (HMI) to capture the program and process defects in the NIL resist patterns. eScan®315xp is designed for inspection of

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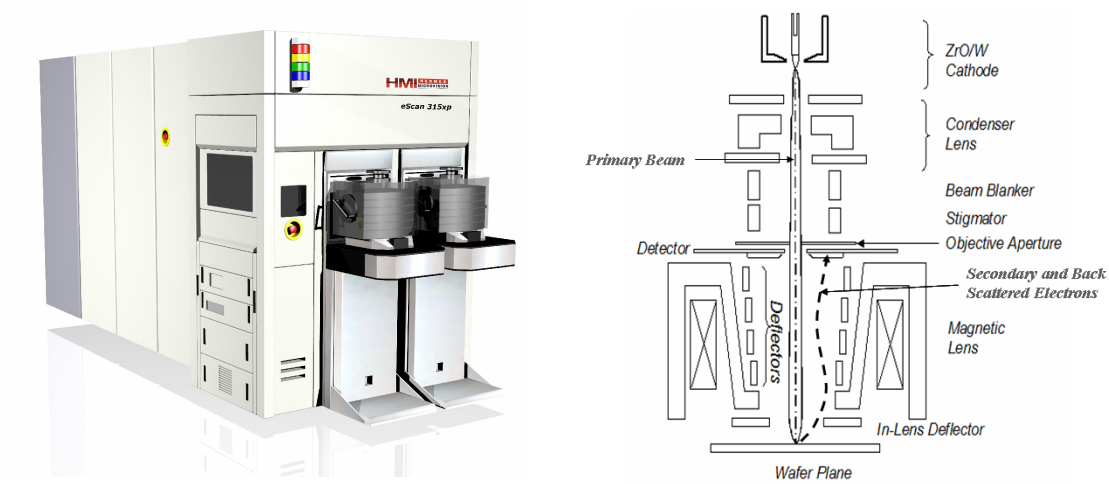
both random and systematic defects on production wafers with a minimum inspection pixel size of 10nm, and a maximum inspection pixel field of 18k x 18k. It operates at scan rate of 100MHz. It can inspect both electrical defects and physical defects, including physical defects on photoresist for after development inspection (ADI) wafers. Figure 5a is the image of the system and Figure 5b is the schematic of the system, which is used e-beam column with swinging objective retarding immersion lens (SORIL) to achieve high-resolution and large scan field for leap and scan EBI applications. [4] In most fab applications, EBI systems are used to capture electrical defects such as circuit open or short and device leakage, taking advantage of the EBI unique voltage contrast (VC) effects. [5], [6], [7], [8] EBI systems have also being used for photolithography process window qualification of contact masks. [9] VC defect inspection usually needs higher beam current to charge the sample surface and does not require the highest resolution. However, to capture sub-10nm program defects on NIL resist patterns in this study, we need to optimize the e-beam condition to achieve the highest resolution while minimizing the surface charging effect.



(a) (b)

Figure 5. Image of eScan®315xp (a) and its schematics (b).

Experiment Results

In this experiment, we used the optimized e-beam condition as: landing energy (LE) 2000 volt, beam current 3nA, 6k x 6k scan pixel field, and 8 scan averages. First, we studied sensitivity using 15nm and 10nm pixel sizes. Due to charging concerns, we inspected two die, one with a 15nm pixel size and another one with a 10nm pixel size, as shown in Figure 6. We focused our inspections on the 32 nm section of the program defects illustrated in Figure 1. The capture rate of program defects of 10nm pixel and 15nm pixel is compared in Figure 7a and Figure 7b, respectively. We can see that

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the 10nm pixel captured more program defects, especially for the dot pattern and line/space pattern. We confirmed that EBI with smaller pixel can really help to capture smaller physical defects, thus the capability to run inspection with a pixel size as small as 10nm becomes very critical for sub-10nm physical defects.

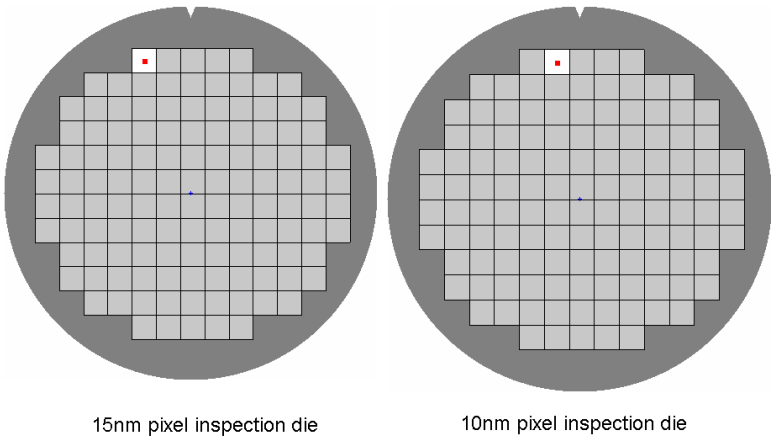
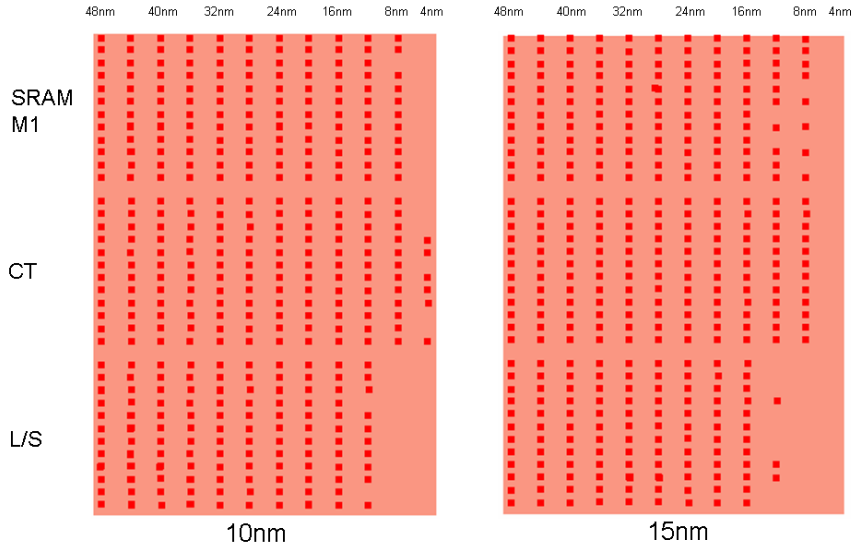


Figure 6. Die map and the locations of inspected dies.



(a) (b)

Figure 7. Die map with 10nm pixel size EBI (a) and 15nm pixel size EBI (b).

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To get a better idea of the 10nm EBI program defect capture rate, we inspected five dies on the wafer as illustrated in Figure 8. We also focused the inspection on the 32nm section of program defects, illustrated in Figure 1. Figure 9 shows the die map of program defects. For the program defects, we found that EBI is most sensitive to the dot pattern and least sensitive to line/space pattern. We've confidently captured all of the program defects down to 8nm in both the dot patterns and SRAM M1 patterns. Figure 10 shows some examples of inspection patch images of captured program defects of each designed pattern. Some eScan®315xp 5nm pixel size review images are showing in Figure 11. The program defect capture rate is summarized in Table 1.

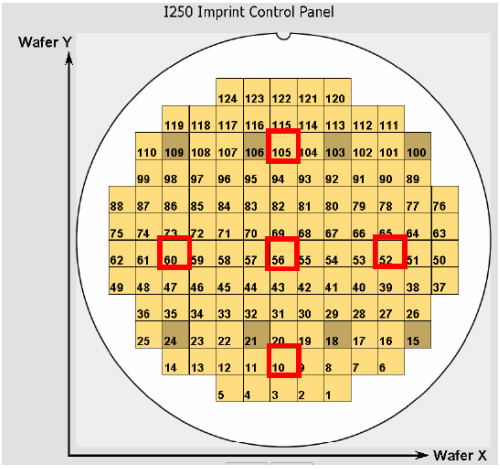

Figure 8. Die map and the locations of inspected dies.

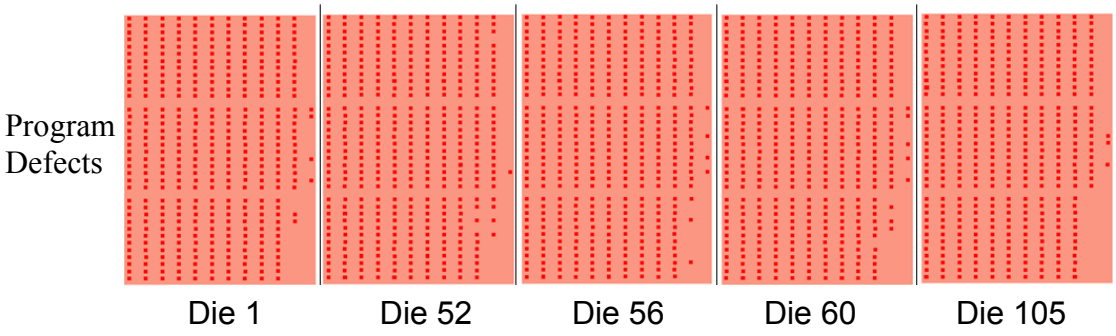

Figure 9. Defect map of program defects of the inspected dies.

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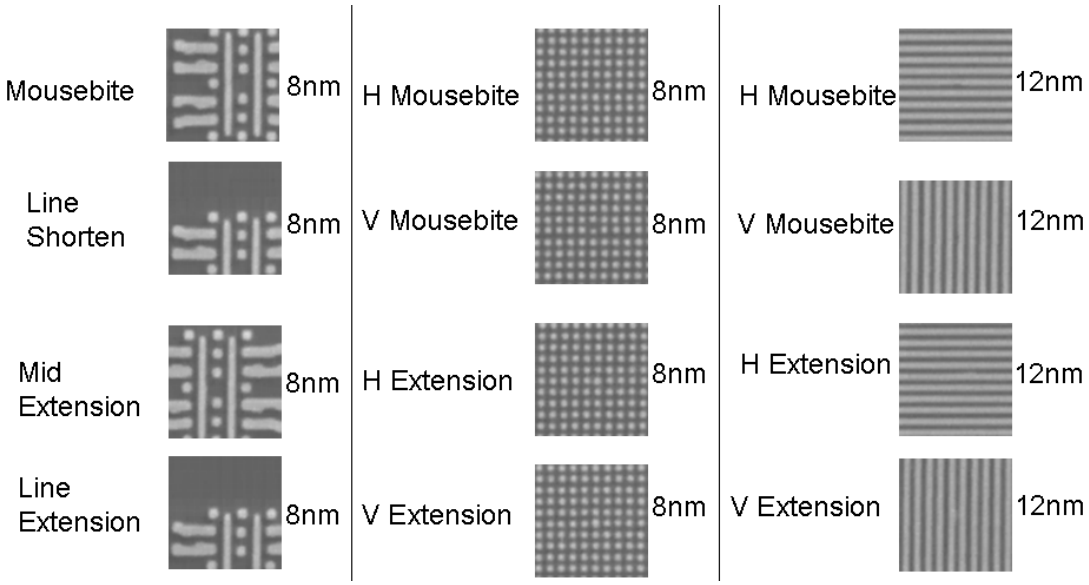

Figure 10. Patch images of captured program defects of each designed pattern.

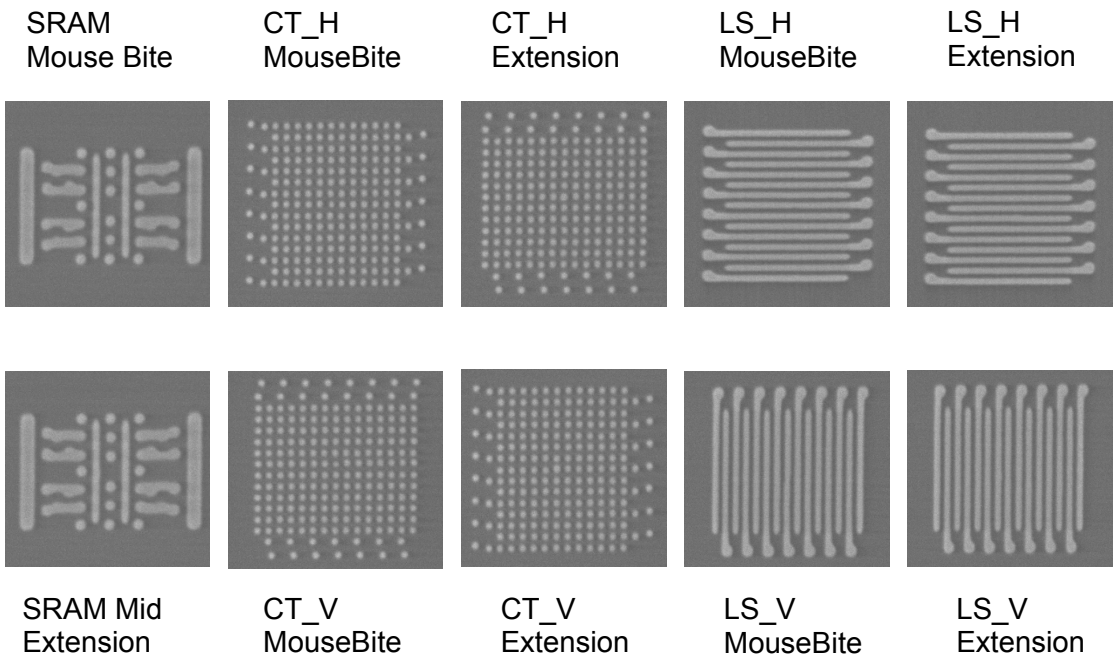

Figure 11. Review images of 8nm program defects.

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		48nm	44nm	40nm	36nm	32nm	28nm	24nm	20nm	16nm	12nm	8nm	4nm
SRAM	Mousebite	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%
	Shorten	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%
	Mid Extension	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	0%
	Extension	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	93%	0%
CT	H_Mousebite	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	40%
	V_Mousebite	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	40%
	H_Extension	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	13%
	V_Extension	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	20%
L/S	H_Mousebite	100%	100%	100%	100%	100%	100%	100%	100%	100%	93%	20%	0%
	V_Mousebite	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	27%	0%
	H_Extension	100%	100%	100%	100%	100%	100%	100%	100%	100%	87%	7%	0%
	V_Extension	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	27%	0%

Table 1, Programmed defect capture rate of with 10nm pixel size.

In this experiment, we found that the amount of captured program defects is about the same for each die. Because the mask used to imprint the sample wafers was of research quality, it should be noted that several defects that were not programmed were also detected. Defects in the original mask may also cause additional process related defects. Examples of repeating defects captured during inspection are depicted in Figure 12. Figure 12 shows images of defects from die 52, die 56 and die 60. The inserted inspection patch images in Figure 12 clearly show that these are repeating defects with the same patterns. They are defects on the mask, either formed during the mask manufacturing or formed because some kind of contaminant or particle caused the feature to plug. Further experimentation with higher quality masks is required to determine the root cause and reduce the defectivity on the mask. Capturing the repeating defects on wafer can be a solution for printable mask defects that are invisible in mask inspection, such as a phase defect on a EUV mask.

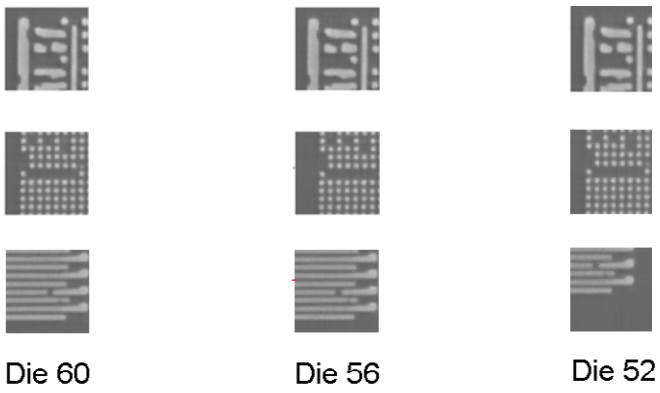

Figure 11. Repeating defects in three inspected dies.

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Summary

In this study, we generated a patterned wafer using a 32nm NIL mask with program defects. We used the high-resolution EBI system to inspect 32nm NIL resist wafer with program defects sized from 4nm to 48nm to check the sensitivity of the EBI system. We found that the sensitivity is pattern related, most sensitive to dots and least sensitivity to line/space. With 10nm inspection pixel size, we can confidently capture all defects 16nm or larger in all these designed patterns. For dot pattern, we can confidently capture all defects 8nm or larger. We proved that EBI is a solution for NIL defect detection, monitoring and reduction. It also can be a solution for printable mask defects that are invisible in mask inspection.

Acknowledgement

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