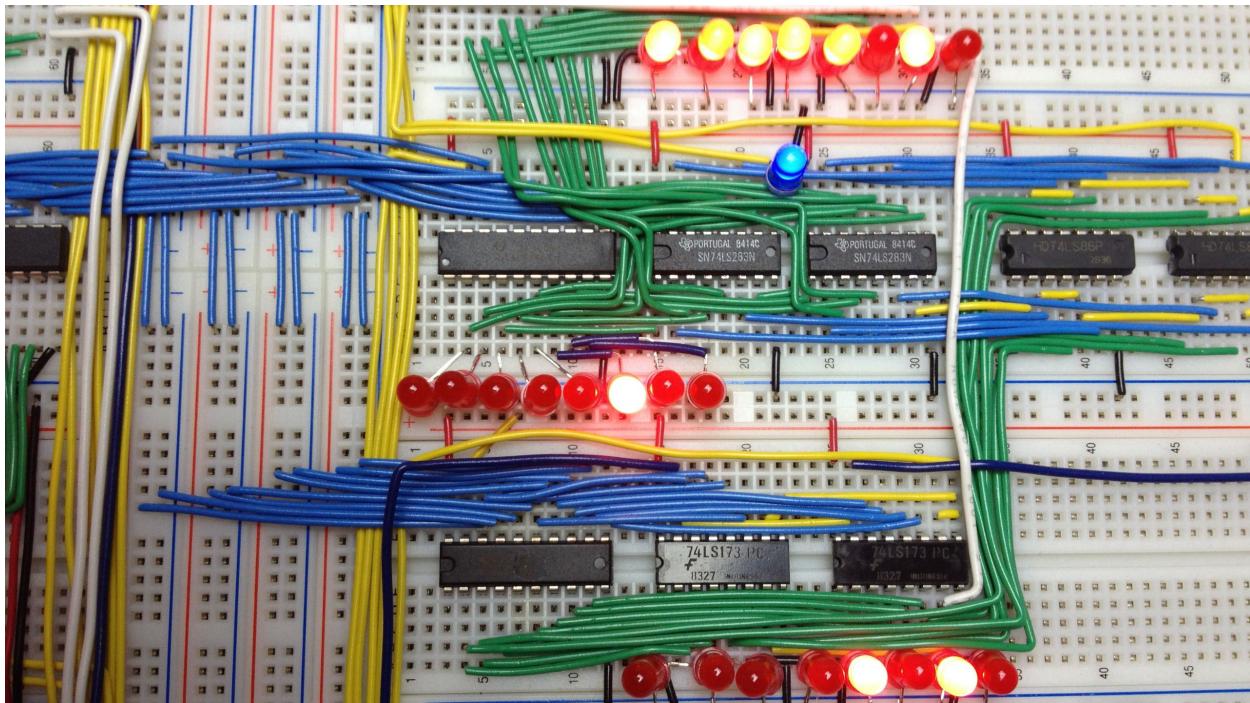


SAP-2S: Building an 8 Bit Breadboard Computer

Daniel Gitzel, Trammell Hudson, Rachel Malbin, Chris Mulligan, and Jay Smith

Fall 2017



In the fall of 2017 a group of TSers are going to follow Ben Eater's (<https://eater.net/>) YouTube guide to building a variant of the SAP-1 8 bit computer on breadboards. The SAP-1's full name is Simple As Possible-1, from the 1970s era text book [Digital Computer Electronics](#) by Malvino & Brown.

We'll be tweaking and improving it slightly, so our version will be called the SAP-2S.

The computer will be built primarily using 1970s era TTL Integrated Circuits, the [classic 7400 series](#), specifically the 74LS series, Low-power Schottky variant. These chips have a typical 10 ns gate delay, and a remarkable-for-the-time 2 mW dissipation, using 5 volts.

The computer is composed of several modules, each of which performs just a few basic functions. These modules can be built and tested separately, and then assembled together.

- Clock module (CLK)
- Registers (A, B, IR)
- Arithmetic and logic unit (ALU)
- Random access memory (RAM)
- Program counter (PC)
- Output (OUT)
- Bringing it all together (BUS)
- Control logic (CONT)

Conventions

In order to follow Ben's videos, and enable easier assembly, we'll be following certain conventions across all the modules.

- Wire colors:
 - **Red** is 5V (Vcc)
 - **Black** is ground (GND)
 - White is clock (CLK)
 - **Yellow** (yellow) is control, eg write enable WE, load LD, etc (CONT)
 - **Blue** is data, particularly data going to/from the bus (BUS)
 - **Green** is internal wiring within a module
 - **Orange** is typically manual control/settings, particularly during testing
 - **Brown** is clear and reset (CLR)
- Column 1 should always be on the left of the breadboard
- Pin 1 should always be on the bottom left, with the notch to the left
- For final assembly, breadboards should remove the *BOTTOM* bus bar, and keep the top
- The LSB is on the right, when possible.

Changes we're making

We're tweaking the system Ben built slightly to make it a little more powerful, and a little more fun for demoing. Many folks have done these extensions, such as [LoneRegister](#) with extra RAM and instructions.

Reset Button

Ben often finds it helpful to reset his system, but it's all spread around. In <https://youtu.be/HtFro0UKqkk> Ben creates a reset button near the instruction register, let's do that.

64k SRAM chip

The RAM chips that Ben used isn't readily available, is very weird, and has very limited capacity. Instead, let's try a slightly fancier IDT7164 64k CMOS SRAM chip. We won't use most of that, but we'll use 256 bytes, or 2k.

It directly has tri-state output and is a single chip, so it should be much simpler.

Changes:

- We don't need the 74LS04 inverters
- The IDT7164 SRAM uses the same pins for Data in and Data Out, so it only has a single bus input/output, but uses control lines to choose whether to output, write, or neither.

ROM programs

The computer Ben builds could be called a full [Von Neumann architecture](#), where instructions are stored in RAM. While this is powerful and flexible, and how modern computers work, unfortunately, that makes it a little more difficult to run programs. Every time the computer loses power the programs have been lost.

So we need to either re-program them by hand after each boot (like Ben), find a way to load RAM with instructions on each boot (how modern computers work, copying from hard drives into RAM) like with [an Arduino programmer](#), or fetch instructions from non-volatile memory like an EEPROM.

Let's do the latter, turning the RAM module into a RAM/ROM module. This is a [Harvard Architecture](#)-ish design. We could have the ROM chip share a lot of the functionality with the RAM chip, particularly the Memory Address Register, but we'll allow the computer to choose whether to read from RAM or ROM.

Changes:

1. Add a ROM chip to the RAM breadboard, and connect its IO to the bus.
 - We may still want 74LS245 tri-state output buffers so we can put LEDs on the RAM & ROM chips.
2. Use the (now 8 bit) Memory Access Register as the address for the ROM chip.
3. Create a new control signal (DO for ROM **Disk Out?** PO for **Program Out?** EO for **EEPROM Out?**) to output the contents of ROM memory onto the bus.
4. Add that control line to the micro code EEPROMs
5. (Optionally?) Add an instruction for read ROM into register A.
6. (Optionally?) Add physical DIP switches for the higher order addresses in the RAM chip – this would let a user select from multiple programs in the EEPROM.
7. Optionally add an instruction and/or button for writing to ROM.

8 microcode steps

This is a small change, but Ben resets his opcode (T) clock after just 6 steps. We'll be needing an extra clock cycle to fetch the extra argument from ROM, so since we don't care about performance, let's go a full 8 steps, in case we want to make more complicated instructions.

Changes:

- 1) Skip the reset part of the control logic, where he short circuits the counter.
- 2) Add T7 and T8 LEDs

Intermediate

8 bit memory addresses

One big limitation in Ben's system is the memory addresses are limited to just 4 bits. Which limits the computer to only 16 possible memory locations! Oh no!

We're going to build our system to use 8 bit memory addresses. That gives us access to a *massive* 256 locations. This requires a few changes:

Changes:

1. The Program Counter (PC) needs to be an 8 bit register/counter. That means cascading two 74LS161 together, and connecting all 8 bits to the bus.
2. The Memory Address Register needs to be a full 8 bits
3. The Memory Address DIP switch should be 8 bits
4. The instruction set will change slightly, with memory addresses stored as a separate word in memory. So the code to load from memory address 0xAB, would be two bytes. The first byte would be the LDA instruction, and the following byte would be 0xAB. That means we need to add an fetch cycle from ROM into Memory Address Register, and advance the PC again.

Future Work

Three microcode control EEPROMs

This is probably something we should just do, in case we need it later.

Changes:

1. Change from `uint_16` to `uint_32` for the instructions.
2. Use the last 2 bits to select which chip we're using.

Assembler

We could write a nice simple assembler. Perhaps in Arduino, or perhaps in Python. Then folks can fully code in a nice machine language, and the assembler will turn that into bytecode.

Hex output

It wouldn't be too hard to add a Hex mode output to the output EEPROM, in addition to unsigned and twos-complement modes.

Full ALU

The SAP-1 that Ben implements doesn't perform any logic functions besides adding. For example, we can't do comparison, which means we can't have branches and if statements and such. We could replace the two 4 bit adders with the 74LS181 4-bit ALU. It provides:

Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations. Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations.

This would likely require adding 4 additional control lines, and an additional controller EEPROM to control them (and perhaps require changing how the EEPROMs are coded, since 20 bits is an awkward number). It would also require additional instructions to actually use those functions, which means we'd (possibly) need to expand to 6 or 8 bit instructions.

Conditional Jump

I feel like it's pretty essential to a computer to perform a conditional jump. At least a jump-if-carry, which when cleverly combined with subtraction might be sufficient, but really requires the ALU to be easy.

6 bit instructions

Perhaps we want to be able to use more than 16 instructions. Let's figure that 64 is enough though, so we'll make our instructions into 6 bits, leaving 2 bits left for in-instruction immediates. While that's not much for immediates, it does let us have the three most useful binary numbers in the same instruction: 0, 1, or 2. We can always make two versions of the "immediates" commands, where one version really loads from the next byte of ROM.

ASCII Output

YouTuber [Ptrk25](#) added a new module to theirs that takes the output value and decodes it as ASCII, printing it out and letting you build up a message character by character (ie keeping state). I imagine it uses a full microcontroller (arduino?) to capture the values when told, and then drive the LCD.

Again, for the CPU this would likely require more control lines and another control EEPROM to handle the control logic.

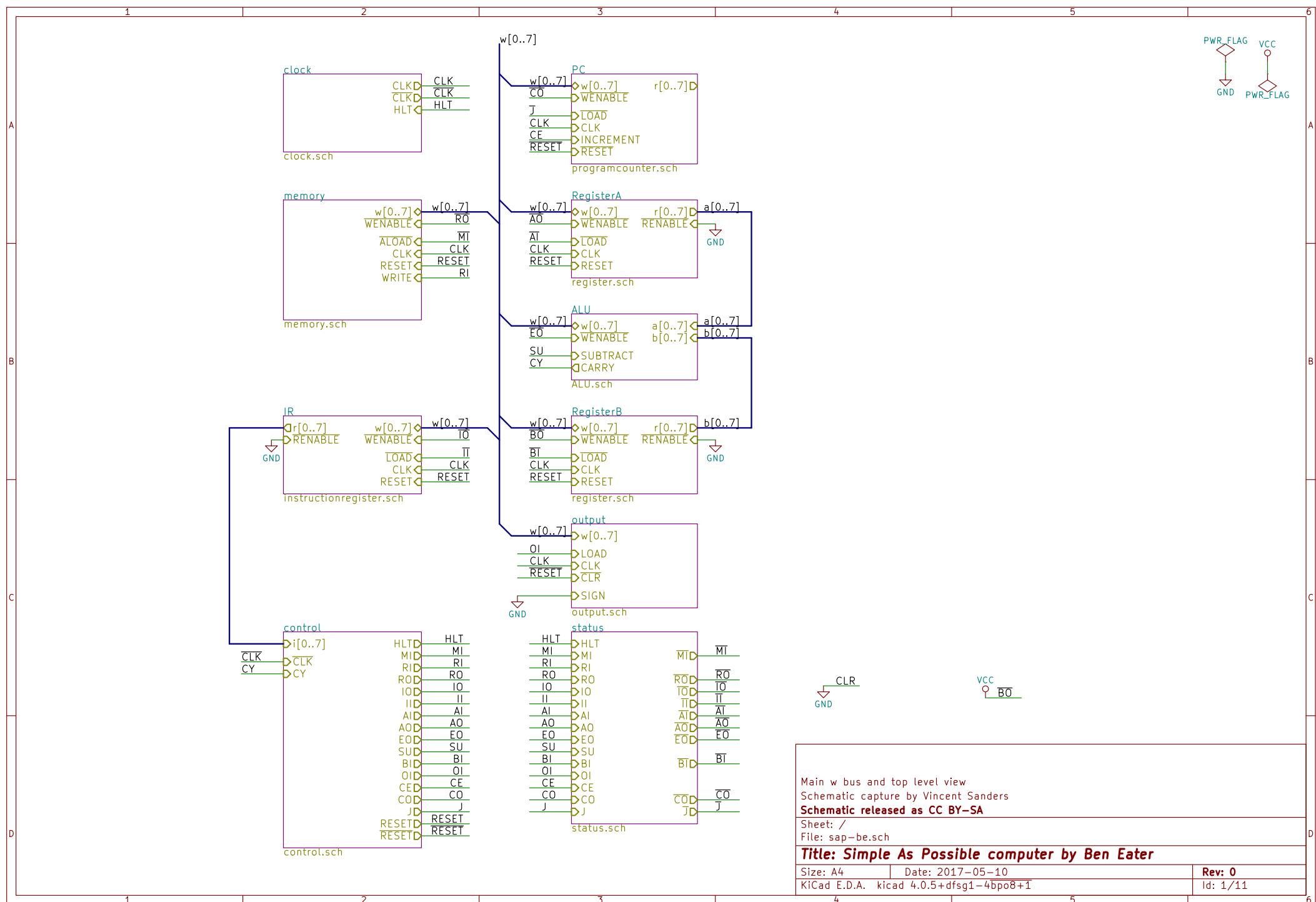
Schematics

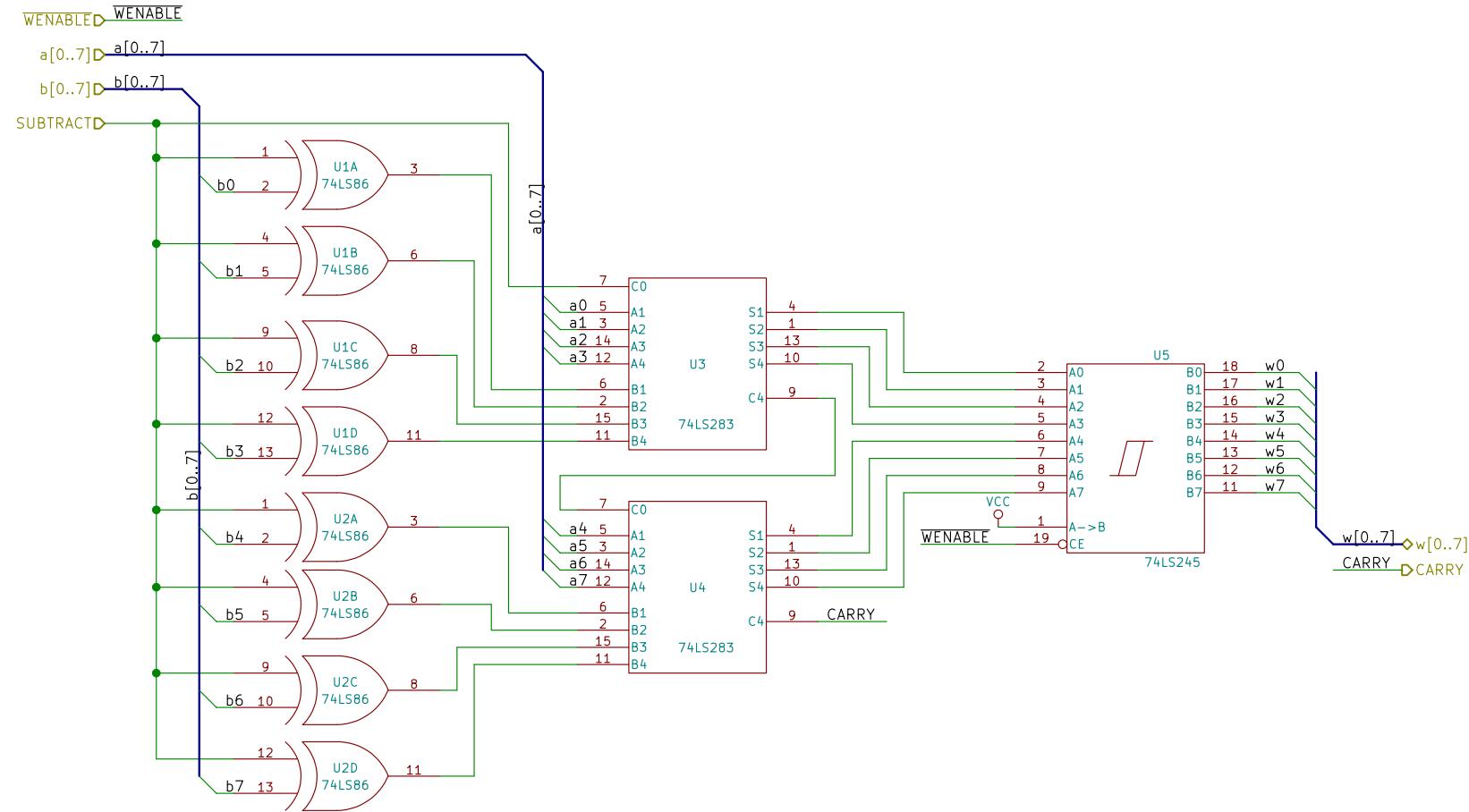
Following this introduction are a set of schematics drawn by [Vincent Sanders aka kyllikki](#). These schematics may be helpful in assembling the various components.

Datasheets

Following those schematics are excerpts from the datasheets for all the components we'll be using. Even more details online.

| Qty | Part Number | Description | Modules |
|-----|-------------|----------------------------------|-------------------|
| 4 | LM555 | 555 timer IC | CLK, OUT |
| 1 | 74LS00 | Quad NAND gate | RAM |
| 5 | 74LS04 | Hex inverter | CLK, RAM, CONT |
| 2 | 74LS08 | Quad AND gate | CLK, OUT |
| 1 | 74LS32 | Quad OR gate | CLK |
| 1 | 74LS76 | Dual JK flip-flop -> 74LS112 | OUT |
| 2 | 74LS86 | Quad XOR gate | ALU |
| 1 | 74LS112 | Dual J-K flip-flop | OUT |
| 1 | 74LS138 | 3-to-8 line decoder | CONT |
| 1 | 74LS139 | Dual 2-line to 4-line decoder | OUT |
| 4 | 74LS157 | Quad 2-to-1 line data selector | RAM |
| 4 | 74LS161 | 4-bit synchronous binary counter | PC, CONT |
| 7 | 74LS173 | 4-bit D-type register | REG, RAM |
| 2 | 74LS181 | 4-bit Arithmetic Logic Unit | ALU |
| 2 | 74LS189 | 64-bit RAM -> IDT7164 | RAM |
| 6 | 74LS245 | Octal bus transceiver | REG, ALU, RAM, PC |
| 1 | 74LS273 | Octal D flip-flop | OUT |
| 2 | 74LS283 | 4-bit binary full adder | ALU |
| 1 | IDT7164 | 64k (8k x 8-bit) SRAM | RAM |
| 4 | SA56-11SRWA | 7-segment LED | OUT |
| 4 | AT28C64B | EEPROM | OUT, CONT |
| 1 | 74HC595 | 8-bit shift register | EEPROM programmer |





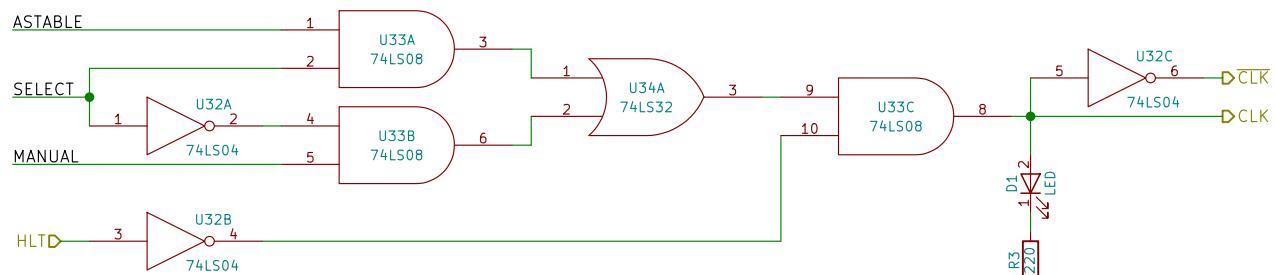
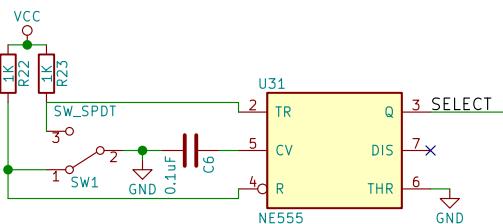
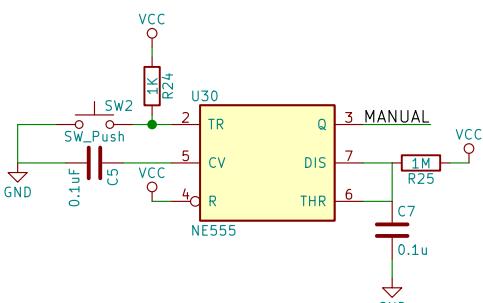
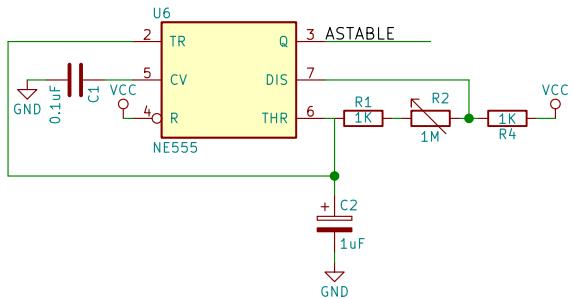
Arithmetic Logic Unit
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /ALU/
File: ALU.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. kicad 4.0.5+dfsg1-4bpo8+1

Rev: 0
Id: 2/11



Clock generation with manual step and halt
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

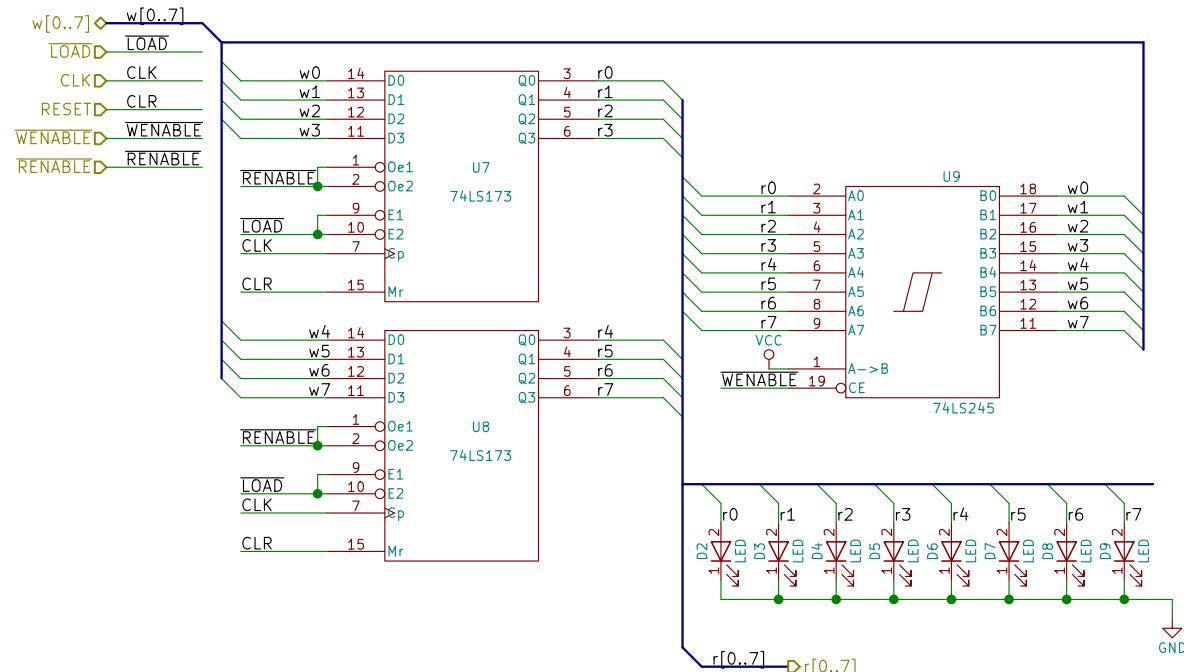
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Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. kicad 4.0.5+dfsg1-4bpo8+1

Rev: 0
Id: 3/11

A



B

C

D

Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

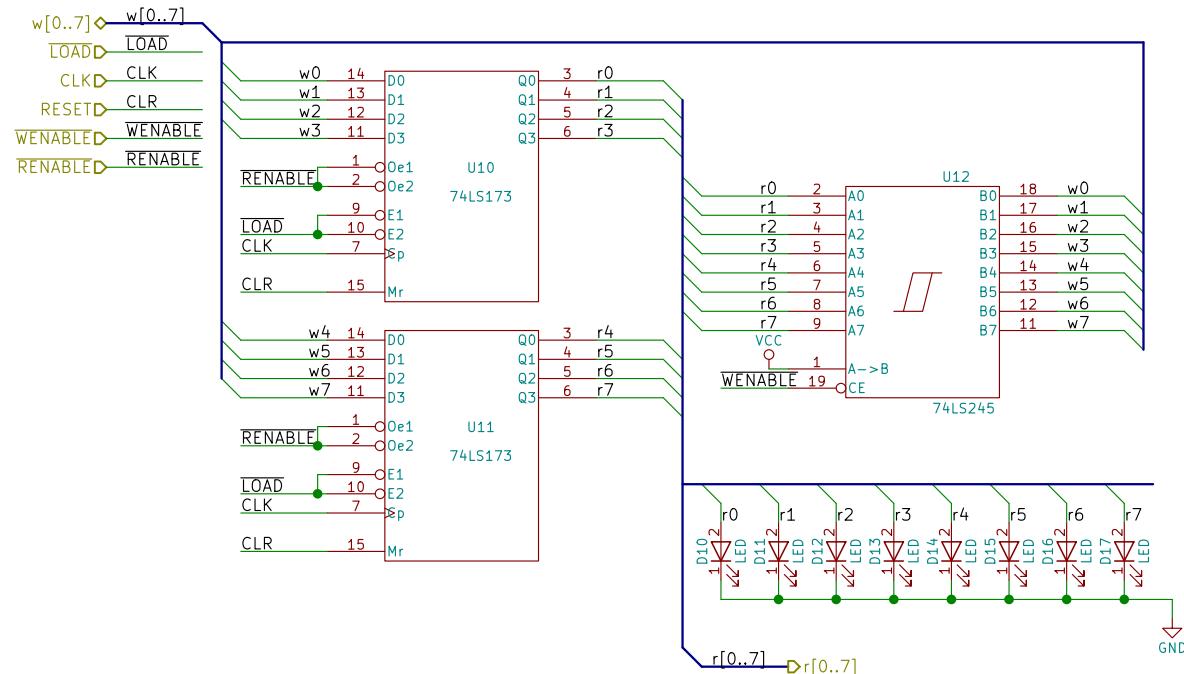
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File: register.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. kicad 4.0.5+dfsg1-4bpo8+1

Rev: 0
Id: 4/11

A



B

C

D

Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /RegisterA/
File: register.sch

Title: Simple As Possible computer by Ben Eater

| | |
|----------------------------------------|------------------|
| Size: A4 | Date: 2017-05-10 |
| KiCad E.D.A. kicad 4.0.5+dfsg1-4bpo8+1 | Rev: 0 |

| |
|----------|
| Id: 5/11 |
|----------|

A

B

C

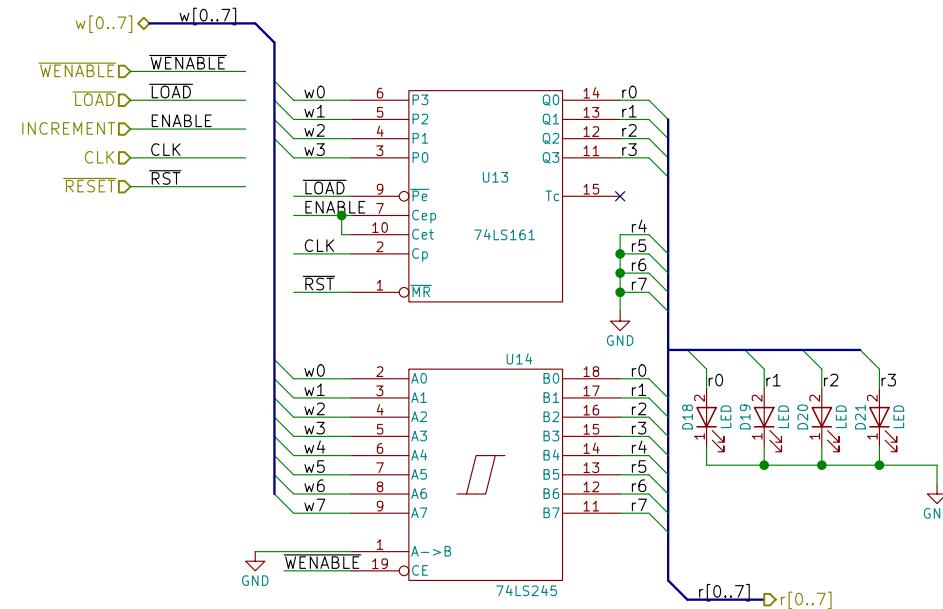
D

A

B

C

D



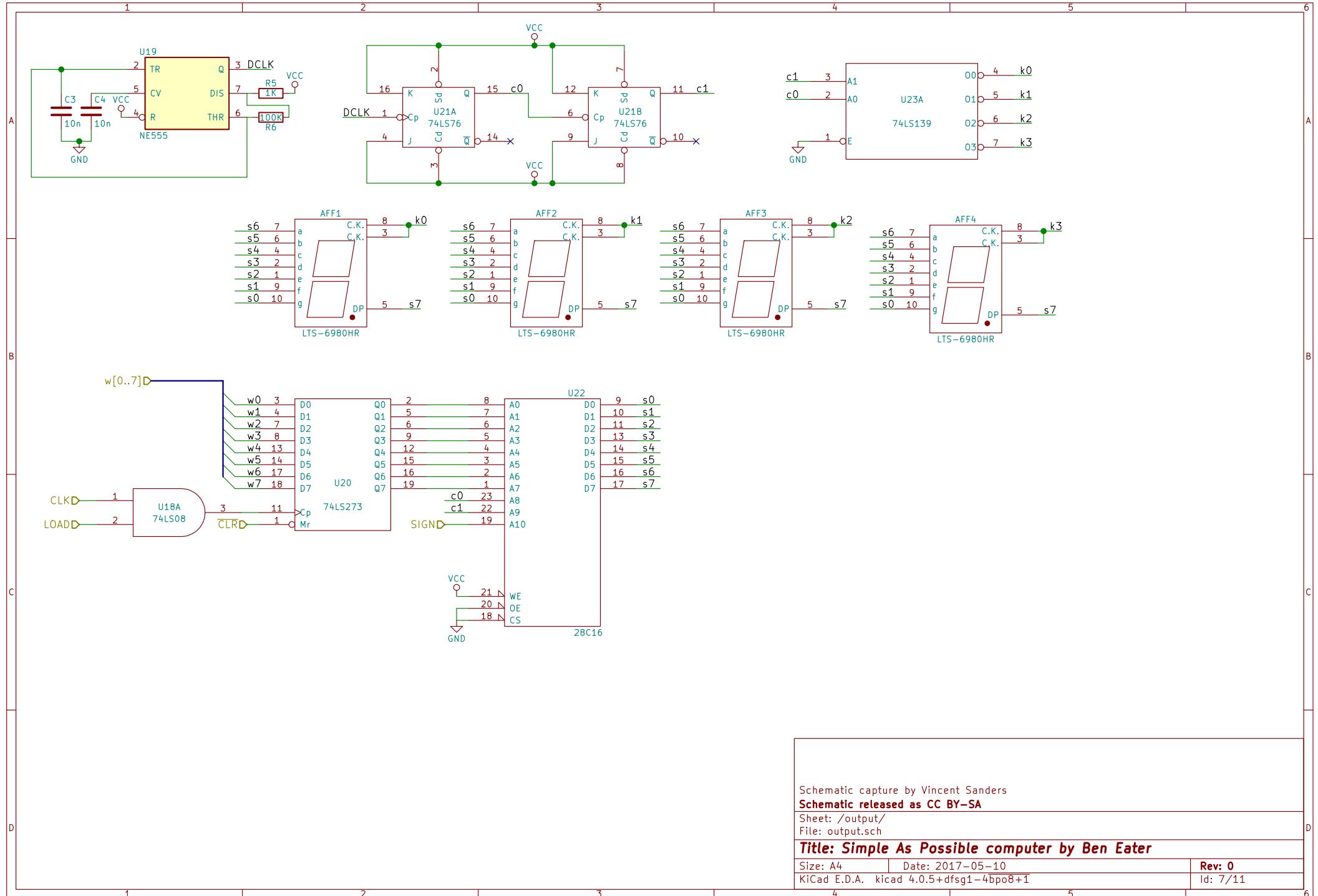
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

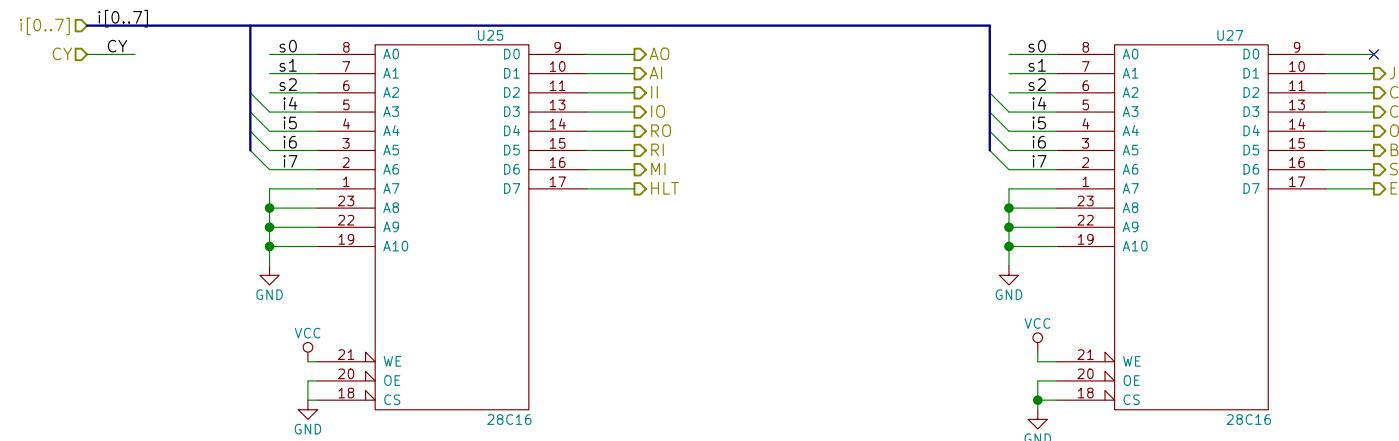
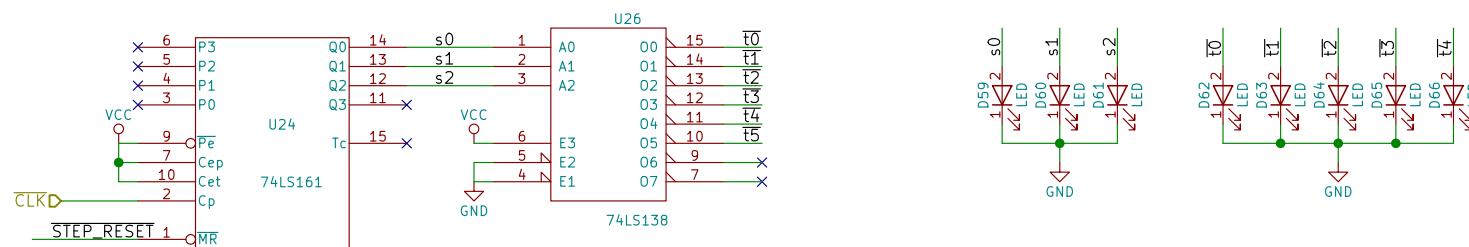
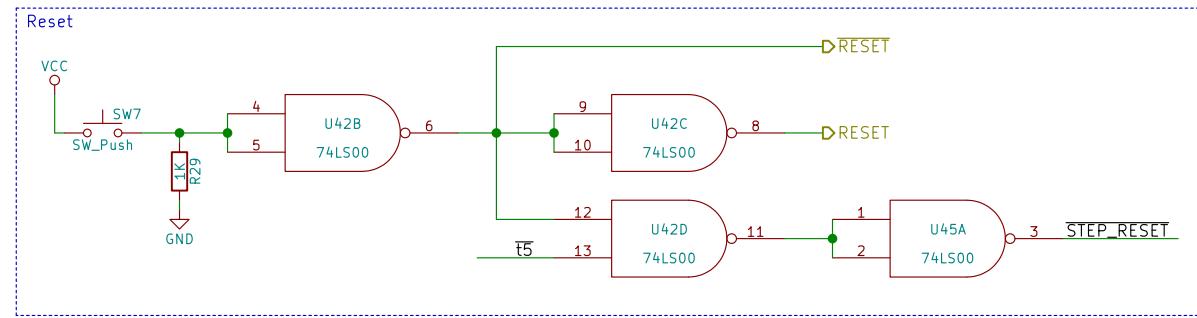
Sheet: /PC/
File: programcounter.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. kicad 4.0.5+dfsg1-4bpo8+1

Rev: 0
Id: 6/11





Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /control/
File: control.sch

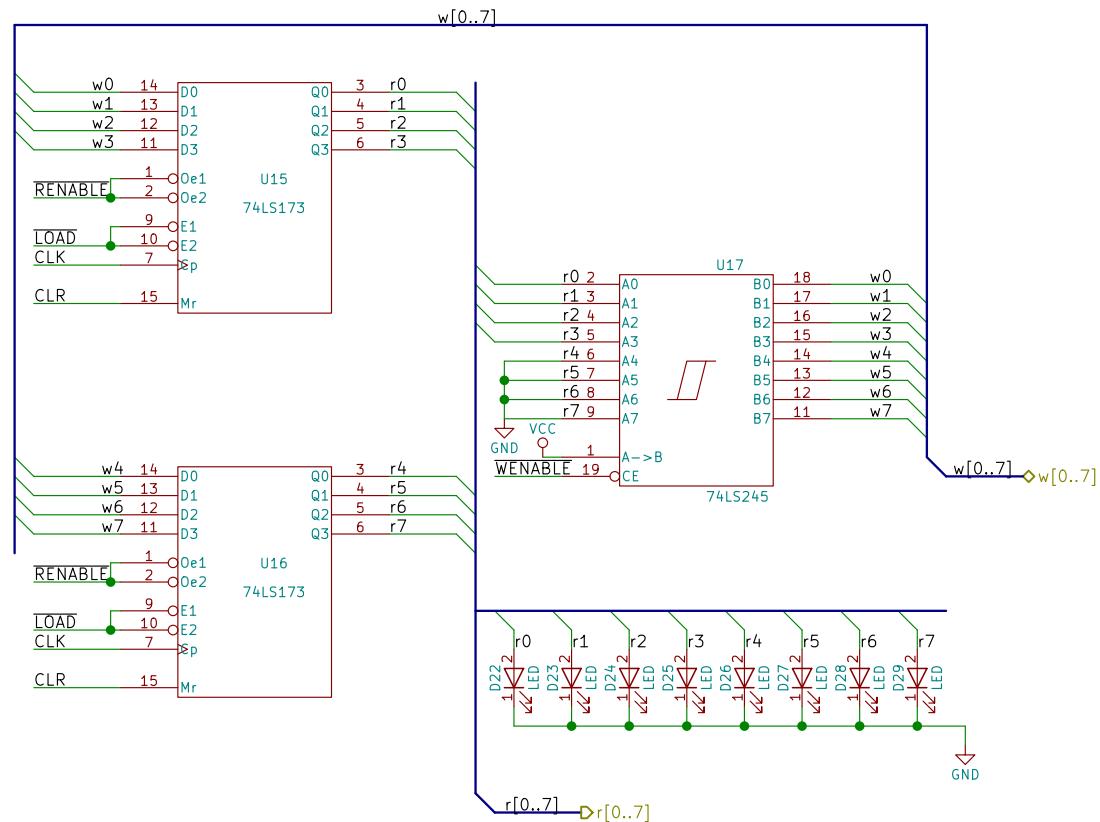
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Size: A4 Date: 2017-05-10
KiCad E.D.A. kicad 4.0.5+dfsg1-4bpo8+1

Rev: 0
Id: 9/11

A

LOAD LOAD
 CLKD CLK
 RESET CLR
 WENABLE WENABLE
 RENABLE RENABLE



B

A

C

B

D

C

D

Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /IR/
 File: instructionregister.sch

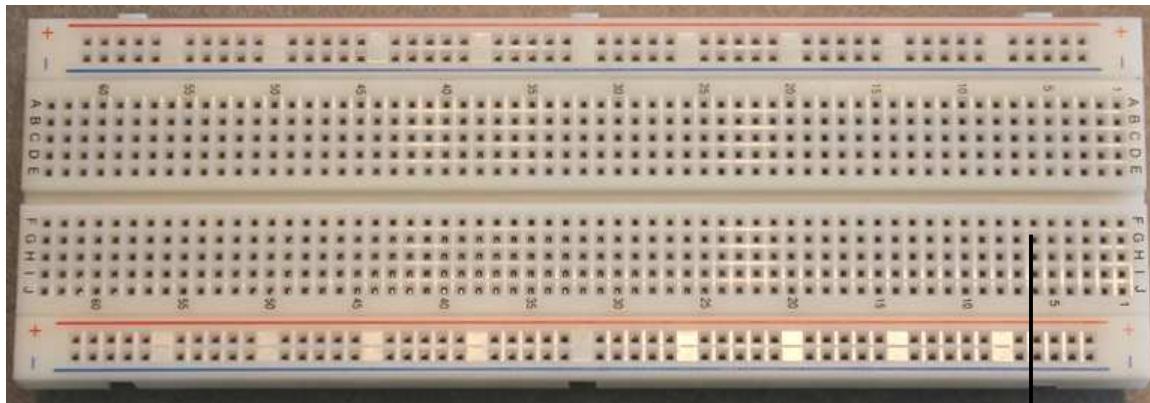
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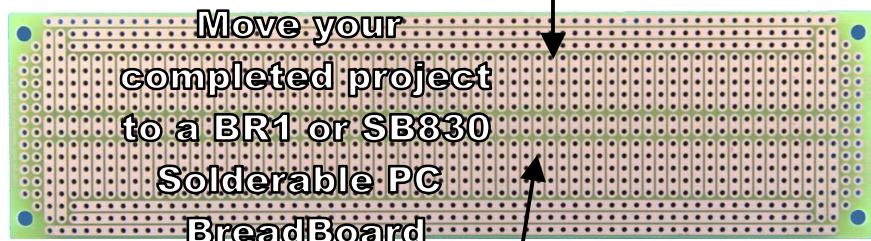
BB830, BB830T – Plug-in BreadBoards



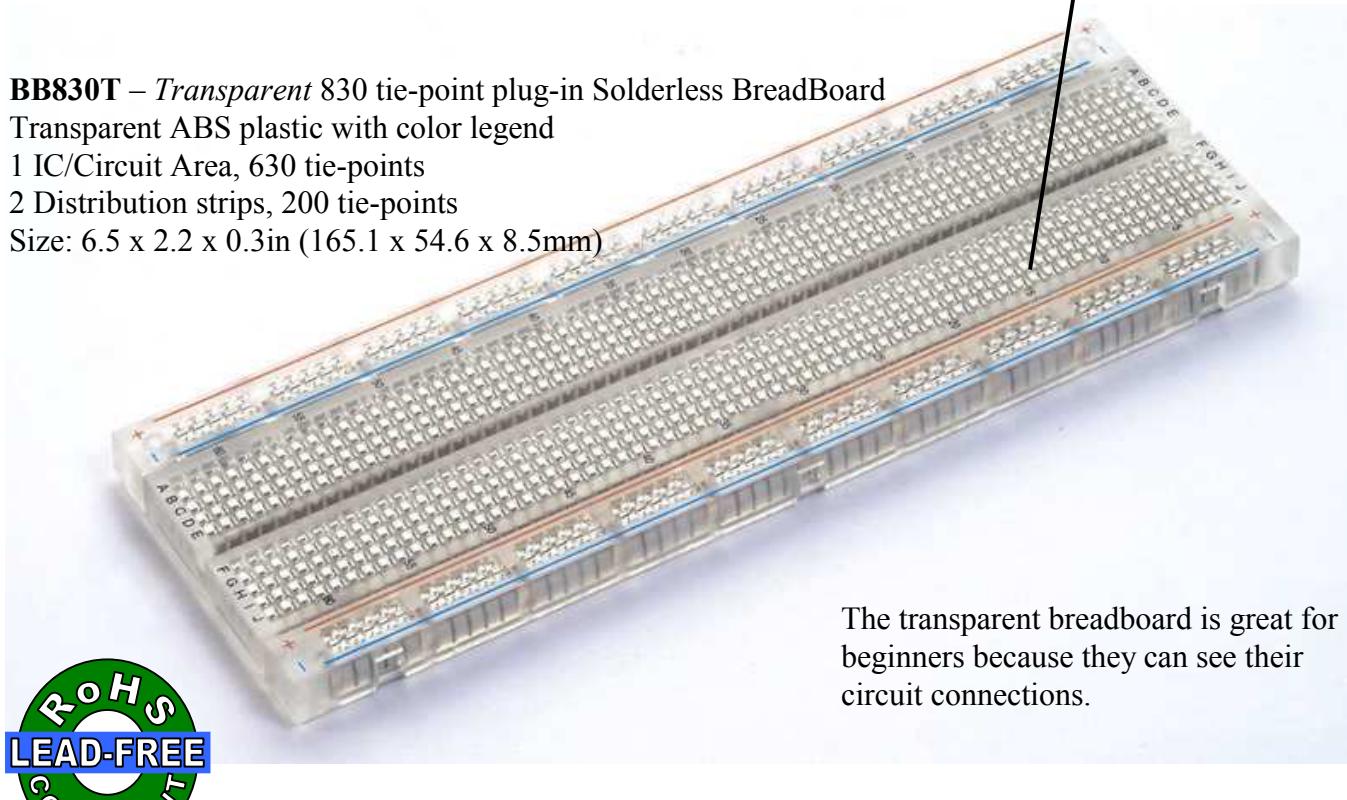
830 tie point solderless “plug-in” breadboards provide a quick way to build and test circuits for experimentation or when learning electronics.



BB830 - 830 tie-point plug-in Solderless BreadBoard, ABS plastic with color legend
1 IC/Circuit Area, 630 tie-points
2 Distribution strips, 200 tie-points
Size: 6.5 x 2.2 x 0.3in
(165.1 x 54.6 x 8.5mm)



BB830T – Transparent 830 tie-point plug-in Solderless BreadBoard
Transparent ABS plastic with color legend
1 IC/Circuit Area, 630 tie-points
2 Distribution strips, 200 tie-points
Size: 6.5 x 2.2 x 0.3in (165.1 x 54.6 x 8.5mm)



The transparent breadboard is great for beginners because they can see their circuit connections.

BusBoard Prototype Systems - Built for designers

www.BusBoard.com sales@busboard.com

BPS-MAR-(BB830)-001 Rev 4.00

Solderless BreadBoard Specifications

BB300 Body Material: White ABS Plastic with Black Printed Legend

BB400/BB830 Body Material: White ABS Plastic with Color Printed Legend

BB830T Body Material: Transparent ABS Plastic with Color Printed Legend

Hole Pitch/Style: 0.1" (2.54 mm), Square Wire Holes

ABS Heat Distortion Temperature: 84° C. (183° F.)

Spring Clip Contact: Phosphor Bronze with Plated Nickel Finish

Contact Life: 50,000 insertions

Rating: 36 Volts, 2 Amps

Insertion Wire Size: 21 to 26 AWG wire, or 0.025" Square post headers
0.016 to 0.028 inches diameter (0.4 to 0.7mm diameter)

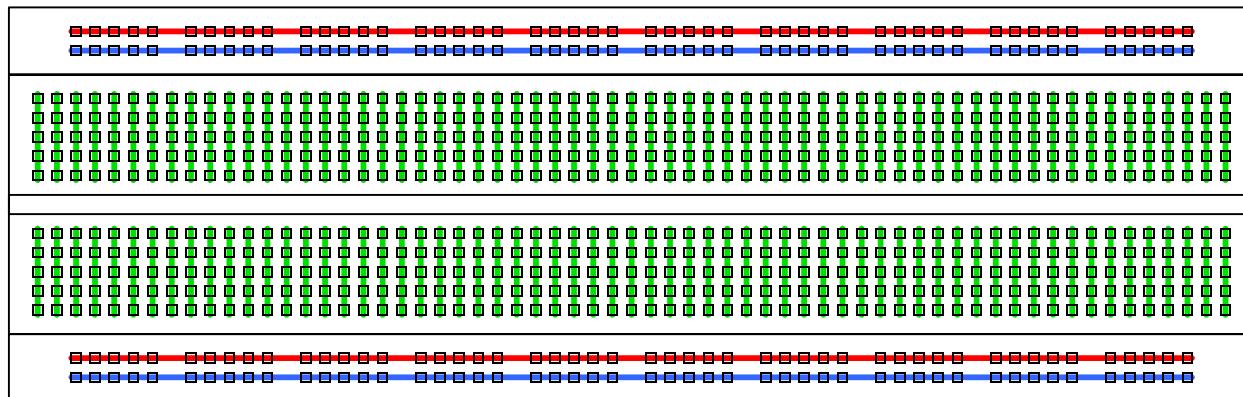
Backing: Peelable adhesive tape for attaching to a surface.
Metal back plate provided with 830 tie point breadboards.

Metal Back Plate Thickness: 0.031 inches (0.8mm)

All BPS BreadBoards are Lead-Free and *RoHS Compliant*.

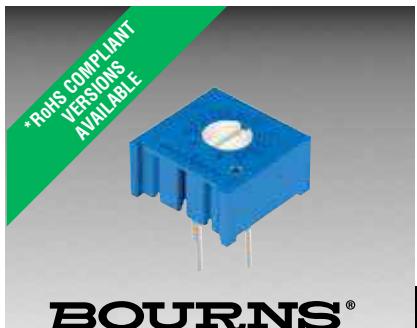


Internal Connections



The BB830 and BB830T breadboards have 63 vertical columns on top and 63 columns below. Each column has 5 connected holes each (the green lines). This is the circuit area. There are also 4 "rails" (or distribution strips) for power and ground running horizontally (the red and blue lines).

A distribution strip can be used to carry a signal if it is not needed for power or ground.



BOURNS®

Features

- Single Turn / Cermet / Industrial / Sealed
- Available on tape and reel
- Available with a knob for finger adjust
- Available with extended shaft
- Available with cross-slot rotor
- Top and side adjust types (F, P, H, W, X most popular)

- RoHS compliant* version available
- For trimmer applications/processing guidelines, [click here](#)

3386 - 3/8 " Square Trimpot® Trimming Potentiometer

Electrical Characteristics

| | |
|------------------------------------|---------------------------------------------------------|
| Standard Resistance Range | 10 ohms to 2 megohms (see standard resistance table) |
| Resistance Tolerance | ±10 % std. (tighter tolerance available) |
| Absolute Minimum Resistance | 2 ohms max. |
| Contact Resistance Variation | 2 % or 3 ohms max. (whichever is greater) |
| Adjustability | |
| Voltage Divider | ±0.05 % |
| Rheostat..... | ±0.15 % |
| Resolution | Infinite |
| Insulation Resistance | 500 vdc. 1,000 megohms min. |
| Dielectric Strength | |
| Sea Level..... | 900 vac |
| 70,000 Feet | 350 vac |
| Adjustment Angle | 280 ° nom. |

Environmental Characteristics

| | |
|-------------------------------|----------------------------------------------------------------------------------------|
| Power Rating (300 volts max.) | |
| 85 °C | 0.5 watt |
| 125 °C | 0 watt |
| Temperature Range ... | -55 °C to +125 °C |
| Temperature Coefficient ... | ±100 ppm/°C |
| Seal Test | 85 °C Fluorinert† |
| Humidity | MIL-STD-202 Method 103 96 hours (2 % ΔTR, 10 Megohms min.) |
| Vibration | 30 G (1 % ΔTR; 1 % ΔVR) |
| Shock | 100 G (1 % ΔTR; 1 % ΔVR) |
| Load Life.. | 1,000 hours 0.5 watt @ 70 °C (3 % ΔTR; 3 % or 3 ohms, whichever is greater, CRV) |
| Rotational Life | 200 cycles (4 % ΔTR; 3 % or 3 ohms, whichever is greater, CRV) |

Physical Characteristics

| | |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------|
| Mechanical Angle | 310 ° nom. |
| Torque..... | 5.0 oz-in. max. |
| Stop Strength | 15.0 oz -in. min. |
| Terminals | Solderable pins |
| Weight | 0.03 oz. |
| Marking..... | Manufacturer's trademark, resistance code, wiring diagram, date code, manufacturer's model number and style |
| Flammability | U.L. 94V-0 |
| Standard Packaging..... | 50 pcs. per tube |
| Wiper | 50 % (Actual TR) ±10 % |
| Adjustment Tool..... | H-90 |

*RoHS Directive 2002/95/EC Jan. 27, 2003 including annex and RoHS Recast 2011/65/EU June 8, 2011.

†"Fluorinert" is a registered trademark of 3M Co.

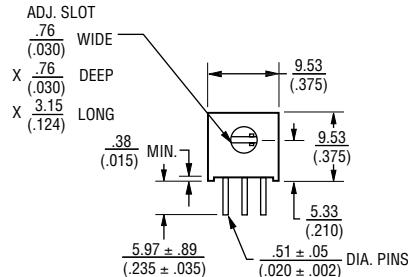
Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.

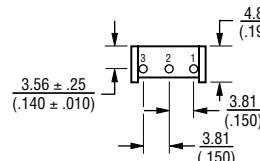
Users should verify actual device performance in their specific applications.

Product Dimensions

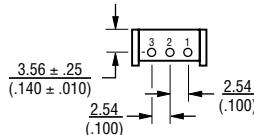
Common Dimensions Side Adjust Models B,C,J,X



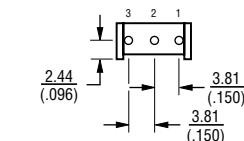
3386B



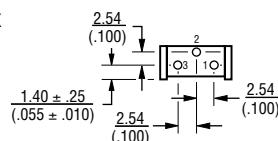
3386C



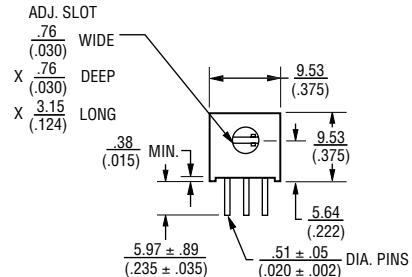
3386J



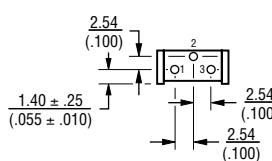
3386X



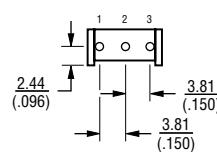
Common Dimensions Side Adjust Models H,S,W



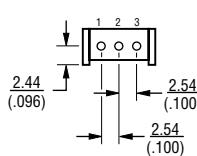
3386H



3386S



3386W



DIMENSIONS: MM
(INCHES)

TOLERANCES: ± 0.25
(.010) EXCEPT WHERE NOTED

How To Order

3386 P - 1 - 103 T LF

| | |
|---------------------------------------------------------------------------------------------------------|-------------|
| Model _____ | Style _____ |
| Standard or Modified Product Indicator | |
| -1 = Standard Product | |
| -EY5 = Extended Shaft | |
| Resistance Code _____ | |
| Optional Suffix Letter _____ | |
| T = Knob** | |
| Packaging Designator _____ | |
| Blank = Tube (Standard) | |
| R = Tape & Reel (W and U Pin Styles Only) | |
| A = Ammo Pack (W and U Pin Styles Only) | |
| Tape and reel material meets Antistatic ANSI/ESD 5541-2003 packaging standards. | |
| Terminations _____ | |
| LF = 100 % Tin-plated (RoHS compliant) | |
| Blank = 90 % Tin / 10 % Lead-plated (Standard) | |
| **Knob option is available only in standard tube packaging. Not recommended for side load applications. | |
| Consult factory for other available options. | |

Standard Resistance Table

| Resistance (Ohms) | Resistance Code |
|-------------------|-----------------|
| 10 | 100 |
| 20 | 200 |
| 50 | 500 |
| 100 | 101 |
| 200 | 201 |
| 500 | 501 |
| 1,000 | 102 |
| 2,000 | 202 |
| 5,000 | 502 |
| 10,000 | 103 |
| 20,000 | 203 |
| 25,000 | 253 |
| 50,000 | 503 |
| 100,000 | 104 |
| 200,000 | 204 |
| 250,000 | 254 |
| 500,000 | 504 |
| 1,000,000 | 105 |
| 2,000,000 | 205 |

Popular distribution resistance values listed in boldface. Special resistances available.

SERIES 78B

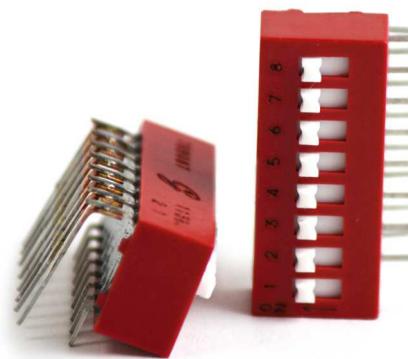
Right Angle Option

FEATURES

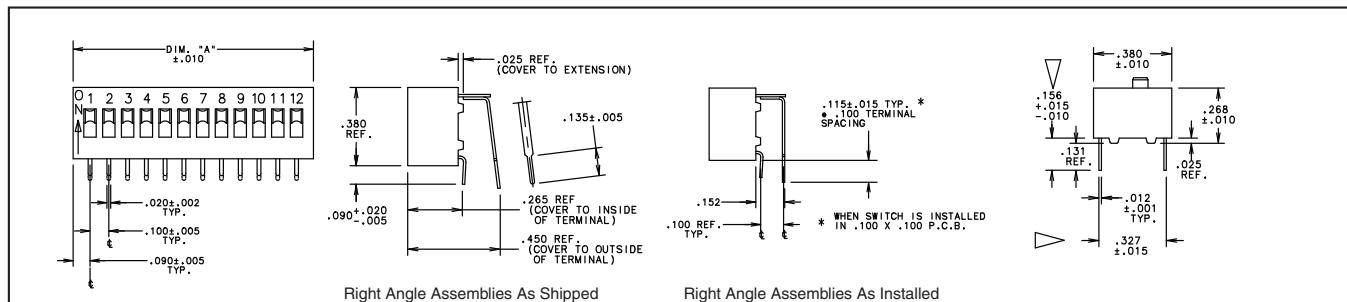
- Easy Access
- SPST Circuitry
- 1-10 and 12 positions available
- Sealed versions available

APPLICATIONS

Telecommunications, computers and peripherals, instruments and controls.



Series 78B DIMENSIONS in inches (and millimeters)



SPECIFICATIONS

Mechanical

Mechanical Life: 2,000 operations per switch.

Operation Temp: -40°C to + 85°C

Storage Temp: -55°C to + 85°C

Vibration Test: Per Method 204, Test Condition B, 1 mS opening (10 mS allowed)

Shock Test: MIL-STD-202F METHOD 213 Test Condition A, 1ms (10 allowed)

Electrical

Electrical Life: 10,000 operations per switch 24VDC, 25mA.

Non-Switching Rating: 100mA, 50VDC.

Switching rating: 150mA, 30DVC; 10mA, 50mVDC

Contact Resistance: 30mΩ max. at initial.

Insulation Resistance: (at 100VDC) 5,000MΩ min.

Dielectric Strength: 750VAC/1 minute.

Capacitance: 2pF max.

Soldering and Cleaning Process

*For the most current soldering & cleaning processing guidelines, reference Grayhill Dip Switch Processing Information, Bulletin 1234

Cleaning tape sealed products:

Passes immersion test using water/detergent. Acceptable solutions include 1-1-1 trichlorethane, freon, (TF, TE, or TMS), isopropyl alcohol, detergent (140°F maximum). Terpene acceptable for Series 90 only. Solutions which are not recommended include acetone, methylenechloride, freon TMC. Pressure wash cleaning processes are not recommended for tape seal switches.

Wave Soldering: Recommended solder temperature: 500°F (260C) max 5 seconds.

Hand Soldering: Use a soldering iron of 30 Watts or less, controlled at 608°F (320°C) approximately 2 seconds while applying solder.

Cleaning: Tape sealed versions withstand cleaning processes.

Materials

Contact Ball: Brass with gold plating over nickel

Terminals: Brass with gold plating over nickel

Nonconductive Parts: Plastic UL94V-0

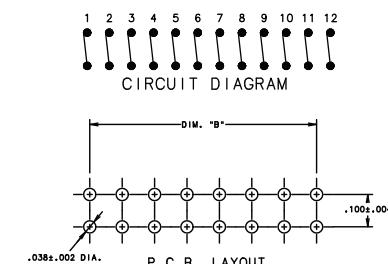
Potting Material: Epoxy

Shorting Member (Ball): Brass, gold-plated over nickel barrier.

Protective Cover: Polycarbonate.

Tape Seal: Polyester film

Tape Seal Integrity: Passes gross leak test using 125°C fluorinert for 20 seconds minimum. Reference MIL-STD-202, Method 112.



ORDERING INFORMATION

Series 78B, 78F, 78G, 78H, 78J, 78K, 78RB Styles available as right angle

Number of Positions 1 through 12 (depending on Series)

RoHS compliant

78B08SRAT

Right Angle

S= Top Tape Sealed, Blank=Unsealed

78R

78K

78H

78F

78J

Tape Sealed



LM555 Single Timer

Features

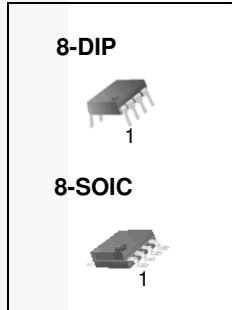
- High-Current Drive Capability: 200 mA
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From μ s to Hours
- Turn off Time Less Than 2 μ s

Applications

- Precision Timing
- Pulse Generation
- Delay Generation
- Sequential Timing

Description

The LM555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the delay is controlled by one external resistor and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.



Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package | Packing Method |
|-------------|-----------------------------|----------|---------|----------------|
| LM555CN | 0 ~ +70°C | LM555CN | DIP 8L | Rail |
| LM555CM | | LM555CM | SOIC 8L | Rail |
| LM555CMX | | LM555CM | SOIC 8L | Tape & Reel |

Block Diagram

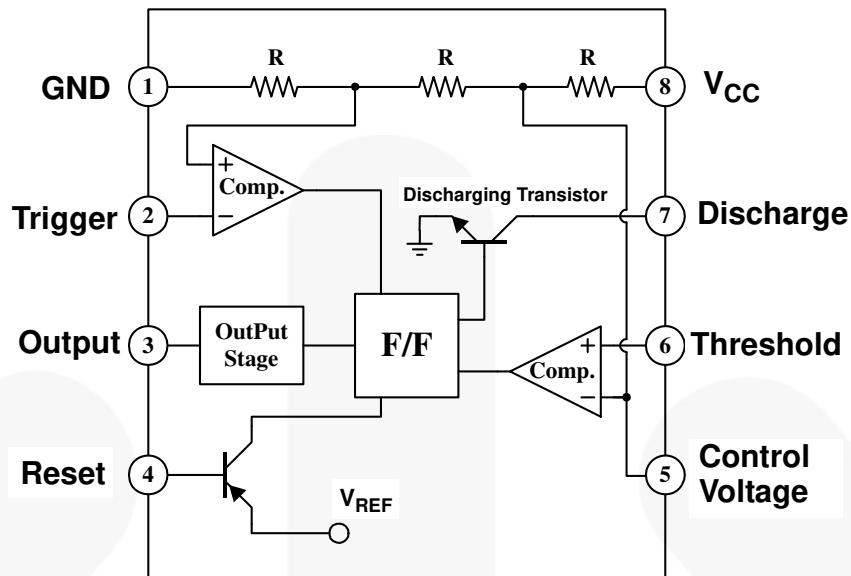


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|------------|----------------------------------|------------|------|
| V_{CC} | Supply Voltage | 16 | V |
| T_{LEAD} | Lead Temperature (Soldering 10s) | 300 | °C |
| P_D | Power Dissipation | 600 | mW |
| T_{OPR} | Operating Temperature Range | 0 ~ +70 | °C |
| T_{STG} | Storage Temperature Range | -65 ~ +150 | °C |

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5 \sim 15 \text{ V}$ unless otherwise specified.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit | |
|--------------------------------------------------------------|----------------------------|------------------------------------------------------------------------------------|-------------------------------|-------|-------|------------------------|----|
| Supply Voltage | V_{CC} | | 4.5 | | 16.0 | V | |
| Supply Current (Low Stable) ⁽¹⁾ | I_{CC} | $V_{CC} = 5 \text{ V}, R_L = \infty$ | | 3 | 6 | mA | |
| | | $V_{CC} = 15 \text{ V}, R_L = \infty$ | | 7.5 | 15.0 | mA | |
| Timing Error (Monostable) Initial Accuracy ⁽²⁾ | ACCUR | $R_A = 1 \text{ k}\Omega \text{ to } 100 \text{ k}\Omega$ $C = 0.1 \mu\text{F}$ | | 1.0 | 3.0 | % | |
| Drift with Temperature ⁽³⁾ | $\Delta t / \Delta T$ | | | 50 | | ppm / $^\circ\text{C}$ | |
| Drift with Supply Voltage ⁽³⁾ | $\Delta t / \Delta V_{CC}$ | | | 0.1 | 0.5 | % / V | |
| Timing Error (Astable) Initial Accuracy ⁽²⁾ | ACCUR | $R_A = 1 \text{ k}\Omega \text{ to } 100 \text{ k}\Omega$ $C = 0.1 \mu\text{F}$ | | 2.25 | | % | |
| Drift with Temperature ⁽³⁾ | $\Delta t / \Delta T$ | | | 150 | | ppm / $^\circ\text{C}$ | |
| Drift with Supply Voltage ⁽³⁾ | $\Delta t / \Delta V_{CC}$ | | | 0.3 | | % / V | |
| Control Voltage | V_C | $V_{CC} = 15 \text{ V}$ | 9.0 | 10.0 | 11.0 | V | |
| | | $V_{CC} = 5 \text{ V}$ | 2.60 | 3.33 | 4.00 | V | |
| Threshold Voltage | V_{TH} | $V_{CC} = 15 \text{ V}$ | | 10.0 | | V | |
| | | $V_{CC} = 5 \text{ V}$ | | 3.33 | | V | |
| Threshold Current ⁽⁴⁾ | I_{TH} | | | 0.10 | 0.25 | μA | |
| Trigger Voltage | V_{TR} | $V_{CC} = 5 \text{ V}$ | 1.10 | 1.67 | 2.20 | V | |
| | | $V_{CC} = 15 \text{ V}$ | 4.5 | 5.0 | 5.6 | V | |
| Trigger Current | I_{TR} | $V_{TR} = 0 \text{ V}$ | | 0.01 | 2.00 | μA | |
| Reset Voltage | V_{RST} | | 0.4 | 0.7 | 1.0 | V | |
| Reset Current | I_{RST} | | | 0.1 | 0.4 | mA | |
| Low Output Voltage | V_{OL} | $V_{CC} = 15 \text{ V}$ | $I_{SINK} = 10 \text{ mA}$ | | 0.06 | 0.25 | V |
| | | | $I_{SINK} = 50 \text{ mA}$ | | 0.30 | 0.75 | V |
| | | $V_{CC} = 5 \text{ V}$, $I_{SINK} = 5 \text{ mA}$ | | | 0.05 | 0.35 | V |
| High Output Voltage | V_{OH} | $V_{CC} = 15 \text{ V}$ | $I_{SOURCE} = 200 \text{ mA}$ | | 12.5 | | V |
| | | | $I_{SOURCE} = 100 \text{ mA}$ | 12.75 | 13.30 | | V |
| | | $V_{CC} = 5 \text{ V}$, $I_{SOURCE} = 100 \text{ mA}$ | | 2.75 | 3.30 | | V |
| Rise Time of Output ⁽³⁾ | t_R | | | | 100 | | ns |
| Fall Time of Output ⁽³⁾ | t_F | | | | 100 | | ns |
| Discharge Leakage Current | I_{LKG} | | | | 20 | 100 | nA |

Notes:

- When the output is high, the supply current is typically 1 mA less than at $V_{CC} = 5 \text{ V}$.
- Tested at $V_{CC} = 5.0 \text{ V}$ and $V_{CC} = 15 \text{ V}$.
- These parameters, although guaranteed, are not 100% tested in production.
- This determines the maximum value of $R_A + R_B$ for 15 V operation, the maximum total $R = 20 \text{ M}\Omega$, and for 5 V operation, the maximum total $R = 6.7 \text{ M}\Omega$.

Application Information

Table 1 below is the basic operating table of 555 timer.

Table 1. Basic Operating Table

| Reset (PIN 4) | V_{TR} (PIN 2) | V_{TH} (PIN 6) | Output (PIN 3) | Discharging Transistor (PIN 7) |
|------------------|---------------------|---------------------|-------------------|--------------------------------------|
| Low | X | X | Low | ON |
| High | $< 1/3 V_{CC}$ | X | High | OFF |
| High | $> 1/3 V_{CC}$ | $> 2/3 V_{CC}$ | Low | ON |
| High | $> 1/3 V_{CC}$ | $< 2/3 V_{CC}$ | | Previous State |

When the low signal input is applied to the reset terminal, the timer output remains low regardless of the threshold voltage or the trigger voltage. Only when the high signal is applied to the reset terminal, the timer's output changes according to threshold voltage and trigger voltage.

When the threshold voltage exceeds 2/3 of the supply voltage while the timer output is high, the timer's internal discharge transistor turns on, lowering the threshold voltage to below 1/3 of the supply voltage. During this time, the timer output is maintained low. Later, if a low signal is applied to the trigger voltage so that it becomes 1/3 of the supply voltage, the timer's internal discharge transistor turns off, increasing the threshold voltage and driving the timer output again at high.

1. Monostable Operation

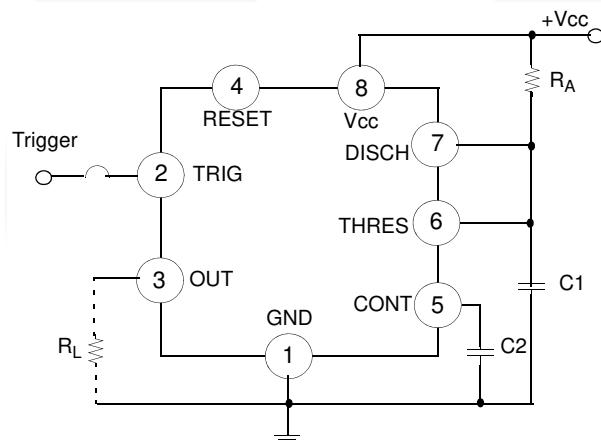
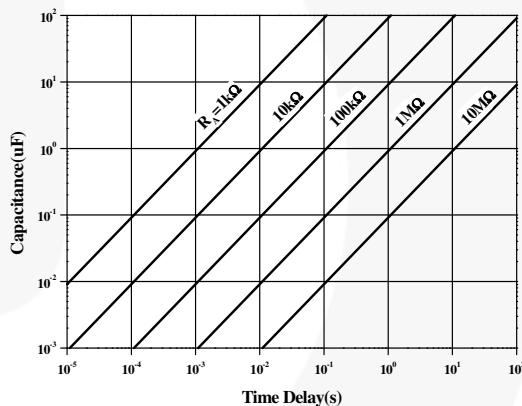


Figure 2. Monostable Circuit



**Figure 3. Resistance and Capacitance vs.
Time Delay (t_D)**

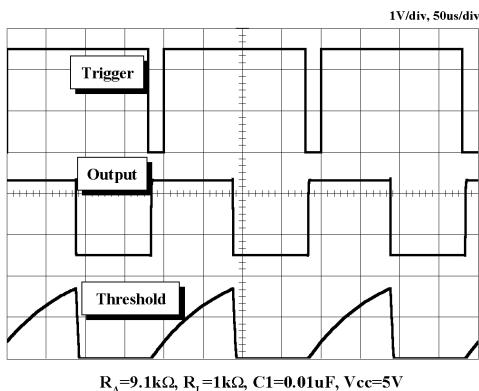


Figure 4. Waveforms of Monostable Operation

1. Monostable Operation

Figure 2 illustrates a monostable circuit. In this mode, the timer generates a fixed pulse whenever the trigger voltage falls below $V_{CC}/3$. When the trigger pulse voltage applied to the #2 pin falls below $V_{CC}/3$ while the timer output is low, the timer's internal flip-flop turns the discharging transistor off and causes the timer output to become high by charging the external capacitor C1 and setting the flip-flop output at the same time.

The voltage across the external capacitor C1, V_{C1} increases exponentially with the time constant $t = R_A \cdot C$ and reaches $2 V_{CC}/3$ at $t_D = 1.1 R_A \cdot C$. Hence, capacitor C1 is charged through resistor R_A . The greater the time constant $R_A C$, the longer it takes for the V_{C1} to reach $2 V_{CC}/3$. In other words, the time constant $R_A C$ controls the output pulse width.

When the applied voltage to the capacitor C1 reaches $2 V_{CC}/3$, the comparator on the trigger terminal resets the flip-flop, turning the discharging transistor on. At this time, C1 begins to discharge and the timer output converts to low. In this way, the timer operating in the monostable repeats the above process. Figure 3 shows the time constant relationship based on R_A and C. Figure 4 shows the general waveforms during the monostable operation.

It must be noted that, for a normal operation, the trigger pulse voltage needs to maintain a minimum of $V_{CC}/3$ before the timer output turns low. That is, although the output remains unaffected even if a different trigger pulse is applied while the output is high, it may be affected and the waveform does not operate properly if the trigger pulse voltage at the end of the output pulse remains at below $V_{CC}/3$. Figure 5 shows such a timer output abnormality.

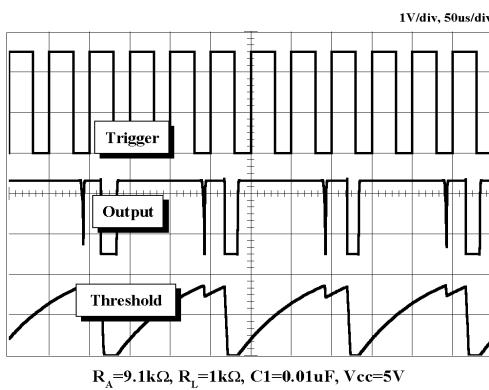


Figure 5. Waveforms of Monostable Operation
(abnormal)

2. Astable Operation

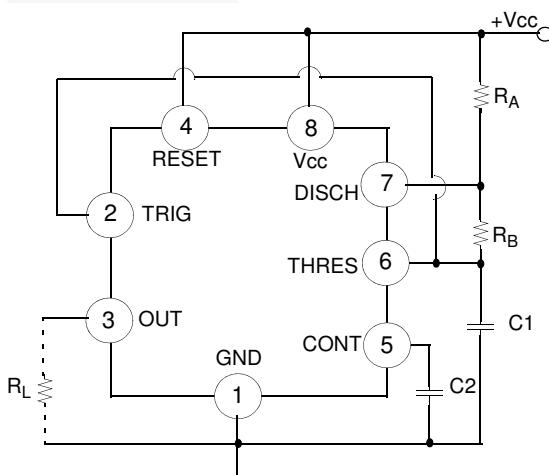


Figure 6. A Stable Circuit

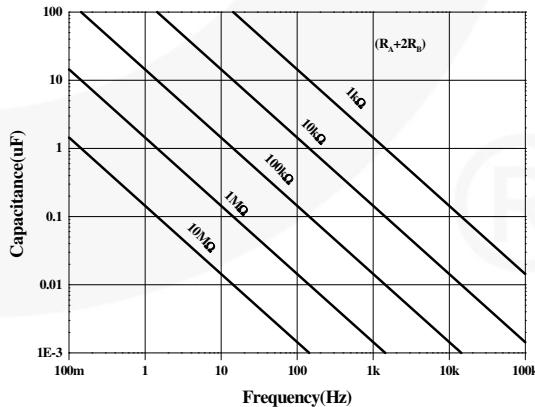


Figure 7. Capacitance and Resistance vs. Frequency

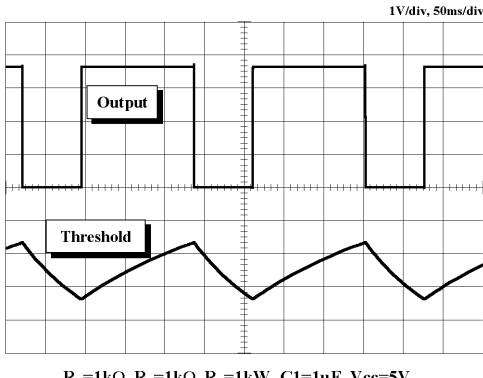
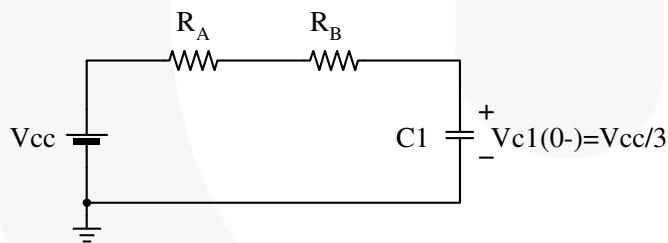


Figure 8. Waveforms of Astable Operation

An astable timer operation is achieved by adding resistor R_B to Figure 2 and configuring as shown on Figure 6. In the astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi-vibrator. When the timer output is high, its internal discharging transistor turns off and the V_{C1} increases by exponential function with the time constant $(R_A+R_B)*C$.

When the V_{C1} , or the threshold voltage, reaches $2 V_{CC}/3$; the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This turns on the discharging transistor and the $C1$ discharges through the discharging channel formed by R_B and the discharging transistor. When the V_{C1} falls below $V_{CC}/3$, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging transistor turns off and the V_{C1} rises again.

In the above process, the section where the timer output is high is the time it takes for the V_{C1} to rise from $V_{CC}/3$ to $2 V_{CC}/3$, and the section where the timer output is low is the time it takes for the V_{C1} to drop from $2 V_{CC}/3$ to $V_{CC}/3$. When timer output is high, the equivalent circuit for charging capacitor $C1$ is as follows:



$$C_1 \frac{dv_{c1}}{dt} = \frac{V_{cc} - V(0-)}{R_A + R_B} \quad (1)$$

$$V_{C1}(0+) = V_{CC}/3 \quad (2)$$

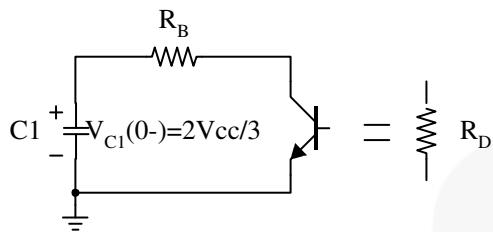
$$V_{C1}(t) = V_{CC} \left(1 - \frac{2}{3} e^{-\left(\frac{t}{(R_A + R_B)C_1} \right)} \right) \quad (3)$$

Since the duration of the timer output high state (t_L) is the amount of time it takes for the $V_{C1}(t)$ to reach $2 V_{CC}/3$,

$$V_{C1}(t) = \frac{2}{3} V_{CC} = V_{CC} \left(1 - \frac{2}{3} e^{-\left(\frac{t_H}{(R_A + R_B)C_1} \right)} \right) \quad (4)$$

$$t_H = C_1(R_A + R_B) \ln 2 = 0.693(R_A + R_B)C_1 \quad (5)$$

The equivalent circuit for discharging capacitor C1, when timer output is low is, as follows:



$$C_1 \frac{dv_{C1}}{dt} + \frac{1}{R_A + R_B} v_{C1} = 0 \quad (6)$$

$$v_{C1}(t) = \frac{2}{3} V_{CC} e^{-\frac{t}{(R_A + R_D)C_1}} \quad (7)$$

Since the duration of the timer output low state (t_L) is the amount of time it takes for the $V_{C1}(t)$ to reach $V_{CC}/3$,

$$\frac{1}{3} V_{CC} = \frac{2}{3} V_{CC} e^{-\frac{t_L}{(R_A + R_D)C_1}} \quad (8)$$

$$t_L = C_1 (R_B + R_D) \ln 2 = 0.693 (R_B + R_D) C_1 \quad (9)$$

Since R_D is normally $R_B \gg R_D$ although related to the size of discharging transistor,

$$t_L = 0.693 R_B C_1 \quad (10)$$

Consequently, if the timer operates in astable, the period is the same with ' $t = t_H + t_L = 0.693(R_A + R_B)C_1 + 0.693R_B C_1 = 0.693(R_A + 2R_B)C_1$ '

because the period is the sum of the charge time and discharge time. Since frequency is the reciprocal of the period, the following applies:

$$\text{frequency, } f = \frac{1}{t} = \frac{1.44}{(R_A + 2R_B)C_1} \quad (11)$$

3. Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 9. illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

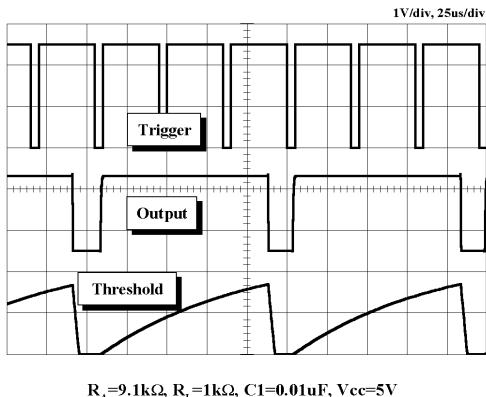


Figure 9. Waveforms of Frequency Divider Operation

4. Pulse Width Modulation

The timer output waveform may be changed by modulating the control voltage applied to the timer's pin 5 and changing the reference of the timer's internal comparators. Figure 10 illustrates the pulse width modulation circuit.

When the continuous trigger pulse train is applied in the monostable mode, the timer output width is modulated according to the signal applied to the control terminal. Sine wave, as well as other waveforms, may be applied as a signal to the control terminal. Figure 11 shows the example of pulse width modulation waveform.

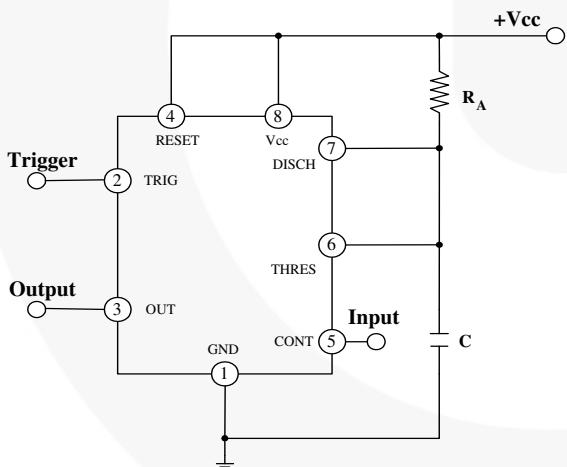


Figure 10. Circuit for Pulse Width Modulation

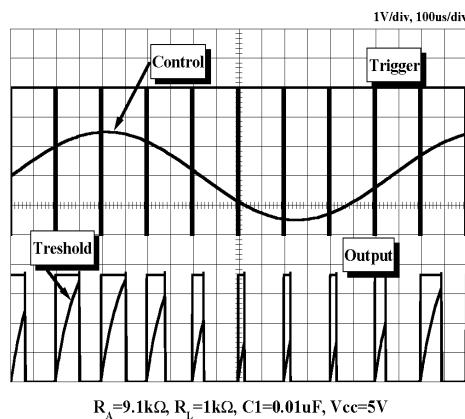


Figure 11. Waveforms of Pulse Width Modulation

5. Pulse Position Modulation

If the modulating signal is applied to the control terminal while the timer is connected for the astable operation, as in Figure 12, the timer becomes a pulse position modulator.

In the pulse position modulator, the reference of the timer's internal comparators is modulated, which modulates the timer output according to the modulation signal applied to the control terminal.

Figure 13 illustrates a sine wave for modulation signal and the resulting output pulse position modulation; however, any wave shape be used.

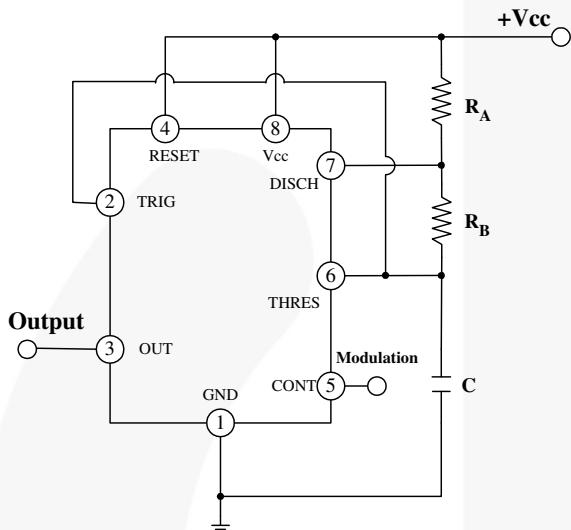


Figure 12. Circuit for Pulse Position Modulation

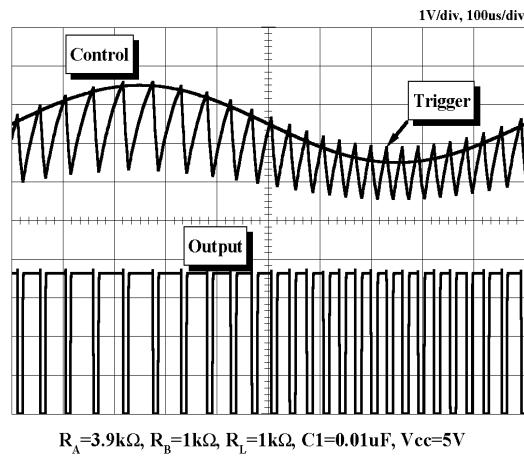


Figure 13. Waveforms of pulse position modulation

6. Linear Ramp

When the pull-up resistor R_A in the monostable circuit shown in Figure 2 is replaced with constant current source, the V_{C1} increases linearly, generating a linear ramp. Figure 14 shows the linear ramp generating circuit and Figure 15 illustrates the generated linear ramp waveforms.

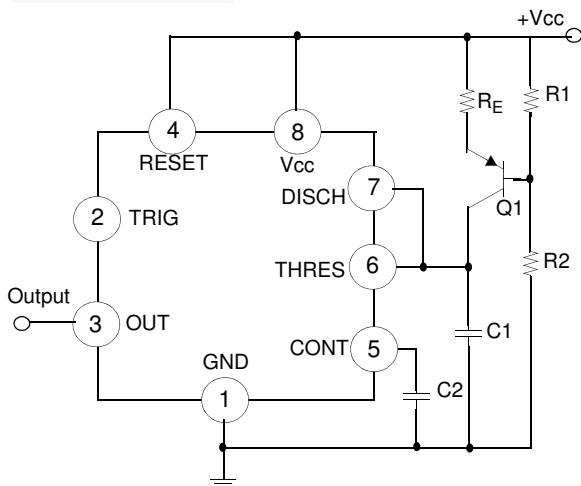


Figure 14. Circuit for Linear Ramp

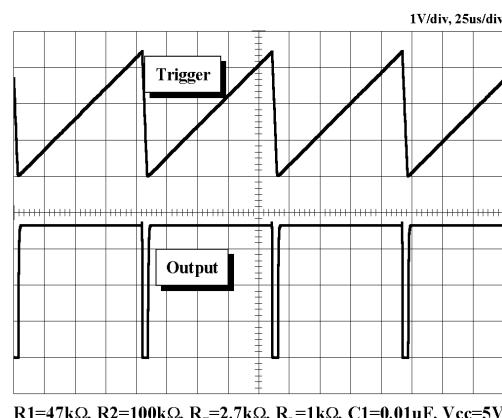


Figure 15. Waveforms of Linear Ramp

In Figure 14, current source is created by PNP transistor Q1 and resistor R1, R2, and R_E .

$$I_C = \frac{V_{CC} - V_E}{R_E} \quad (12)$$

Here, V_E is

$$V_E = V_{BE} + \frac{R_2}{R_1 + R_2} V_{CC} \quad (13)$$

For example, if $V_{CC} = 15$ V, $R_E = 20$ k Ω , $R_1 = 5$ k Ω , $R_2 = 10$ k Ω , and $V_{BE} = 0.7$ V,
 $V_E = 0.7$ V + 10 V = 10.7 V, and
 $I_C = (15 - 10.7) / 20$ k = 0.215 mA.

When the trigger starts in a timer configured as shown in Figure 14, the current flowing through capacitor C1 becomes a constant current generated by PNP transistor and resistors.

Hence, the V_C is a linear ramp function as shown in Figure 15. The gradient S of the linear ramp function is defined as follows:

$$S = \frac{V_p - p}{t} \quad (14)$$

Here the V_{p-p} is the peak-to-peak voltage.

If the electric charge amount accumulated in the capacitor is divided by the capacitance, the V_C comes out as follows:

$$V = Q/C \quad (15)$$

The above equation divided on both sides by t gives:

$$\frac{V}{t} = \frac{Q \cdot t}{C} \quad (16)$$

and may be simplified into the following equation:

$$S = I/C \quad (17)$$

In other words, the gradient of the linear ramp function appearing across the capacitor can be obtained by using the constant current flowing through the capacitor.

If the constant current flow through the capacitor is 0.215 mA and the capacitance is 0.02 μ F, the gradient of the ramp function at both ends of the capacitor is $S = 0.215$ m / 0.022 μ = 9.77 V/ms.

SNx400, SNx4LS00, and SNx4S00 Quadruple 2-Input Positive-NAND Gates

1 Features

- Package Options Include:
 - Plastic Small-Outline (D, NS, PS)
 - Shrink Small-Outline (DB)
 - Ceramic Flat (W)
 - Ceramic Chip Carriers (FK)
 - Standard Plastic (N)
 - Ceramic (J)
- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package
- Inputs Are TTL Compliant; $V_H = 2$ V and $V_{IL} = 0.8$ V
- Inputs Can Accept 3.3-V or 2.5-V Logic Inputs
- SN5400, SN54LS00, and SN54S00 are Characterized For Operation Over the Full Military Temperature Range of -55°C to 125°C

2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-Ray Players
- Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)

3 Description

The SNx4xx00 devices contain four independent, 2-input NAND gates. The devices perform the Boolean function $Y = A \cdot B$ or $Y = \bar{A} + B$ in positive logic.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------------------------------|-----------|--------------------|
| SN74LS00DB | SSOP (14) | 6.20 mm × 5.30 mm |
| SN7400D, SN74LS00D, SN74S00D | SOIC (14) | 8.65 mm × 3.91 mm |
| SN74LS00NSR | PDIP (14) | 19.30 × 6.35 mm |
| SNJ5400J, SNJ54LS00J, SNJ54S00J | CDIP (14) | 19.56 mm × 6.67 mm |
| SNJ5400W, SNJ54LS00W, SNJ54S00W | CFP (14) | 9.21 mm × 5.97 mm |
| SN54LS00FK, SN54S00FK | LCCC (20) | 8.89 mm × 8.89 mm |
| SN7400NS, SN74LS00NS, SN74S00NS | SO (14) | 10.30 mm × 5.30 mm |
| SN7400PS, SN74LS00PS | SO (8) | 6.20 mm × 5.30 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Gate (Positive Logic)

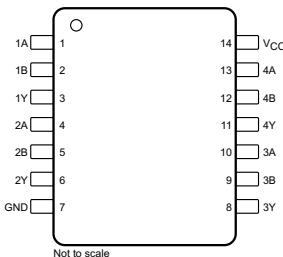


An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

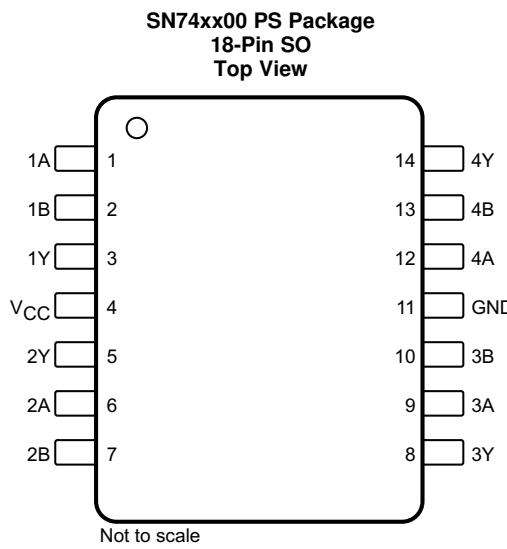
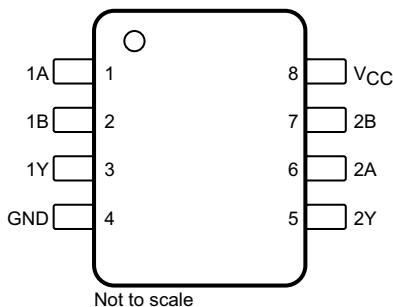
5 Pin Configuration and Functions

**SN5400 J, SN54xx00 J and W, SN74x00 D, N, and NS, or
SN74LS00 D, DB, N, and NS Packages
14-Pin CDIP, CFP, SOIC, PDIP, SO, or SSOP**

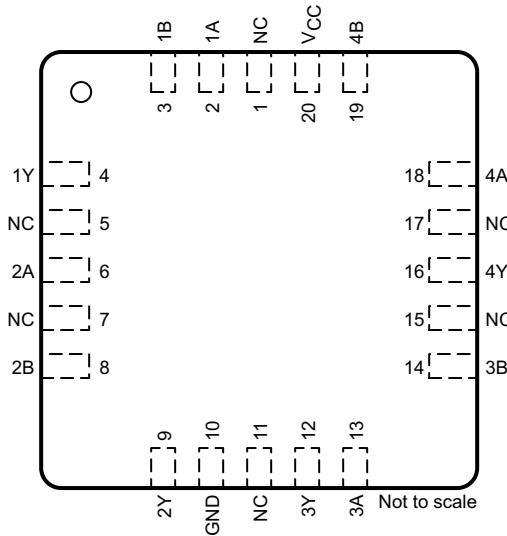
Top View



**SN5400 W Package
14-Pin CFP
Top View**



**SN54xx00 FK Package
20-Pin LCCC
Top View**



Pin Functions

| NAME | PIN | | | | I/O | DESCRIPTION |
|------|------------------------------------|------------------|-----------------|------|-----|---------------|
| | CDIP, CFP, SOIC, PDIP, SO, SSOP | SO (SN74xx00) | CFP (SN5400) | LCCC | | |
| 1A | 1 | 1 | 1 | 2 | I | Gate 1 input |
| 1B | 2 | 2 | 2 | 3 | I | Gate 1 input |
| 1Y | 3 | 3 | 3 | 4 | O | Gate 1 output |
| 2A | 4 | 6 | 6 | 6 | I | Gate 2 input |
| 2B | 5 | 7 | 7 | 8 | I | Gate 2 input |
| 2Y | 6 | 5 | 5 | 9 | O | Gate 2 output |
| 3A | 10 | — | 9 | 13 | I | Gate 3 input |
| 3B | 9 | — | 10 | 14 | I | Gate 3 input |

Pin Functions (continued)

| NAME | PIN | | | | I/O | DESCRIPTION |
|-----------------|------------------------------------|------------------|-----------------|------------------------|-----|---------------|
| | CDIP, CFP, SOIC, PDIP, SO, SSOP | SO (SN74xx00) | CFP (SN5400) | LCCC | | |
| 3Y | 8 | — | 8 | 12 | O | Gate 3 output |
| 4A | 13 | — | 12 | 18 | I | Gate 4 input |
| 4B | 12 | — | 13 | 19 | I | Gate 4 input |
| 4Y | 11 | — | 14 | 16 | O | Gate 4 output |
| GND | 7 | 4 | 11 | 10 | — | Ground |
| NC | — | — | — | 1, 5, 7, 11, 15, 17 | — | No connect |
| V _{CC} | 14 | 8 | 4 | 20 | — | Power supply |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------------------------------------|--------------------|-----|-----|------|
| Supply voltage, V _{CC} ⁽²⁾ | | 7 | | V |
| Input voltage | SNx400 and SNxS400 | 5.5 | | V |
| | SNx4LS00 | 7 | | |
| Junction temperature, T _J | | 150 | | °C |
| Storage temperature, T _{stg} | | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings: SN74LS00

| | | | VALUE | UNIT |
|--------------------|----------------------------|--------------------------------------------------------------------------------|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. ESD Tested on SN74LS00N package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|-----------------|---------------------------|--------------------------------|------|-----|------|------|
| V _{CC} | Supply voltage | SN54xx00 | 4.5 | 5 | 5.5 | V |
| | | SN74xx00 | 4.75 | 5 | 5.25 | |
| V _{IH} | High-level input voltage | | 2 | | | V |
| V _{IL} | Low-level input voltage | SNx400, SN7LS400, and SNx4S00 | | | 0.8 | V |
| | | SN54LS00 | | | 0.7 | |
| I _{OH} | High-level output current | SN5400, SN54LS00, and SN74LS00 | | | -0.4 | mA |
| | | SNx4S00 | | | -1 | |
| I _{OL} | Low-level output current | SNx400 | | | 16 | mA |
| | | SN5LS400 | | | 4 | |
| | | SN7LS400 | | | 8 | |
| | | SNx4S00 | | | 20 | |

8 Detailed Description

8.1 Overview

The SNx4xx00 devices are quadruple, 2-input NAND gates which perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = A + B$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

The operating voltage of SN74xx00 is from 4.75-V to 5.25-V V_{CC} . The operating voltage of SN54xx00 is from 4.5-V to 5.5-V V_{CC} . The SN54xx00 devices are rated from -55°C to 125°C whereas SN74xx00 device are rated from 0°C to 70°C .

8.4 Device Functional Modes

Table 1 lists the functions of the devices.

Table 1. Functional Table (Each Gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

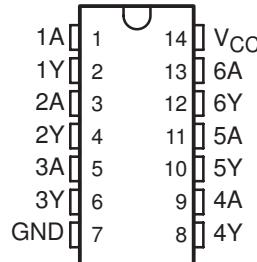
- Dependable Texas Instruments Quality and Reliability

description/ordering information

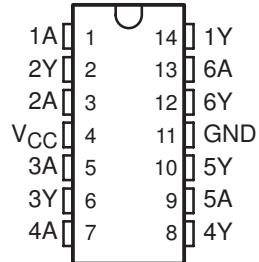
These devices contain six independent inverters.

SN5404 . . . J PACKAGE

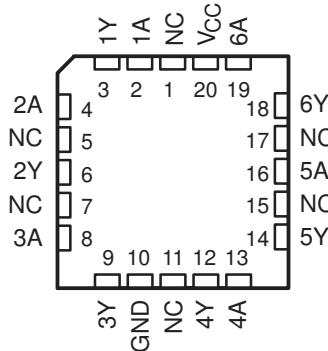
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



**SN5404 . . . W PACKAGE
(TOP VIEW)**



**SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS**

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

ORDERING INFORMATION

| TA | PACKAGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN7404N |
| | | Tube | SN74LS04N |
| | | Tube | SN74S04N |
| | SOIC – D | Tube | SN7404D |
| | | Tape and reel | SN7404DR |
| | | Tube | SN74LS04D |
| | | Tape and reel | SN74LS04DR |
| | | Tube | SN74S04D |
| | | Tape and reel | SN74S04DR |
| | SOP – NS | Tape and reel | SN7404NSR |
| | | Tape and reel | SN74LS04NSR |
| | | Tape and reel | SN74S04NSR |
| | SSOP – DB | Tape and reel | SN74LS04DBR |
| –55°C to 125°C | CDIP – J | Tube | SN5404J |
| | | Tube | SNJ5404J |
| | | Tube | SN54LS04J |
| | | Tube | SN54S04J |
| | | Tube | SNJ54LS04J |
| | | Tube | SNJ54S04J |
| | CFP – W | Tube | SNJ5404W |
| | | Tube | SNJ54LS04W |
| | | Tube | SNJ54S04W |
| | LCCC – FK | Tube | SNJ54LS04FK |
| | | Tube | SNJ54S04FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|---------|----------|
| H | L |
| L | H |



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SN5408, SN54LS08, SN54S08
 SN7408, SN74LS08, SN74S08
QUADRUPLE 2-INPUT POSITIVE-AND GATES
 SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

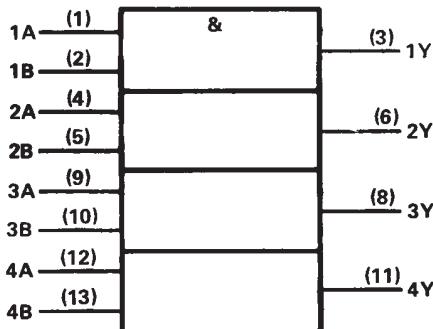
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C .

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

logic symbol†

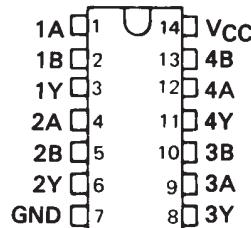


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

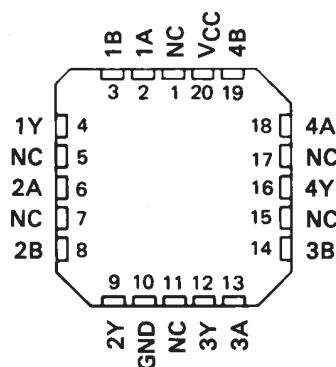
Pin numbers shown are for D, J, N, and W packages.

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
 SN7408 . . . J OR N PACKAGE
 SN74LS08, SN74S08 . . . D, J OR N PACKAGE

(TOP VIEW)

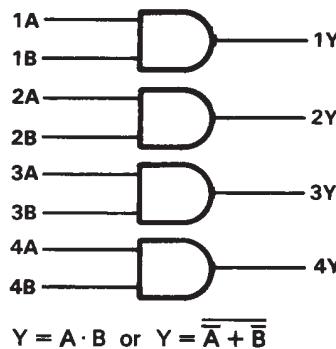


SN54LS08, SN54S08 . . . FK PACKAGE
 (TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



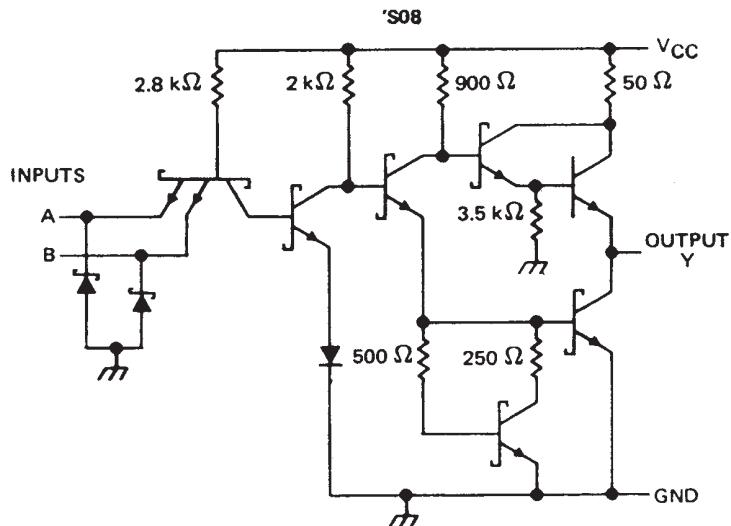
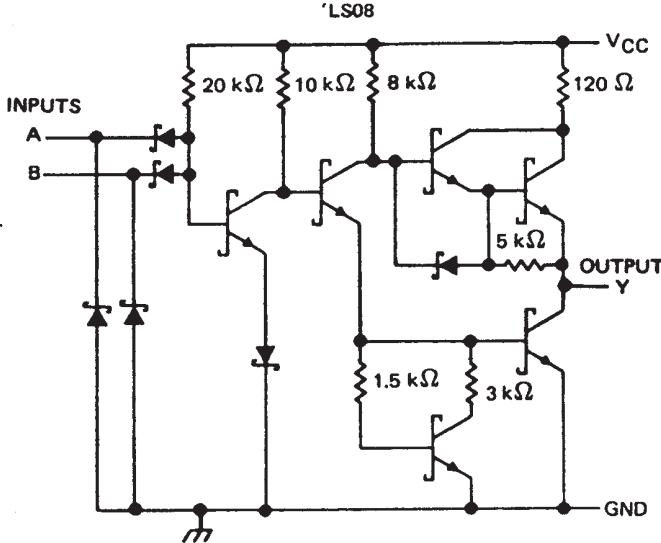
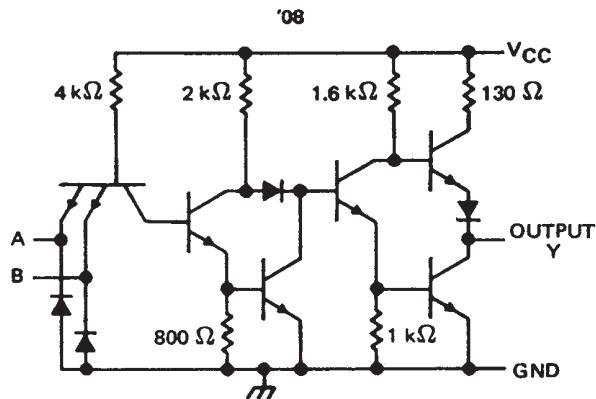
SN5408, SN54LS08, SN54S08

SN7408, SN74LS08, SN74S08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

schematics (each gate)



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--------------------------------------------------------|----------------|
| Supply voltage, V _{CC} (see Note 1) | 7 V |
| Input voltage: '08, 'S08 | 5.5 V |
| 'LS08 | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**SN5432, SN54LS32, SN54S32,
SN7432, SN74LS32, SN74S32**
QUADRUPLE 2-INPUT POSITIVE-OR GATES

DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

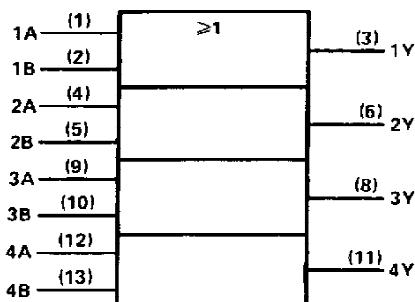
description

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C . The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

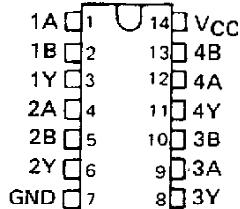
| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

logic symbol†

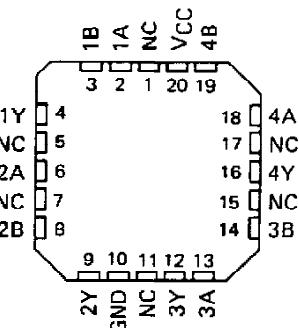
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, or W packages.

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . N PACKAGE
SN74LS32, SN74S32 . . . D OR N PACKAGE

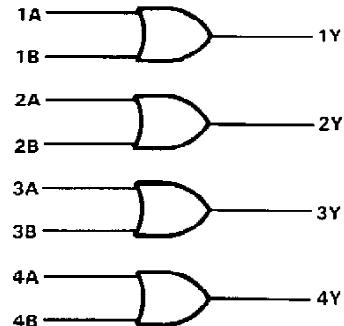
(TOP VIEW)



SN54LS32, SN54S32 . . . FK PACKAGE
(TOP VIEW)



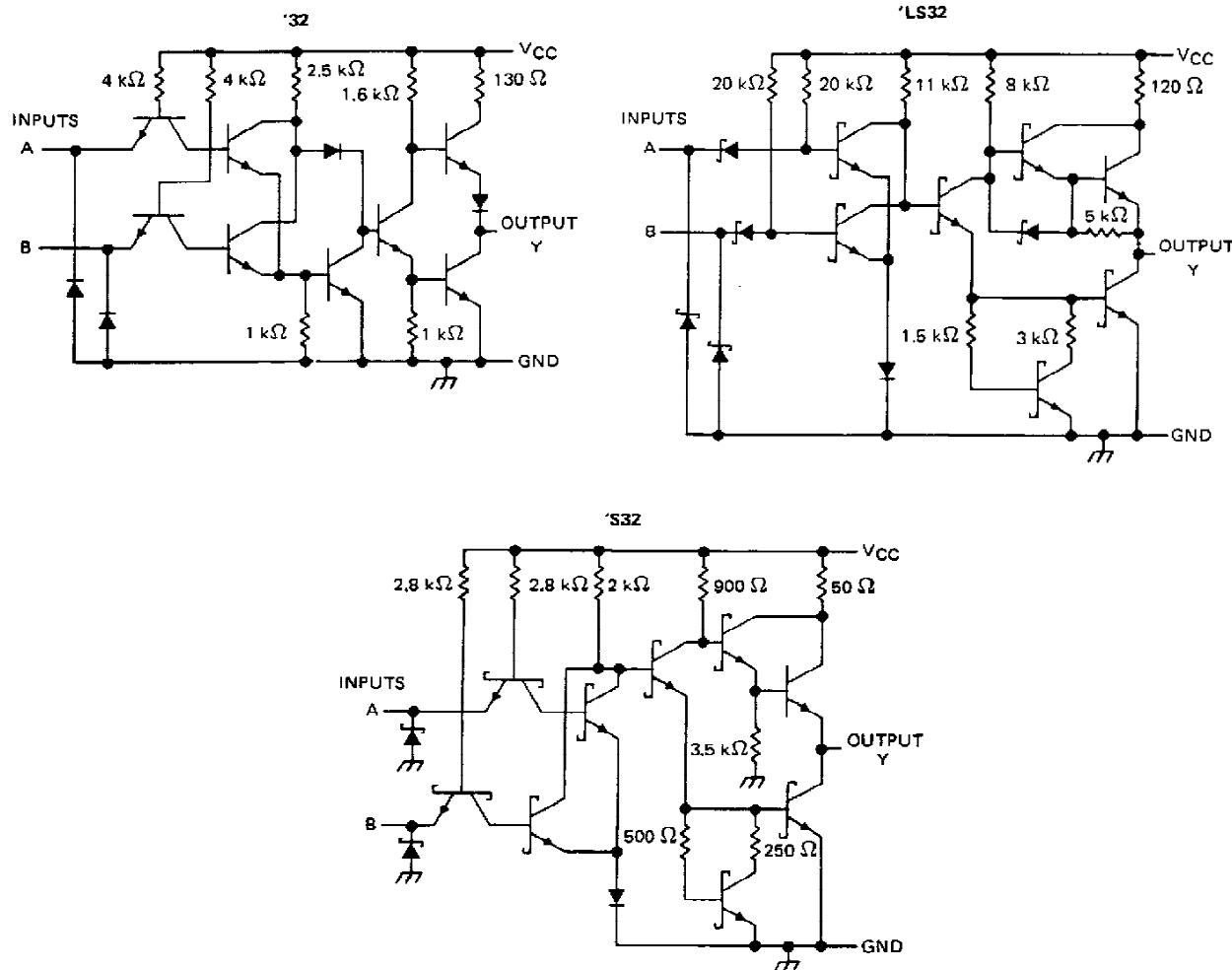
NC - No internal connection

logic diagram**positive logic**

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

**SN5432, SN54LS32, SN54S32,
SN7432, SN74LS32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--------------------------------------------------------|----------------|
| Supply voltage, V _{CC} (see Note 1) | 7 V |
| Input voltage: '32, 'S32 | 5.5 V |
| 'LS32 | 7 V |
| Operating free-air temperature: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS
INSTRUMENTS

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- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

| TYPE | TYPICAL AVERAGE | TYPICAL |
|--------|---------------------------|----------------------------|
| | PROPAGATION DELAY TIME | TOTAL POWER DISSIPATION |
| '86 | 14 ns | 150 mW |
| 'LS86A | 10 ns | 30.5 mW |
| 'S86 | 7 ns | 250 mW |

description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

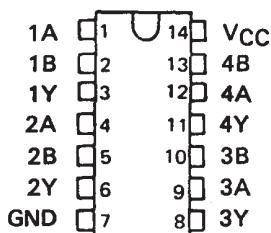
The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from 0°C to 70°C .

SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE

SN7486 . . . N PACKAGE

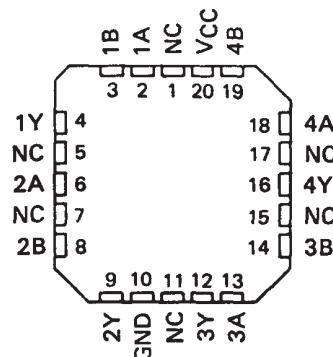
SN74LS86A, SN74S86 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS86A, SN54S86 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



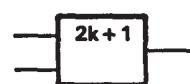
The output is active (low) if all inputs stand at the same logic level (i.e., $A=B$).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

OBSOLETE - No Longer Available

SN5486, SN54LS86A, SN54S86

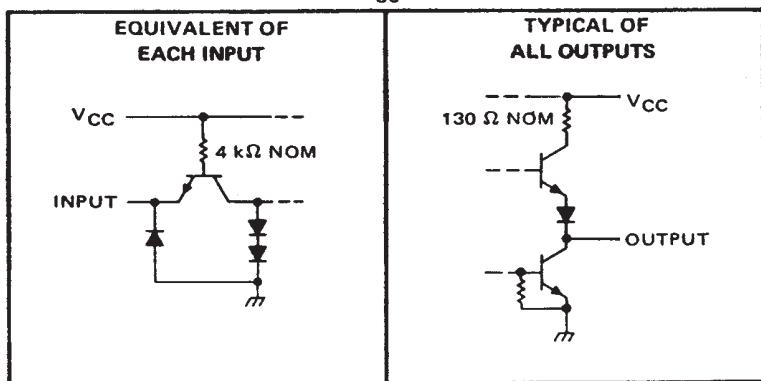
SN7486, SN74LS86A, SN74S86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

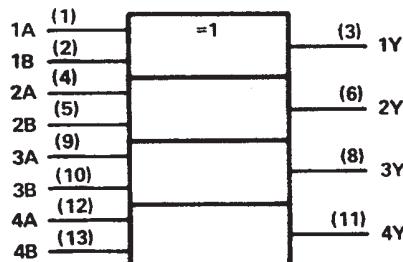
SDLS124 – DECEMBER 1972 – REVISED MARCH 1988

schematics of inputs and outputs

'86

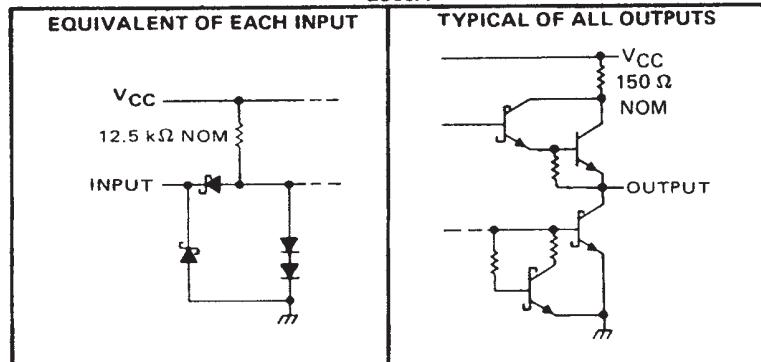


logic symbol†



†This symbol is in accordance with
ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

'LS86A

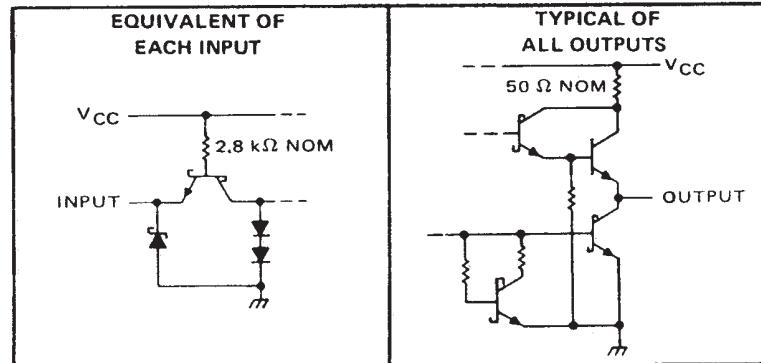


FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H = high level, L = low level

'S86



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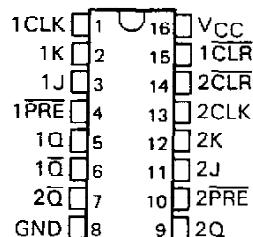
**SN54LS112A, SN54S112, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR**

D2661, APRIL 1982—REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54LS112A, SN54S112 . . . J OR W PACKAGE
SN74LS112A, SN74S112A . . . D OR N PACKAGE

(TOP VIEW)



description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

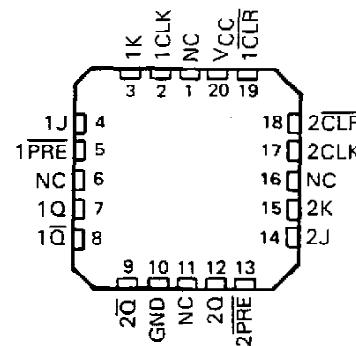
The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of $\sim -55^{\circ}\text{C}$ to 125°C . The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each flip-flop)

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|----------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | ↓ | L | L | Q ₀ | \bar{Q}_0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q ₀ | \bar{Q}_0 |

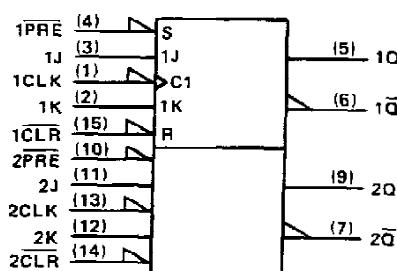
[†]The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN54LS112A, SN54S112 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol[‡]

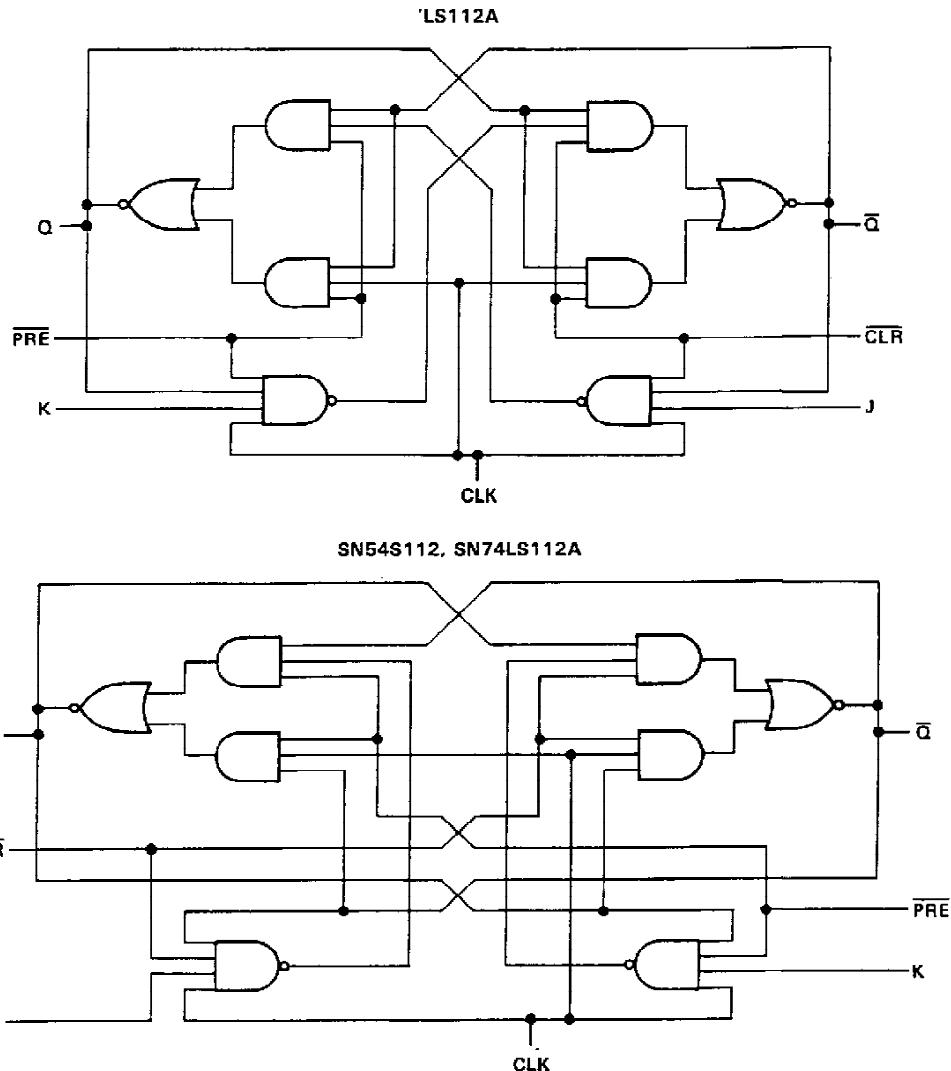


[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS112A, SN54S112, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

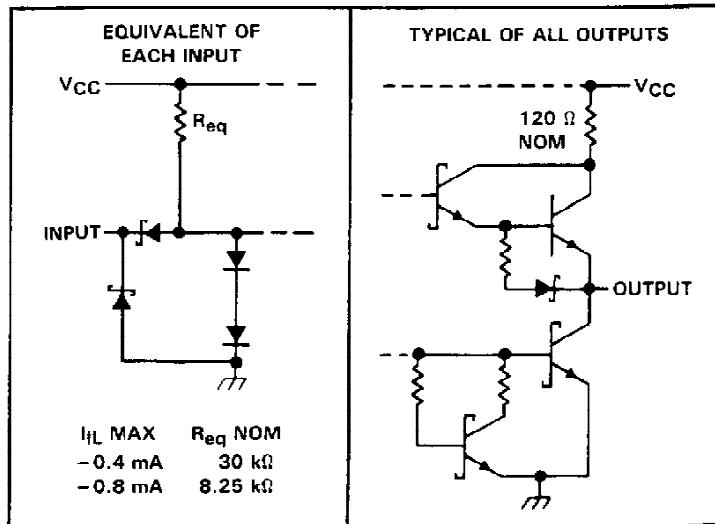
logic diagrams (positive logic)



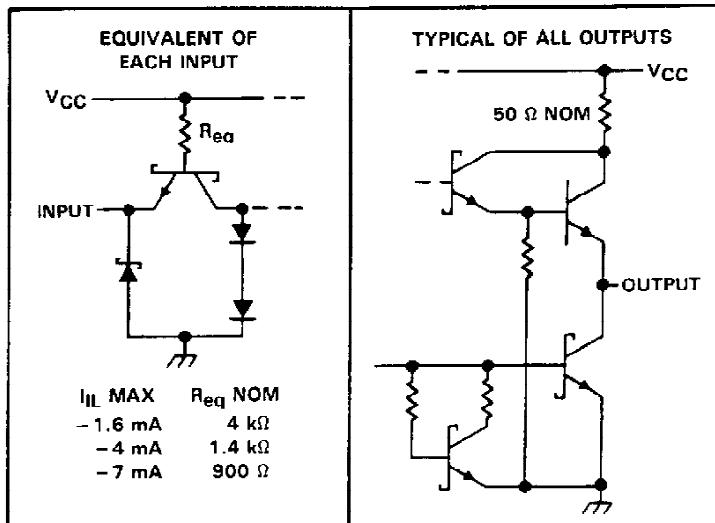
SN54LS112A, SN54S112, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs

'LS112A



SN54S112, SN74S112A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--------------------------------------------------------|----------------|
| Supply voltage, V _{CC} (see Note 1) | 7 V |
| Input voltage: 'LS112A | 7 V |
| SN54LS112, SN74LS112A | 5.5 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS112A, SN74LS112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

| | | | SN54LS112A | | | SN74LS112A | | | UNIT |
|--------------------|--------------------------------|------------------|------------|-----|------|------------|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| I _{OH} | High-level output current | | | | -0.4 | | | -0.4 | mA |
| I _{OL} | Low-level output current | | | | 4 | | | 8 | mA |
| f _{clock} | Clock frequency | | 0 | 30 | 0 | 0 | 30 | MHz | |
| t _w | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | PRE or CLR low | 25 | | | 25 | | | |
| t _{su} | Set up time-before CLK↓ | Data high or low | 20 | | | 20 | | | ns |
| | | CLR inactive | 25 | | | 25 | | | |
| | | PRE inactive | 20 | | | 20 | | | |
| t _h | Hold time-data after CLK↓ | | 0 | | | 0 | | | ns |
| T _A | Operating free-air temperature | | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | SN54LS112A | | | SN74LS112A | | | UNIT |
|-----------------------------|------------------------------------------------------------------------------------------------|-----------------------------------------------|------------------|-----|------------|------------------|------|------|
| | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | | | -1.5 | | -1.5 | V |
| V _{OH} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA | | 0.25 | 0.4 | 0.25 | 0.4 | | V |
| | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA | | | | 0.35 | 0.5 | | |
| I _I | J or K CLR or PRE CLK | V _{CC} = MAX, V _I = 7 V | 0.1 | | 0.1 | | | mA |
| | | | 0.3 | | 0.3 | | | |
| | | | 0.4 | | 0.4 | | | |
| I _{IH} | J or K CLR or PRE CLK | V _{CC} = MAX, V _I = 2.7 V | 20 | | 20 | | | μA |
| | | | 60 | | 60 | | | |
| | | | 80 | | 80 | | | |
| I _{IL} | J or K All other | V _{CC} = MAX, V _I = 0.4 V | -0.4 | | -0.4 | | | mA |
| | | | -0.8 | | -0.8 | | | |
| I _{OS[§]} | V _{CC} = MAX, see Note 2 | -20 | -100 | -20 | -100 | -20 | -100 | mA |
| I _{CC} (Total) | V _{CC} = MAX, see Note 3 | 4 | 6 | 4 | 6 | 4 | 6 | mA |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SDLS014

DECEMBER 1972—REVISED MARCH 1988

- Designed Specifically for High-Speed:
Memory Decoders
Data Transmission Systems
- 3 Enable Inputs to Simplify Cascading
and/or Data Reception
- Schottky-Clamped for High Performance

description

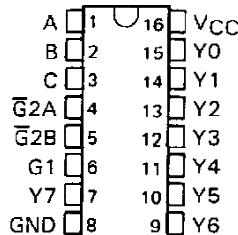
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138, SN54S138, and SN74S138A decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

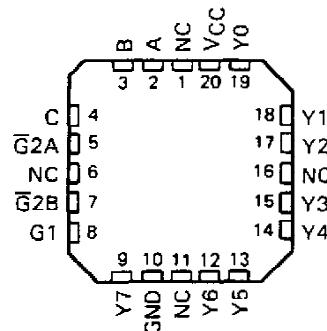
All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS138 and SN74S138A are characterized for operation from 0°C to 70°C .

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138A . . . D OR N PACKAGE
(TOP VIEW)

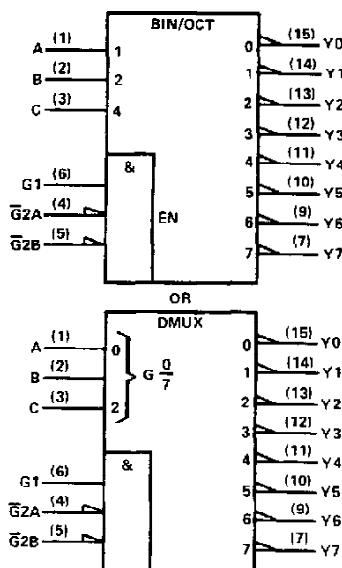


SN54LS138, SN54S138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbols[†]



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

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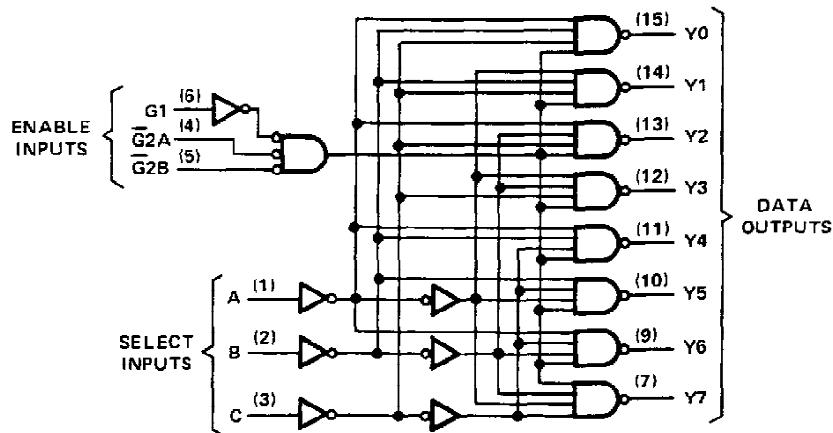
TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE-TO 8-LINE DECODERS/DEMULTIPLEXERS

logic diagram and function table

'LS138, SN54S138, SN74S138A



Pin numbers shown are for D, J, N, and W packages.

'LS138, SN54138, SN74S138A
FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | | | | | |
|--------|--------|-------|---------|-------|-------|-------|-------|-------|-------|-------|
| ENABLE | SELECT | | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| G1 | G2* | C B A | | | | | | | | |
| X | H | X X X | H H H | H H H | H H H | H H H | H H H | H H H | H H H | H H H |
| L | X | X X X | H H H | H H H | H H H | H H H | H H H | H H H | H H H | H H H |
| H | L | L L L | L H H | H H H | H H H | H H H | H H H | H H H | H H H | H H H |
| H | L | L L H | H L H | H H H | H H H | H H H | H H H | H H H | H H H | H H H |
| H | L | L H L | H H L | H H H | H H H | H H H | H H H | H H H | H H H | H H H |
| H | L | L H H | H H H | H H H | H H H | H H H | H H H | H H H | H H H | H H H |
| H | L | H L L | H H H | H H H | H H H | H H H | L H H | H H H | H H H | H H H |
| H | L | H L H | H H H | H H H | H H H | H H H | H H H | L H H | H H H | H H H |
| H | L | H H L | H H H | H H H | H H H | H H H | H H H | H L H | H H H | H H H |
| H | L | H H H | H H H | H H H | H H H | H H H | H H H | H H H | H L H | H H H |
| H | L | H H H | H H H | H H H | H H H | H H H | H H H | H H H | H H L | H H H |

* $\bar{G}2 = \bar{G}2A + \bar{G}2B$

H = high level, L = low level, X = irrelevant

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS139A, SN54S139, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS

SDLS013A

DECEMBER 1972 - REVISED MARCH 1988

- Designed Specifically for High-Speed:
Memory Decoders
Data Transmission Systems
- Two Fully Independent 2- to 4-Line Decoders/Demultiplexers
- Schottky Clamped for High Performance

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

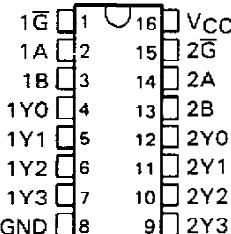
All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and SN54S139 are characterized for operation range of -55°C to 125°C . The SN74LS139A and SN74S139A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

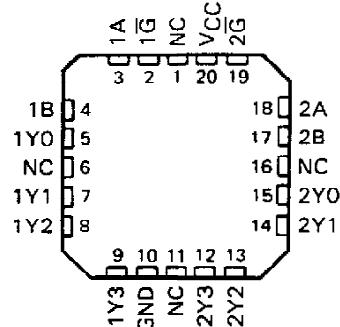
| INPUTS | | OUTPUTS | | | |
|--------|--------|---------|----|----|----|
| ENABLE | SELECT | Y0 | Y1 | Y2 | Y3 |
| G | B A | | | | |
| H | X X | H | H | H | H |
| L | L L | L | H | H | H |
| L | L H | H | L | H | H |
| L | H L | H | H | L | H |
| L | H H | H | H | H | L |

H = high level, L = low level, X = irrelevant

SN54LS139A, SN54S139 . . . J OR W PACKAGE
SN74LS139A, SN74S139A . . . D OR N PACKAGE
(TOP VIEW)

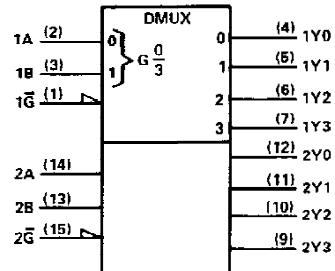
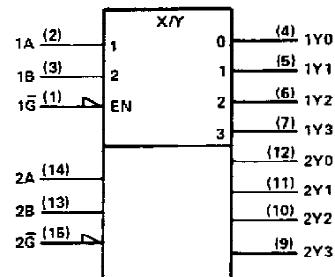


SN54LS139A, SN54S139 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

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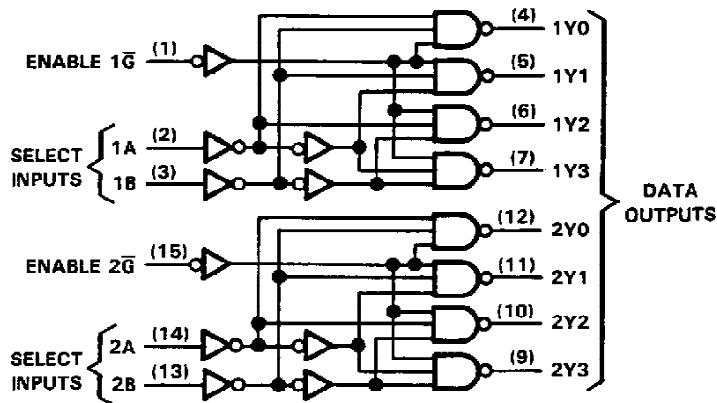
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TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

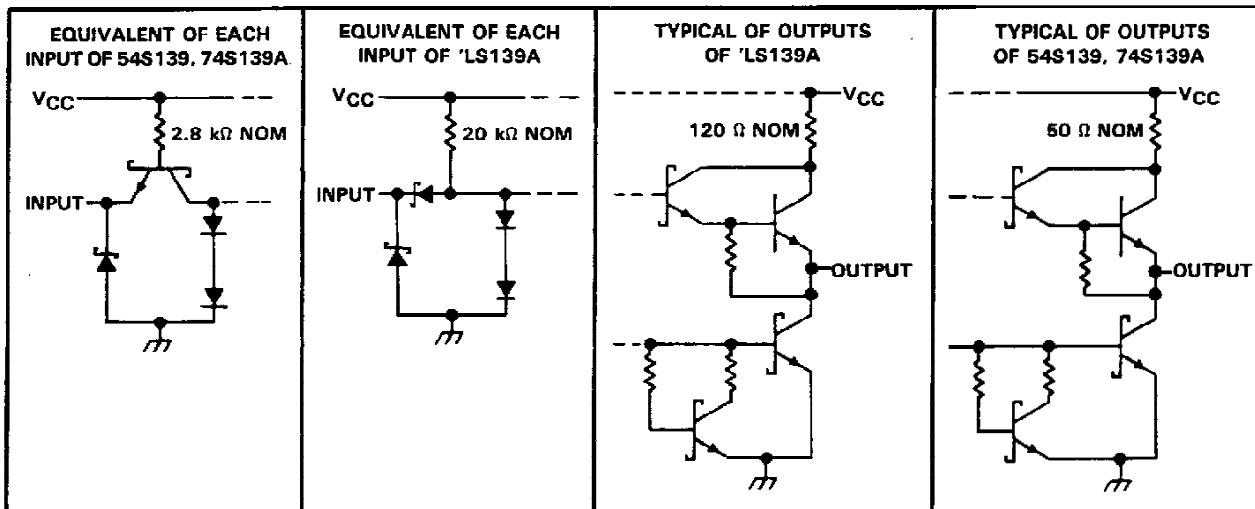
SN54LS139A, SN54S139, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|----------------------------------------------------------------------|----------------|
| Supply voltage, V _{CC} (See Note 1) | 7 V |
| Input voltage: 'LS139A | 7 V |
| 54S139, 74S139A | 5.5 V |
| Operating free-air temperature range: SN54LS139A, SN54S139 | -55°C to 125°C |
| SN74LS139A, SN74S139A | 0° C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SDLS058

**SN54157, SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158**
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

MARCH 1974 — REVISED MARCH 1988

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

| TYPES | TYPICAL AVERAGE PROPAGATION TIME | TYPICAL POWER DISSIPATION | SN54157, SN54LS157, SN54S157, SN54LS158, SN54S158 . . . J OR W PACKAGE SN74157 . . . N PACKAGE SN74LS157, SN74S157, SN74LS158, SN74S158 . . . D OR N PACKAGE |
|--------|-------------------------------------------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | (TOP VIEW) | | |
| '157 | 9 ns | 150 mW | A/B 1 16 VCC |
| 'LS157 | 9 ns | 49 mW | 1A 2 15 G |
| 'S157 | 5 ns | 250 mW | 1B 3 14 4A |
| 'LS158 | 7 ns | 24 mW | 1Y 4 13 4B |
| 'S158 | 4 ns | 195 mW | 2A 5 12 4Y |
| | | | 2B 6 11 3A |
| | | | 2Y 7 10 3B |
| | | | GND 8 9 3Y |

applications

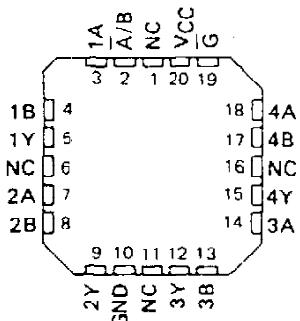
- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables
(One Variable Is Common)
- Source Programmable Counters

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

SN54LS157, SN54S157, SN54LS158,
SN54S158 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

| INPUTS | | | OUTPUT Y | |
|-------------|---------------|---|----------|----------------------------------|
| STROBE G | SELECT A/B | A | B | '157, 'LS157, 'S157 'LS158 |
| H | X | X | X | L H |
| L | L | L | X | L H |
| L | L | H | X | H L |
| L | H | X | L | L H |
| L | H | X | H | H L |

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--------------------------------------------------------|----------------|
| Supply voltage, V _{CC} (See Note 1) | 7 V |
| Input voltage: '157, 'S158 | 5.5 V |
| 'LS157, 'LS158 | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

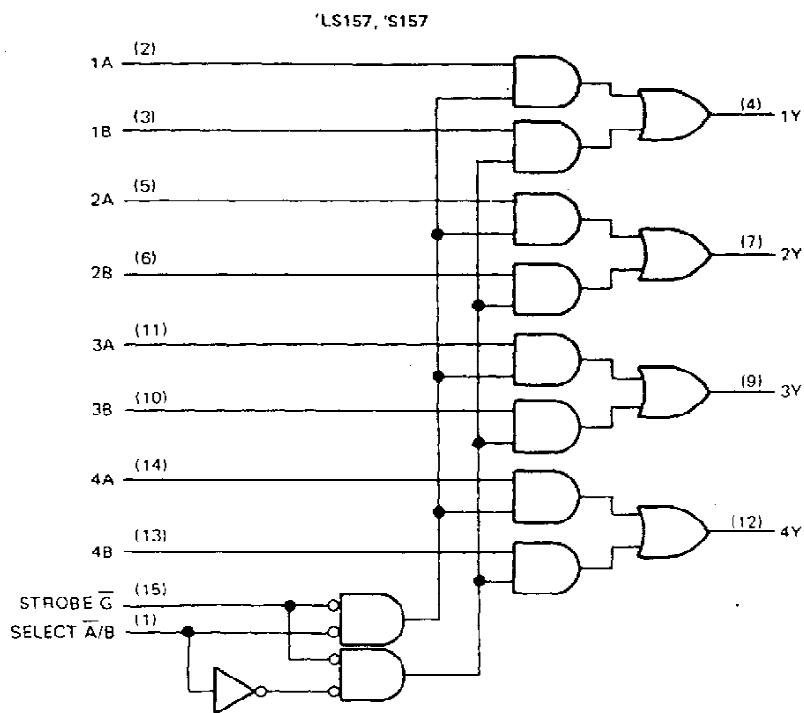
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TEXAS
INSTRUMENTS

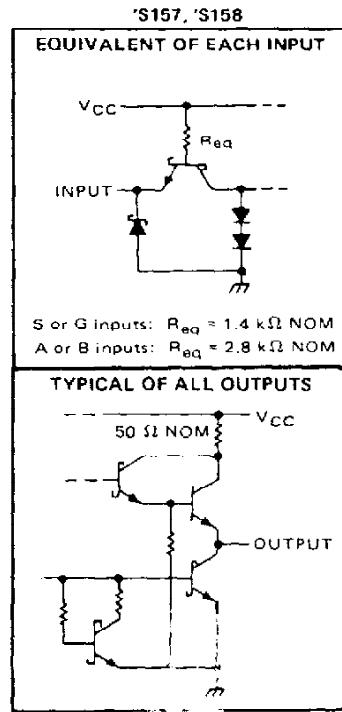
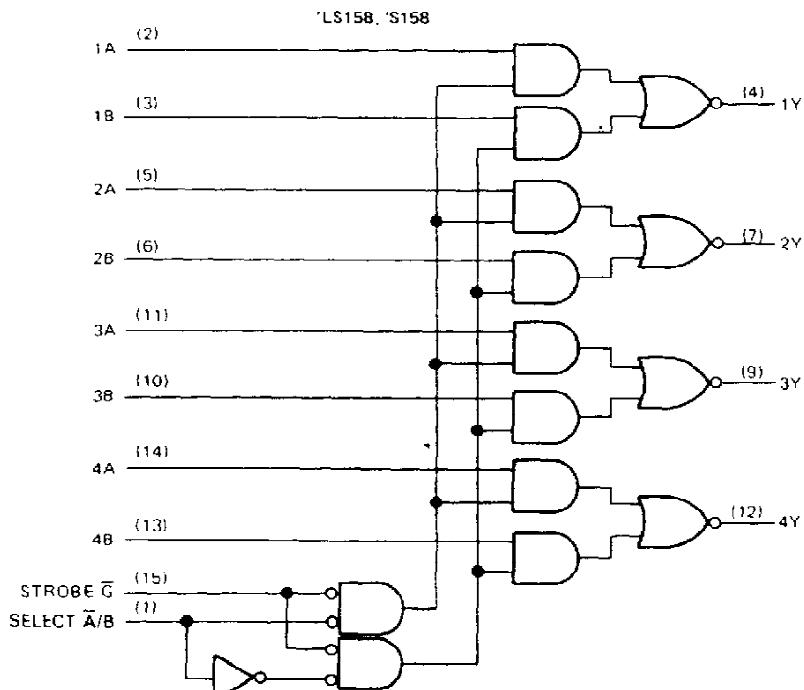
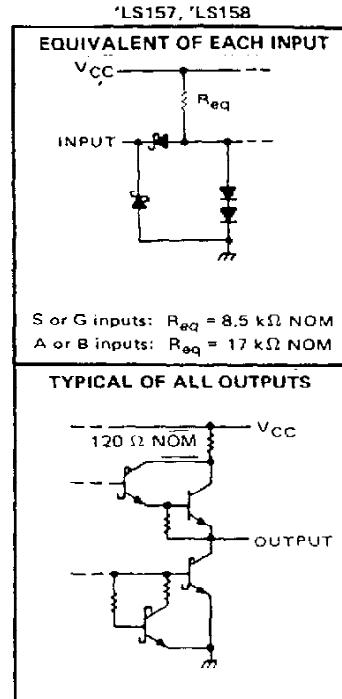
POST OFFICE BOX 5012 - DALLAS, TEXAS 75222

**SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74LS157, SN74LS158, SN74S157, SN74S158**
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

logic diagrams (positive logic)



schematics of inputs and outputs



Pin numbers shown are for D, J, N, and W packages.


**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS**

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

**'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS**

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

| TYPE | TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT | | MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
|----------------------|---------------------------------------------|-------|-------------------------|---------------------------|
| | TYPICAL | CLOCK | | |
| '160 thru '163 | 14 ns | | 32 MHz | 305 mW |
| 'LS162A thru 'LS163A | 14 ns | | 32 MHz | 93 mW |
| 'S162 and 'S163 | 9 ns | | 70 MHz | 475 mW |

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

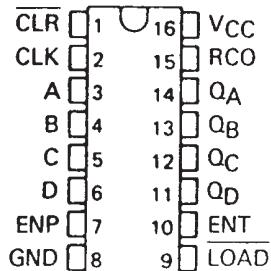
These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

SERIES 54', 54LS' . . . J OR W PACKAGE

SERIES 74' . . . N PACKAGE

SERIES 74LS', 74S' . . . D OR N PACKAGE

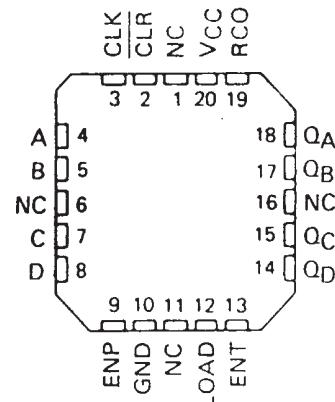
(TOP VIEW)



NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

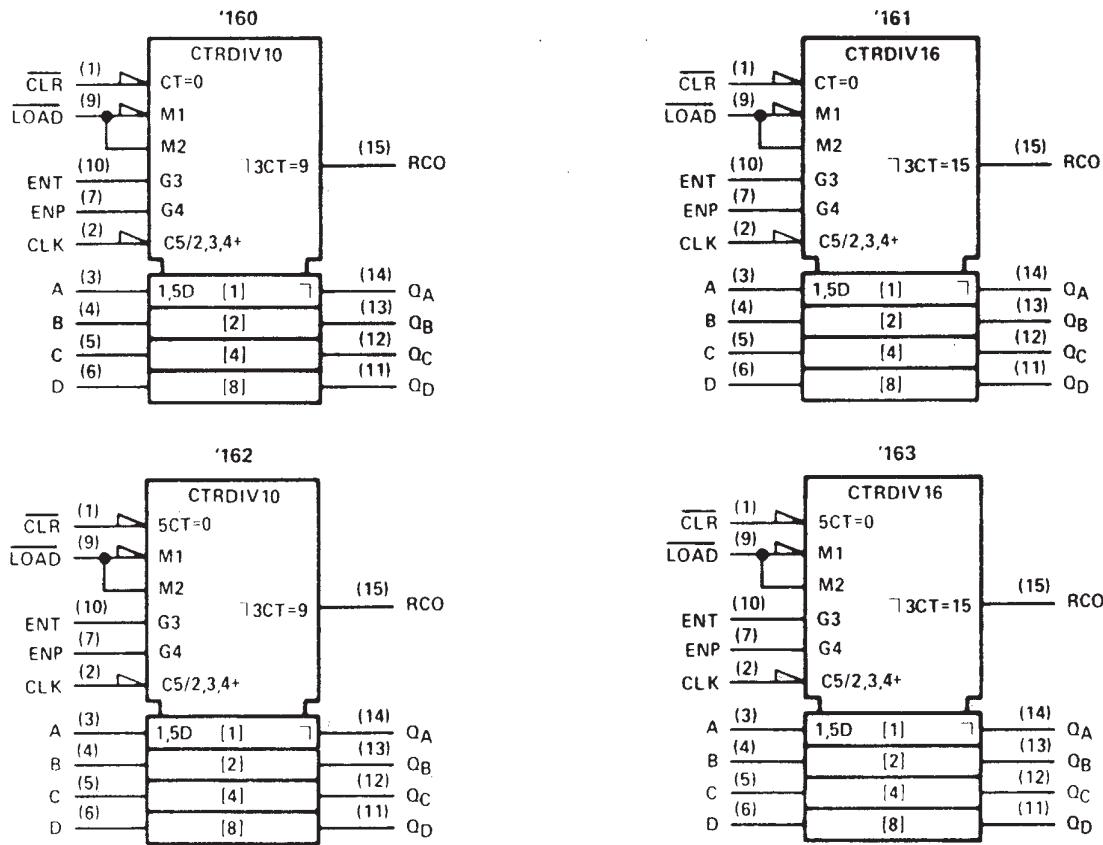
**SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS**

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols†



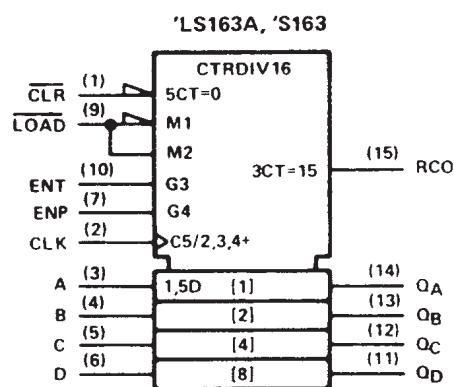
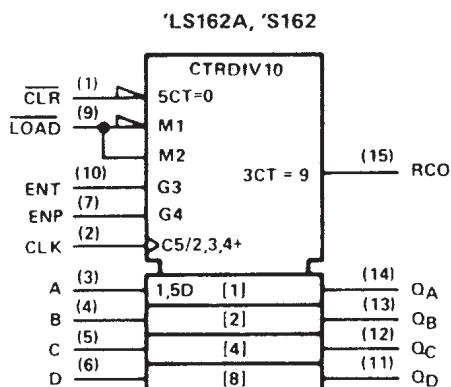
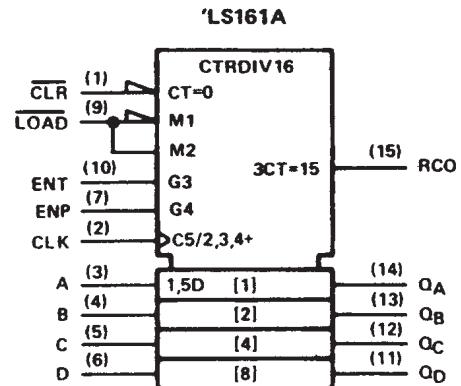
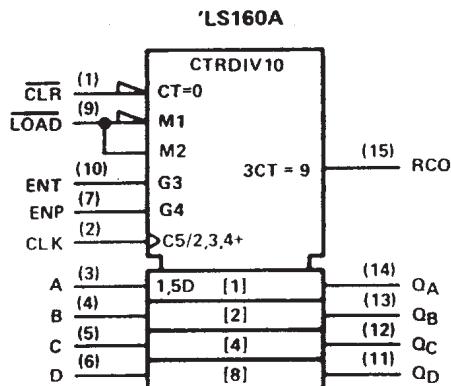
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

**SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS**

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic symbols (continued)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

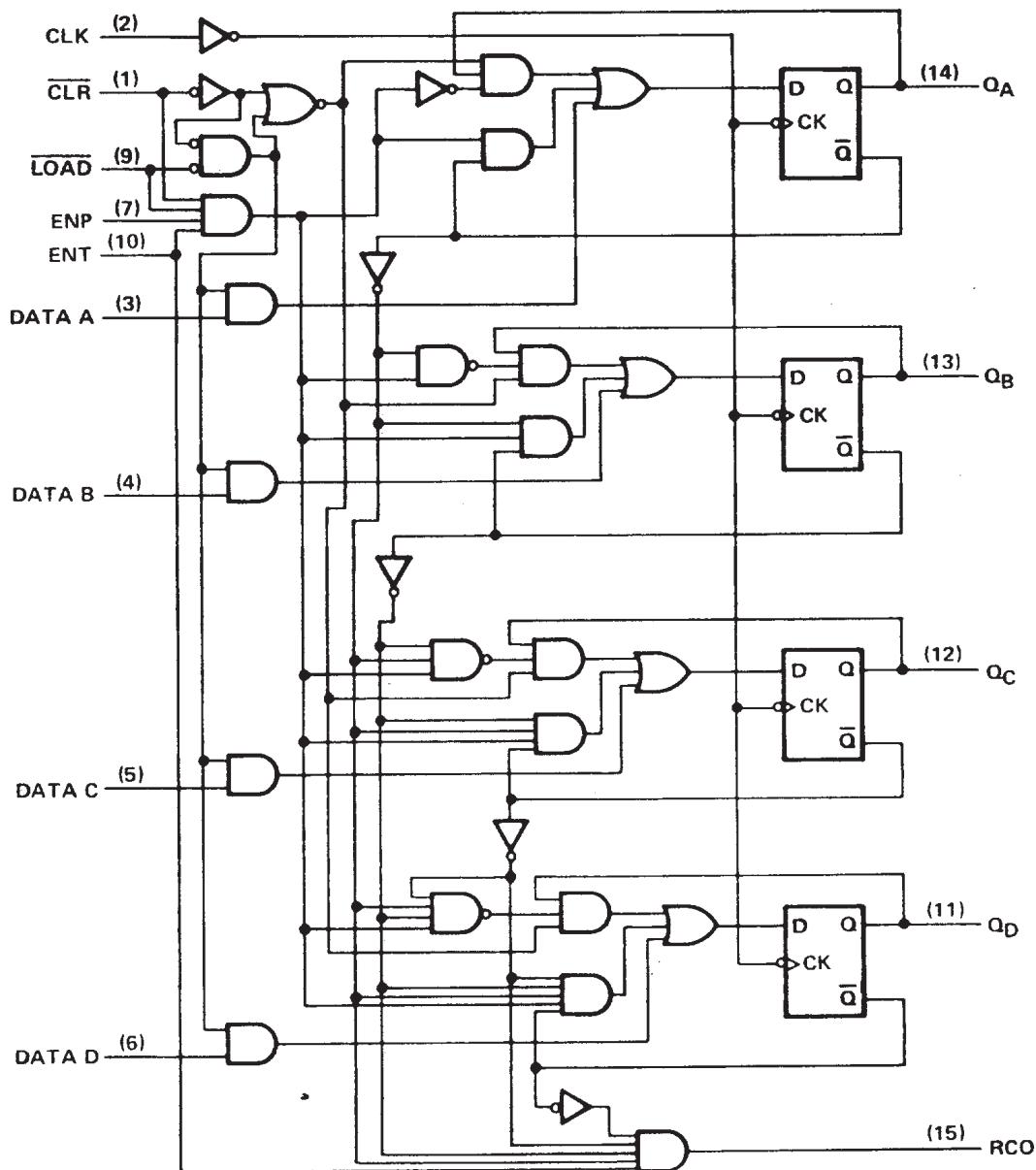
SN54LS161A, SN54LS163A, SN74LS161A, SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic diagram (positive logic)

SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



Pin numbers shown are for D, J, N, and W packages.

SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

- 3-State Outputs Interface Directly With System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:
 - Parallel Load
 - Do Nothing (Hold)
- For Application as Bus Buffer Registers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

| TYPE | TYPICAL PROPAGATION DELAY TIME | MAXIMUM CLOCK FREQUENCY |
|---------|--------------------------------|-------------------------|
| '173 | 23 ns | 35 MHz |
| 'LS173A | 18 ns | 50 MHz |

description

The '173 and 'LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable (\bar{G}_1 , \bar{G}_2) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74173 and SN74LS173A are characterized for operation from 0°C to 70°C .



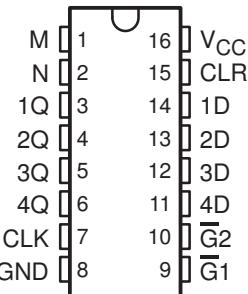
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

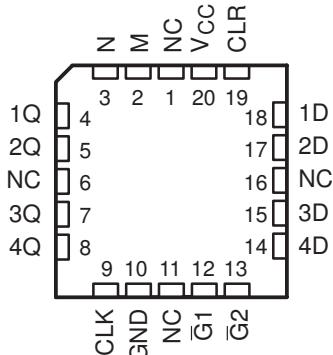


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SN54173, SN54LS173A . . . J OR W PACKAGE
SN74173 . . . N PACKAGE
SN74LS173A . . . D OR N PACKAGE
(TOP VIEW)



SN54LS173A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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**SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS**

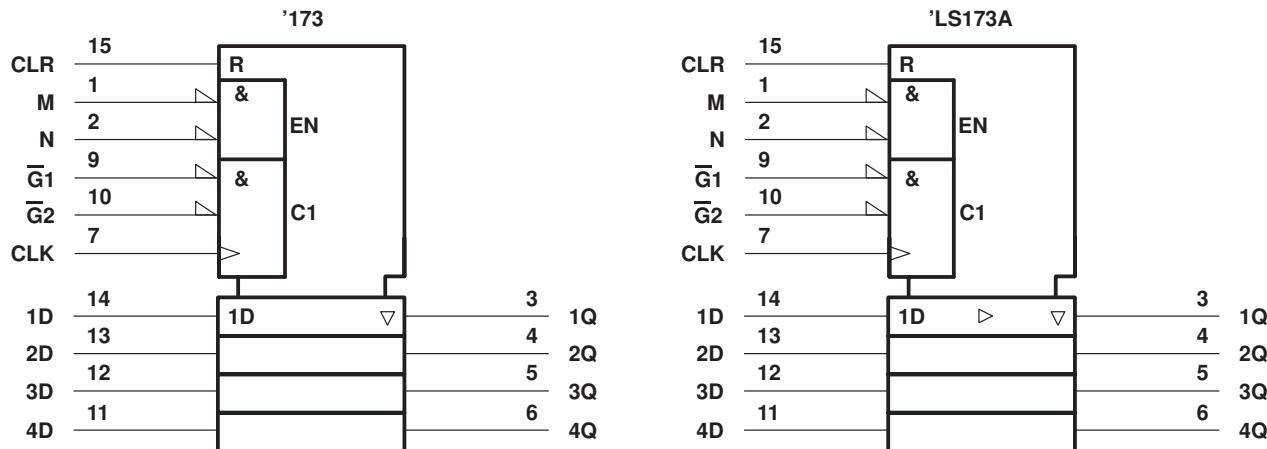
SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

FUNCTION TABLE

| | | INPUTS | | | OUTPUT Q |
|-----|-----|-------------|-------------|-----------|-------------|
| CLR | CLK | DATA ENABLE | | DATA D | |
| | | \bar{G}_1 | \bar{G}_2 | | |
| H | X | X | X | X | L |
| L | L | X | X | X | Q_0 |
| L | ↑ | H | X | X | Q_0 |
| L | ↑ | X | H | X | Q_0 |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

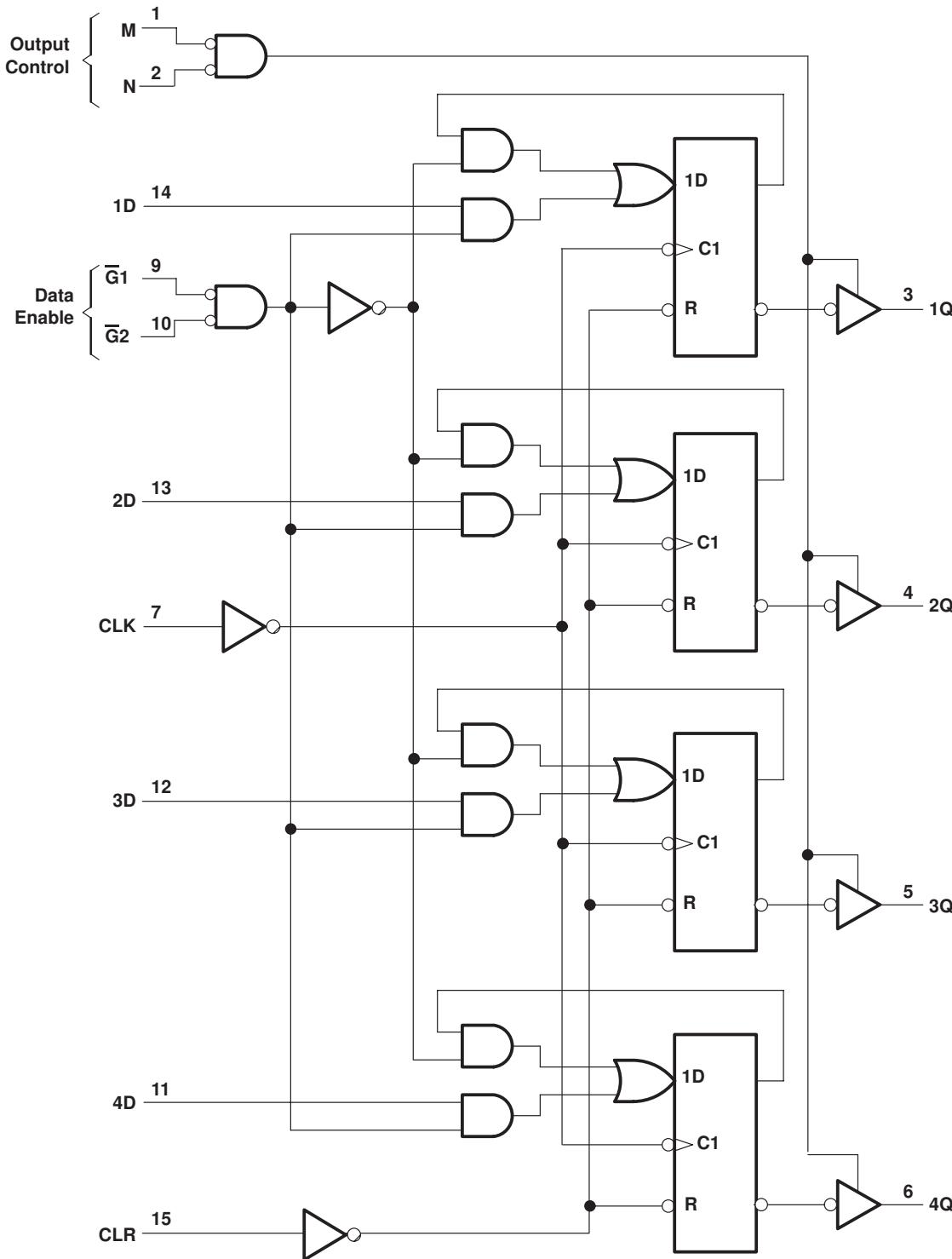
When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

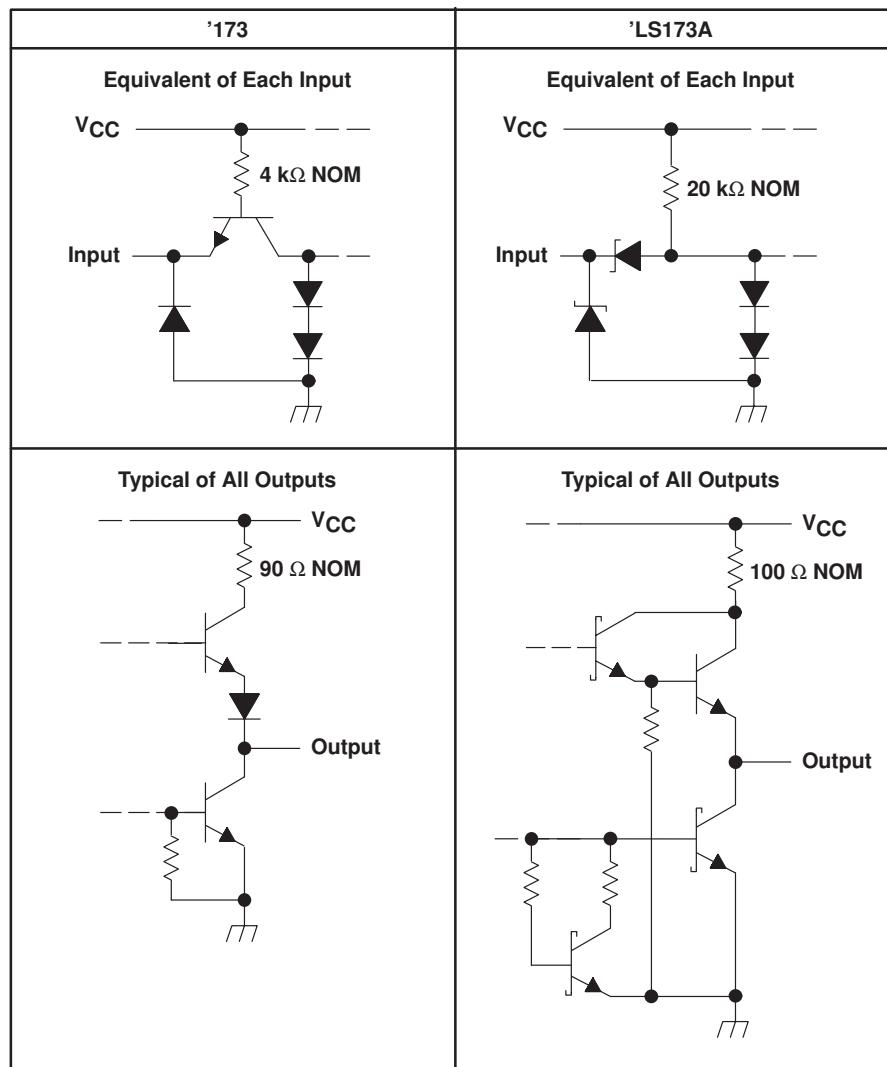
SN54173, SN54LS173A, SN74173, SN74LS173A

4-BIT D-TYPE REGISTERS

WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|------------------------------------------------------------------------|-----------------|
| Supply voltage, V_{CC} (see Note 1) | -0.5 V to 7 V |
| Input voltage: '173 | -0.5 V to 5.5 V |
| 'LS173A | -0.5 V to 7 V |
| Off-state output voltage | -0.5 V to 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 113°C/W |
| N package | 78°C/W |
| Storage temperature range, T_{STG} | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

DM74LS181 4-Bit Arithmetic Logic Unit

General Description

The DM74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

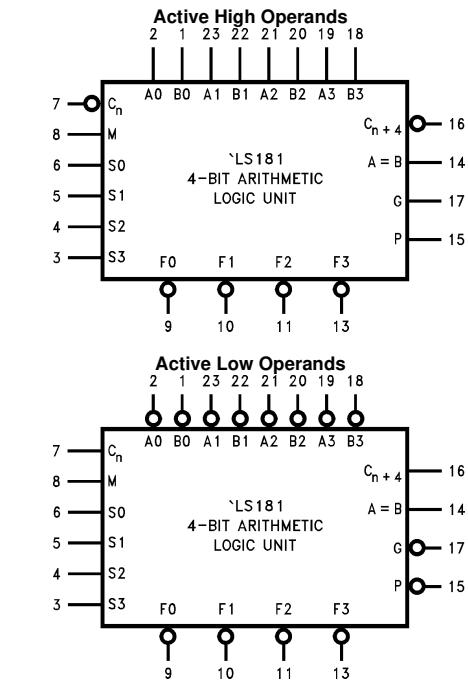
Features

- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
- Full lookahead for high speed arithmetic operation on long words

Ordering Code:

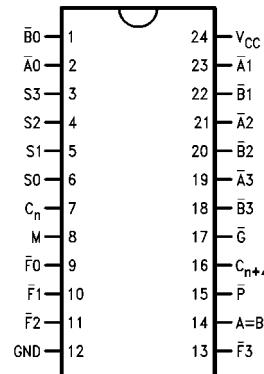
| Order Number | Package Number | Package Description |
|--------------|----------------|-----------------------------------------------------------------------|
| DM74LS181N | N24A | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide |

Logic Symbols



V_{CC} = Pin 24
GND = Pin 12

Connection Diagram



Pin Descriptions

| Pin Names | Description |
|------------------|-------------------------------------|
| Ā0-Ā3 | Operand Inputs (Active LOW) |
| B̄0-B̄3 | Operand Inputs (Active LOW) |
| S0-S3 | Function Select Inputs |
| M | Mode Control Input |
| C _n | Carry Input |
| F̄0-F̄3 | Function Outputs (Active LOW) |
| A=B | Comparator Output |
| G | Carry Generate Output (Active LOW) |
| P | Carry Propagate Output (Active LOW) |
| C _{n+4} | Carry Output |

Functional Description

The DM74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals \bar{P} (Carry Propagate) and \bar{G} (Carry Generate). In the ADD mode, \bar{P} indicates that \bar{F} is 15 or more, while \bar{G} indicates that \bar{F} is 16 or more. In the SUBTRACT mode, \bar{P} indicates that \bar{F} is zero or less, while \bar{G} indicates that \bar{F} is less than zero. \bar{P} and \bar{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four

DM74LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The $A = B$ output from the device goes HIGH when all four \bar{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The $A = B$ output is open-collector and can be wired-AND with other $A = B$ outputs to give a comparison for more than four bits. The $A = B$ signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

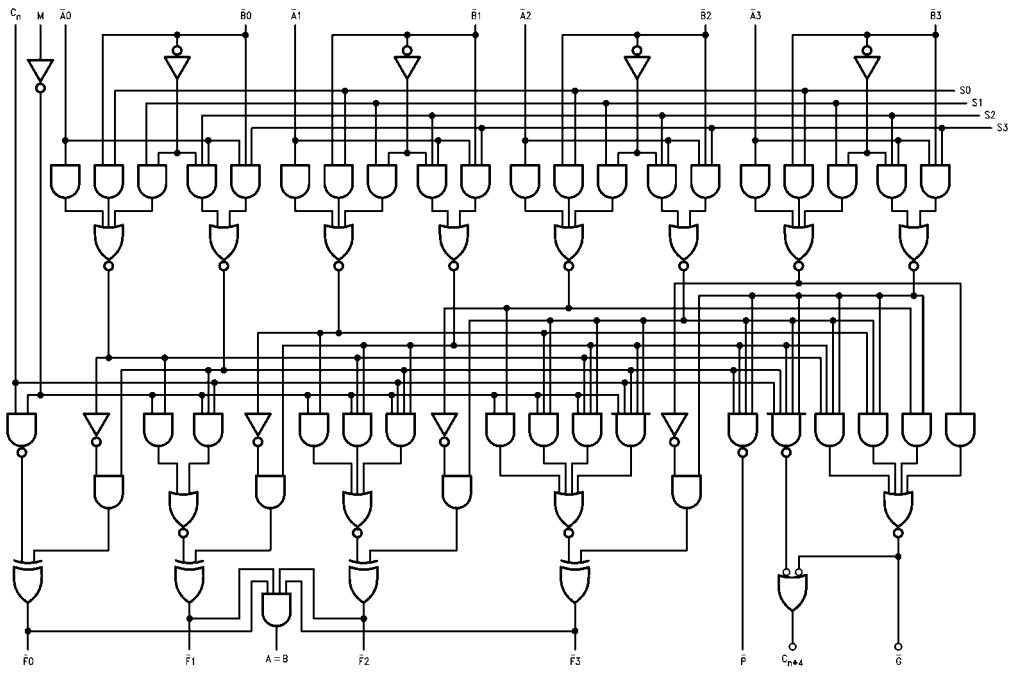
The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

| Mode Select Inputs | | | | Active LOW Operands & F_n Outputs | | Active HIGH Operands & F_n Outputs | |
|-----------------------|----|----|----|----------------------------------------|-------------------------------------------------|-----------------------------------------|-------------------------------------------------|
| S3 | S2 | S1 | S0 | Logic (M = H) | Arithmetic (Note 2) (M = L) ($C_n = L$) | Logic (M = H) | Arithmetic (Note 2) (M = L) ($C_n = H$) |
| L | L | L | L | \bar{A} | A minus 1 | \bar{A} | A |
| L | L | L | H | \bar{AB} | AB minus 1 | $\bar{A} + \bar{B}$ | $A + B$ |
| L | L | H | L | $\bar{A} + \bar{B}$ | \bar{AB} minus 1 | $\bar{A}B$ | $A + \bar{B}$ |
| L | L | H | H | Logic 1 | minus 1 | Logic 0 | minus 1 |
| L | H | L | L | $\bar{A} + \bar{B}$ | A plus ($A + \bar{B}$) | \bar{AB} | $A + \bar{AB}$ |
| L | H | L | H | \bar{B} | AB plus ($A + \bar{B}$) | \bar{B} | $(A + B) + \bar{AB}$ |
| L | H | H | L | $\bar{A} \oplus \bar{B}$ | A minus B minus 1 | $\bar{A} \oplus B$ | A minus B minus 1 |
| L | H | H | H | $A + \bar{B}$ | $A + \bar{B}$ | \bar{AB} | AB minus 1 |
| H | L | L | L | $\bar{A}B$ | A plus ($A + B$) | $\bar{A} + B$ | $A + AB$ |
| H | L | L | H | $A \oplus B$ | A plus B | $\bar{A} \oplus \bar{B}$ | A plus B |
| H | L | H | L | B | \bar{AB} plus ($A + B$) | B | $(A + \bar{B}) + AB$ |
| H | L | H | H | $A + B$ | $A + B$ | AB | AB minus 1 |
| H | H | L | L | Logic 0 | A plus A (Note 1) | Logic 1 | A plus A (Note 1) |
| H | H | L | H | \bar{AB} | AB plus A | $A + \bar{B}$ | $(A + B) + A$ |
| H | H | H | L | AB | \bar{AB} minus A | $A + B$ | $(A + \bar{B}) + A$ |
| H | H | H | H | A | A | A | A minus 1 |

Note 1: Each bit is shifted to the next most significant position.

Note 2: Arithmetic operations expressed in 2s complement notation.

Logic Diagram

Absolute Maximum Ratings (Note 3)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-----------------|--------------------------------|------|-----|------|-------|
| V _{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} | HIGH Level Input Voltage | 2 | | | V |
| V _{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I _{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I _{OL} | LOW Level Output Current | | | 8 | mA |
| T _A | Free Air Operating Temperature | 0 | | 70 | °C |

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 4) | Max | Units |
|-----------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------|------------------------------|---------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | HIGH Level Output Voltage | V _{CC} = Min, I _{OH} = Max, V _{IL} = Max | 2.7 | | | V |
| V _{OL} | LOW Level Output Voltage | V _{CC} = Min, I _{OL} = Max, V _{IH} = Min | | 0.35 | 0.5 | V |
| | | I _{OL} = 4 mA, V _{CC} = Min | | 0.25 | 0.4 | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 7V | M input A _n , B _n S _n C _n | | 0.1 0.3 0.4 0.5 | mA |
| I _{IH} | HIGH Level Input Current | V _{CC} = Max, V _I = 2.7V | M input A _n , B _n S _n C _n | | 20 60 80 100 | μA |
| I _{IL} | LOW Level Input Current | V _{CC} = Max, V _I = 0.4V | M input A _n , B _n S _n C _n | | -0.4 -1.2 -1.6 -2.0 | mA |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 5) | | -20 | | -100 mA |
| I _{CC} | Supply Current | V _{CC} = Max, B _n , C _n = GND S _n , M, A _n = 4.5V | | | 37 | mA |

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

SNx4LS245 Octal Bus Transceivers With 3-State Outputs

1 Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

2 Applications

- Building Automation
- Electronic Point of Sale
- Factory Automation and Control
- Test and Measurement

3 Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

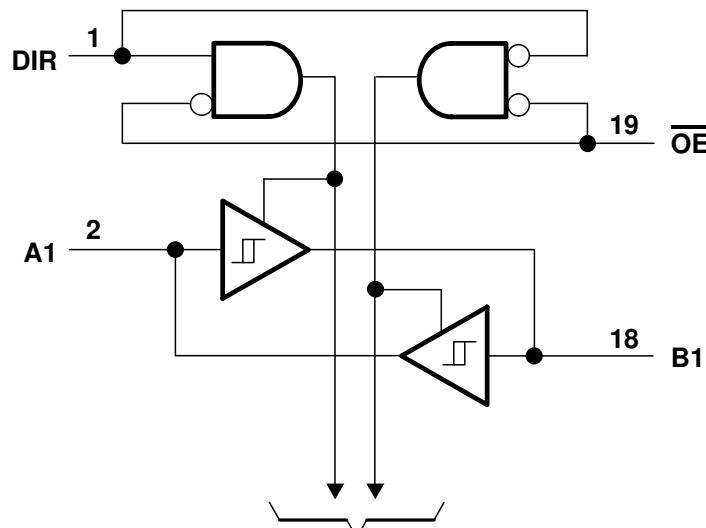
The SNx4LS245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the device so that the buses are effectively isolated.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------|
| SN54LS245J | CDIP (20) | 24.20 mm × 6.92 mm |
| SN54LS245W | CFP (20) | 7.02 mm × 13.72 mm |
| SN54LS245FK | LCCC (20) | 8.89 mm × 8.89 mm |
| SN74LS245DB | SSOP (20) | 7.20 mm × 5.30 mm |
| SN74LS245DW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74LS245N | PDIP (20) | 24.33 mm × 6.35 mm |
| SN74LS245NS | SO (20) | 12.60 mm × 5.30 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



To Seven Other Channels

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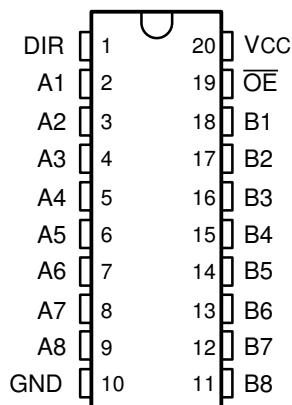
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

5 Device Comparison Table

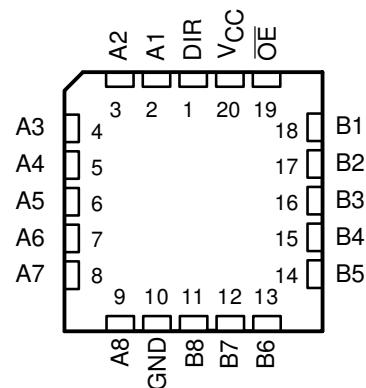
| TYPE | I_{OL} (SINK CURRENT) | I_{OH} (SOURCE CURRENT) |
|-----------|----------------------------|------------------------------|
| SN54LS245 | 12 mA | -12 mA |
| SN74LS245 | 24 mA | -15 mA |

6 Pin Configuration and Functions

J, W, DB, DW, N, or NS Package
20-Pin CDIP, CFP, SSOP, SOIC, PDIP, or SO
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|----------------------------------------------------------------------------------------------------|
| NO. | NAME | | |
| 1 | DIR | I | Controls signal direction; Low = Bx to Ax, High = Ax to Bx |
| 2 | A1 | I/O | Channel 1, A side |
| 3 | A2 | I/O | Channel 2, A side |
| 4 | A3 | I/O | Channel 3, A side |
| 5 | A4 | I/O | Channel 4, A side |
| 6 | A5 | I/O | Channel 5, A side |
| 7 | A6 | I/O | Channel 6, A side |
| 8 | A7 | I/O | Channel 7, A side |
| 9 | A8 | I/O | Channel 8, A side |
| 10 | GND | — | Ground |
| 11 | B8 | O/I | Channel 8, B side |
| 12 | B7 | O/I | Channel 7, B side |
| 13 | B6 | O/I | Channel 6, B side |
| 14 | B5 | O/I | Channel 5, B side |
| 15 | B4 | O/I | Channel 4, B side |
| 16 | B3 | O/I | Channel 3, B side |
| 17 | B2 | O/I | Channel 2, B side |
| 18 | B1 | O/I | Channel 1, B side |
| 19 | \overline{OE} | I | Active low output enable; Low = all channels active, High = all channels disabled (high impedance) |
| 20 | V _{CC} | — | Power supply |

SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

SDLS090 – OCTOBER 1976 – REVISED MARCH 1988

- Contains Eight Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators

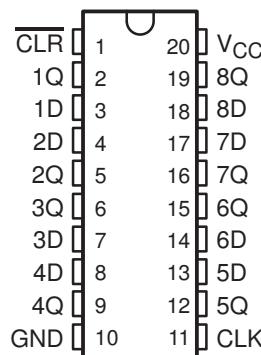
description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

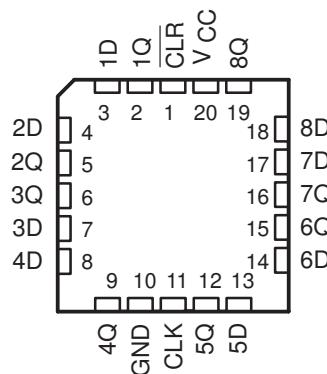
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

SN54273, SN74LS273 . . . J OR W PACKAGE
SN74273 . . . N PACKAGE
SN74LS273 . . . DW OR N PACKAGE
(TOP VIEW)



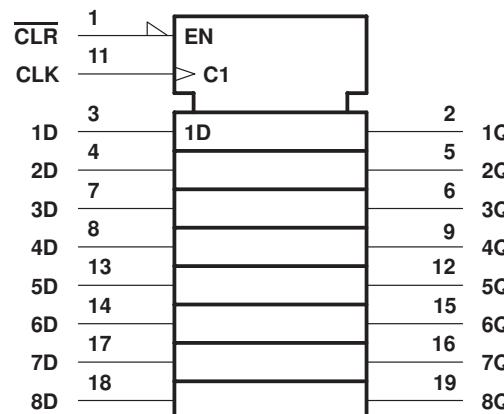
SN54LS273 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT Q |
|--------|-------|---|----------------|
| CLEAR | CLOCK | D | |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q ₀ |

logic symbol†



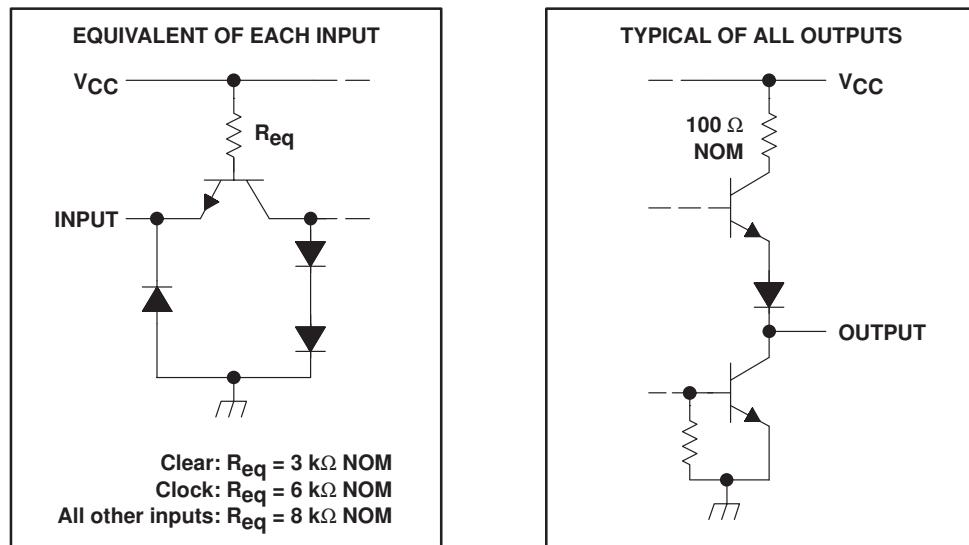
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, N, and W packages.

SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

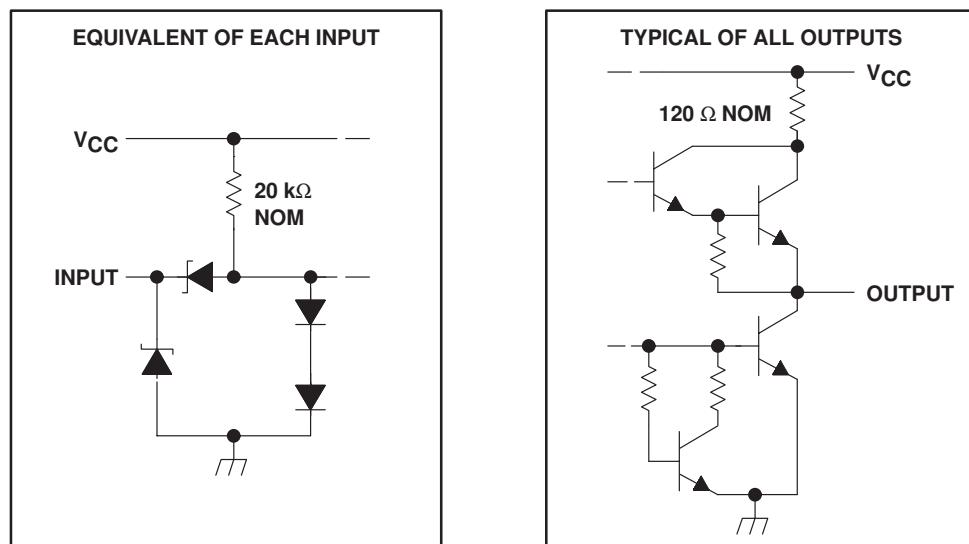
SDLS090 – OCTOBER 1976 – REVISED MARCH 1988

schematics of inputs and outputs

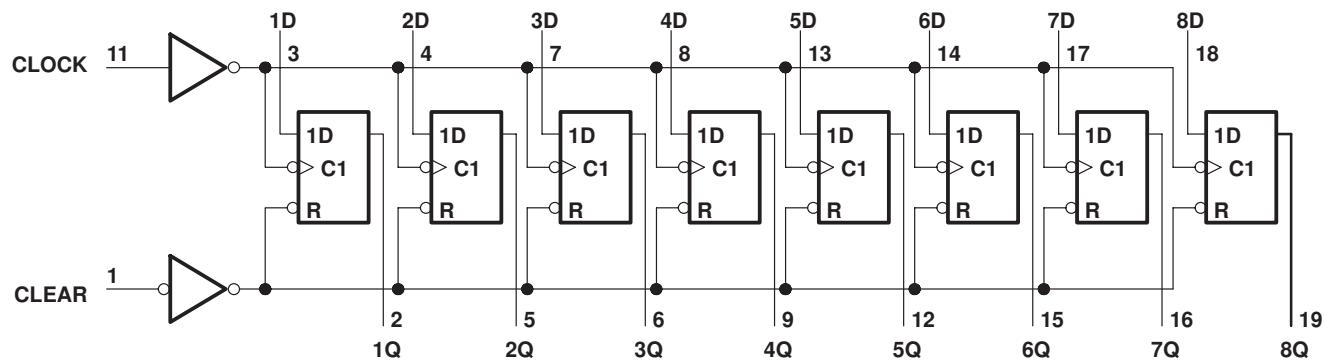
'273



'LS273



logic diagram (positive logic)



Pin numbers shown are for the DW, J, N, and W packages.

- Full-Carry Look-Ahead Across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

TYPICAL ADD TIMES

| TYPE | TWO 8-BIT WORDS | TWO 16-BIT WORDS | TYPICAL POWER DISSIPATION PER ADDER |
|--------|-----------------------|------------------------|-------------------------------------------|
| | | | |
| '283 | 23ns | 43ns | 310 mW |
| 'LS283 | 25ns | 45ns | 95 mW |
| 'S283 | 15ns | 30ns | 510 mW |

description

The '283 and 'LS283 adders are electrically and functionally identical to the '83A and 'LS83A, respectively; only the arrangement of the terminals has been changed. The 'S283 high performance versions are also functionally identical.

These improved full adders perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds, typically, for the '283 and 'LS283, and 7.5 nanoseconds for the 'S283. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full temperature range of -55°C to 125°C . Series 74, Series 74LS, and Series 74S circuits are characterized for 0°C to 70°C operation.

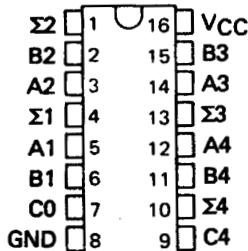
SN54283, SN54LS283 . . . J OR W PACKAGE

SN54S283 . . . J PACKAGE

SN74283 . . . N PACKAGE

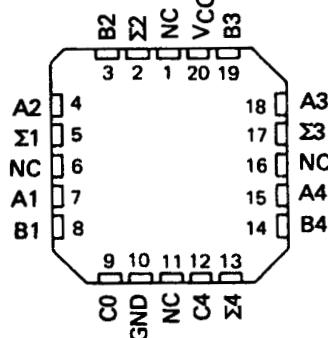
SN74LS283, SN74S283 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS283, SN54S283 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

| INPUT | | | | OUTPUT | | | | | | | |
|-------|----|----|----|----------------|----|----|----|----------------|----|----|----|
| | | | | WHEN CO = L | | | | WHEN CO = H | | | |
| A1 | B1 | A2 | B2 | Σ1 | Σ2 | C2 | C4 | Σ1 | Σ2 | C2 | C4 |
| | | | | A3 | B3 | E3 | E4 | A3 | B3 | E3 | E4 |
| L | L | L | L | L | L | L | L | H | L | H | L |
| H | L | L | L | H | L | L | L | L | H | L | L |
| L | H | L | L | H | L | L | L | L | H | H | L |
| H | H | L | L | L | H | L | L | H | H | H | L |
| L | L | H | L | L | H | L | H | L | H | H | H |
| H | L | H | L | L | H | H | L | L | L | L | H |
| L | H | H | L | H | H | L | H | L | L | L | H |
| H | H | H | L | L | L | H | L | H | L | H | H |
| L | L | L | H | L | H | H | L | H | H | L | H |
| H | L | L | H | H | H | H | L | L | L | L | H |
| L | H | L | H | H | H | L | H | H | L | H | H |
| H | H | L | H | L | L | L | H | H | L | H | H |
| L | L | H | H | H | H | L | H | H | L | H | H |
| H | L | H | H | H | H | L | H | H | L | H | H |
| L | H | H | H | H | H | H | L | H | H | H | H |
| H | H | H | H | H | H | H | H | H | H | H | H |

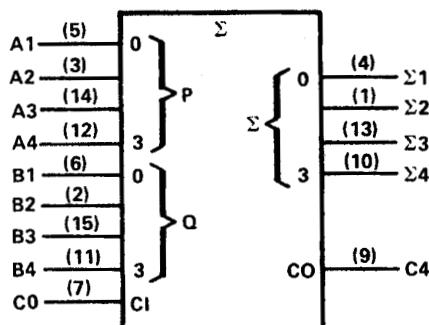
H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and CO are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ_3 , Σ_4 , and C4.

**SN54283, SN54LS283, SN54S283,
SN74283, SN74LS283, SN74S283
4-BIT BINARY FULL ADDERS WITH FAST CARRY**

SDLS095A – OCTOBER 1976 – REVISED MARCH 1988

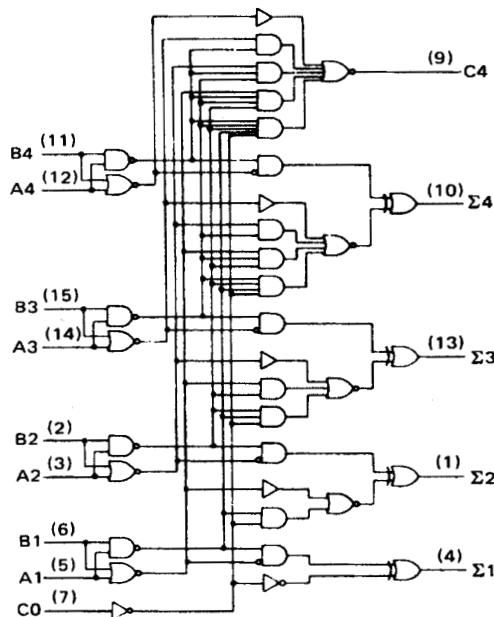
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

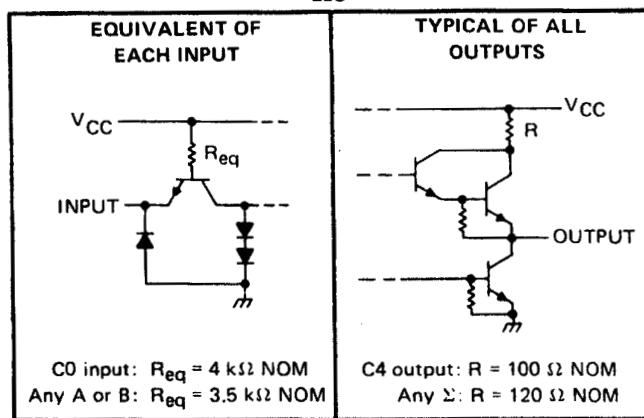
logic diagram (positive logic)



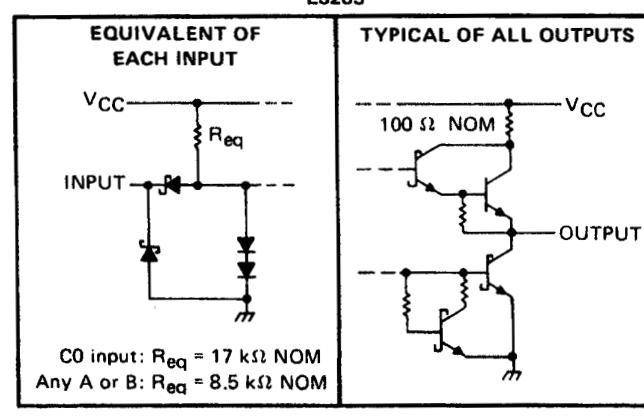
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

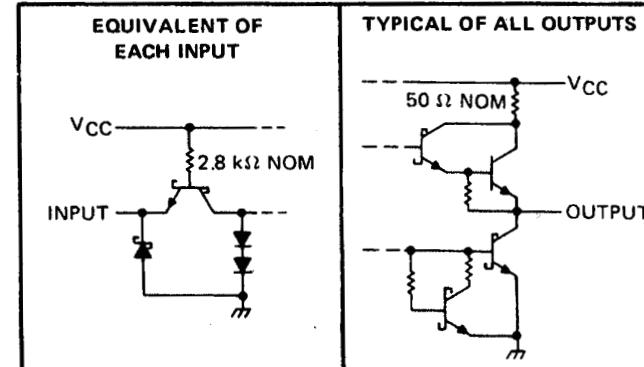
'283



'LS283



'S283



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--------------------------------------------------------------------|----------------|
| Supply voltage, V _{CC} (see Note 1) | 7V |
| Input voltage: '283, 'S283 | 5.5V |
| 'LS283 | 7V |
| Interemitter voltage (see Note 2) | 5.5V |
| Operating free-air temperature range: SN54283, SN54LS283, SN54S283 | -55°C to 125°C |
| SN74283, SN74LS283, SN74S283 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '283 and 'S283 only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.



CMOS Static RAM 64K (8K x 8-Bit)

IDT7164S
IDT7164L

Features

- ◆ High-speed address/chip select access time
 - Military: 20/25/35/45/55/70/85/100ns (max.)
 - Industrial: 20/25ns (max.)
 - Commercial: 20/25ns (max.)
- ◆ Low power consumption
- ◆ Battery backup operation – 2V data retention voltage (L Version only)
- ◆ Produced with advanced CMOS high-performance technology
- ◆ Inputs and outputs directly TTL-compatible
- ◆ Three-state outputs
- ◆ Available in 28-pin DIP, CERDIP and SOJ
- ◆ Military product compliant to MIL-STD-883, Class B
- ◆ Green parts available, see ordering information

Description

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using high-performance, high-reliability CMOS technology.

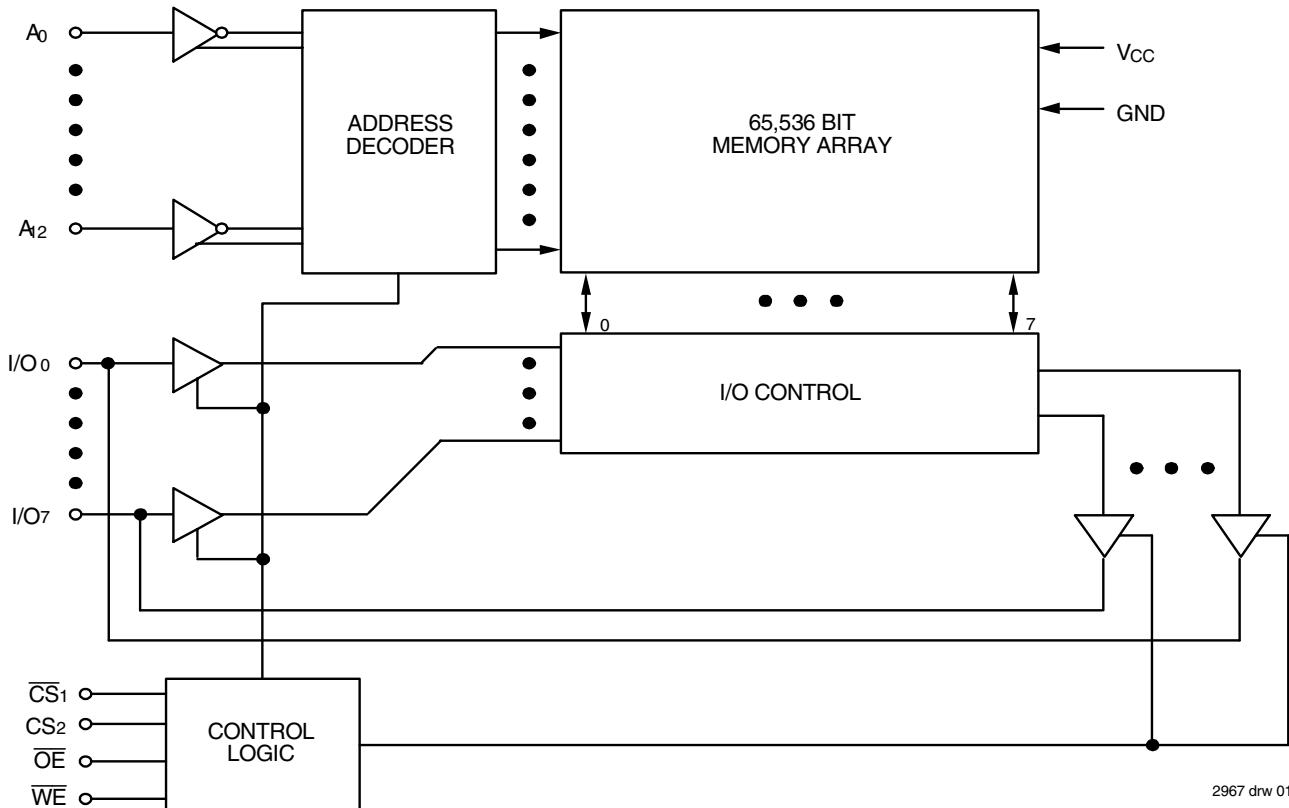
Address access times as fast as 20ns are available and the circuit offers a reduced power standby mode. When \overline{CS}_1 goes HIGH or CS_2 goes LOW, the circuit will automatically go to, and remain in, a low-power standby mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil CERDIP, a 28-pin 600 mil CERDIP, 300mil Plastic DIP and 300mil SOJ

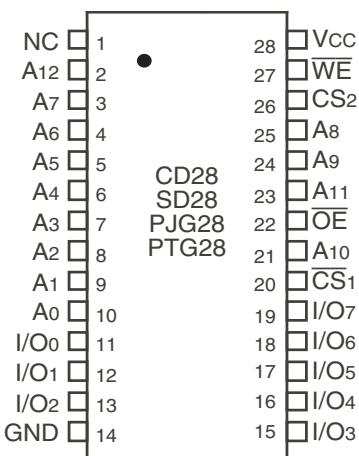
Military grade product is manufactured in compliance with MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



DECEMBER 2016

Pin Configurations



2967 drw 02

**DIP/SOJ
Top View**

Pin Descriptions

| Name | Description |
|-------------|-------------------|
| A0 - A12 | Address |
| I/O0 - I/O7 | Data Input/Output |
| CS1 | Chip Select |
| CS2 | Chip Select |
| WE | Write Enable |
| OE | Output Enable |
| GND | Ground |
| Vcc | Power |

2967 tbl 01

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|-----------|------|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input HIGH Voltage | 2.2 | — | Vcc + 0.5 | V |
| V _{IL} | Input LOW Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

2967 tbl 05

NOTE:

1. V_{IL} (min.) = -1.5V for pulse width less than 10ns, once per cycle.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Com'l. | Mil. | Unit |
|----------------------------------|--------------------------------------|--------------|--------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| T _A | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | 50 | mA |

2967 tbl 02

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{cc} + 0.5V.

Truth Table^(1,2,3)

| WE | CS1 | CS2 | OE | I/O | Function |
|----|-----------------|------------------------------------|----|---------------------|----------------------------|
| X | H | X | X | High-Z | Deselected - Standby (lsb) |
| X | X | L | X | High-Z | Deselected - Standby (lsb) |
| X | V _{HC} | V _{HC} or V _{LC} | X | High-Z | Deselected - Standby (lsb) |
| X | X | V _{LC} | X | High-Z | Deselected - Standby (lsb) |
| H | L | H | H | High-Z | Output Disabled |
| H | L | H | L | DATA _{OUT} | Read Data |
| L | L | H | X | DATA _{IN} | Write Data |

2967 tbl 03

NOTES:

1. CS2 will power-down CS1, but CS1 will not power-down CS2.
2. H = V_{IH}, L = V_{IL}, X = don't care.
3. V_{LC} = 0.2V, V_{HC} = V_{cc} - 0.2V

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | V _{cc} |
|------------|-----------------|-----|-----------------|
| Military | -55°C to +125°C | 0V | 5V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5V ± 10% |

2967 tbl 04

Part Number: SA56-11SRWA Super Bright Red

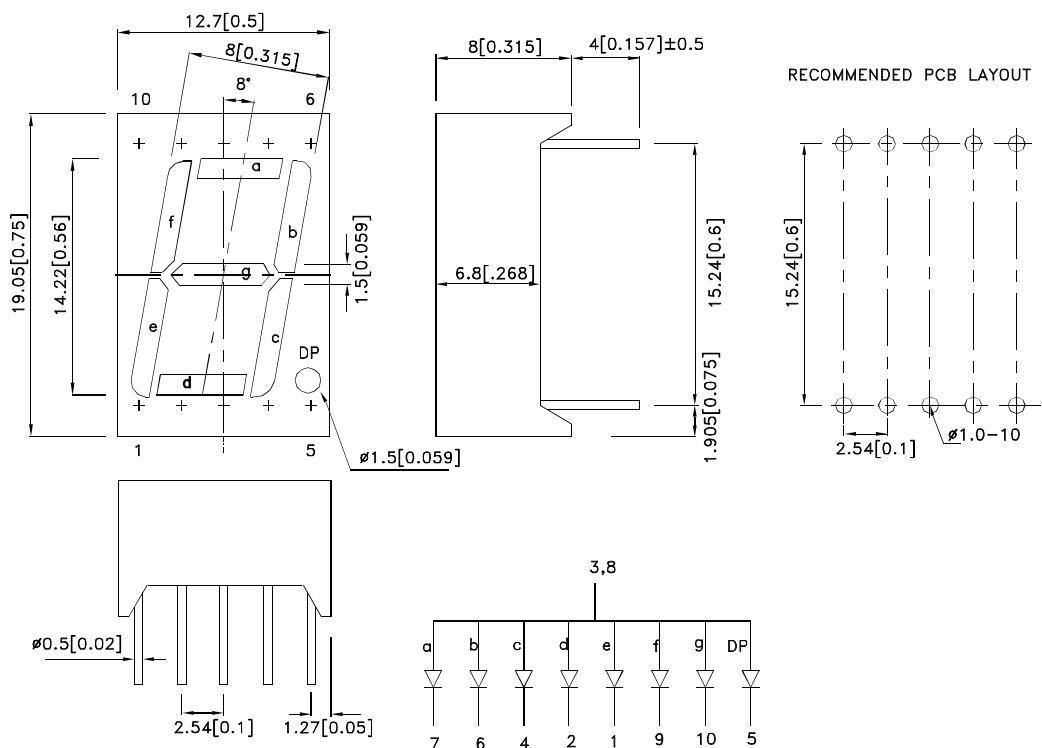
Features

- 0.56 inch digit height.
- Low current operation.
- Excellent character appearance.
- Easy mounting on P.C. boards or sockets.
- Mechanically rugged.
- Standard : gray face, white segment.
- RoHS compliant.

Description

The Super Bright Red source color devices are made with Gallium Aluminum Arsenide Red Light Emitting Diode.

Package Dimensions& Internal Circuit Diagram



Notes:

1. All dimensions are in millimeters (inches), Tolerance is $\pm 0.25(0.01")$ unless otherwise noted.
2. The specifications, characteristics and technical data described in the datasheet are subject to change without prior notice.



Kingbright

Selection Guide

| Part No. | Dice | Lens Type | I _V (ucd) [1] @ 10mA | | Description |
|-------------|---------------------------|----------------|---------------------------------|-------|---------------------------------|
| | | | Min. | Typ. | |
| SA56-11SRWA | Super Bright Red (GaAlAs) | White Diffused | 14000 | 34000 | Common Anode, Rt. Hand Decimal. |

Note:

1. Luminous intensity/ luminous Flux: +/-15%.

Electrical / Optical Characteristics at TA=25°C

| Symbol | Parameter | Device | Typ. | Max. | Units | Test Conditions |
|--------------------|--------------------------|------------------|------|------|-------|---------------------------|
| λ_{peak} | Peak Wavelength | Super Bright Red | 660 | | nm | I _F =20mA |
| λ_D [1] | Dominant Wavelength | Super Bright Red | 640 | | nm | I _F =20mA |
| $\Delta\lambda/2$ | Spectral Line Half-width | Super Bright Red | 20 | | nm | I _F =20mA |
| C | Capacitance | Super Bright Red | 45 | | pF | V _F =0V;f=1MHz |
| V _F [2] | Forward Voltage | Super Bright Red | 1.85 | 2.5 | V | I _F =20mA |
| I _R | Reverse Current | Super Bright Red | | 10 | uA | V _R =5V |

Notes:

1. Wavelength: +/-1nm.
2. Forward Voltage: +/-0.1V.

Absolute Maximum Ratings at TA=25°C

| Parameter | Super Bright Red | Units |
|---------------------------------|-----------------------|-------|
| Power dissipation | 75 | mW |
| DC Forward Current | 30 | mA |
| Peak Forward Current [1] | 155 | mA |
| Reverse Voltage | 5 | V |
| Operating / Storage Temperature | -40°C To +85°C | |
| Lead Solder Temperature[2] | 260°C For 3-5 Seconds | |

Notes:

1. 1/10 Duty Cycle, 0.1ms Pulse Width.
2. 2mm below package base.

Features

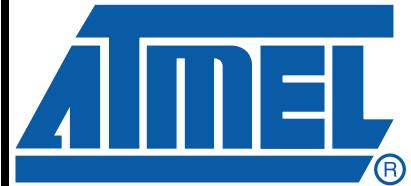
- **Fast Read Access Time – 150 ns**
- **Automatic Page Write Operation**
 - Internal Address and Data Latches for 64 Bytes
- **Fast Write Cycle Times**
 - Page Write Cycle Time: 10 ms Maximum (Standard)
 - 2 ms Maximum (Option – Ref. AT28HC64BF Datasheet)
 - 1 to 64-byte Page Write Operation
- **Low Power Dissipation**
 - 40 mA Active Current
 - 100 µA CMOS Standby Current
- **Hardware and Software Data Protection**
- **DATA Polling and Toggle Bit for End of Write Detection**
- **High Reliability CMOS Technology**
 - Endurance: 100,000 Cycles
 - Data Retention: 10 Years
- **Single 5V ±10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-wide Pinout**
- **Industrial Temperature Ranges**
- **Green (Pb/Halide-free) Packaging Option Only**

1. Description

The AT28C64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.



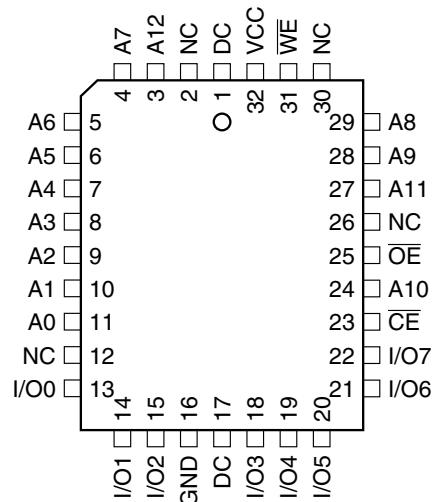
64K (8K x 8) Parallel EEPROM with Page Write and Software Data Protection

AT28C64B

2. Pin Configurations

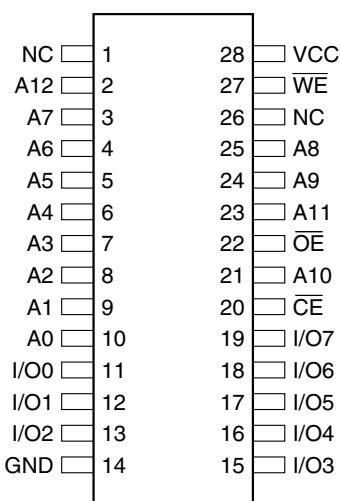
| Pin Name | Function |
|-----------------|---------------------|
| A0 - A12 | Addresses |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| I/O0 - I/O7 | Data Inputs/Outputs |
| NC | No Connect |
| DC | Don't Connect |

2.2 32-lead PLCC Top View

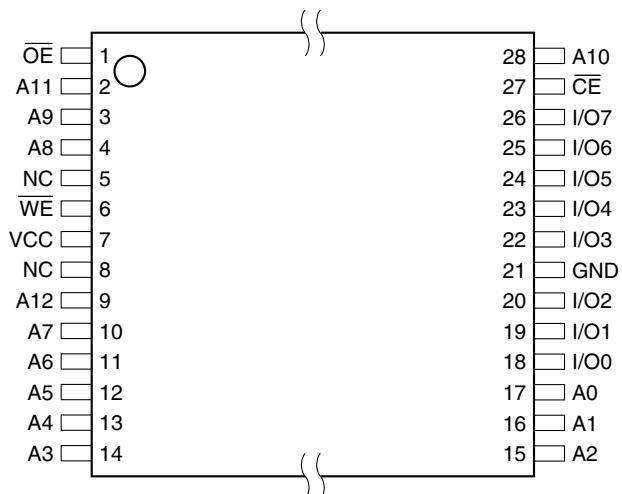


Note: PLCC package pins 1 and 17 are Don't Connect.

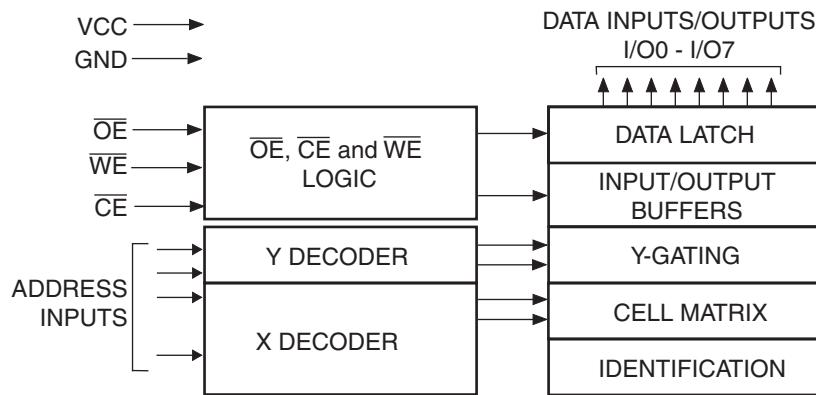
2.1 28-lead PDIP, 28-lead SOIC Top View



2.3 28-lead TSOP Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT28C64B is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either \overline{CE} or \overline{OE} is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

4.2 Byte Write

A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the AT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within $150\ \mu s$ (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each \overline{WE} high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.4 DATA Polling

The AT28C64B features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at any time during the write cycle.

4.5 Toggle Bit

In addition to DATA Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

4.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel® has incorporated both hardware and software features that will protect the memory against inadvertent writes.

4.6.1 Hardware Data Protection

Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8 V (typical), the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8 V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of \overline{OE} low, \overline{CE} high, or \overline{WE} high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a write cycle.

4.6.2 Software Data Protection

A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (see “Software Data Protection Algorithms” on [page 10](#)). After writing the 3-byte command sequence and waiting t_{WC} , the entire AT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC} , read operations will effectively be polling operations.

4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5 V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

5. DC and AC Operating Range

| | |
|------------------------------|--------------------|
| | AT28C64B-15 |
| Operating Temperature (Case) | -40°C - 85°C |
| V _{CC} Power Supply | 5V ±10% |

6. Operating Modes

| Mode | CE | OE | WE | I/O |
|-----------------------|-----------------|-------------------------------|-----------------|------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} |
| Write ⁽²⁾ | V _{IL} | V _{IH} | V _{IL} | D _{IN} |
| Standby/Write Inhibit | V _{IH} | X ⁽¹⁾ | X | High Z |
| Write Inhibit | X | X | V _{IH} | |
| Write Inhibit | X | V _{IL} | X | |
| Output Disable | X | V _{IH} | X | High Z |
| Chip Erase | V _{IL} | V _H ⁽³⁾ | V _{IL} | High Z |

Notes: 1. X can be V_{IL} or V_{IH}.

2. See "AC Write Waveforms" on page 8.

3. V_H = 12.0V ±0.5V.

7. Absolute Maximum Ratings*

| | |
|------------------------------------------------------|---------------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) | |
| with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to V _{CC} + 0.6V |
| Voltage on OE and A9 with Respect to Ground | -0.6V to +13.5V |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

8. DC Characteristics

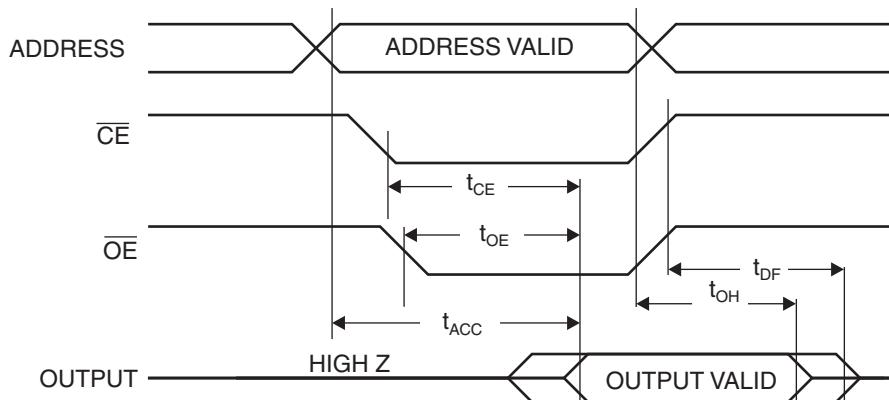
| Symbol | Parameter | Condition | Min | Max | Units |
|------------------|--------------------------------------|-----------------------------------------------------|-----|------|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} + 1V | | 10 | µA |
| I _{LO} | Output Leakage Current | V _{I/O} = 0V to V _{CC} | | 10 | µA |
| I _{SB1} | V _{CC} Standby Current CMOS | CE = V _{CC} - 0.3V to V _{CC} + 1V | | 100 | µA |
| I _{SB2} | V _{CC} Standby Current TTL | CE = 2.0V to V _{CC} + 1V | | 2 | mA |
| I _{CC} | V _{CC} Active Current | f = 5 MHz; I _{OUT} = 0 mA | | 40 | mA |
| V _{IL} | Input Low Voltage | | | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.40 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 µA | 2.4 | | V |



9. AC Read Characteristics

| Symbol | Parameter | AT28C64B-15 | | Units |
|-------------------|-----------------------------------------------------------------------------------------|-------------|-----|-------|
| | | Min | Max | |
| t_{ACC} | Address to Output Delay | | 150 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 150 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 0 | 70 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} to Output Float | 0 | 50 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | ns |

10. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾



- Notes:
1. \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 3. t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5 \text{ pF}$).
 4. This parameter is characterized and is not 100% tested.

SNx4HC595 8-Bit Shift Registers With 3-State Output Registers

1 Features

- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Low Power Consumption: 80 μ A (Maximum) I_{CC}
- t_d = 13 ns (Typical)
- ± 6 -mA Output Drive at 5 V
- Low Input Current: 1 μ A (Maximum)
- Shift Register Has Direct Clear
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Network Switches
- Power Infrastructure
- LED Displays
- Servers

3 Description

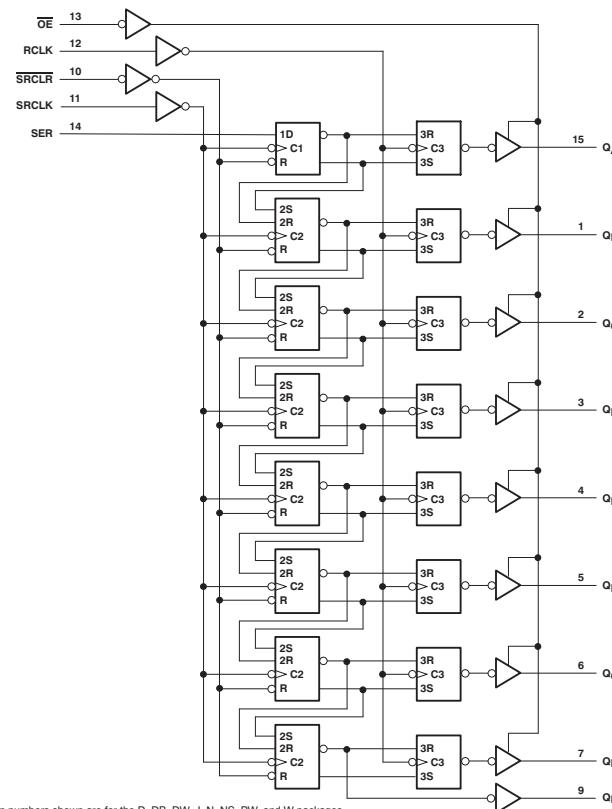
The SNx4HC595 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (\overline{OE}) input is high, the outputs are in the high-impedance state.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SN54HC595 | LCCC (20) | 8.89 mm x 8.89 mm |
| | CDIP (16) | 21.34 mm x 6.92 mm |
| SN74HC595 | PDIP (16) | 19.31 mm x 6.35 mm |
| | SOIC (16) | 9.90 mm x 3.90 mm |
| SN74HC595 | SOIC (16) | 10.30 mm x 7.50 mm |
| | SSOP (16) | 6.20 mm x 5.30 mm |
| | TSSOP (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



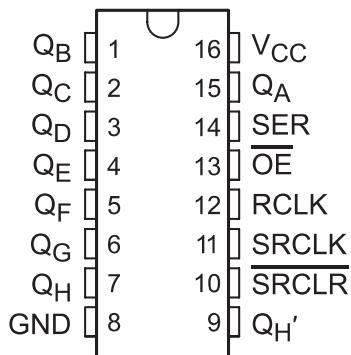
Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.



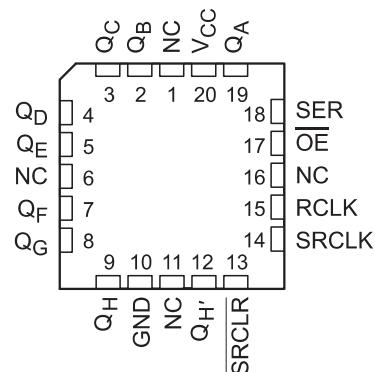
An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

6 Pin Configuration and Functions

D, N, NS, J, DB, or PW Package
16-Pin SOIC, PDIP, SO, CDIP, SSOP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|-----------------|--------------------------------------------------|------|-----|------------------------|
| | SOIC, PDIP, SO, CDIP, SSOP, or TSSOP | LCCC | | |
| GND | 8 | 10 | — | Ground Pin |
| OE | 13 | 17 | I | Output Enable |
| Q _A | 15 | 19 | O | Q _A Output |
| Q _B | 1 | 2 | O | Q _B Output |
| Q _C | 2 | 3 | O | Q _C Output |
| Q _D | 3 | 4 | O | Q _D Output |
| Q _E | 4 | 5 | O | Q _E Output |
| Q _F | 5 | 7 | O | Q _F Output |
| Q _G | 6 | 8 | O | Q _G Output |
| Q _H | 7 | 9 | O | Q _H Output |
| Q _{H'} | 9 | 12 | O | Q _{H'} Output |
| RCLK | 12 | 14 | I | RCLK Input |
| SER | 14 | 18 | I | SER Input |
| SRCLK | 11 | 14 | I | SRCLK Input |
| SRCLR | 10 | 13 | I | SRCLR Input |
| NC | — | 1 | — | No Connection |
| | | 16 | | |
| | | 11 | | |
| | | 16 | | |
| V _{CC} | — | 20 | — | Power Pin |

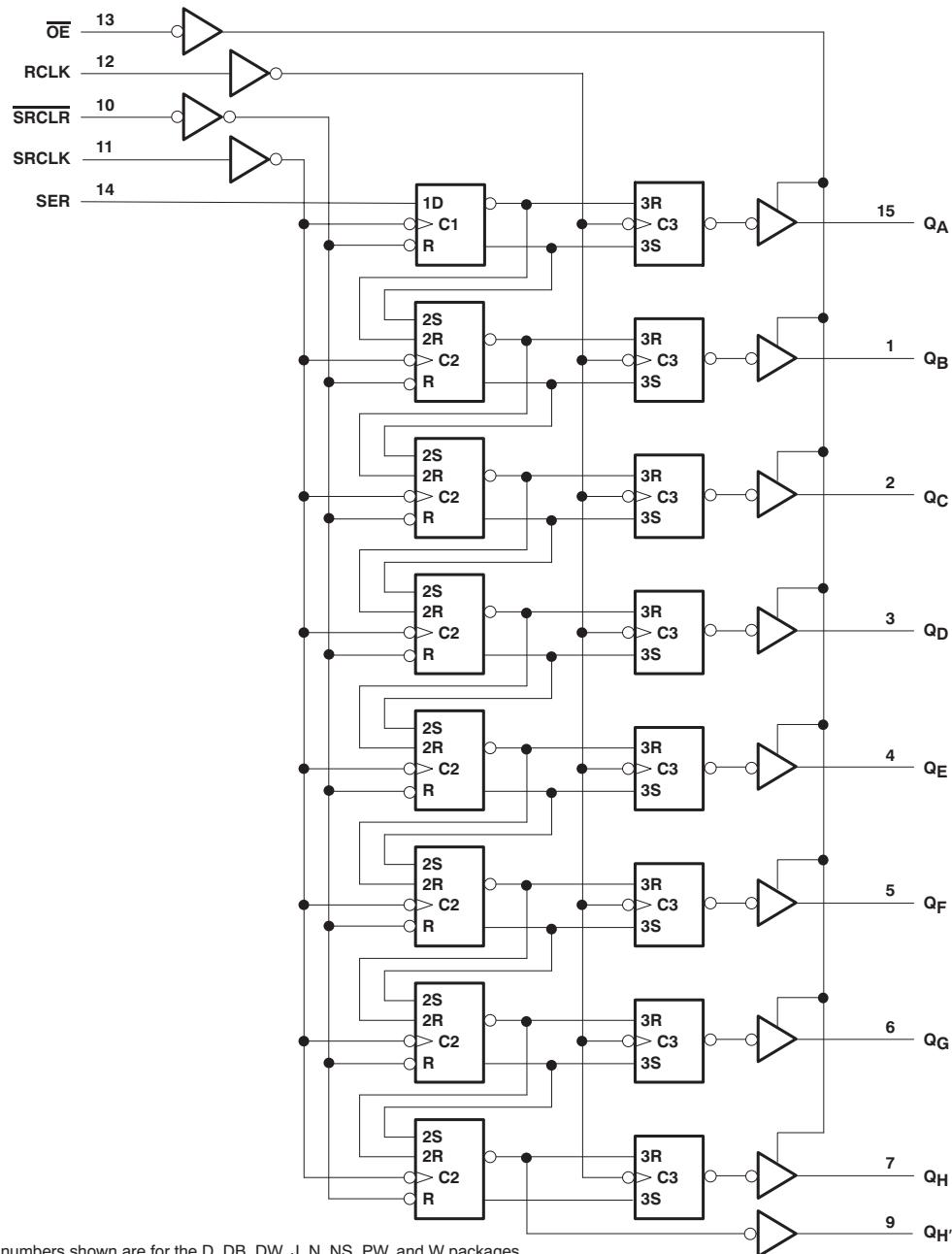
9 Detailed Description

9.1 Overview

The SNx4HC595 is part of the HC family of logic devices intended for CMOS applications. The SNx4HC595 is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

9.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

The SNx4HC595 devices are 8-bit Serial-In, Parallel-Out Shift Registers. They have a wide operating current of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The devices have a low power consumption of 80- μ A (Maximum) I_{CC} . Additionally, the devices have a low input current of 1 μ A (Maximum) and a \pm 6-mA Output Drive at 5 V.

9.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SNx4HC595 devices.

Table 1. Function Table

| INPUTS | | | | | FUNCTION |
|--------|------------|--------------|------------|-----------|--------------------------------------------------------------------------------------------------------------|
| SER | SRCLK | <u>SRCLR</u> | RCLK | <u>OE</u> | |
| X | X | X | X | H | Outputs $Q_A - Q_H$ are disabled. |
| X | X | X | X | L | Outputs $Q_A - Q_H$ are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | \uparrow | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | \uparrow | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | X | X | \uparrow | X | Shift-register data is stored in the storage register. |