

Final Review

CSCI 2021: Machine Architecture and Organization

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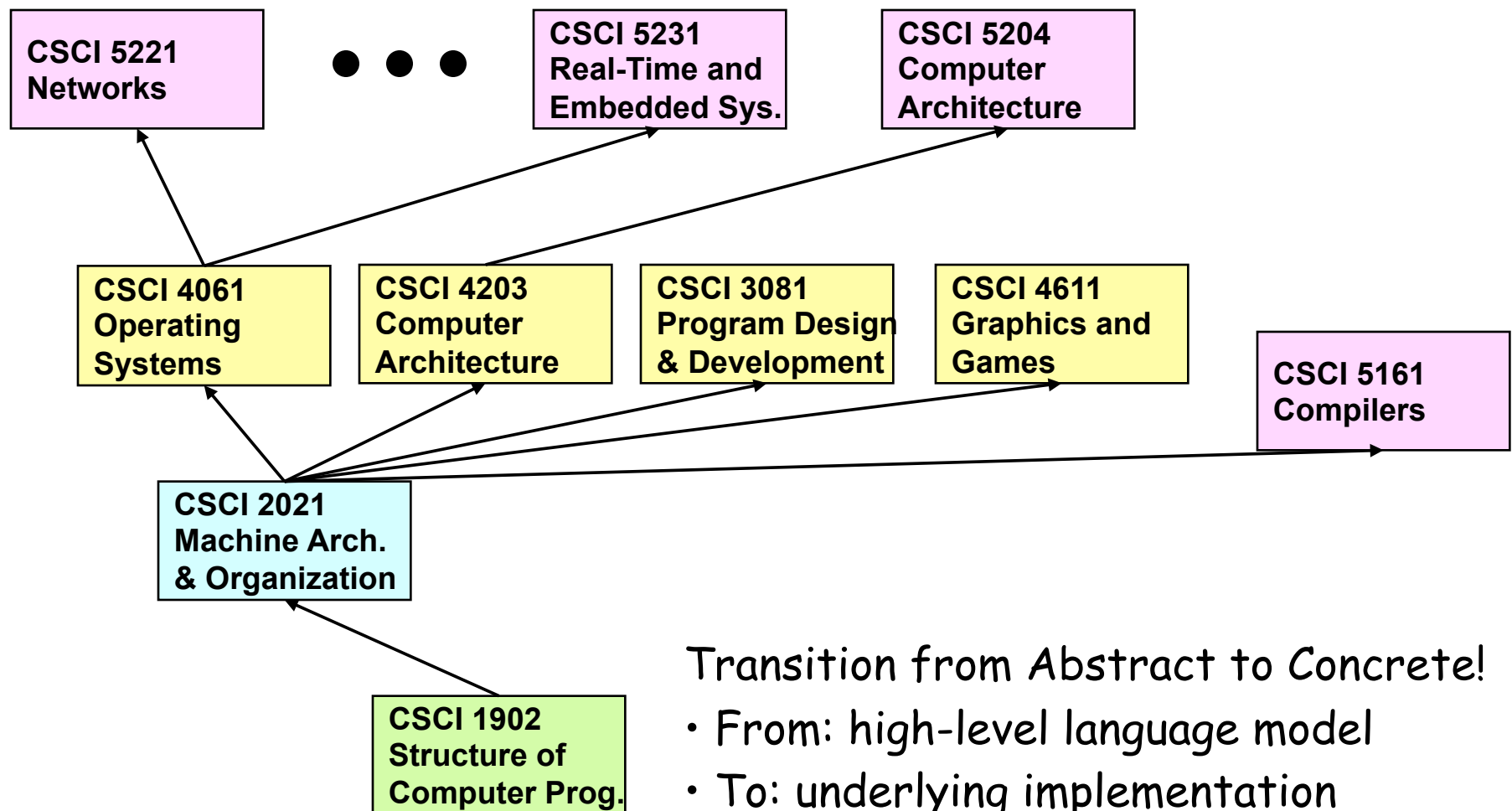
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UNIVERSITY OF MINNESOTA

Role within Curriculum

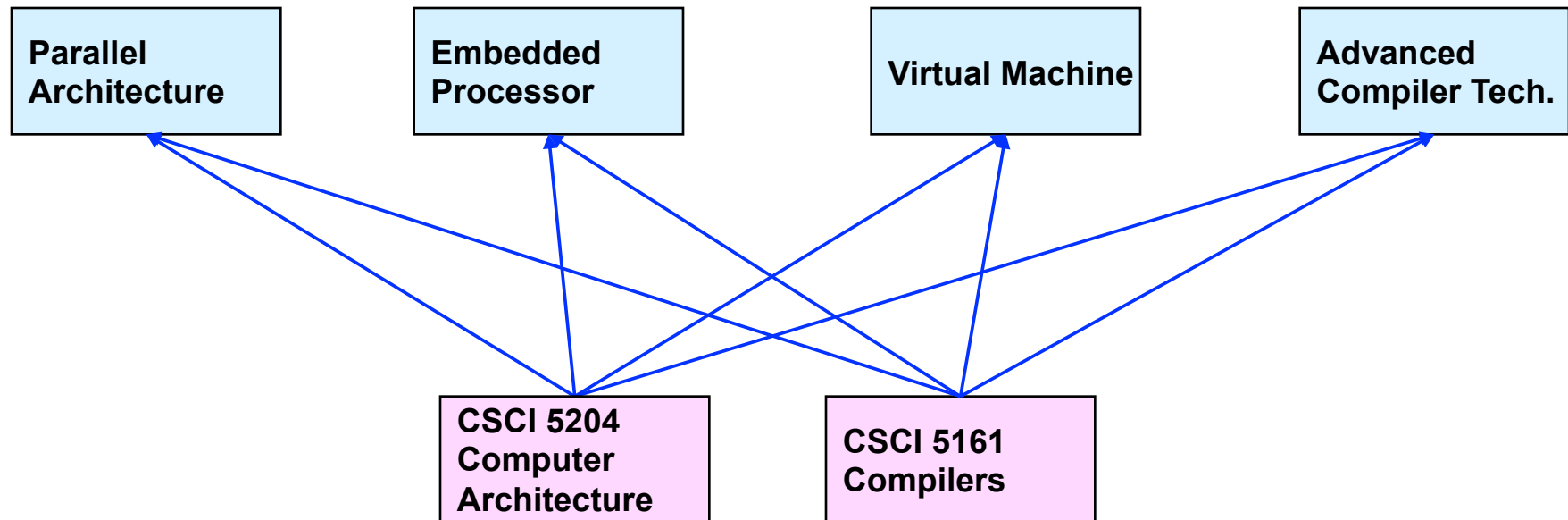


Transition from Abstract to Concrete!

- From: high-level language model
- To: underlying implementation

Computer Architecture & Compiler

A few 8000-level courses



Final Reviews

\$100

\$200

\$300

\$400

\$100

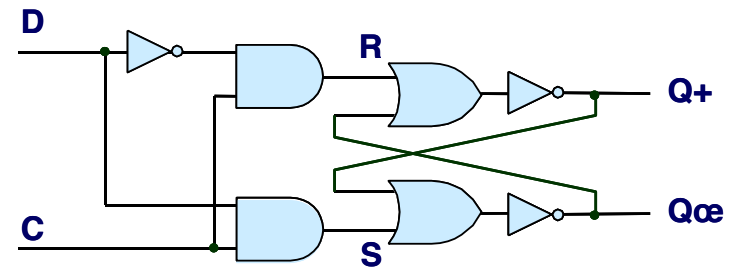
Design a digital circuit that determines if a 4-bit binary number is evenly divisible by 3.



\$200

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Latching



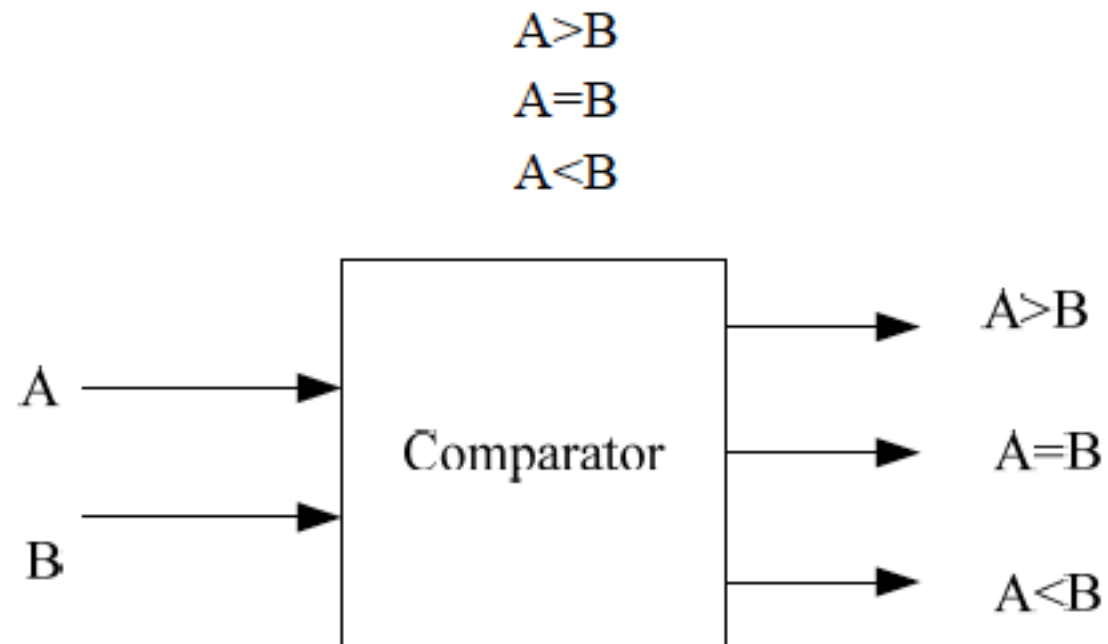
Can you design a D-latch
Using only NAND gates?



?

\$300

Design a 4-bit comparator.



\$400

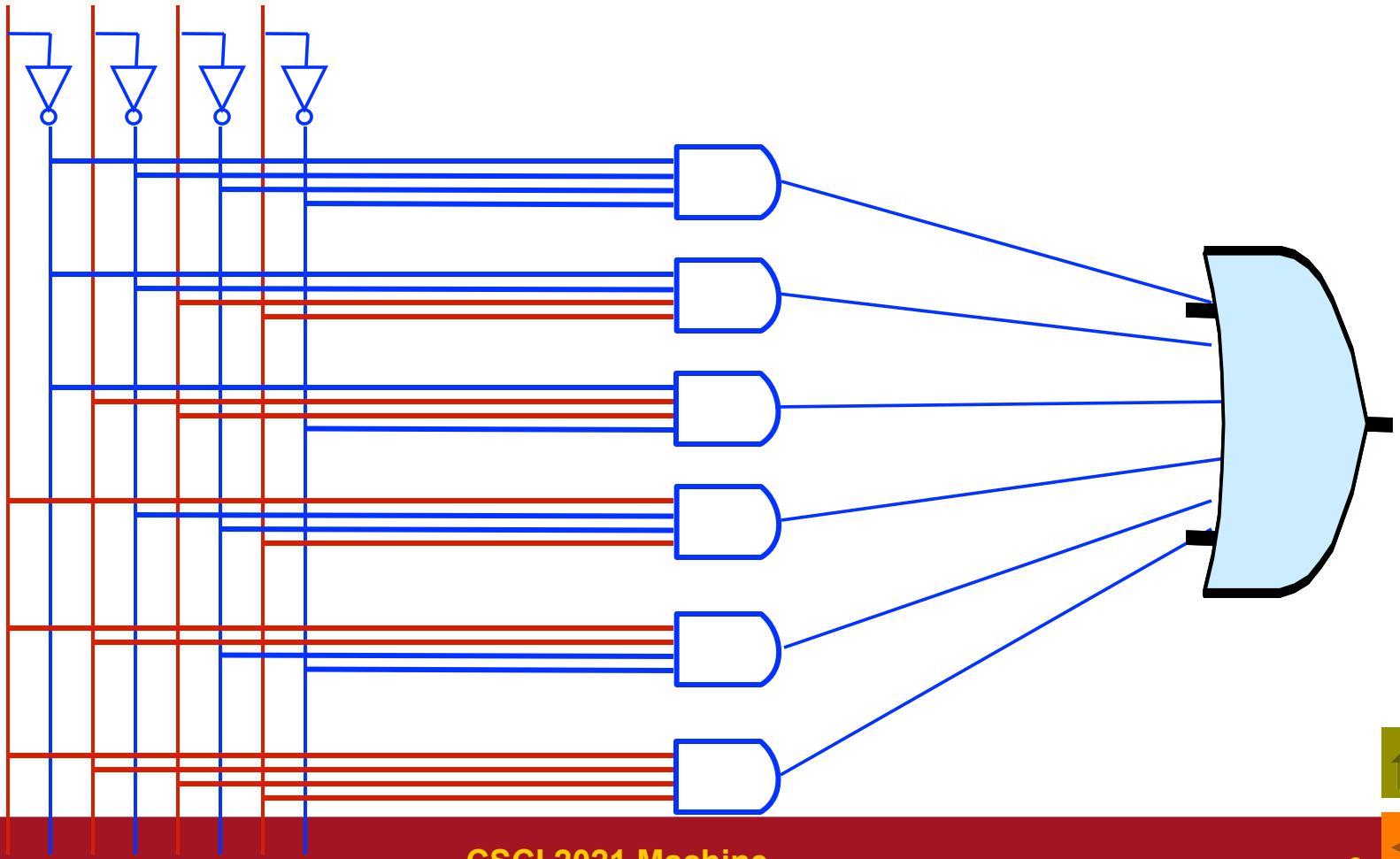
Design a sequential circuit that has a one-bit input (x) and a one-bit output (z). In this design, a new bit is read from the input stream in every clock cycle.

The output (z) is 1, if and only if the total number of 1's received from the input (x) is divisible by 3 (e.g. 0, 3, 6). In other words, the input sequence {0, 0, 1, 1, 0, 1, 0, 1} will result in the following output {1, 1, 0, 0, 0, 1, 1, 0}.

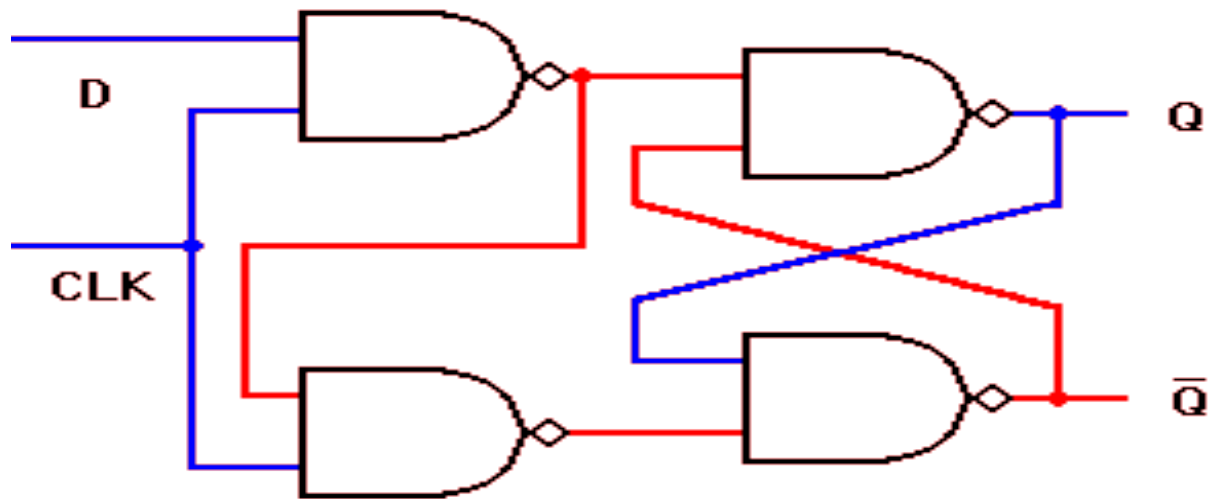


Answer: \$100

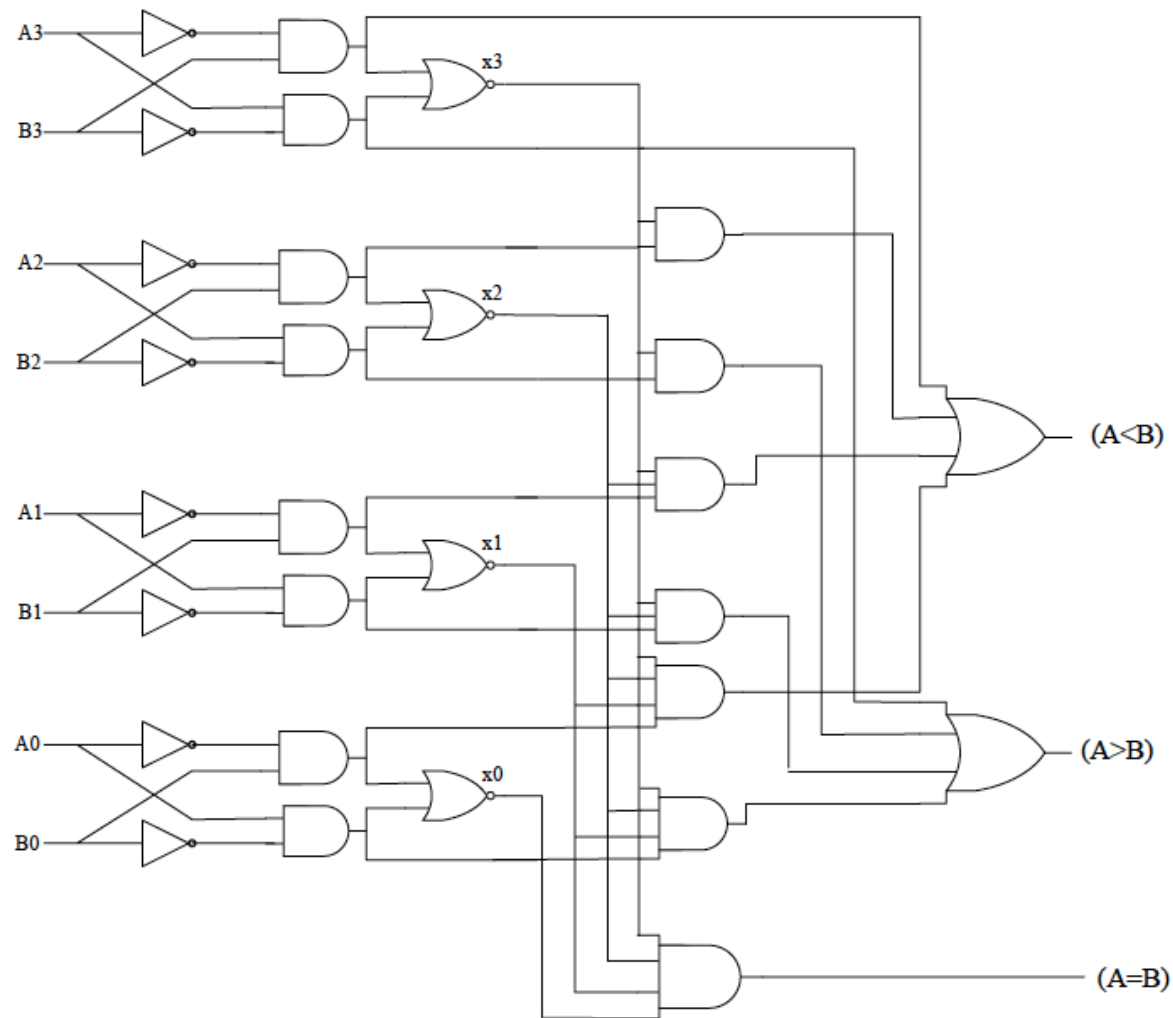
0000, 0011, 0110, 1001, 1100, 1111



Answer: \$200



Answer: \$300



300

(1) $A = B : A_3=B_3, A_2=B_2, A_1=B_1, A_0=B_0$

$$x_i = A_i B_i + A_i' B_i'$$

$$\text{XOR-Invert} = (A_i B_i' + A_i' B_i)'$$

$$= (A_i' + B_i)(A_i + B_i')$$

$$= A_i' A_i + A_i' B_i' + A_i B_i + B_i B_i'$$

$$= A_i B_i + A_i' B_i'$$

Output: $x_3 x_2 x_1 x_0$

300

(2) $A > B$

Output: $A^3B'^3 + x^3A^2B'^2 + x^3x^2A^1B'^1 + x^3x^2x^1A^0B'^0$

(3) $(A < B)$

Output: $A'^3B^3 + x^3A'^2B^2 + x^3x^2A'^1B^1 + x^3x^2x^1A'^0B^0$

300

Design the comparator with multiplexer

300

One bit comparator

Answer: \$400

