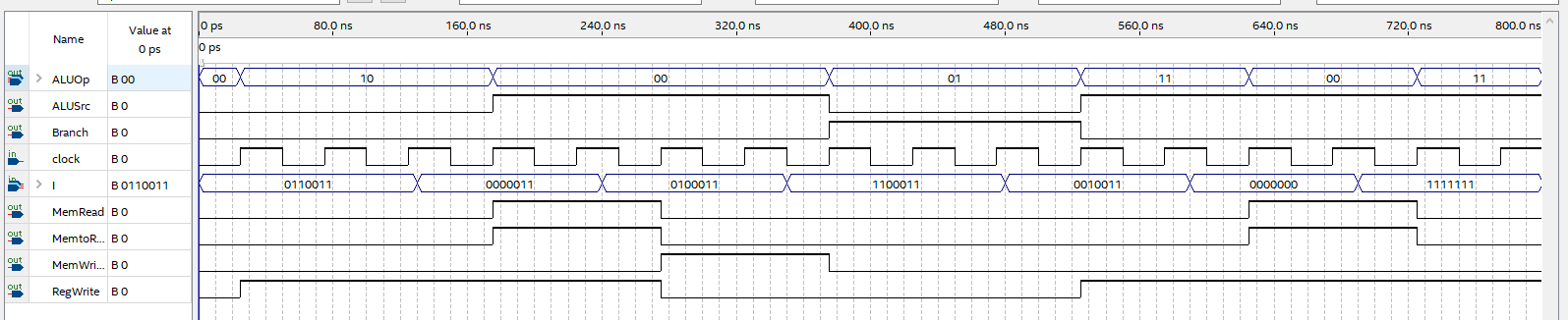
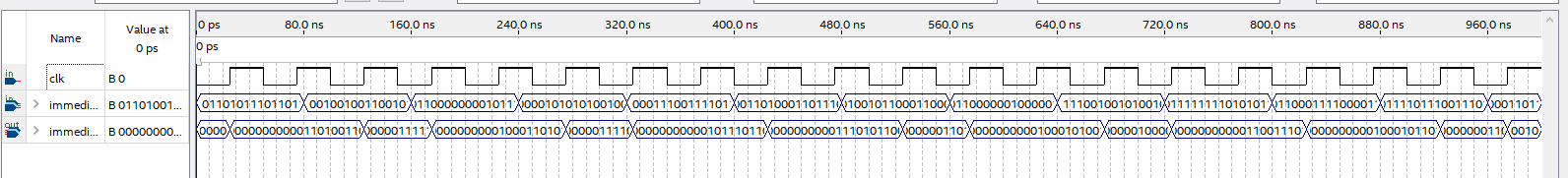
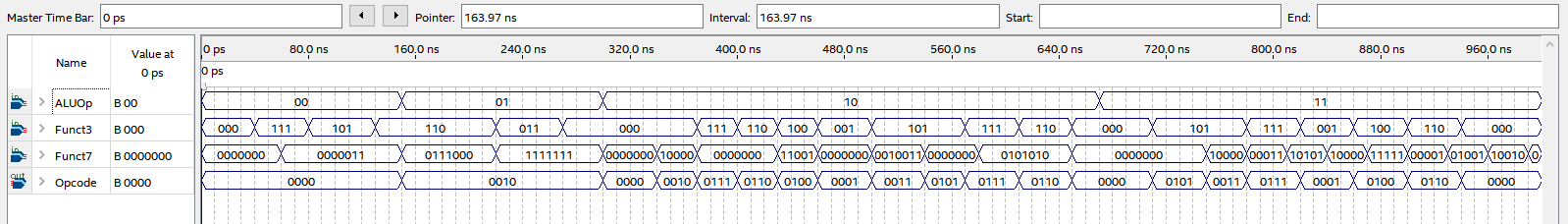
Control unit (waveform in control unit project)



Immgen

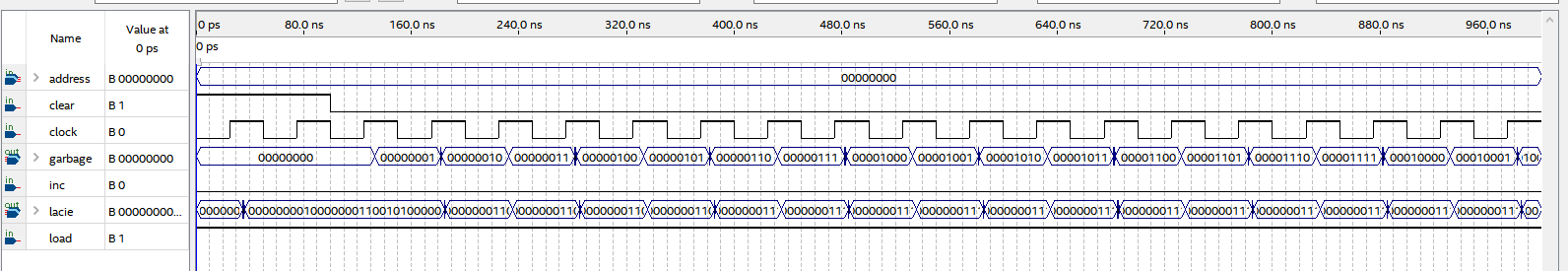


ALU control (waveform 9 and in alu control project)

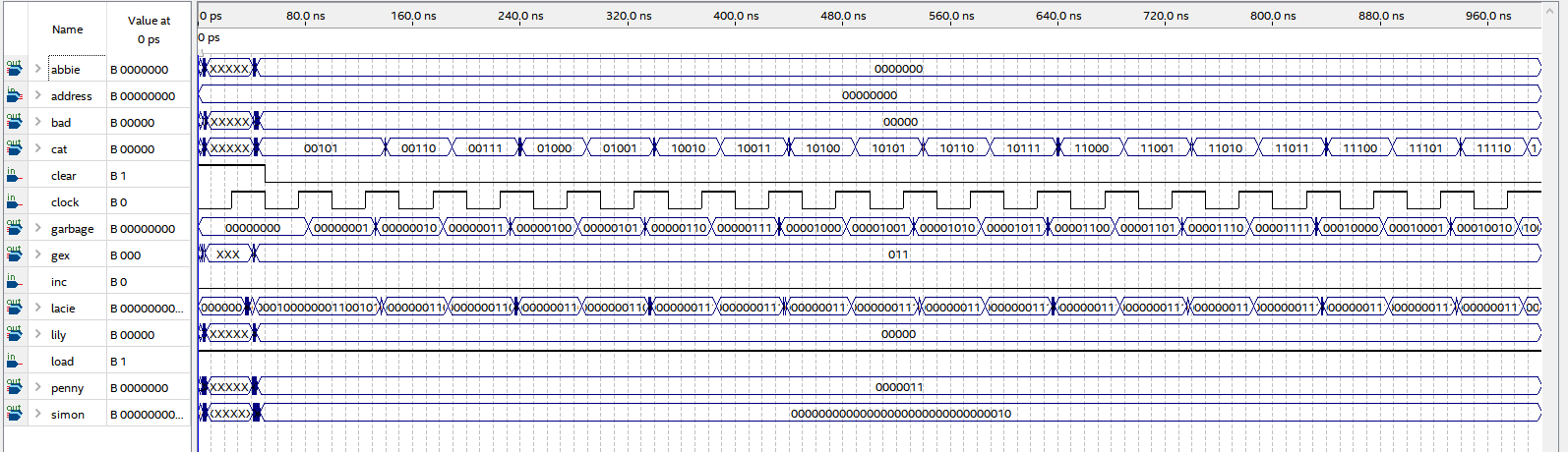


As I had issues when trying to do the entire datapath I went through this component by component (adding to the ones already in the datapath… I guess if this were an ANOVA test it would be sequentialThinking Face on Apple iOS 13.3) checking each of their outputs. Here they are:

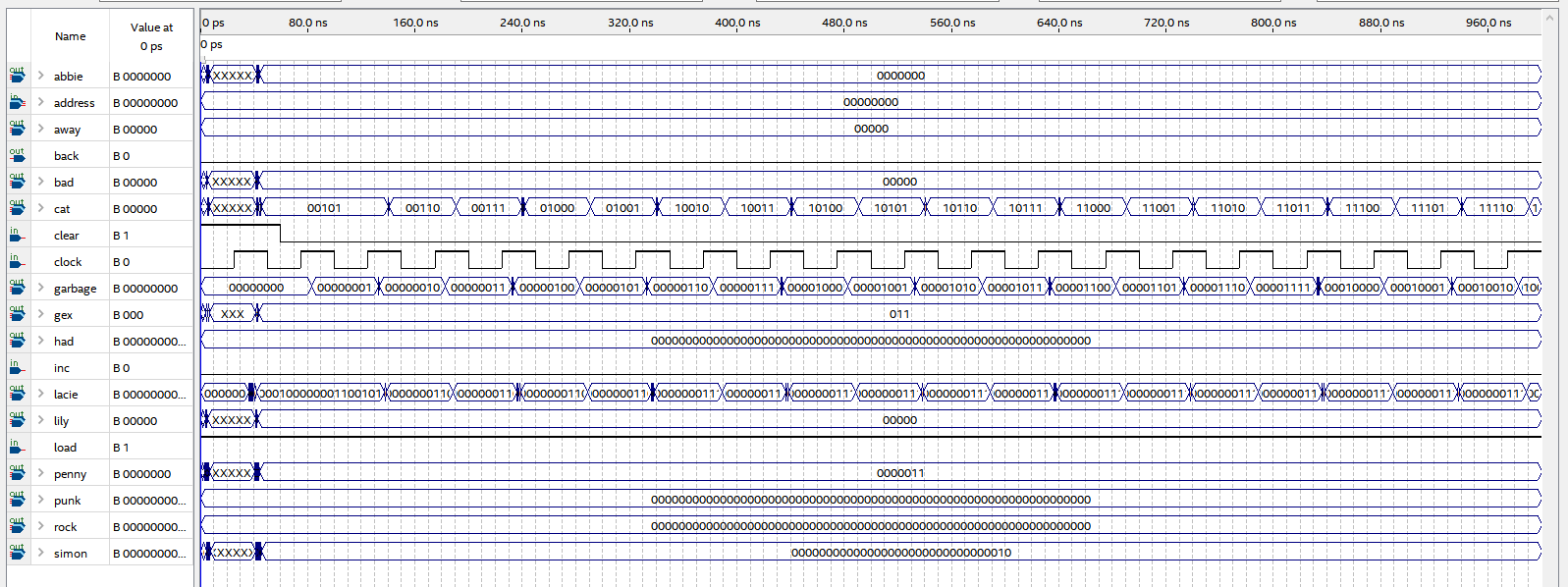
IF 2 ns delay (waveform1)



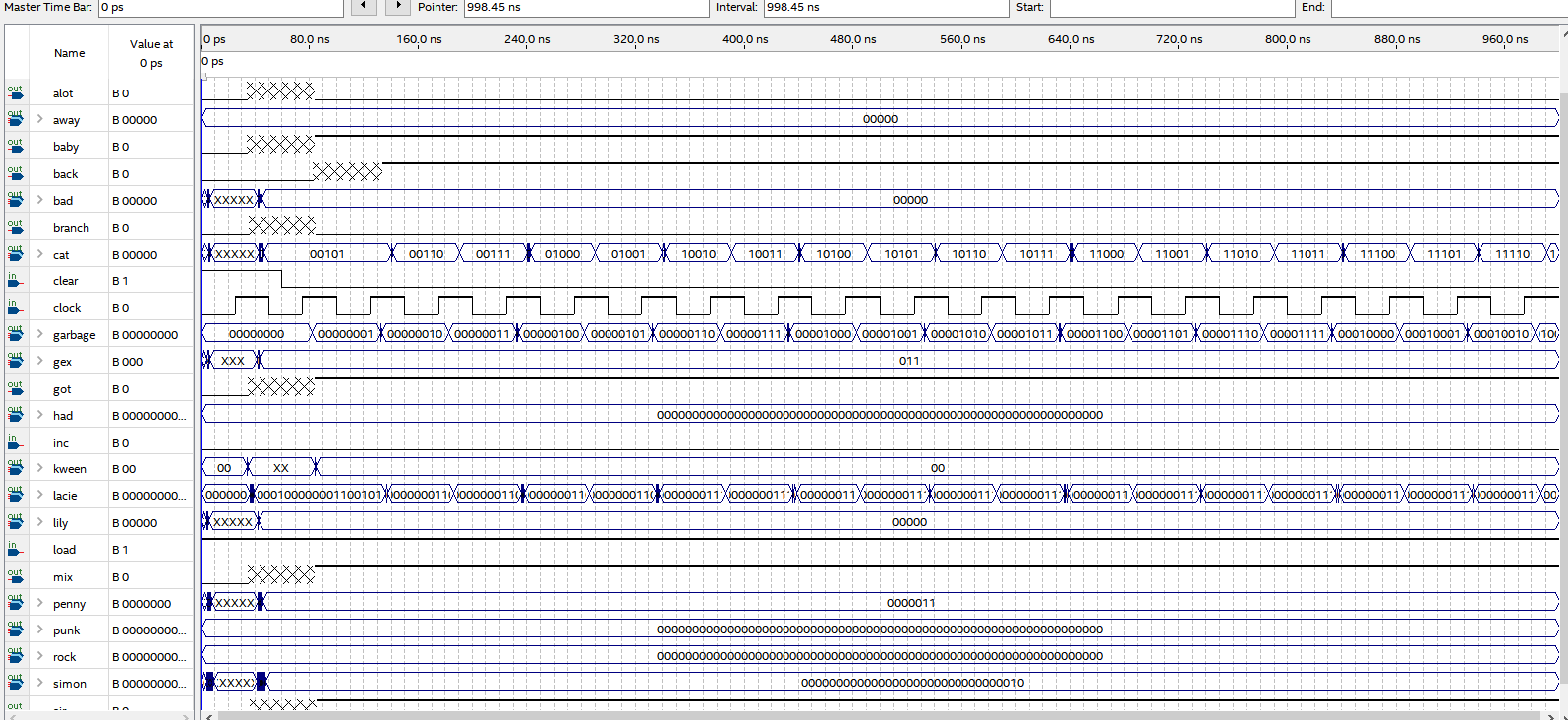
Decoder 8 ns delay (waveform2)



Register file, anything from a control unit comes as 0 since it has not been instantiated yet 7 ns delay (waveform3)



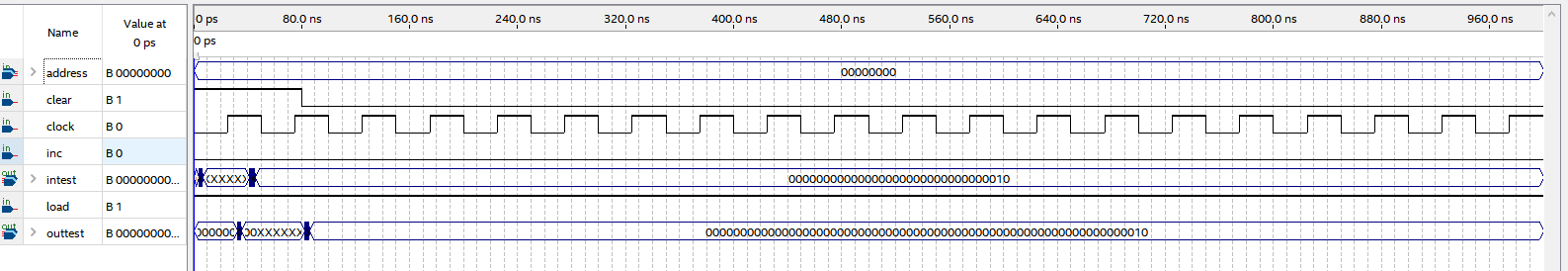
Control unit delay 7 ns (waveform4)



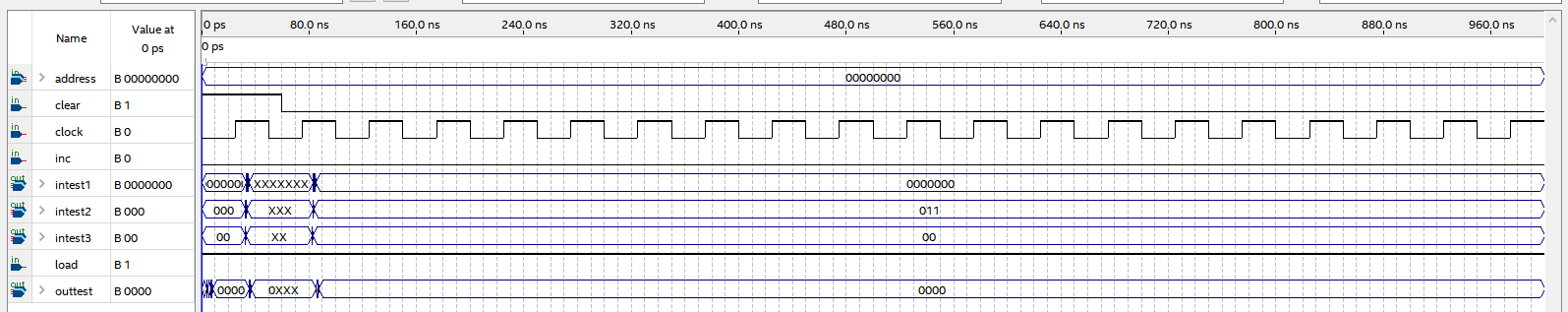


Signals are getting out of hand so only testing ones specific to the unit at hand (should have been doing this the whole time but don’t want to fix it now)

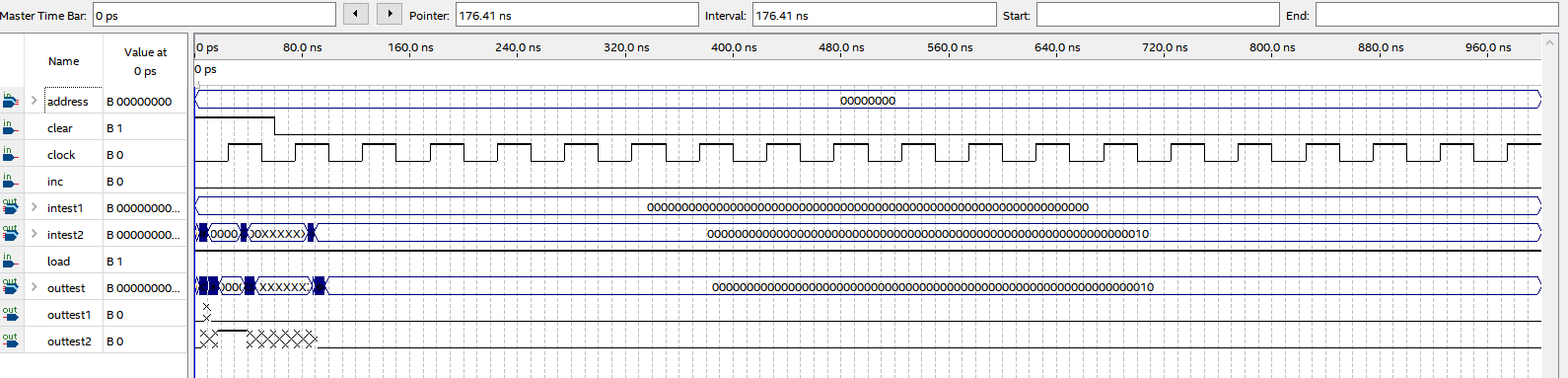
Immgen 5 ns delay didn’t add the vhdl still worked.. is this a bad idea (waveform5)



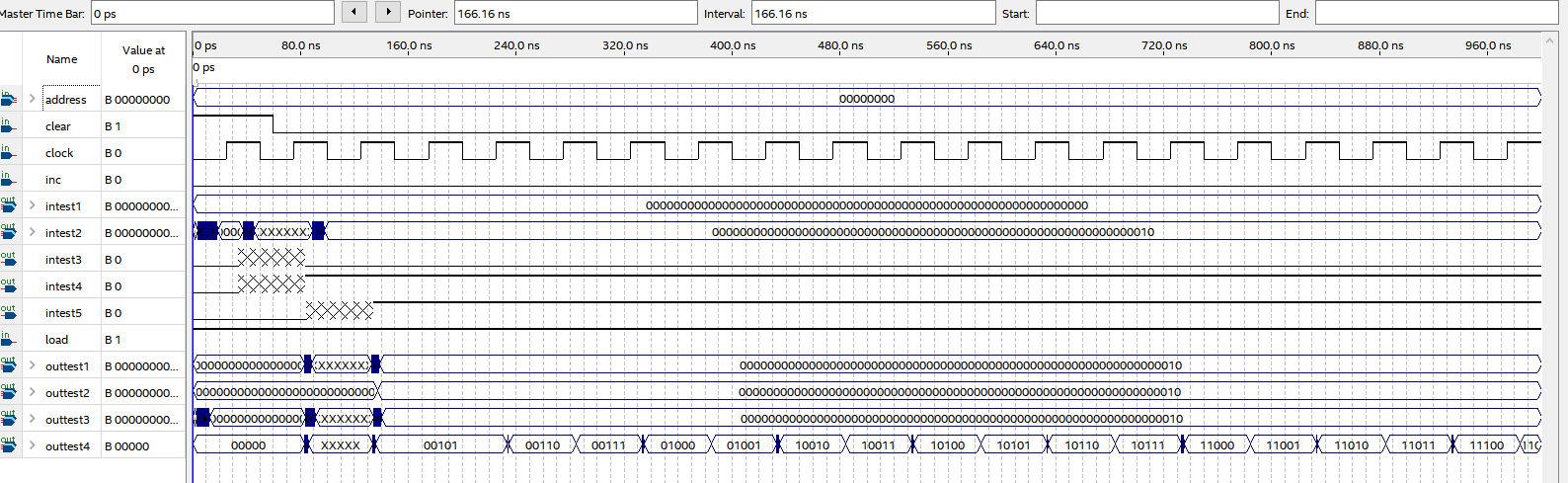
ALU control Delay 3 ns (waveform6)

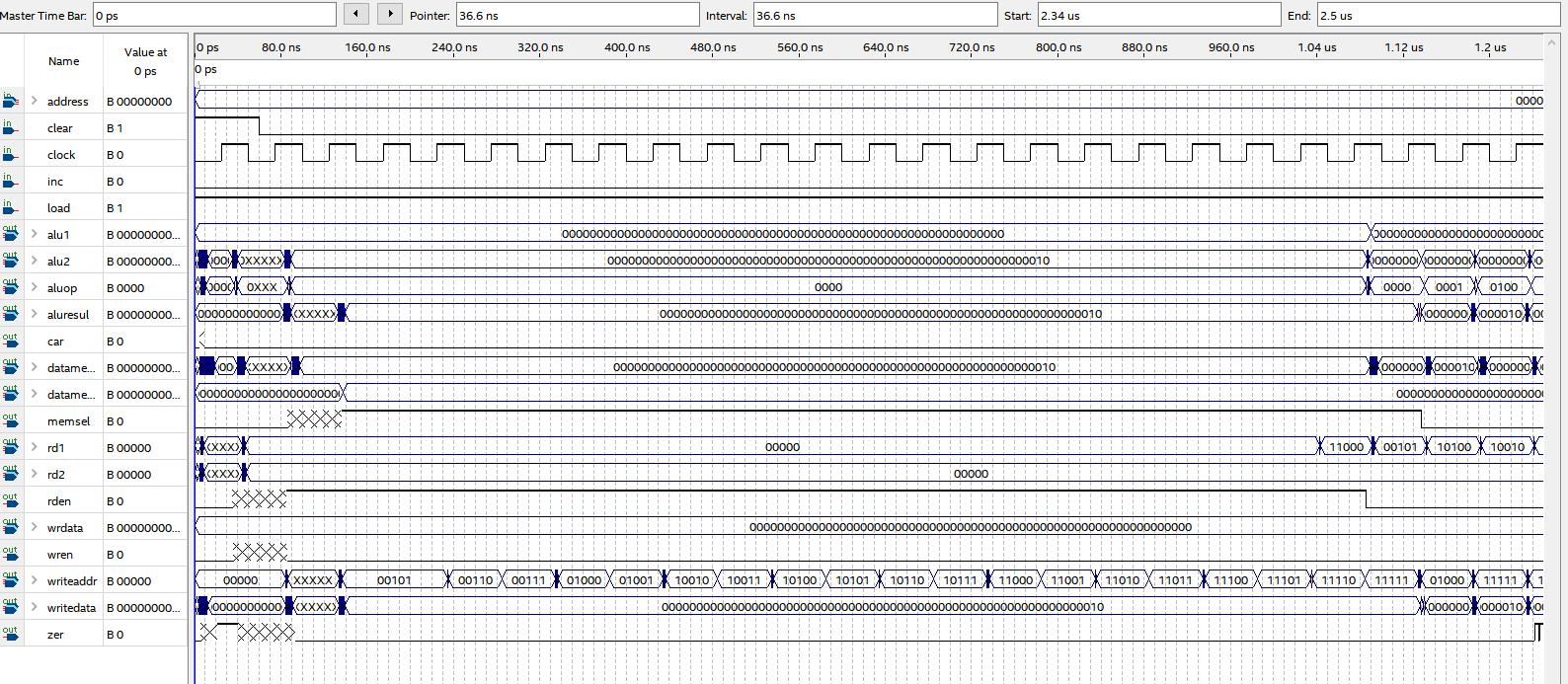


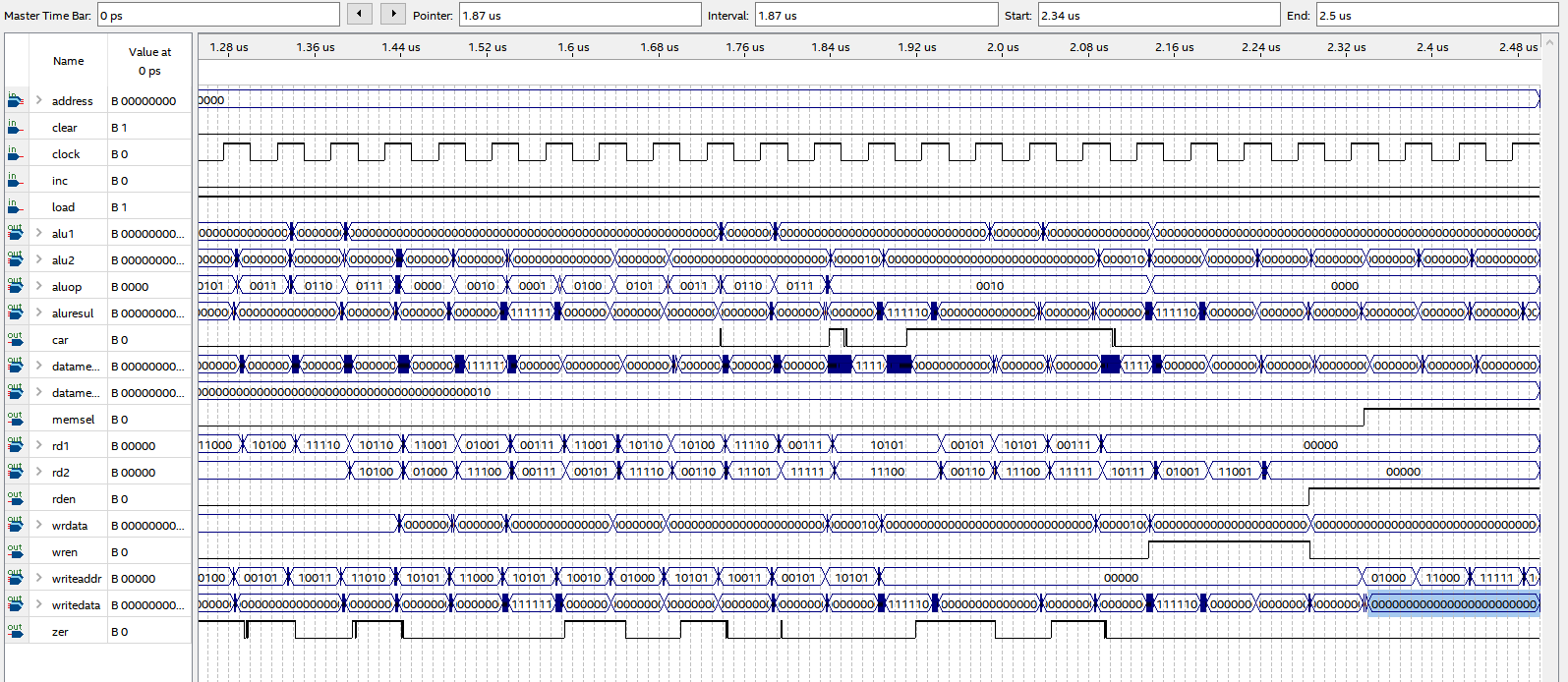
ALU 64 delay 12 ns (waveform7)



Data\_mem (full path) 11 ns delay (waveform)

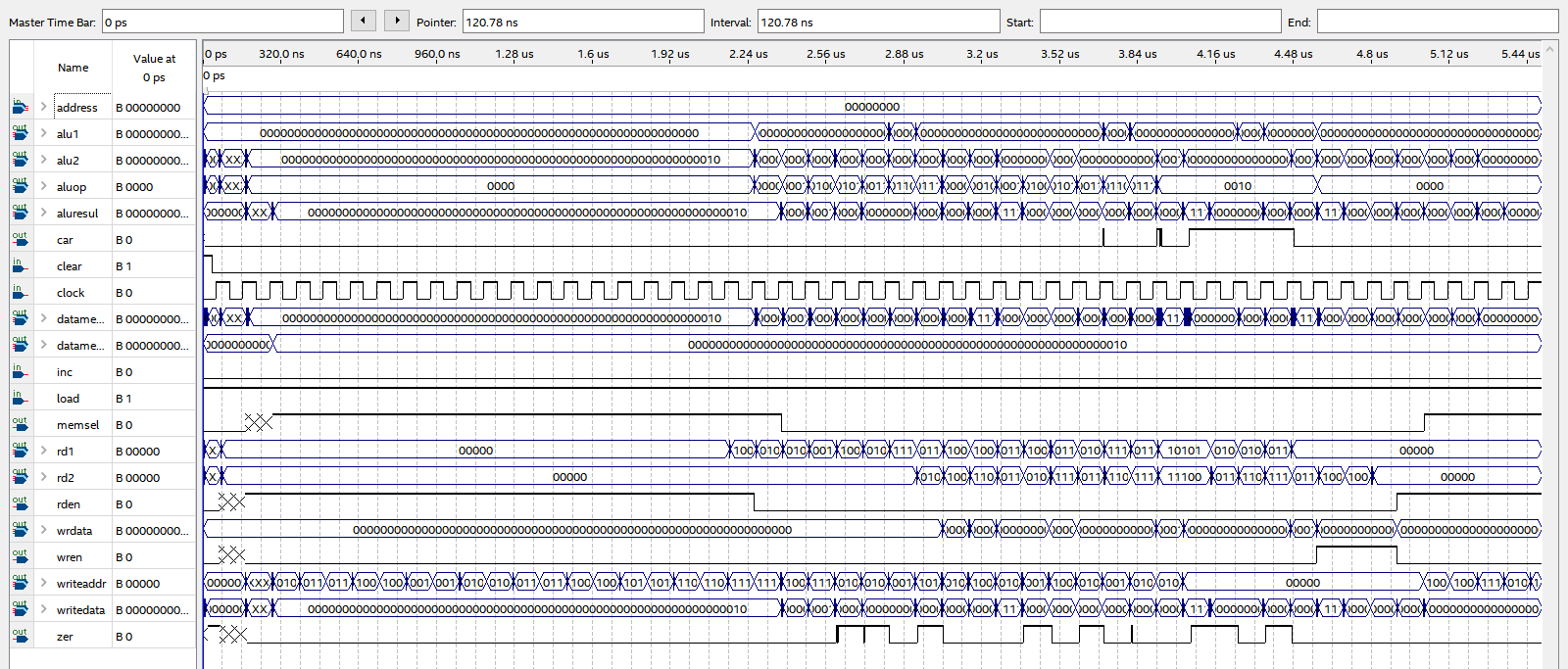






Worst case here gave 23 ns so used a 50% duty cycle at 50 ns period, however we see the subtraction gives the longest delay (as it has a bit flip and an addition) and from the previous lab we know that this occurs when we subtract 0 from 1 with a carry on each level. Because we are using 2’s compliment this means we start with 11111111 – 11111111 so when the bits are flipped for subtraction we get 11111111+ 00000001. The one in the LSB starts the carry. This delay was approx 53 ns, so to be sure that we can handle this delay we use a 50% duty cycle at 110 ns period pictured below for the testing and the actual datapath with no ouputs.

(Waveform)



Waveform10

