B.Sc. Engg. (CSE)/HD(CSE), 4th Sem. Date: August 30, 2019 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination — Summer Semester, A. Y. 2018-2019
Course No.: EEE 4483 — Time: 90 Minutes
Course Title: Digital Electronics and Pulse Techniques — Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper. All symbols bear their usual meanings.

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1. a) Mentioning differential and common inputs applied to an op-amp, derive the following equation, where A_d and A_c have their usual meanings. Draw relevant diagrams that are helpful to explain the steps of derivation. 8

$$\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c}$$

b) What is quantization error? Explain how successive approximation ADC works. 2+6

c) What is the difference between std_logic and bit? 2

d) Implement the equation using op-amps: 7

$$11x_1 - 7x_2 - 20\frac{d^2}{dt^2}x_3 + \iint 12x_4\,dt - 5\iint y = 0$$

Where x_1, x_2, x_3 and x_4 are the inputs and y is the output.

2. a) Show the capacitor charging and discharging path drawing the internal block diagram of a 555 Timer. 5

b) Derive the design equations from the circuit schematics from 2(a). From the derived design equations find the period, frequency and duty cycle. Draw the timing diagram of capacitor voltage, comparator outputs (set and reset), output from the flip-flop and transistor voltage. 8+3

c) Draw the pin diagram of LM741 IC. 3

d) With relevant equations and diagrams explain the operation of OpAmp as Differentiator and Integrator. 2+1

e) Why anti-aliasing filter is used?

3. a) What are the different layers of abstraction in digital system design? Draw the Gajski and Kuhn's Y-chart showing different design domains. 3

b) Briefly explain the vector types in VHDL. 2+5

c) What is the significance of process statement in VHDL? Explain with example. 3

d) Design a VHDL testbench for a full-adder circuit. 3

4. a) Determine the output voltage of the circuit in Fig. 4(a).

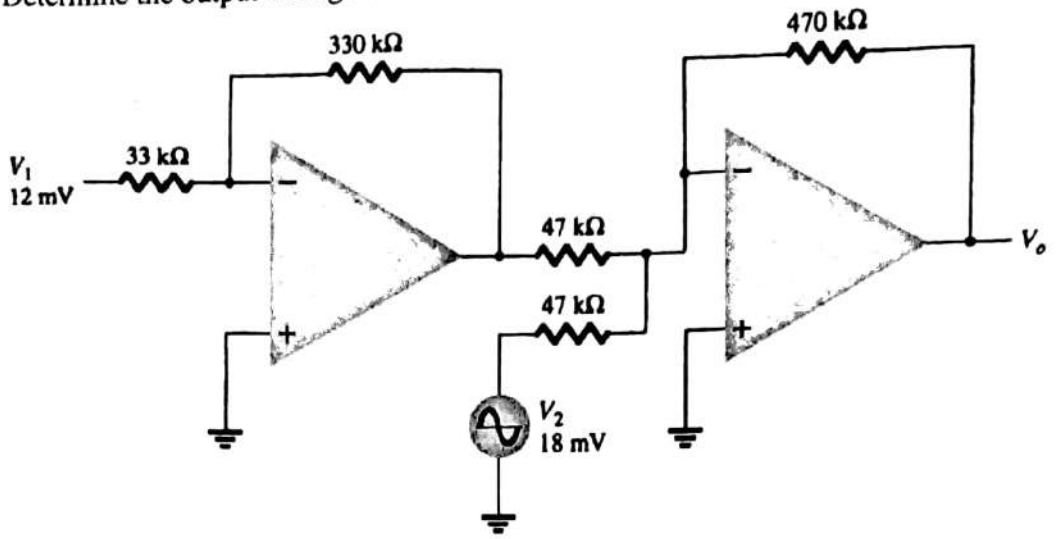

Fig. 4(a)

b) What are the disadvantages of binary-weighted input digital-to-analog converter (DAC)? How to overcome the disadvantages by using R-2R ladder DAC? 5

c) What are the different types of PWM signals? Explain their difference with necessary figures. 5

d) Explain the operation of a sample and hold (S/H) circuit. Draw the generic block diagram of S/H circuit. Assuming sinusoidal signal as input, draw the output from the switching gate, sampled output and final version of the signal from the S/H circuit. 6

e) Mention at least 5 libraries while writing a VHDL program. 3

f) What is the significance of high input impedance in operational amplifiers? 2