B. Sc. Engg. / HD CSE 2nd Semester (110)

21 August 2017 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION

SUMMER SEMESTER, 2016-2017

DURATION: 1 Hour 30 Minutes

FULL MARKS: 75

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **4 (Four)** questions. Answer any **3 (Three)** of them.

Figures in the right margin indicate marks.

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1. a) What are the benefits of universal gates? Implement the functionalities of NAND gates using NOR gates and the functionalities of NOR gates using NAND gates. 7

   b) Analyze the two output combinational circuit shown in Figure 1. Obtain the Boolean Functions for the two outputs and explain the circuit operations. 10

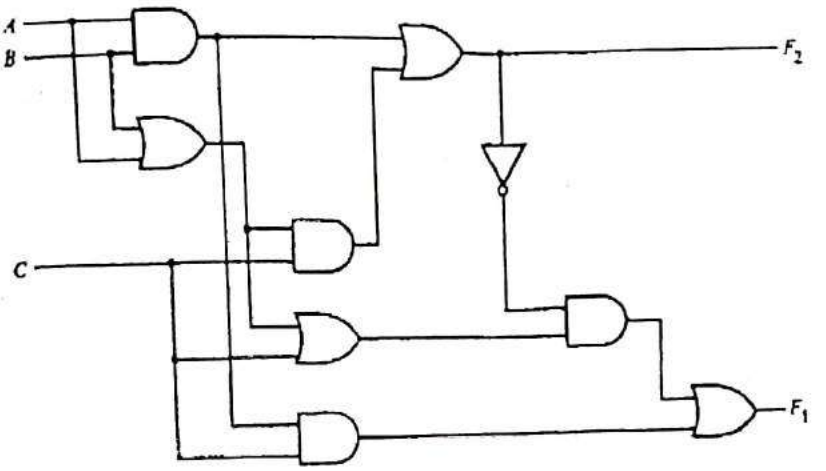

Figure 1: Combinational circuit.

   c) Simplify the following Boolean expressions to a minimum number of literals. 8

   i. $(A + B)'(A' + B')$

   ii. $(x'y' + z)' + z + xy + wz$

2. a) Generally NAND and NOR gates are implemented and verified using 2 inputs. Can you extend the number of inputs of them (more than two) as we do for AND or OR gates. Justify your answer with proper explanation and circuit diagram. 5

   b) *Parity generator* is a circuit that generates parity bit in the transmitter and *parity checker* is one that checks the parity in receiver. Now draw two circuit diagrams of parity generator and parity checker using exclusive-or and equivalence gates only for *4-bit message*. Consider **even parity** for parity generation and checking. 8

   c) Following *Design Procedure*, design a 4-bit binary-to-gray code converter including function table and logic diagram. 12

3. a) Simplify the following Boolean functions using Karnaugh-Map in (i) POS and (ii) SOP form. 12

   i. $F = ABC + A'B'CD' + A'BC'D$

   a. $d = B'D + A'BD' + AB'D'$

   ii. $F(w,x,y,z) = \prod(1, 3, 5, 7, 13, 15)$

b) Simplify the following Boolean function by means of *Quine-McCluskey* method and also implement the simplified expression using NOR gates only.

$$F(w,x,y,z) = \sum(0,1,5,7,8,10,14,15).$$

4. a) Suppose for arithmetic addition of two decimal digits, augend and addend are taken in BCD together with a possible carry from a previous stage. The output sum of the decimal digits must be represented in BCD. Now construct a block diagram that can solve the abovementioned problem with necessary function table and simplification steps.

b) It is necessary to multiply two binary numbers, each two bits long, in order to form their product in binary. Let the two numbers be represented by $a_1\ a_0$ and $b_1\ b_0$ where subscript 0 denotes the least significant bit.

i. Determine the number of output lines required.
ii. Find the simplified Boolean expressions for each output following necessary procedures.
iii. Draw the circuit diagram.

c) What is a self-complementary code? What are the advantages of these codes over BCD? Give corresponding examples that verify your answer.