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B.Sc. Engg. / HD CSE 2nd Semester 27 October 2018

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION **SUMMER SEMESTER, 2017-2018**

DURATION: 3 Hours **FULL MARKS: 150**

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

There are 8 (eight) questions. Answer any 6 (six) of them.

Figures in the right margin indicate marks.

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1. a) Show that the dual of the exclusive-OR is equal to its complement. 5

   b) Find the value of x for the following equations: 10

   i. x = 9's complement of $(453)_{10}$

   ii. $(110101.101)_2 = (x)_4$

   iii. x = BCD of 8620

   iv. x = Excess-3 code of 37

   c) Define following terms (Draw diagram if necessary): 10

   i. Demultiplexer

   ii. Encoder

   iii. Pulse and Edge Trigger

   iv. Race Condition

2. a) Suppose, input to a combinational circuit is a 4 bit binary number. Design a circuit with minimum gates for the following: 15

   i. Output, P = 1, if the number is prime

   ii. Output, Q = 1, if the number is divisible by 3

   b) Obtain the simplified Boolean expressions for output *F* and *G* in terms of the input variables in the circuit of Figure below and construct their truth table. 10

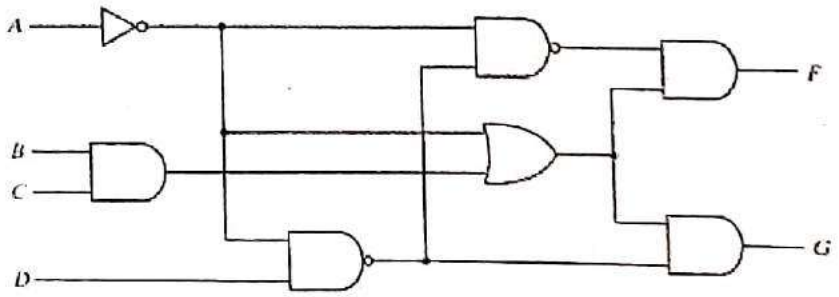

Figure 1: A combinational Circuit.

3. a) Design a combinational circuit that generates the 9's complement of a BCD digit. 10

   b) Show that the characteristic equation for the complement output of a *JK* flip-flop is $Q(t+1) = J'Q' + KQ$. 8

   c) Explain the differences among a truth table, a state table, a characteristic table, and an excitation table. Also, write the differences among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation. 7

4. a) What is Master-Slave flip-flop? Explain with block diagram and logic diagram. 5
   b) Design the conversion of JK flip flop into D flip flop and T flip flop. 10
   c) Design a 5 bit parity generator and parity checker with their corresponding equations. 10

5. a) Design a BCD to Seven segment display circuit using decoder. 10
   b) A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations. 15

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

   i. Draw the logic diagram of the circuit.
   ii. List the state table for the sequential circuit.
   iii. Draw the corresponding state diagram.

6. a) Design a modulo-16 counter, using JK flip flop with the following sequence:
   7,6,5,4,3,2,1,0,8,9,10,11,12,13,14,15,7,6,5,... 20
   b) What is the maximum propagation delay from clock to output for the counter of the Question 6.(a)? Explain your answer assuming necessary variables. 5

7. a) What is the difference between serial and parallel transfer? What type of register is used in each case? 5
   b) Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table (Table 1). 10

Table 1: Selection modes

S_1	S_0	**Register Operation**
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

   c) Write down the necessary equation accomplished by a 4 bit binary adder. Design that 4 bit magnitude comparator following those equations. 10

8. a) The content of a 4 bit shift register is initially 1101. The register is shifted six times to the right, with the serial input being 101101. What is the content of the register after each shift? 5
   b) Construct a binary counter that counts from 0 through binary 127. 10
   c) What is carry propagation delay of Binary Parallel Adder? How it can be reduced? Explain with necessary equation and figure. 10