B. Engg. / HD CSE 2nd Semester

31 October 2017

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SESTER FINAL EXAMINATION — SUMMER SEMESTER, 2016-2017

RATION: 3 Hours — FULL MARKS: 150

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.
There are 8 (eight) questions. Answer any 6 (six) of them.
Figures in the right margin indicate marks.

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a. Sensors are used to monitor the pressure and the temperature of a chemical solution stored in a vat. The circuitry for each sensor produces a HIGH voltage when a specified maximum value is exceeded. An alarm requiring a LOW voltage input must be activated when either the pressure or the temperature is excessive. Design a circuit for this application. 5

b. i. Find the complement of $F = x + yz$; then show that $F.F' = 0$ and $F + F' = 1$. 10
ii. Show that the dual of the exclusive-OR is equal to its complement.

c. Design a combinational circuit that converts a decimal digit from 2,4,2,1 code to 8,4,-2,-1 code. 10

a. Use a Karnaugh map to simplify the following expression to minimum form as directed: 12
i. $F(W,X,Y,Z) = (X+Y')(W+Z')(X'+Y'+Z')(W+X+Y+Z)$ *(To minimum SOP form)*
ii. $F(A,B,C,D) = A'B' + AB'+C'D'+CD'$ *(To minimum POS form)*

b. A majority function is a combinational circuit which generates output 1 when the input variables have more 1s than 0s and 0 otherwise. Based on this argument design a 3-input majority function. 8

c. Show that $A \odot B \odot C \odot D = \sum (0, 3, 5, 6, 9, 10, 12, 15)$. 5

a. In number system, complements play a vital role in subtraction. There are two different methods of complement - r's and (r-1)'s complements. What are the basic reasons behind using two different types of complements in number system? 5

b. An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, and g) select the corresponding segments in the display, as shown in Fig. 1(a). The numeric display chosen to represent the decimal digit is shown in Fig. 1(b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display. 20

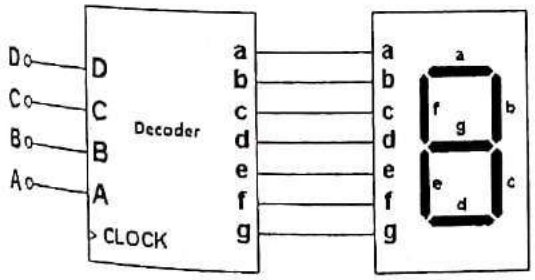

Figure 1(a): Segment Designation.

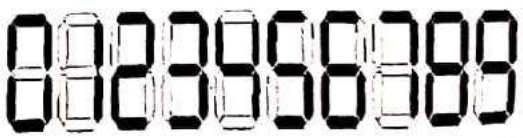

Figure 1(b): Numerical designation for display.

a. What are the differences between a synchronous counter and an asynchronous counter? 7

b. In sequential circuit, "Race around condition" creates a problem generating unstable output. Explain how it is generated in sequential circuit but not in combinational circuit with appropriate timing diagram. Describe possible remedies to fix this problem with appropriate examples and figures. 8

c) How can a universal shift register can be developed from a bidirectional shift register? Draw a figure of a 4 bits universal shift register where register operation will be selected according to the following table (Table 1).

Table 1: Register option table for question 4(c)

Mode Variables		Register Operation
S_1	S_0	
0	0	Parallel Loading
0	1	Shift Left
1	0	Shift Right
1	1	No Change

5. a) Write down the truth table of a D flip-flop. From the table prove that $Q_{(t+1)} = D$. Where D is the present input and $Q_{(t+1)}$ is the next state of the output.

b) Consider an analog clock as Fig. 2(a) and corresponding binary analog clock which is also presented in Fig. 2(b). In this binary analog clock, you can count from 0001(Binary of 1_{10}) to 1100(Binary of 12_{10}). Now you have to draw an asynchronous counter circuitry considering this binary analog clock.

*[**Hints:** An asynchronous counter starts counting from its highest or lowest possible state. For 4 bits asynchronous counter, lowest and highest states are 0000 and 1111 respectively. But both of these states are absent for this scenario. So initially you can start your count from 0000 state but it won't be repeated anymore.]*

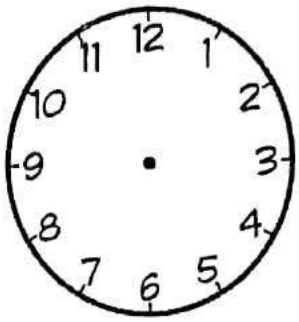

Figure 2(a): Analog Clock.

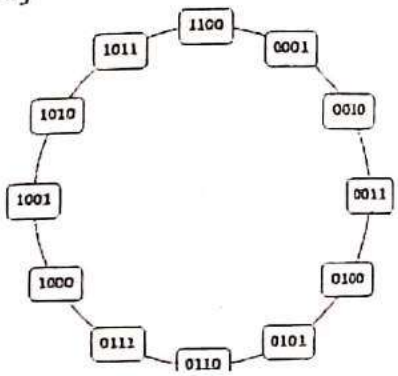

Figure 2(b): Binary Analog Clock.

c) Discuss relative comparison among R-S flip flop, J-K flip flop and Master-Slave flip flop with the help of appropriate diagrams and truth tables.

6. a) "The ROM is used to implement a complex combinational circuit in one IC package."-based on this statement discuss its internal configuration and how it is used as memory device.

b) How is the 4-to-2 encoder different from a 4-to-1 multiplexer? Draw the truth tables for following combinational circuits:
   i. 16-to-4 priority encoder.
   ii. 16-to-1 multiplexer.

c) Derive the state diagram from the following state table (Table 2).

Table 2: State table for question 6(c)

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Reduce the number of the states in the state table and tabulate the reduced state table. Also show the reduced state diagram.

starting from state 'd' of the given state table, find the output sequence (different states) generated with an input sequence 0 1 1 1 0 0 1 0 0 1 1. Do the same for the reduced state table state diagram and show that the output sequence is the same for the both cases for a same input sequence.

To build a ripple counter toggle (T) flip flop is normally used. In a Digital Logic Design sessional experiment you are asked to implement a 4 bit ripple up-down counter but there is scarcity of T flip flop in laboratory. Only you can use D flip flop as they are available at that moment. You know the conversion between different flip flops. Now how can you implement T flip flop using only D flip flop? 8

For an output cycle of 10 clock pulses, draw the 3 outputs Q_0, Q_1 and Q_2 of the ripple counter on the grid in Fig. 3. State which output is the MSB and which is the LSB. Assume that you start in the all-zeros state (000) as shown below. Assume the J-K flip-flops are rising-edge-triggered. 7

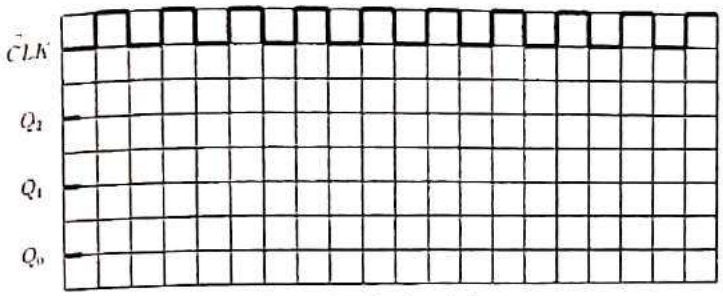

Figure 3: Timing Diagram.

A full subtractor is a combinational circuit that can take three bits as input and produce two bits as output. Now implement a full subtractor circuitry using convenient multiplexer. 10

In Fig. 4 a Pattern Detection Machine is demonstrated which recognizes the sequence "0110". This pattern detection machine is nothing but a finite state machine that represents a sequential circuit. It produces output *found = 1* when the sequence is occurred otherwise *found = 0*. Based on this scenario answer the following questions: 20

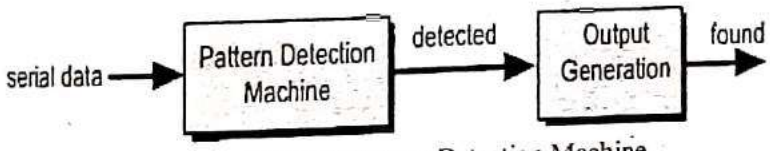

Figure 4: Pattern Detection Machine.

i. Draw and label the transitions in the state diagram where states are **START**, **GOT0**, **GOT01**, **GOT011**, and **GOT0110**.

ii. Write the state table from the state diagram.

iii. Using J-K flip flop build a pattern detector circuit which can detect the sequence "0110" following *Design procedure*.

iv. For the following input bit stream, generate the output bit stream considering '*overlapping*' condition:
Input bit stream = 00111001101101010 5

What is the purpose of power-on **LOAD** input in register?