B. Engg. / HD CSE 2nd Semester (64)

25 October 2016

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MESTER FINAL EXAMINATION — SUMMER SEMESTER, 2015-2016

RATION: 3 Hours — FULL MARKS: 150

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **8 (eight)** questions. Answer any **6 (six)** of them.

Figures in the right margin indicate marks.

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1) Describe the operation of a 3-bit up-down ripple counter using J-K flip-flop with relevant diagram. 7

2) Explain the operation of a 4 bit bidirectional shift register using D flip-flop and provide necessary figure. 10

3) Distinguish between PLA and PAL. Design disjoined PLA and PAL for the Boolean functions given below: 8

$X(a,b,c) = \sum (2,3,5,7)$

$Y(a,b,c) = \sum (0,1,5)$

$Z(a,b,c) = \sum (0,2,3,5)$

4) a) Find the value of **x** for the following equations: 5

i. $(13442)_7 = (321020)\mathbf{x}$

ii. $(110101)_2 = (\mathbf{x})_{\text{Gary code}}$

b) Describe the operation of a clocked S-R flip-flop with appropriate truth table, characteristic table, excitation table, characteristic equation and graphic symbol. How can a clocked S-R flip-flop can be converted into a clocked D flip-flop? 10

c) Design an asynchronous BCD counter and explain its operation. Mention a different type of name for this counter. 10

5) a) Draw the following combinational logic circuit with appropriate truth table: 10

i. Octal-to-binary encoder

ii. Binary-to-octal decoder

b) Derive the state diagram from the following state table given in Table 1. Reduce the number of the states in the state table and tabulate the reduced state table. Also show the reduced state diagram. 10

Table 1: State table for Question 3(b)

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Starting from state '*d*' of the given state table, find the output sequence generated with an input sequence 0 1 1 1 0 0 1 0 0 1 1. Do the same for the reduced state table/state diagram and show that the output sequence is the same for the both cases for a same input sequence.

c) Write down the truth table of a T flip-flop. From the table prove that $Q_{(t+1)} = \overline{Q_{(t)}}$. Where $Q_{(t)}$ is the present state and $Q_{(t+1)}$ is the next state of the output.

4. a) How can a full adder be implemented with the help of half adder? Draw necessary diagram.
   b) Explain 'Race around' condition with appropriate timing diagram. Describe possible remedies with appropriate examples.
   c) Explain how a 2-bit gray code counter can be developed with J-K flip-flop with necessary diagram.

5. a) Design a 16:1 multiplexer with the help of 4:1 multiplexer.
   b) What are the differences between a synchronous and an asynchronous counter?
   c) How can register store data with the help of flip-flop which store only a single bit? Explain with necessary diagram.

6. a) "NAND and NOR gates can be defined as universal gate"- Explain. Design all basic logic gates using NAND and NOR gates.
   b) How can a universal shift register can be developed from a bidirectional shift register? Draw a figure of a universal shift register.
   c) What do you mean by preset and clear input in the flip-flop? Use J-K flip-flop to describe their operations with necessary diagram and truth table.

7. a) Obtain the simplified expressions in i. POS and ii. SOP form for the Boolean function: $F(w,x,y,z) = \prod(0,1,2,4,5,7,11,15)$
   b) Develop the state table containing the present state, next state, input and output for the state diagram given below. Also find out the state equations for this state diagram.

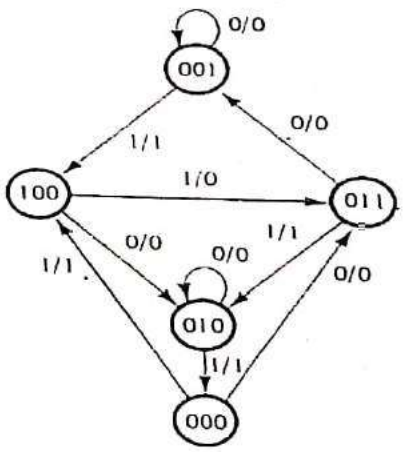

Figure 1: State diagram for Question 7(b)

   c) "Flip-flop can be used to develop a counter"- Explain with necessary timing diagram.

8. a) Distinguish between edge triggering and pulse duration/level triggering. Explain how a step signal can be converted to an impulse signal using necessary circuit diagram.
   b) Convert the D flip-flop to the T flip-flop following necessary steps.
   c) Compare among R-S, J-K and master-slave J-K flip-flops with necessary diagram.