B.Sc. Engg. in CSE/SWE 3rd Semester | 27 February 2020 (Afternoon)

# ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
## ORGANISATION OF ISLAMIC COOPERATION (OIC)
## Department of Computer Science and Engineering (CSE)

**MID SEMESTER EXAMINATION** | **WINTER SEMESTER, 2019-2020**

**DURATION: 1 Hour 30 Minutes** | **FULL MARKS: 75**

## CSE 4305: Computer Organization and Architecture

**Programmable calculators are not allowed. Do not write anything on the question paper.**

There are **4 (Four)** questions. Answer any **3 (Three)** of them.

Figures in the right margin indicate marks.

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a) To asses a system following SPEC benchmark suit, we have to consider a specific calculation procedure. 12

i. Mention each steps of that calculation procedure using respective evaluation flowchart.

ii. What type of mean will be used to calculate overall metric? Justify your assertion.

iii. How does this assessment procedure will take into account a system with multiple processors?

b) A hypothetical machine has three instruction with their binary code: 8

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory
0011 = Load AC from I/O device
0111 = Store AC to I/O device

In these cases, the 12-bit address identifies a particular I/O along with memory locations. Show the program execution only drawing registers, buffers of I/O devices and memory contents in hexadecimal for the following program:

i. Load AC from I/O device 5
ii. Add content of memory location 940
iii. Store AC to device 6
iv. Store the I/O device address (where final result was stored) to memory location 941

[Hints: You should follow the instruction cycle state diagram to complete the program execution. Also assume I/O device 5 has the value of 3 and the memory location 940 contains a value of 2.]

c) Define following terms: 5

i. XU
ii. RC delay
iii. ISR
iv. Thrashing
v. Sense Amplifier

2. a) What happens when a check bit rather than a data bit is in error? How many check bits are needed if the Hamming error correction code is used to correct single bit and detect double bits errors in a 1024-bit data word? Justify your answer. 5

b) Draw the structure of the IAS computer figuring out its all major components proposed by von Newmann. Also quote the key points from his proposal based on what this structure was outlined. 10

c) Consider a machine with a byte addressable main memory of $2^{16}$ bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. 10

i. How is a 16-bit memory address divided into tag, line number, and byte number?

ii. Into what line would each of the following byte addresses be stored?

0001 0001 0001 1011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010

iii. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

iv. How many total bytes of memory can be stored in the cache?

v. Why the tag is also stored in the cache?

3. a) Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 μs; level 2 contains 100,000 words and has an access time of 0.1 μs. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. For simplicity, we ignore the time required for the processor to determine whether the word is in level 1 or level 2. If 95% of the memory accesses are found in level 1, what is the average time to access a word? 5

b) Consider the following 20-bit data: 20

01010000111100111001

i. How many additional bits are required to develop an SEC-DED code for the data mentioned above?

ii. Develop the algebraic expression to calculate the check bits respectively.

iii. Develop an SEC-DED code and present all data and check bits properly following their layout.

iv. Show that your derived expressions will correctly identify an error in data bit 5.

4. a) Criticize different types of approaches to handle multiple interrupts concisely. 5

b) "The set associative mapped cache can be implemented as fully associative cache or direct mapped cache as well" – justify this statement. Draw figures if necessary. 7

c) Table 1 shows the execution times, in seconds, for five different benchmark programs on three machines: 13

Table 1: Execution time in seconds for different processors.

| Benchmark | Processor | | |
|---|---|---|---|
| | R | M | Z |
| E | 417 | 244 | 134 |
| F | 83 | 70 | 70 |
| H | 66 | 153 | 135 |
| I | 39,449 | 35,527 | 66,000 |
| K | 772 | 368 | 369 |

i. Compute the speed metric for each processor for each benchmark, normalized to machine ***R*** treating as the reference system. Compute the arithmetic mean value for each system.

ii. Repeat question (i) using M as the reference machine.

iii. Which machine is the slowest based on each of the preceding two calculations?

iv. Repeat the calculations of questions (i) and (ii) using the geometric mean. Which machine is the slowest based on the two calculations?