ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

**SEMESTER FINAL EXAMINATION** **SUMMER SEMESTER, 2018-2019**
**DURATION: 3 Hours** **FULL MARKS: 150**

# CSE 4205: Digital Logic Design

**Programmable calculators are not allowed. Do not write anything on the question paper.**
There are **8 (eight)** questions. Answer any **6 (six)** of them.
Figures in the right margin indicate marks.

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1. a) The state of a 12-bit register is 100010010111. What is its content if it represents: 10
   i. Three decimal digits in BCD?
   ii. Three decimal digits in the excess-3 code?
   iii. Three decimal digits in the 84-2-1 code?
   iv. A binary number?
   v. Three decimal digits in Gray code?

   b) Can you extend the number of inputs of NAND or NOR gates more than two as AND or OR gates? Justify your answer with proper explanation and circuit diagram. 5

   c) Prove the following theorems with proper justification: 10
   i. De Morgan
   ii. Absorption
   iii. Involution

2. a) What is digital system? If Boolean algebra is an algebraic structure defined by a set of elements, $B$ together with two binary operators, + and ·, briefly describe all Huntington postulates those are satisfied by this assumption. 8

   b) Implement the following Boolean function $F$, together with the don't care conditions $d$, using no more than two NOR gates: 10

$$F(A,B,C,D) = \Pi(0,1,3,5,6,7,8,9,11,13,15)$$
$$d(A,B,C,D) = \Pi(2,3,4,6,7,9,10,11,12,13,14,15)$$

   Assume that both the normal and complement inputs are available.

   c) What is the benefits of Universal gates? Implement NAND gates using NOR gates and NOR gates using NAND gates. 7

3. a) If $F_1$ and $F_2$ are two Boolean functions, prove that $F_1 + F_2$ contains the sum of the minterms of $F_1$ and $F_2$. 5

   b) Draw the multiple-level NOR and multiple-level NAND circuits for the following Boolean expression: 10

$$CD(B+C)A + (BC' + DE') + A(B+C+D) + ABC$$

   c) i. What are the differences between canonical and standard form? 10
   ii. Which form is preferable to implement a Boolean function in Design procedure? Justify your answer.
   iii. Which form can be derived from a function represented in truth table?

4. a) *Subtractor* is a combinational circuit that subtracts two numbers and produces their differences. Design the circuits of half subtractor and full subtractor following the Design procedure. 25

   b) If we increase the number of bits in binary numbers to be subtracted, binary ripple borrow subtractor will be required. Design a four bit binary ripple borrow subtractor.

   c) Borrow propagation time is a critical attribute in computational time to generate correct output. To reduce the borrow propagation time, borrow look-ahead logic is a mostly used technique. Now step by step design a Borrow look ahead generator logic for four bit subtractor.

d) When we perform the subtraction with paper and pencil, an underflow is not a problem. Underflow is a problem for digital systems because of limited storage space. Now design an Underflow detection that will identify the occurrence of an underflow.

5. a) *"A sequential circuit is specified by a time sequence of inputs, outputs, and internal states"* – justify this statement comparing with combinational circuit. 5

b) Briefly describe following counters with appropriate timing diagram: 10

i. Ring counter

ii. Johnson counter

c) Step by step perform "Analysis Procedure" for the following sequential circuit (Figure 1): 10

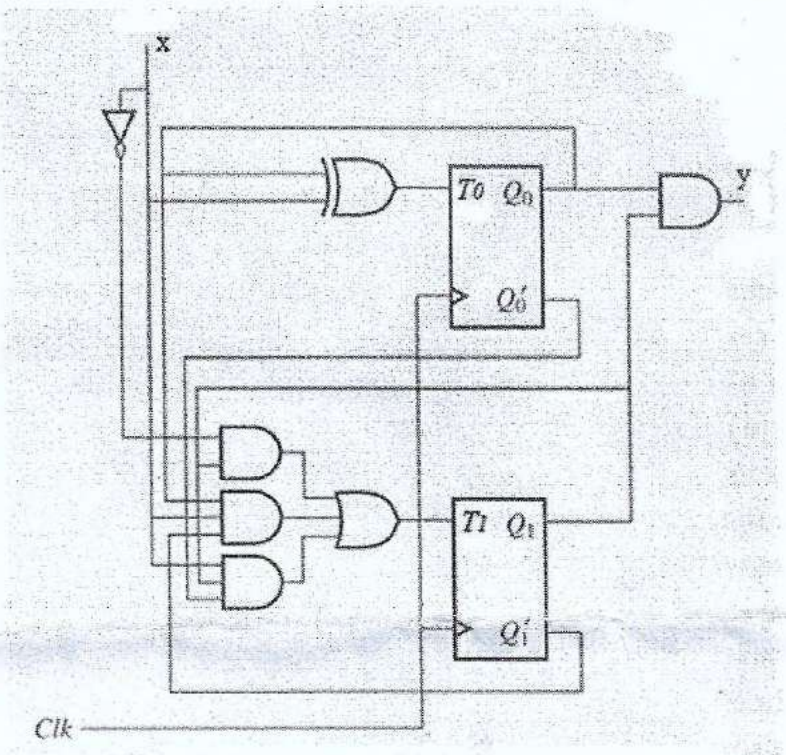


Figure 1: A sequential circuit.

6. a) Explain 'Race around' condition in sequential circuit with appropriate timing diagram and reasoning. Describe possible remedies to overcome this problem with necessary examples and diagrams. 10

b) i. Design a BCD Ripple up-down counter with negative edge triggered JK flip flops. 15

ii. Show the timing diagram for the above designed counter.

iii. What are the problems of the above designed counter?

7. a) What is the *Direct inputs* in sequential circuit? Explain their necessities and limitations with truth table. 5

b) Draw the circuit diagrams of following registers: 10

i. SISO ii. SIPO iii. PISO iv. PIPO

c) Draw the circuit diagram of a 4 bit universal shift register using SR flip flops. 10

8. a) i. Implement the following Boolean function, $F$ with a 16x1 multiplexer and external gates: 20

$$F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

ii. From question (i), can the function $F$ be implemented using a 4x1 multiplexer only? Justify your answer.

b) A digital system has a clock generator that produces pulses at a frequency of 80 MHz. Now in a particular component of that system, a clock is required with a cycle time of 50 ns. How can that customized clock be provided from the central clock generator? 5