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B.Sc. Engg. CSE 3rd Semester 07 March 2019 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION **WINTER SEMESTER, 2018-2019**

DURATION: 1 Hour 30 Minutes **FULL MARKS: 75**

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **4 (four)** questions. Answer any **3 (three)** of them.

Figures in the right margin indicate marks.

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1. a) What are the key distinguishing features of a microprocessor comparing with microcontroller? 7
   b) Draw a typical multicore configuration that supports PCIe and also mention different kinds of components those can be attached with PCIe. 8
   c) There are a few basic design elements that serve to classify and differentiate cache architectures. Among those key elements "Replacement Policy" and "Write Policy" are crucial as they are involved in writing on cache and main memory respectively. Briefly describe them mentioning their different techniques to implement. 10

2. a) Consider a system with three I/O devices: a printer, a disk, and a communications line, with increasing priorities of 2, 4, and 5, respectively. A user program begins at t = 0 taking 20 units time in total for completion. At t = 10, a printer interrupt occurs requiring total 10 units of time to be completed; at t = 15, another communication interrupt raises and also takes 10 units of time; a disk interrupt occurs at t = 20 taking same amount of time. How will a processor manage this multiple interrupts situation through a single interrupt pin serving all ISRs belonging to their respective interrupts? Suggest a solution with the help of a timing diagram how and when the interrupts will be enabled or disabled. 7
   b) Briefly characterize Amdahl's law and Little's Law with appropriate examples. Why are they necessary in measurement of computer performance? 6
   c) Write short notes on the following: 12
      i. Cache Coherency and its approaches
      ii. Comparison between RAM and ROM
      iii. An individual cell structure of SRAM and DRAM

3. a) The concept of a family of compatible computers was both novel and extremely successful. A customer with modest requirements and a budget to match could start with the relatively inexpensive model and later, if the customer's needs grew, he could upgrade to a faster machine with more memory without sacrificing the investment in already developed software. Which characteristics do you think that a family should follow to accomplish the preceding? 7
   b) Given the 11-bit data word 00100101010, generate the corresponding composite word for the Hamming code that corrects single errors and detects double errors. Show the steps of calculation. 6

c) Four benchmark programs are executed on three computers with the following results in Table 1: 12

Table 1: Execution time in second for Computer A, B, and C

	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100

The Table shows the execution time in seconds, with 100,000,000 instructions executed in each of the four programs. Calculate the MIPS values for each computer for each program. Then calculate the arithmetic and harmonic means of the MIPS values assuming equal weights for the four programs, and rank the computers based on arithmetic mean and harmonic mean.

4. a) A program consisting of a total of 300 instructions contains a 50-instruction loop that is executed 15 times. The processor contains a cache. Fetching and executing an instruction that is in the main memory requires 20 time units. If the instruction is found in the cache, fetching and executing it requires only 2 time units. Ignore operand data accesses. Assume that the cache is initially empty, that it is large enough to hold the loop, and that the program starts with all instructions in the main memory. 10

   i. Calculate the ratio of program execution time without the cache to execution time with the cache. This ratio is called the speedup due to the use of the cache.
   ii. Generalize part (i) by replacing the constants 300, 50, 15, 20, and 2 with the variables w, x, y, m, and c. Develop an expression for speedup.
   iii. For the values w = 300, x = 50, m = 20, and c = 2 what value of y results in a speedup of 5?

   b) For the hexadecimal main memory addresses 111111, 666666, BBBBBB, find out the following information, in hexadecimal format considering 64KB cache and 16MB main memory where line size and block size is 4 bytes each: 10

   i. Tag, Line, and Word values for a direct-mapped cache
   ii. Tag and Word values for an associative cache
   iii. Tag, Set, and Word values for a two-way set-associative cache

   c) Define the following terms: 5

   i. Hard Failure
   ii. EPROM
   iii. Flash Memory
   iv. Hamming Distance
   v. Syndrome