Homework 1

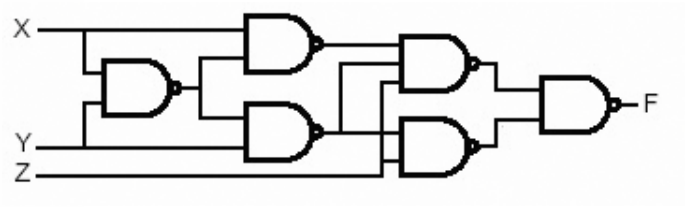
Name _____

SID _____

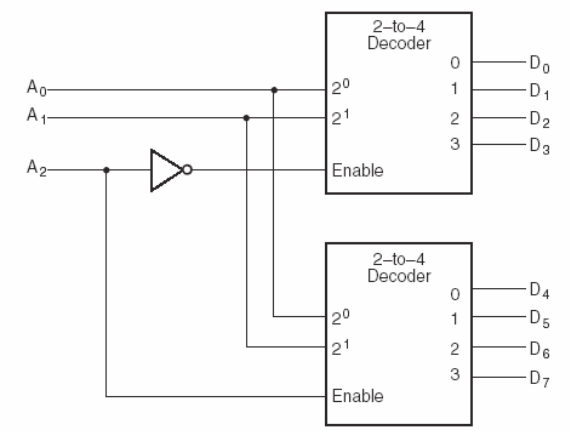
1. Using the structural Verilog module, below left, as a pattern, write a structural Verilog description of the circuit diagrammed on the right.

```
module decoder_2_to_4_st_v(E_n, A0, A1, D0_n, D1_n, D2_n, D3_n);
  input E_n, A0, A1;
  output D0_n, D1_n, D2_n, D3_n;

  wire A0_n, A1_n;
  not
    g0(A0_n, A0),
    g1(A1_n, A1);
    g2(E, E_n);

  nand
    g3(D0_n, A0_n, A1_n, E),
    g4(D1_n, A0, A1_n, E),
    g5(D2_n, A0_n, A1, E),
    g6(D3_n, A0,A1, E);

endmodule
```

Structural Verilog Description of a 2-to-4 Line Decoder

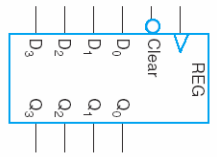


2. Write a structural Verilog description of the circuit diagrammed below. Assume the name and port list for the 2-to-4 decoders is as follows: `dec_2to4 (input [1:0] D, input Enable, output [3:0] Y);`



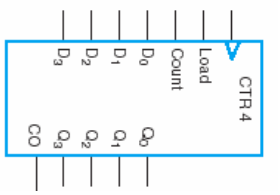
A 3-to-8 Decoder Constructed with Two 2-to-4 Decoders

3. Include a two-input AND gate with the register shown on the right. Connect the AND gate output to the clock input of the register. One input of the AND gate comes from the "master clock." The other input of the AND gate provides a parallel load control. Explain the operation of the modified register.

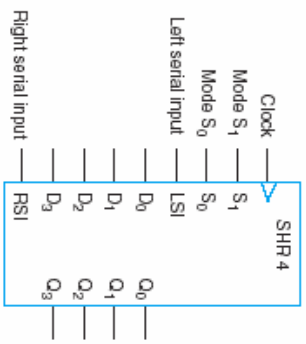


4. The content of a four-bit shift register is initially 1101. The register is shifted six times to the right with the serial input being 101101. You are to show the contents of the register **after each** shift

5. Create a detailed schematic diagram for a 16-bit binary counter with parallel load using four "instances" of the 4-bit binary counter shown below. You must show **all connections** for **all inputs and outputs**.



6. Create a detailed schematic diagram for an 8-bit bidirectional shift register with parallel load using two "instances" of the 4-bit bidirectional shift register shown in the diagram to the right. You must show **all connections** for **all inputs and outputs**.



7. The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

(a) 2K X 16; **(b) 64K X 8**; **(c) 16M X 32**; **(d) 4G X 16**.

8. Specify the number of bytes that can be stored in the memories list in problem 7.

9. **(a)** How many **32K X 8** RAM chips are needed to provide a memory system of **1M X 32**?
(b) How many lines of the address must be used to access **1M X 32**?
(c) How many of these lines are connected to the address inputs of all chips?
(d) How many lines must be decoded for the RAM chip select inputs?
(e) Specify the size of the "bank select" decoder.

10. **Use** the Xilinx tools to compile and simulate the behavioral description of the 4-bit adder shown below (adder_4.v). Your Xilinx Simulator stimulus must include at least 8 different combinations for inputs A, B and C0, displaying all the inputs and outputs. **Print out the results of the Simulator waveforms**.

```
module adder_4_b_v(A, B, C0, S, C4);
   input [3:0] A, B;
   input C0;
   output [3:0] S ;
   output C4;

   assign {C4, S } = A + B + C0;
endmodule
```

Behavioral Description of a 4-Bit Adder Using Verilog

Note: Do your work on separate sheets of paper. You are to staple all of your work together, using these sheets as your cover sheets.