Computer Architecture Lab

Lab13 – Week #13

MPLAB Media Processing Laboratory

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Write configuration file

- To seek help, type the following command
  - ./sim-cache -h

The cache config parameter <config> has the following format:

<name>:<nsets>:<bsize>:<assoc>:<repl>

<name> - name of the cache being defined
<nsets> - number of sets in the cache
<bsize> - block size of the cache
<assoc> - associativity of the cache
<repl> - block replacement strategy, 'l'-LRU, 'f'-FIFO, 'r'-random

Examples: -cache:dl1 dl1:4096:32:1:l
-dtlb dtlb:128:4096:32:r

Simulation procedure

1. cd simplesim-3.0

```
mpl@mpl-virtual-machi
mpl@mpl-virtual-machine:~$ cd simplesim-3.0/
mpl@mpl-virtual-machine:~/simplesim-3.0$
```

2. Cache setting : gedit ./config/mycache.cfg

Open — mycache.cfg — ~/simplesim-3.0/config

```
1 -cache:il1 il1:32:16:1:l      #Instruction L1 cache
2
3 -cache:dl1 none               #Data L1 cache
4 -cache:il2 il2:256:64:1:l     #Instruction L2 cache
5 -cache:dl2 none               #Data L2 cache
6 -tlb:itlb none                #Instruction TLB
7 -tlb:dtlb none                #Data TLB
```

3. Check .trace file

```
sim: ** simulation statistics **
sim_num_insn                362765 # total number of instructions executed
sim_num_refs                104761 # total number of loads and stores executed
sim_elapsed_time                 1 # total simulation time in seconds
sim_inst_rate          362765.0000 # simulation speed (in insts/sec)
il1.accesses                362765 # total number of accesses
il1.hits                    247961 # total number of hits
il1.misses                  114804 # total number of misses
il1.replacements            114772 # total number of replacements
il1.writebacks                   0 # total number of writebacks
il1.invalidations                0 # total number of invalidations
il1.miss_rate               0.3165 # miss rate (i.e., misses/ref)
il1.repl_rate               0.3164 # replacement rate (i.e., repls/ref)
il1.wb_rate                 0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                0.0000 # invalidation rate (i.e., invs/ref)
il2.accesses                114804 # total number of accesses
il2.hits                    105675 # total number of hits
il2.misses                    9129 # total number of misses
il2.replacements              8887 # total number of replacements
il2.writebacks                   0 # total number of writebacks
il2.invalidations                0 # total number of invalidations
il2.miss_rate               0.0795 # miss rate (i.e., misses/ref)
il2.repl_rate               0.0774 # replacement rate (i.e., repls/ref)
```

Simulation example (1/3)

- Unified vs splits
- Block size = 16, Associativity = 1
- Simulate the performance of the cache under the following condition
  - ✓ ./sim-cache –config configfile path application path
  - ✓ Ex) ~/simplesim-3.0/sim-cache -config ~/simplesim-3.0/config/mycache.cfg bin/go.little.ss 20 9 inputs/2stone9.in 2> traces/go.trace > results/go.out

# of Sets	Unified cache Miss rate	Unified cache AMAT	Split cache		Split cache AMAT
			Inst. Miss rate	Data Miss rate	
64					
128					
256					
512					

Simulation example (2/3)

- Unified cache
  - ✓ # of sets = 64

Open ~/simplesim-3.0/config/mycache.cfg

```
1 -cache:il1 il1:64:16:1:l
2
3 -cache:dl1 none
4 -cache:il2 none
5 -cache:dl2 none
6 -tlb:itlb none
7 -tlb:dtlb none
```

- go.trace

```
92 sim: ** simulation statistics **
93 sim_num_insn              279322583 # total number of instructions executed
94 sim_num_refs              109094805 # total number of loads and stores executed
95 sim_elapsed_time                 11 # total simulation time in seconds
96 sim_inst_rate          25392962.0909 # simulation speed (in insts/sec)
97 il1.accesses              279322583 # total number of accesses
98 il1.hits                  192235384 # total number of hits
99 il1.misses                 87087199 # total number of misses
100 il1.replacements          87087135 # total number of replacements
101 il1.writebacks                   0 # total number of writebacks
102 il1.invalidations                 0 # total number of invalidations
103 il1.miss_rate                0.3118 # miss rate (i.e., misses/ref)
104 il1.repl_rate                0.3118 # replacement rate (i.e., repls/ref)
```

Simulation example (3/3)

- m88ksim.trace

```
71 sim: ** simulation statistics **
72 sim_num_insn                29241863 # total number of instructions executed
73 sim_num_refs                 8043271 # total number of loads and stores executed
74 sim_elapsed_time                   1 # total simulation time in seconds
75 sim_inst_rate           29241863.0000 # simulation speed (in insts/sec)
76 il1.accesses               29241863 # total number of accesses
77 il1.hits                   26057273 # total number of hits
78 il1.misses                  3184590 # total number of misses
79 il1.replacements            3184526 # total number of replacements
80 il1.writebacks                    0 # total number of writebacks
81 il1.invalidations                  0 # total number of invalidations
82 il1.miss_rate                 0.1089 # miss rate (i.e., misses/ref)
83 il1.repl_rate                 0.1089 # replacement rate (i.e., repls/ref)
```

- swim.trace

```
71 sim: ** simulation statistics **
72 sim_num_insn                 326909 # total number of instructions executed
73 sim_num_refs                 122720 # total number of loads and stores executed
74 sim_elapsed_time                   1 # total simulation time in seconds
75 sim_inst_rate            326909.0000 # simulation speed (in insts/sec)
76 il1.accesses                 326909 # total number of accesses
77 il1.hits                     211692 # total number of hits
78 il1.misses                   115217 # total number of misses
79 il1.replacements             115153 # total number of replacements
80 il1.writebacks                    0 # total number of writebacks
81 il1.invalidations                  0 # total number of invalidations
82 il1.miss_rate                 0.3524 # miss rate (i.e., misses/ref)
83 il1.repl_rate                 0.3522 # replacement rate (i.e., repls/ref)
```

Simulation example 2 (1/2)

- Unified cache
  - ✓ # of sets = 128

Open ▾ mycache.cfg ~/simplesim-3.0/config

```
1 -cache:il1 il1:128:16:1:l
2
3 -cache:dl1 none
4 -cache:il2 none
5 -cache:dl2 none
6 -tlb:itlb none
7 -tlb:dtlb none
```

- go.trace

```
92 sim: ** simulation statistics **
93 sim_num_insn              279322583 # total number of instructions executed
94 sim_num_refs              109094805 # total number of loads and stores executed
95 sim_elapsed_time                 11 # total simulation time in seconds
96 sim_inst_rate          25392962.0909 # simulation speed (in insts/sec)
97 il1.accesses              279322583 # total number of accesses
98 il1.hits                  207878802 # total number of hits
99 il1.misses                 71443781 # total number of misses
100 il1.replacements          71443653 # total number of replacements
101 il1.writebacks                   0 # total number of writebacks
102 il1.invalidations                 0 # total number of invalidations
103 il1.miss_rate                0.2558 # miss rate (i.e., misses/ref)
104 il1.repl_rate                0.2558 # replacement rate (i.e., repls/ref)
```

Simulation example 2 (2/2)

- m88ksim.trace

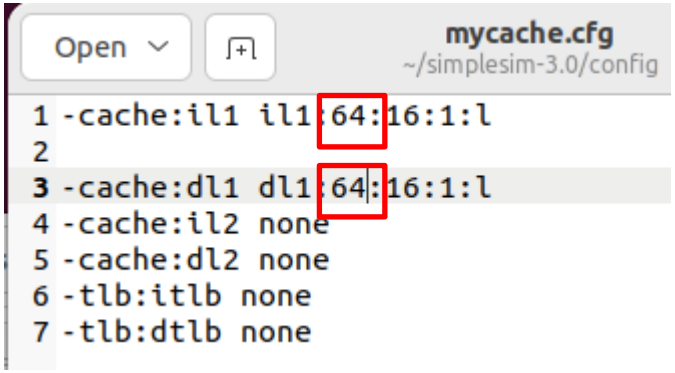
```
71 sim: ** simulation statistics **
72 sim_num_insn                29241863 # total number of instructions executed
73 sim_num_refs                 8043271 # total number of loads and stores executed
74 sim_elapsed_time                   1 # total simulation time in seconds
75 sim_inst_rate           29241863.0000 # simulation speed (in insts/sec)
76 il1.accesses               29241863 # total number of accesses
77 il1.hits                   28623226 # total number of hits
78 il1.misses                   618637 # total number of misses
79 il1.replacements            618509 # total number of replacements
80 il1.writebacks                   0 # total number of writebacks
81 il1.invalidations                0 # total number of invalidations
82 il1.miss_rate                0.0212 # miss rate (i.e., misses/ref)
83 il1.repl_rate                0.0212 # replacement rate (i.e., repls/ref)
```

- swim.trace

```
71 sim: ** simulation statistics **
72 sim_num_insn                 326909 # total number of instructions executed
73 sim_num_refs                 122720 # total number of loads and stores executed
74 sim_elapsed_time                   1 # total simulation time in seconds
75 sim_inst_rate            326909.0000 # simulation speed (in insts/sec)
76 il1.accesses                 326909 # total number of accesses
77 il1.hits                     235519 # total number of hits
78 il1.misses                    91390 # total number of misses
79 il1.replacements              91262 # total number of replacements
80 il1.writebacks                   0 # total number of writebacks
81 il1.invalidations                0 # total number of invalidations
82 il1.miss_rate                0.2796 # miss rate (i.e., misses/ref)
83 il1.repl_rate                0.2792 # replacement rate (i.e., repls/ref)
```

Simulation example 3 (1/4)

- Split cache
  - ✓ # of sets = 64



- in .trace file

```
18 # -config                    # load configuration from a file
19 # -dumpconfig                # dump configuration to a file
20 # -h                     false # print help message
21 # -v                     false # verbose operation
22 # -d                     false # enable debug message
23 # -i                     false # start in Dlite debugger
24 -seed                       1 # random number generator seed (0 for timer seed)
25 # -q                     false # initialize and terminate immediately
26 # -chkpt                 <null> # restore EIO trace execution from <fname>
27 # -redir:sim             <null> # redirect simulator output to file (non-interactive only)
28 # -redir:prog            <null> # redirect simulated program output to file
29 -nice                       0 # simulator scheduling priority
30 -max:inst                   0 # maximum number of inst's to execute
31 -cache:dl1       dl1:64:16:1:l # l1 data cache config, i.e., {<config>|none}
32 -cache:dl2               none # l2 data cache config, i.e., {<config>|none}
33 -cache:il1       il1:64:16:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2|none}
34 -cache:il2               none # l2 instruction cache config, i.e., {<config>|dl2|none}
35 -tlb:itlb                none # instruction TLB config, i.e., {<config>|none}
36 -tlb:dtlb                none # data TLB config, i.e., {<config>|none}
37 -flush                 false # flush caches on system calls
38 -cache:icompress       false # convert 64-bit inst addresses to 32-bit inst equivalents
39 # -pcstat               <null> # profile stat(s) against text addr's (mult uses ok)
```

Simulation example 3 (2/4)

- go.trace

```
 92 sim: ** simulation statistics **
 93 sim_num_insn              279322583 # total number of instructions executed
 94 sim_num_refs              109094805 # total number of loads and stores executed
 95 sim_elapsed_time                 13 # total simulation time in seconds
 96 sim_inst_rate          21486352.5385 # simulation speed (in insts/sec)
 97 il1.accesses              279322583 # total number of accesses
 98 il1.hits                  192235384 # total number of hits
 99 il1.misses                 87087199 # total number of misses
100 il1.replacements           87087135 # total number of replacements
101 il1.writebacks                    0 # total number of writebacks
102 il1.invalidations                 0 # total number of invalidations
103 il1.miss_rate                0.3118 # miss rate (i.e., misses/ref)
104 il1.repl_rate                0.3118 # replacement rate (i.e., repls/ref)
105 il1.wb_rate                   0.0000 # writeback rate (i.e., wrbks/ref)
106 il1.inv_rate                  0.0000 # invalidation rate (i.e., invs/ref)
107 dl1.accesses              109434718 # total number of accesses
108 dl1.hits                   91333093 # total number of hits
109 dl1.misses                 18101625 # total number of misses
110 dl1.replacements           18101561 # total number of replacements
111 dl1.writebacks              6727957 # total number of writebacks
112 dl1.invalidations                 0 # total number of invalidations
113 dl1.miss_rate                0.1654 # miss rate (i.e., misses/ref)
114 dl1.repl_rate                0.1654 # replacement rate (i.e., repls/ref)
```

Simulation example 3 (3/4)

- m88ksim.trace

```
sim: ** simulation statistics **
sim_num_insn                29241863 # total number of instructions executed
sim_num_refs                 8043271 # total number of loads and stores executed
sim_elapsed_time                   1 # total simulation time in seconds
sim_inst_rate          29241863.0000 # simulation speed (in insts/sec)
il1.accesses                29241863 # total number of accesses
il1.hits                    26057273 # total number of hits
il1.misses                   3184590 # total number of misses
il1.replacements             3184526 # total number of replacements
il1.writebacks                     0 # total number of writebacks
il1.invalidations                  0 # total number of invalidations
il1.miss_rate                 0.1089 # miss rate (i.e., misses/ref)
il1.repl_rate                 0.1089 # replacement rate (i.e., repls/ref)
il1.wb_rate                   0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                  0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses                 8146536 # total number of accesses
dl1.hits                     6358885 # total number of hits
dl1.misses                   1787651 # total number of misses
dl1.replacements             1787587 # total number of replacements
dl1.writebacks                336209 # total number of writebacks
dl1.invalidations                  0 # total number of invalidations
dl1.miss_rate                 0.2194 # miss rate (i.e., misses/ref)
dl1.repl_rate                 0.2194 # replacement rate (i.e., repls/ref)
```

Simulation example 3 (4/4)

- swim.trace

```
71 sim: ** simulation statistics **
72 sim_num_insn                326909 # total number of instructions executed
73 sim_num_refs                122720 # total number of loads and stores executed
74 sim_elapsed_time                 1 # total simulation time in seconds
75 sim_inst_rate           326909.0000 # simulation speed (in insts/sec)
76 il1.accesses                326909 # total number of accesses
77 il1.hits                    211692 # total number of hits
78 il1.misses                  115217 # total number of misses
79 il1.replacements            115153 # total number of replacements
80 il1.writebacks                   0 # total number of writebacks
81 il1.invalidations                0 # total number of invalidations
82 il1.miss_rate                0.3524 # miss rate (i.e., misses/ref)
83 il1.repl_rate                0.3522 # replacement rate (i.e., repls/ref)
84 il1.wb_rate                  0.0000 # writeback rate (i.e., wrbks/ref)
85 il1.inv_rate                 0.0000 # invalidation rate (i.e., invs/ref)
86 dl1.accesses                124167 # total number of accesses
87 dl1.hits                    101746 # total number of hits
88 dl1.misses                   22421 # total number of misses
89 dl1.replacements             22357 # total number of replacements
90 dl1.writebacks                11653 # total number of writebacks
91 dl1.invalidations                0 # total number of invalidations
92 dl1.miss_rate                0.1806 # miss rate (i.e., misses/ref)
93 dl1.repl_rate                0.1801 # replacement rate (i.e., repls/ref)
```

Thank You