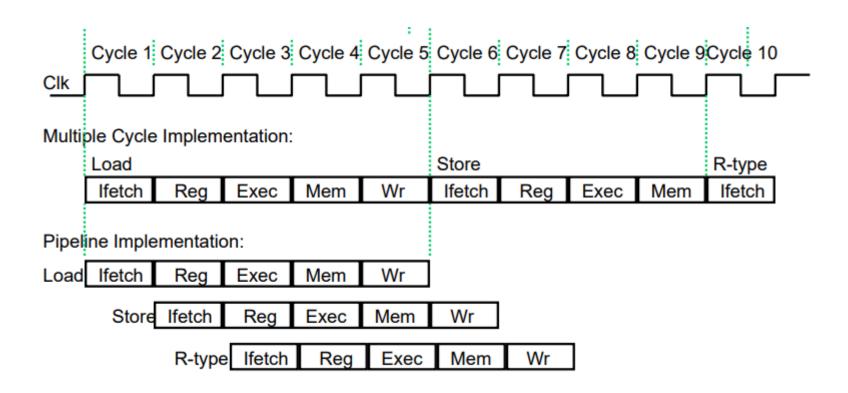
# Computer Architecture Lab

Lab10 – Week #10



### Pipeline

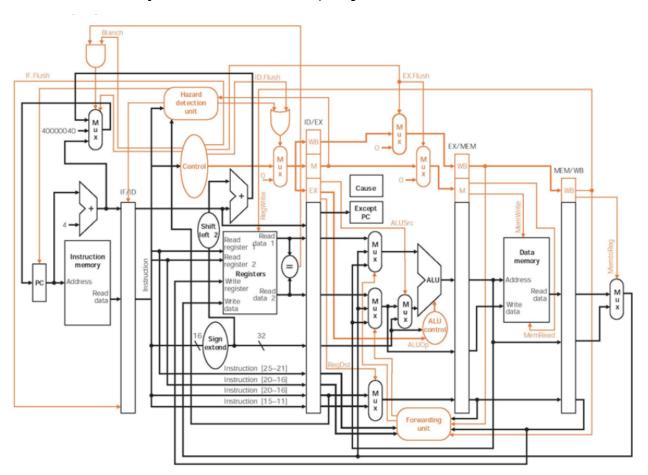
- Execute multiple instructions at the same time
- Sequential executions





## Pipeline

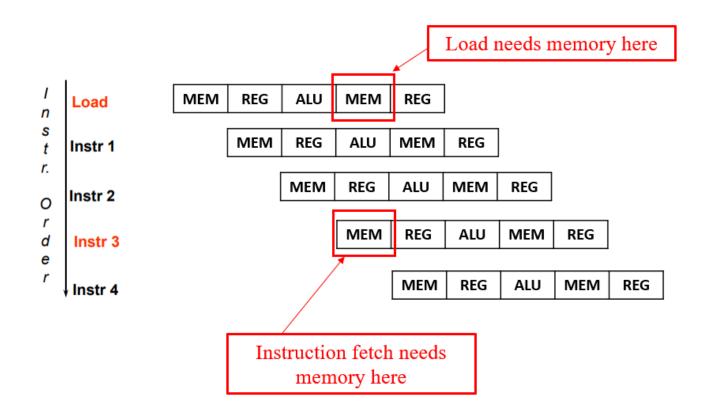
- ➤ Pipeline architecture
  - ✓ For reference only! (Not same as project circuit)





#### Structural hazards

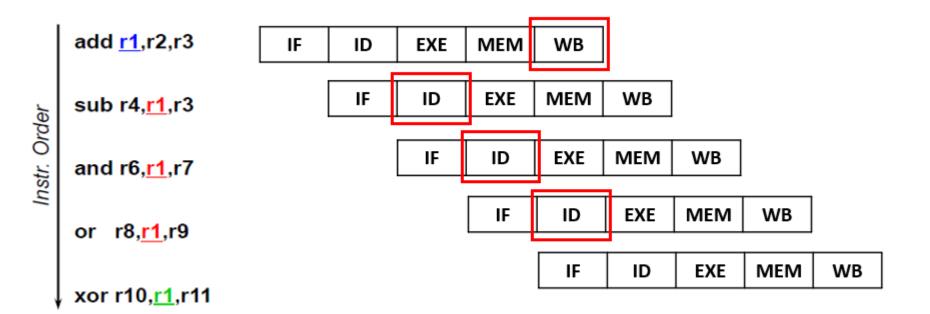
- > Different instructions are using the same resource at the same time
- > Ex) Case of single memory





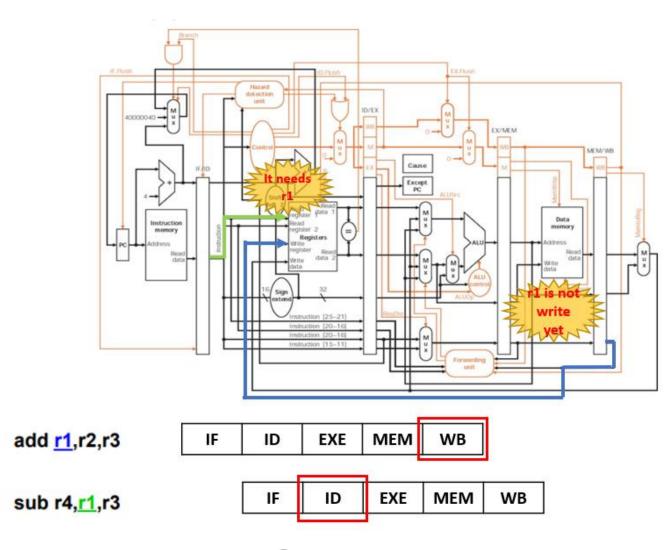
#### Data hazards

- Attempt to use item before it is ready
- > Instruction depends on result of prior instruction still in the pipeline





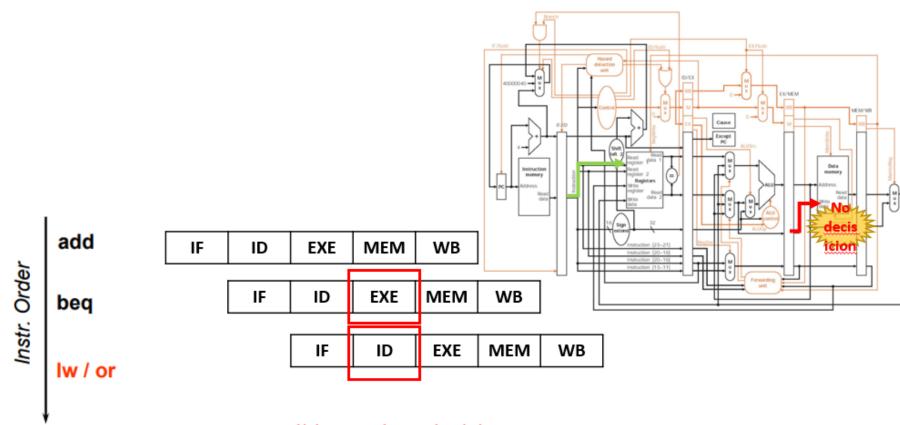
#### Data hazards





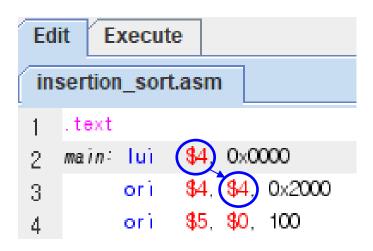
#### Control hazards

> Attempt to make a decision before condition is evaulated



It didn't make a decision yet





✓ Hazard occurred!



Fetch Decode ori Exe Mem

Mem

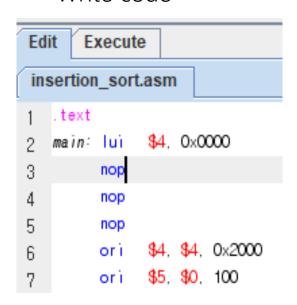
Wb



lui

#### By using MARS

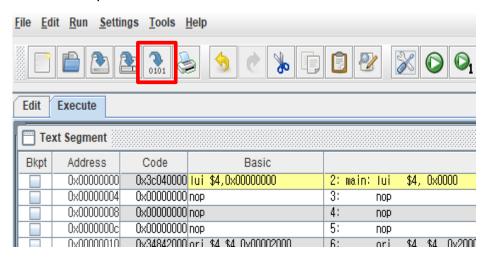
✓ Write code



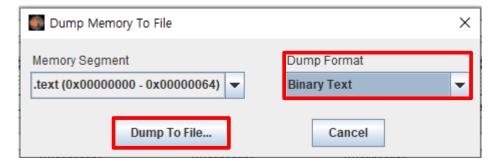
✓ Assemble current

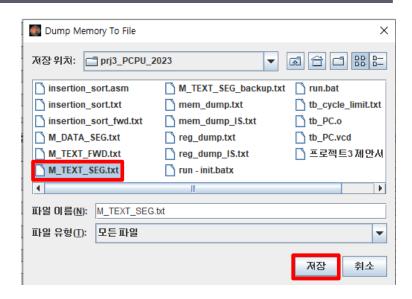


#### ✓ Dump



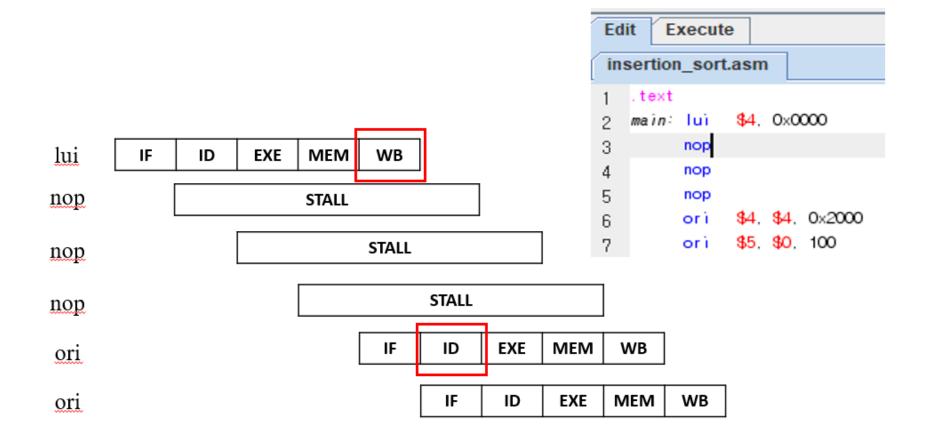
#### ✓ Dump to file





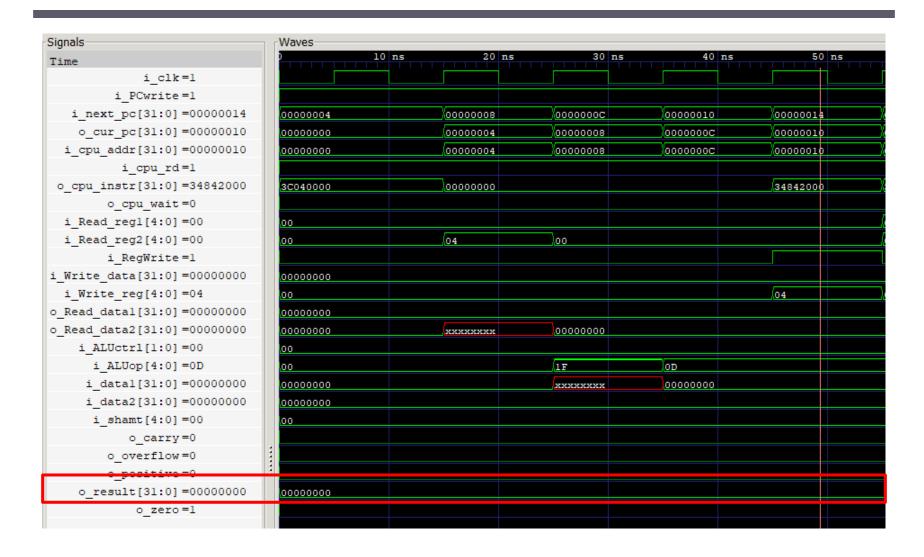
M\_TEXT\_SEG.txt - Windows 메모장







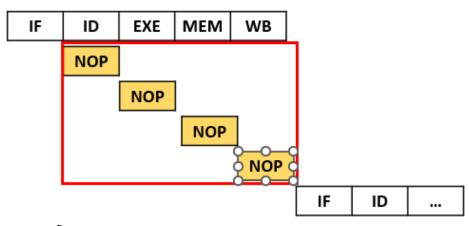
#### Simulation



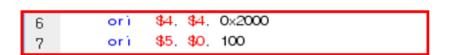


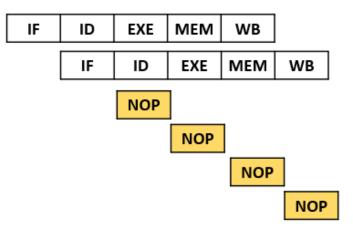
#### Remove NOP

"nop" is wasting time



➤ Remove unnecessary "NOP" to improve performance







#### Run.bat

- > Try to reduce cycle
- mem\_dump\_IS.txt and MEM\_DUMP.txt will compare each other to check operation rightly

```
| H020-3-1647-01: Computer Architecture | CE.KW.AC.KR | FST info: dumpfile tb_PC.vcd opened for output.
| Break signal: 0, # of Cycles: 7000
```

```
교합니다: mem_dump_IS.txt - MEM_DUMP.TXT
```



# Thank You