

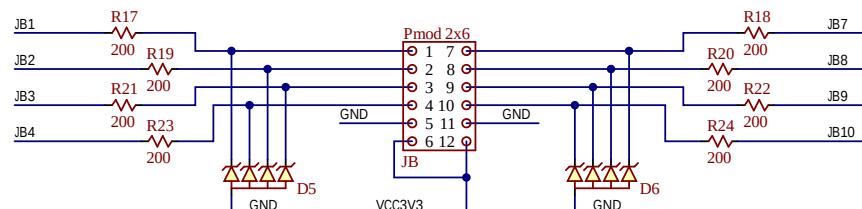
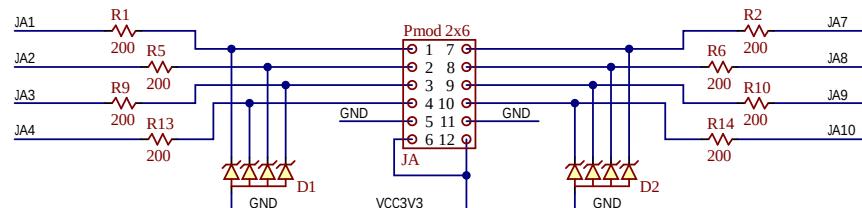
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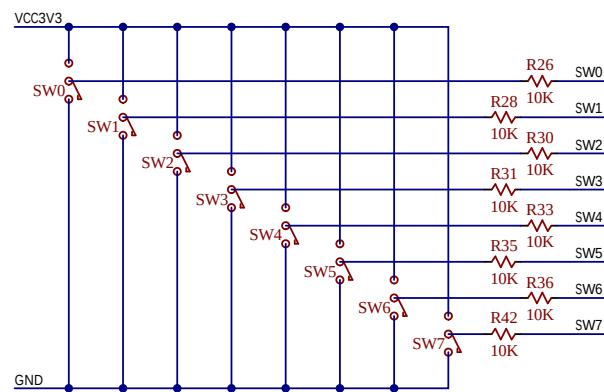
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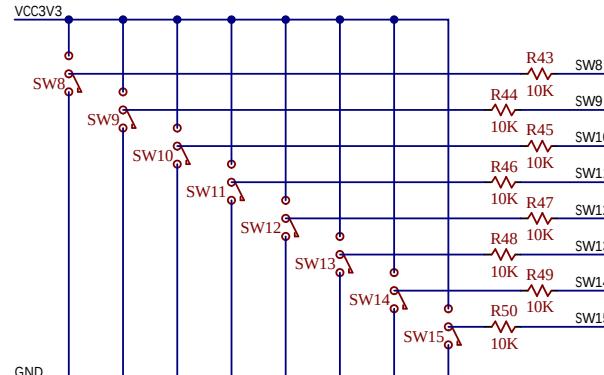
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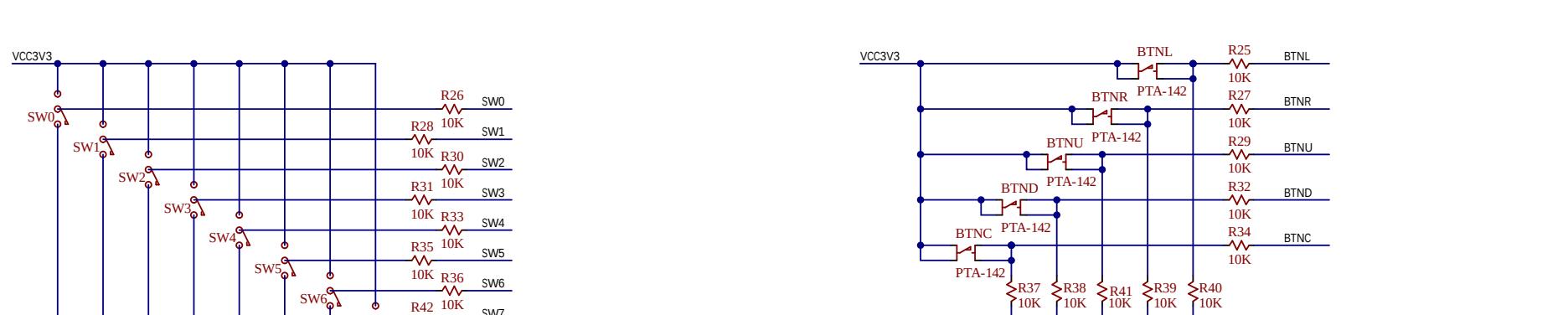
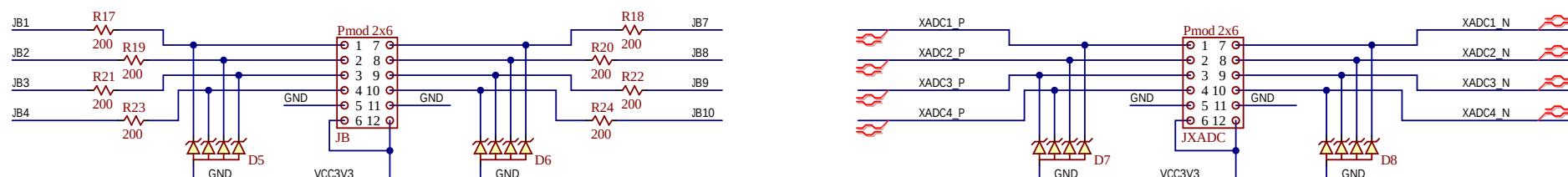
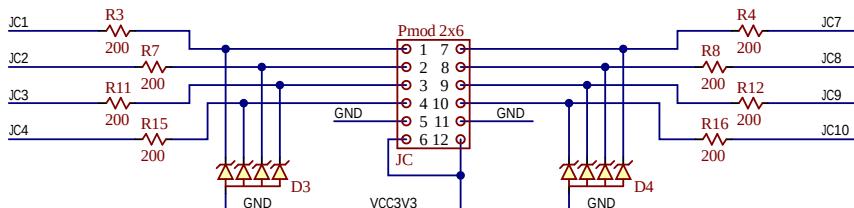
C



D

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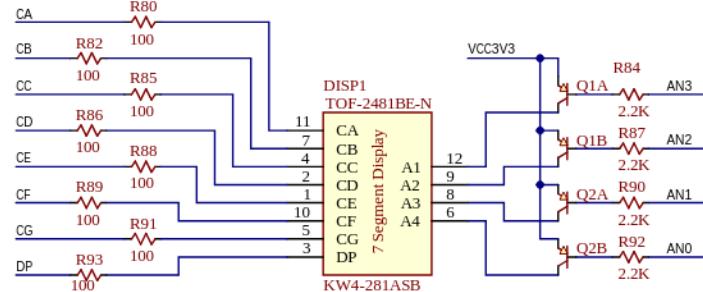
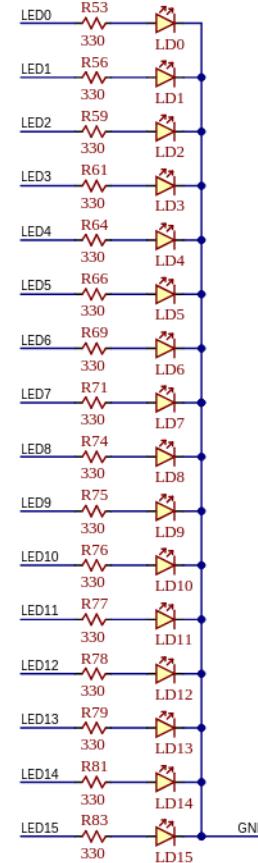
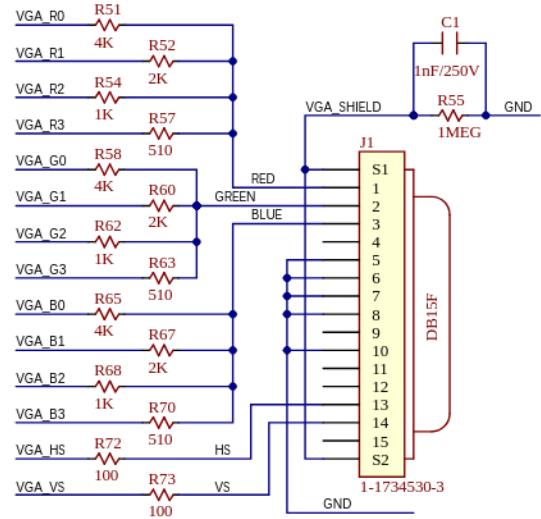
Circuit  
PMOD\_I/O  
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Author GMA  
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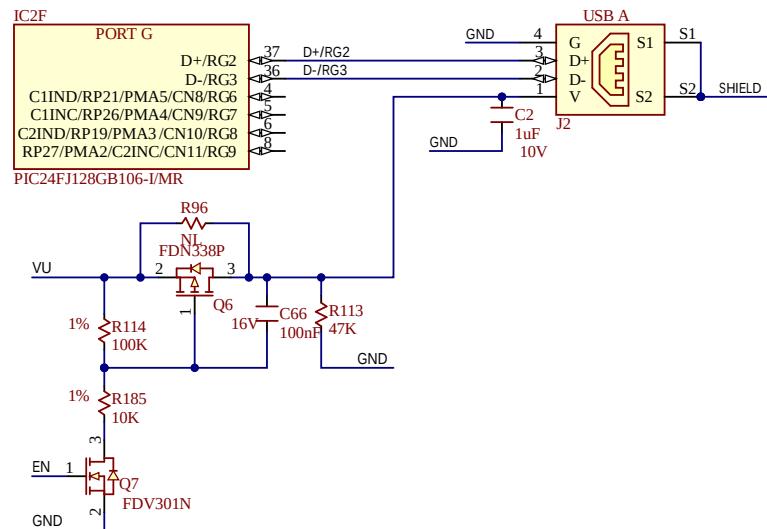
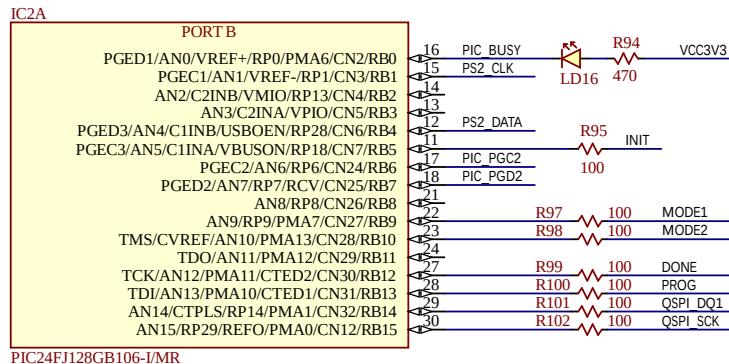
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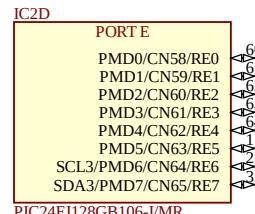
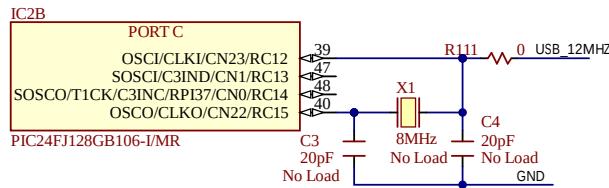
Title <h1>Basys 3</h1>	Rev D.1
Circuit 7 SEG, VGA, LEDs	
Doc# 500-183	
Engineer MTA	
Author GMA	
Date 2/5/2021	
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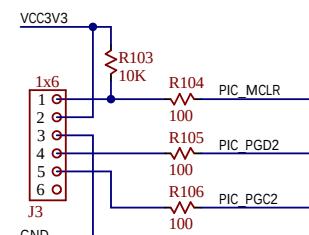
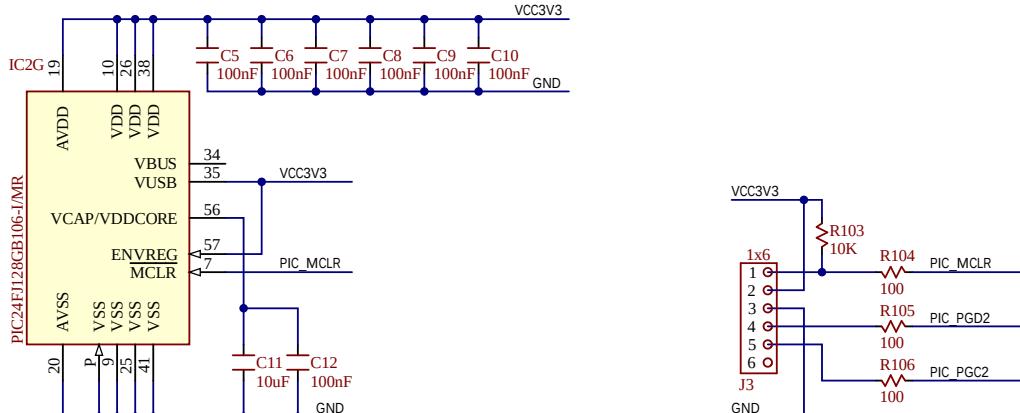
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B



C



D

A

B

C

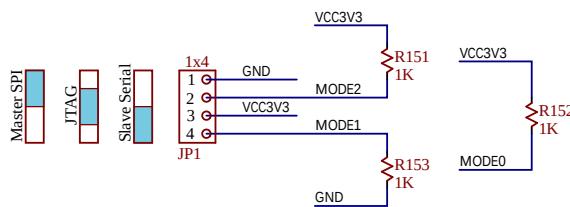
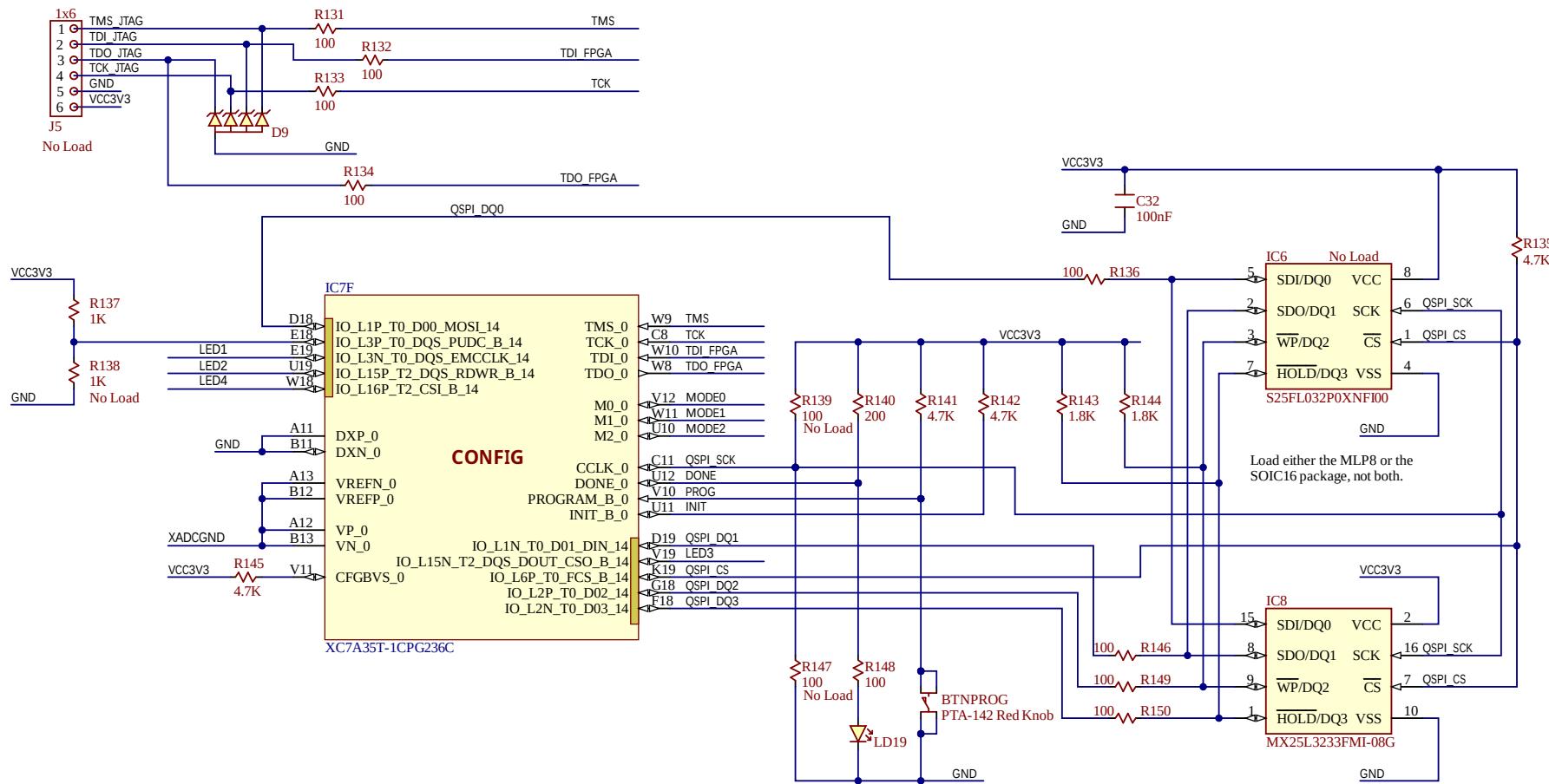
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IC7A

**BANK 14**

VGA_G3	D17	IO_0_14	IO_L4P_T0_D04_14	H19	VGA_R1
LED6	U14	IO_25_14	IO_L4N_T0_D05_14	H19	VGA_R0
			IO_L5P_T0_D06_14	H17	VGA_G1
			IO_L5N_T0_D07_14	G17	VGA_G2
			IO_L6N_T0_D08_VREF_14	H19	VGA_R2
			IO_L7P_T1_D09_14	H17	VGA_G0
			IO_L7N_T1_D10_14	H18	VGA_B3
			IO_L8P_T1_D11_14	H18	VGA_B1
			IO_L8N_T1_D12_14	H18	VGA_B2
			IO_L9P_T1_DQS_14	N18	VGA_B0
			IO_L9N_T1_DQS_D13_14	N19	VGA_R3
			IO_L10P_T1_D14_14	P19	VGA_H5
			IO_L10N_T1_D15_14	R19	VGA_VS
			IO_L11P_T1_SRCC_14	M18	JC2
			IO_L11N_T1_SRCC_14	M19	JC8
			IO_L12P_T1_MRCC_14	H17	JC7
			IO_L12N_T1_MRCC_14	K17	JC1
			IO_L13P_T2_MRCC_14	N17	JC3
			IO_L13N_T2_MRCC_14	P17	JC9
			IO_L14P_T2_SRCC_14	P18	JC4
			IO_L14N_T2_SRCC_14	R18	JC10
			IO_L16N_T2_A15_D31_14	Y19	BTNL
			IO_L17P_T2_A14_D30_14	T17	BTNR
			IO_L17N_T2_A13_D29_14	T18	BTNU
			IO_L18P_T2_A12_D28_14	T17	BTND
			IO_L18N_T2_A11_D27_14	V18	BTNC
			IO_L19P_T3_A10_D26_14	V16	SW1
			IO_L19N_T3_A09_D25_VREF_14	V17	SW0
			IO_L20P_T3_A08_D24_14	V16	SW2
			IO_L20N_T3_A07_D23_14	V17	SW3
			IO_L21P_T3_DQS_14	V15	SW5
			IO_L21N_T3_DQS_A06_D22_14	V15	SW4
			IO_L22P_T3_A05_D21_14	V13	SW7
			IO_L22N_T3_A04_D20_14	V14	SW6
			IO_L23P_T3_A03_D19_14	V15	LED5
			IO_L23N_T3_A02_D18_14	V16	LED0
			IO_L24P_T3_A01_D17_14	V13	LED8
			IO_L24N_T3_A00_D16_14	V14	LED7

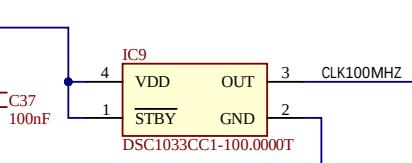
XC7A35T-1CPG236C

IC7B

**BANK 16**

IO_L6P_T0_16	A14	JB1
IO_L6N_T0_VREF_16	A15	JB7
IO_L11P_T1_SRCC_16	C15	JB9
IO_L11N_T1_SRCC_16	B15	JB3
IO_L12P_T1_MRCC_16	A16	JB2
IO_L12N_T1_MRCC_16	A17	JB8
IO_L13P_T2_MRCC_16	C16	JB10
IO_L13N_T2_MRCC_16	B16	JB4
IO_L14P_T2_SRCC_16	C17	PS2_CLK
IO_L14N_T2_SRCC_16	B17	PS2_DATA
IO_L19P_T3_16	B18	UART_RXD_IN
IO_L19N_T3_VREF_16	A18	UART_RXD_OUT

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IC7C

**BANK 34**

IO_L1P_T0_34	R2	SW15
IO_L1N_T0_34	J2	SW10
IO_L2P_T0_34	R3	SW11
IO_L2N_T0_34	T3	SW9
IO_L3P_T0_DQS_34	J1	SW14
IO_L3N_T0_DQS_34	U1	SW13
IO_L5P_T0_34	V2	SW8
IO_L5N_T0_34	W2	SW12
IO_L6P_T0_34	V3	LED9
IO_L6N_T0_VREF_34	W3	LED10
IO_L9P_T1_DQS_34	U3	LED11
IO_L9N_T1_DQS_34	U2	ANO
IO_L11P_T1_SRCC_34	U4	AN1
IO_L11N_T1_SRCC_34	V4	AN2
IO_L12P_T1_MRCC_34	W5	CLK100MHZ
IO_L12N_T1_MRCC_34	W4	AN3
IO_L13P_T2_MRCC_34	W7	CA
IO_L13N_T2_MRCC_34	W6	CB
IO_L14P_T2_SRCC_34	U8	CC
IO_L14N_T2_SRCC_34	V8	CD
IO_L16N_T2_34	U5	CE
IO_L19P_T3_34	V5	CF
IO_L19N_T3_VREF_34	U7	CG
	V7	DP

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IC7D

**BANK 35**

IO_L1P_T0_AD4P_35	G3	JA10
IO_L1N_T0_AD4N_35	G2	JA4
IO_L2P_T0_AD12P_35	H2	JA3
IO_L2N_T0_AD12N_35	H1	JA7
IO_L3P_T0_DQS_AD5P_35	J1	JA1
IO_L3N_T0_DQS_AD5N_35	K2	JA8
IO_L5P_T0_AD13P_35	I2	JA2
IO_L5N_T0_AD13N_35	I1	LED15
IO_L6N_T0_VREF_35	J3	XA1_P
IO_L7P_T1_AD6P_35	K3	XA1_N
IO_L7N_T1_AD6N_35	L3	XA2_P
IO_L8P_T1_AD14P_35	M3	XA2_N
IO_L8N_T1_AD14N_35	M2	XA3_P
IO_L9P_T1_DQS_AD7P_35	M1	XA3_N
IO_L9N_T1_DQS_AD7N_35	N2	XA4_P
IO_L10P_T1_AD15P_35	N1	XA4_N
IO_L10N_T1_AD15N_35	N3	LED13
IO_L12P_T1_MRCC_35	P3	LED12
IO_L12N_T1_MRCC_35	P1	LED14
IO_L19N_T3_VREF_35		

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IC7E

**BANK 216**

MGTRREF_216	C7	
MGTPTXP0_216	D2	
MGTPTXN0_216	D1	
MGTPTXP1_216	B2	
MGTPTXN1_216	A2	
MGTREFCLKP_216	B8	
MGTREFCLKN_216	A8	
MGTREFCLK0_216	B10	
MGTREFCLK1_216	A10	
MGTPRXP0_216	B4	
MGTPRXN0_216	B6	
MGTPRXP1_216	A4	
MGTPRXN1_216	A6	
		GND

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Title  
**Basys 3**

Circuit

FPGA BANKS

Doc# 500-183

Engineer MTA

Author GMA

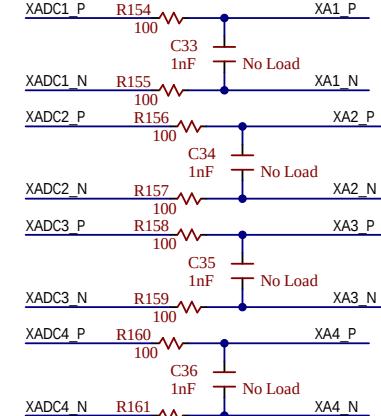
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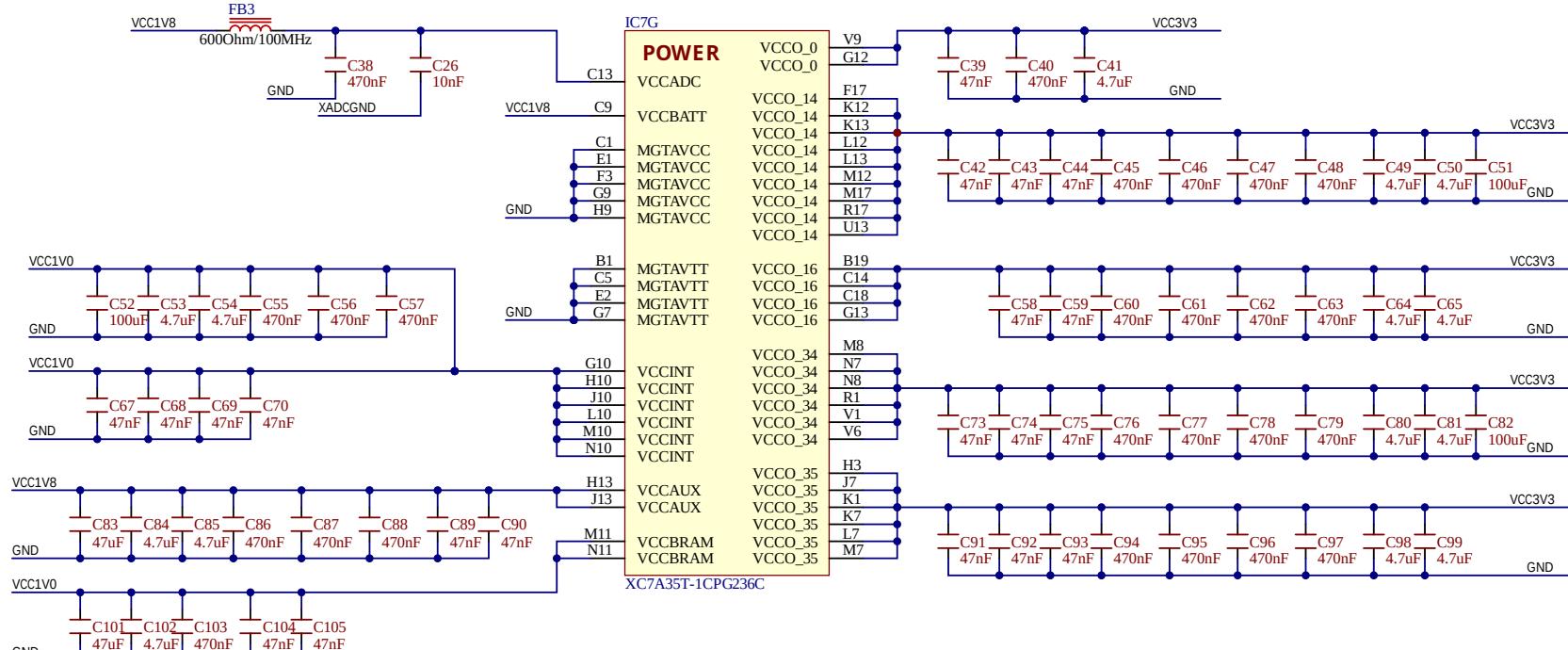
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Engineer	MTA
Author	GMA
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