Jesse Cho

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Education

Northwestern University **June 2027 (Expected)**
Bachelor of Science in Electrical Engineering *GPA: 3.97/4.00*

Washington University in St. Louis **Aug 2023 – May 2024**
Bachelor of Science in Electrical Engineering *GPA: 4.00/4.00*

Skills

Technical: Circuit Design and Analysis, Soldering, Oscilloscope, Digital Multimeter, Breadboard Prototyping
Software: Cadence Virtuoso Suite, MATLAB, Simulink, Git, Altium Designer, LabVIEW, LTspice, Microsoft Office Suite
Programming Languages: Python, C/C++, Java, LaTeX

Experience

Research Assistant **Oct 2024 – Present**
Bio-Inspired Sensors and Optoelectronics Lab (PI: Prof. Hooman Mohseni) *Northwestern University*

- Modeled six electrode arrangements and performed simulations in Cadence to determine their transfer functions
- Designed and simulated a single-transistor amplifier for AM modulation of neural signals, achieving a gain of 50
- Shadowed a grad student on the design, layout, and simulation of a VCO, gaining experience in analog design
- Presented research progress and deliverables in the weekly group meeting for neural sensing ASIC project

Research Assistant **May 2024 – Sept 2024**
Analog and Mixed-Signal IC Design Lab (PI: Prof. Suhwan Kim) *Seoul National University*

- Implemented a sensored sinusoidal control BLDC motor driver using ESP32 and C, reducing torque ripple by 45%
- Designed a simplified Field Oriented Control algorithm to reduce computational cost by 30%, simulated in Simulink
- Produced a 20-page technical report detailing the design process of the motor driver, presented to 8 engineers
- Measured performance of manufactured PCBs using an oscilloscope, ensuring accuracy of component datasheet

Projects

6T SRAM Bank | *Cadence Virtuoso Suite* **Feb 2025 - Mar 2025**

- Implemented a 4x4 SRAM bank featuring 6T SRAM cells, a sense amplifier, and bitline conditioning circuitry
- Developed a testbench for the SRAM bank and validated complete functional correctness and timing performance
- Optimized the area of the 6T SRAM cell layout to 0.7 μm2, similar to that of commercial IP cells in 65 nm

Audio Spectrum Visualizer | *ESP32, C++, Soldering* **Sep 2024 – Dec 2024**

- Designed and implemented an 8x8 LED matrix featuring transistors, shift registers, and analog RC filter banks
- Programmed LED animations in C++ on the ESP32, used Fast Fourier Transform to update the frequency spectrum

PiCar Rover | *Raspberry Pi, Python, OpenCV, Matplotlib* **Jan 2024 – May 2024**

- Built a rover controller with Python using camera data and OpenCV to automatically follow generated paths
- Simulated obstacle environments and implemented avoidance algorithms using ultrasonic sensors and Python
- Utilized Raspberry Pi platform for control and data collection from camera, ADC, and ultrasonic sensors via GPIO
- Implemented PID control to maintain desired speed of the rover and used Matplotlib to plot data for analysis

Buck Converter with Feedback | *LTspice, C++, Oscilloscope* **May 2024 – Aug 2024**

- Calculated and selected optimal component values, utilized LTspice to simulate and verify circuit performance
- Generated 100kHz frequency and 50% duty cycle PWM signal using an Arduino Nano with C++ to drive the MOSFET
- Extensively tested the DC-DC converter with an oscilloscope to verify operational reliability under varying loads