# Jesse Cho (조재현)

CONTACT Information 2420 Campus Drive 560-120A Evanston, IL 60201 +1 (314) 450 0375 jessecho2027@u.northwestern.edu http://chojesse.github.io

Research Interests

End-to-end design of analog and RF/mmWave electronic systems with custom silicon ICs for communication, sensing, and biomedical applications

EDUCATION

## Northwestern University

Evanston, IL June 2026

B.S. in Electrical Engineering

• GPA: 3.98/4.00

• Completing undergraduate degree in three years

Research Experience

#### **Querrey Simpson Institute for Bioelectronics**

Evanston, IL June 2025 – Present

Undergraduate Researcher, Northwestern University Advisors: Prof. John A. Rogers, Dr. Vasant Iyer

- Designed and taped out a bioresorbable DC-DC converter in TSMC 180 nm, integrating a low-voltage ring oscillator, phase shifter, and 4-stage charge pump to achieve 4x voltage gain
- Performed lithography and etching to fabricate dummy chips mimicking the top-metal sacrificial layer, characterized trench depth as a function of etch time using mechanical profilometry
- Designed a thermistor temperature-to-frequency converter PCB for integration with my charge pump, characterized it in an environmental chamber
- Designing an analog front-end for a bioresorbable, implantable ECG readout system using a capacitively-coupled chopper IA and SAR ADC

### **Bio-Inspired Sensors and Optoelectronics Lab**

Evanston, IL

Undergraduate Researcher, Northwestern University

Oct 2024 - Present

Advisor: Prof. Hooman Mohseni

- Designed and built an *in vitro* electrical phantom that mimics *in vivo* electrophysiological recording environments by generating controlled current dipoles in PBS for testing brain-computer interfaces
- Developed a forward model in Python to simulate extracellular potentials generated by cortical current dipoles from neural activity
- Collected frequency-dependent impedance data for five electrode types (bipolar, ECoG, EEG, EMG, MEA), fitted lumped-element models to the data, and characterized signal transfer from the electrode to the ASIC's input stage
- Designed and assembled PCBs required for measurement, including a voltage-follower buffer and an opto-isolator

### Analog and Mixed-Signal IC Design Lab

Summer Intern, Seoul National University Advisor: Prof. Suhwan Kim (in memoriam) Seoul, South Korea June 2024 – Sept 2024

- Implemented a proof-of-concept BLDC motor driver with sensored sinusoidal control using ESP32 and C++
- Designed a simplified Field-Oriented Control algorithm that runs on an 8-bit MCU with reduced computational cost, modeled in Simulink using ideal blocks
- Verified stable long-term operation of a PV energy harvesting system based on DCR current sensing using a PV array simulator, DC power analyzer, oscilloscope, and IR thermometer

#### **PRESENTATIONS**

"Design of a Bioresorbable DC-DC Converter in 180nm Silicon CMOS," Querrey Simpson Institute for Bioelectronics Summer 2025 Undergraduate/MS Symposium. Northwestern University, Evanston, IL, August 2025.

"Implementation of BLDC Motor Drivers and Algorithm Design for Simplified Field-Oriented Control," Analog and Mixed-Signal IC Design Lab Summer Internship Final Presentation. Seoul National University, Seoul, South Korea, September 2024.

SKILLS

**EDA Tools:** Cadence Virtuoso (Schematic XL, ADE Assembler/Explorer, Layout XL), Siemens Calibre (nmDRC, LVS, PEX), Altium Designer

**Microfabrication:** Reactive-ion Etching, Plasma Cleaner, Spinner, Mask Aligner, Profilometer (Optical and Stylus), Probe Station, Microscope

**Test Instruments:** Oscilloscope, Spectrum Analyzer, Lock-in Amplifier, DC Power Analyzer, Function Generator

Software: Simulink, LabVIEW, LTspice, SolidWorks, Microsoft Visio, Vim

**Programming Languages:** MATLAB, Python, C/C++, LATEX

Awards and Funding

Awarded KRW 2,000,000 stipend (approx. USD \$1400) from Analog and Mixed-Signal IC Design Lab, Seoul National University, Summer 2024

Dean's List, Washington University in St. Louis and Northwestern University, all terms attended, 2023 – 2025