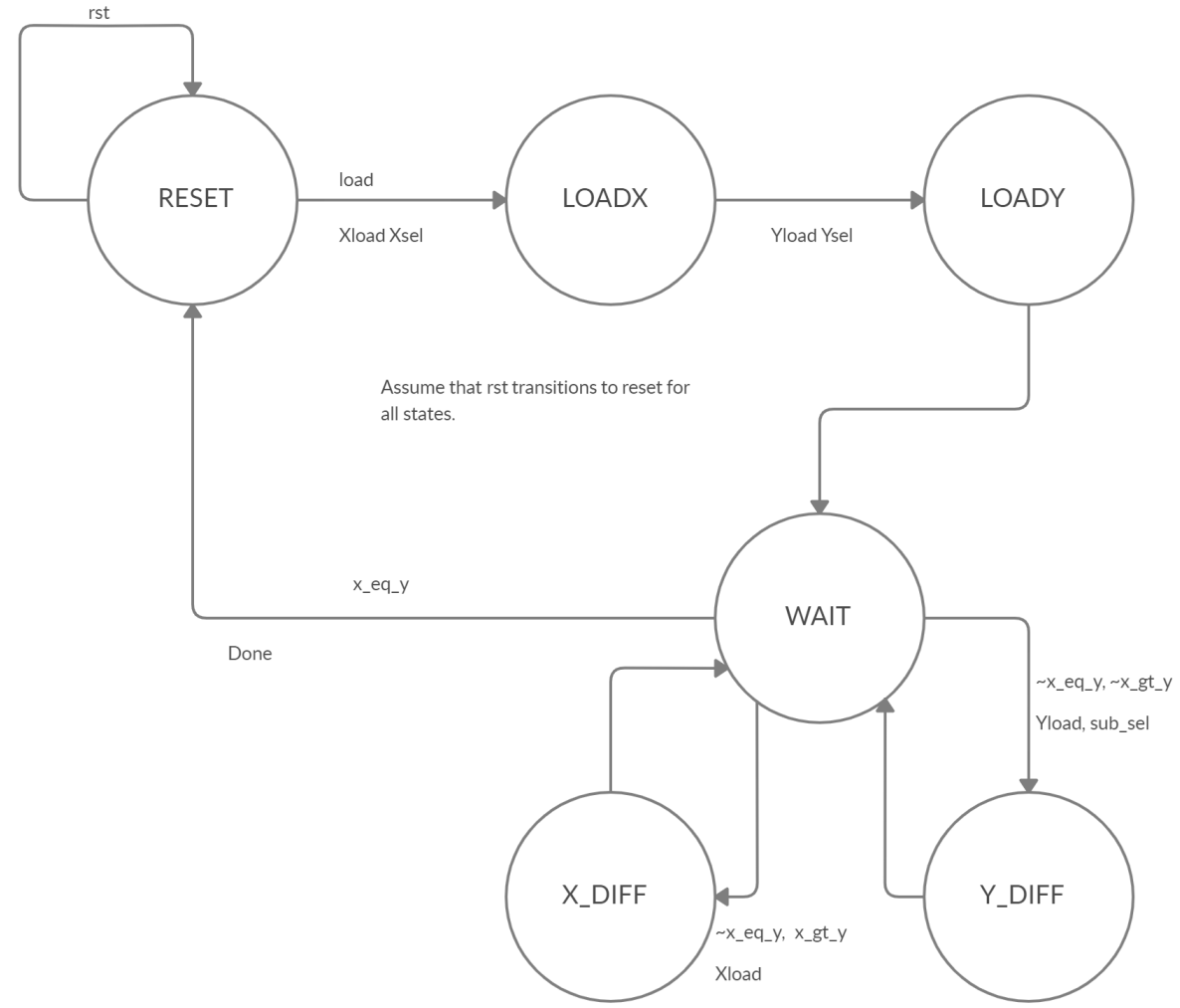
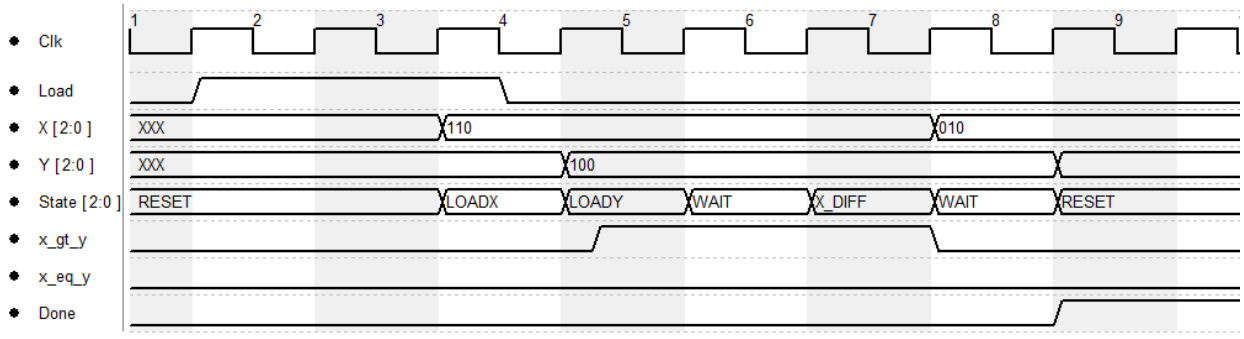
Cory Holt

ECE 440 H2





Problem 2.1

```
`timescale 1ns / 1ps
module SV_2_1
    logic a, b;
    initial begin
            a = 0; b = 1;
        #3  a = 1; b = 0;
        #3  b = 1;
        #2  a = 0;
        #3  a = 1; b = 0;
        #1  a = 0;
    end
    initial
        #16 $finish
endmodule
```

Problem 2.3

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
//////////////////////////////////////////////////////////////////////////////////
parameter WIDTH = 4;
module alu(
    input cIn,
    input logic [1:0] fn,
    input logic [WIDTH-1:0] a,
    input logic [WIDTH-1:0] b,
    output logic [WIDTH-1:0] out,
    output logic cOut,
    output logic N,
    output logic Z,
    output logic V
    );
    enum logic [1:0] {fn_add, fn_and, fn_or, fn_xor} op;

    always_comb
        unique case (fn)
            fn_add: begin
                    out = a + b + cIn;
                    N = out[WIDTH-1];
                    Z = (out == '0);
                    V = (a[WIDTH-1] ^~ b[WIDTH-1]) & (a[WIDTH-1] ^ out[WIDTH-1]);
                    cOut = out[WIDTH]
                    end
            fn_and: begin
                    out = a & b;
                    end
            fn_or:  begin
                    out = a | b;
                    end
            fn_xor: begin
                    out = a ^ b;
                    end
        endcase
   endmodule
```

Testbench code for alu

```
`timescale 1ns / 1ps
parameter WIDTH = 4
module alu_tb
    logic cIn,
    logic [1:0] fn,
    logic [WIDTH-1:0] a,
    logic [WIDTH-1:0] b,
    initial begin
            a = 4'b1111; b = 4'b0000; cIn = 1;
        #5  fn = 2'b00;
        #5  fn = 2'b01;
        #5  fn = 2'b10;
        #5  fn = 2'b11;
        #5  a = 4'b0101; b = 4'b0101; cIn = 0;
        #5  fn = 2'b00;
        #5  fn = 2'b01;
        #5  fn = 2'b10;
        #5  fn = 2'b11;
    end
    initial
        #3 $finish
endmodule
```