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Project 2 Brief Report

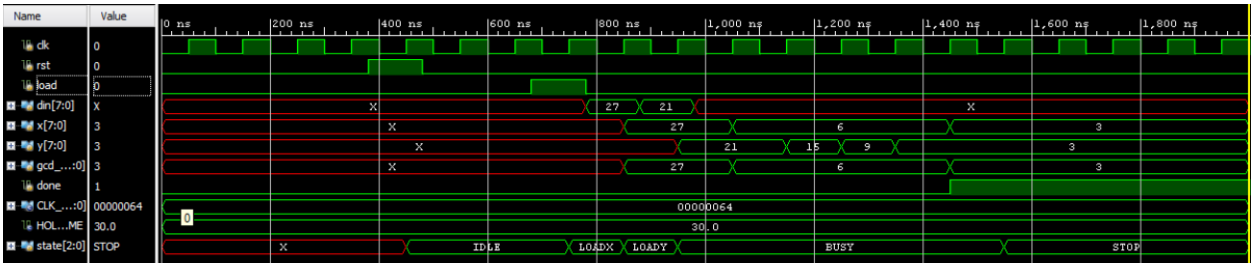
1-30-20

For the design of this project, I based my design primarily from the given SV code for the in-class designs. I altered the code where necessary to meet project specifications. Having a framework to base this project off of was very helpful in that it allowed me to mess with the code and see what worked and didn't work as I was implementing this design. I am still very unexperienced with SV, but I definitely feel like I have a much better understanding of the overall structure we should be following, and how modules interact with each other.

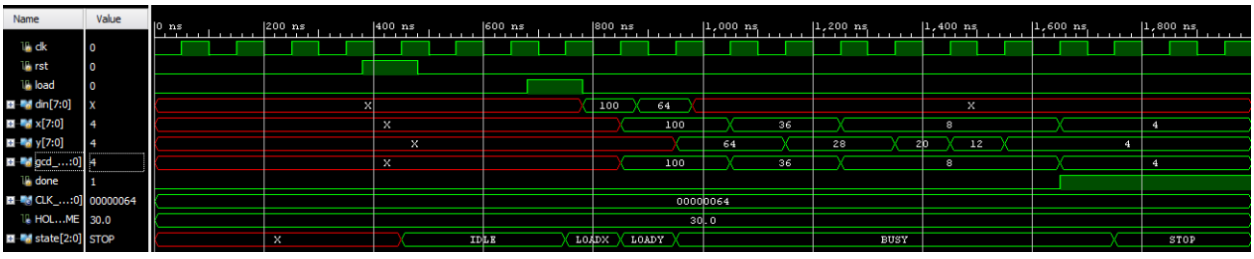
The first problem I struggled with was the syntax of SystemVerilog and use of the Vivado software. It is a bit of a hurdle to understand the file hierarchy and how Vivado understands that hierarchy. After I implemented the design into SV, I began debugging the design. I initially had a signal always being driven low and also trying to be driven high by a different portion of the module. The synthesis tool pointed this out and allowed me to fix the problem. After that, the synthesis report came back all green, so I moved on to check the behavioral sims. The simulations showed that the X register was not loading properly, and that my testbench was the culprit, as the data was being asserted too early for the registers to read it. After closer inspection, it turned out that a single missing semicolon after a #CLK_PRD statement was missing. This apparently caused it to not run the delay and my timing was off completely. Adding a semicolon resolved this problem and the core then behaved as expected.

**Behavioral Sims**

X = 27, Y = 21

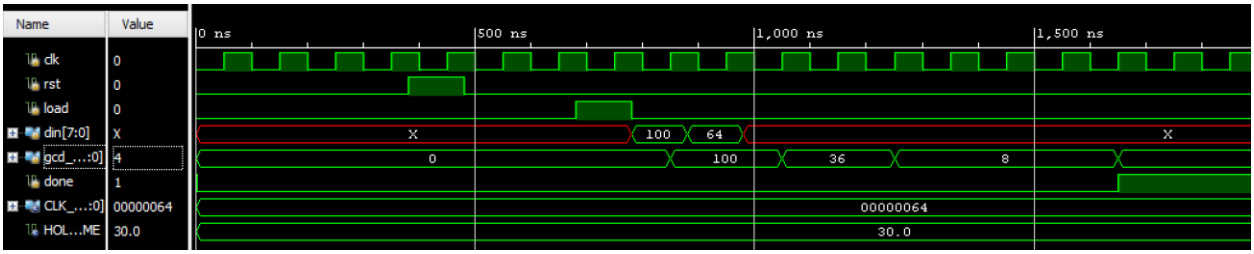



X = 100, Y = 64

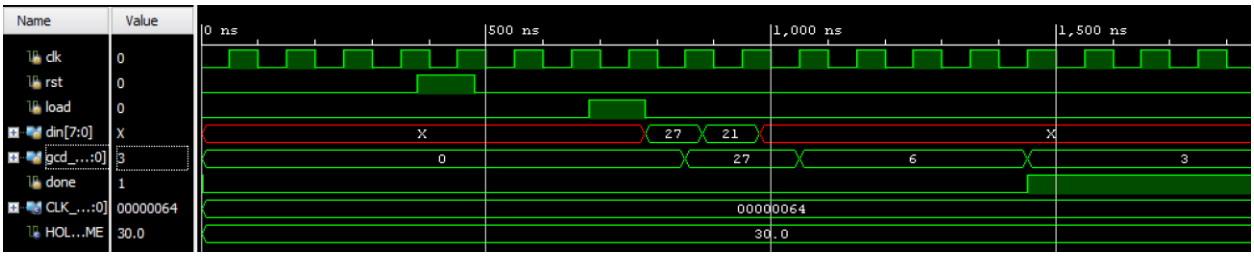


## Post Synthesis Sims

X = 100, Y = 64




X = 27, Y = 21




## Synthesis Report

```
#-----------------------------------------------------------

# Vivado v2016.4 (64-bit)

# SW Build 1756540 on Mon Jan 23 19:11:23 MST 2017

# IP Build 1755317 on Mon Jan 23 20:30:07 MST 2017

# Start of session at: Thu Jan 30 16:55:38 2020

# Process ID: 17164

# Current directory: D:/ECE 440/project2/project2.runs/synth_1

# Command line: vivado.exe -log gcd_core.vds -product Vivado -mode batch -messageDb
vivado.pb -notrace -source gcd_core.tcl

# Log file: D:/ECE 440/project2/project2.runs/synth_1/gcd_core.vds

# Journal file: D:/ECE 440/project2/project2.runs/synth_1\vivado.jou

#-----------------------------------------------------------

source gcd_core.tcl -notrace

Command: synth_design -top gcd_core -part xc7z010clg400-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7z010'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7z010'

INFO: Launching helper process for spawning children vivado processes
```

```
INFO: Helper process launched with PID 8012

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:08 . Memory
(MB): peak = 282.746 ; gain = 72.254

---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'gcd_core' [D:/ECE
440/project2/project2.srcs/sources_1/new/gcd_core.sv:23]

INFO: [Synth 8-638] synthesizing module 'dp' [D:/ECE
440/project2/project2.srcs/sources_1/new/dp.sv:23]

INFO: [Synth 8-256] done synthesizing module 'dp' (1#1) [D:/ECE
440/project2/project2.srcs/sources_1/new/dp.sv:23]

INFO: [Synth 8-638] synthesizing module 'fsm' [D:/ECE
440/project2/project2.srcs/sources_1/new/fsm.sv:21]

INFO: [Synth 8-155] case statement is not full and has no default [D:/ECE
440/project2/project2.srcs/sources_1/new/fsm.sv:34]

INFO: [Synth 8-256] done synthesizing module 'fsm' (2#1) [D:/ECE
440/project2/project2.srcs/sources_1/new/fsm.sv:21]

INFO: [Synth 8-256] done synthesizing module 'gcd_core' (3#1) [D:/ECE
440/project2/project2.srcs/sources_1/new/gcd_core.sv:23]

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:06 ; elapsed = 00:00:09 . Memory
(MB): peak = 319.203 ; gain = 108.711

---------------------------------------------------------------------------------


Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

|      |Item              |Errors |Warnings |Status |Description       |

+------+------------------+-------+---------+-------+------------------+

|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:10 .
Memory (MB): peak = 319.203 ; gain = 108.711

---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xc7z010clg400-1

INFO: [Project 1-570] Preparing netlist for logic optimization
```

```
Processing XDC Constraints

Initializing timing engine

Parsing XDC File [D:/ECE 440/project2/project2.srcs/constrs_1/new/constraint.xdc]

Finished Parsing XDC File [D:/ECE
440/project2/project2.srcs/constrs_1/new/constraint.xdc]

Completed Processing XDC Constraints


INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.


Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.020 .
Memory (MB): peak = 606.430 ; gain = 0.000

-----------------------------------------------------------------------------

Finished Constraint Validation : Time (s): cpu = 00:00:16 ; elapsed = 00:00:24 .
Memory (MB): peak = 606.430 ; gain = 395.938

-----------------------------------------------------------------------------

-----------------------------------------------------------------------------

Start Loading Part and Timing Information

-----------------------------------------------------------------------------

Loading part: xc7z010clg400-1

-----------------------------------------------------------------------------

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:16 ; elapsed =
00:00:24 . Memory (MB): peak = 606.430 ; gain = 395.938

-----------------------------------------------------------------------------

-----------------------------------------------------------------------------

Start Applying 'set_property' XDC Constraints

-----------------------------------------------------------------------------

-----------------------------------------------------------------------------

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:16 ; elapsed
= 00:00:24 . Memory (MB): peak = 606.430 ; gain = 395.938

-----------------------------------------------------------------------------

INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'fsm'

INFO: [Synth 8-5544] ROM "state" won't be mapped to Block RAM because address size
(3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "yload" won't be mapped to Block RAM because address size
(3) smaller than threshold (5)
```

```
INFO: [Synth 8-5544] ROM "xload" won't be mapped to Block RAM because address size
(3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "state" won't be mapped to Block RAM because address size
(1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "state" won't be mapped to Block RAM because address size
(1) smaller than threshold (5)

-------------------------------------------------------------------------------------
--------------

                   State |                     New Encoding |                Previous
Encoding

-------------------------------------------------------------------------------------
--------------

                    IDLE |                              000 |
000

                   LOADX |                              001 |
001

                   LOADY |                              010 |
010

                    BUSY |                              011 |
011

                    STOP |                              100 |
100

-------------------------------------------------------------------------------------
--------------

INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding
'sequential' in module 'fsm'

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:24 .
Memory (MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------------


Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start RTL Component Statistics
```

```
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
          3 Input      8 Bit       Adders := 2
+---Registers :
                       8 Bit    Registers := 2
+---Muxes :
          2 Input      8 Bit        Muxes := 2
         10 Input      3 Bit        Muxes := 1
          5 Input      1 Bit        Muxes := 1
          2 Input      1 Bit        Muxes := 6
          3 Input      1 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module dp
Detailed RTL Component Info :
+---Adders :
          3 Input      8 Bit       Adders := 2
+---Registers :
                       8 Bit    Registers := 2
+---Muxes :
          2 Input      8 Bit        Muxes := 2
Module fsm
Detailed RTL Component Info :
+---Muxes :
         10 Input      3 Bit        Muxes := 1
          5 Input      1 Bit        Muxes := 1
          2 Input      1 Bit        Muxes := 6
```

```
          3 Input      1 Bit        Muxes := 1
-------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Part Resource Summary
-------------------------------------------------------------------------------
Part Resources:
DSPs: 80 (col length:40)
BRAMs: 120 (col length: RAMB18 40 RAMB36 20)
-------------------------------------------------------------------------------
Finished Part Resource Summary
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:17 ; elapsed =
00:00:25 . Memory (MB): peak = 606.430 ; gain = 395.938
-------------------------------------------------------------------------------


Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start Timing Optimization
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
```

```
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:28 ; elapsed =
00:00:36 . Memory (MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------

---------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:28 ; elapsed = 00:00:36 . Memory
(MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------


Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------

Start Technology Mapping

---------------------------------------------------------------------------

---------------------------------------------------------------------------

Finished Technology Mapping : Time (s): cpu = 00:00:28 ; elapsed = 00:00:36 . Memory
(MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------


Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------

Start IO Insertion

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---------------------------------------------------------------------------

Start Flattening Before IO Insertion

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---------------------------------------------------------------------------

Finished Flattening Before IO Insertion
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Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 . Memory (MB):
peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------------


Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

|      |Item              |Errors |Warnings |Status |Description       |

+------+------------------+-------+---------+-------+------------------+

|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Start Renaming Generated Instances

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---------------------------------------------------------------------------------

Finished Renaming Generated Instances : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37
. Memory (MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------------


Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Rebuilding User Hierarchy

---------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 .
Memory (MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Renaming Generated Ports

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Ports : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 .
Memory (MB): peak = 606.430 ; gain = 395.938

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---------------------------------------------------------------------------------

Start Handling Custom Attributes

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---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 .
Memory (MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Renaming Generated Nets

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Nets : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 .
Memory (MB): peak = 606.430 ; gain = 395.938

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Writing Synthesis Report

---------------------------------------------------------------------------------


Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+
```

Report Cell Usage:

| | Cell | Count |
|---|---|---|
| 1 | BUFG | 1 |
| 2 | CARRY4 | 5 |
| 3 | LUT2 | 16 |
| 4 | LUT3 | 2 |
| 5 | LUT4 | 11 |
| 6 | LUT5 | 20 |
| 7 | LUT6 | 4 |
| 8 | FDRE | 19 |
| 9 | IBUF | 11 |
| 10 | OBUF | 9 |

Report Instance Areas:

| | Instance | Module | Cells |
|---|---|---|---|
| 1 | top | | 98 |
| 2 | dp2 | dp | 49 |
| 3 | fsm2 | fsm | 28 |

---

Finished Writing Synthesis Report : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 .
Memory (MB): peak = 606.430 ; gain = 395.938

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:17 ; elapsed = 00:00:23 .
Memory (MB): peak = 606.430 ; gain = 108.711

Synthesis Optimization Complete : Time (s): cpu = 00:00:29 ; elapsed = 00:00:37 .
Memory (MB): peak = 606.430 ; gain = 395.938

```
INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 16 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.


INFO: [Common 17-83] Releasing license: Synthesis

28 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:28 ; elapsed = 00:00:35 . Memory (MB): peak =
606.430 ; gain = 395.938

INFO: [Common 17-1381] The checkpoint 'D:/ECE
440/project2/project2.runs/synth_1/gcd_core.dcp' has been generated.

report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.167 . Memory (MB):
peak = 606.430 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Thu Jan 30 16:56:18 2020...
```

## Source Code:

### gcd_core.sv

```
`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////
//////

// GCD Core. Code by Cory Holt for ECE 440

//////////////////////////////////////////////////////////////////////////////////
//////

module gcd_core(

    input logic clk, rst, load,

    input logic [7:0] din,

    output logic [7:0] gcd_rslt,

    output logic done

    );
```

```
// internal signals
    logic xsel, xload, ysel, yload;
    logic x_eq_y, x_gt_y;

    //dp and controller instances
    dp dp2 (.*
        );

    fsm fsm2 (.*
        );
endmodule
```

**dp.sv**

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
// GCD Core Data Path. Code by Cory Holt for ECE 440
////////////////////////////////////////////////////////////////////////////////
module dp(
    input logic clk, xload, xsel, yload, ysel,
    input logic [7:0] din,
    output logic [7:0] gcd_rslt,
    output logic x_eq_y, x_gt_y
    );
    //internal signals
    logic [7:0] x_m_y; //x minus y
    logic [7:0] y_m_x; //x minus y
    logic [7:0] x, y;

    //comparators
    assign x_eq_y = (x == y);
    assign x_gt_y = (x >= y);
```

```
    //Two subtractors
    assign x_m_y = (x - y);
    assign y_m_x = (y - x);

    always_ff @(posedge clk)
    begin
        if (xload)
            if (xsel)
                x <= din;
            else
                x <= x_m_y;
        if (yload)
            if (ysel)
                y <= din;
            else
                y <= y_m_x;
    end
    assign gcd_rslt = x;
endmodule
```

**fsm.sv**

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
// GCD Core Controller. Code by Cory Holt for ECE 440
////////////////////////////////////////////////////////////////////////////////
module fsm(
    input logic clk, rst, x_eq_y, x_gt_y, load,
    output logic xload, yload, done, xsel, ysel
    );
    typedef enum logic [2:0]
        {IDLE, LOADX, LOADY, BUSY, STOP} statetype;
    statetype state;
    //State logic begins here.
```

```
always_ff @(posedge clk)
begin
if (rst)
    state <= IDLE;
else
    case (state)
        IDLE : if (load)
                    state <= LOADX;
                else
                    state <= IDLE;
        LOADX : state <= LOADY;
        LOADY : state <= BUSY;
        BUSY :  begin
                if (!x_gt_y && !x_eq_y)
                    begin
                    state <= BUSY;
                    end
                else if (x_gt_y && !x_eq_y)
                    begin
                    state <= BUSY;
                    end
                else
                    begin
                    state <= STOP;
                    end
                end
        STOP :  begin
                    if(rst || load)
                        state <= IDLE;
                    else
                        state <= STOP;
                end
        endcase
```

```
end
//Output logic begins here.
always_comb begin
    xload = 0;
    xsel = 0;
    yload = 0;
    ysel = 0;
    done = 0;

    if (state == LOADX)
        begin
            xload = 1;
            xsel = 1;
        end
    if (state == LOADY)
        begin
            yload = 1;
            ysel = 1;
        end
    if (state == BUSY)
        begin
            if (!x_gt_y && !x_eq_y)
                begin
                    yload = 1;
                end
            else if (x_gt_y && !x_eq_y)
                begin
                    xload = 1;
                end
            else
                begin
                    done = 1;
                end
```

```
            end
        if (state == STOP)
            begin
                done = 1;
            end
    end //End always_comb


endmodule
```

**tb.sv**

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// GCD Core Testbench
//////////////////////////////////////////////////////////////////////////////////
module tb(
    );
    logic clk, rst, load;
    logic [7:0] din;
    logic [7:0] gcd_rslt;
    logic done;

    gcd_core uut(.*);
        parameter CLK_PRD = 100;
        parameter HOLD_TIME = (CLK_PRD*0.3);
        initial begin
            clk <= 0;
            forever #(CLK_PRD/2) clk = ~clk;
        end
        initial begin
            rst = 0;
            load = 0;
            din = 8'bx;
```

```
            #100
            @(posedge clk);
            #HOLD_TIME
            repeat(2) #CLK_PRD;
            rst = 1;
            #CLK_PRD;
            rst = 0;
            repeat(2) #CLK_PRD;
            load = 1;
            #CLK_PRD;
            load = 0;
            din = 8'd27; //LOAD val 1
            #CLK_PRD;
            //load = 0;
            din = 8'd21; //LOAD val 2
            #CLK_PRD;
            din = 8'bx;
            #CLK_PRD;
            begin: run_loop
                forever
                    begin
                        @(posedge clk);
                        if(done) disable run_loop;
                    end
            end
        end
endmodule
```