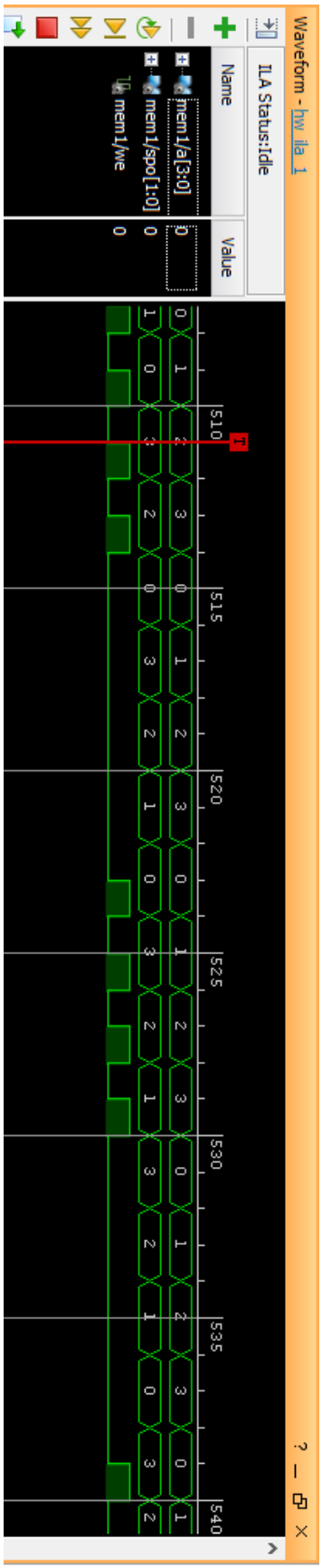
Cory Holt

ECE 440 p6



This was a simple project made more complex by simple mistakes I made. The first issue I ran into was selecting the wrong nets. I did not select the signals associated with the memory module. I selected the signals connected to the outputs and “wrapper” hardware. As it turns out, once implementation runs, those nets change names and it becomes harder to identify the correct signals, and in some cases they disappear completely. I then tried to fix that problem by selecting more signals associated with the memory module and adding those to the ILA but that ended up turning the debug core into a mess of excess signals. Eventually I was able to remove the core completely and start over. Starting fresh, I ensured I had the correct signals selected. This created the core correctly and I was able to then select the correct trigger conditions.