ECE 440

Cory Holt

HW #1

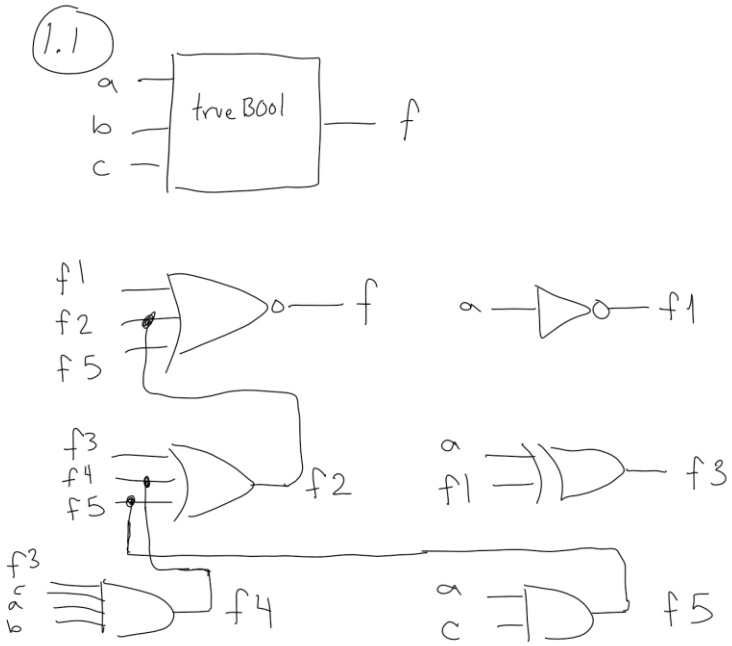
1. Exercises 1.1 and 1.3 (SV) (but not constrained to structural!)
    1. Problem 1.1:

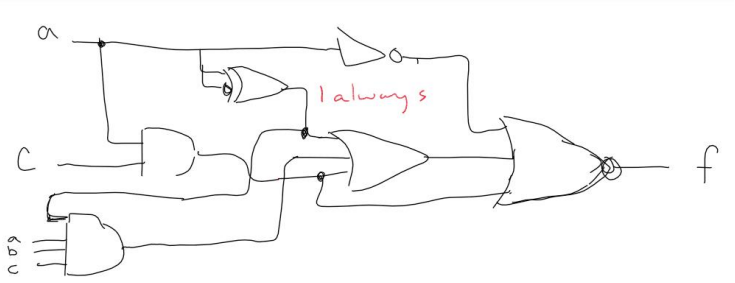
```
module ProblemThree
    (output logic f, g,
    input logic a, b, c, d, e);

    xor #6 g4(f, f6, f7, f8)
    not    g5(f3, f1)
           g8(f8, f4)
           g10(f9, d)
           g11(f10, e)
    and #4 g2(f2, a, f1)
           g3(f6,f2,f3)
    and #6 g9(g, f9, f10, f4, f5)
    nand #5 g1(f1, b, c)
            g6(f7, f3, d)
            g12(f5, f1, c)
    or #4  g7(f4, c, e)

endmodule: ProblemThree
```

    2. Problem 1.3:





$$f = \bar{a} \oplus (ac) \oplus 1$$

$$f = \bar{a}\,\overline{(ac)} + a(ac)$$

$$f = \bar{a}(\bar{a} + \bar{c}) + ac$$

$$f = \left[\bar{a} + \bar{a}\bar{c} + ac\right] \oplus 1$$

$$f = \overline{\left[\bar{a} + \bar{a}\bar{c} + ac\right]}$$

$$f = a\,ac\,\overline{ac} = ac(\bar{a} + \bar{c})$$

$$= \bar{a}ac + ac\bar{c}$$

$$f = 0$$

2. How does the Zynq architecture differ from "traditional" FPGAs? (e.g. Spartan 3E)
    1. The Zync architecture is unique in that it uses a “hard” ARM processor in conjunction with FPGA logic. Zync is a “System on Chip” which provides all the resources needed, digital and analog, to implement a solution that would have otherwise required multiple devices.
3. What resources are provided in the PL of the Zynq?
    1. The programable logic section contains an optional MicroBlaze Processor, a “soft” processor. The PL is composed of configurable logic blocks and I/O blocks. In addition, the PL has access to Block RAMs and DSP48E1 modules for faster arithmetic.
4. What type of interface is available between the PS and the PL in the Zynq?
    1. Zync uses AXI4 standard communication to allow the PS and the PL to work together.