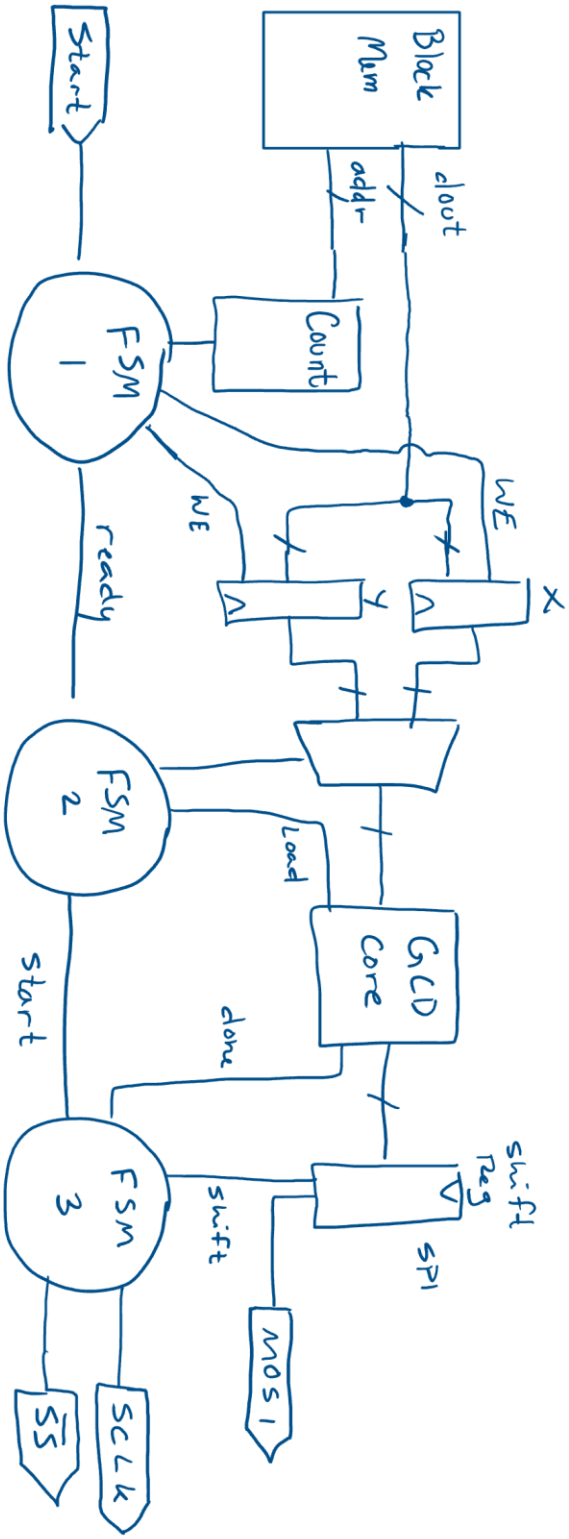
Cory Holt

ECE 440 H7

2/23/20



- FSM 1
    - Handles the transfer from memory to two parallel registers. Controls an address counter and a comparator to check if dout == 0.
- FSM 2
    - Similar to project 3, this FSM controls the inputs to the GCD_core. It handles the timing requirements and selecting the proper inputs from the two parallel temp registers.
- FSM 3
    - This FSM handles the SPI communications. I think a shift register can be used to shift the bits out one-by-one. This FSM will control the shifting as well as the slower clock of the SCLK. I am not sure how to implement the slower clock speed yet, but my intent is to send out the results as they are calculated. So this FSM will send a signal back to the core when it is clear to begin another computation.