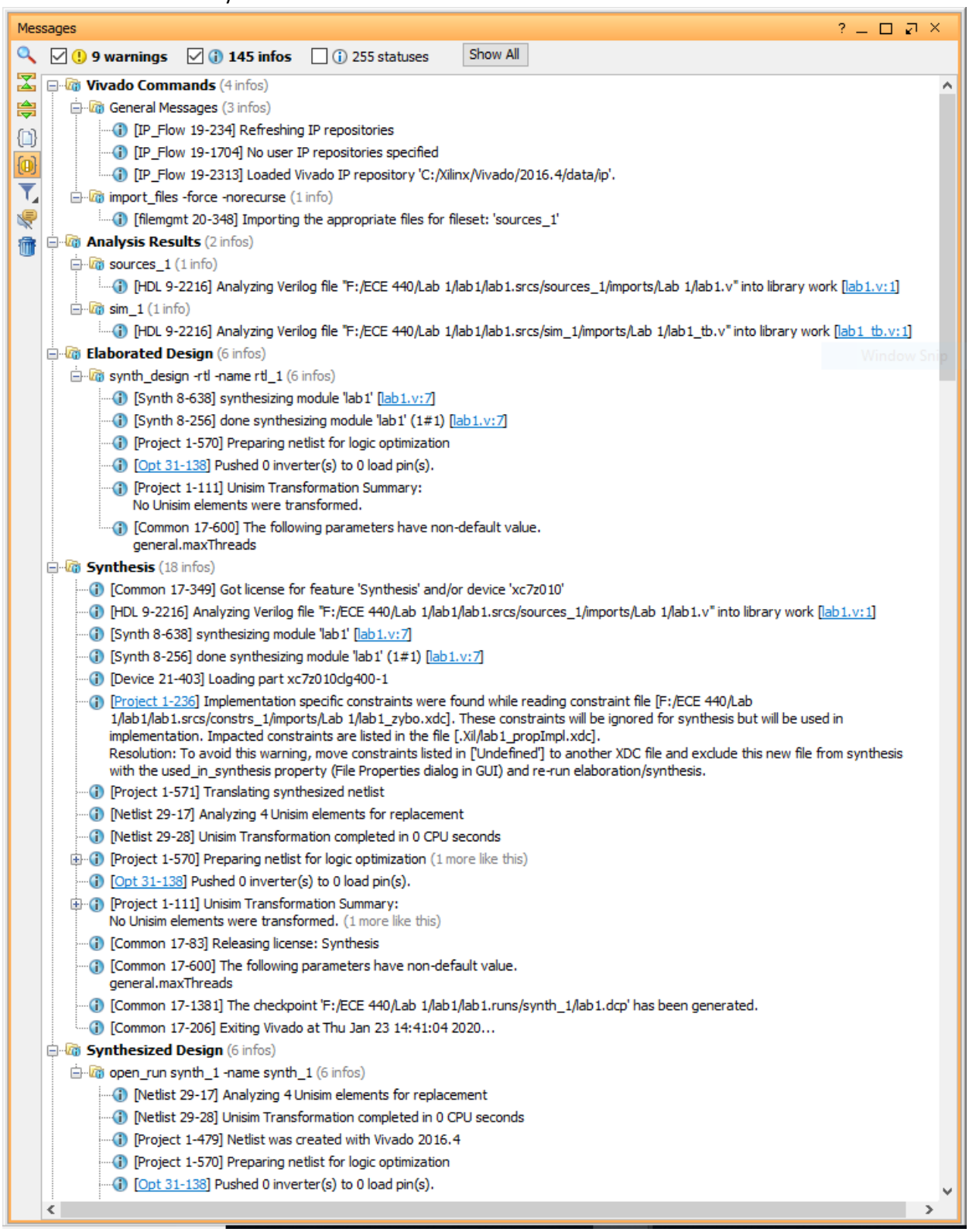
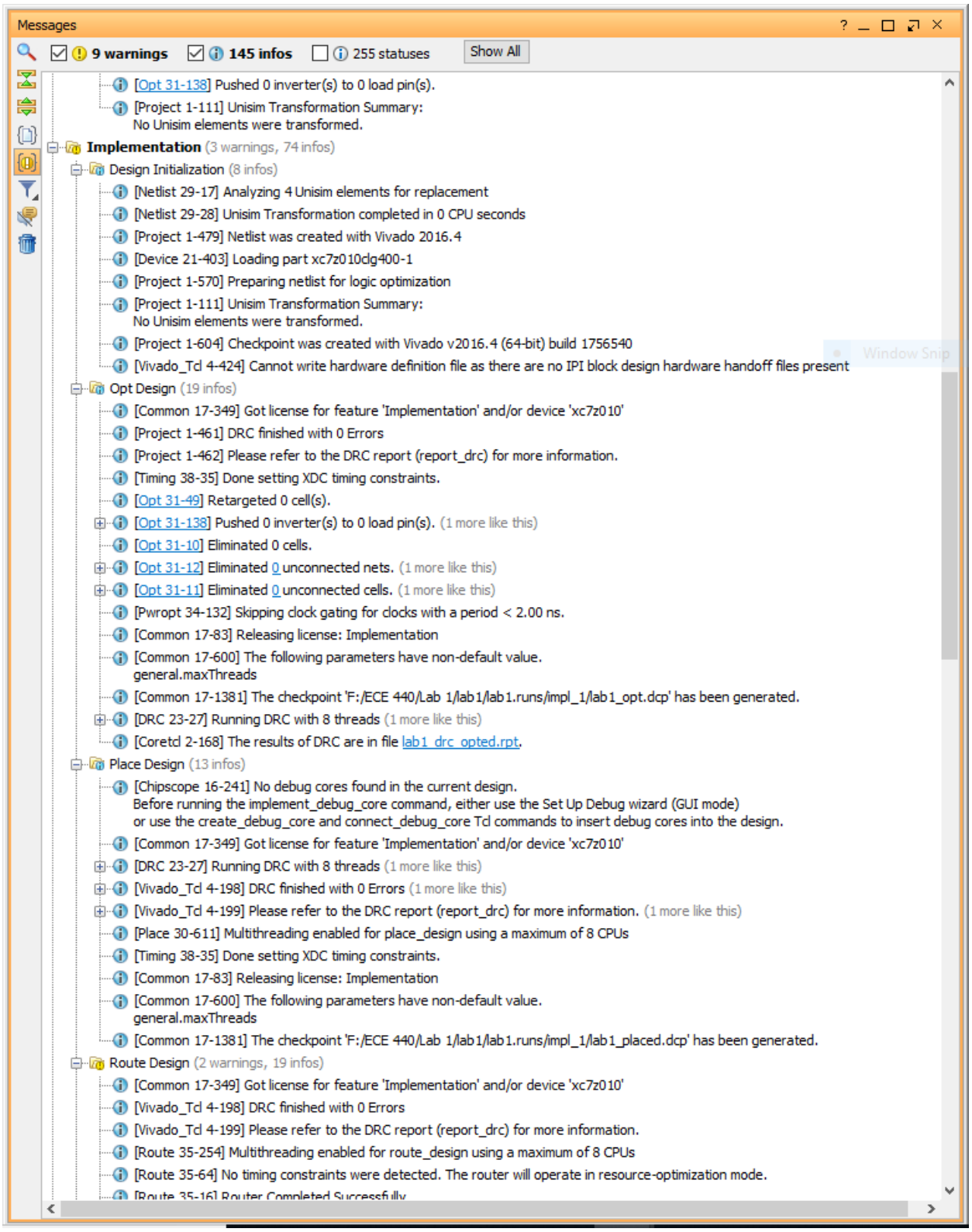
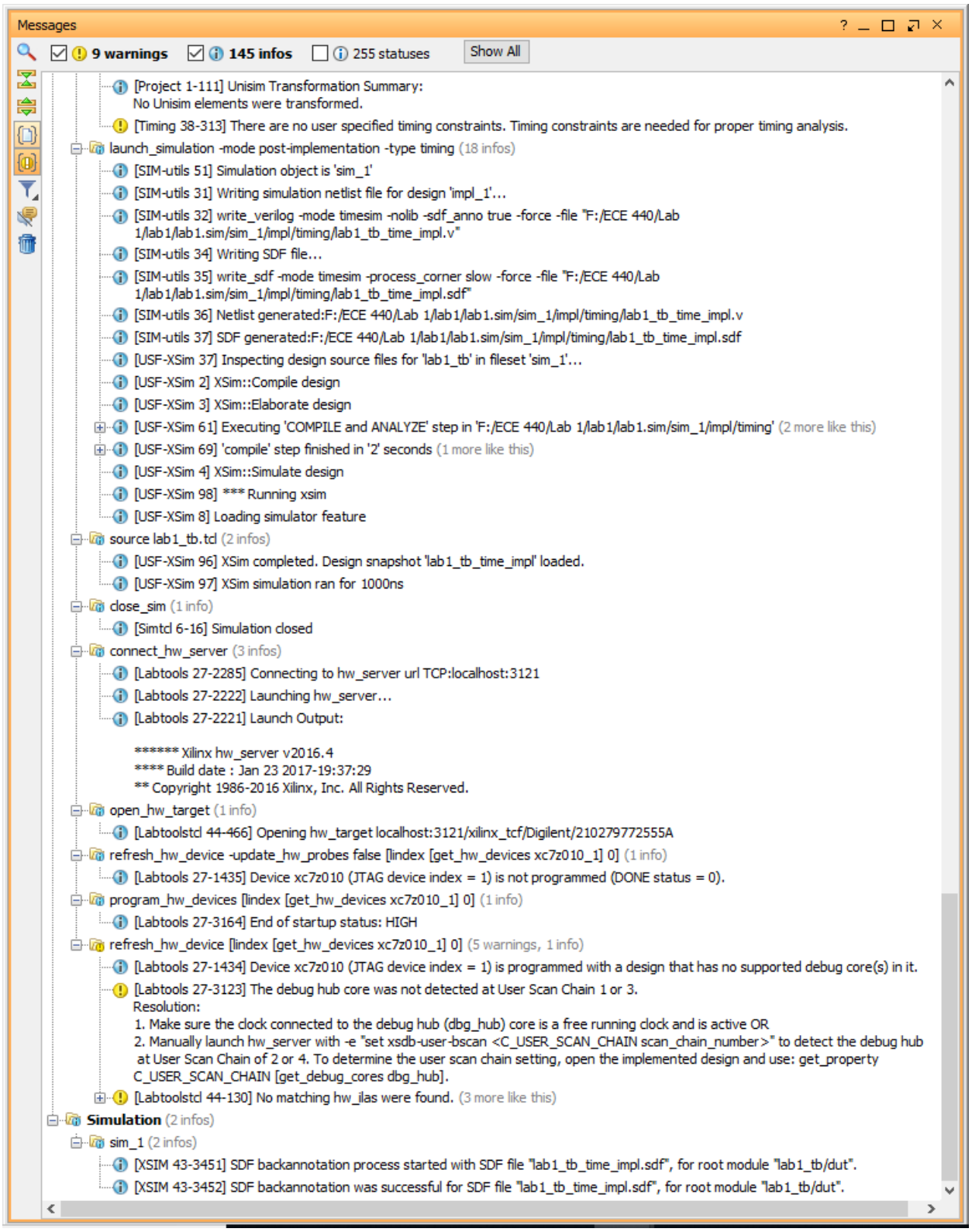
Lab 1 Deliverables – Cory Holt




Messages
9 warnings
145 infos
255 statuses
Show All
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
Implementation (3 warnings, 74 infos)
Design Initialization (8 infos)
[Netlist 29-17] Analyzing 4 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2016.4
[Device 21-403] Loading part xc7z010clg400-1
[Project 1-570] Preparing netlist for logic optimization
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
[Project 1-604] Checkpoint was created with Vivado v2016.4 (64-bit) build 1756540
[Vivado_Tcl 4-424] Cannot write hardware definition file as there are no IPI block design hardware handoff files present
Opt Design (19 infos)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
[Project 1-461] DRC finished with 0 Errors
[Project 1-462] Please refer to the DRC report (report_drc) for more information.
[Timing 38-35] Done setting XDC timing constraints.
[Opt 31-49] Retargeted 0 cell(s).
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
[Opt 31-10] Eliminated 0 cells.
[Opt 31-12] Eliminated 0 unconnected nets. (1 more like this)
[Opt 31-11] Eliminated 0 unconnected cells. (1 more like this)
[Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
[Common 17-83] Releasing license: Implementation
[Common 17-600] The following parameters have non-default value.
general.maxThreads
[Common 17-1381] The checkpoint 'F:/ECE 440/Lab 1/lab1/lab1.runs/impl_1/lab1_opt.dcp' has been generated.
[DRC 23-27] Running DRC with 8 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file lab1_drc_opted.rpt.
Place Design (13 infos)
[Chipscope 16-241] No debug cores found in the current design.
Before running the implement_debug_core command, either use the Set Up Debug wizard (GUI mode)
or use the create_debug_core and connect_debug_core Tcl commands to insert debug cores into the design.
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
[DRC 23-27] Running DRC with 8 threads (1 more like this)
[Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
[Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs
[Timing 38-35] Done setting XDC timing constraints.
[Common 17-83] Releasing license: Implementation
[Common 17-600] The following parameters have non-default value.
general.maxThreads
[Common 17-1381] The checkpoint 'F:/ECE 440/Lab 1/lab1/lab1.runs/impl_1/lab1_placed.dcp' has been generated.
Route Design (2 warnings, 19 infos)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
[Vivado_Tcl 4-198] DRC finished with 0 Errors
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
[Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
[Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.
[Route 35-16] Router Completed Successfully


Messages
9 warnings
145 infos
255 statuses
Show All
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
[Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
launch_simulation -mode post-implementation -type timing (18 infos)
[SIM-utils 51] Simulation object is 'sim_1'
[SIM-utils 31] Writing simulation netlist file for design 'impl_1'...
[SIM-utils 32] write_verilog -mode timesim -nolib -sdf_anno true -force -file "F:/ECE 440/Lab 1/lab1/lab1.sim/sim_1/impl/timing/lab1_tb_time_impl.v"
[SIM-utils 34] Writing SDF file...
[SIM-utils 35] write_sdf -mode timesim -process_corner slow -force -file "F:/ECE 440/Lab 1/lab1/lab1.sim/sim_1/impl/timing/lab1_tb_time_impl.sdf"
[SIM-utils 36] Netlist generated:F:/ECE 440/Lab 1/lab1/lab1.sim/sim_1/impl/timing/lab1_tb_time_impl.v
[SIM-utils 37] SDF generated:F:/ECE 440/Lab 1/lab1/lab1.sim/sim_1/impl/timing/lab1_tb_time_impl.sdf
[USF-XSim 37] Inspecting design source files for 'lab1_tb' in fileset 'sim_1'...
[USF-XSim 2] XSim::Compile design
[USF-XSim 3] XSim::Elaborate design
[USF-XSim 61] Executing 'COMPILE and ANALYZE' step in 'F:/ECE 440/Lab 1/lab1/lab1.sim/sim_1/impl/timing' (2 more like this)
[USF-XSim 69] 'compile' step finished in '2' seconds (1 more like this)
[USF-XSim 4] XSim::Simulate design
[USF-XSim 98] *** Running xsim
[USF-XSim 8] Loading simulator feature
source lab1_tb.tcl (2 infos)
[USF-XSim 96] XSim completed. Design snapshot 'lab1_tb_time_impl' loaded.
[USF-XSim 97] XSim simulation ran for 1000ns
close_sim (1 info)
[Simtcl 6-16] Simulation closed
connect_hw_server (3 infos)
[Labtools 27-2285] Connecting to hw_server url TCP:localhost:3121
[Labtools 27-2222] Launching hw_server...
[Labtools 27-2221] Launch Output:
****** Xilinx hw_server v2016.4
**** Build date : Jan 23 2017-19:37:29
** Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.
open_hw_target (1 info)
[Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210279772555A
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7z010_1] 0] (1 info)
[Labtools 27-1435] Device xc7z010 (JTAG device index = 1) is not programmed (DONE status = 0).
program_hw_devices [lindex [get_hw_devices xc7z010_1] 0] (1 info)
[Labtools 27-3164] End of startup status: HIGH
refresh_hw_device [lindex [get_hw_devices xc7z010_1] 0] (5 warnings, 1 info)
[Labtools 27-1434] Device xc7z010 (JTAG device index = 1) is programmed with a design that has no supported debug core(s) in it.
[Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3.
Resolution:
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User Scan Chain of 2 or 4. To determine the user scan chain setting, open the implemented design and use: get_property C_USER_SCAN_CHAIN [get_debug_cores dbg_hub].
[Labtoolstcl 44-130] No matching hw_ilas were found. (3 more like this)
Simulation (2 infos)
sim_1 (2 infos)
[XSIM 43-3451] SDF backannotation process started with SDF file "lab1_tb_time_impl.sdf", for root module "lab1_tb/dut".
[XSIM 43-3452] SDF backannotation was successful for SDF file "lab1_tb_time_impl.sdf", for root module "lab1_tb/dut".

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# Vivado v2016.4 (64-bit)

# SW Build 1756540 on Mon Jan 23 19:11:23 MST 2017

# IP Build 1755317 on Mon Jan 23 20:30:07 MST 2017

# Start of session at: Thu Jan 23 14:40:29 2020

# Process ID: 388

# Current directory: F:/ECE 440/Lab 1/lab1/lab1.runs/synth_1

# Command line: vivado.exe -log lab1.vds -product Vivado -mode batch -
messageDb vivado.pb -notrace -source lab1.tcl

# Log file: F:/ECE 440/Lab 1/lab1/lab1.runs/synth_1/lab1.vds

# Journal file: F:/ECE 440/Lab 1/lab1/lab1.runs/synth_1\vivado.jou

#-----------------------------------------------------------

Sourcing tcl script 'C:/Xilinx/Vivado/2016.4/scripts/init.tcl'

source lab1.tcl -notrace

Command: synth_design -top lab1 -part xc7z010clg400-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7z010'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7z010'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 13696

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Starting RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:10 .
Memory (MB): peak = 325.586 ; gain = 114.055

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INFO: [Synth 8-638] synthesizing module 'lab1' [F:/ECE 440/Lab
1/lab1/lab1.srcs/sources_1/imports/Lab 1/lab1.v:7]

INFO: [Synth 8-256] done synthesizing module 'lab1' (1#1) [F:/ECE 440/Lab
1/lab1/lab1.srcs/sources_1/imports/Lab 1/lab1.v:7]

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Finished RTL Elaboration : Time (s): cpu = 00:00:06 ; elapsed = 00:00:11 .
Memory (MB): peak = 362.848 ; gain = 151.316

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Report Check Netlist:

	Item	Errors	Warnings	Status	Description
1	multi_driven_nets	0	0	Passed	Multi driven nets

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:11 . Memory (MB): peak = 362.848 ; gain = 151.316

INFO: [Device 21-403] Loading part xc7z010clg400-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [F:/ECE 440/Lab 1/lab1/lab1.srcs/constrs_1/imports/Lab 1/lab1_zybo.xdc]

Finished Parsing XDC File [F:/ECE 440/Lab 1/lab1/lab1.srcs/constrs_1/imports/Lab 1/lab1_zybo.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [F:/ECE 440/Lab 1/lab1/lab1.srcs/constrs_1/imports/Lab 1/lab1_zybo.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/lab1_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/lab1_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.038 . Memory (MB): peak = 589.406 ; gain = 0.000

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Finished Constraint Validation : Time (s): cpu = 00:00:12 ; elapsed =
00:00:21 . Memory (MB): peak = 589.406 ; gain = 377.875

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Start Loading Part and Timing Information

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Loading part: xc7z010clg400-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:12 ;
elapsed = 00:00:21 . Memory (MB): peak = 589.406 ; gain = 377.875

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Start Applying 'set_property' XDC Constraints

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Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:13 ;
elapsed = 00:00:21 . Memory (MB): peak = 589.406 ; gain = 377.875

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ; elapsed =
00:00:21 . Memory (MB): peak = 589.406 ; gain = 377.875

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start RTL Component Statistics
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----
Detailed RTL Component Info :
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----
Finished RTL Component Statistics
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
----
Hierarchical RTL Component report
---------------------------------------------------------------------------
----
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
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---------------------------------------------------------------------------
----
Start Part Resource Summary
---------------------------------------------------------------------------
----
Part Resources:
DSPs: 80 (col length:40)
BRAMs: 120 (col length: RAMB18 40 RAMB36 20)
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----
Finished Part Resource Summary
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Start Cross Boundary and Area Optimization
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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:13 ;
elapsed = 00:00:22 . Memory (MB): peak = 589.406 ; gain = 377.875

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Timing Optimization

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:21 ; elapsed
= 00:00:30 . Memory (MB): peak = 620.688 ; gain = 409.156

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Finished Timing Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:30
. Memory (MB): peak = 620.688 ; gain = 409.156

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |
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Start Technology Mapping
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-------------------------------------------------------------------------------
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Finished Technology Mapping : Time (s): cpu = 00:00:21 ; elapsed = 00:00:30 .
Memory (MB): peak = 630.305 ; gain = 418.773
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Report RTL Partitions:
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| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
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----
Start IO Insertion
-------------------------------------------------------------------------------
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-------------------------------------------------------------------------------
----
Start Flattening Before IO Insertion
-------------------------------------------------------------------------------
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-------------------------------------------------------------------------------
----
Finished Flattening Before IO Insertion
-------------------------------------------------------------------------------
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----
Start Final Netlist Cleanup
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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:21 ; elapsed = 00:00:30 .
Memory (MB): peak = 630.305 ; gain = 418.773

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Report Check Netlist:

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|      |Item              |Errors |Warnings |Status |Description       |

+------+------------------+-------+---------+-------+------------------+

|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:21 ; elapsed =
00:00:30 . Memory (MB): peak = 630.305 ; gain = 418.773

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:21 ; elapsed =
00:00:30 . Memory (MB): peak = 630.305 ; gain = 418.773

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:21 ; elapsed =
00:00:30 . Memory (MB): peak = 630.305 ; gain = 418.773

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:21 ; elapsed =
00:00:30 . Memory (MB): peak = 630.305 ; gain = 418.773

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:21 ; elapsed =
00:00:30 . Memory (MB): peak = 630.305 ; gain = 418.773
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Start Writing Synthesis Report
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Report BlackBoxes:
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| |BlackBox name |Instances |
+-+--------------+----------+
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Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT1 |     1|
|2     |LUT2 |     2|
|3     |LUT3 |     1|
|4     |IBUF |     4|
|5     |OBUF |     4|
+------+-----+------+


Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    12|
+------+---------+-------+------+
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Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed =
00:00:30 . Memory (MB): peak = 630.305 ; gain = 418.773

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:11 ; elapsed =
00:00:17 . Memory (MB): peak = 630.305 ; gain = 153.203

Synthesis Optimization Complete : Time (s): cpu = 00:00:21 ; elapsed =
00:00:31 . Memory (MB): peak = 630.305 ; gain = 418.773

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 4 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.


INFO: [Common 17-83] Releasing license: Synthesis

15 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB):
peak = 642.258 ; gain = 399.746

INFO: [Common 17-600] The following parameters have non-default value.

general.maxThreads

INFO: [Common 17-1381] The checkpoint 'F:/ECE 440/Lab
1/lab1/lab1.runs/synth_1/lab1.dcp' has been generated.

report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.119 .
Memory (MB): peak = 642.258 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Thu Jan 23 14:41:04 2020...
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