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ECE 440

Project 4

2-14-20

I found this project to be pretty easy. It was very straightforward to implement. The trickiest part was setting the correct specifications for the memory module. When I initially created the coefficient file to initialize the memory, I added the entries backwards. This meant that when I ran my simulations, the results were different from what others were getting, so I knew I had done something wrong. It was pretty easy to see that I had simply initialized the memory module "backwards." I could not figure out how to update the contents of the memory without going through the memory wizard again, so I simply fixed the .coe file and reran the memory creation tool. Interestingly, the reversed data made it easier for me to recognize the pattern of change in the memory. When the entries initially matched with their addresses, there was a time where the data out "doubled up" just after the write sequence. The data out held its last value for twice the amount of time, so I was able to see the shifting pattern that occurred.

Aside from that mistake, I ran into no major issues. The testbench was simple and the simulations ran as expected with no errors. Behavioral even matched with post-implementation right away. Overall, this was a straightforward and pretty easy project.

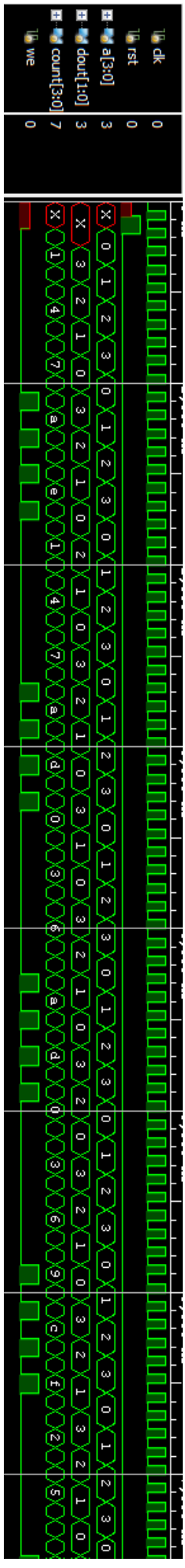
```
module ALC( input logic rst, clk,
            output logic [1:0] dout
          );
    //internal signals
    logic [3:0] count;
    logic [3:0] a;
    logic [1:0] spo;
    logic [1:0] d;
    logic we;
    dist_mem_gen_0 mem1 (
      .a(a),      // input wire [3 : 0] a
      .d(d),      // input wire [1 : 0] d
      .clk(clk),  // input wire clk
      .we(we),    // input wire we
      .spo(spo)  // output wire [1 : 0] spo
    );

    always_ff @(posedge clk)
    begin
        dout <= spo;
        if(rst) count <= 0;
        else
            count <= count + 1;
    end // End always_ff

    always_comb begin
        a = count[2:1];
        d = (dout - 1);
        we = (count[3] & count[0]);
    end

endmodule
```

Behavioral Simulation



Post-Implementation