rst_ps7_0_100M

slowest_sync_clk | mb_reset
ext_reset_in | bus_struct_reset[0:0]
aux_reset_in | peripheral_reset[0:0]
mb_debug_sys_rst | interconnect_aresetn[0:0]
dcm_locked | peripheral_aresetn[0:0]

Processor System Reset

ps7_0_axi_periph

S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN | M00_AXI
M00_ACLK
M00_ARESETN

AXI Interconnect

axi_gpio_0

S_AXI
s_axi_aclk
s_axi_aresetn | GPIO

AXI GPIO

leds_4bits

processing_system7_0

DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0_ACLK | M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N

ZYNQ7 Processing System

DDR
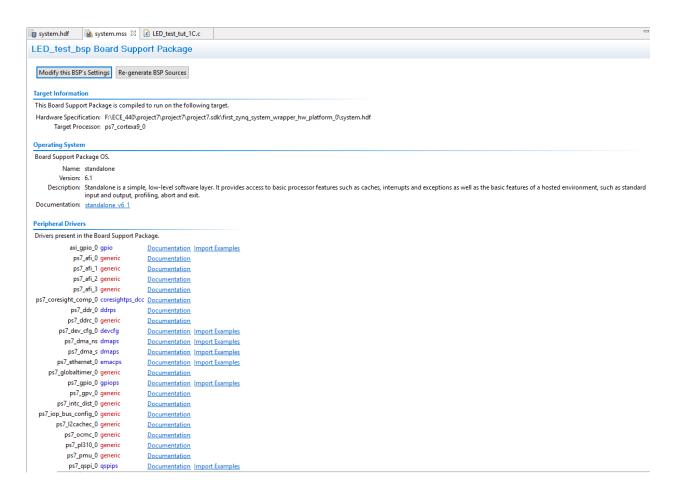FIXED_IO

Target FPGA Device: 7z010
            Part: xc7z010clg400-1
    Created With: Vivado 2016.4
      Created On: Mon Mar 09 13:06:45 2020

Address Map for processor ps7_cortexa9_[0-1]

Cell	Base Addr	High Addr	Slave I/f	Mem/Reg
ps7_intc_dist_0	0xf8f01000	0xf8f01fff		REGISTER
ps7_gpio_0	0xe000a000	0xe000afff		REGISTER
ps7_scutimer_0	0xf8f00600	0xf8f0061f		REGISTER
ps7_slcr_0	0xf8000000	0xf8000fff		REGISTER
axi_gpio_0	0x41200000	0x4120ffff	S_AXI	REGISTER
ps7_scuwdt_0	0xf8f00620	0xf8f006ff		REGISTER
ps7_l2cachec_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_scuc_0	0xf8f00000	0xf8f000fc		REGISTER
ps7_qspi_linear_0	0xfc000000	0xfcffffff		MEMORY
ps7_pmu_0	0xf8893000	0xf8893fff		REGISTER
ps7_afi_1	0xf8009000	0xf8009fff		REGISTER
ps7_afi_0	0xf8008000	0xf8008fff		REGISTER
ps7_qspi_0	0xe000d000	0xe000dfff		REGISTER
ps7_usb_0	0xe0002000	0xe0002fff		REGISTER
ps7_afi_3	0xf800b000	0xf800bfff		REGISTER
ps7_afi_2	0xf800a000	0xf800afff		REGISTER
ps7_globaltimer_0	0xf8f00200	0xf8f002ff		REGISTER
ps7_dma_s	0xf8003000	0xf8003fff		REGISTER
ps7_iop_bus_config_0	0xe0200000	0xe0200fff		REGISTER
ps7_xadc_0	0xf8007100	0xf8007120		REGISTER
ps7_ddr_0	0x00100000	0x1fffffff		MEMORY
ps7_ddrc_0	0xf8006000	0xf8006fff		REGISTER
ps7_ocmc_0	0xf800c000	0xf800cfff		REGISTER
ps7_pl310_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_uart_1	0xe0001000	0xe0001fff		REGISTER
ps7_coresight_comp_0	0xf8800000	0xf88fffff		REGISTER
ps7_ttc_0	0xf8001000	0xf8001fff		REGISTER
ps7_scugic_0	0xf8f00100	0xf8f001ff		REGISTER
ps7_ethernet_0	0xe000b000	0xe000bfff		REGISTER
ps7_dev_cfg_0	0xf8007000	0xf80070ff		REGISTER
ps7_dma_ns	0xf8004000	0xf8004fff		REGISTER
ps7_sd_0	0xe0100000	0xe0100fff		REGISTER
ps7_gpv_0	0xf8900000	0xf89fffff		REGISTER
ps7_ram_1	0xffff0000	0xfffffdff		MEMORY
ps7_ram_0	0x00000000	0x0002ffff		MEMORY

LED_test_bsp Board Support Package

[Modify this BSP's Settings]   [Re-generate BSP Sources]

Target Information

This Board Support Package is compiled to run on the following target.

   Hardware Specification: F:\ECE_440\project7\project7\project7.sdk\first_zynq_system_wrapper_hw_platform_0\system.hdf

   Target Processor: ps7_cortexa9_0

Operating System

Board Support Package OS.

   Name: standalone

   Version: 6.1

   Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.

   Documentation: standalone_v6_1

Peripheral Drivers

Drivers present in the Board Support Package.

axi_gpio_0	gpio	Documentation	Import Examples
ps7_afi_0	generic	Documentation	
ps7_afi_1	generic	Documentation	
ps7_afi_2	generic	Documentation	
ps7_afi_3	generic	Documentation	
ps7_coresight_comp_0	coresightps_dcc	Documentation	
ps7_ddr_0	ddrps	Documentation	
ps7_ddrc_0	generic	Documentation	
ps7_dev_cfg_0	devcfg	Documentation	Import Examples
ps7_dma_ns	dmaps	Documentation	Import Examples
ps7_dma_s	dmaps	Documentation	Import Examples
ps7_ethernet_0	emacps	Documentation	Import Examples
ps7_globaltimer_0	generic	Documentation	
ps7_gpio_0	gpiops	Documentation	Import Examples
ps7_gpv_0	generic	Documentation	
ps7_intc_dist_0	generic	Documentation	
ps7_iop_bus_config_0	generic	Documentation	
ps7_l2cachec_0	generic	Documentation	
ps7_ocmc_0	generic	Documentation	
ps7_pl310_0	generic	Documentation	
ps7_pmu_0	generic	Documentation	
ps7_qspi_0	qspips	Documentation	Import Examples

```
12:24:08 INFO   : 'targets -set -filter {jtag_cable_name =~ "Digilent Zybo 210279772555A" && level==0} -index 1' command is executed.
12:24:08 INFO   : 'fpga -state' command is executed.
12:24:08 INFO   : Connected to target on host '127.0.0.1' and port '3121'.
12:24:09 INFO   : Jtag cable 'Digilent Zybo 210279772555A' is selected.
12:24:09 INFO   : 'jtag frequency' command is executed.
12:24:09 INFO   : Sourcing of 'F:/ECE_440/project7/project7/project7.sdk/first_zynq_system_wrapper_hw_platform_0/ps7_init.tcl' is done.
12:24:09 INFO   : Context for 'APU' is selected.
12:24:09 INFO   : Hardware design information is loaded from 'F:/ECE_440/project7/project7/project7.sdk/first_zynq_system_wrapper_hw_platform_0/system
12:24:09 INFO   : Context for 'APU' is selected.
12:24:09 INFO   : 'stop' command is executed.
12:24:10 INFO   : 'ps7_init' command is executed.
12:24:10 INFO   : 'ps7_post_config' command is executed.
12:24:10 INFO   : Context for processor 'ps7_cortexa9_0' is selected.
12:24:10 INFO   : Processor reset is completed for 'ps7_cortexa9_0'.
12:24:10 INFO   : Context for processor 'ps7_cortexa9_0' is selected.
12:24:10 INFO   : The application 'F:/ECE_440/project7/project7/project7.sdk/LED_test/Debug/LED_test.elf' is downloaded to processor 'ps7_cortexa9_0'.
12:24:10 INFO   : ----------------XSDB Script----------------
connect -url tcp:127.0.0.1:3121
source F:/ECE_440/project7/project7/project7.sdk/first_zynq_system_wrapper_hw_platform_0/ps7_init.tcl
targets -set -nocase -filter {name =~"APU*" && jtag_cable_name =~ "Digilent Zybo 210279772555A"} -index 0
loadhw F:/ECE_440/project7/project7/project7.sdk/first_zynq_system_wrapper_hw_platform_0/system.hdf
targets -set -nocase -filter {name =~"APU*" && jtag_cable_name =~ "Digilent Zybo 210279772555A"} -index 0
stop
ps7_init
ps7_post_config
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo 210279772555A"} -index 0
rst -processor
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo 210279772555A"} -index 0
dow F:/ECE_440/project7/project7/project7.sdk/LED_test/Debug/LED_test.elf
----------------End of Script----------------

12:24:10 INFO   : Memory regions updated for context APU
12:24:10 INFO   : Context for processor 'ps7_cortexa9_0' is selected.
12:24:10 INFO   : 'con' command is executed.
12:24:10 INFO   : ----------------XSDB Script (After Launch)----------------
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo 210279772555A"} -index 0
con
----------------End of Script----------------

12:24:10 INFO   : Launch script is exported to file 'F:\ECE_440\project7\project7\project7.sdk\.sdk\launch_scripts\xilinx_c-c++_application_(system_de
```