

Instruction cache		Data cache		
0	1	0	1	
0×100 0×104	9x18+ (7x105	0x2000	0×2003 0×2013	
9×102 0×100	11×105 0×103 0×101	0×2002	0×2011	

caches use the Least Recently Used algorithm for the block replacement. They are initially empty.

Complete the following table for the instruction and data accesses.  $M = 0 \times 100 \times 700 \times 100 \times$ 

Time	Instr Addr	Hit/Miss	Data Addr	Hit/Miss
1	0×1000 → <b>0</b> ×	,	0×20000 → <b>0</b> x	
2	0x1004 → 0x1	· ·	0×20024 <b>→ 0</b> ×	
3	0x1008	H	,	
4	0x100C	Н		
5	0x1010	М		
6	0x1000	Н	0x20004	Н
7	0x1004	Н	0x20028	Н
8	0x1020	М		
9	0x <u>102</u> 4	H		
10	0x1010	Н		
11	0x1014	H		
12	0x1040	M		
13	70x <u>104</u> 4	H	0x20030	M
14	0x1008	M	0x20031	H
15	0x100C	H	0x20032	Н
16	0x1050	M		
17	0x1054	H		
18	0x1058	H	<b>7</b> 7 0x20110	М
19	0x <u>101</u> 8	Н		
20	0x1030	, W	0x20130	M
21	0x1034	Н	0x20134	Н
23	0x1050	M		
24	0x1010	M	0x20024	H
25	0x1054	H		•

Suppose an L2 unified cache is added to the system. It is a 4-way set associative cache with 4 sets and block size of 16 bytes.

L1 Instruction cache			L1 Data cache
0	1	0	1
0x104	0x101 0x105	0×2000	Dx 2003 0x 2013
9×402 0×100	0×105 0×103- 0×101	0× 2002	0x 2011
	L2 u	nified cache	
0	1	2	3
0x100	0×101	0x 2002	0x 2003
0×2000	0×102	0×102	0×103
0x104	104 0x 2011		0×2013
Complete the foll	lowing table for the instructi	on and data accesses.	M ← Main Mem L1 ← Hit L2 ← Hit in L2 in L

			L2 <del>-</del>	Hit III L2
Time	Instr Addr	${ m L1/L2/Miss}$	Data Addr	${ m L1/L2/Miss}$
1	0x1000 → <b>()</b> ×	100 M	0x20000 -> 0>	2000 M
2	0x1004	L1	0x20024 → <b>(</b> )	2∞2 M
3	0x1008 → <b>0</b> x	100 L1		
4	0x100C	LI		
5	0x1010	M		
6	0x1000	L1	0x20004	L1
7	0x1004	L1	0x20028 → <b>0</b>	×2002 L1
8	0x1020	M		
9	0x1024	L1		
10	0x1010	L1		
11	0x1014	L1		
12	0x1040	M		
13	0x1044	L1	0x20030	M
14	0x1008	L2	0x20031	L1
15	0x100C	L1	0x20032	L1
16	0x1050	M		
17	0x1054	L1 '		
18	0x1058	L1	0x20110	M
19	0x1018	L1		·
20	0x1030	, M	0x20130	M
21	0x1034	L1	0x20134	L1
23	0x1050	L2		
24	0x1010	L2	0x20024	L1
25	0x1054	L1		_