Exercise

Assume that a computer system is equipped with two L1 caches i.e. L1 data cache, and L1 instruction cache. Each of the cache is a 2-way set associative cache with 2 sets and block size of 16 bytes. The caches use the Least Recently Used algorithm for the block replacement. They are initially empty.

Instruction cache		Data cache	
0	1	0	1

Complete the following table for the instruction and data accesses.

Time	Instr Addr	Hit/Miss	Data Addr	Hit/Miss
1	0x1000		0x20000	
2	0x1004		0x20024	
3	0x1008			
4	0x100C			
5	0x1010			
6	0x1000		0x20004	
7	0x1004		0x20028	
8	0x1020			
9	0x1024			
10	0x1010			
11	0x1014			
12	0x1040			
13	0x1044		0x20030	
14	0x1008		0x20031	
15	0x100C		0x20032	
16	0x1050			
17	0x1054			
18	0x1058		0x20110	
19	0x1018			
20	0x1030		0x20130	
21	0x1034		0x20134	
23	0x1050			
24	0x1010		0x20024	
25	0x1054			

Suppose an L2 unified cache is added to the system. It is a 4-way set associative cache with 4 sets and block size of 16 bytes.

L1 Instruction cache		L1 Data cache	
0	1	0	1

L2 unified cache			
0	1	2	3

Complete the following table for the instruction and data accesses.

Time	Instr Addr	L1/L2/Miss	Data Addr	L1/L2/Miss
1	0x1000		0x20000	
2	0x1004		0x20024	
3	0x1008			
4	0x100C			
5	0x1010			
6	0x1000		0x20004	
7	0x1004		0x20028	
8	0x1020			
9	0x1024			
10	0x1010			
11	0x1014			
12	0x1040			
13	0x1044		0x20030	
14	0x1008		0x20031	
15	0x100C		0x20032	
16	0x1050			
17	0x1054			
18	0x1058		0x20110	
19	0x1018			
20	0x1030		0x20130	
21	0x1034		0x20134	
23	0x1050			
24	0x1010		0x20024	
25	0x1054			