Exercise 5

Assume that a computer system is equipped with L1 and L2 caches:

- *L1 data cache* is a 2-way set associative cache with 2 sets and block size of 32 bytes.
- *L1 instruction cache* is a 2-way set associative cache with 2 sets and block size of 32 bytes.
- *L2 unified cache* is a 4-way set associative cache with 4 sets and block size of 32 bytes.

The caches use the Least Recently Used algorithm for the block replacement, and are initially empty.

L1 Instruction cache		L1 Data cache	
0	1	0	1

L2 Unified cache			
0	1	2	3

Complete the table below to show how the following memory addresses can be accessed. Write *L1* when the specified memory address is found in one of the L1 caches, *L2* when the memory address is found in the L2 cache, and *Miss* when the memory address is not available in both levels of caches.

Time	Instr Addr	L1/L2/Miss	Data Addr	L1/L2/Miss
1	`0x410`		`0x20000`	
2	`0x414`		`0x20024`	
3	`0x430`		`0x20060`	
4	`0x434`			
5	`0x418`			
6	`0x400`		`0x20004`	
7	`0x440`		`0x200C8`	
8	`0x460`		`0x20028`	
9	`0x450`		`0x200C4`	
10	`0x430`			
11	`0x400`			
12	`0x460`			
13	`0x440`			

```
#define N 1000

int array_compare(int A[N], int B[N]) {
  int i;

  for(i=0; i<N, i++) {
    if (A[i] != B[i]) {
      return 0;
    }
  }

  return 1;
}
```

Suppose our computer uses a 2-way set associative cache with 4 sets, and cache line size is 16 bytes (4 integers). Here, we assume that the starting address of the arrays `A` and `B` are address `0` and address `0x10000`, respectively.

1. What is the hit rate when both arrays are identical?

2. What is the hit rate after we make the cache line size be 64 bytes? We still assume that both arrays are still identical.