Nitish Kumar Srivastava

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Objective Internship in Computer Architecture / VLSI design.

Education

Ph.D. student, ECE, Cornell University *Aug'14-present*
Advisors: Prof. David Albonesi & Prof. Zhiru Zhang
CGPA: 4.01/4.0

B.Tech, ECE, Indian Institute of Technology, Kanpur *July'10-May'14*
Institute Rank 1, GPA: 10/10

Research

Data Dependent Frequency Scaling using Desynchronization *June'15*
Under Dr. Rajit Manohar, ECE, Cornell University
- Designed efficient clock network using asynchronous handshakes to dynamically scale the frequency.
- Can scale frequency of processors every cycle based on dynamic instruction stream.
- Used RISCV rocket chip developed at U.C. Berkely to demonstrate the proposed methodology.

Accelerating Face Detection on Programmable SoC Using HLS *Jan'15*
Under Dr. Zhiru Zhang, ECE, Cornell University
- Designed accelerator for Viola Jones face detection algorithm using High Level Synthesis.
- Able to achieve a frame rate suitable for realtime applications.
- Provided a realistic benchmark with sufficient complexity to stress state-of-the-arts HLS tools.

Exploiting data-reuse patterns in stencil applications on spatial architectures *Dec'16*
Under Dr. David Albonesi, Dr. Zhiru Zhang and Dr. Christopher Batten, ECE, Cornell University
- Using existing X-loops based architecture as the starting point.

Publications

- **Accelerating Face Detection on Programmable SoC Using C-Based Synthesis.**
Nitish Srivastava, Steve Dai, Rajit Manohar and Zhiru Zhang, Int'l Symposium on FPGAs, 2017
- **Flexible and dynamic power allocation in broadband multi-beam satellites.**
Nitish Srivastava, and A. K. Chaturvedi, IEEE Communications Letters 17.9 (2013): 1722-1725.

Course Projects

Pointer-Chase Prefetcher for Linked Data Structures *Mar'15*
- Designed the hardware for Linked Data Structure prefetcher in Verilog.
- Extended the ISA to support compiler hints to prefetch graph nodes into the cache.
- Evaluated the design for power, energy and performance by passing it through the ASIC tool-flow of Design Compiler, ICC place and route and Prime Time.

B.Tech Project

Passive RFID Tag Chip Redesign for Low Power Operations *Feb'14*
- Designed digital and analog circuitry of a passive RFID Tag.
- Applied various power reduction techniques in different modules of digital block.

Selected Awards

- Selected as a **Cornell Fellow** in 2014 for outstanding academic performance.
- **President's Gold Medal** for best academic performance in the graduating batch, 2014.
- **Proficiency Medal** and **Pratik Mishra Gold Medal** for the best performance in ECE 2014.
- Awarded **Viterbi scholarship** (20 selections all over India) in 2013.
- **All India Rank (AIR) 364(99.99 percentile)** in IIT JEE'10.

Technical Skills

Hardware Verilog, BSV, Design Compiler, Encounter, SDSoC, VCS, Prime Time, gem5
Software C, C++, Python, Java, MATLAB, OpenMP, CUDA, LaTeX, LINUX, bash

Relevant Courses

Computer Architecture	Operating Systems	Compilers
Complex ASIC design	Algorithms	Machine Learning