**TRANSACTION STRUCTURE**

**1) Address Structure**

a)BURST LENGTH

AXI4 supports burst length of 1 to 16 for fixed burst type. It extends burst length support for the INCR burst type to 1 to 256 transfers. For wrapping bursts, the burst length must be 2, 4, 8, or 16 and a burst must not cross a 4KB address boundary

2)Burst Type and Burst Address

Fixed: Address=Start Address

Increment: Address=Start address+ Transfer size i.e. (Address\_N = Aligned\_Address + (N – 1) × Number\_Bytes)

Wrap: Start address must be aligned i.e. (Address\_N = Wrap\_Boundary + (Number\_Bytes × Burst\_Length))

AxBURST[1:0] Burst type

0b00 FIXED

0b01 INCR

0b10 WRAP

0b11 Reserved

**2) Data read & write structure**

a)Write Strobe

The WSTRB[n:0] signals when HIGH, specify the byte lanes of the data bus that contain valid information

**3) Read & Write Response structure**

RRESP[1:0] BRESP[1:0] Response

0b00 OKAY

0b01 EXOKAY

0b10 SLVERR

0b11 DECERR