

ANALOGUE ELECTRONICS

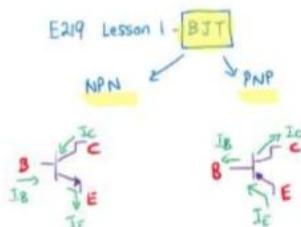
LESSON 1 (BJT)



E219 Lesson 1 – BJT (Bipolar Junction Transistor) Summary

What are Transistor ?

Transistor is a semiconductor device that can be used at amplify voltage, current , and power. With a small signal applied to the input of the transistor, the output can be hundreds or even thousands times larger than the input signal. Transistor can also be use as a switch.



$$I_E = I_B + I_C$$

Node voltages : V_C , V_B , V_E

Voltage across BC junction . V_{BC}

Voltage across BE junction , V_{BE}

Voltage across CE junction , V_{CE}

Supply voltages : V_{CC} , V_{BB} , V_{EE}

Base current : I_B

Emitter current : I_E

Collector current: I_C

DC Current Gain, Beta : β_{DC}

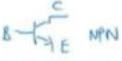
$$\beta_{DC} = \frac{I_C}{I_B} \quad \text{--- --- --- For Active mode only}$$

$$\alpha_{DC} = \frac{I_C}{I_E} \quad \text{--- --- } \alpha_{DC} < 1$$

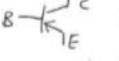
$$\alpha_{DC} = \frac{\beta_{DC}}{\beta_{DC} + 1}$$

Alpha DC , α_{DC}




NPN

	B-E junction	B-C junction
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward


PNP

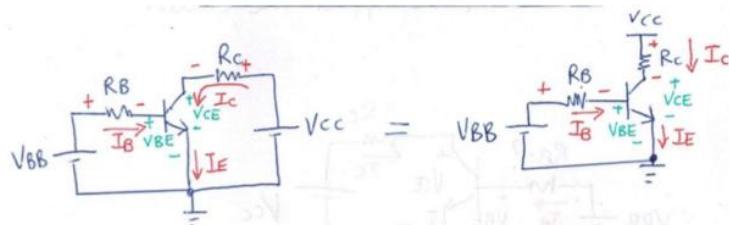
	E-B junction	C-B junction
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

LESSON 2 (BJT Active)

E219 – Lesson 2 Summary (BJT Amplifier in Active Mode)

BJT (Common Emitter configuration)

Circuit 1



Based on the circuit above,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$I_E = I_C + I_B$$

$$V_{BE} = 0.7V$$

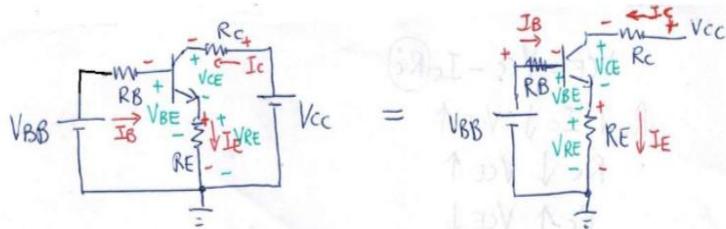
$$\beta_{DC} = \frac{I_C}{I_B} \quad (\text{for active mode only})$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_E = 0V$$

$$V_{BE} = V_B - V_E = V_B, \quad V_{CE} = V_C - V_E = V_C$$

Circuit 2



Based on this circuit,

$$I_B = \frac{V_{BB} - V_{BE} - V_{RE}}{R_B}$$

$$V_{BE} = 0.7V \quad , \quad I_E = I_C + I_B$$

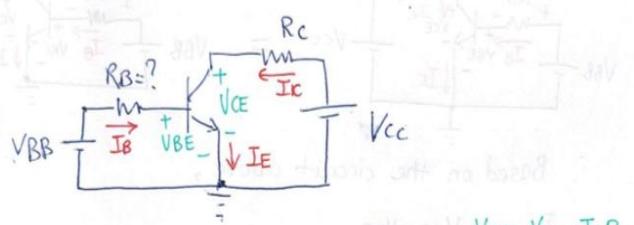
$$\beta_{DC} = \frac{I_C}{I_B} \quad (\text{for active mode only})$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_E = V_{RE} = I_E R_E \neq 0V$$

$$V_{BE} = V_B - V_E \neq V_B \quad , \quad V_{CE} = V_C - V_E \neq V_C$$

1. How does the choice of R_B affect the circuit?



$$R_B \uparrow \text{ more resistance at Base } \quad I_B \downarrow \quad I_C \downarrow \quad V_{CE} \uparrow$$
$$I_C = \beta_{DC} \times I_B$$

$$R_B \downarrow \quad I_B \uparrow \quad I_C \uparrow \quad V_{CE} \downarrow$$

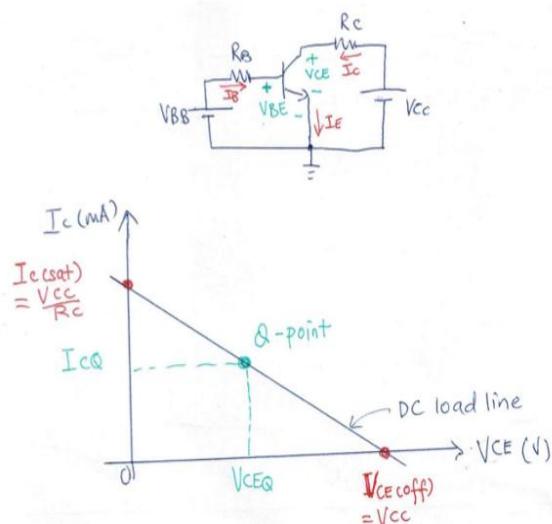
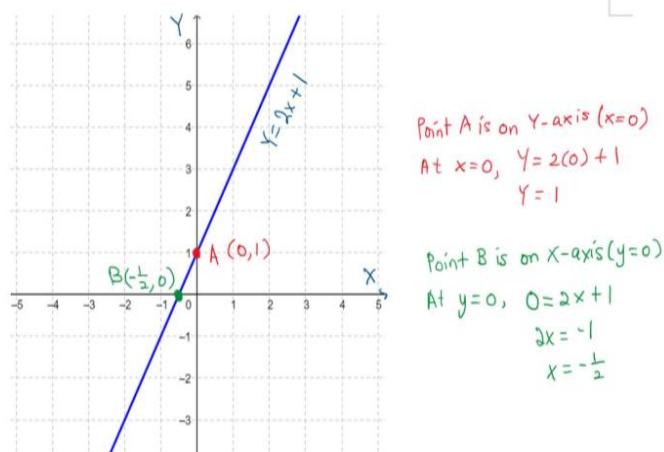
2. How does the choice of R_C affect the circuit?
(see above)

$$V_{CE} = V_{CC} - I_C R_C$$

$$R_C \downarrow \quad V_{CE} \uparrow$$

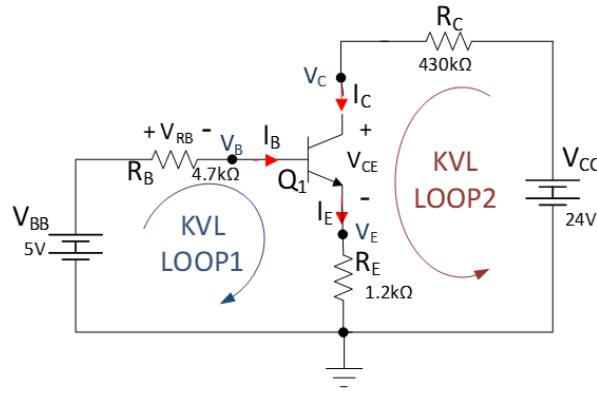
$$R_C \uparrow \quad V_{CE} \downarrow$$

Recap



- ① This is a I_c - V_{ce} characteristic graph.
- ② BJT in Active mode \Rightarrow Application : Amplifier
- ③ For amplifier circuit \Rightarrow operate Q-point at the mid-point for
- ④ DC load line ($I_{c(\text{sat})}$, $V_{ce(\text{off})}$, Q-point, I_{cQ} , V_{ceQ})

7. Consider the following BJT circuit that operating in active mode.



Given that $\beta_{DC} = 70$ and $I_E = [(\beta_{DC} + 1)I_B]$, determine the current values of I_B , I_C and I_E .

$$\begin{aligned} V_{BB} &= V_{RB} + V_{BE} + V_{RE} \\ 5 &= I_B R_B + 0.7 + I_E R_E \\ &= 4.7k I_B + 0.7 + 1.2k I_E \quad \textcircled{1} \end{aligned}$$

$$\begin{aligned} I_E &= (\beta_{DC} + 1) I_B \\ &= (70 + 1) I_B \\ &= 71 I_B \quad \textcircled{2} \end{aligned}$$

Sub \textcircled{2} into \textcircled{1} :

$$\begin{aligned} 5 &= 4.7k I_B + 0.7 + 1.2k (71 I_B) \\ &= 4.7k I_B + 0.7 + 85.2k I_B \\ &= 89.9k I_B + 0.7 \\ 89.9k I_B &= 4.3 \\ I_B &= \underline{\underline{47.83 \mu A}} \quad \text{**} \end{aligned}$$

$$\begin{aligned} I_E &= 71 I_B \\ &= 71 (47.83 \mu A) \\ &= \underline{\underline{3.396 mA}} \quad \text{**} \end{aligned}$$

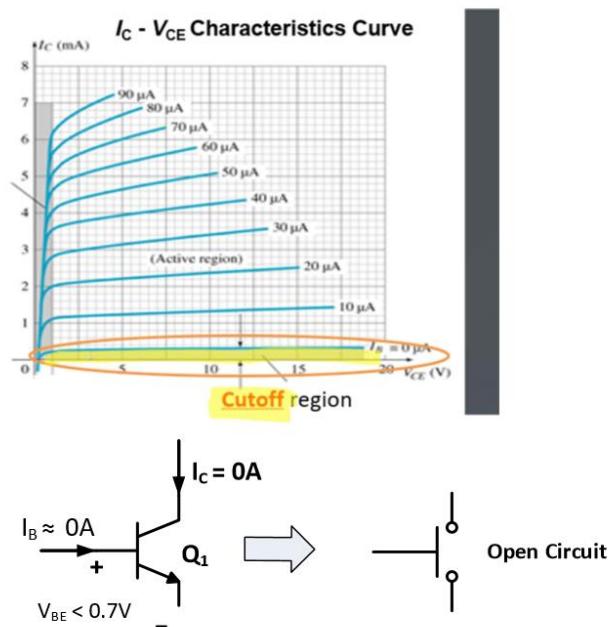
$$\begin{aligned} \beta_{DC} &= \frac{I_C}{I_B} \\ 70 &= \frac{I_C}{I_B} \end{aligned}$$

$$\begin{aligned} I_C &= 70 I_B \\ &= 70 (47.83 \mu A) \\ &= \underline{\underline{3.3481 mA}} \quad \text{**} \end{aligned}$$

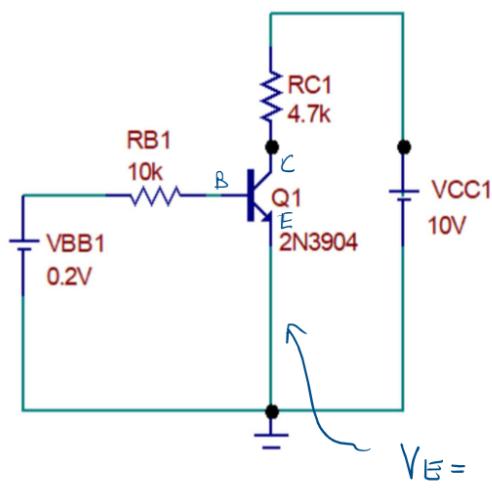
LESSON 3 (BJT Switch)

E219 : Lesson 3 Summary

- 1) BJT as an Open Switch (in Cut off Mode)



BJT Mode Of Operation	B-E Junction	B-C Junction
Cut-off	Reverse Bias	Reverse Bias



$V_{BE} < 0.2V$ (reverse biased)

$$I_B =$$

$$I_C =$$

$$V_{RC1} =$$

$$V_C =$$

$$V_{CE} =$$

$$V_B =$$

$$\sqrt{RB_1} =$$

$$I_E =$$

$$\beta_{DC} = 125.53$$

Application: When BJT Switch is ON



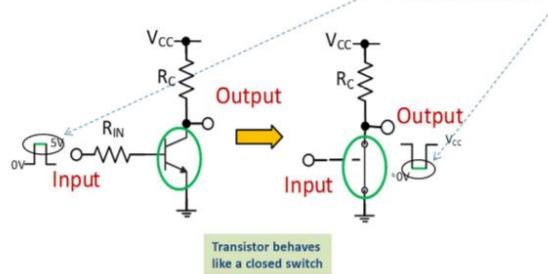
- Input = 5 V, "switch" is ON (BJT driving into saturation mode)

- Assume ideal saturation mode, $V_{CE(SAT)} \approx 0 V$
(i.e. short circuit)

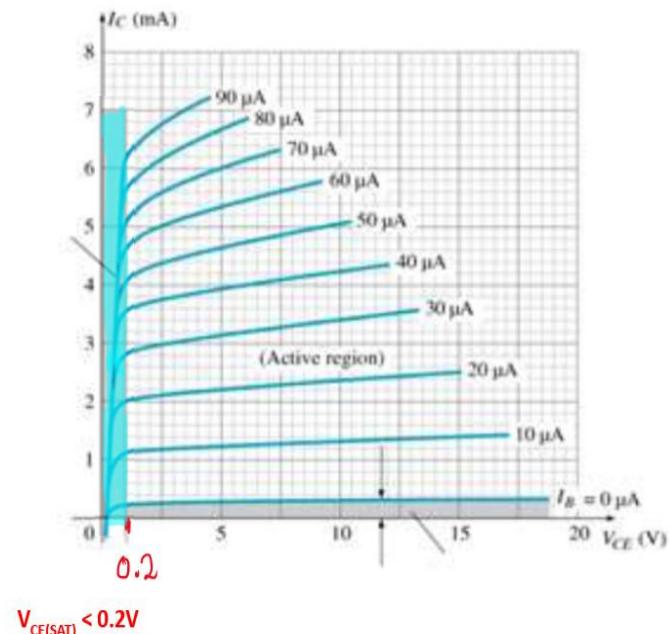
- The output voltage = **0V**

- Collector current, $I_{C(SAT)} \approx V_{CC}/R_C$
(max. possible collector current)

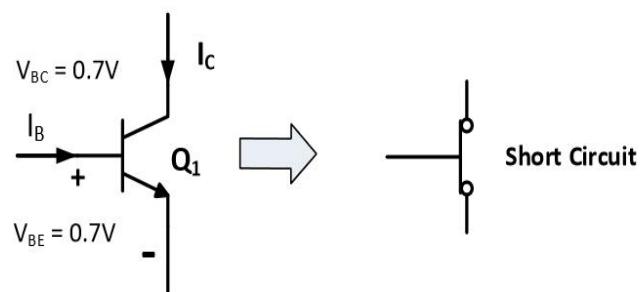
*Notice the signal inversion
between input and output*



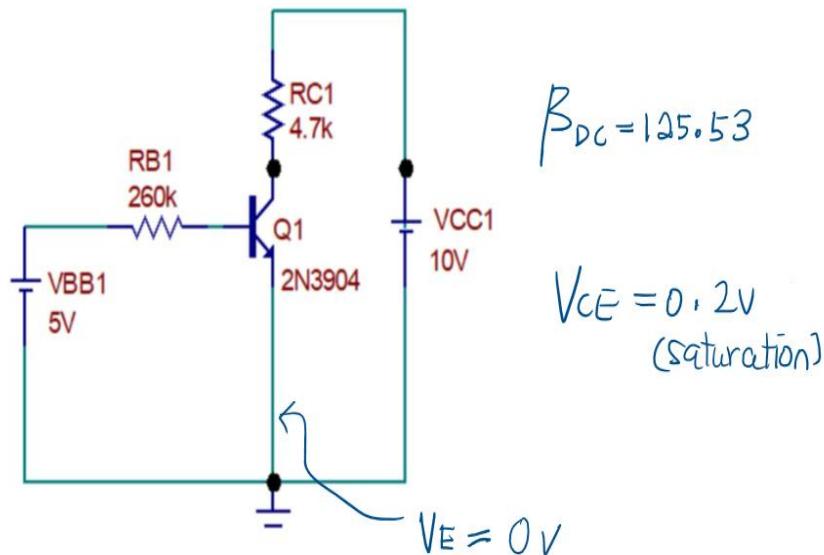
2) BJT as a Closed Switch (in **Saturation** Mode)



$V_{CE(SAT)} < 0.2\text{V}$



BJT Mode Of Operation	B-E Junction	B-C Junction
Cut-off	Reverse Bias	Reverse Bias
Active	Forward Bias	Reverse Bias
Saturation	Forward Bias	Forward Bias



$$V_{BE} = 0.7V$$

$$I_B = \frac{V_{BB1} - V_{BE}}{R_{B1}} = \frac{5 - 0.7}{260 \times 10^3} = 16.54 \mu A$$

$$I_C = \beta_{DC} \times I_B = 125.53 (16.54 \mu) = 2.076 mA$$

$$V_{CE} = V_C = 0.2428V$$

$$V_C = V_{CE} = 10 - 9.7572 = 0.2428V$$

$$V_B = V_{BE} = 0.7V$$

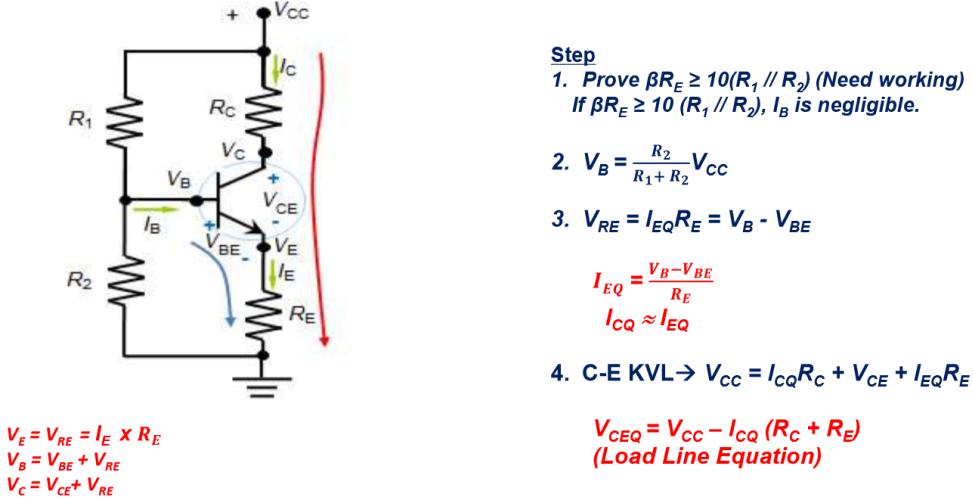
$$V_{RB} = 5 - 0.7 = 4.3V$$

$$V_{RC} = I_C R_C = (2.076 \times 10^{-3})(4700) = 9.7572V$$

$$I_E = I_B + I_C = 2.093 mA$$

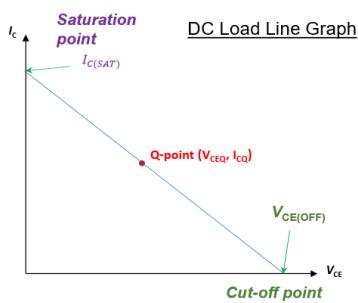
LESSON 4 (Voltage Divider Bias, DC Load Line (CE))

Analysis of Voltage Divider Bias Circuit



DC Load Line → NPN BJT Circuit

Academic use



X-intercept: $y (I_c) = 0, I_c = 0$ mean **Cutoff mode**

Load Line Equation for CE connection

$$V_{ce} = V_{cc} - I_c R_c - I_c R_E \quad (I_E \approx I_c)$$

$V_{ce(off)} = V_{cc}$ (X-intercept point or Cutoff point)

Y-intercept: $x (V_{ce}) = 0, V_{ce} = 0$ mean **Saturation mode**

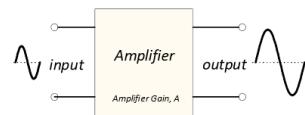
Load Line Equation for CE connection

$$V_{ce} \approx V_{cc} - I_c R_c - I_c R_E \quad (I_E \approx I_c)$$

$$I_{c(SAT)} \approx \frac{V_{cc}}{R_c + R_E} \quad (\text{Y-intercept point or Saturation point})$$



How do we define an Amplifier?



$$\text{No-load Voltage Gain, } A_{VNL} = \frac{V_{out}}{V_{in}}$$

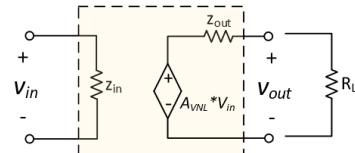
$$\text{Loaded Voltage Gain, } A_{VL} = \frac{V_{out}}{V_{in}}$$

$$\text{Input Impedance, } z_{in} = \frac{V_{in}}{I_{in}}$$

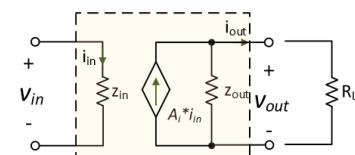
$$\text{Output Impedance, } z_{out} = \frac{V_{out}}{I_{out}}$$

(with $V_{in} = 0 \text{ V}$)

$$\text{No-load Current Gain, } A_i = \frac{I_{out}}{I_{in}}$$



Voltage Amplifier

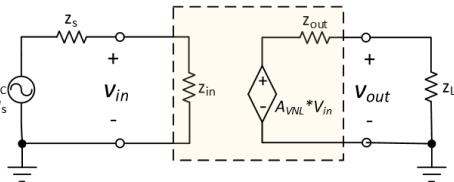


Current Amplifier



Ideal Voltage Amplifier

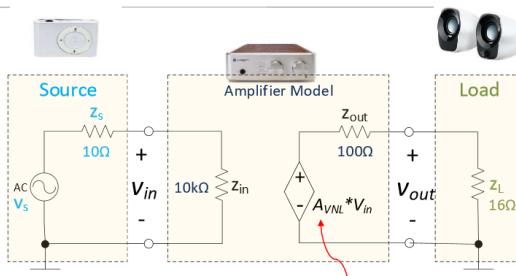
- Ideal voltage amplifier:
- Infinite no-load gain, A_{VNL}
 - Infinite input impedance, Z_{in}
 - Zero output impedance, Z_{out}



- **Infinite gain** provides an ideal case as amplifier is supposed to provide as high gain as possible. In reality, this is not possible.
- With **infinite input impedance**, there would be no current in the input circuit. The entire V_s will drop across Z_{in} (*Open circuit voltage*).
 $\Rightarrow V_{in} \approx V_s$
- With **zero output impedance**, there would be no reduction at output voltage
 $\Rightarrow V_{out} \approx V_s$ (Hint: Think about *Voltage Divider Rule*)



Self-Test (5 mins)



The amplifier has a **No load voltage Gain, A_{VNL}** of 20. Determine the voltage value for V_{in} and V_{out} if $V_s = 2V_{RMS}$.

$$V_{in} = \frac{10k}{10k+10} \times 2V_{RMS} = 1.998V_{RMS}$$

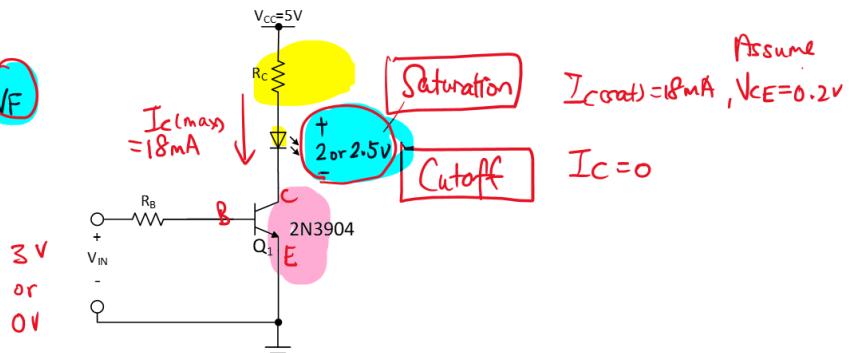
$$V_{out} = \frac{16}{16+100} \times 1.998V_{RMS} (A_{VNL}) = 5.517V_{RMS}$$

LESSON 5 (Worksheet Discussion)

Q10

KVL Loop 2.

$$V_{CC} = V_{RC} + V_{CE} + V_F$$



Below are the specifications that you will have to satisfy while designing the LED driver.

V_{IN}	LED Light	LED Current (A)
3V	ON	Maximum 18m
0V	OFF	$\approx 0A$

The selection of beta value can be anything as it is not certain given that the I_C - V_{CE} characteristic curve is not listed in the datasheet. The only available information is Page 2 – ON CHARACTERISTICS showing $I_C = 10mA$; $V_{CE} = 1V$ with a possible min. H_{FE} of 100. From the table, we can observe that if $I_C = 18mA$ (specification requirement) with a low V_{CE} , the H_{FE} should be slightly smaller or equal to 100.

ON CHARACTERISTICS*

<u>h_{FE}</u>	DC Current Gain	$I_C = 0.1 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 1.0 \text{ mA}, V_{CE} = 1.0 \text{ V}$ <u>$I_C = 10 \text{ mA}, V_{CE} = 1.0 \text{ V}$</u> <u>$I_C = 50 \text{ mA}, V_{CE} = 1.0 \text{ V}$</u> <u>$I_C = 100 \text{ mA}, V_{CE} = 1.0 \text{ V}$</u>	40 70 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 1.0 \text{ mA}$ $I_C = 50 \text{ mA}, I_B = 5.0 \text{ mA}$		0.2 0.3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 1.0 \text{ mA}$ $I_C = 50 \text{ mA}, I_B = 5.0 \text{ mA}$	0.65	0.85 0.95	V V

Assume h_{FE} or $\beta_{DC} = 100$,

LESSON 6 (CE Circuit)

CE Amplifier with bypass H_T , C_E

$$r'_e = \frac{25 \text{ mV}}{I_{\text{EQ}}}$$

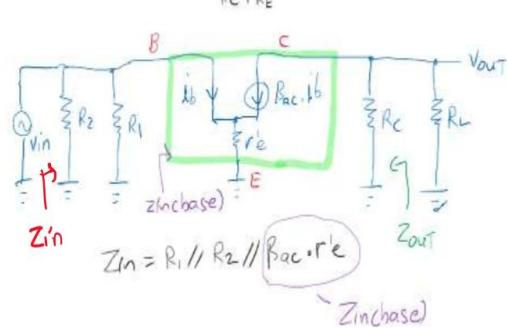
$$r'_e = \frac{h_{ie}}{h_{fe}} \text{ (best)}$$

$$\beta_{ac} = h_{fe}$$

$$= \frac{i_c}{i_b}$$

$$\beta_{dc} = \frac{i_c}{i_b}$$

$$= h_{FE}$$



$$V_{CEQ} = V_{cc} - I_{cEQ}R_C - I_{E}R_E$$

$$I_{cEQ} = \frac{V_{cc}}{R_C + R_E}$$

$$Z_{in} = R_1 // R_2 // (\beta_{ac} \cdot r'_e)$$

$$Z_{in} = R_1 // R_2 // (\beta_{ac} \cdot i_b)$$

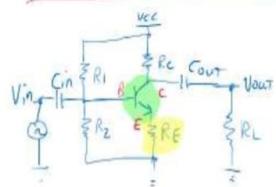
$$Z_{in} = R_1 // R_2 // (\beta_{ac} (r'_e + R_E))$$

$$Z_{out} = R_L$$

$$A_{VNL} = - \frac{R_C}{r'_e} \rightarrow r_L$$

$$A_{VL} = - \frac{(R_C // R_L)}{r'_e} r_L$$

CE Amplifier without bypass H_T , C_E



$$V_{CEQ} = V_{cc} - I_{cEQ}R_C - I_E R_E$$

$$I_{cEQ} = \frac{V_{cc}}{R_C + R_E}$$

$$Z_{in} = R_1 // R_2 // (\beta_{ac} \cdot i_b)$$

$$Z_{in} = R_1 // R_2 // (\beta_{ac} (r'_e + R_E))$$

$$Z_{in} = R_1 // R_2 // (\beta_{ac} (r'_e + R_E))$$

$$Z_{out} = R_L$$

$$A_{VNL} = - \frac{R_C}{(r'_e + R_E)} \rightarrow r_L$$

$$A_{VL} = - \frac{(R_C // R_L)}{(r'_e + R_E)} \rightarrow r_L$$

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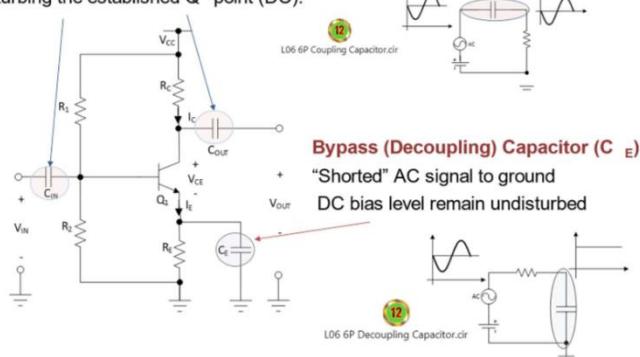
Capacitors in Amplifier

Refer to Smartbook Sec 30-2, Figure 30-3



Coupling Capacitor (C_{in} & C_{out})

Allow AC signal to couple into circuit without disturbing the established Q-point (DC).



h_{ie}	Input impedance (BJT)	Ω	
$h_{fe} = \beta_{ac}$	AC Current Gain	-	
r'_e	AC Emitter Resistance	Ω	$r'_e = \frac{h_{ie}}{h_{fe}}$ Accurate $r'_e = \frac{25mV}{IEQ}$ Inaccurate
Z_{in}	Input Impedance (Amplifier)	Ω	$Z_{in} = \frac{V_{in}}{I_{in}}$
Z_{out}	Output Impedance	Ω	$Z_{out} = \frac{V_{out}}{I_{out}}$
A_{VNL}	Voltage Gain (no load) (no R_L)	Ω	$A_{VNL} = \frac{V_{out\ (without\ R_L)}}{V_{in}}$
A_{VL}	Voltage Gain (with load)	Ω	$A_{VL} = \frac{V_{out\ (with\ R_L)}}{V_{in}}$
$Z_{in\ (base)}$	Input Impedance (base)	Ω	$Z_{in\ (base)} = \beta_{ac} \cdot r'_e$

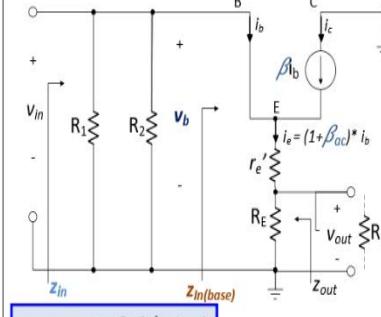
Refer to
OneNote
for more
formulas

LESSON 8 (CC, CB Darlington)

CE (Common Emitter) Amplifier	CC (Common Collector) Amplifier	CB (Common Base) Amplifier
Input : Base Output : Collector AC ground (common) : Emitter	Input : Base Output : Emitter AC ground (common) : Collector	Input : Emitter Output : Collector AC ground (common) : Base
Av : High Ai : low Zin : high Zout : Low	Av : $AVNL \leq 1$, $AVL \leq 1$ Ai : High Zin : High Zout : Low	Av : High Ai : 1 Zout : high Zin : Very low
Phase change, $V_{out} = -V_{in}$ (180° out of phase)	Vout and Vin are in phase	Vout and Vin are In phase
	Emitter Follower (output at E follows input at B)	
Voltage Amplifier (High Av)	Voltage Buffer with $Av=1$ (Unity Gain Voltage Buffer) Voltage buffer is used to remove loading effect on a load. The loading effect is the effect to which a measurement instrument impacts electrical properties like the voltage, current, and resistance of a circuit. In other words, the Loading effect can be defined as the effect on the source by the load impedance.	Current Buffer ($Ai=1$) Used in high frequency circuit (low Zin) for impedance matching.

Refer to previous notes in Lesson 7

AC Equivalent circuit



$$z_{in(base)} \approx \beta_{ac} (r'_e + R_L)$$

$$z_{in} = R_1 // R_2 // \beta_{ac} (r'_e + R_L)$$

$$z_{out} = R_E // r'_e$$

$$A_{VNL} = \frac{R_E}{r'_e + R_E}$$

$$A_{VL} = \frac{(R_E // R_L)}{r'_e + (R_E // R_L)}$$

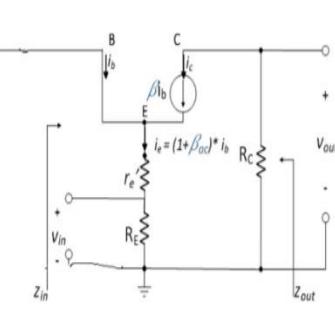
$$A_{VNL} \text{ or } A_{VL} \approx \frac{r_L}{r'_e + r_L} \approx 1$$

Note: AC Load at Emitter

Without load, $r_L = R_E$

With load R_L , $r_L = R_E // R_L$

AC Equivalent circuit



Input impedance, z_{in}

$$z_{in} = R_E // r'_e \\ \approx r'_e$$

Output impedance, z_{out}

$$z_{out} = R_C$$

Current Gain, $A_i \approx 1$

$$A_{VNL} \approx \frac{r_L}{r'_e} \approx \frac{R_C}{r'_e}$$

$$A_{VL} \approx \frac{r_L}{r'_e} \approx \frac{R_C // R_L}{r'_e}$$

Note: AC Load at Collector

Without load, $r_L = R_C$

With load R_L , $r_L = R_C // R_L$

$$V_{out} (\text{with load}) = A_{VL} \times V_{in}$$

$$V_{out} (\text{Without load}) = A_{VNL} \times V_{in}$$

$$i_{out} = V_{out} / R_L$$

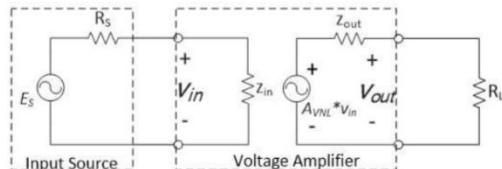
$$i_{in} = V_{in} / Z_{in}$$

$$A_i = i_{out} / i_{in}$$

CC Amplifier

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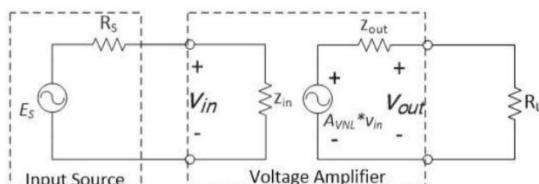
Unity-Gain Voltage Buffer



- An ideal unity-gain voltage buffer has following characteristics:
 - ✓ Voltage Gain is 1
 - ✓ Z_{in} is infinite
 - ✓ Z_{out} is zero
- A voltage buffer is a circuit used to remove loading effect of a low-impedance load, on a high-impedance output circuit
- A CC amplifier has voltage gain of approximately 1, and relatively high input and low output impedances
=> Used as voltage buffer

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Unity-Gain Voltage Buffer



- An ideal unity-gain voltage buffer has following characteristics:
 - ✓ Voltage Gain is 1
 - ✓ Z_{in} is infinite
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- A voltage buffer is a circuit used to remove loading effect of a low-impedance load, on a high-impedance output circuit
- A CC amplifier has voltage gain of approximately 1, and relatively high input and low output impedances
=> Used as voltage buffer



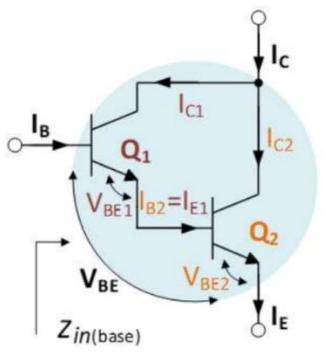
Darlington Pair

Darlington pair uses a special two-transistor configuration to provide **higher current gain (A_i)** and **input impedance (z_{in})** compared to a single transistor

- Very high DC/AC current Gain:

$$\checkmark H_{FE} \approx H_{FE1} \times H_{FE2}$$

$$\checkmark h_{fe} \approx h_{fe1} \times h_{fe2}$$



$$V_{BE} = V_{BE1} + V_{BE2}$$

$$= 0.7V + 0.7V = 1.4V$$

$$z_{in(base)} \approx h_{fe} \times r'_e$$

$$\approx h_{fe1} \times h_{fe2} \times r'_e$$

Multistage Amplifier = Cascaded Amplifier

Multistage Amplifiers

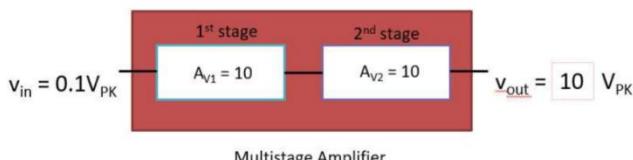
Refer to Smartbook Sec 9-1,



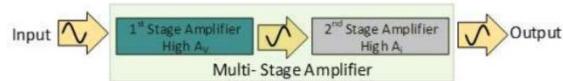
- When two or more amplifier stages can be connected together in series, they are referred to as cascade amplifier
- The overall voltage gain of a cascade amplifier is the product of the stages.

$$\text{Overall Voltage Gain, } A_V = \frac{v_{out}}{v_{in}}$$

$$A_V = A_{V1} \times A_{V2}$$



Best of both world

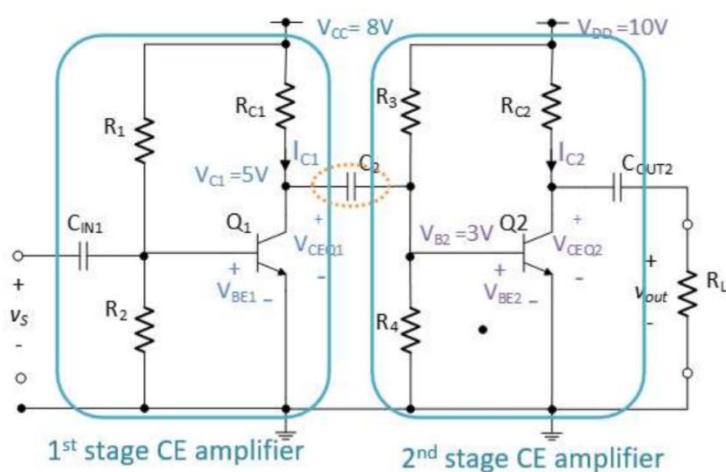


- 1st Stage : To provides high A_v : Use **CE** amplifier
- 2nd Stage : To provides high A_i : Use **CC** amplifier

Multistage Amplifier

1st stage : CE Amplifier

2nd stage : CE Amplifier



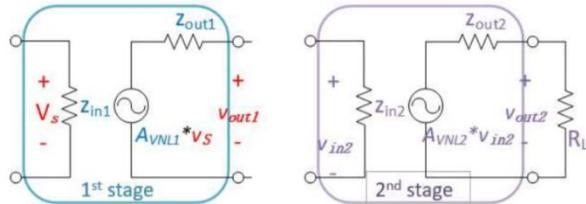
Capacitor , C_2 provides DC isolation in between 2 amplifier stages.

V_{out} of 1st stage = V_{in} of 2nd stage

Multistage Amplifiers – Voltage amplifier model



- Alternatively, **Voltage Amplifier Model** can be used to analyze multistage amplifier
- Individual stages are treated independently before cascading them together



When the above 2 amplifier stages are cascaded together,
 z_{out} of 1st stage will be in series with z_{in} of 2nd stage

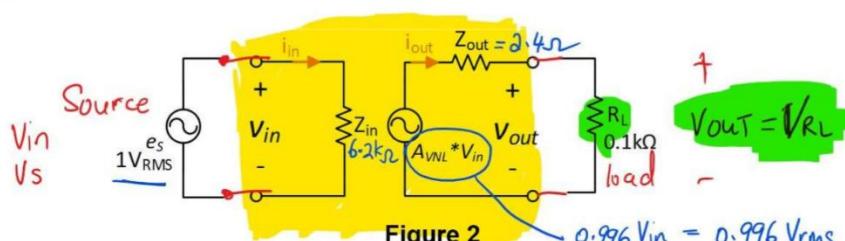
$$V_{in2} = V_{out1} = \frac{Z_{in2}}{Z_{in2} + Z_{out1}} \times A_{VNL1} \times V_s$$

$$V_{out2} = \frac{R_L}{R_L + Z_{out2}} \times A_{VNL2} \times V_{in2}$$

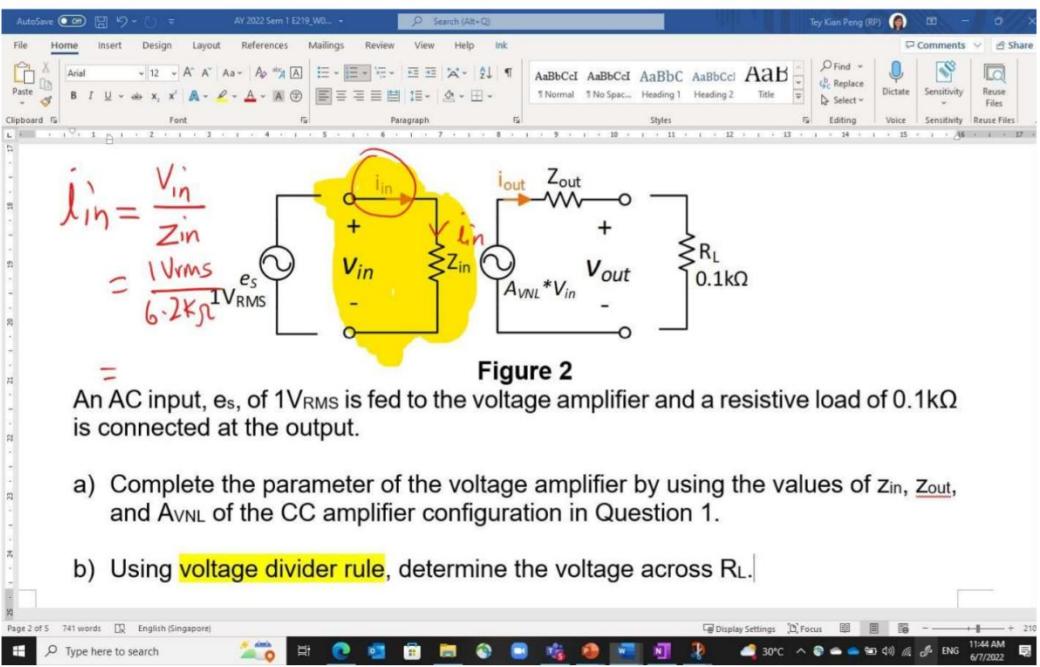
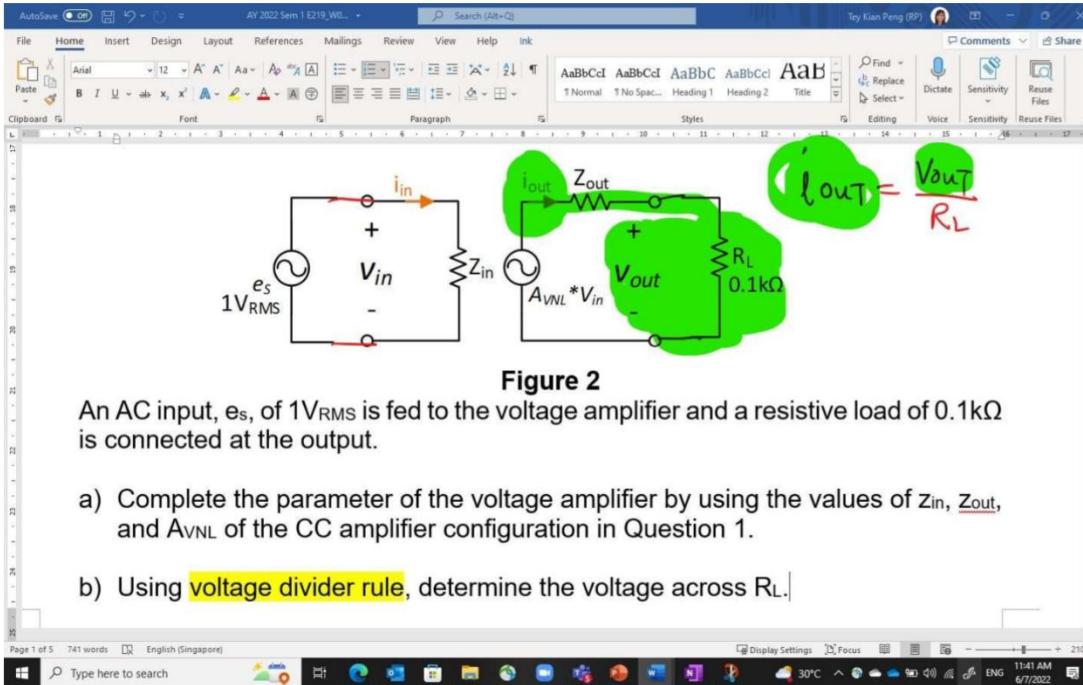
$$\text{Overall loaded voltage gain of multistage amplifier } A_v = \frac{V_{out2}}{V_s}$$

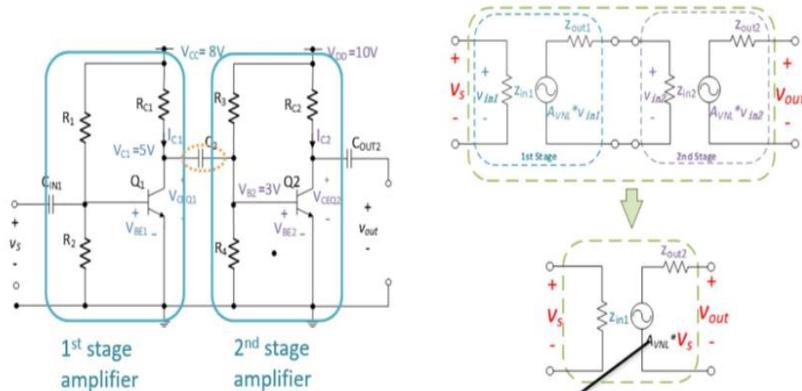
Overall A_{VNL} of multistage amplifier = $A_{VNL1} \times A_{VNL2}$

- 2) The CC amplifier circuit in Figure 1 can be represented by the following voltage amplifier model.



An AC input, e_s , of $1V_{rms}$ is fed to the voltage amplifier and a resistive load of $0.1k\Omega$ is connected at the output.

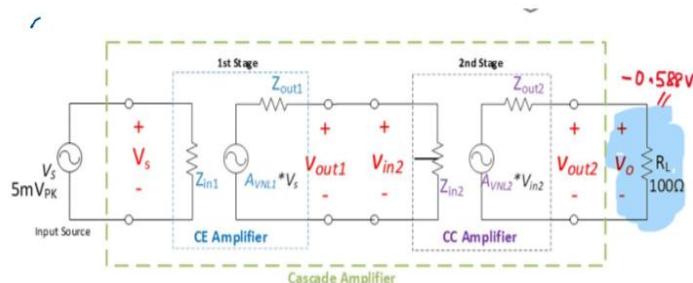




Determine the overall unload voltage gain, A_{VNL}

$$\text{Overall } A_{VNL} \text{ of multistage amplifier} = A_{VL1} \times A_{VNL2}$$

WS Q5



- a) The table listed some of amplifier parameters of each amplifier stage.
Complete the rest of the amplifier parameters in the table.

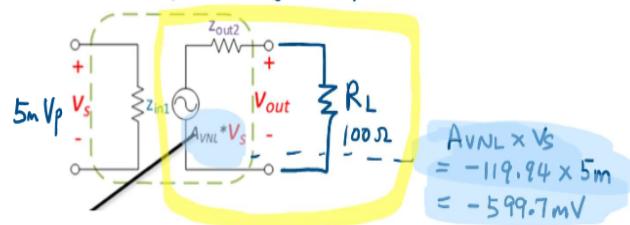
CE Amplifier		CC Amplifier	
h_{fe1}	150	h_{fe2}	180
h_{ie1}	$2k\Omega$	h_{ie2}	<u>4000</u>
Z_{in1}	1.57 k Ω	Z_{in2}	8.17 k Ω
R_c	2k Ω	R_{E2}	1k Ω
r'_{e1}	$= h_{ie1}/h_{fe1} = 2k / 150 = 13.3\Omega$	r'_{e2}	$= h_{ie2}/h_{fe2} = 400 / 180 = 2.22\Omega$
A_{VNL1}	$= -R_c/r'_{e1} = -150$	A_{VNL2}	$= R_{E2} / (r'_{e2} + R_{E2}) = 0.997$
Z_{out1}	$= R_c = 2k\Omega$	Z_{out2}	$= R_{E2} // r'_{e2} = 2.22\Omega$

$$A_{VL1} = \frac{-(R_c // R_L)}{r'_{e1}}$$

$$R_L = Z_{in2} \text{ (cascade amplifier)} = 8.17k\Omega$$

$$A_{VL1} = - \frac{(2k // 8.17k)}{13.3} = -120.3$$

Overall Voltage Amplifier model



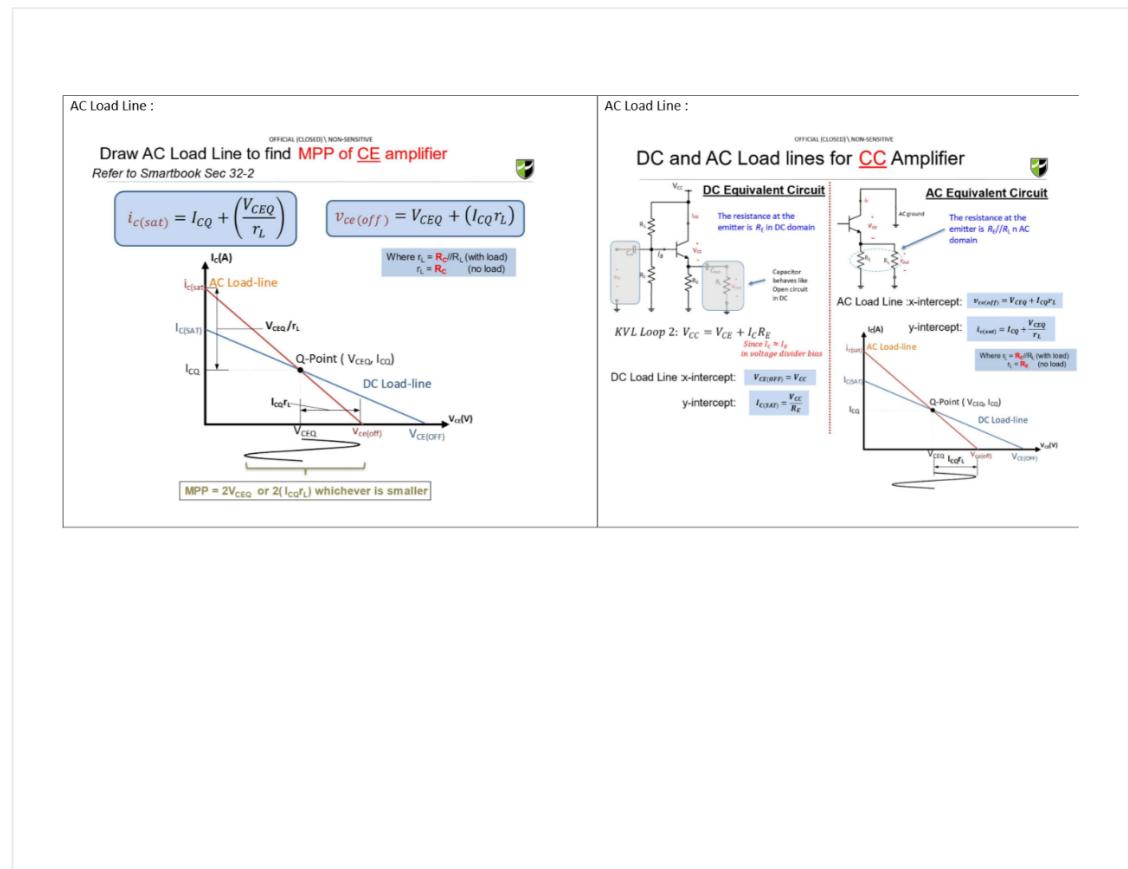
$$A_{VN2} \times V_s \\ = -119.94 \times 5m \\ = -599.7mV$$

$$A_{VN2} = A_{VL1} \times A_{VL2} \\ = (-120.3)(0.997) \\ = -119.94$$

$$V_{out} = \frac{R_L}{R_L + Z_{out2}} \times (A_{VN2} \times V_s) \\ = \frac{100}{100 + 2.22} \times (-599.7mV) \\ = \underline{\underline{0.5867 V_{pk}}} \quad \text{**}$$

LESSON 9 (AC Load Line)

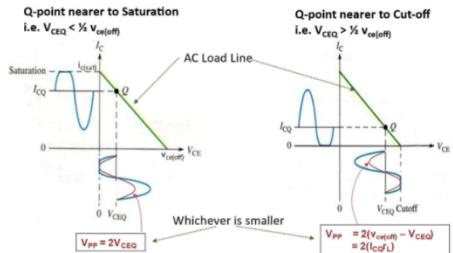
CE (Common Emitter) Amplifier	CC (Common Collector) Amplifier
<p>Input : Base Output : Collector AC ground (common) : Emitter</p> <p>DC Load Line :</p> <p>DC Load Line Graph:</p> <p>$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E}$</p> <p>$V_{CE(OFF)} = V_{CC}$</p> <p>$I_{C(Q)} = I_{CQ} + \frac{V_{CEQ}}{r_L}$</p> <p>$V_{CE(OFF)} = V_{CEQ} + (I_{CQ} r_L)$</p> <p>Where $r_L = R_L / R_L$ (with load) $r_L = R_C$ (no load)</p> <p>Cut-off point</p> <p>Saturation point</p> <p>Q-point (V_{CEQ}, I_{cQ})</p> <p>Cut-off point</p> <p>DC Load Line :</p> <p>DC Load Line Graph:</p> <p>$I_{C(SAT)} = \frac{V_{CC}}{R_E}$</p> <p>$V_{CE(OFF)} = V_{CC}$</p> <p>$I_{C(Q)} = I_{CQ} + \frac{V_{CEQ}}{r_L}$</p> <p>$V_{CE(OFF)} = V_{CEQ} + (I_{CQ} r_L)$</p> <p>Cut-off point</p> <p>Saturation point</p> <p>Q-point (V_{CEQ}, I_{cQ})</p> <p>Cut-off point</p>	<p>Input : Base Output : Emitter AC ground (common) : Collector</p> <p>DC Load Line :</p> <p>DC Load Line Graph:</p> <p>$I_{C(SAT)} = \frac{V_{CC}}{R_E}$</p> <p>$V_{CE(OFF)} = V_{CC}$</p> <p>$I_{C(Q)} = I_{CQ} + \frac{V_{CEQ}}{r_L}$</p> <p>$V_{CE(OFF)} = V_{CEQ} + (I_{CQ} r_L)$</p> <p>Cut-off point</p> <p>Saturation point</p> <p>Q-point (V_{CEQ}, I_{cQ})</p> <p>Cut-off point</p>



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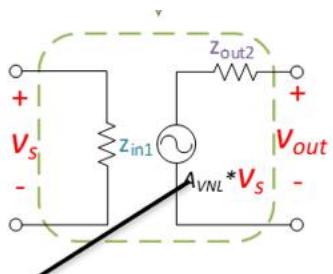
Maximum Possible Peak -to-Peak Output Voltage Swing

The maximum possible peak -to-peak output voltage swing (MPP) is considered based on the following conditions of the AC load -line:



AC load-line would be different from DC load-line!!
They will only intersect at the Q-point

Gradient of AC load line is always steeper than gradient of DC load line.



Lesson 10 (Power Efficiency, Amplifier Class)

Power Efficiency, η

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Refer to Smartbook Sec 32-2



- Efficiency = $\eta = p_{out(ac)} / P_{in(DC)} \times 100\%$

where

$$p_{out(ac)} = \frac{v_{rms}^2}{R_L} = \frac{MPP^2}{8R_L}$$

$$P_{in(DC)} = V_{CC}I_{CC}$$

Relationship
between v_{rms} & v_{pp} ?

- An ideal case of 100% power efficiency would mean a total conversion of DC power to AC power!
- Transistor Power Dissipation:

$$P_{DQ} = V_{CEQ}I_{CQ}$$

- Efficiency for Class-A amplifiers < 25%

What is Class
A Amplifier?

Section 1: Class A Amplifier

Resource: [Class A Amplifier](#)

- Consider the voltage-divider biased Common Emitter (CE) amplifier shown in Figure 1 below.

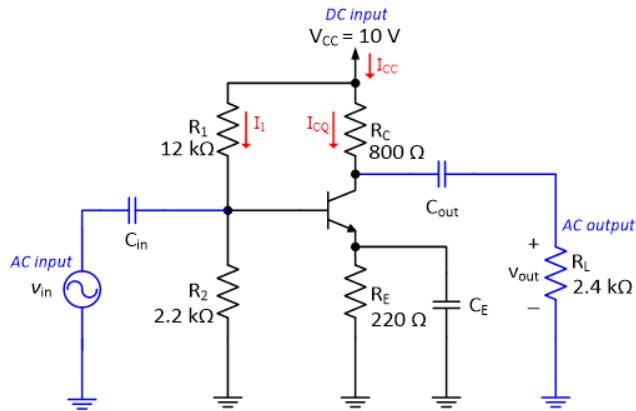


Figure 1

$$I_{cc(\text{sat})} = \frac{V_{cc}}{R_c + R_E}$$

$$r_L = R_C // R_L$$

$$i_{\text{sat}} = I_{cq} + \frac{V_{CEQ}}{r_L}$$

$$V_{ce(\text{off})} = V_{CEQ} + I_{cq} r_L$$

$$M_P = V_{ce(\text{off})} - V_{CEQ}$$

$$M_{PP} = 2 M_P$$

$$P_o(\text{ac}) = \frac{V_{pp}^2}{8R_L} = \frac{M_{PP}^2}{8R_L}$$

$$P_o(\text{ac}) = \frac{V_{rms}^2}{R_L}$$

$$I_{cc} = I_i + I_{cq}$$

$$I_i = \frac{V_{cc}}{R_1 + R_2}$$

$$P_{i(\text{dc})} = V_{cc} (I_{cc}) = V_{cc} (I_i + I_{cq})$$

$$\eta = \frac{P_o(\text{ac})}{P_{i(\text{dc})}} \times 100\% \quad (\%)$$

How Does Class AB Amplifier Work?



DC Power: $P_{DC} = V_{CC} \times I_{CC}$ (for single power supply)

Current from V_{CC} : $I_{CC} = I_{R1} + I_{CQ} + I_{AV}$

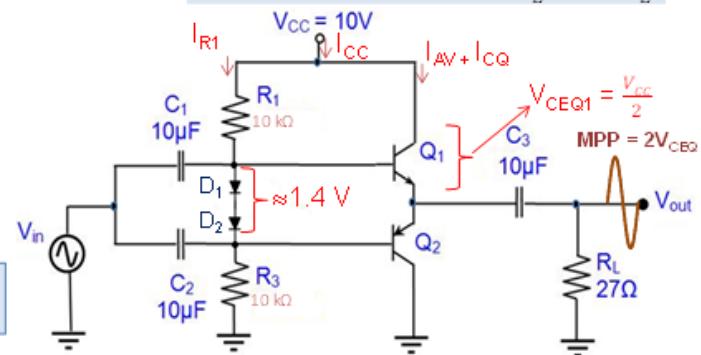
$$I_{CQ} = I_{R1} = \frac{V_{CC} - 2(V_D)}{(R_1 + R_3)}$$

Diode characteristics of D_1 and D_2 are selected to match the base-emitter diode characteristics of the Q_1 & Q_2 transistors

Since Q_1 conducts $\frac{1}{2}$ AC cycle,

$$I_{AV} = \frac{i_{C(sat)}}{\pi} = \frac{V_{CEQ1}}{\pi R_L} = \frac{V_{CC}}{2\pi R_L}$$

$$\text{AC Power: } p_{out(ac)} = \frac{MPP^2}{8R_L} = \frac{V_{CC}^2}{8R_L}$$



- Diode Biasing cause both Q_1 and Q_2 to slightly conduct
- Small amount of I_{CQ}
- Either Q_1 or Q_2 BJT is conducting at any moment, eliminating cross-over distortion

How Does Class AB Amplifier Work?



DC Power: $P_{DC} = (2V_{CC}) \times I_{CC}$ (for dual power supply)

Current from V_{CC} : $I_{CC} = I_{R1} + I_{CQ} + I_{AV}$

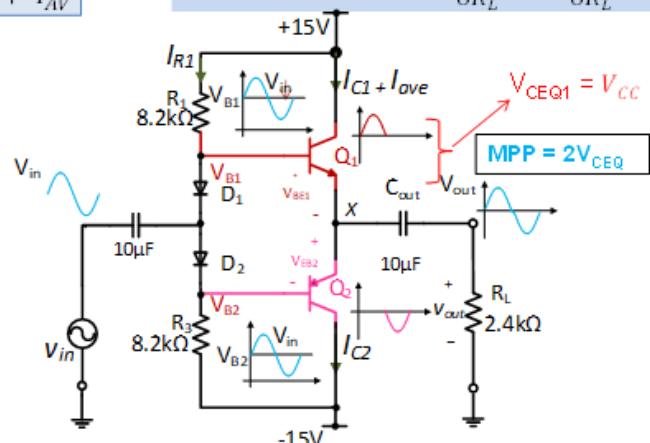
$$I_{CQ} = I_{R1} = \frac{2V_{CC} - 2(V_D)}{(R_1 + R_3)}$$

Diode characteristics of D_1 and D_2 are selected to match the base-emitter diode characteristics of the Q_1 & Q_2 transistors

Since Q_1 conducts $\frac{1}{2}$ AC cycle,

$$I_{AV} = \frac{i_{C(sat)}}{\pi} = \frac{V_{CEQ1}}{\pi R_L} = \frac{V_{CC}}{\pi R_L}$$

$$\text{AC Power: } p_{out(ac)} = \frac{MPP^2}{8R_L} = \frac{(2V_{CC})^2}{8R_L}$$



- Diode Biasing cause both Q_1 and Q_2 to slightly conduct
- Small amount of I_{CQ}
- Either Q_1 or Q_2 BJT is conducting at any moment, eliminating cross-over distortion

Classification of Power Amplifiers



Class	Operating Cycle	Maximum Power Efficiency	Remarks
A	360°	25%	<ul style="list-style-type: none"> Transistor is biased such that the output current flows for the entire cycle of the input signal Operates over the linear range of load line, hence minimum distortion to output waveform
B	180°	78.5%	<ul style="list-style-type: none"> Transistor is at cut-off mode when there is no AC input signal, i.e. Q-point in cut-off region Transistor only conducts for half the input cycle Requires push-pull configuration to achieve full-output cycle
AB	180° to 360°	25% to 78.5%	<ul style="list-style-type: none"> Transistor is biased at a dc level above the zero base current level of class B power amplifiers and above one-half the supply voltage level of class A Reduces distortion in Class B, with improved power efficiency compared to Class A

Others: Class C, D, E....

Class B (dual power supplies)

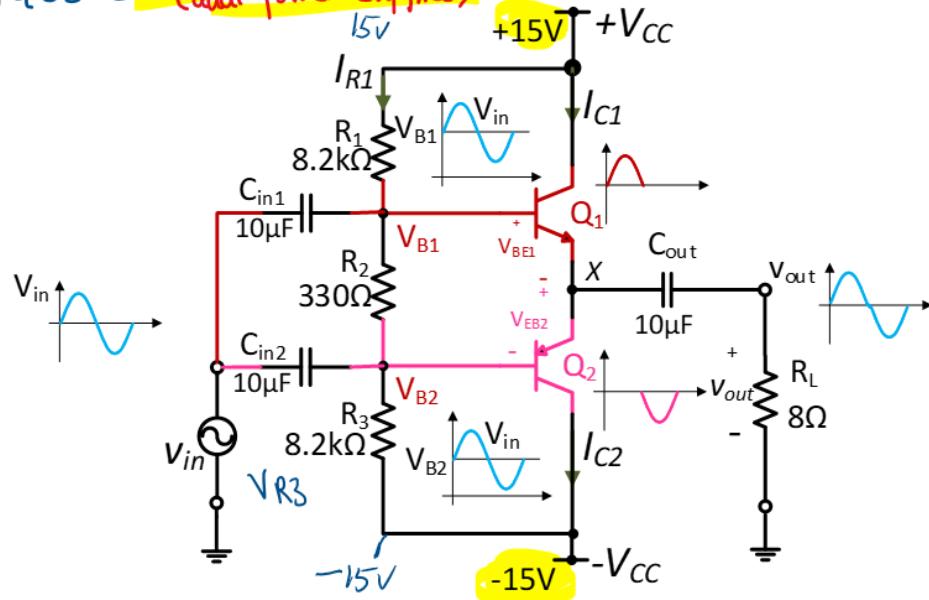


Figure 4

$$V_x = 0V$$

$$I_{R1} = \frac{V_{CC} - (-V_{CC})}{R_1 + R_2 + R_3}$$

$$V_{R1} = I_{R1} \times R_1$$

$$V_{B1} = V_{CC} - V_{R1}$$

$$V_{BE1} = V_{B1} - V_x$$

$$V_{R3} = I_{R1} \times R_3$$

$$V_{B2} = -V_{CC} + V_{R3}$$

$$V_{EB2} = V_x - V_{B2}$$

$$I_{CQ(sat)} = I_{CQ} + \frac{V_{CEQ}}{R_L}$$

$$I_{CQ} = 0A, R_L = R_L$$

$$\therefore I_{CQ(sat)} = \frac{V_{CEQ}}{R_L}$$

$$I_{C1(AVG)} = \frac{I_{CQ(sat)}}{\pi}$$

$$I_{CC} = I_{R1} + I_{C1(AVG)}$$

$$MPP = +V_{CC} - (-V_{CC})$$

$$P_{o(cac)} = \frac{MPP^2}{8R_L}$$

$$P_{o(cac)} = \frac{V_{rms}^2}{R_L}$$

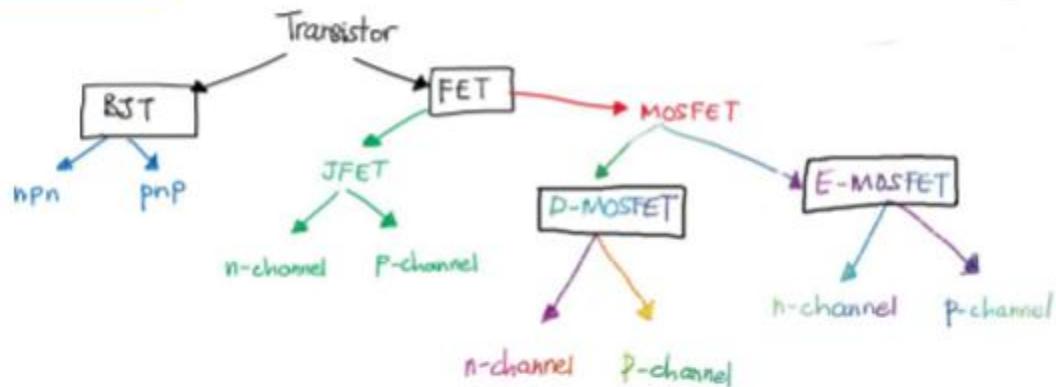
$$P_{o(cac)} = 2V_{CC} \times I_{CC} \\ = 2V_{CC} [I_{R1} + I_{C1(AVG)}]$$

$$\eta = \frac{P_{o(cac)}}{P_{i(cac)}} \times 100\%$$

Lesson 11 (E-MOSFET (DC ANALYSIS), Bias Line Equation)

E219 P11 MOSFET

1) Types of transistors



Keys :

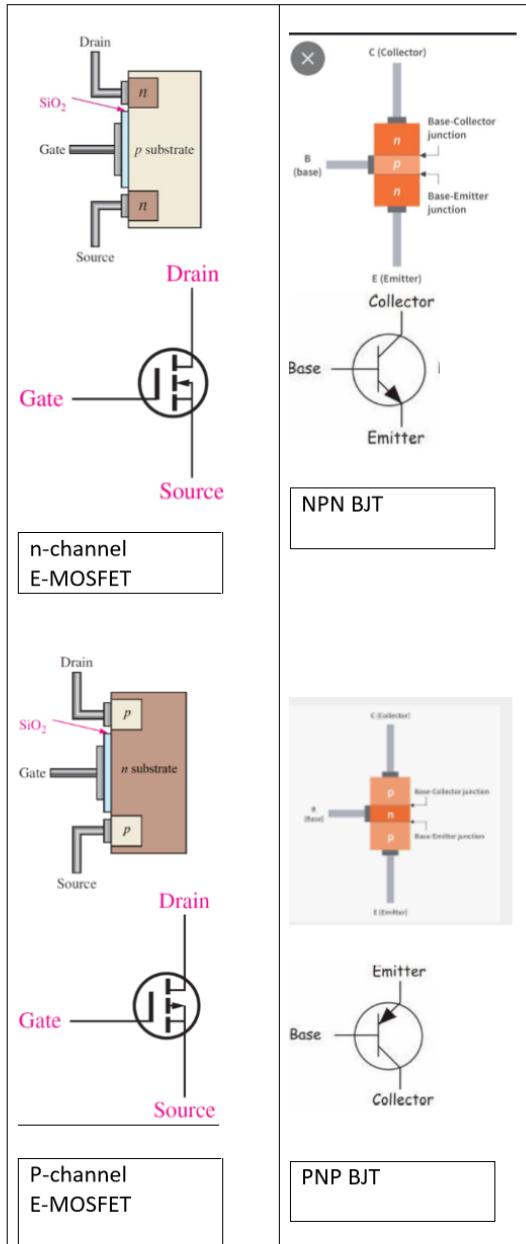
BJT – Bipolar Junction Transistor

FET – Field Effect Transistor

JFET – Junction Field Effect Transistor

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

2) Identify the Transistor Structure



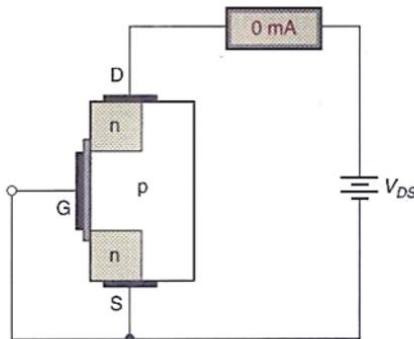
3) Operation of E-MOSFET

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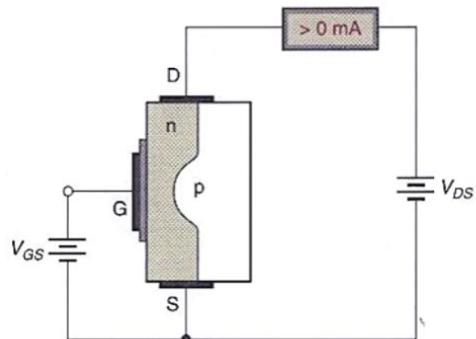
E-MOSFET Operation Mode



- Operates **only** in **enhancement mode**
 - Gate-source voltage V_{GS} needs to be supplied appropriately above the required threshold voltage $V_{GS(th)}$ to form a channel for non-zero drain current I_D to flow
 - For a N-Channel E-MOSFET, as V_{GS} is increasingly positive above the threshold value $V_{GS(th)}$, the channel width increases, hence drain current I_D increases

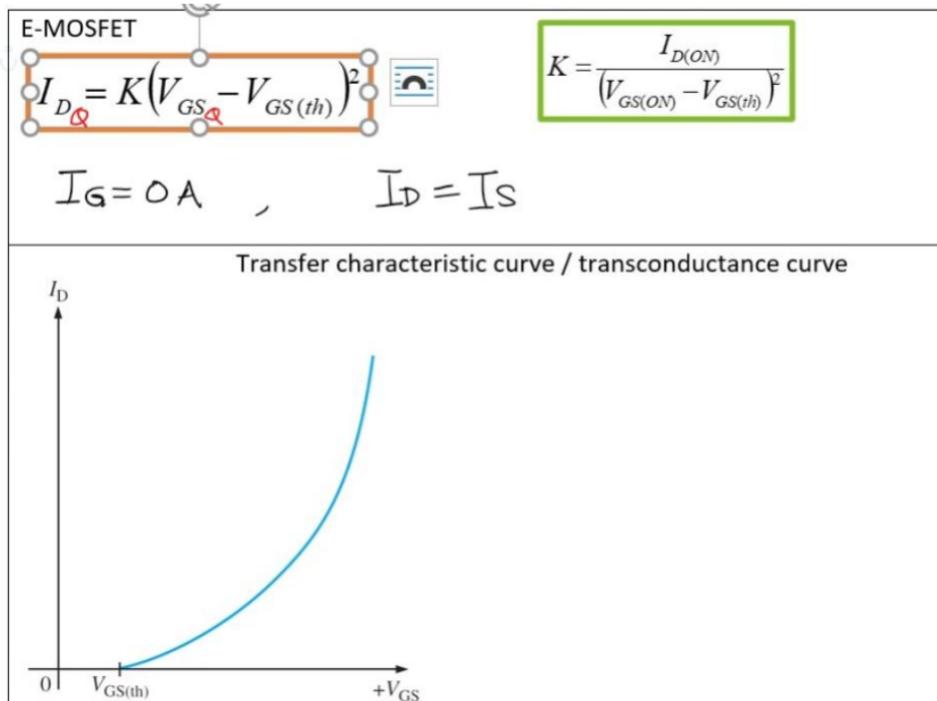


(a) $I_D = 0 \text{ mA}$ when $V_{GS} = 0 \text{ V}$



(b) $I_D > 0 \text{ mA}$ when V_{GS} is sufficient to form a channel.

4) Characteristic equations



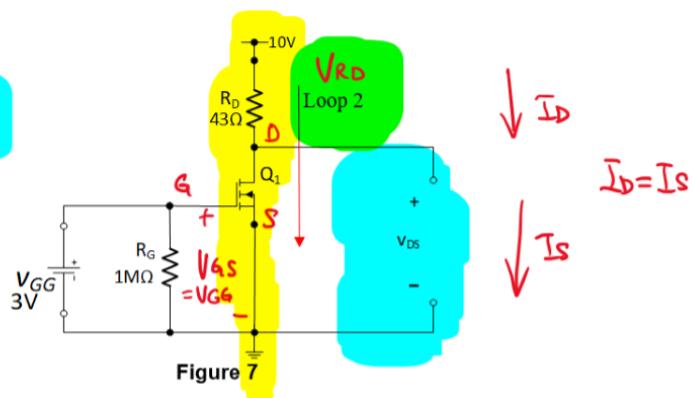
- E-MOSFET is a normally “Off” device because there is absence of inversion layer in the channel when no voltage is applied at the gate terminal, causing the MOSFET to be switched off.
- When a voltage V_{GS} is applied at the gate terminal, an inversion layer will be formed in the channel. When $V_{GS} > V_{th}$, the inversion layer will be formed connecting the source to the drain, switching on the MOSFET.
- $I_G = 0 A$. Due to the thin insulating layer of SiO_2 between the gate terminal and channel.
- As $V_{GS} > V_{GS(\text{TH})}$, the channel width increases (enhance), hence I_D increases.
- The threshold voltage, $V_{GS(\text{TH})}$ of the E-MOSFET can be extracted using the I_D - V_D curve in the simulation file. In this file, the $V_{GS(\text{TH})}$ of 2N7000 NMOSFET is $\sim 2V$.
- E-MOSFET is known as a Voltage Controlled Device as an increase in V_{GS} or V_{DS} results in a increase of channel width, hence increase in the current I_D

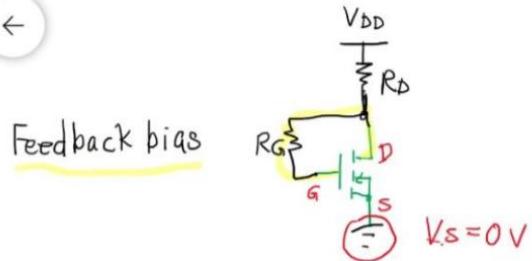
Gate biased

The specified value of $I_{D(ON)}$, at the given value of $V_{GS(ON)}$ can typically be found in E-MOSFET datasheet. Extract those values to calculate the constant k parameter for the following E-MOSFET using typical values.

$$10V = V_{RD} + V_{DS}$$

$$= I_D R_D + V_{DS}$$





1. $I_G = 0 \text{ A}$, $I_D = I_S$

2. $V_{GS} = V_G - V_S \cancel{= 0} = V_G$

3. $V_{DS} = V_D - V_S \cancel{= 0} = V_D$

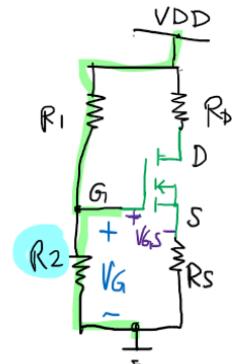
4. $V_G = V_D \therefore V_{GS} = V_{DS}$

5. KVL Loop 2 : $V_{DD} = I_D R_D + V_{DS}$

$V_{DD} = I_D R_D + V_{GS}$ — Bias Line equation.



Voltage Divider Bias



1. $I_G = 0A, I_D = I_S$
2. $V_{DS} = V_D - V_S$
3. $\star \quad V_{GS} = V_G - V_S$
4. $V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$
5. $V_{GS} = V_G - I_D R_S \quad \dots \dots \text{Bias Line equation.}$
6. KVL Loop 2: $V_{DD} = I_D R_D + V_{DS} + I_D R_S$

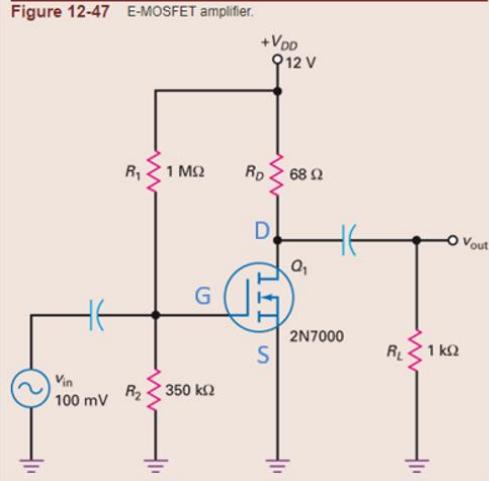
E-MOSFET Biasing: Voltage-Divider Bias (without R_s)

Refer to Smartbook Sec 12-11,



- E-MOSFET Amplifier has to bias at a stable Q-point in **Active region**

$$\bullet \quad V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$



$$\bullet \quad V_S = 0 \text{ V, therefore } V_{GS} = V_G - V_S = V_G$$

$$\bullet \quad \text{Assume } V_{GS} > V_{GS(TH)}$$

$$I_D = k(V_{GS} - V_{GS(TH)})^2$$

$$\bullet \quad \text{From datasheet, find the value of } V_{GS(TH)} \text{ and } I_{D(ON)}. \text{ Hence calculate}$$

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_{GS(TH)})^2}$$

$$\bullet \quad \text{Evaluate K and hence } I_D$$

$$\bullet \quad \text{KVL Loop 2:} \quad V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$

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1 Lesson 11 MOSFET Structure

2 MOSFET Structure

3 MOSFET Structure

4 MOSFET Structure

5 MOSFET Structure

MOSFET Structure
Refer to Smartbook Sec 31-4, Enhancement type MOSFETs

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$V_{GS} \uparrow I_D \uparrow$

Figure 12-10 NMOS schematic symbols: (a) N-channel device; (b) P-channel device.

(a) N-channel device: A schematic diagram showing a p-n-p-n junction. The top p-type layer is the drain, the bottom n-type layer is the source, and the middle p-type layer is the channel. The gate terminal (G) is connected to the top p-layer through a thin insulating layer of SiO_2 . The substrate is connected to the bottom n-layer. A voltage V_{GS} is applied between the gate and source, and a load resistor R_D is connected between the drain and a positive power supply V_{DD} .

(b) P-channel device: A schematic diagram showing a n-p-n-p junction. The top n-type layer is the drain, the bottom p-type layer is the source, and the middle n-type layer is the channel. The gate terminal (G) is connected to the top n-layer through a thin insulating layer of SiO_2 . The substrate is connected to the bottom p-layer. A voltage V_{GS} is applied between the gate and source, and a load resistor R_D is connected between the drain and a positive power supply V_{DD} .

- E-MOSFET is a normally "Off" device. There will be absence of inversion layer in the channel when no voltage is applied at the gate terminal, causing the MOSFET to be switched off.
- When a voltage V_{GS} is applied at the gate terminal, an inversion layer will be formed in the channel. When $V_{GS} > V_{th}$, the inversion layer will be formed connecting the source to the drain, switching on the MOSFET. I_D flow
- There is no gate current I_G flowing in MOSFET. This is due to the thin insulating layer of SiO_2 between the gate terminal and channel.

$I_G = 0 \text{ A}$

Slide 2 of 8 English (Singapore) Accessibility: Investigate

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Lesson 12 (E-MOSFET, AC ANALYSIS)

Lesson 12 Summary

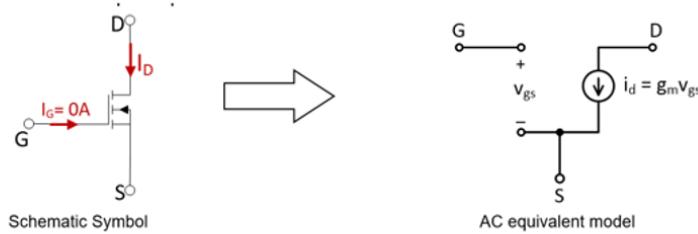
Both BJT and MOSFET \rightarrow Voltage Amplifier

BJT vs MOSFET (in Voltage Amplifier)

- High Av

MOSFET vs BJT (in voltage Amplifier)

- High Z_{in}
- Greater temperature stability
- Smaller size (used in IC)



$$I_D = g_m V_{GS} \quad \text{where: transconductance, } g_m(S) = \frac{\Delta I_D}{\Delta V_{GS}}$$

$A' \frac{A'}{V} \text{ or } S$

g_m : Trans-conductance

$$g_m = 2\sqrt{k \times I_{DQ}}$$

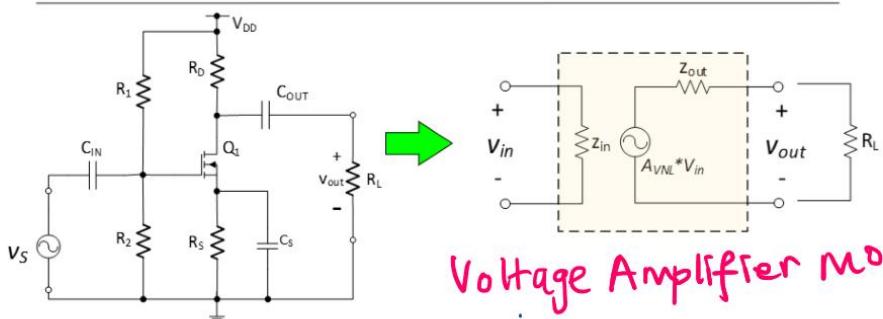
$$g_m = 2k(V_{GSQ} - V_{GS(TH)})$$

$$k = \frac{I_{D(QN)}}{[V_{GS(QN)} - V_{GS(TH)}]^2}$$

$\frac{A}{V^2}$

$$I_D = k [V_{GS} - V_{GS(TH)}]^2$$

Parameters of Interest for a Voltage Amplifier



Voltage Amplifier Model

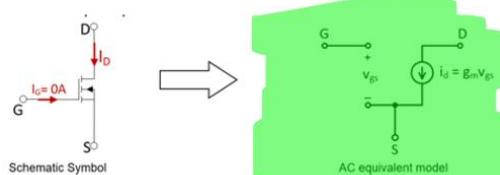
Same as BJT, the same voltage amplifier model can be used for E-MOSFET!

Draw DC Equivalent circuit for E-MOSFET.
Same rule as BJT !

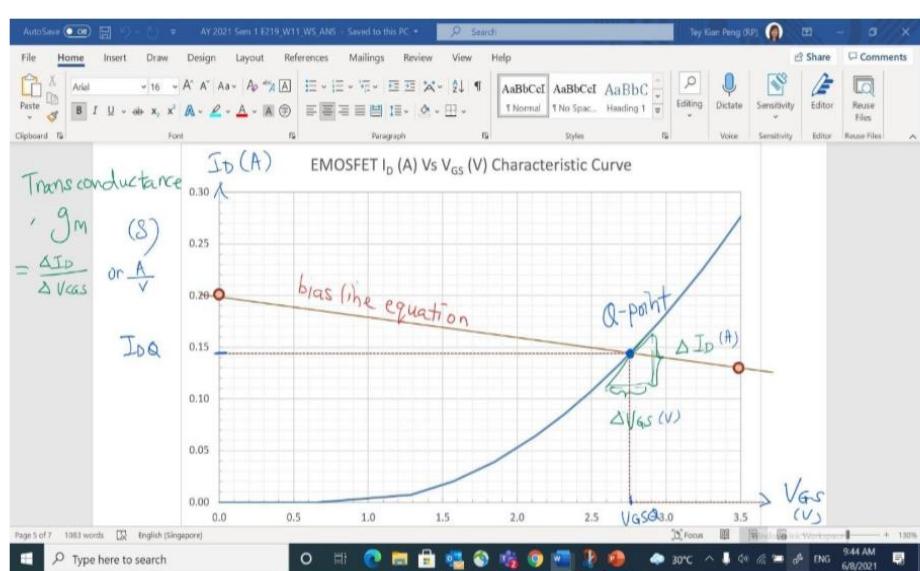
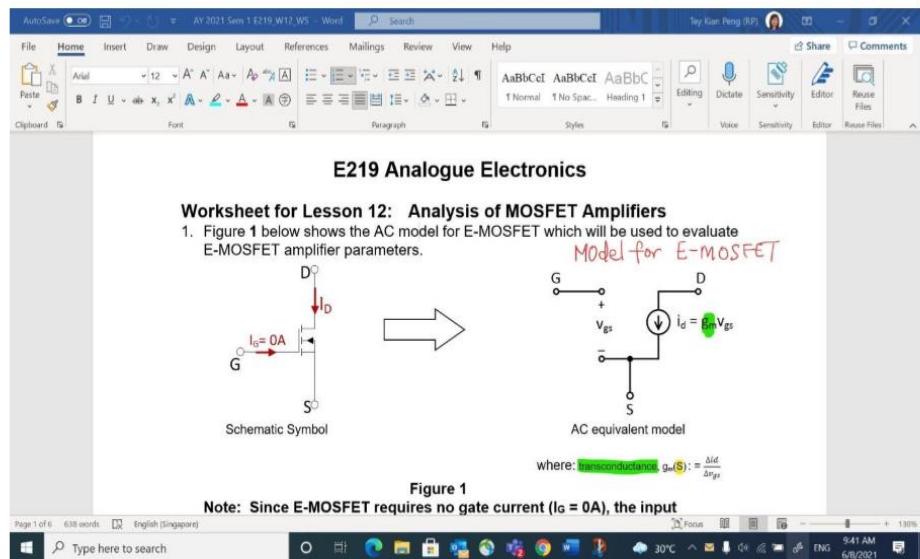
All \rightarrow open

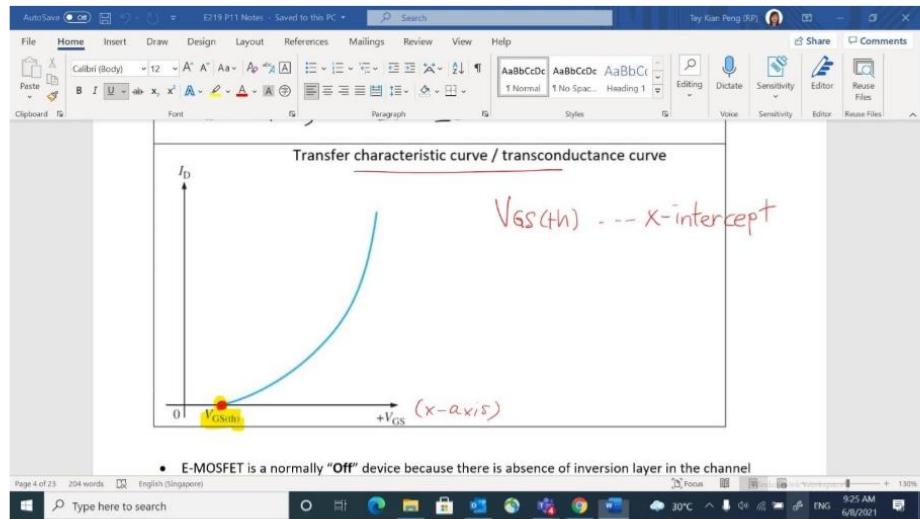
Draw AC Equivalent Circuit for E-MOSFET

Same rule as BJT except you use a different AC equivalent model for E-MOSFET !



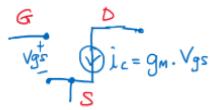
- Replace E-MOSFET with its AC model
- All DC supply to \perp
- All \rightarrow shorted





Draw AC Equivalent Circuit (E-MOSFET)

1. Replace  with AC equivalent model



2. All $\rightarrow \leftarrow$ short \leftrightarrow

3. All DC supplies \perp

$$g_m = 2K(V_{GSQ} - V_{Gsth}) \text{ or } g_m = 2\sqrt{K \times I_{DQ}}$$

$$K = \frac{I_{DQcon}}{(V_{GScon} - V_{Gsth})^2}$$

Unit A/V^2

AC Analysis of Feedback Bias Circuit

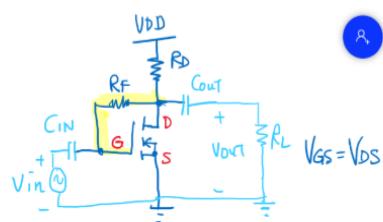
1. Learn to draw AC Equivalent Circuit

2. $A_{VNL} = -g_m R_D$

$$A_{VL} = -g_m (R_D \parallel R_L)$$

$$3. Z_{in} = \frac{R_F}{(1 - A_{VNL})}$$

$$4. Z_{out} = R_D$$



Common Source E-MOSFET
Feedback Bias circuit.

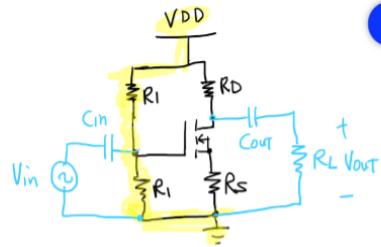
AC Analysis of Voltage Divider Bias circuit

1. Learn to draw AC Equivalent Circuit

$$A_{VNL} = -g_m R_D$$
$$A_{VL} = -g_m (R_D \parallel R_L)$$

$$Z_{in} = R_1 \parallel R_2$$

$$Z_{out} = R_D$$



Common Source E-MOSFET
Voltage Divider Bias circuit