Title

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Overview

Analog multipliers working principles

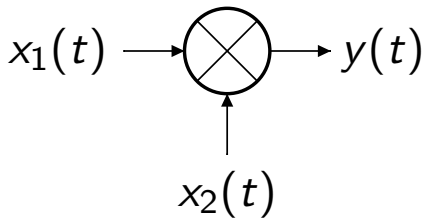


Figure: Representation of a mixer

Analog Multiplier circuit that performs the product between two signals. Spectral components from a certain frequency band are moved to another by means of intrinsic non-linear behaviour (modulation).

Analog multipliers working principles

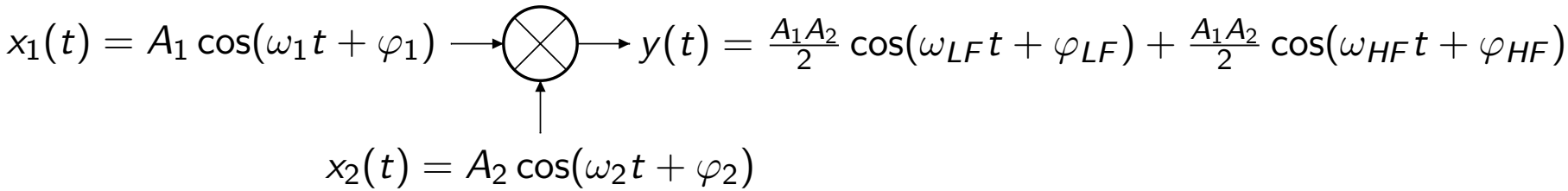


Figure: Working principle

Given two signals

$$x_1(t) = A_1 \cos(\omega_1 t + \varphi_1)$$
$$x_2(t) = A_2 \cos(\omega_2 t + \varphi_2)$$

The output is

$$y(t) = x_1(t) \cdot x_2(t)$$

Analog multipliers working principles

$$
\begin{aligned}
y(t) &= x_1(t) \cdot x_2(t) \\
&= A_1 A_2 \cos(\omega_1 t + \varphi_1) \cos(\omega_2 t + \varphi_2) \\
&= \frac{A_1 A_2}{2} \{\cos[(\omega_1 - \omega_2)t + \varphi_1 - \varphi_2] + \cos[(\omega_1 + \omega_2)t + \varphi_1 + \varphi_2]\} \\
&= A \cos(\omega_{LF} t + \varphi_{LF}) + A \cos(\omega_{HF} t + \varphi_{HF})
\end{aligned}
$$

Two **new** out-of-phase spectral component at output:

Down-converted at lower frequency: $\omega_{LF} = |\omega_1 - \omega_2| < \omega_1, \omega_2$

Up-converted at higher frequency: $\omega_{HF} = |\omega_1 + \omega_2| > \omega_1, \omega_2$

Analog multipliers working principles

Mixers are *bi-direction* three-port. At each port a signal is associated

- RF radio frequency component, high frequency signal;
- IF intermediate frequency component, low frequency signal;
- LO local oscillator (pump), provided by external source.

Depending on input/output signal configuration we can have *downconverting* or *upconverting* modulators.

Figure: Working configuration: downconversion (right), upconversion (left).

Analog multipliers working principles

Depending on which **devices** are employed and driving mode one has:

Passive mixers switches (diodes and transistors) are used introducing *conversion loss*;

Active mixers amplifying devices are used with the possibility of *conversion gain*.

Depending on the circuit **architecture** one has:

Single balanced mixers one input component is suppressed at output, one can pass through the circuit though;

Double balanced mixers circuit symmetries performs the rejection of both input component at the output.

nMOS-based mixer

Suppose to drive a nMOSFET gate with two-tone signal, one has:

$$v_{GS}(t) = v_{RF}(t) + v_{LO}(t)$$
$$i_D(t) = k(v_{GS}(t) - V_{th})^2$$

having $v_{RF} << v_{LO}$:

$$\begin{aligned} i_D(t) &\simeq k(v_{LO}(t) - V_{th})^2 + 2k(v_{LO}(t) - V_{th})v_{RF}(t) \\ &= I_D(t) + g_m(t)v_{RF}(t) \end{aligned}$$

that is called Small Signal Large Signal Model. We have possibility of **gain**.

Mixer figures of merit

To qualify the mixer operation some figures of merit are defined (downconversion mixer):

- **Conversion gain**

$$A_{conv} = \frac{P_{IF}}{P_{RF}}$$

whose behaviour is linear in log scale:

$$P_{IF}|_{dB_m} = A_{conv}|_{dB} + P_{RF}|_{dB_m} + 30dB$$

- **1dB compression point** due to gain saturation caused by harmonic distortion at too high input power values:

$$P_{IF}|_{-1dB} = P_{IF}|_{dB_m,ideal} - 1dB$$

Mixer figures of merit

- **Third order distortion** most important output spurious contribution due to gain compression:

$$i_D(t) = I_D|_{V_{GS}} + a v_{gs}(t) + b v_{gs}^2(t) + c v_{gs}^3(t) + \dots$$
$$\propto a v_{gs}(t) + b v_{gs}^2(t) + \frac{3}{4} c \cos(\omega_0 t) + \frac{1}{4} c \cos(3\omega_0 t)$$

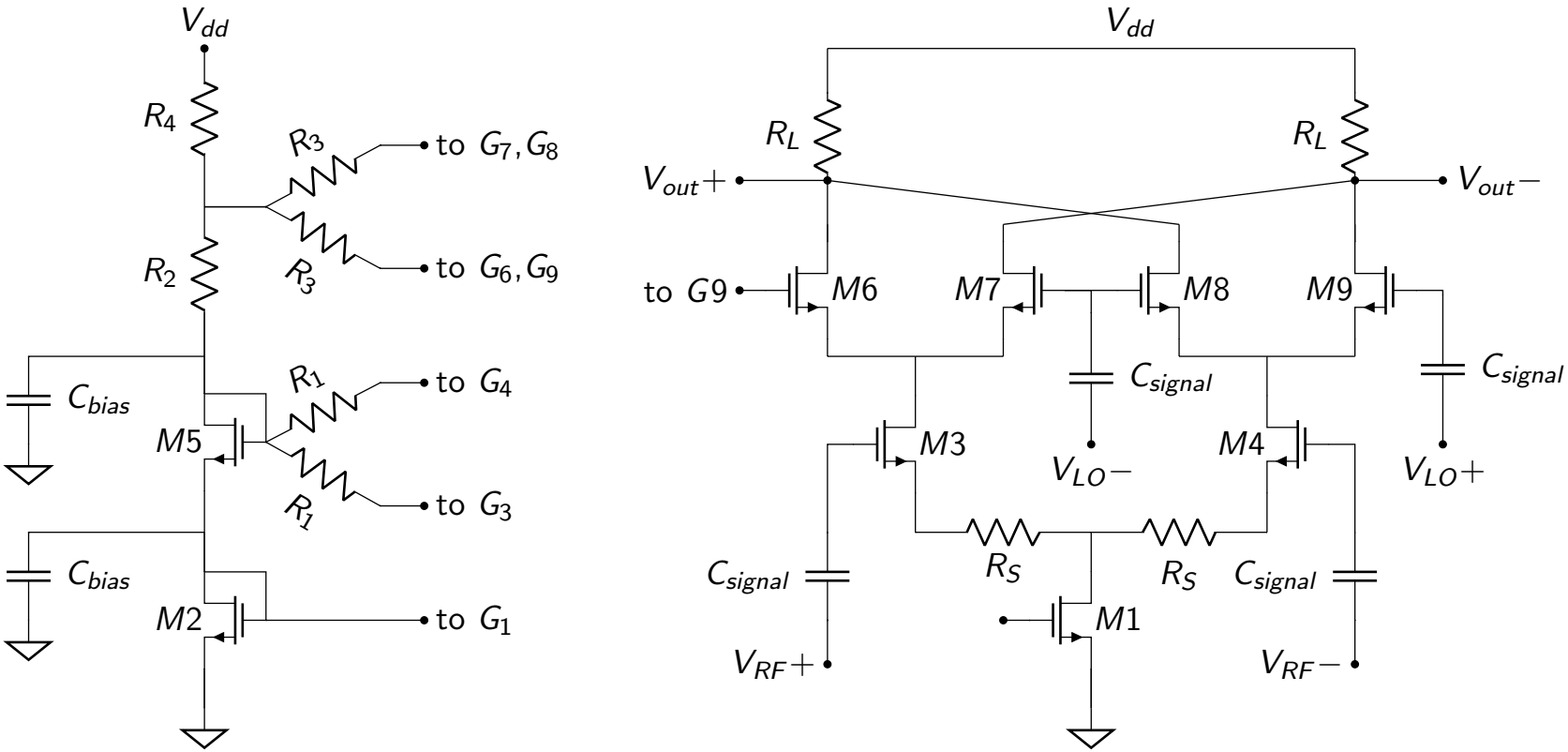
  Even order distortion gives additional DC offset, odd order distortion gives always in-band unwanted components.

- **Third order intermodulation** it happens with two-tone input signals because of frequency intermodulation. Most important contribution comes from IM_3: $m = \pm 2, \pm 1$ and $n = \pm 2, \pm 1$. Given $f_{RF1} = f_0$ and $f_{RF2} = f_0 + \delta f$:

$$f_{IF,IM3}|_{m=2,n=-1} = 2 f_{RF1} - f_{RF2} - f_{LO} = f_{IF} - \delta f$$

1. Analog multipliers theory
   - Introduction
   - Analysis of a Gilbert cell based multiplier
2. Circuit design
   - Design by hand of a down-converting Gilbert cell
   - Design by simulation
   - Layout of the Gilbert cell
3. Simulation vs schematic
   - Simulation setup
   - Time and frequency domain analysis

Gilbert cell circuit analysis - Bias net



(a) *Bias net* (b) *Gilbert cell*

Figure: Full schematic

Gilbert cell overview

A Gilbert-cell mixer is an active double-balanced analog multiplier. This topology provides:

- Reasonable conversion gain;
- Good input frequency components rejection at the output port, high linearity;
- Good isolation between ports;
- Integrability in CMOS technology.

We can recognise **four main blocks**: bias net, gain stage, mixing stage and load.

Gilbert cell circuit analysis - Bias net

The bias net includes:

- Current mirror: M_1, M_2;
- Voltage reference generator: M_5, R_1, R_2, R_3, R_4 and R_5.

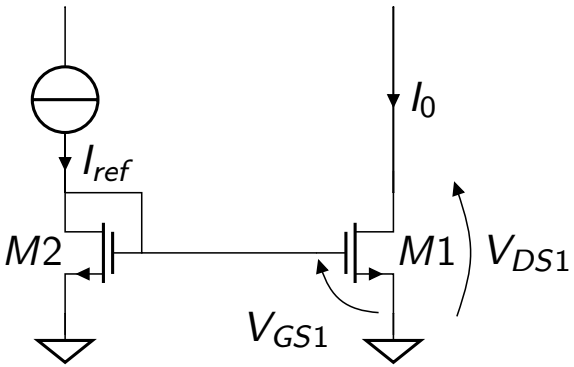


Figure: Current mirror

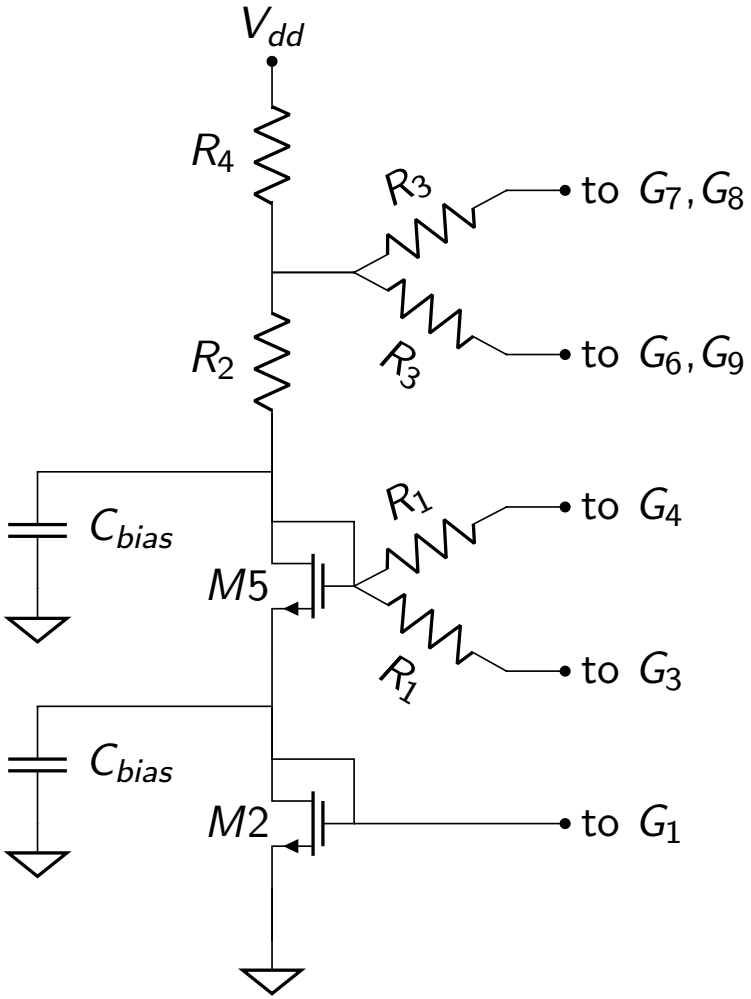


Figure: Biasing network

Gilbert cell circuit analysis - Bias net

Current sink's transistors are in **saturation** (high output resistance, better current source), therefore $V_{GS} \geq V_{th}$ and $V_{DS} > V_{od} = V_{GS} - V_{th}$. M_2 is diode connected, therefore the requirement holds only for M_1:

$$V_{DS1} \geq V_{od1} = V_{th} - \sqrt{\frac{2I_0}{\beta_n}}$$

In saturation, if transistors are identical:

$$I_0 = \frac{\beta_{n1}}{2}(V_{GS1} - V_{th})^2(1 + \lambda_1 V_{DS1})$$

$$I_{REF} = \frac{\beta_{n2}}{2}(V_{GS1} - V_{th})^2(1 + \lambda_1 V_{GS1})$$

Hence:

$$\frac{I_0}{I_{REF}} = \frac{W_1/L_1}{W_2/L_2}$$

Gilbert cell circuit analysis - Bias net

Ideally current mirroring only dependent on **geometrical** parameters.
However:

- To have good current source long channel required, since $r_o = 1/\lambda I_0 \propto L$. Using short channel devices i_D more dependent on λ and tolerances;
- Due to fabrication precision, MOSFET's parameters may vary:

$$\frac{I_0}{I_{REF}} \simeq 1 + \frac{\Delta K_n}{K_n} + 2\frac{\Delta V_{th}}{V_{od}}$$

Wide circuits, temperature gradients and small overdrive voltage significantly induce mirroring errors.

Gilbert cell circuit analysis - Bias net

- M5 is diode connected.
- R2 and R4 make a resistive voltage divider used to bias the mixing stage.
- R1 and R3 are used to bias net to the gain stage. They also acts as high impedance for the RF and LO signals coming from outside the circuit and prevents them to be injected into the bias net.
- Capacitors C1 and C2 shunt possible non-DC disturbances coming from the Gilbert cell, improving the bias net isolation.

Gilbert cell circuit analysis - Gain stage

The gain stage is the mixer's **linear amplifier**. It must handle the power coming from the input RF signal with low distortion, providing some amplification:

- M_3 and M_4 are common source degenerated differential pair affected by body effect0;
- R_S are degeneration resistances.

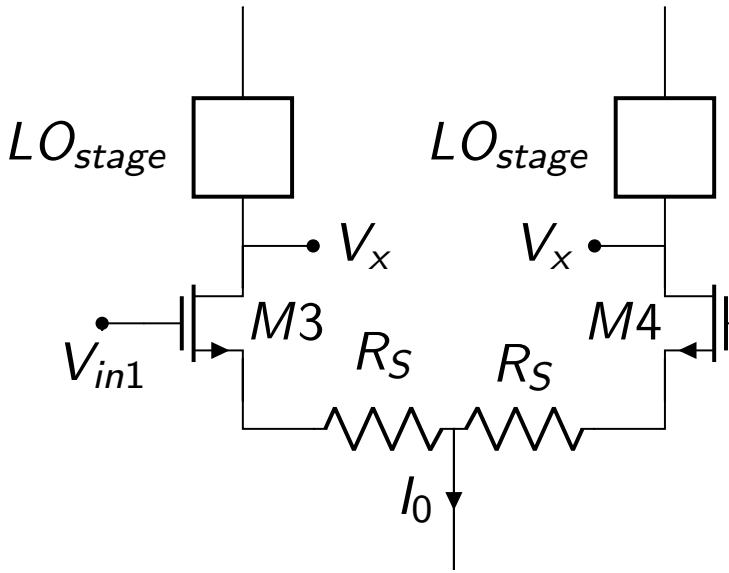


Figure: Gain stage.

Gilbert cell circuit analysis - Gain stage

Since this is a differential pair each transistor transconductance is given by $g_m = \sqrt{\beta_n I_0}$. Thanks to source degeneration we reduce bias dependency and increase **linearity** (high order harmonics suppression). The equivalent transconductance is:

$$G_{m,eq} = \frac{g_m}{1 + g_m R_S}$$

Linearity and low noise properties are also achieved by increasing transistors' dimensions. Output voltage V_X could be affected by changes in parameters, affecting the whole circuit symmetry. The error voltage is given by:

$$V_{o,offset} = \Delta Vth + \frac{V_{GS} - V_{th}}{2}\left(- \frac{\delta R}{2R}\frac{\Delta W/L}{2W/L}\right)$$

Gilbert cell circuit analysis - Mixing stage

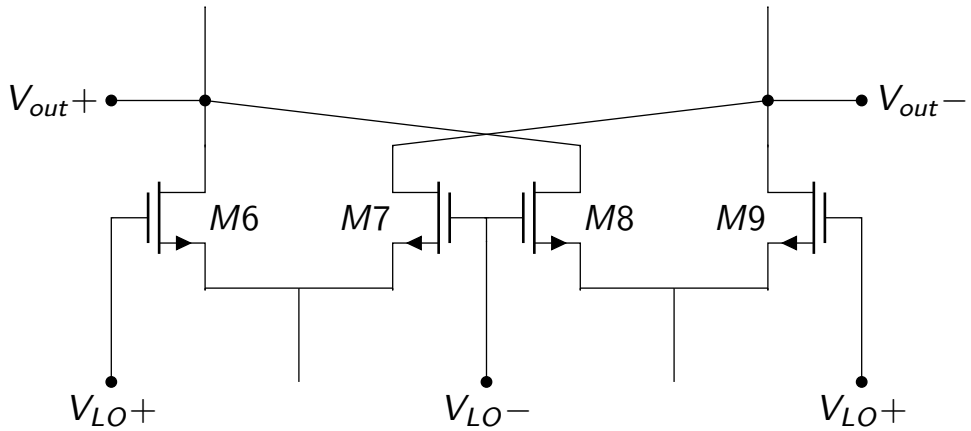


Figure: Mixing stage

Mixing stage is made up of switching-like driven transistors that acts as **pulse amplitude modulators**. A complementary sinusoidal signal is applied to the gates of each pair (V_{LO}), large enough to ensure the **abrupt switching** of one MOSFET whereas the other must be kept in saturation (not in triode!).

Gilbert cell circuit analysis - Mixing stage

Compromise in driving signal required:

- small amplitude of LO signals produce slower switching speed and power waste as common mode signal at the output;
- too large LO signals drive the device in triode, producing spikes and unwanted feed-through reducing overall speed.

Switching speed is related to MOSFET transition frequency:

$$f_T \propto V_{od}/L$$

Then fast devices are obtained with **short channel** length and **large overdrive**. Larger devices introduce parasitic capacitance, detrimental for the conversion efficiency and speed. Maximum working frequency must be below $f_T/10$.

Gilbert cell circuit analysis - Mixing stage

Mixing stage is non linear, however given the square wave current flowing through each device:

$$i_D(t) = I_{pk}\left(\frac{1}{2} - \frac{2}{\pi}\sum_{n=1,3,5\ldots}\frac{1}{n}\sin(n\omega t)\right)$$

one has the instantaneous gain:

$$A_c|_{switch} = \frac{2}{\pi}$$

associated to first harmonic, ideally not depending on device properties. For real devices the actual gain is lower.

Gilbert cell circuit analysis - Load stage

Two resistors are employed as loads. They are required to provide enough gain to the stage, active loads are not necessary since overall gain is low. They are less noisy than transistors (Flicker noise at low frequency), less reliable for what concern tolerances though.

Gilbert cell circuit analysis - Conversion gain

The circuit is non-linear, therefore it is not possible to define a gain. It can be demonstrated that the **conversion gain** for the cell is:

$$A_{vC} = \frac{V_{IF,rms}}{V_{RF,rms}} = \frac{2}{\pi} \frac{R_L}{\frac{1}{g_{m3,4}} + R_S}$$

Some important facts hold:

- in first approximation the conversion gain does not depends on the amplitude of the LO signal;
- both LO and RF components are rejected at the output;

Gilbert cell circuit analysis - Conversion gain

$$A_{vC} = \frac{V_{IF,rms}}{V_{RF,rms}} = \frac{2}{\pi} \frac{R_L}{\frac{1}{g_{m3,4}} + R_S}$$

- it is possible to keep only the IF component by filter out the HF signal;
- the degeneration resistance R_S improve the stage's linearity. In fact, if properly chosen, one has: $A_{vC}|_{g_m 3,4 \ll R_S} \simeq \frac{2}{\pi} \frac{R_L}{R_S}$. Besides to linearity, the conversion gain is less sensitive with respect to the RF stage bias point;
- no informations about frequency behaviour appear with this kind of analysis.

Design specifications

Technology and purposes

Technology used is MOSIS AMI 0.6μm. Loose constraint of $\sim 1mm$ is taken for maximum gate width. This technology is old fashioned and not the best for this purpose.

Supply voltage

Supply voltage is chosen $5V$

Frequencies

Single frequency down-converting mixer with:
f_{RF}=110 MHz, f_{LO}=100 MHz, f_{IF}=10 MHz.

Conversion Gain

Voltage conversion gain is chosen A_{vC}=4. All transistors are supposed saturated.

Used parameters

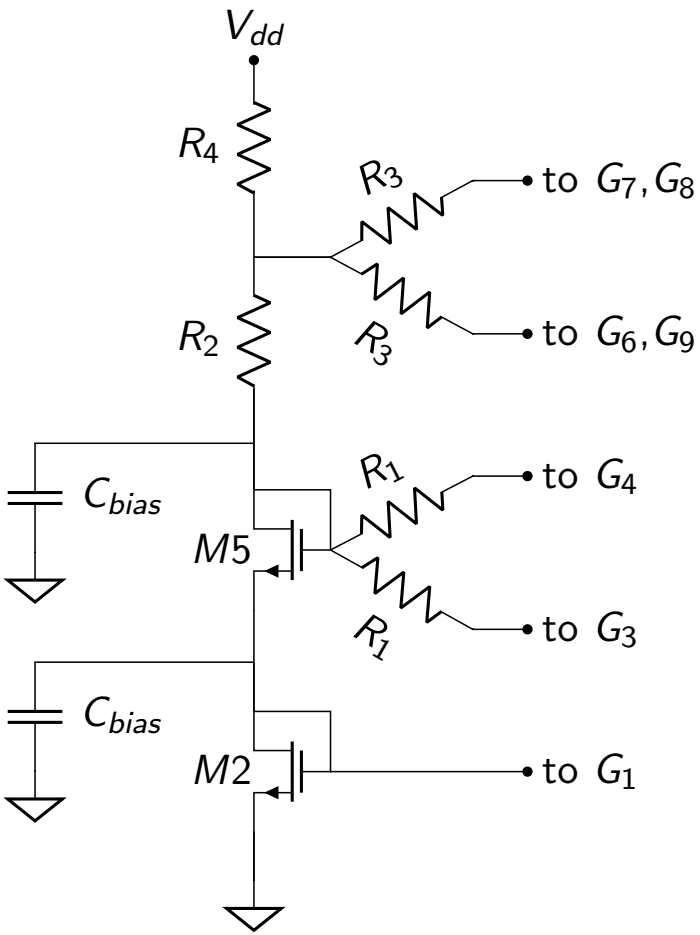
Table

Parameter	Name	Value	Unit
A_{vC}	Voltage Conversion gain	4	
V_{DD}	Supply voltage	5	V
I_0	Cell biasing current	5	mA
V_{th0}	n-MOS threshold w.o. body effect	0.709	V
K_n	n-MOS physical parameter	116	$\mu A/V^2$
I_{dss}	Maximum channel current density	466	$\mu A/\mu m$
ϕ_P	Fermi potential	0.7	V
γ_B	Body effect coefficient	0.5	V
L_{min}	Technology minimum length	0.6	μm

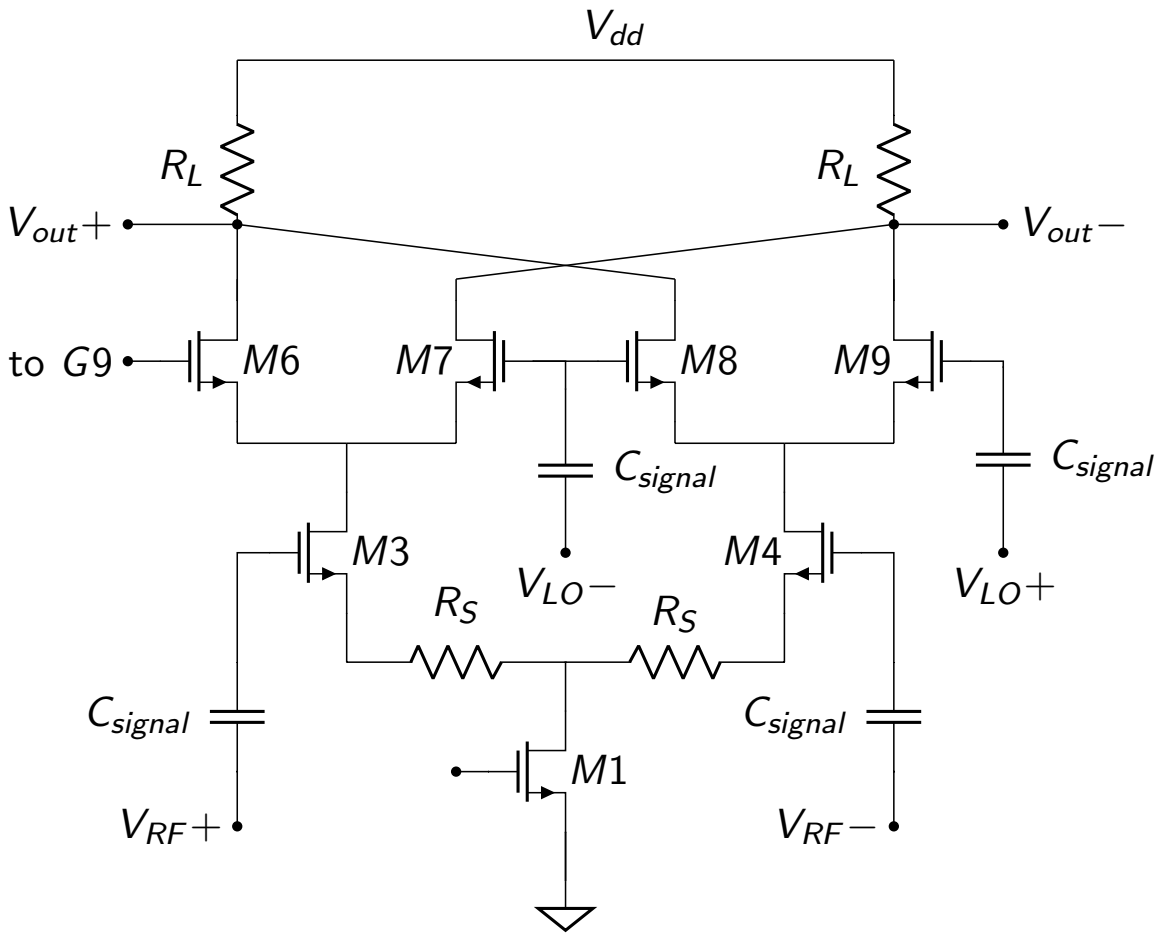
Gilbert Cell design (by hand)

1. Bottom-up design
2. Level 1 model
3. Results: affected by short channel effects. led to redesign on CAD tool, but reported as follows for the sake of completeness.

Reference schematic



(a) *Bias net*



(b) *Gilbert mixer*

Figure: Bias net and Gilbert Mixer schematic

Current bias design

To have good mirroring this must be satisfied:

$$V_{GS1} = V_{VGS2}$$
$$V_{DS1} = V_{DS2}$$
$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

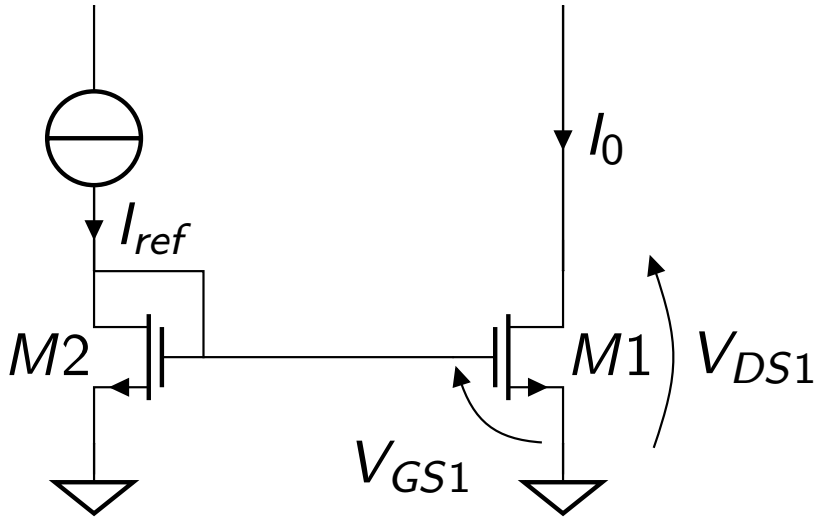


Figure: Biasing current mirror

Current bias design

Valu we chose to impose are:

$$I_{ref} = I_0 = 5mA$$
$$V_{od1} = V_{od2} = 0.4V$$
$$L_1 = L_2 = 3L_{mim} = 1.8\mu m$$

from which we derive...

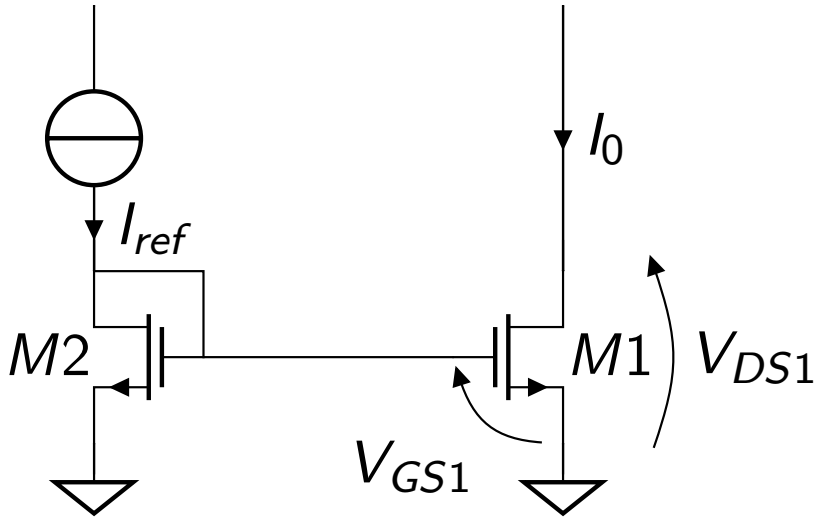


Figure: Biasing current mirror

Current bias design

...we derive gate width and gate bias

$$W_1 = \frac{2I_0}{K_n V_{od1}^2} L_1 = 969.8\mu m$$

$$V_{th1} = V_{th2} = V_{th0}$$

(Since there's no body effect)

$$V_{GS2} = V_{DS2} = V_{th0} + \sqrt{\frac{2I_0 L_1}{K_n W_1}} = 1.1V$$

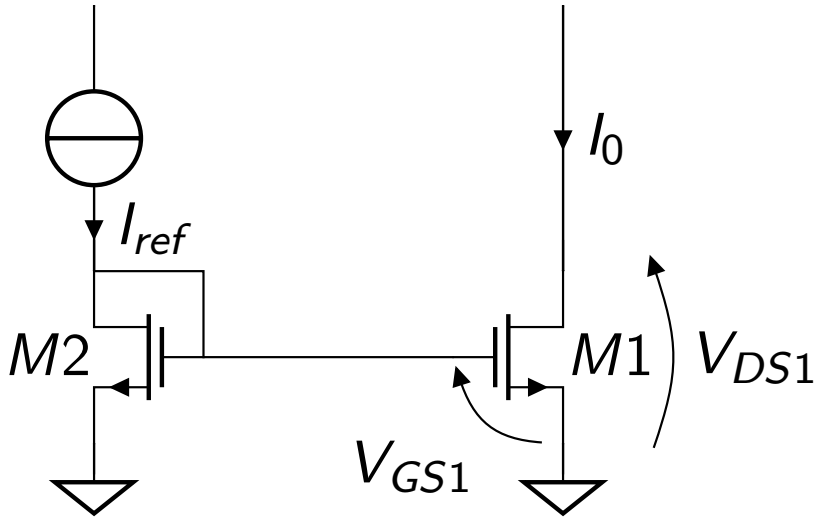


Figure: Biasing current mirror

Load resistance design

I_0 is evenly split into M3 and M4. Since LO transistors are turned on only two at a time, in each LO transistor flows also half I_0 when on. In order to have enough output swing we decided to drop across the load:

$$V_{R_L} = \frac{1}{3} \cdot V_{DD}$$

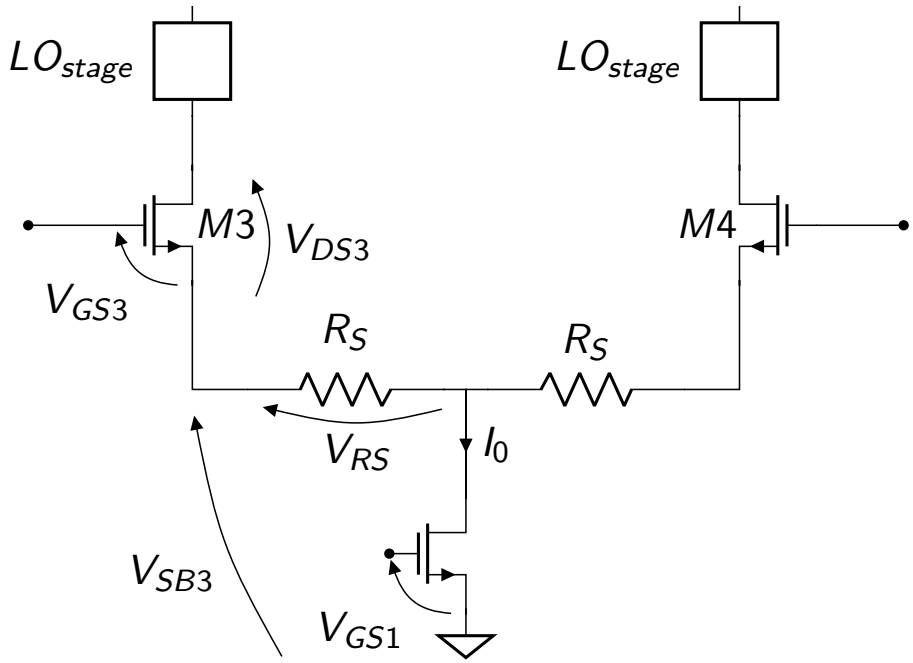


Figure: Current split in LO stage

Load resistance design

This leads to the choosing of load

$$R_L = \frac{\frac{1}{3}V_{DD}}{I_0/2} = 667\Omega$$

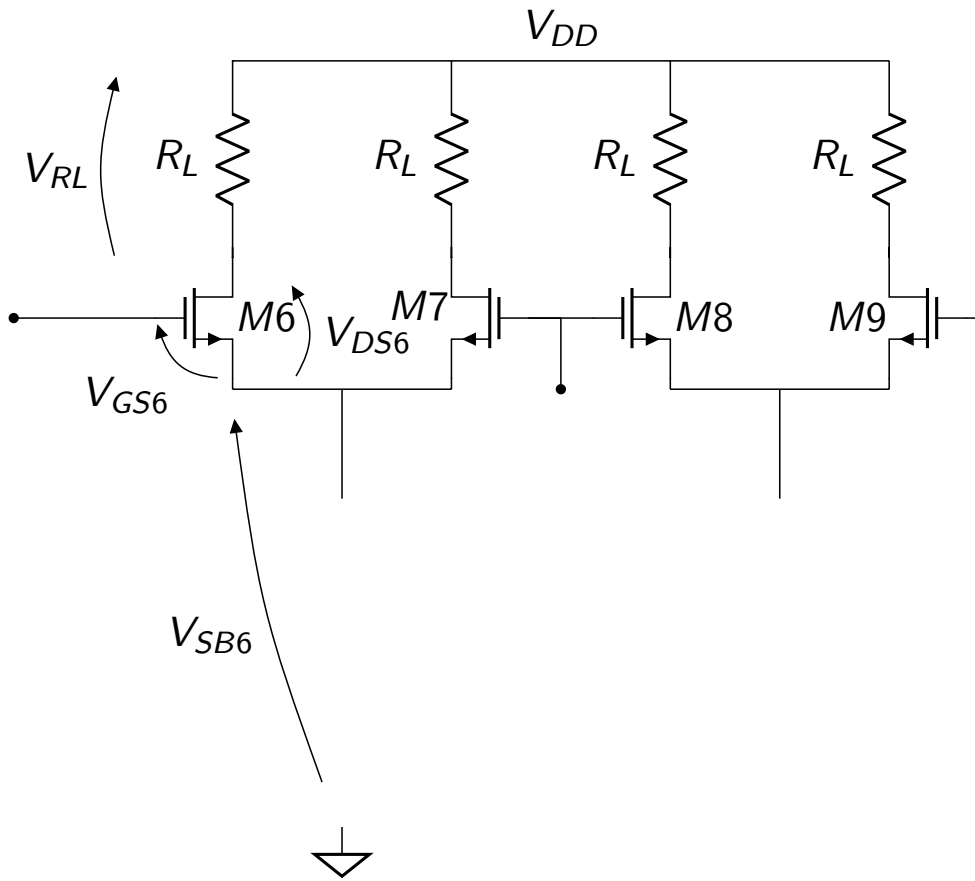


Figure: Load voltage drop

Gain stage design

R_S is chosen in order to increase stage linearity without provoking a too large drop.

$$R_S = 10\Omega$$

$$V_{R_S} = \frac{R_S}{I_0/2} = 25mV$$

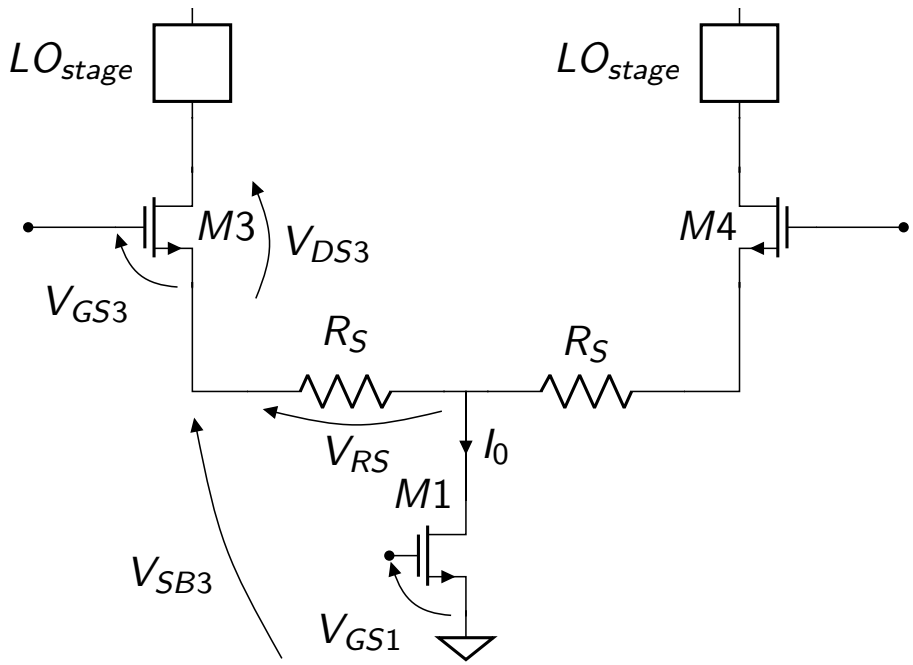


Figure: Gain stage

Gain stage design

Given the previous specification $A_{vC} = 4$ and conversion gain expression

$$A_{vC} = \frac{V_{IF,rms}}{V_{RF,rms}} = \frac{2}{\pi} \frac{R_L}{\frac{1}{g_{m3,4}} + R_S}$$

We can then evaluate transconductance and gate width (provided $L = 3L_{min} = 1.8\mu m$)

$$g_{m3} = \frac{\pi}{2} \frac{1}{\frac{R_L}{A_{vC}} - R_S} = 10mS$$

$$W_3 = g_{m3}^2 \frac{2L_3}{K_n I_0} = 624\mu m$$

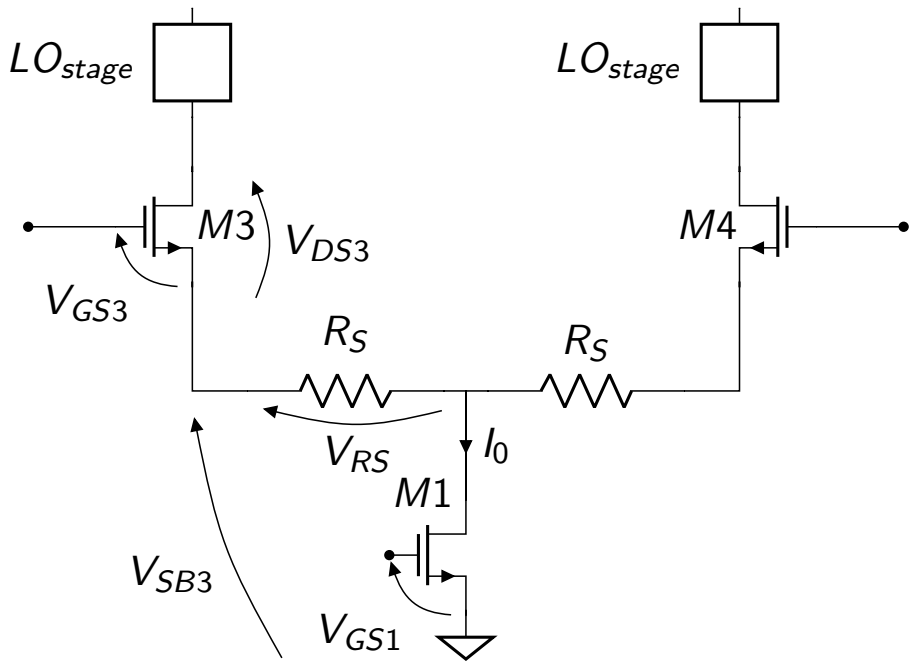


Figure: Gain stage

Gain stage design

M3 is subjected to body effect, thus:

$$V_{SB3} = V_{DS1} + V_{R_S}$$

$$V_{th3} = V_{th0} + \gamma_B\left(\sqrt{2\phi_P + V_{SB3}} - \sqrt{2\phi_P}\right) = 0.957V$$

This leads to an higher gate-source voltage:

$$V_{od3} = \sqrt{\frac{I_0}{K_n W_3/L_3}} = 0.353V$$

$$V_{GS3} = V_{th3} + V_{od3} = 1.31V$$

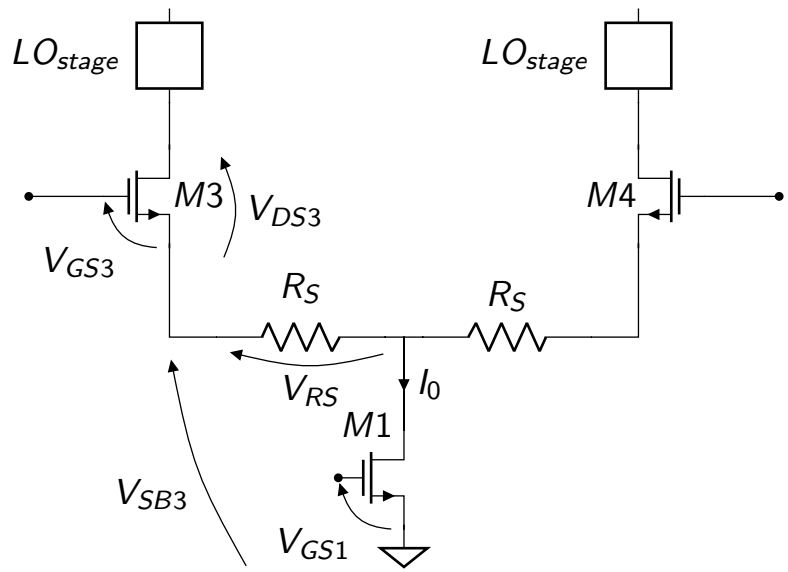


Figure: Gain stage

Gain stage design

We impose to have half the supply voltage to drop on the gain and current mirror stages. From here we can find drain to source voltage of M3:

$$V_{DS3} = \frac{1}{2}V_{DD} - V_{DS1} = 1.4V$$

Since this is higher than overdrive, M3 saturation is guaranteed if on. Based on this we evaluate the gate bias voltage that keeps underneath stages saturated:

$$V_{G3} = V_{GS3} + V_{R_S} + V_{DS1} = 2.425V$$

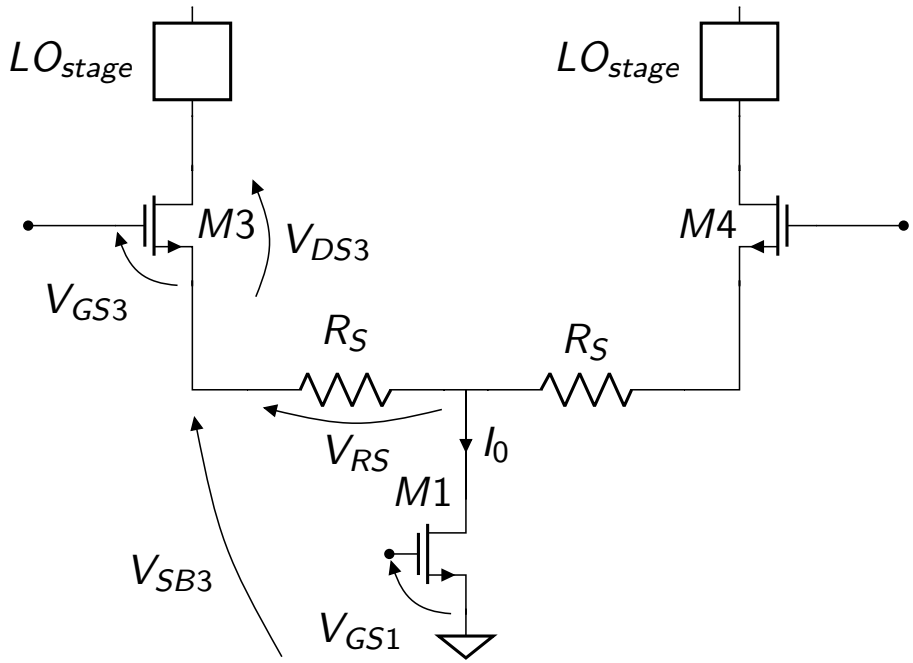


Figure: Gain stage

Mixing stage design

A very small overdrive is needed to foster fast transitions on LO stage.

$$V_{od6} = 150mV$$

But small overdrives produce large gate width. To limit this, the minimum gate length was chosen for LO stage. Then we can derive gate width:

$$L_6 = L_{min}$$

$$W_6 = \frac{I_0 L_6}{K_n V_{od6}^2} = 1.1mm$$

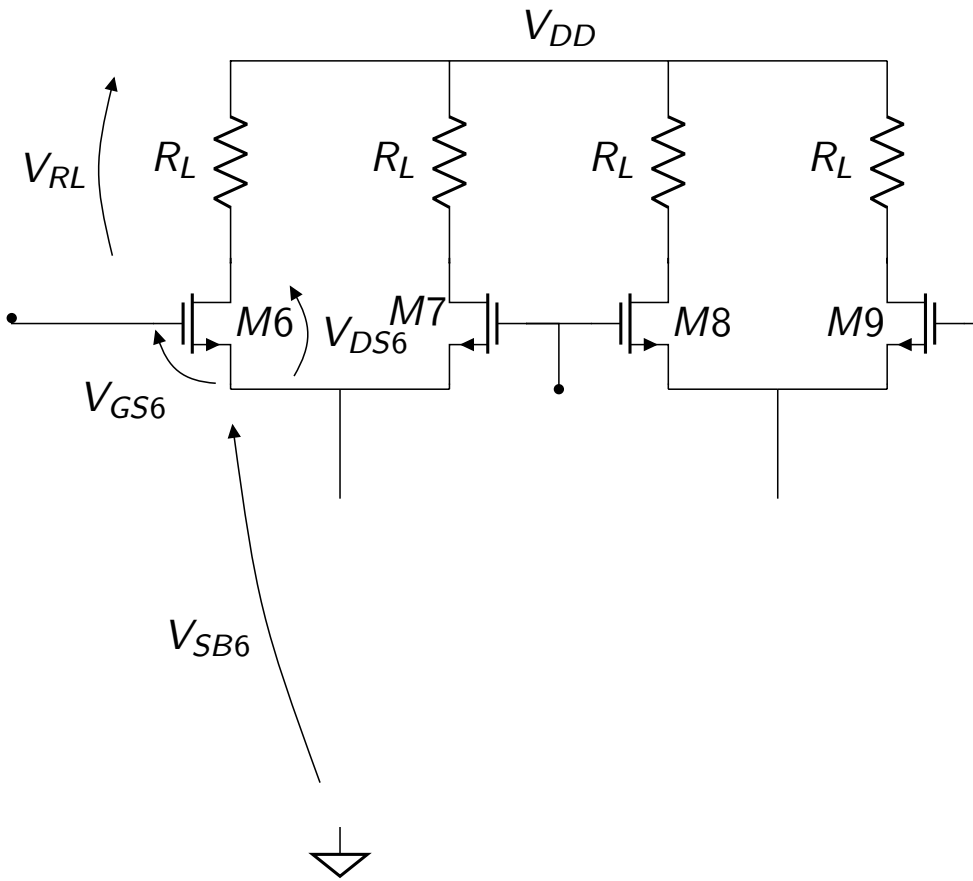


Figure: Gain stage

Mixing stage design

We can take into account body effect to evaluate the threshold voltage and so the gate bias for LO stage.

$$V_{SB6} = V_{DS1} + V_{R_S} + V_{DS3} = 2.525V$$
$$V_{th6} = 1.18V$$
$$V_{GS6} = 1.326V$$
$$V_{G6} = V_{GS6} + V_{DS1} + V_{R_S} + V_{DS3} = 3.855V \quad (1)$$

All short-channel effect that produce a more complex threshold voltage dependence are not taken into account here.

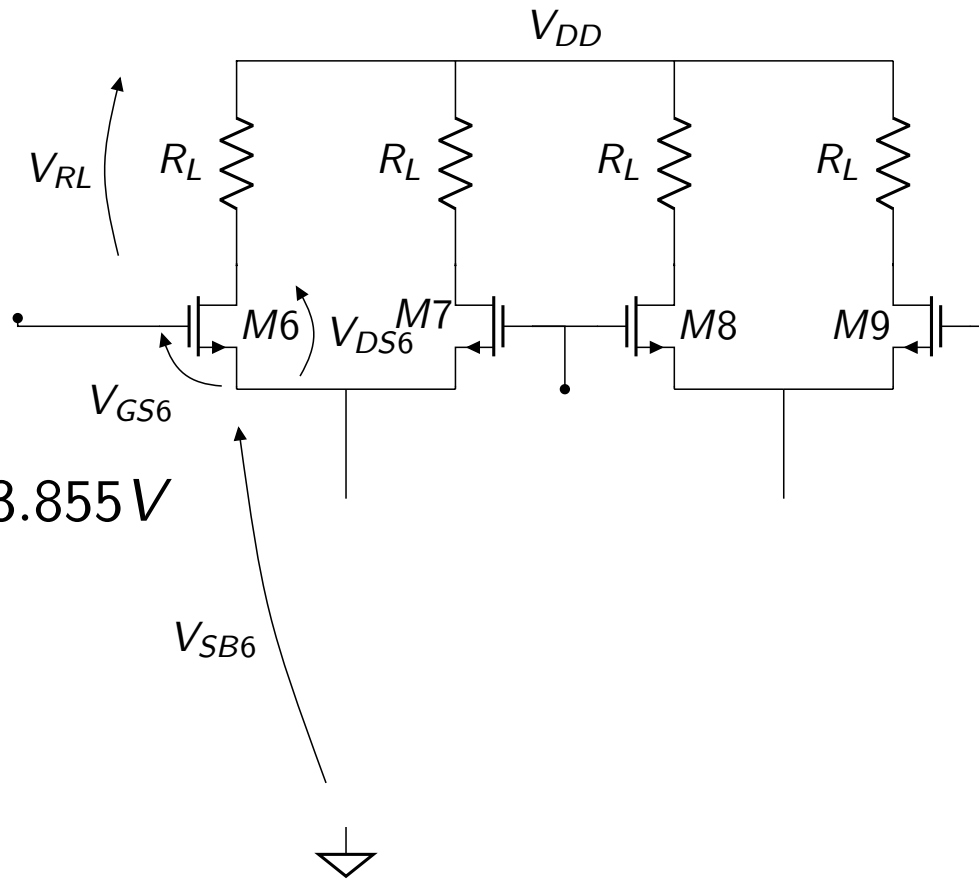


Figure: Gain stage

Gilbert cell CAD design - Introduction

A new design approach, based on **simulation and characterization of each device** is required, since:

- Level 1 model simulation result proven to be not enough accurate to correctly describe the behaviour of the circuit (no correspondence between calculation and simulation);
- Gate width suggested in literature by:

$$W_{opt} = \frac{1}{3\omega L C_{ox} R_g}$$

yield too large devices (W$\geq$1mm).

Gilbert cell CAD design - Step 1

Step 1 : **maximize** g_{m3}.

To do that we **impose**:

- $M_{3,4}$ dimensions:

$$L_3 = 3L_{min} = 1.8\mu m$$
$$50\mu m \leq W_3 \leq 500\mu m$$

- Circuit consumption: $I_0 \approx 5mA$;
- Voltage drops on $M_{3,4}$ nodes:

$$V_{SB3} = V_{DS1} = V_{DS3} = 1.5V$$

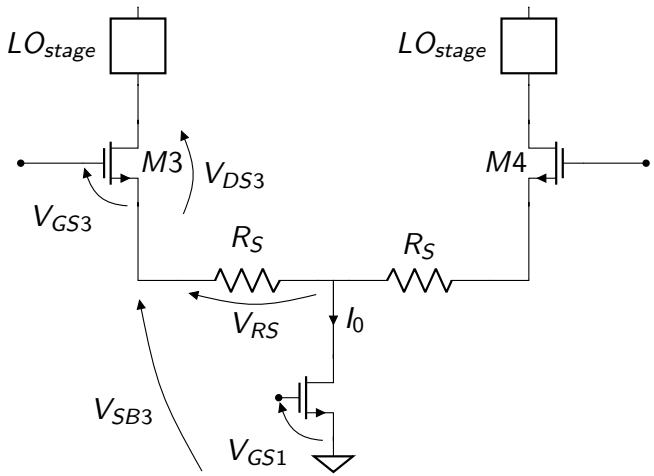


Figure: Gain stage.

Gilbert cell CAD design - Step 1

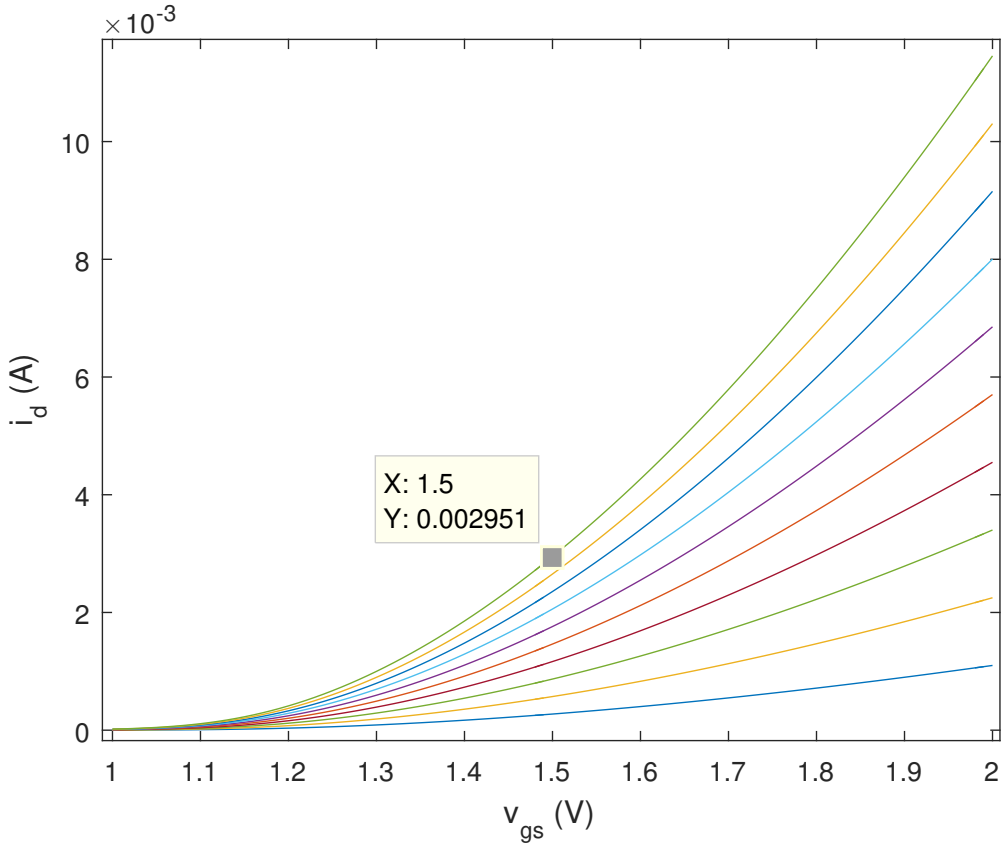


Figure: Drain current versus gate-source voltage of the RF stage, with W_3 varying from 50μm to 500μm, $V_{DS3} = 1.5V$.

Gilbert cell CAD design - Step 1

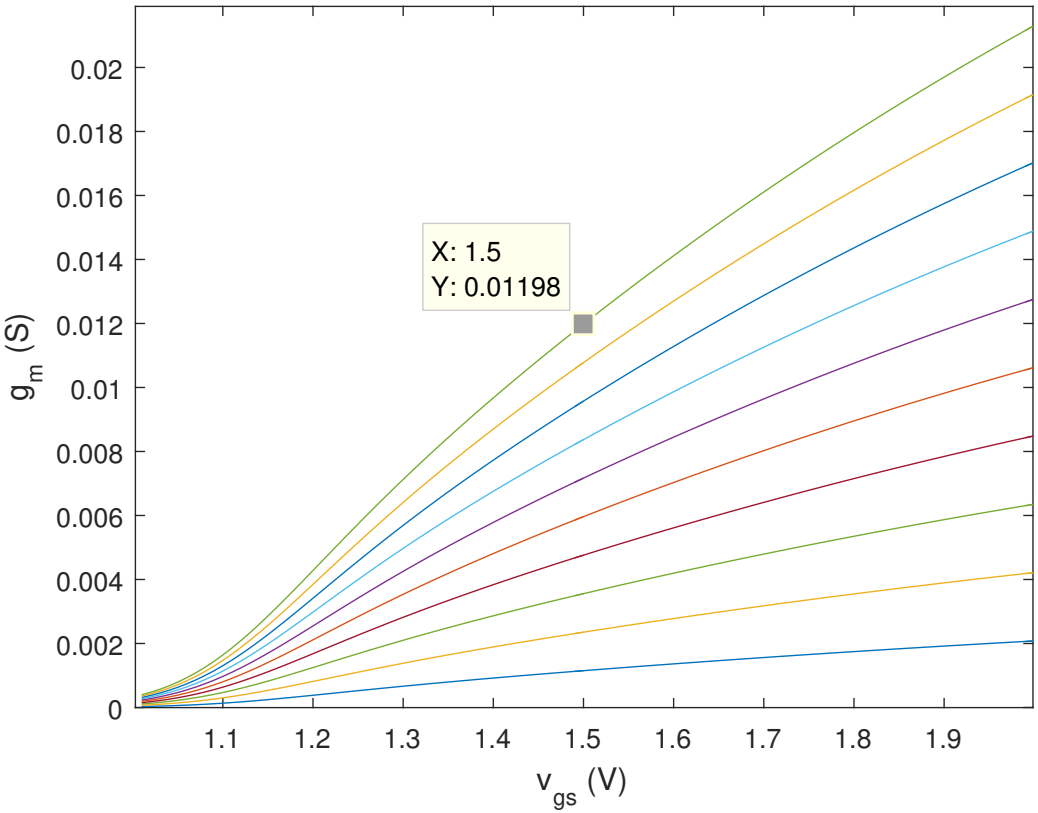


Figure: Transconductance versus gate-source voltage of the RF stage, with W_3 varying from 50μm to 500μm, $V_{DS3} = 1.5V$.

Gilbert cell CAD design - Step 1

We chose:

- $W_3 = 500\mu m$m
- $V_{GS3} = 1.5$V
- $g_{m3} = 11.9$mS
- $I_0/2 = 2.9$mA

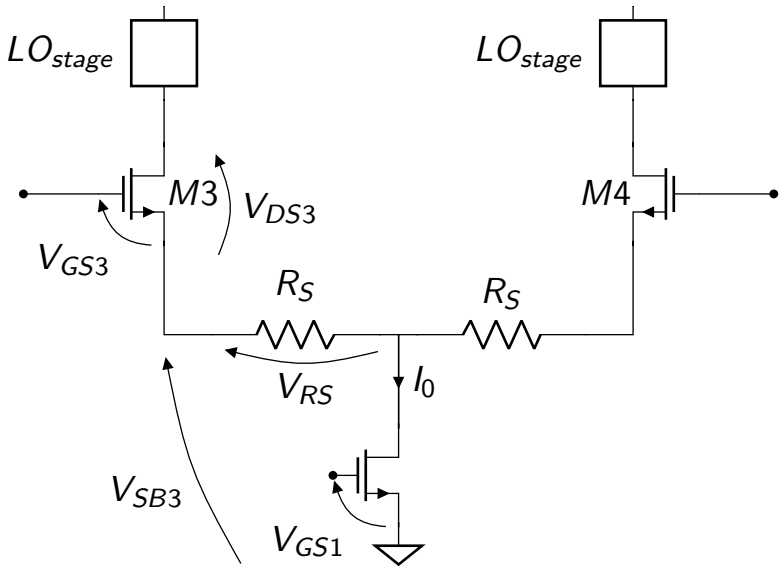


Figure: Gain stage.

Gilbert cell CAD design - Step 2

Step 2 : **design the current sink**.

we **have**:

- voltage on R_S:

$$V_{R_S} = 2.9mA \cdot 10\Omega = 29mV$$

- Voltages on M_1

$$V_{DS1} = 1.5V - V_{R_S} = 1.471V$$
$$V_{GS1} = 1.471V$$

From simulation we get W_3=373μm to have I_0=5.8mA.

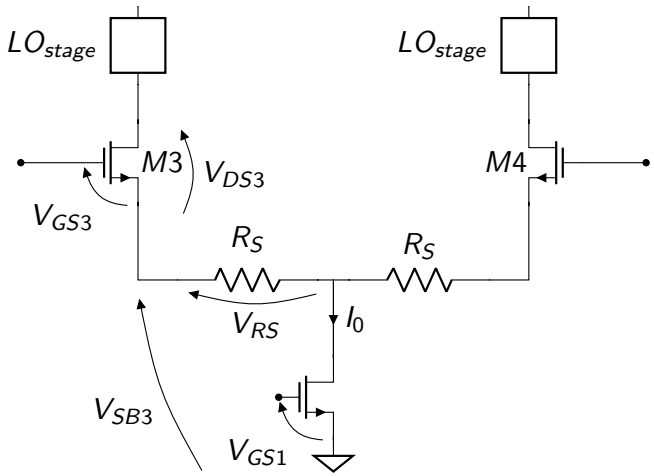


Figure: Gain stage.

Gilbert cell CAD design - Step 2

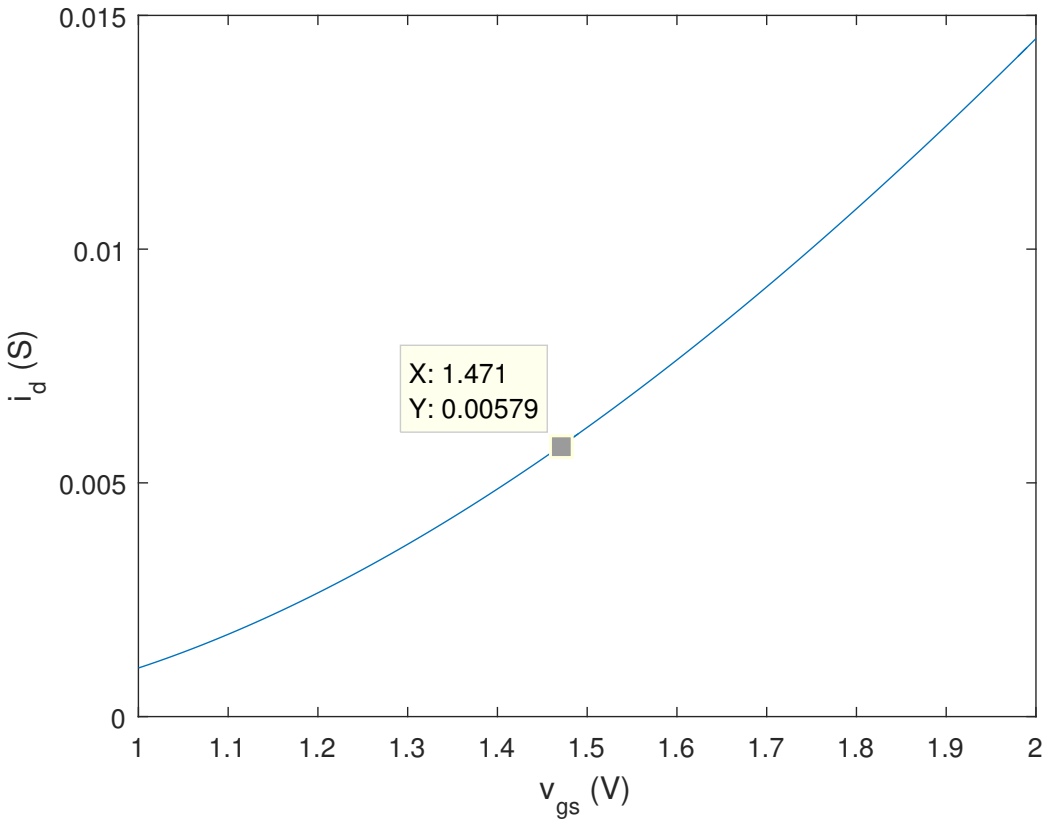


Figure: Drain current versus gate-source voltage of the bias transistor M1, with W=373μm

Gilbert cell CAD design - Step 3

Step 3 : **design the mixing stage**.

From **design spec** we have:

$$A_v \approx \frac{2}{\pi}\left(\frac{R_L}{R_S + \frac{1}{g_{m3}}}\right) = 4$$

therefore

$$R_L = A_v \cdot \left(\frac{\pi}{2} \cdot \frac{1}{g_{m3}} + R_S\right)$$
$$= 4 \cdot \left(\frac{\pi}{2} \cdot \frac{1}{11.9mS} + 10\Omega\right) = 577\Omega$$

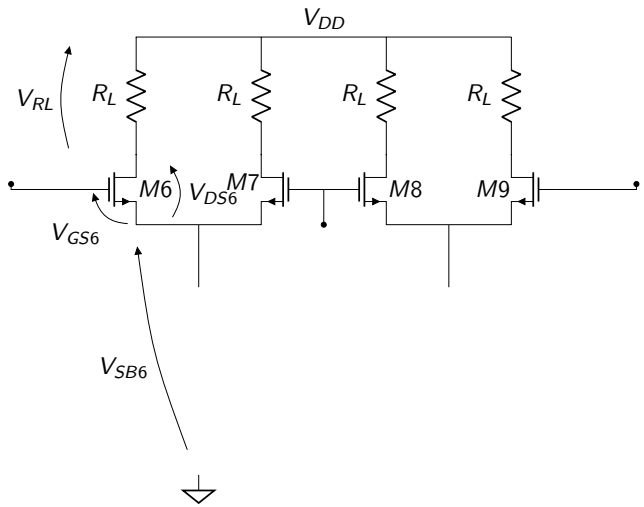


Figure: Gain stage.

Gilbert cell CAD design - Step 3

One has:

$$V_{SB6} = V_{DS1} + V_{R_S} + V_{DS3}$$
$$= 1.47V + 0.029V + 1.5V = 3V$$

hence:

$$V_{R_L} = 2.9mA \cdot 577\Omega = 1.673V$$
$$V_{DS6} = V_{dd} - V_{R_L} - V_{SB6} = 327mV$$

We need *switches* slightly above threshold.

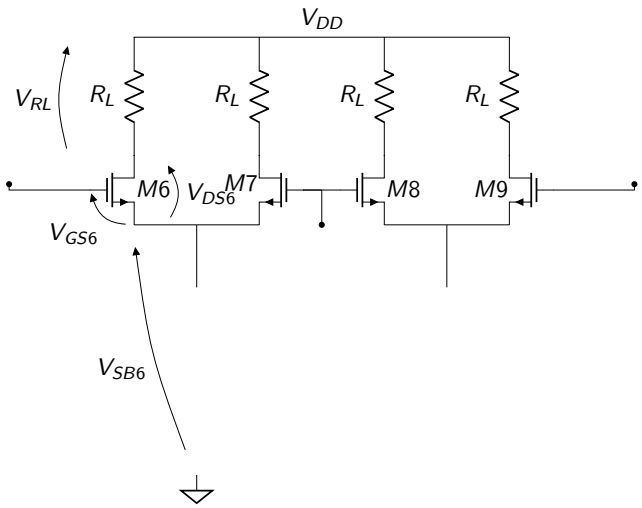


Figure: Gain stage.

Gilbert cell CAD design - Step 3

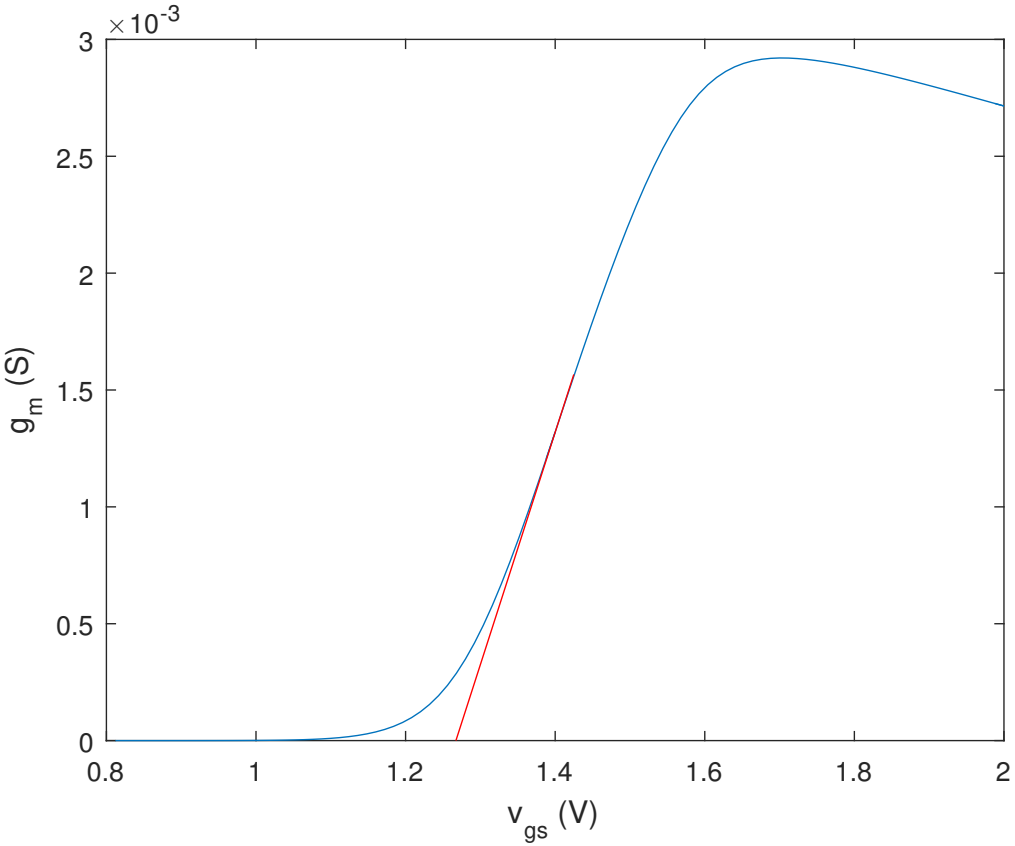


Figure: Extrapolation of M6 threshold voltage from transconductance versus the V_{GS} curve. The threshold is located at $1.27V$.

Gilbert cell CAD design - Step 3

From simulation we chose V_{od6}=60mV. Then:

$$V_{GS6} = V_{th6} + \Delta V_6 = 1.33V$$

By characterizing the device:

$$W_6 = 170.3\mu m$$
$$L = L_{min} = 0.6\mu m$$

Minimum gate length: fast but noisy.

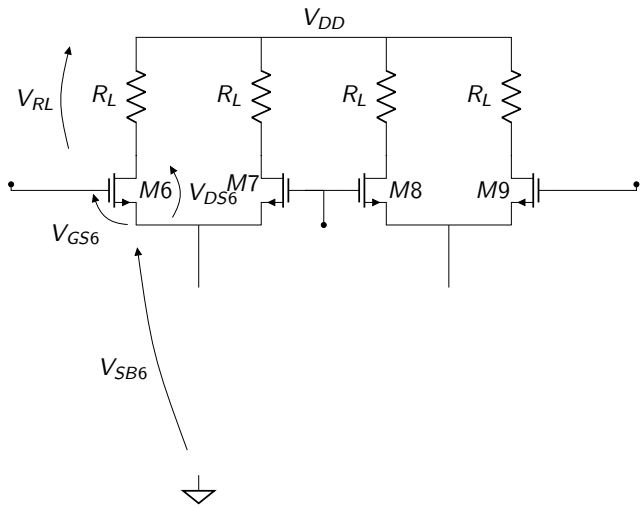


Figure: Gain stage.

Bias net design - M_5

Now the bias net is designed. From **spec**:

$$V_{G1} = 1.471V$$
$$V_{G3} = 3V$$
$$V_{G6} = 4.33V$$

We chose mirroring ratio 1:1, $L_2 = 1.8\mu m$ (same length of M_1) and $V_{GS2} = V_{DS2} = 1.471V$. To have I_0=5.8mA from **simulation**:

$$W_2 = 373\mu m$$

Since $V_{G5} = 3V$, from **simulation**:

$$W_5 = 130.45\mu m$$
$$L_5 = 0.6\mu m$$

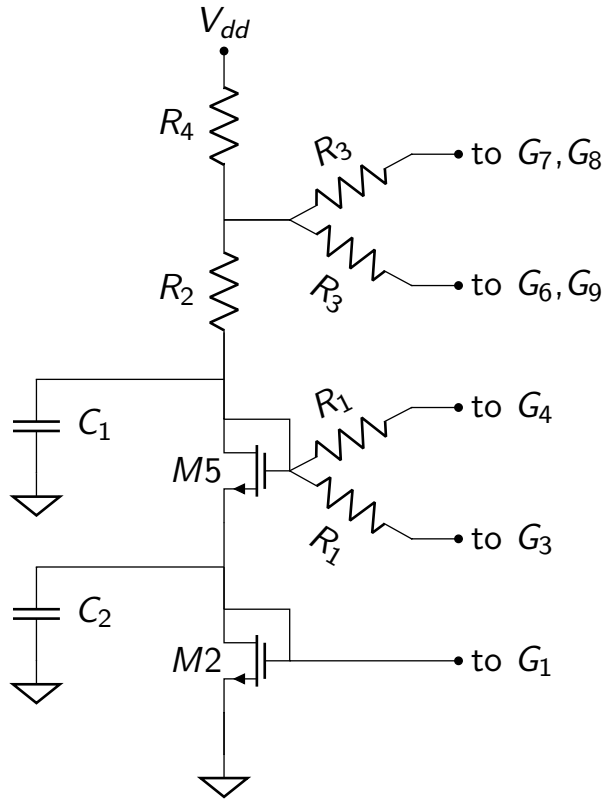


Figure: Reference biasing network schematic

Bias net design - R_2,R_4

Voltage drop on R_2 and R_4:

$$R_2 + R_4 = \frac{V_{dd} - V_{G5}}{I_0} = 344\Omega$$

Since $V_{G6} = 4.33V$:

$$R_2 = 229\Omega$$
$$R_4 = 115\Omega$$

The static power consumption is
$P = 5.8mA \cdot 5V = 29mW$

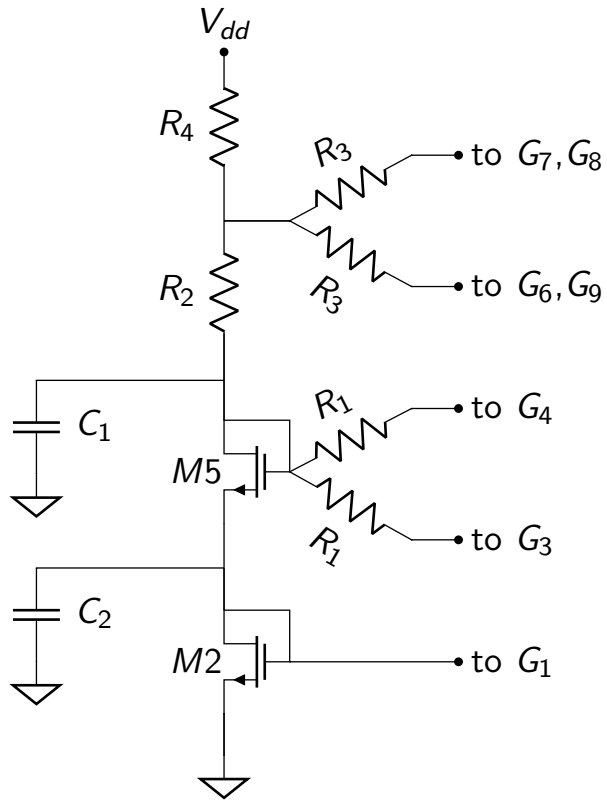


Figure: Reference biasing network schematic

Bias net design - $R_{1,3}$ and $C_{1,2}$

Resistors R_1 and R_3 act as AC block:

$$R_1 = R_3 = 30k\Omega$$

Equivalent resistance seen from C_1:

$$R_{eq} \simeq R_1//R_3//R_2//R4 = 76.4\Omega$$

Pole frequency un decade before f_{LO}:

$$C_1 \geq 10 \cdot \frac{1}{2\pi \cdot R_{eq} \cdot \frac{f_{lo}}{10}} = 20.8pF$$

From **optimization**: $C_1 = C_2 = 25pF$.

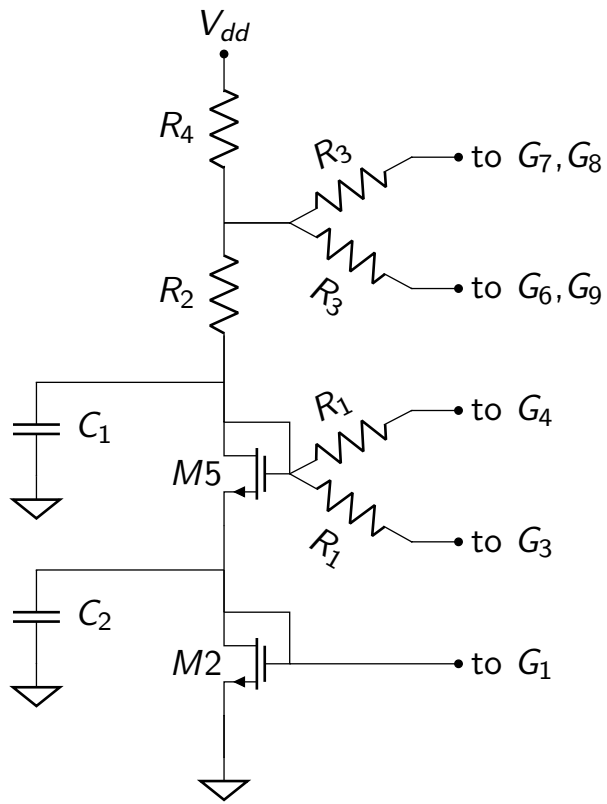


Figure: Reference biasing network schematic

Design CAD validation - Full circuit

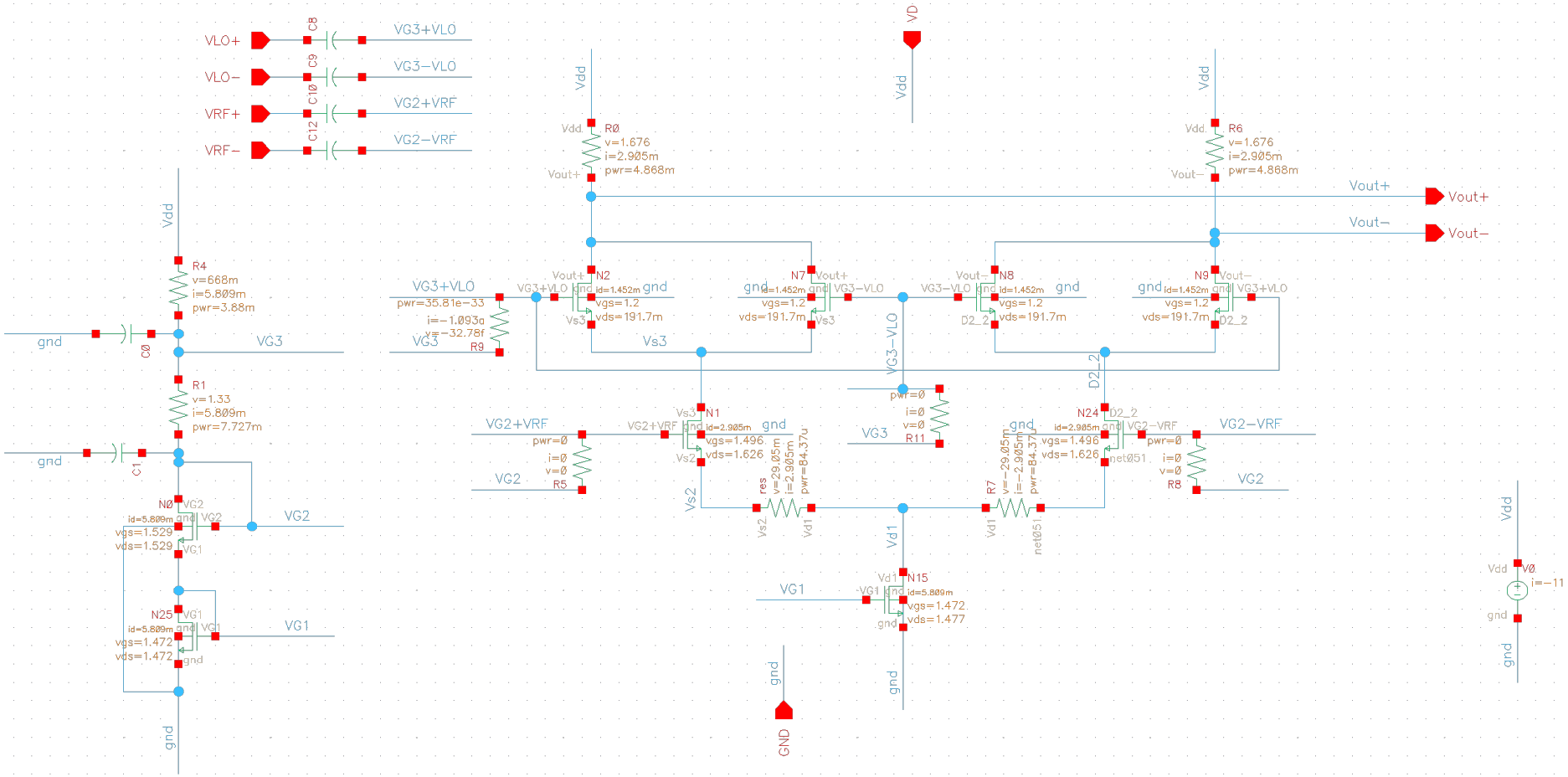


Figure: Gilbert cell and bias network schematic

Design CAD validation - Gain stage

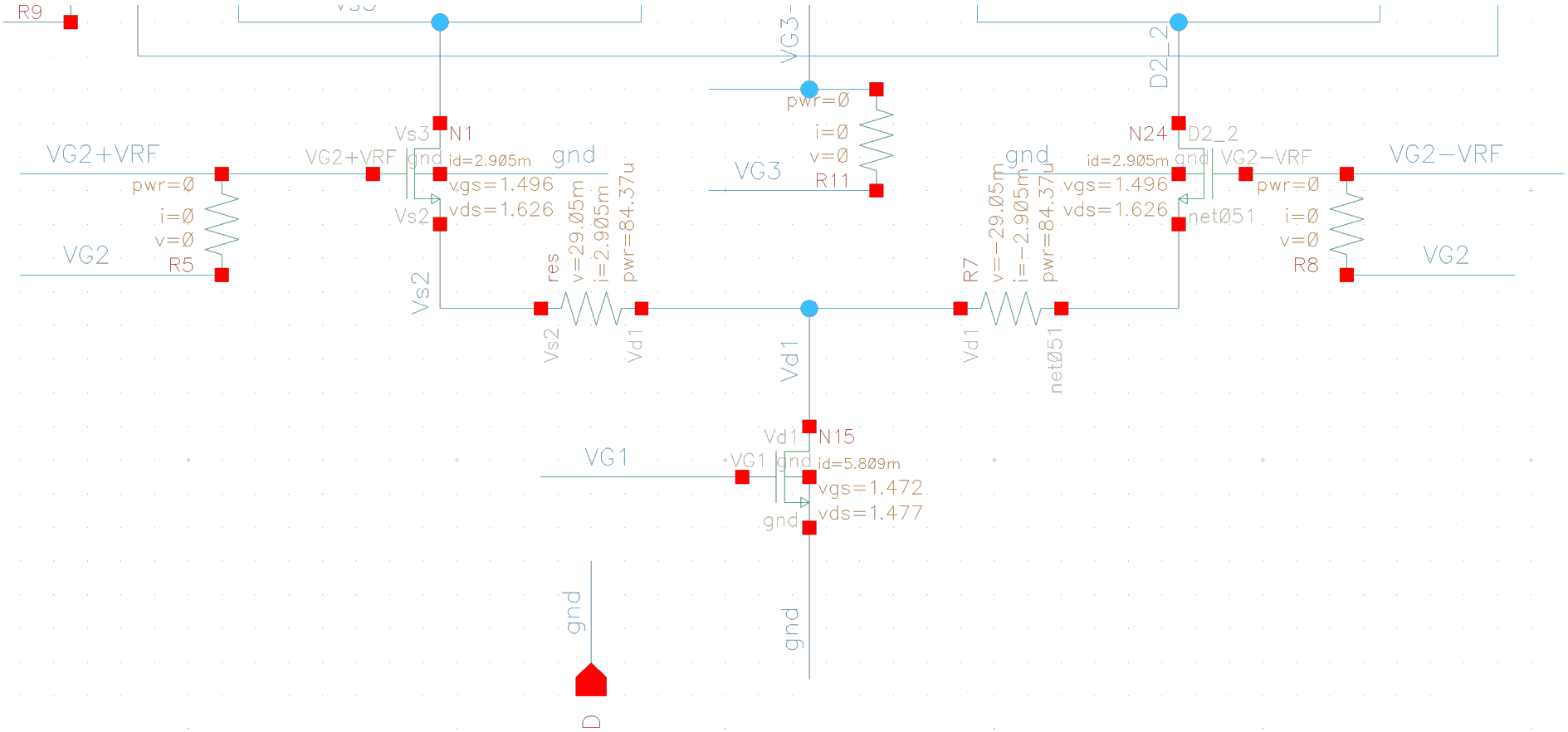


Figure: Close up view on current sink and RF stage

Design CAD validation - Mixing stage

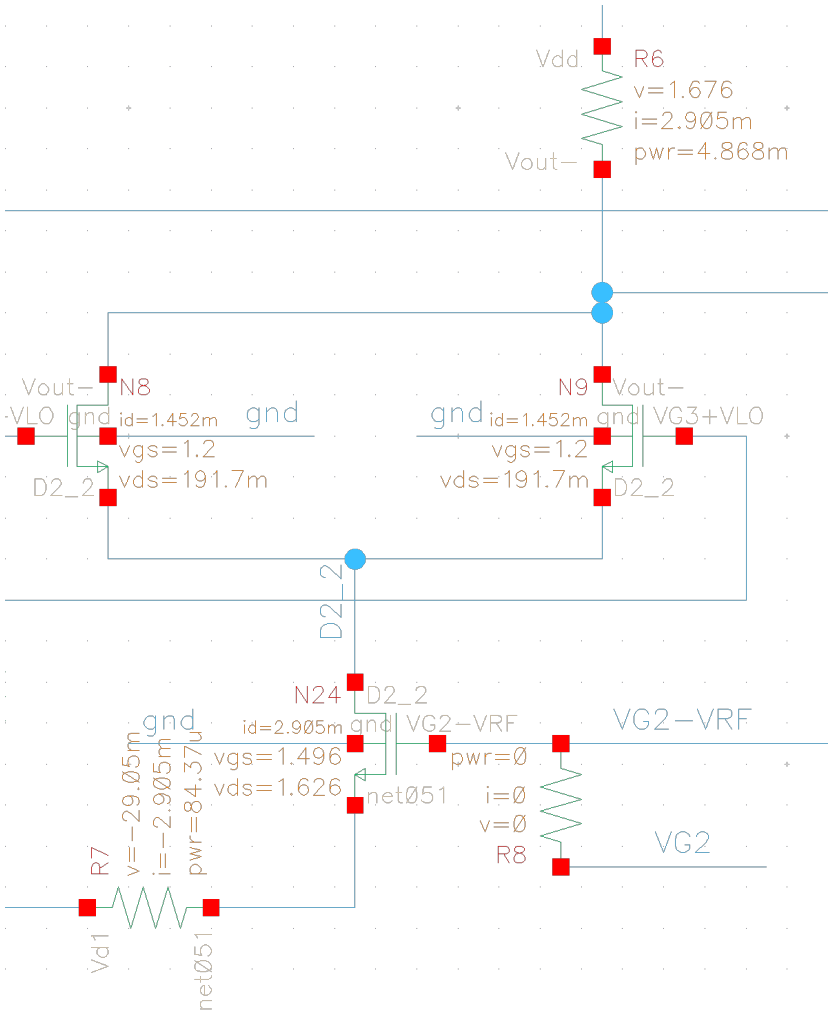


Figure: Close up view of LO stage

Design CAD validation - Bias net

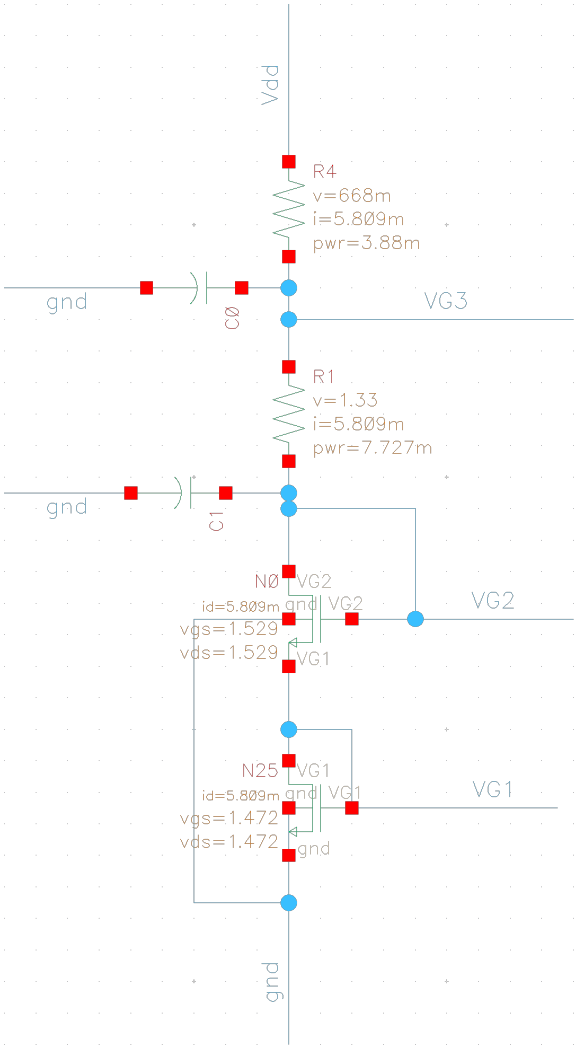


Figure: Close up view of LO stage

Layout strategy

- Common centroid, interdigitated structures: less gradients;
- Multi-finger structure with same-length for transistors fingers: minimize encroachment;
- Components with same alignment: uniform error distribution;
- Dummy elements: less border effects;
- Limited substrate noise with guard rings;
- Minimum number of crossed connections and metal changes in the routing process;
- Compact and symmetric structure;
- Guard rings used because of circuit width and shared body contact for each MOSFET.
- **Every device has been optimized** to have correspondence between circuit and layout.

Layout - Gain and Mixing stage

A **symmetric** input low noise differential stage is desired. A common centroid structure is employed along with dummy elements (shorted drain and source).
Same approach with mixing stage. Designed to be easily stacked above RF stage, with the two witching stages kept close to each other.

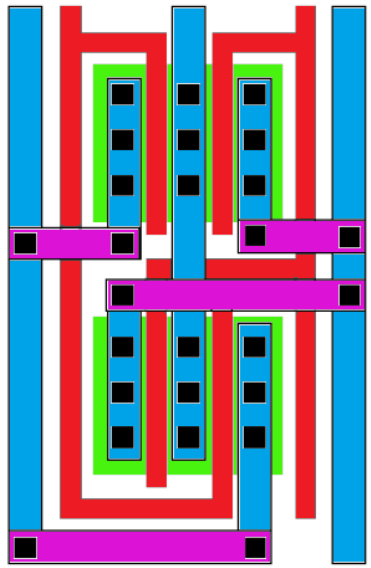
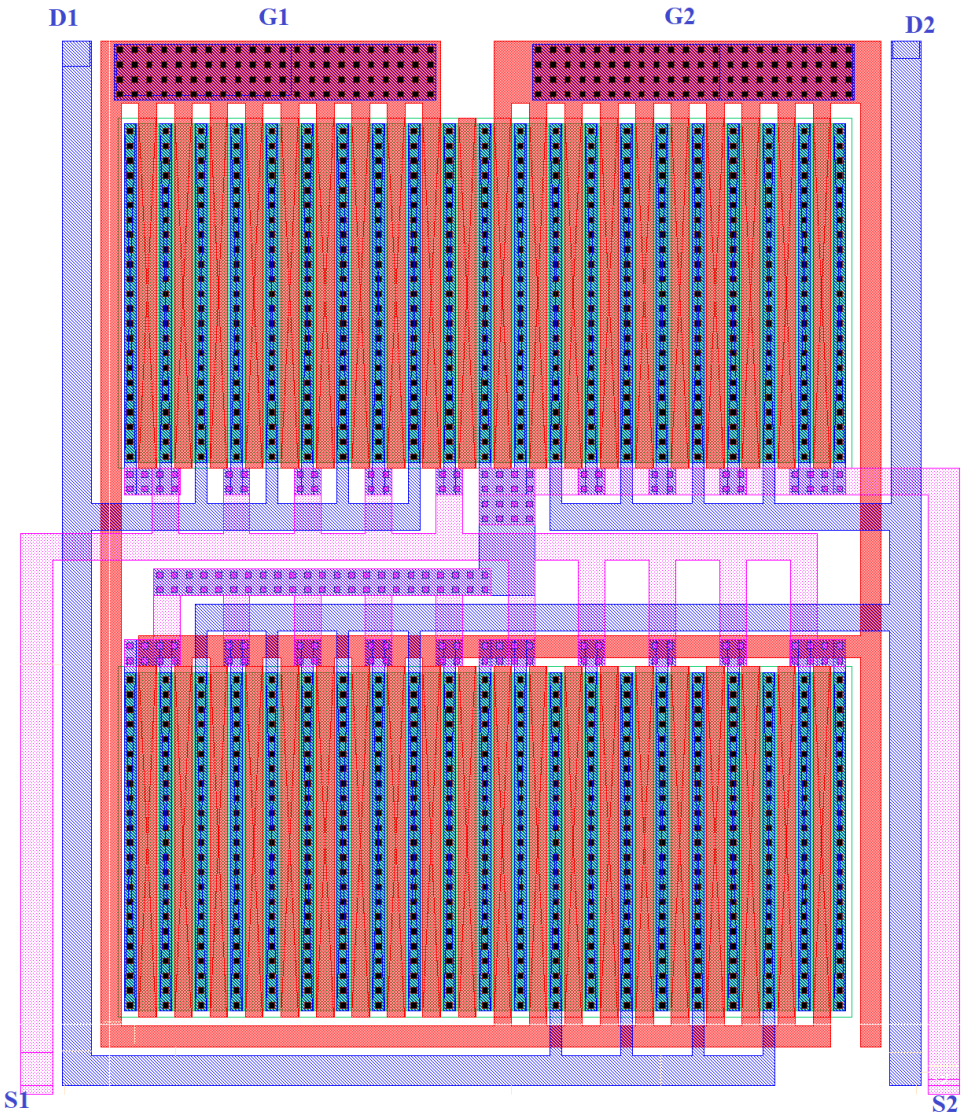


Figure: Common centroid structure used for differential RF stage

Layout - Gain stage

$M_{3,4}$ parameters:

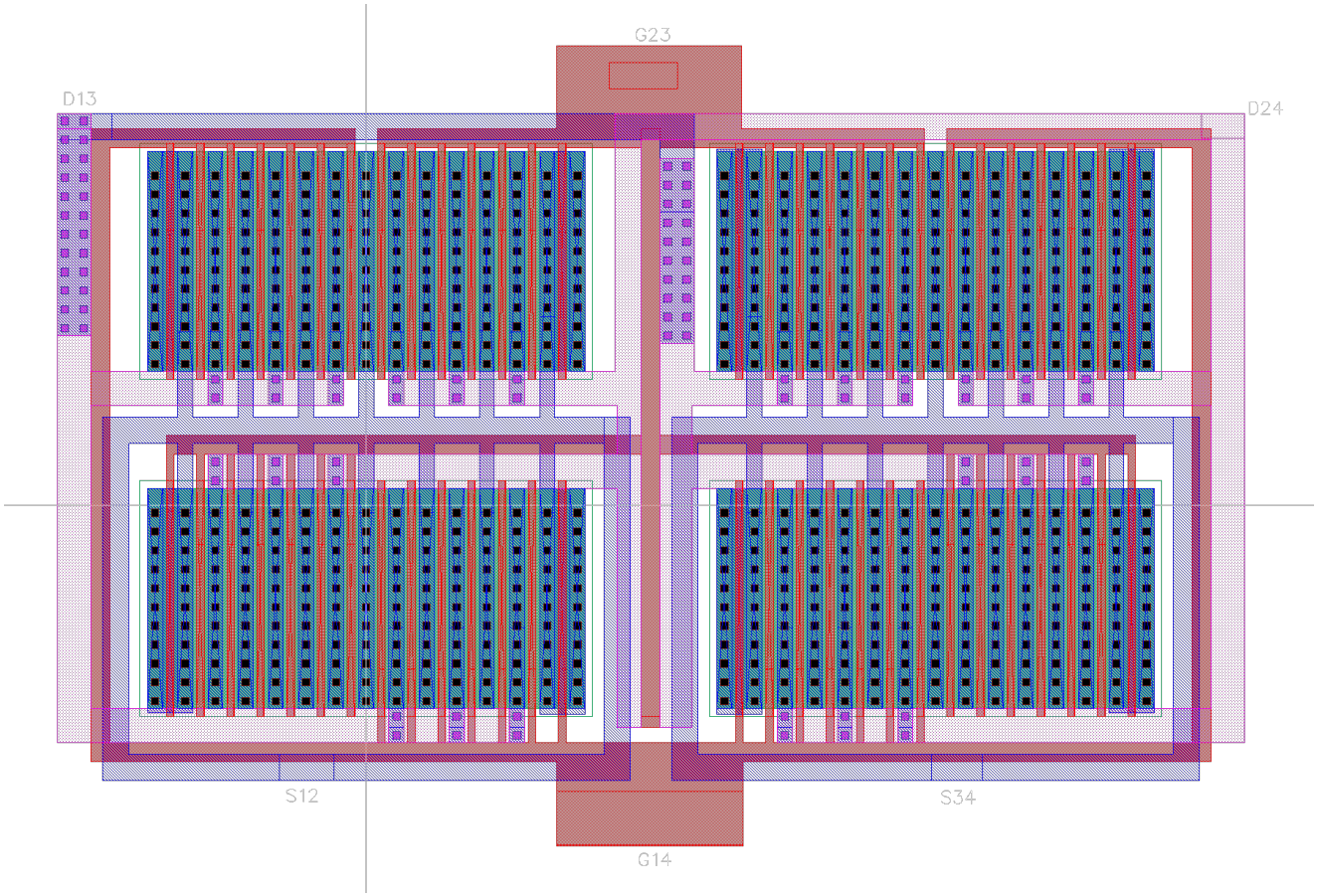
- m $= 18(+2)$
- w*=34.35μm
- W $= 618.3\mu$m (vs 500μm)
- L $= 1.8\mu$m
- y $= 126\mu$m
- x $= 99.45\mu$m



Layout - Mixing stage

$M_{6,7,8,9}$ parameters:

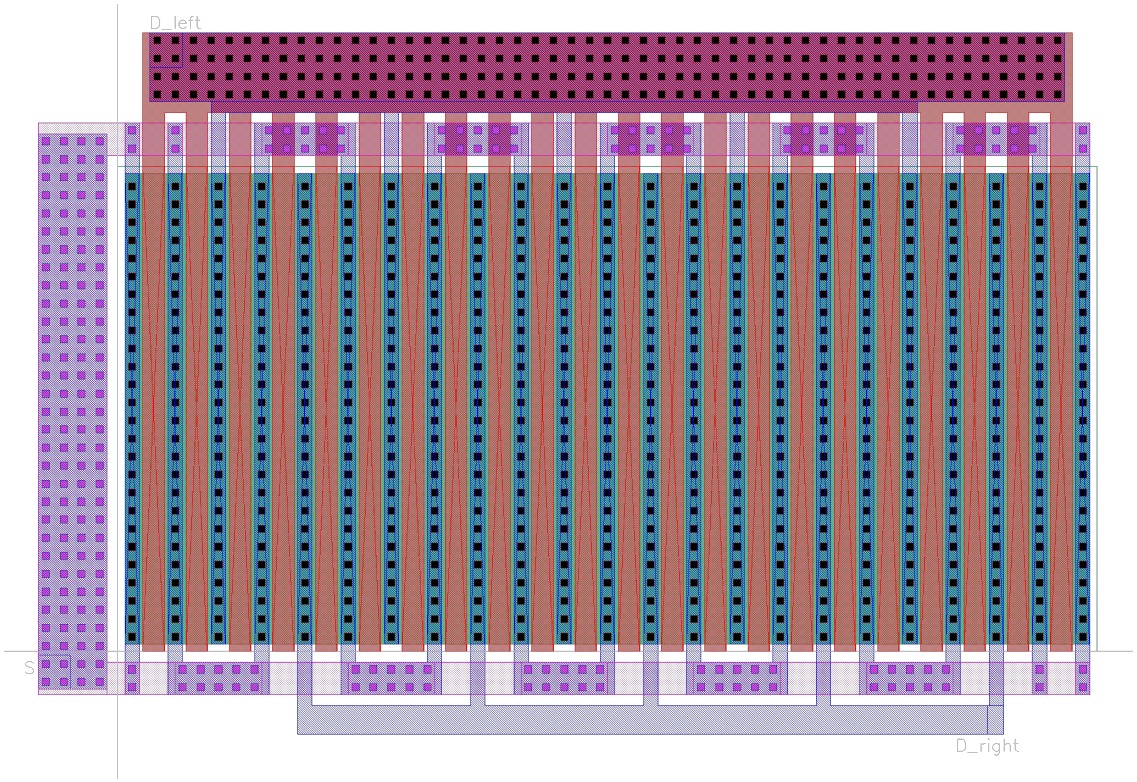
- m $= 12(+2)$
- w*=17.55μm
- W $= 210.6\mu$m (vs 170.3μm)
- L $= 0.6\mu$m
- y $= 56.85\mu$m
- x $= 87.6\mu$m



Layout - Current mirror

Current mirror shows multifinger interdigitated structure with dummy elements. $M_{1,2}$ parameters:

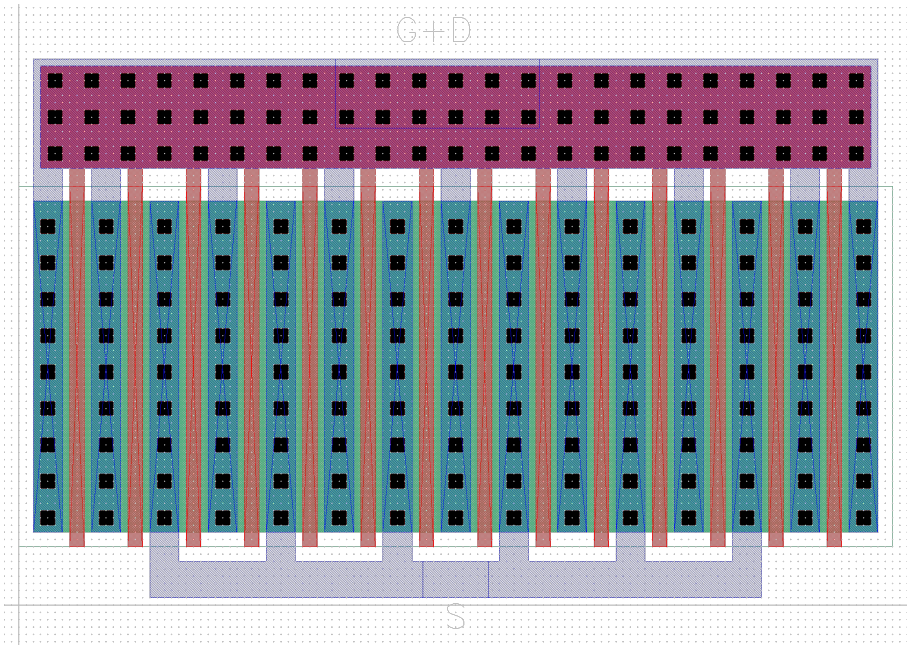
- m = 10(+1)
- w*=39.15μm
- W = 391.15μm (vs 373μm)
- L = 1.8μm
- y = 61.5μm
- x = 87.75μm



Layout - M_5

M_5 shows multifinger interdigitated structure with dummy elements. M_5 parameters:

- m $= 12(+2)$
- w*=13.65μm
- W $= 163.8\mu$m (vs 130.45μm)
- L $= 1.8\mu$m
- y $= 25.2\mu$m
- x $= 35.55\mu$m



Layout - C_{bias}

$C_{1,2}$ are poly capacitors (poly1 + elec) in order to reduce dimensions and improve tolerances. Common centroid layout with n-well ring (connected to V_{DD}) to reduce fringing field leaks along with dummy elements.

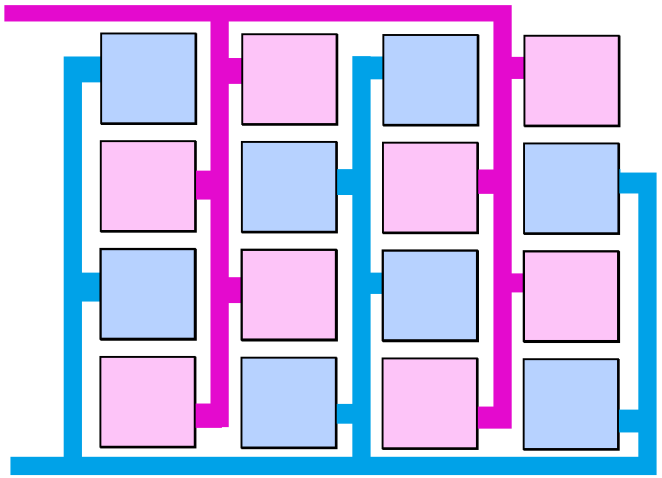
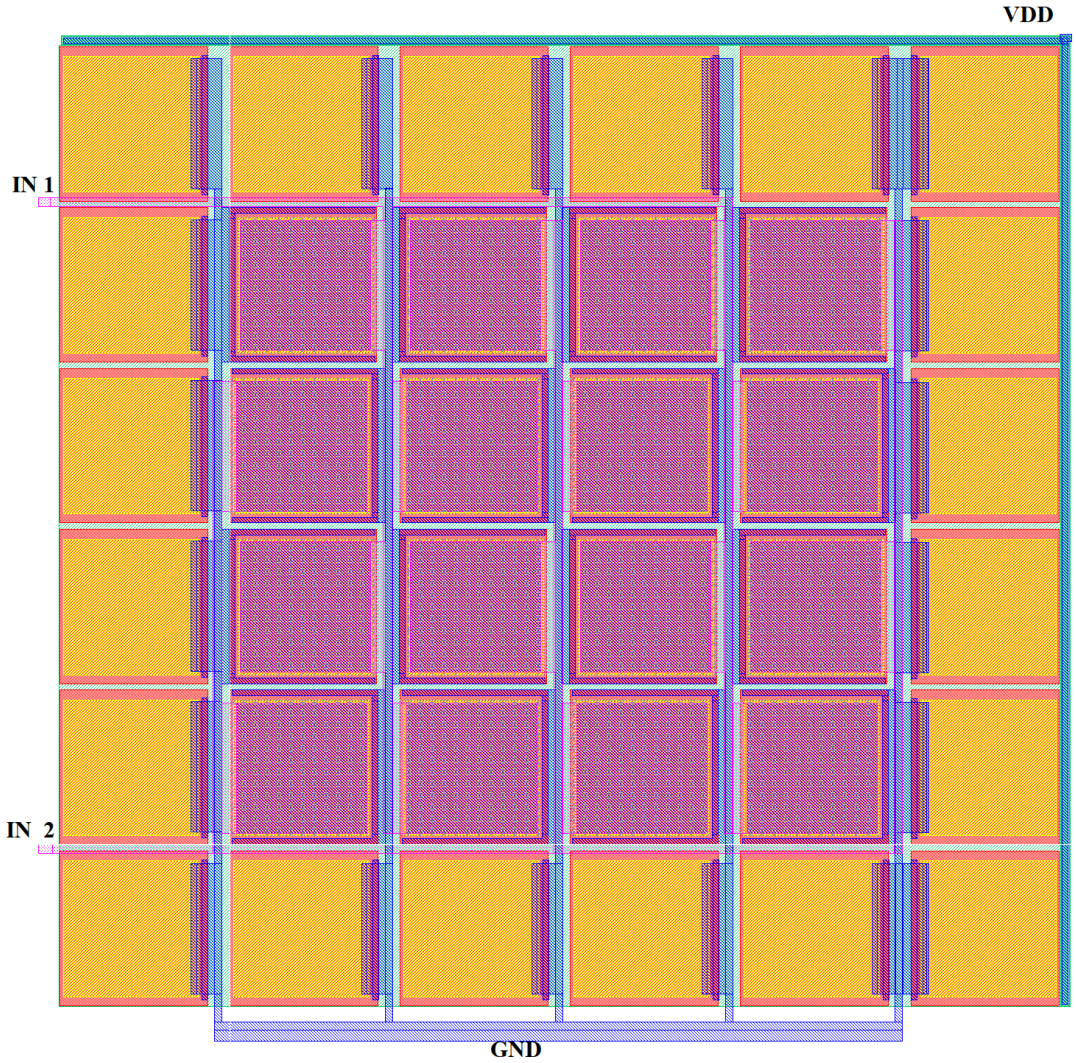


Figure: Bias capacitors layout structure

Layout - C_{bias}

- y = 448.65μm
- x = 472.5μm
- C_{bias}=25.9pF



Layout - C_{signal}

C_{signal} are large capacitance ($\simeq$nF). Multilayer structure impossible because of *CMOS design rule 11.6*. Good matching required then common centroid structure is used. Series resistance reduced by surrounding metal plates. n-well ring connected to V_{DD} to reduce fringing field.

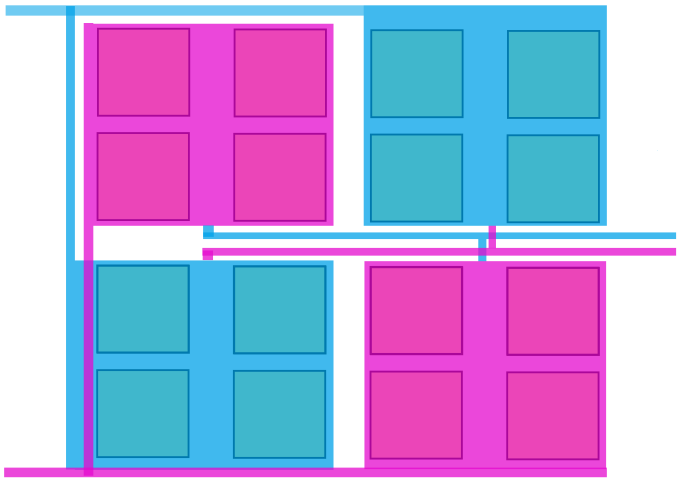
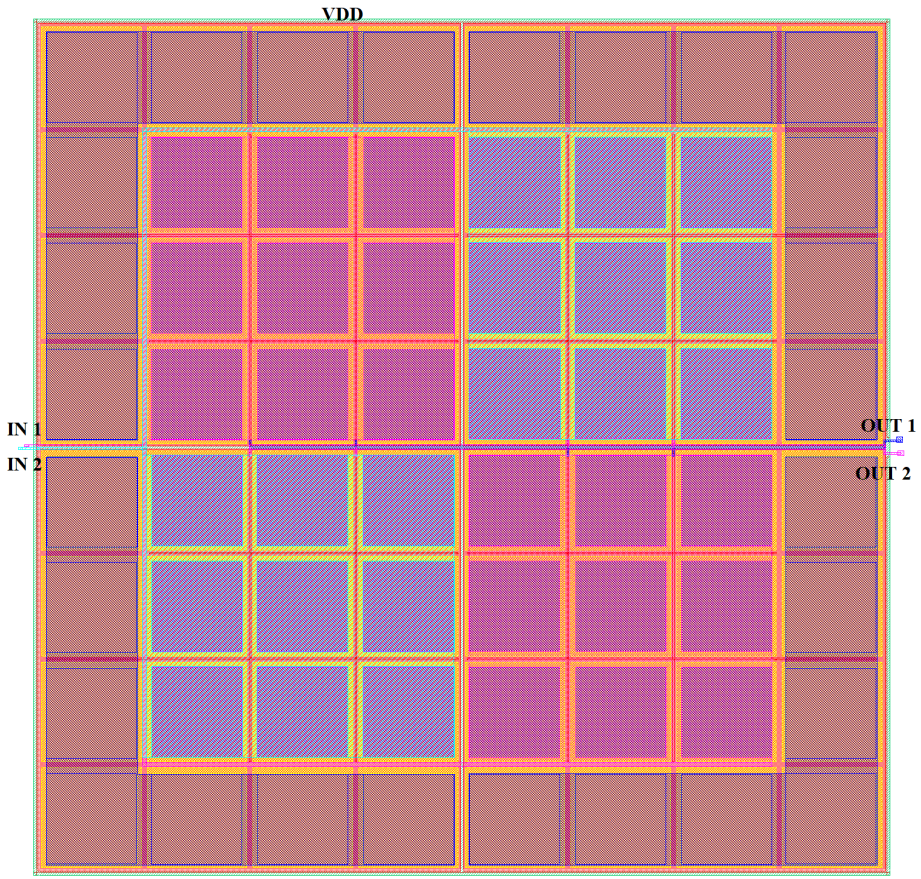


Figure: Common centroid structure of the signal capacitors

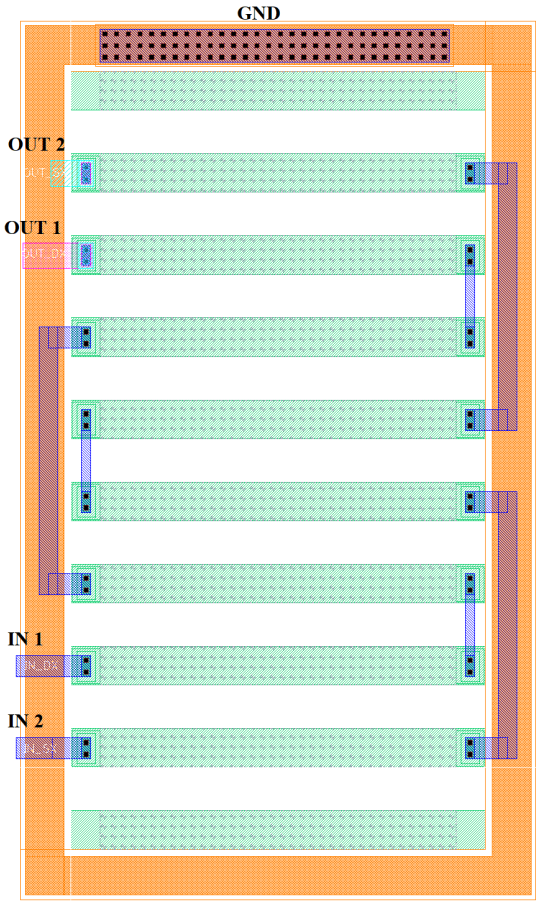
Layout - C_{signal}

- y = 678.45μm
- x = 480.25μm
- C_{bias}=90.1pF



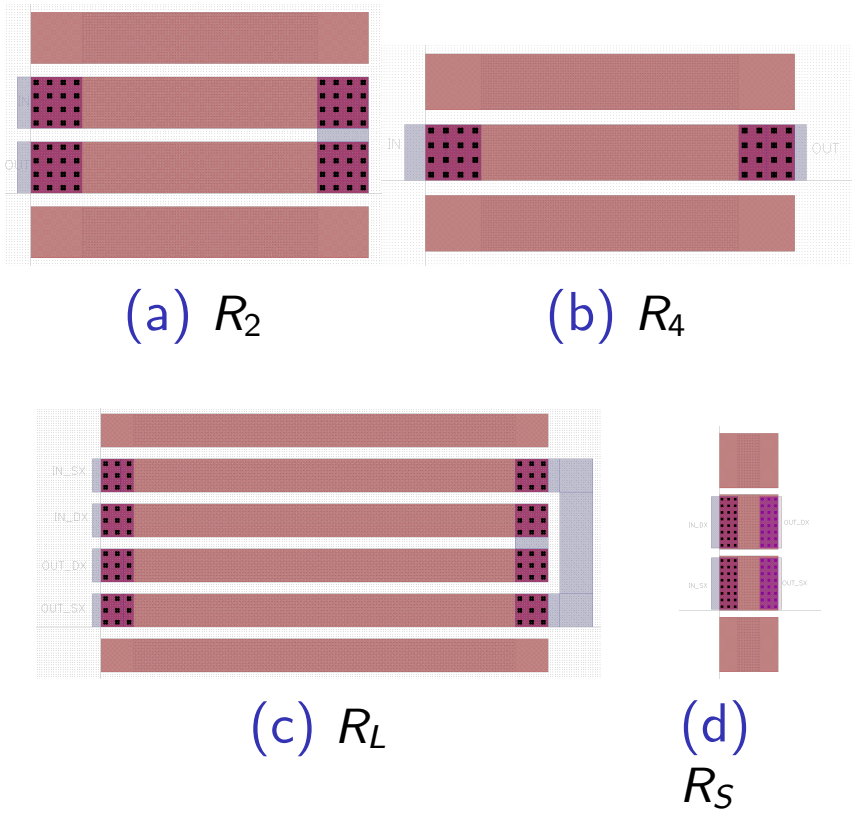
Layout - $R_{1,3}$

$R_{1,3}$ are large then n-well technology necessary with common centroid structure to improve gradients (precision not necessary though). Nearby mixing stage, then guard ring needed to avoid substrate currents.



Layout - R_2,R_4,R_L,R_S

R_2,R_4,R_L and R_S are smaller than $R_{1,3}$ therefore poly1 resistors can be used, improving also precision.
Common centroid structure with dummy elements.



(a) R_2 (b) R_4 (c) R_L (d) R_S

Figure: Poly resistors layout

Layout - Resistors parameters

Table: Resistors parameters

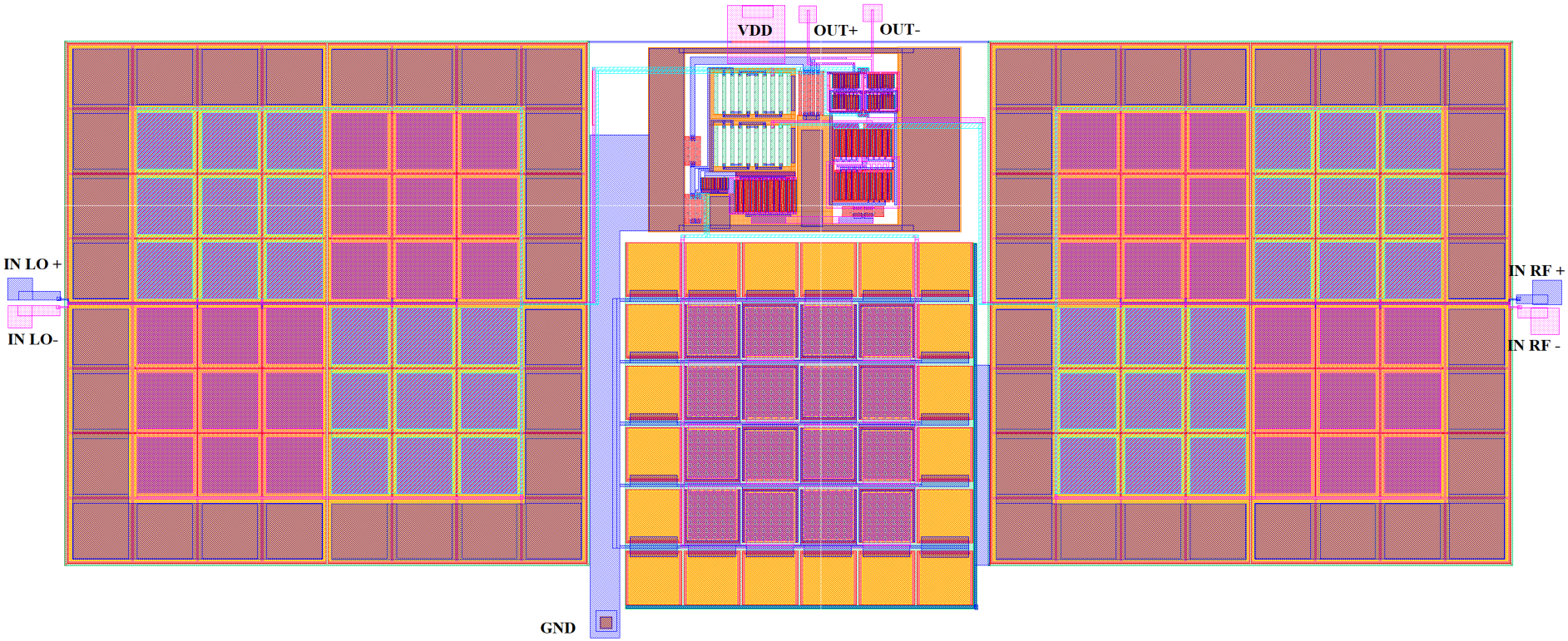
Parameter	$R_{1,3}$	R_2	R_4	R_L	R_S
y $[\mu m]$	112.05	27.45	20.1	32.4	54
x $[\mu m]$	66.3	37.35	37.65	63	13.35
h $[\mu m]$	4.95	5.7	5.7	4.2	12.45
w $[\mu m]$	46.5	26.1	26.25	48.6	4.95
m	4	2	1	1	1
R^* $[\Omega]$	7545	114.5	115.1	289.3	9.94
R_{tot} $[\Omega]$	30180	229	115.1	289.3	9.94

Layout - Full circuit

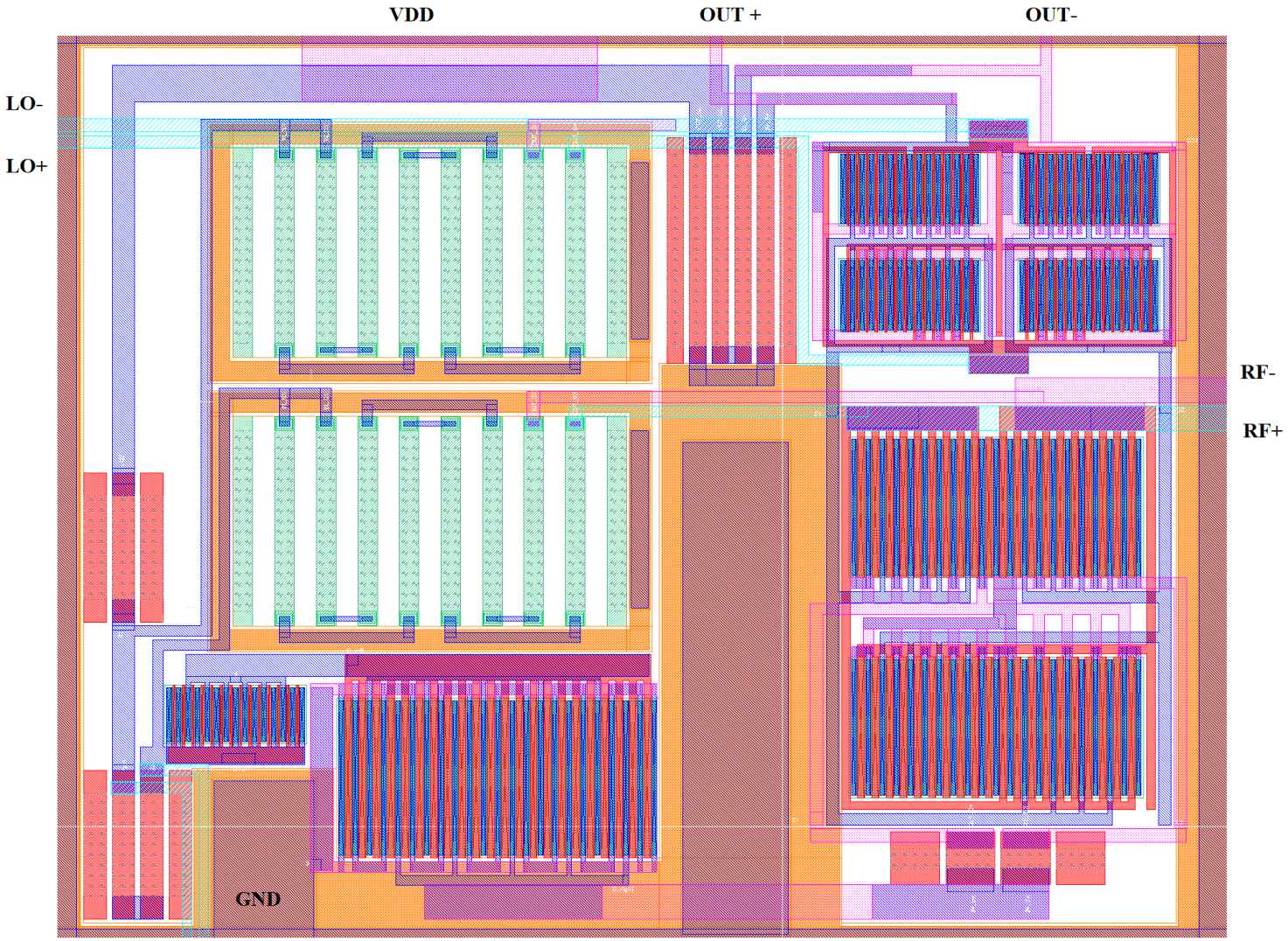
Merging:

- Components placed to shorten interconnections, emphasize symmetries and matching to make paths equal for high frequency signals;
- Body contacts placed where possible, then connected to ground, to capture free charges in the substrate (less noise).
- Occupied area: $A \simeq 0.7mm \cdot 1.8mm = 1.26mm^2$;
- Large amount of area occupied by capacitors.

Layout - Full circuit



Layout - Full circuit without capacitors



1. Analog multipliers theory
   - Introduction
   - Analysis of a Gilbert cell based multiplier
2. Circuit design
   - Design by hand of a down-converting Gilbert cell
   - Design by simulation
   - Layout of the Gilbert cell
3. Simulation vs schematic
   - Simulation setup
   - Time and frequency domain analysis

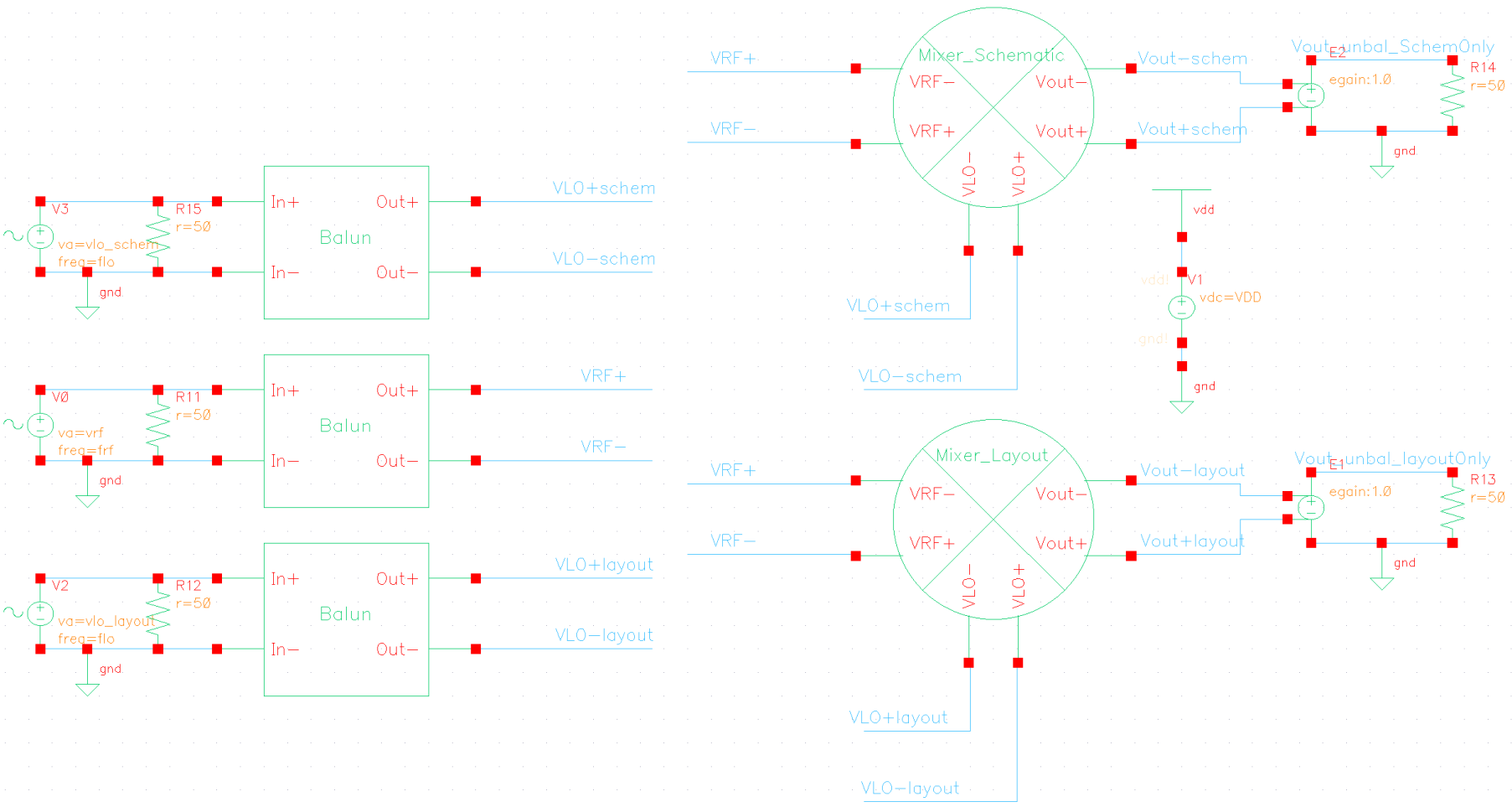
Analysis

Developed analysis:

- Time domain output mixed signal and spectral components;
- Oscillator signal amplitude to maximize output component;
- Conversion gain and 1dB compression point;
- Single tone IIP_3;
- Two tone IIP_3;
- Bandwidth and CMRR of RF stage (output node filtering of output signal, current mixing);
- Static power dissipation;

Used frequencies: f_{LO}=110MHz, f_{RF}=100MHz, with expected f_{IF}=10MHz.

Simulation setup



Simulation setup

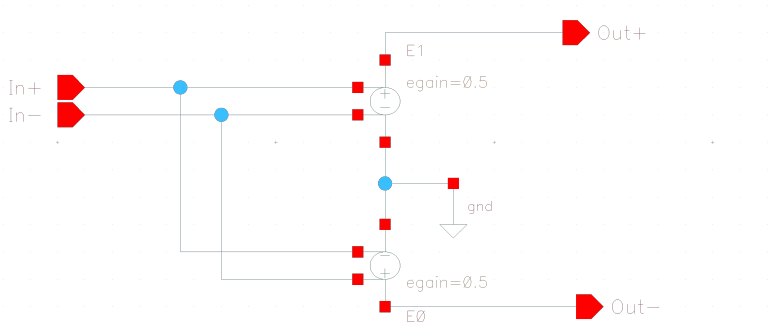


Figure: Balun schematic.

- Ideal baluns simulate a 50 Ω impedance matching condition and produce differential inputs.
- Power supply net, implicitly connected to both layout and schematic.
- Mixer's loads, represented by 50Ω resistors connected to unitary gain driven generator. Used both for ideal impedance matching purposes and to convert differential output from mixers to single-ended.

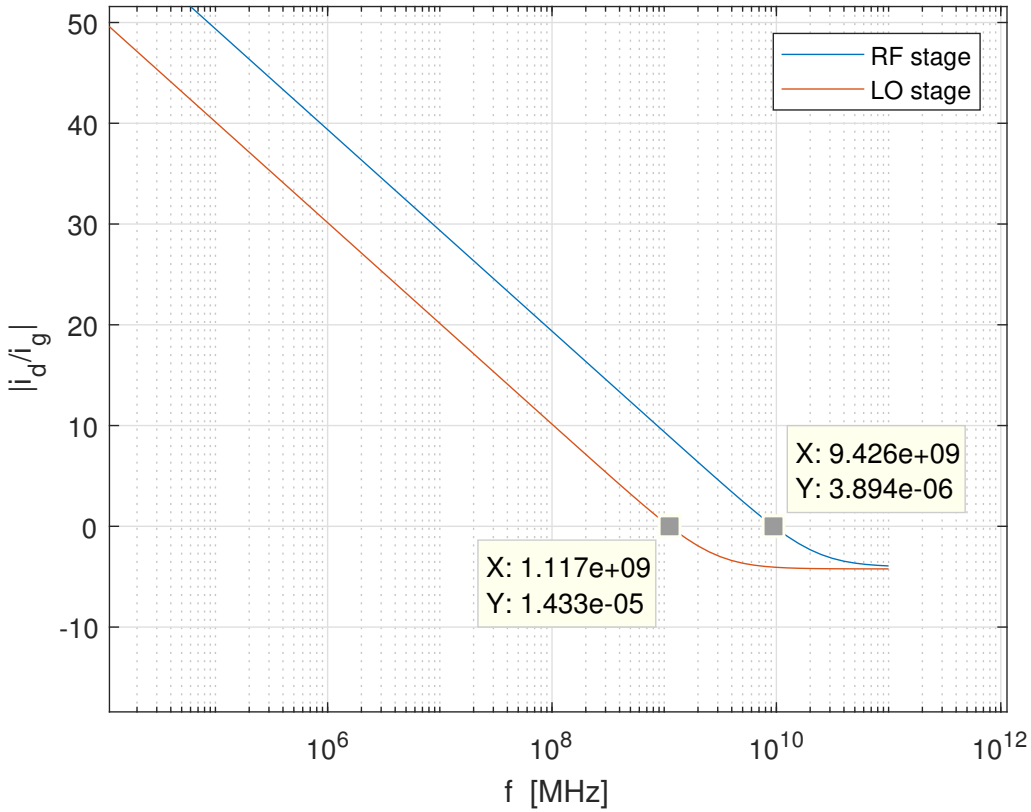
Bandwidth evaluation - Transition frequency

Dynamic analysis is complex when dealing with non-linear circuits. The following results try to qualify the circuit in the best way. Always monochromatic signals have been used.

Bandwidth evaluation - Transition frequency

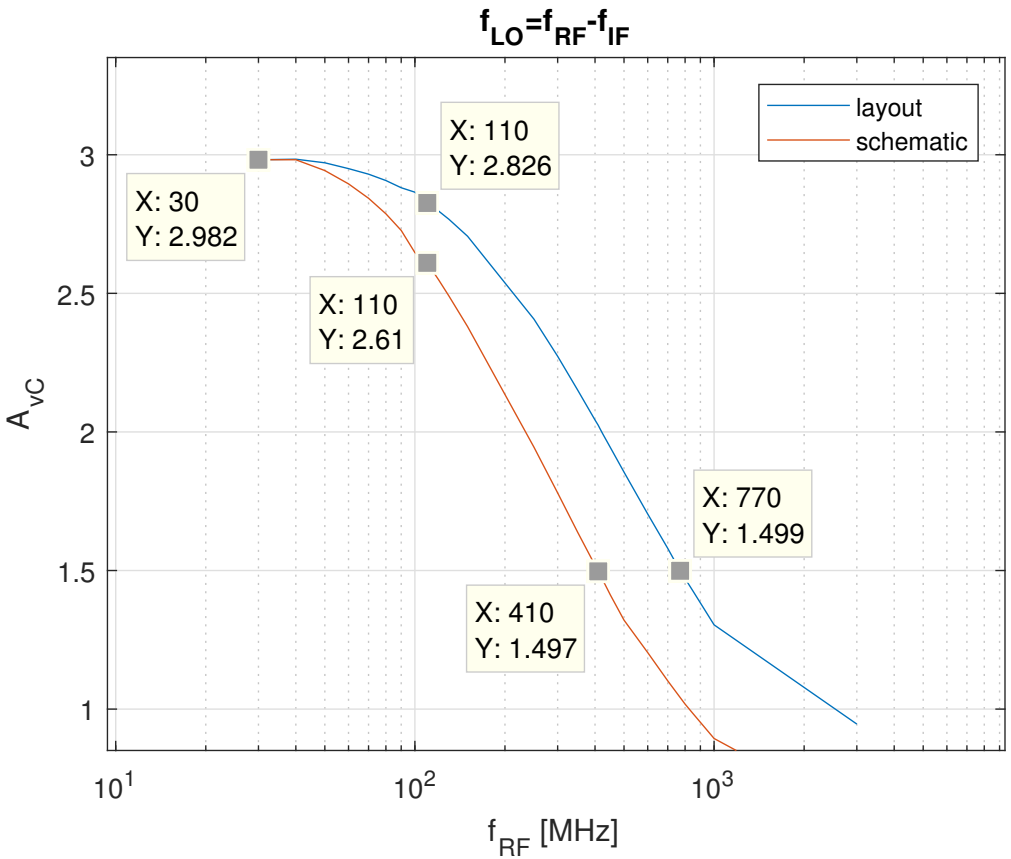
Maximum working frequency must be at least one decade below MOSFET transition frequency f_T. From current gain measurements on M_3 and M_6:

$$f_T|_{RF} = 9.43GHz$$
$$f_T|_{LO} = 1.12GHz$$



Bandwidth evaluation - Transition frequency

Bandwidth evaluated by plotting conversion gain dependency on frequency. The simulation is performed keeping $f_{LO} = f_{RF} - 10\text{MHz}$. -3dB point is located almost two octaves above the maximum operation frequency.



Bandwidth evaluation - Conclusions

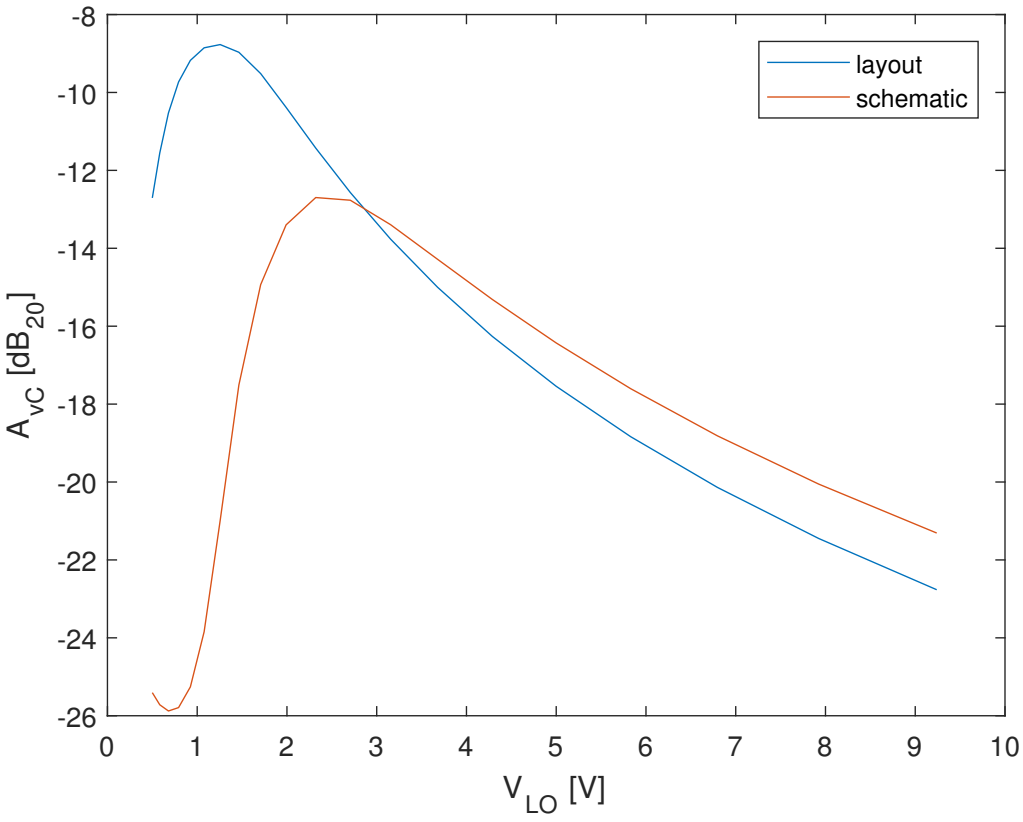
It is important to notice that we **cannot rely on this results** because:

- The technology kit is probably not suited for RF operation;
- The layout extraction does not account for all device and circuit parasitics, that would affect the performances at high frequency. The physical implementation would probably not work;
- Pretending that results are accurate the simulation emulate the worst case operative condition.

Max gain vs LO

LO level must be optimized to get maximum conversion gain. RF power is kept constant, sweeping pump input power.
Layout seems to have better performance than schematic in term of maximum gain.
From simulation:

$$V_{LO,opt}|_{layout} = 1.23V$$
$$V_{LO,opt}|_{schematic} = 2.5V$$



Time domain analysis

It is possible to have a qualitative analysis about the distortion introduced by the circuit (detailed treatise later), by looking at the dft of the mixer's output signal.

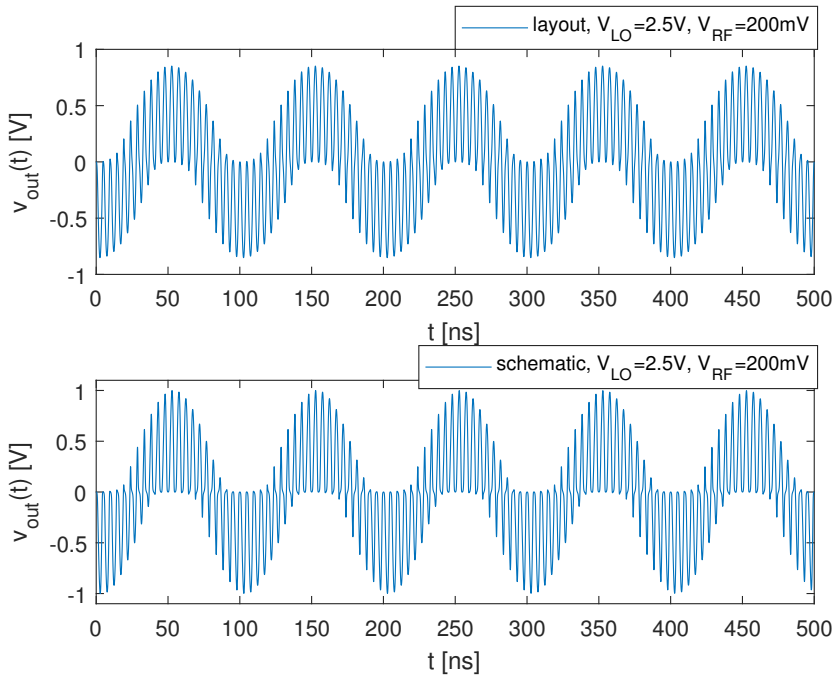


Figure: Time domain waveforms: double balanced differential output with v_{RF}=200mV, f_{RF}=110MHz, v_{RF}=1.23mV, f_{LO}=100MHz.

Output signal spectrum

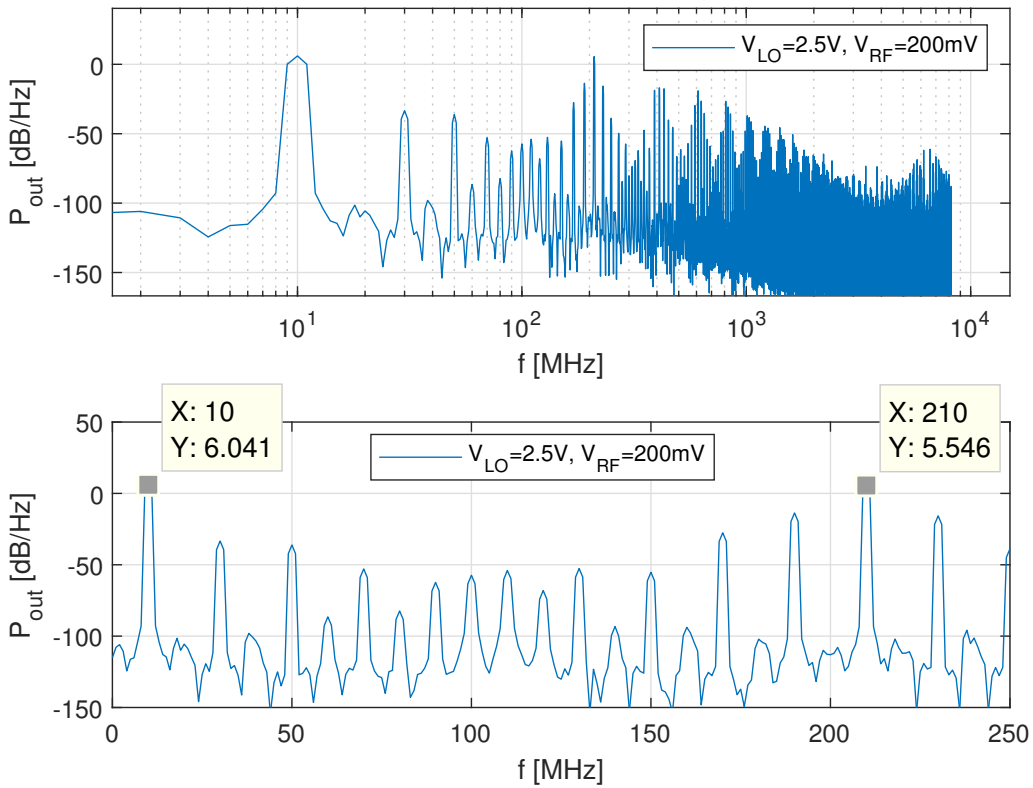


Figure: **Layout**. Discrete Fourier transform: double balanced differential output with v_{RF}=200mV, f_{RF}=110MHz, v_{RF}=1.23mV, f_{LO}=100MHz,cosine squared smoothing function.

Output signal spectrum

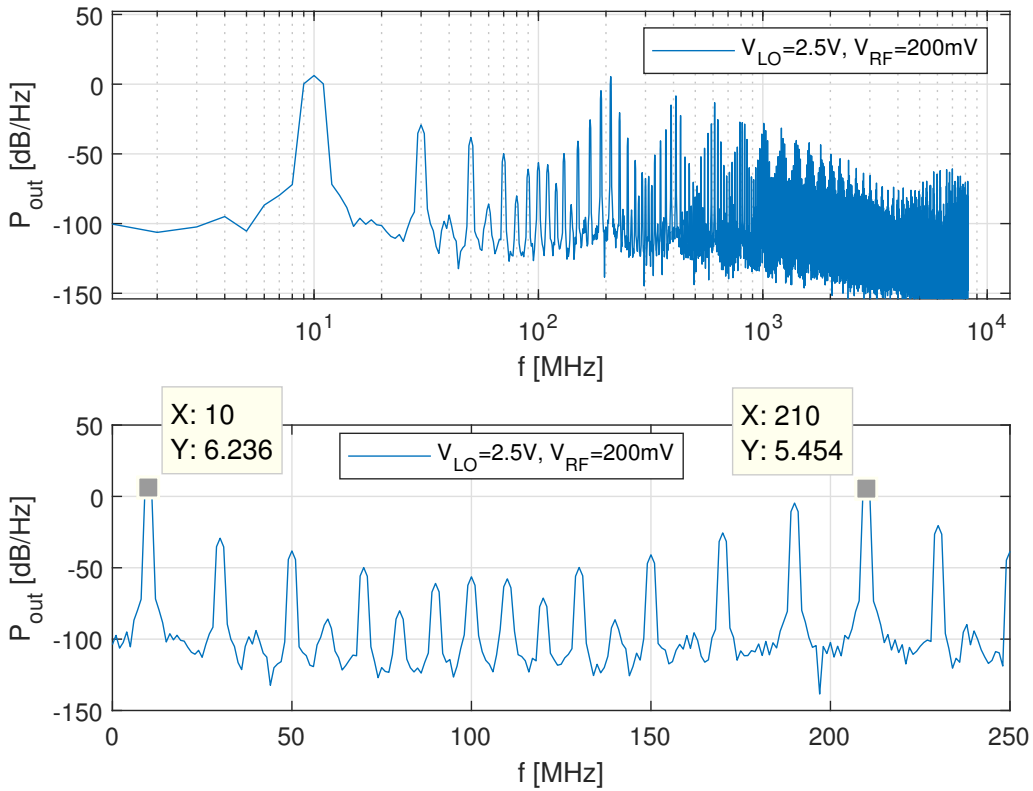


Figure: **Schematic**. Discrete Fourier transform: double balanced differential output with v_{RF}=200mV, f_{RF}=110MHz, v_{RF}=1.23mV, f_{LO}=100MHz,cosine squared smoothing function.