Low Noise Design of a CMOS Gilbert Mixer Cell in 700 MHz

G. O. Barraza Wolf [§] F. H. Gregorio [†] J. E. Cousseau [‡]
Instituto de Investigaciones en Ingeniería Eléctrica (IIIE), CONICET
Departamento de Ingeniería Eléctrica y de Computadoras, Universidad Nacional del Sur
Av. Alem 1253 - (B8000CPB) - Bahía Blanca - ARGENTINA
Email: [§]guillermo.barraza@uns.edu.ar [†]fernando.gregorio@uns.edu.ar [‡]jcousseau@uns.edu.ar

***Abstract*—A design of a MOS Gilbert mixer cell intended for LTE band 28 is presented in this work. The objective is directed to a design with low noise and low third-order intermodulation distortion. The designed mixer can be used in a fully-differential chain, avoiding the implementation of a balun. Since the overall IP3 of a full front-end depends on the IP3 of the each stage, specially those behind the low-noise amplifier (LNA), it is mandatory to have a properly designed mixer. In this design a CMOS 0.18 μm process is employed. The proposed scheme allows to obtain the following characteristic parameters: an IIP3 of 8.69 dBm, a 1dB-compression point of -1.28 dBm, a noise figure of 8.2 dB and draw 30 mA from a 3.3 V power supply.**

***Index Terms*—Gilbert mixer, low noise, CMOS, zero IF receiver, LTE.**

I. INTRODUCTION

Mixer cells are present in all RF receiver front-ends. Main function generally is to down-convert the input signal to a lower frequency. In the case of heterodyne receivers, the target frequency is lower than the RF input but not zero (non-zero intermediate frequency, NZIF). Another important class of receivers is called zero IF (ZIF) where the input signal is shifted directly to baseband. Both receivers are widely used depending on the application under consideration [1].

Among the known designs, Gilbert cell is without a doubt one of the most popular mixer topologies employed in modern RF receivers. The main advantages that offers are: good isolation between ports, reduction of second order harmonics and moderate conversion gain. On the other hand, the main disadvantages are: low third-order intercept point (IP3) and medium-to-high polarization current [2].

Some designs using Gilbert topology have high IP3 and good noise figure, but the conversion gain is low [3]–[5]. Other designs, have high conversion gain, but the noise figure and IP3 may be inappropriate for certain applications [6]–[9]. The design of a double-balanced cell is directed in this work to achieve low noise and high IP3 regarding broadband mobile CMOS applications.

The paper is organized as follows. In Section II the basic Gilbert cell is described. Section III describes the detailed design of the mixer including equations and employed rules. Simulation results are presented in Section IV. Finally, Section V presents the conclusions.

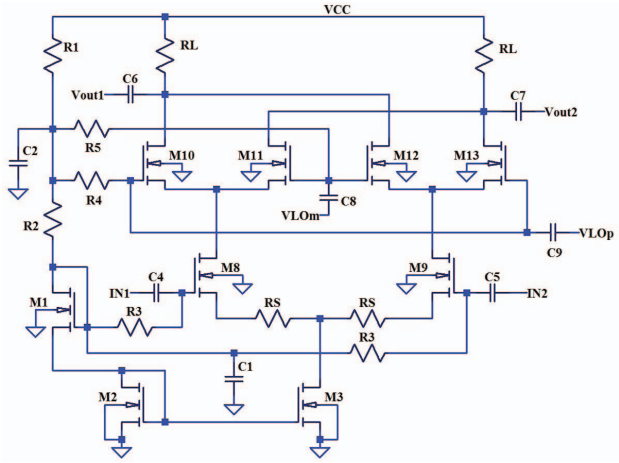

Fig. 1. Gilbert mixer cell diagram.

II. BASIC GILBERT MIXER CELL

Gilbert mixer architecture, shown in Fig. 1, consists of two cross-coupled differential pairs biased by a common current source. An RF input signal is applied to the lower transistors M8-M9, which form a differential amplifier whose outputs are modulated by the commutation transistors M10, M11, M12 and M13. These transistors are switched on and off by a 180-degree out-of-phase signal applied from the local oscillator (LO). Since M10-M12 transistors are switched at different instants of time, IN1 and IN2 signals at the drains of M8-M9 are sent to Vout1 terminal. Similarly, when M11-M13 transistors are switched, IN1 and IN2 signals are connected to the Vout2 terminal [2], [10].

It is often useful to include source resistances for the M8-M9 differential pair to improve linearity and increase the input signal dynamic range. That can be done at the cost of some increase in the noise figure as discussed in the following section. Just small source resistances are required for M8-M9 because significant values may reduce the gain-bandwidth product and can also lead to instability [11].

III. GILBERT MIXER CELL DESIGN

To design a robust Gilbert mixer cell, it is necessary to have special care with parameters such as

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a) Supply voltage
b) Intermodulation distortion (IP3)
c) Conversion gain
d) Noise figure
e) 1 dB compression point
f) Input and output impedances

A. Specifications

The following specifications are defined with the premise to design a low-complexity low-noise mixer with applications in front-ends of LTE receivers.

$$\begin{cases} \text{Freq. RF: 700 MHz} \\ \text{Freq. LO: 700 MHz} \\ \text{Power comsumption} \leqslant \text{100 mW} \\ \text{IP3} > \text{5 dBm} \\ A_v > \text{6 dB} \\ \text{P1dB} > \text{-5 dBm} \\ \text{Zin: 50 } \Omega \\ \text{Vcc: 3.3 V} \end{cases}$$

B. Cell design

There are several ways to design the differential pair M8-M9 in Fig. 1 [4], [5]. Since it amplifies the RF input, the noise added by this pair must be minimized in order to obtain a low-noise mixer cell. A good method to obtain low power dissipation with low noise is the procedure described in [12], where the optimum transistor's width is given by

$$W_{opt} = \frac{1}{3\omega L C_{ox} R_g} \tag{1}$$

where ω is the operation frequency $2\pi 700 \times 10^6$ rad/sec, L is the length of transistor 3 $L_{min} = 0.54\ \mu m$, C_{ox} is the MOSFET oxide capacitance per unit of area $8.63 \times 10^{-3}\ F/m^2$, and R_g is the source resistance (50 Ω). Therefore, the optimum width for transistors is

$$W_{opt} = 833\,\mu m$$

Gate-source capacity C_{gs} is dependent of transistor's size. Then, the capacity can be estimated as [13]

$$C_{gs} = \frac{2}{3} W L C_{ox} = 2.58\,pF \tag{2}$$

Other important aspect to take care with for high-frequency applications is the speed at which design can operates. Transition frequency for MOSFET devices can be approximated by [13]

$$f_T \approx \frac{g_m}{2\pi C_{gs}} = \frac{3KP_n(V_{gs} - V_T)}{4\pi L^2 C_{ox}} = \frac{3\mu_n V_{od}}{4\pi L^2} \tag{3}$$

where V_{od} is the overdrive voltage. From Eq. 3 is clear that to obtain high speed devices, short channel lengths should be employed.

Note that high V_{od} voltages helps to achieve high f_T but reduces the output swing. Therefore, some constraint on the channel length must be imposed. Lengths from 2 to 5 times the minimum technology length L_{min} are usually a good practice rule [12]. With this criteria it is chosen $L = 3.L_{min}$ in Eq. 1.

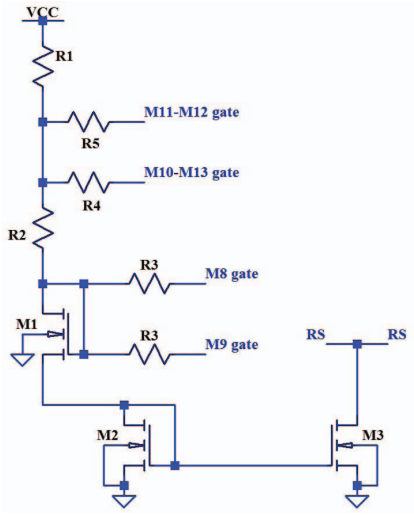

Fig. 2. Mirror current source.

Other aspect to consider is the value of source resistance R_S. In this design, it is used $R_S = 10\,\Omega$. Larger values will improve linearity but increase the noise figure. Some designs replace source resistances with source inductances to avoid additional noise and the DC drop, but the resulting behaviour is frequency-dependent which is not desired.

The total current through M3 is chosen in 30 mA according to a power restriction. Therefore, current I_D through M8 and M9 is 15 mA and V_{GS} can be calculated from MOSFET saturation equation. Then

$$V_{GS} = \sqrt{\frac{I_D}{\mu_n C_{ox}(1/2)(W/L)}} + V_T = 0.682\,V \tag{4}$$

Knowing the current I_D, transconductance of M8-M9 can be calculated as [13]

$$g_m = \sqrt{2\mu_n C_{ox} I_D (W/L)} = 0.0749\,S \tag{5}$$

Now, using Eq. 3, the transition frequency is $f_T \approx 4.6\,GHz$ which is 5 times larger than operating frequency.

On the other hand, the voltage conversion gain can be approximated by [14]

$$A_v \approx \frac{2}{\pi} \frac{R_L}{R_S + \dfrac{1}{g_m}} \tag{6}$$

which conduces to $R_L = 73\Omega$ with the desired gain and R_S values.

C. Bias design

Mirror current source employed to set the current and bias in all transistors of Fig. 1 is shown separately in Fig. 2. This design employs $20K\Omega$ resistances to isolate input signals from polarization. Table I summarizes the design parameters of the current source.

Component	Value
M1	8.34/0.54 μm
M2	8.34/0.54 μm
M3	833/0.54 μm
R1	2.67 $K\Omega$
R2	556 Ω
R3, R4, R5	20 $K\Omega$

TABLE I
DESIGN PARAMETERS OF THE CURRENT SOURCE.

IV. SIMULATION RESULTS

Some analyses were carried out to evaluate the performance of the proposed design. Simulations, made in Cadence Spectre, were based on PSS (Periodic Steady-State), PAC (Periodic AC) and PXF (Periodic Transfer Function) analyses [15]. Simulation set-up is presented in Fig. 3.

Voltage conversion gain versus LO power curves are shown in Figs. 4 and 5. LO power was varied in the range of -10 to 20 dBm. Fundamental tone in simulator and RF input frequency were set in 700 MHz (direct conversion architecture). Note that a load impedance of 1000 Ω at IF port allows to handle a wider range of LO power to obtain the minimum specified gain of 6 dB. Power levels shown in these figures and the corresponding *rms* LO voltages are summarized in Table II. These values are useful to determine the required LO signal level.

Fig. 6, illustrates the 1 dB compression point. It can be observed, that compression level is -1.28 dBm.

Third-order intercept point (IP3) analysis, shown in Fig. 7, was carried out varying power of RF signal from -30 dBm to 10 dBm. From this analysis, the IIP3 (input referred IP3) obtained is 8.7 dBm.

Isolation between RF-LO, LO-RF, LO-IF and RF-IF ports are illustrated in Figs. 8, 9, 10 and 11, respectively. In our design isolation values were not specified. However, good isolation levels were reached as illustrated in these figures.

DSB noise figure vs. frequency for 6.5 dBm LO power level is shown in Fig. 12.

Finally, Table III presents a performance comparison with previous published papers. It can be observed that our circuit has a high P1dB and IIP3, which means good linearity. However, even when the noise figure (NF) is small, is not as small as other designs that use source degeneration inductance [16], [17].

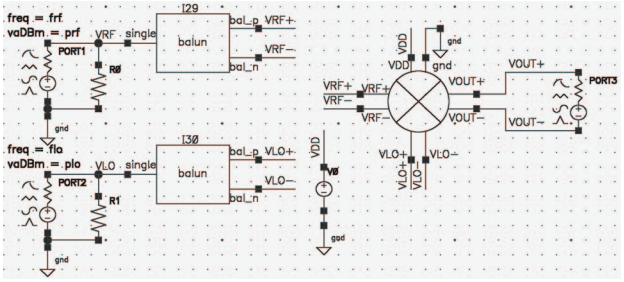

Fig. 3. Simulation set-up.

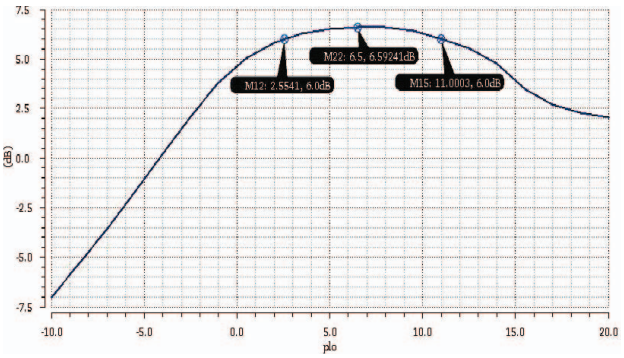

Fig. 4. Voltage conversion gain vs. LO power (Load impedance at IF port was set in 500 Ω).

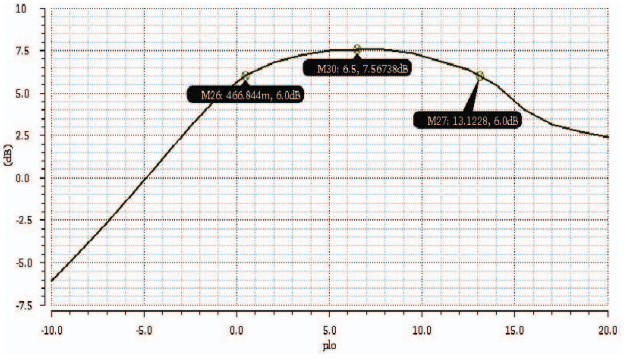

Fig. 5. Voltage conversion gain vs. LO power (Load impedance at IF port was set in 1000 Ω).

Load IF port = 500 Ω				Load IF port = 1 KΩ			
plo $[dBm]$		vlo $[V_{rms}]$		plo $[dBm]$		vlo $[V_{rms}]$	
Min.	2.5	Min.	0.3	Min.	0.5	Min.	0.2
Ideal	6.5	Ideal	0.5	Ideal	6.5	Ideal	0.5
Max.	11	Max.	0.8	Max.	13.1	Max.	1

TABLE II
LO POWER AND *rms* VOLTAGE NEEDED TO OBTAIN THE MINIMUM SPECIFIED GAIN OF 6 DB FOR TWO DIFFERENT LOAD IMPEDANCES AT IF PORT (PLO: LO POWER. VLO: LO *rms* VOLTAGE).

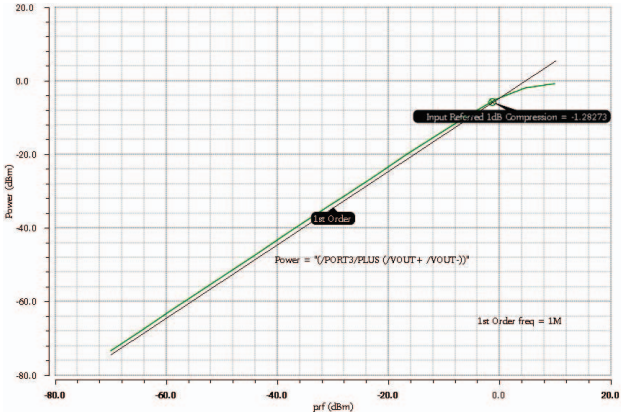

Fig. 6. 1 dB compression point (P1dB).

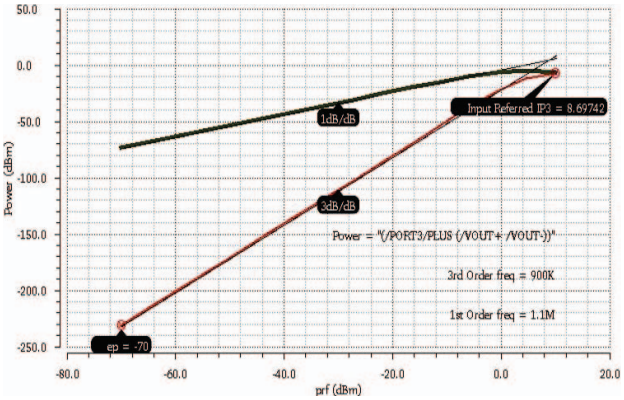

Fig. 7. Input referred third-order intercept point (IIP3).

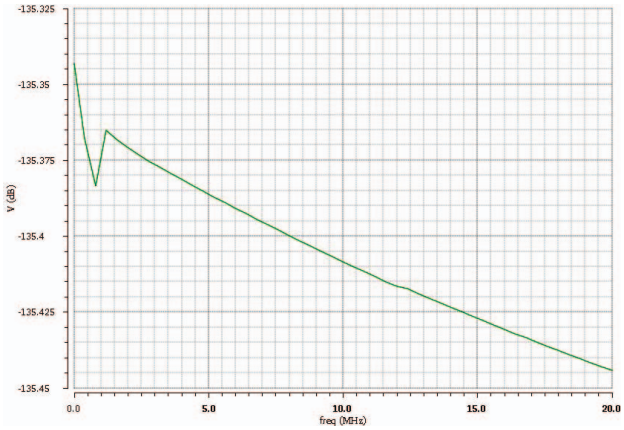

Fig. 8. Isolation RF-LO ports.

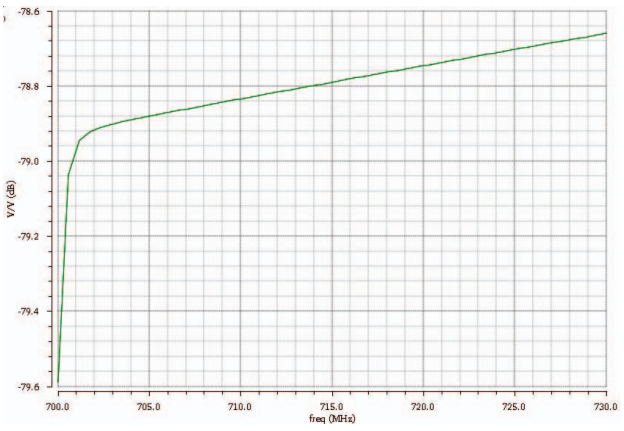

Fig. 9. Isolation LO-RF ports.

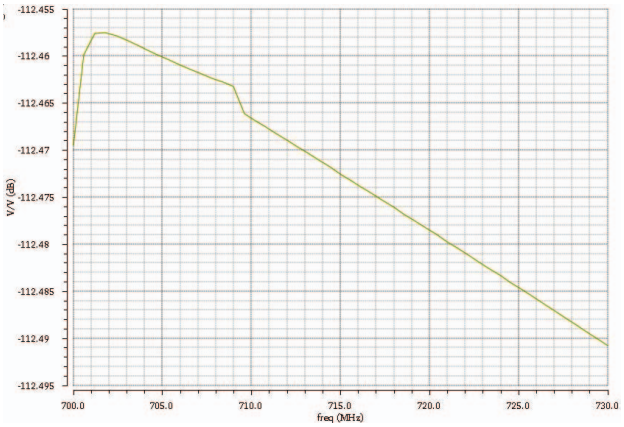

Fig. 10. Isolation LO-IF ports.

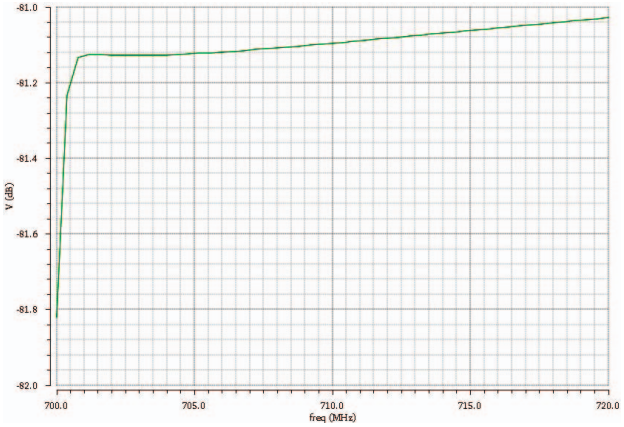

Fig. 11. Isolation RF-IF ports.

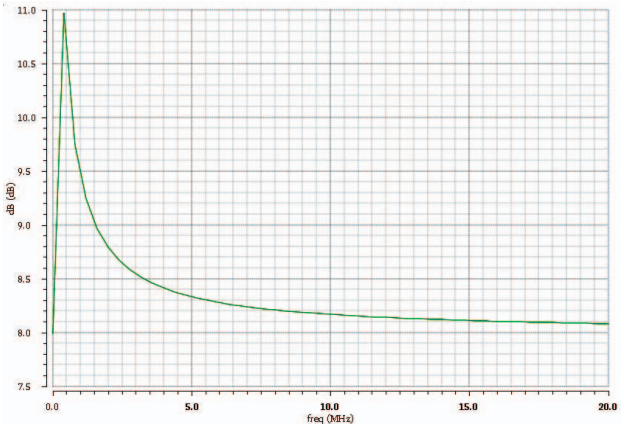

Fig. 12. DSB noise figure.

V. CONCLUSIONS

This work, shows a design of a Gilbert mixer addressing low-noise and low third-order intermodulation products reaching a better performance if compared with the previous proposals. Due to mixer has differential RF inputs, the presented design is suitable for using with differential LNAs, avoiding

Ref.	Tech. [nm]	Freq. [MHz]	P1dB [dBm]	IIP3 [dBm]	NF [dB]	CG [dB]	VCC [V]
This work	180	700	-1.28	8.69	8.2	7.5	3.3
[16]	65	700	NA	0.5	6.4	15.4	1.8
[18]	350	900	-15.4	-3.3	NA	1.1	2
[19]	90	916	-10.48	8.45	NA	-6.37	1.2
[17]	180	2650	-23.5	-14	6.5	24	1.2

TABLE III
COMPARISON WITH OTHER PUBLISHED PAPERS.

baluns whose behavior is normally frequency-dependent. The IIP3 reached is enough to meet in-band IIP3 specifications [20]. On the other hand, the optimum width for RF transistors ensures low noise conditions. It is included a negative feedback in the presented design with source resistances verifying an improvement in the mixer linearity. It is worth to mention that applications with higher values of IIP3 may require the use of a passive mixer [20]. Parasitic effects of layout were not analyzed in this work, but are taken into account in the implementation being currently developed.

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