Technische Universität Hamburg-Harburg

Institut für Nanoelektronik

Design and Characterization of CMOS Gilbert Mixer at 130 nm Technology for Impedance Measurement System of Human Cell

Institute for Nanoelectronics

Master Student Project

from

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Foreword

I would like to thank my parents, who provided me with all the support I needed throughout my academic life. Without their efforts and guidance, I would not be here to do Master course. I would like to thank Prof. Krautschneider for providing me with the opportunity to work at the Institute for Nanoelectronics, and for providing me with adequate background knowledge in his lectures in the previous semesters. I am grateful to my supervisor Paola Vega, for guiding me throughout my project work, and pointing me in the right direction whenever I was in crossroads. I would also like to thank Mr. Mielke, for providing me with support in setting up my account, and access to the Cadence software. Last but not the least, I would like to thank my friends (particularly Pragothi bora, Jorge Prada, Rajiv Ranjan) who were doing their project at the institute in parallel, for providing me with good company and helping me to solve problems related to cadence during my work.

Hamburg, 16 July 2014 Guru kartheek Pedapalli

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1 Introduction

In the recent days, Electrochemical Impedance Spectroscopy (EIS) is widening its area of applications into many fields. There is a significant boost in the rate of publications in this topic [Las], [BECRW99]. In simple terms, Electrochemical impedance spectroscopy is a method of measuring the electrical impedance of a substance as a function of the frequency of an applied electrical current. EIS is measured based on the external field's interaction with the dipole moment of a particular sample, usually stated by permittivity. It is also regarded as an experimental technique that describes electrochemical systems. This method gauges system impedance over a series of frequencies. Thus, frequency response involving dissipation properties and energy storage is disclosed.

Tissue electrical impedance is used to differentiate normal and cancerous tissues in a variety of organs, including breast, cervix, skin, bladder and prostate [HR07].This method is useful to characterize cellular changes quantitatively. Predominantly, the characteristics and integrity of the population's plasma membranes, cell volumes, intra and extracellular conductivities influence the impedance spectrum.[Mem] Thus, EIS can be used as a method of identifying detectable cellular responses which gives the advantage of collecting prognostic information. [RY05]

Electrical impedance spectroscopy is usually measured by applying an AC potential to the biological cell and then measuring the current through the cell. Assume that we apply a small sinusoidal potential excitation. The response to this potential is an AC current signal. This excitation is done so that the cell's response is pseudo-linear. In a linear (or pseudo-linear) system, the current response to a sinusoidal potential will be a sinusoidal signal at the same frequency but shifted in phase (see Figure 1.1).

The excitation signal, expressed as a function of time, has the form

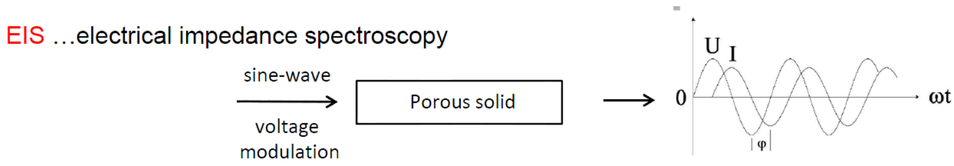

Fig. 1.1. Sinusoidal Current Response in Linear System

$$V_t = V_0 sin(\omega t) \tag{1.1}$$

where V_t is the potential at time t, V_0 is the amplitude of the signal, and 'ω' is the radial frequency. The relationship between radial frequency 'ω' (expressed in radians/second) and frequency f (expressed in Hertz) is:

$$\omega = (2\pi f) \tag{1.2}$$

In a linear system, the response signal, I_t, is shifted in phase (ϕ) and has a different amplitude than I_0.

$$I_t = I_0 sin(\omega t + \phi) \tag{1.3}$$

An expression analogous to Ohm's Law allows us to calculate the impedance of the system as:

$$Z = \frac{V_t}{I_t} = \frac{V_0 sin(\omega t)}{I_0 sin(\omega t + \phi)} = Z_0 \frac{sin(\omega t)}{sin(\omega t + \phi)} \tag{1.4}$$

The impedance is therefore expressed in terms of a magnitude, Z_0, and a phase shift, ϕ

1.1 Project Objective

In our project, the focus is to design and to define the methodology to characterize the **CMOS Gilbert mixer** which is one of the important components used in the integrated circuit in order to find the value of ϕ, phase shift of a current that is passed through the human cells/biological tissues. When we find the above ϕ value in impedance formula, we know all other parameters value to get the value of the impedance. Our main goal is not only measuring impedance of biological tissues but also to characterize their permittivity and conductivity. The integrated circuit which is designed with 130nm technology transistors consists of voltage controlled oscillator, operational amplifier and a Gilbert mixer with a low pass filter at its end. It is used to measure the impedance characteristics of Human cell. Given below is the block diagram of the impedance measurement system.

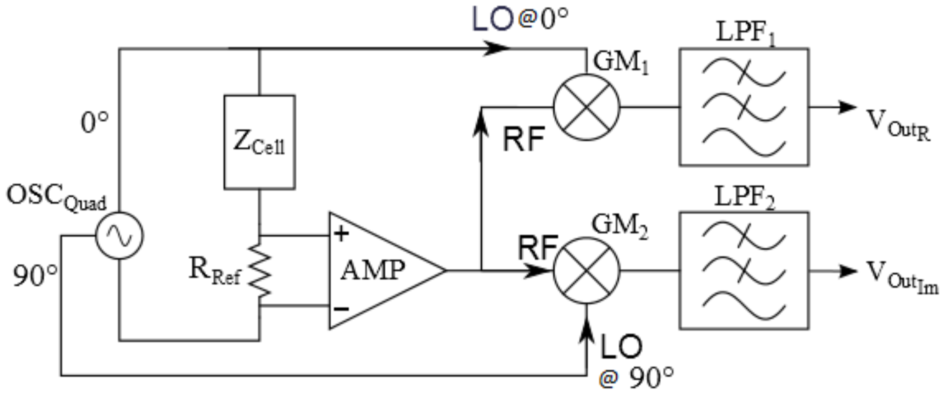

Fig. 1.2. Block Diagram of Impedance Measurement System

Basic Operation of the Circuit: This gives a brief overview of operation that takes place in integrated circuit and also importance of the mixer which will be designed in this project.

In this circuit, the voltage controlled oscillator sends two voltage signals V_{LO} and quadrature phase shifted V_{LO} to the input of the two identical Gilbert mixers which have to be designed in this project. The same voltage signal from oscillator is applied to the human cell/biological tissue which is connected in a parallel path to the oscillator. The Z_{cell} in the circuit refers the human cell. Once the current passes the human cell, it undergoes a phase shift of ϕ and this phase shifted current has to be calculated to find the impedance of cell. So, to get that current passing through the human cell, we have connected the small resistance in series to the cell such that the voltage drop at the resistor is negligible when compared to the input voltage. So, this minute current signal is amplified using an operational amplifier connected across the resistor R_{Ref} in the circuit. The output of the operational amplifier is an amplified RF signal which is sent as one of the inputs to the Gilbert mixer. This Gilbert mixer takes RF signal and LO signals and delivers the mixed output signal which has two frequency components. This

output signal is passed through the low pass filter such that high frequency component is filtered out. The voltage controlled oscillator sends its quadrature shifted signal to another mixer input where it mixes with the same amplified RF signal and delivers the quadrature output component of the previous mixed signal. The reason for calculating the quadrature mixed output signal is $\sin(\phi)$ which is proportional to imaginary part of the impedance, so permittivity can be calculated. $\cos(\phi)$ which is proportional to real part of impedance, so conductivity can be calculated. These both components of zero frequency are essential to calculate the phase difference of the current signal that passes through the human cell. The following is the mathematical analysis of the process that takes place in the impedance measurement system.
Let the voltage delivered by the oscillator be

$$V_{LO}(t) = A_{LO}cos(\omega t) \tag{1.5}$$

The voltage at the output of the operational amplifier be

$$V_{RF}(t) = A_{RF}V_{Ref}(t) \tag{1.6}$$

Since, we know from the above discussion,

$$V_{Ref}(t) = R_{Ref}I_0cos(\omega t + \phi) \tag{1.7}$$

then, the voltage at the output of the mixer can be

$$V_{IF}(t) = V_{LO}(t).V_{RF}(t) \tag{1.8}$$

$$V_{IF}(t) = A_{LO}cos(\omega t).A_{RF}V_{Ref}(t) \tag{1.9}$$

$$V_{IF}(t) = A_{LO}cos(\omega t).A_{RF}R_{Ref}I_0cos(\omega t + \phi t) \tag{1.10}$$

$$V_{IF}(t) = A_{LO}A_{RF}R_{Ref}I_0(cos(\omega t)cos(\omega t + \phi t)) \tag{1.11}$$

$$V_{IF}(t) = \frac{A_{LO}A_{RF}R_{Ref}I_0}{2}(2cos(\omega t)cos(\omega t + \phi t)) \tag{1.12}$$

$$V_{IF}(t) = \frac{A_{LO}A_{RF}R_{Ref}I_0}{2}(cos(2\omega t + \phi) + cos(\phi)) \tag{1.13}$$

The above equation as a mixer output when passes through the low pass filter turns into,

$$V_{IF}(t) = \frac{A_{LO}A_{RF}R_{Ref}I_0}{2}(cos(\phi)) \tag{1.14}$$

Let us name it as $\mathrm{V}_{IF_R}(\mathrm{t})$, where

$$V_{IF_R}(t) = \frac{A_{LO}A_{RF}R_{Ref}I_0}{2}(cos(\phi)) \tag{1.15}$$

Similarly, at the output end of other mixer , we get

$$V_{IF_I}(t) = \frac{A_{LO}A_{RF}R_{Ref}I_0}{2}(sin(\phi)) \tag{1.16}$$

Now, by dividing the above two equations, we get

$$\frac{V_{IF_I}(t)}{V_{IF_R}(t)} = (tan(\phi)) \tag{1.17}$$

$$\phi = arctan\frac{V_{IF_I}(t)}{V_{IF_R}(t)} \tag{1.18}$$

From the above equation, we can find the value of ϕ as we know other parameter values. By substituting this value of ϕ in the equation 1.4 for the impedance Z, we can find the impedance of the human cell. This approach is so simple and cheaper. The only thing to be considered is to make a good design (better figures of merit) of all components in the impedance measurement system. As discussed earlier, there are lots of applications with this system in finding the characteristics like permittivity and conductivity of human cells/biological tissues. In this project, the main objective is to design the Gilbert mixer that is used in this impedance measurement system. As it is a CMOS mixer, it can operate safely in a frequency range of 1MHz-10GHz. Because, at high frequencies the gate of CMOS transistor acts as short circuit which results in unwanted gate current entering into circuit. The high operating frequency of the MOS transistor depends upon transition frequency f_T. Usually, transistors must be applied at frequencies well below f_T to be useful as amplifiers and oscillators [Jon95].

1.2 Project Organization

It is very important to understand the basic working of mixer and different types of the mixers before starting the design of the Gilbert mixer. Chapter 2 discusses briefly about the basic operation of a mixer and different topologies of mixer and also about its non linearity. Chapter 3 illustrates the design overview, design constraints, design analysis and design approach of the mixer circuit.

Chapter 4 introduces the simulation of mixer, different types of simulations that can be done using Sprectre RF Cadence simulator. Figures of merit of mixer circuit and all the steps to characterize important parameters of mixer to know whether it is designed properly or do we need to improve the design further. All pre-layout simulations are done in this chapter. It is one of the important chapters to describe the properties of the mixer and to learn the methodology that characterize a Gilbert mixer using the simulation environment in Cadence's Virtuoso.

Chapter 5 gives a brief overview of Layout of the mixer circuit and the modifications that are done to the circuit after designing the layout. Multi finger transistors and symmetry of layout are described here. Also, post layout simulations were done to characterize the parasitic extracted Gilbert mixer cell and their results are showed in this chapter. Chapter 6 summarizes the conclusions of this work. Also, regarding the next step for this project were discussed.

2 Mixer Topology

2.1 Mixer Definition

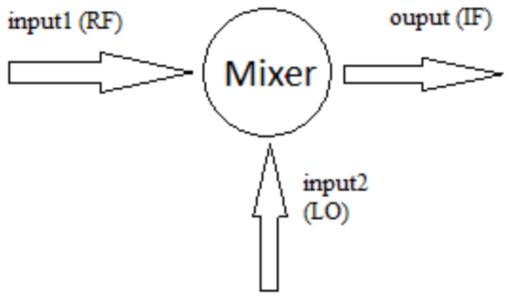

Fig. 2.1. Basic Mixer Model

A mixer is a device that combines two or more signals into one or two composite output signals. It converts RF power at one frequency into power at another frequency that makes signal processing easier. The basic reason for frequency conversion is to allow amplification of the received signal at a frequency other than the RF, or the audio frequency.

Non-Linearity: Non-linear means that the relationship between input power (or voltage) and output power does not plot on a graph as a straight line. Mixer is also a non-linear device, meaning that for small signals it will exhibit constant conversion loss, but at large signals the response will compress and then saturate.

2.2 Types of Mixers

Generally, there are two basic types of mixer circuits. They are:
Additive mixer: It adds two or more signals to produce a composite signal that contains the frequency components of each of the source signals.
Multiplicative mixer: It produces an output signal equal to the product of the two input signals. Multiplicative mixers are often used in conjunction with an oscillator in

the communications field to modulate signal frequencies. Multiplicative mixers can be coupled with a filter to either up-convert or down-convert an input signal frequency, but they are more commonly used to down-convert to a lower frequency to allow for simpler filter designs as done in this project.

The above two types of mixers are further classified into passive and active mixers depending upon the elements used in the mixer device:
Passive Mixers: They use one or more diodes and rely on the non-linear relation between voltage and current to provide the multiplying element. The desired output signal is always of lower power than the input signals. Passive Mixers have higher conversion losses and hence higher noise figures than active mixers although they have better IM3 performance.
Active Mixers: They use an amplifying device (such as a transistor or vacuum tube) to increase the strength of the product signal. Active mixers improve isolation between the ports, but may have higher noise and more power consumption. An active mixer can be less tolerant of overload. But, active mixer can accomplish two jobs at the same time: they mix and they amplify.

Additionally, mixers are classified by their topology into single balanced mixers and double balanced mixers.
Single Balanced Mixer: It allows some of both input signals to pass through to the output. A single balanced mixer is arranged so that either the local oscillator (LO) or signal input (RF) is suppressed at the output, but not both.
Double Balanced Mixers: It has symmetrical paths for both inputs, so that neither of the input signals and only the product signal appears at the output.[Poo12], all ports of this mixer are inherently isolated from each other. However, double balanced mixers are more complex and require higher drive levels than single balanced designs.

Multiplicative mixers have been implemented in a wide variety of ways. Because of that, they are used for frequency conversion of input signals to the required output frequency which can be used according to our application. In this project, we use multiplicative mixer because we need to convert the frequency of the RF input signal that is mixed with LO signal to give an amplified down conversion signal of zero frequency, collected at the output of the low pass filter. This down converted zero frequency signal is used in further calculation of the impedance of the human cell.

2.3 Why Gilbert Mixer ?

Because, Gilbert mixer is the most popular one among the multiplicative mixers. It is an active double balanced mixer and was invented by Howard Jones in 1963. It is chosen in the project because:
- it provides reasonable conversion gain (IF power output with respect to the RF gain input),
- good rejection at the RF and LO ports (attenuation between signal inputs at the RF and LO and its level as measured at the output port),
- differential IF output connection [JM08]
- it is an active mixer in which transistors are used to improve the product signal and
- due to its double balanced topological structure which results in high linearity, improved suppression of spurious products (all even order products of LO and RF are suppressed), better isolation at the ports and also less susceptible to supply voltage noise.
Due to the above advantages, it is widely used as a modulator, phase detector and multiplier in many communication applications. Gilbert mixer improves the quality of mixing the RF and LO signals and delivers the output of required frequency and the feed-through. In this project, the double balanced active down conversion Gilbert mixer is designed with the analyzed specifications.

The active double balanced Gilbert cell is shown below:

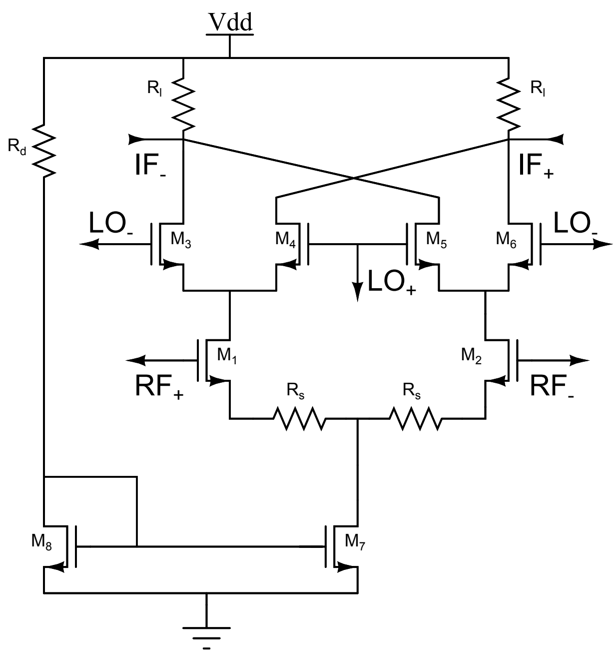

Fig. 2.2. Gilbert Mixer Cell

3 Mixer Design

3.1 Design Overview

The simple Gilbert mixer has four stages. They are:

1. Gain Stage : It is the first stage of the mixer which should have high linearity to handle the power from the operational amplifier in the circuit. The two transistors with the RF terminals act as an amplifier increasing the gain of the signal before mixing.[Pha] To improve linearity, source degeneration resistors can be added to the gain stage of the amplifier. These resistors can be adjusted to increase or decrease linearity or gain. The transistors should be biased to remain in saturation region for high current. The overdrive voltage (V_{gs} – V_t) should be around (200mV to 400mV). The gain of the mixer can be increased in the following ways:

1) Increasing 'W' while keeping 'L' at minimum,

2) Decreasing the source degeneration resistor will increase the gain but decreases linearity.

3) Since, gain of the mixer is proportional to g_m, increasing current also increases the gain as shown by the equation below,

$$g_m = \frac{2I_d}{V_{GS} - V_t} \tag{3.1}$$

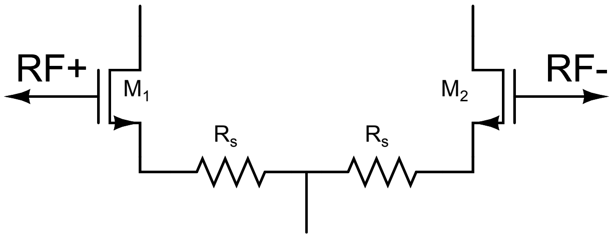

Fig. 3.1. Gain Stage of Gilbert Mixer Cell

2. Switching Stage : In this stage, LO signals should be reasonably large to ensure that the mixer switches properly. Noise is also minimized for large LO. However, when the LO becomes too large, this leads to spikes in the signals, reducing switching speed and increase LO feed through to IF or back to RF ports [Rog].The result of the spikes can also cause transistors to leave the saturation region. The problem of LO to IF feed through has already been mitigated as some of the feed-through at the output is cancelled out due to a 180 degrees phase shift of LO signal in double-balanced Gilbert cell structure. Therefore, transistors in the switching stage also should operate in saturation region to enable perfect switching and reduce the feed through. When one transistor pair is conducting, we want the other pair to be completely off. If two pairs are conducting current at the same time, it will generate noise. Therefore, the overdrive voltage ($V_{gs} - V_t$) should be as close to zero as possible. This is the midpoint between turning the transistor on and off.

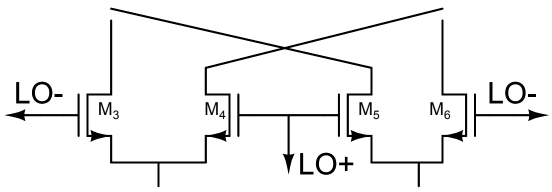

Fig. 3.2. Switch Stage of Gilbert Mixer Cell

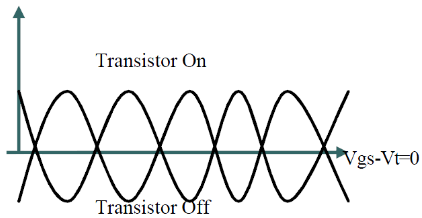

Fig. 3.3. Illustration of LO Switching

3.Current Sink : The current sink for the mixer is provided by the current mirror in the circuit. Generally, transistors in current sink remain in saturation region. While designing a current mirror, the length of transistor M_7 (in Figure 3.4) should be larger than the length of transistor M_8. This results in high output resistance that makes current (I_{ds}) less sensitive to the drain voltage (V_{ds}) of the transistor M_7. At the same time, increase in 'L' value effects the circuit performance by increasing the threshold voltage V_t which in turn results in less voltage head room for mixer. Therefore, the width 'W' also has to be increased for M_7 to keep the current constant.

4.Differential Output stage: The output of the mixer is taken at the terminals IF_+ and IF_-. Gilbert Mixer exploits symmetry to remove the unwanted RF & LO output signals from the IF by cancellation. The load resistance R_l is adjusted to increase the gain of the mixer.

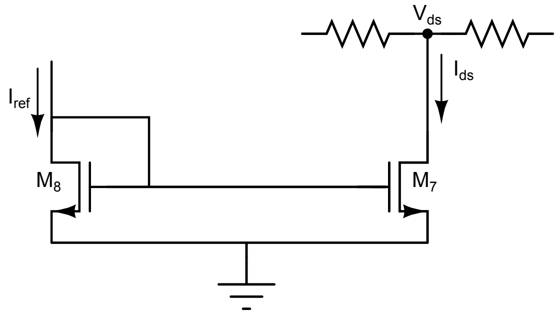

Fig. 3.4. Current Sink of Gilbert Mixer Cell

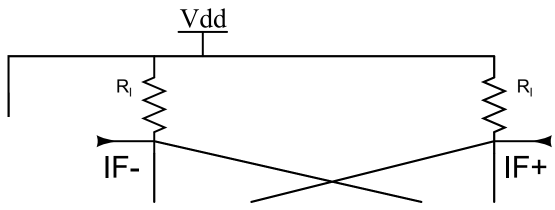

Fig. 3.5. Output Stage of Gilbert Mixer Cell

3.2 Mixer Operation

According to the Figure 2.2 ,The RF signal is applied to the transistors M_l and M_2 which performs a voltage to current conversion. M_l and M_2 provide +/- RF current. When the voltage at the terminal LO_- is large enough so that M_3 and M_6 are turned ON and voltage at the terminal LO_+ is small enough, so that M_4 and M_5 are turned OFF. This results in M_3 and M_6 acting as a closed switches so that

- M_6 is connected to right R_l and
- M_3 is connected to left R_l

as in typical differential amplifier configuration with the output taken at IF terminals.
In the next cycle, the voltage at the terminal LO_+ is large enough so that M_4 and M_5 are turned ON and voltage at the terminal LO_- is small enough, so that M_3 and M_6 are turned OFF. This results in M_4 and M_5 acting as a closed switches so that

- M_4 is connected to right R_l and
- M_5 is connected to left R_l

This also acts as differential amplifier configuration with the output taken at IF terminals which has same value of previous output but with opposite polarity. The two load resistors form a current to voltage transformation giving differential output IF signals. This IF output of a mixer is connected to low pass filter which filters the IF signal with zero frequency in our project. This signal is analyzed and calculated further to find the impedance of the human cell.

3.3 Design Approach

3.3.1 Design Constraints

According to our project requirement, the following are the constraints that are taken for the consideration before designing the mixer circuit.

- the supply voltage V_{DD} = 1.2 Volts.
- We need a down conversion mixer that mixes two signals of same frequency which results in one of the output signals with zero frequency. So $f_{RF} = f_{LO}$
- We are using 130 nm IHP microelectronics technology to design the mixer using Cadence Design Environment. According to this technology constraint, the single-finger structure width of the transistor cannot be more than 10μm.
- The minimum length as per IHP technology is 130nm, but a length of 500nm is chosen as threshold voltage varies for every transistor at the given basic 130nm length. At 500nm, it is observed that the threshold voltage remains constant for all transistors that are used for the mixer.
- As it is a CMOS Gilbert mixer, it can operate in a frequency range of 1MHz-10GHz according to our project specifications.
- For the proper functioning of the mixer, all the transistors should be in saturation region.

3.3.2 Design Analysis

Based on the above considerations, the following specification values are taken for the design

Parameter Name	Value
V_{DD}	1.2 V
V_t	250 mV
I_{ds}	16 μA
I_{ss}	32 μA
β_{eff}	6.33 mA/V^2

Table 3.1. Parameter Values of Mixer

In the above table, V_t is the threshold voltage and β_{eff} is trans conductance parameter of the transistor. The current I_{ss} refers to the current at the current sink. Current I_{ds} refers to the current along the gain stage transistors. The minimum current a human can feel depends on the current type (AC or DC) and frequency. A person can feel at least 1 mA (rms) of AC at 60 Hz, while at least 5 mA for DC. At around 10 mA, AC current passing through the arm of a 68 kg (150 lb) human can cause powerful muscle contractions; the victim is unable to voluntarily control muscles and cannot release an electrified object. This is known as the "let go threshold" and is a criterion for shock hazard in electrical regulations[Cad05]

By taking the above reference into consideration and to keep all the transistors in a saturation region, the possible current that can be used in the design is assumed in μA. By doing parametric analyses of transistors in current sink, gain stage, switch stage sequentially, the width of all transistors were calculated by assuming the length of all transistors to be 500 nm as discussed previously other than M_7 transistor in current sink of the circuit. The input voltage to the RF/ Gain stage and LO/ Switch stage are also calculated so as to keep the transistors in saturation region. There are many deadlocks and dependencies which have to be taken into consideration while designing the specifications for the transistors in order to satisfy the above design constraints. All the calculated values are changed based on the parametric analysis of transistors in Cadence Virtuoso. Finally, the Gilbert mixer schematic circuit is designed with Cadence Virtuoso and the device specifications are mentioned in the tables below.

Transistors	Width (W)	Length (L)
M_1	7μm	500 nm
M_2	7μm	500 nm
M_3	9μm	500 nm
M_4	9μm	500 nm
M_5	9μm	500 nm
M_6	9μm	500 nm
M_7	5.2μm	650 nm
M_8	2μm	500 nm
M_9	2μm	500 nm
M_{10}	10μm	500 nm

Table 3.2. Transistor Specifications of Gilbert Mixer

The biasing stage is added to the existing Gilbert circuit to provide appropriate RF signal such that it should not disturb the DC bias point of the schematic circuit of the mixer. The figure 3.6 shows the biasing stage of the Gilbert mixer cell in green border. The

Resistor	Value
R_s	33 Ω
R_d	4 KΩ
R_l	20 KΩ
R_{rf}	6 KΩ

Table 3.3. Resistor Values in Gilbert Mixer

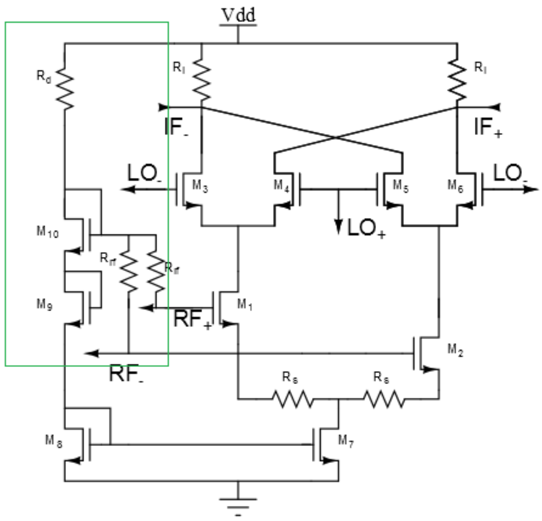

Fig. 3.6. Schematic model of Gilbert Mixer

Resistance R_{rf} is adjusted to transfer the exact voltage V_{ds} of the transistor M_{10} as an input RF signal to the RF terminals of gain stage. Proper biasing is needed to provide the effective isolation at the RF terminal which is the input stage of the Gilbert mixer. This biasing stage is added only for the test bench of the Gilbert mixer that is needed to analyze the characteristics of the Gilbert mixer which will be discussed in the next chapter.

3.4 Design Implementation

The above given schematic model of Gilbert mixer is designed and implemented in cadence tool with its corresponding test bench circuit. The test bench circuit is used to simulate the designed Gilbert mixer. It is also used for the characterization of mixer which will be discussed in next chapter. Please refer below the implemented schematic views of Gilbert mixer and test bench circuit.

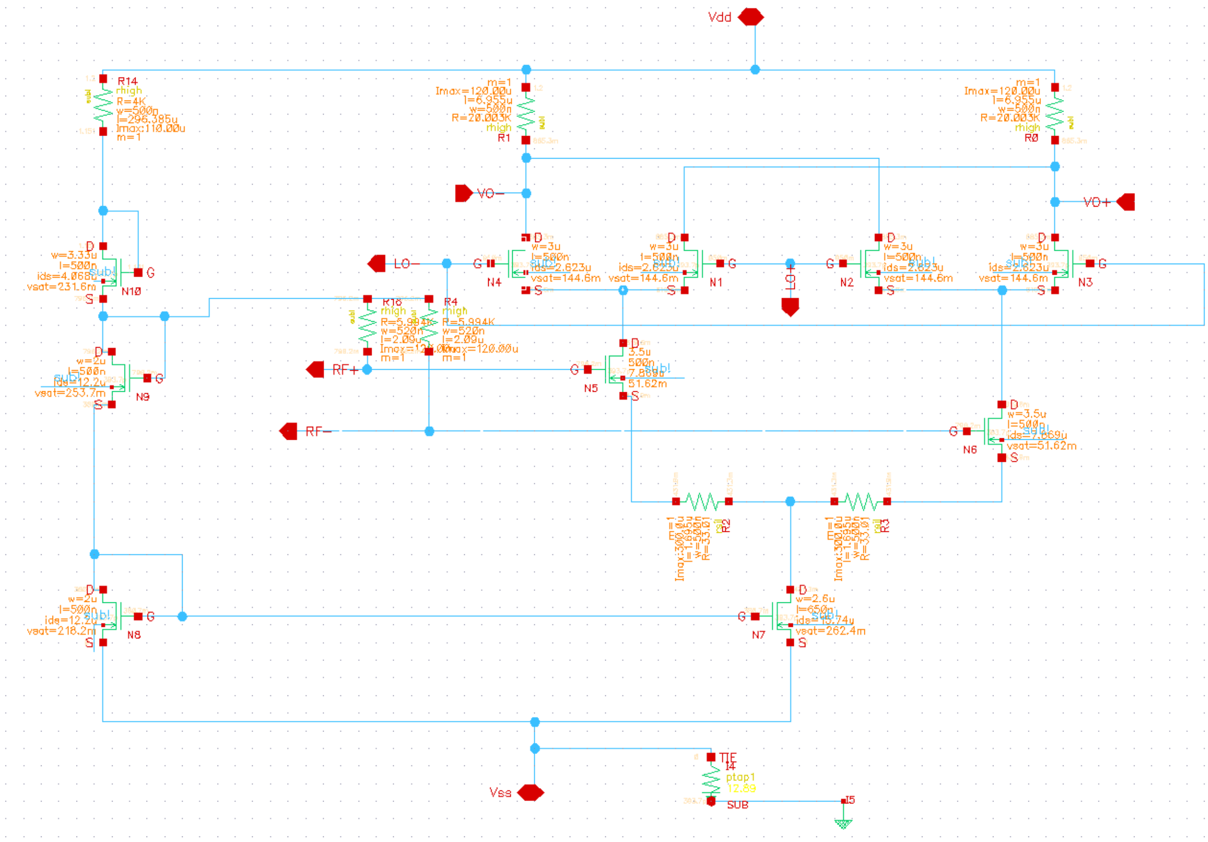

Fig. 3.7. Schematic View of Gilbert Mixer

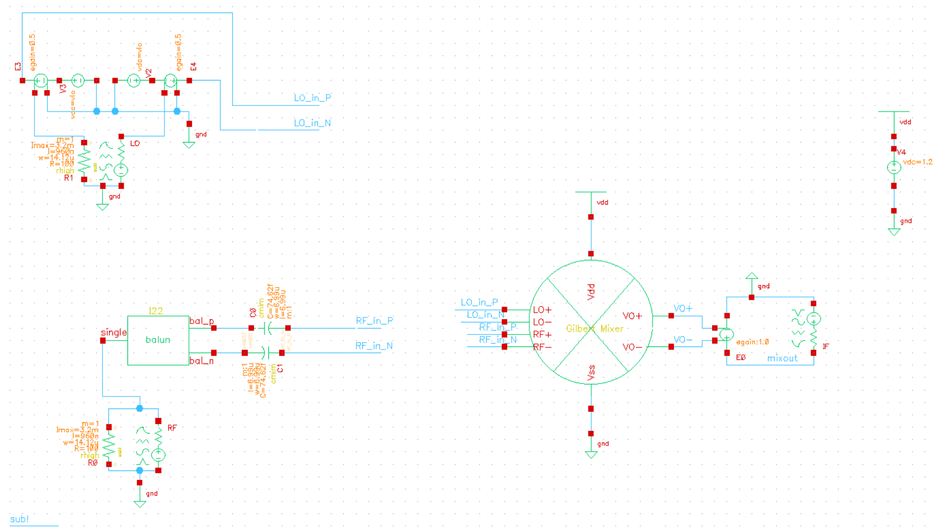

Fig. 3.8. Testbench View of Gilbert Mixer

The following are the components that are used in the test bench of mixer shown in above

figure:
Linear Voltage Controlled Voltage Source: Current through the voltage source is calculated and is defined to be positive if it flows from the positive terminal, through the source, to the negative terminal.
Balun: It is used to generate a differential signal from a single signal, in this case simply for simulation purposes.
Port: The port component is an independent resistive source tied between positive and negative terminals. It is equivalent to a voltage source in series with a resistor, where the reference resistance of the port is the value of the resistor. The port component is most useful as a stimulus in high-frequency circuits, it also has the following unique capabilities: it defines the ports of a circuit to the S-parameter analysis, it has an intrinsic noise source that lets the noise analysis directly compute the noise figure of the circuit. When you specify the voltage on a port, Spectre RF (discussed in next chapter) assumes that the port is properly terminated in its reference resistance. The specified voltage value is not the voltage on the internal voltage source, which is actually set to twice the value specified on the port. If you use a port source to drive an open circuit, the voltage (for DC, transient, AC, and PAC signals) is two times its specified value. However, you can alternatively specify the amplitude of the sine wave in the transient and PAC analyses as the power in dBm delivered by the port when terminated with the reference resistance. The following port convention is assumed:

- Port 1: RF, output of amplifier
- Port 2: LO, output of quadrature VCO
- Port 3: IF, mixer's output

The port source is a real source (with internal resistance) which defines a port and allows variation of the parameters required for the simulation. Since RF and LO are inputs of the mixer, they require the port source and a 50 Ω resistor to match the source's impedance (set by default to 50 Ω), so that the power at the input is the maximum power the source can provide. Magnitudes at the port sources are twice the power at a matched output. At the output IF we need to define a port but not to provide power. This can be achieved by connecting the port source at the output and setting the DC bias and AC magnitudes to zero. In this way, the port is simply terminated by 50 Ω by the port source. In order to avoid altering the bias point of the Gilbert Mixer, the port source can't be connected directly to the outputs. Therefore, we connect a voltage controlled voltage source (vcvs) to the IF output as a control voltage terminals, and the port source to the output terminals of the voltage controlled voltage source.

4 Characterization of Gilbert Mixer

The simulation of Gilbert mixer is done using Spectre RF. It adds a series of analyses that are particularly useful for **RF circuits** to the basic capabilities of the Spectre Circuit Simulator from Cadence Design Systems. It is also highly accurate and high speed analog simulator tool.

4.1 DC Simulation

This analysis shows whether all the transistors in schematic are operating in saturation region. It is used to determine the DC operating point of the mixer. It also gives the annotated information about node voltages in the circuit. With this analysis, each transistor in the circuit can be analyzed and all the parameters related to the transistor are known which is very helpful for further improvement of the design.

4.2 AC Simulation

In this analysis, RF and LO ports in the test bench are given with AC signals and the output IF port is analyzed which has a mixed signal of frequency range f_{LO}-f_{RF} , f_{LO}+f_{RF}. This analysis helps us to find whether the mixer circuit is giving required output in the above mentioned frequency range without many harmonic oscillations or noise.

But, to design a perfect mixer with proper functioning, we should also consider the figures of merit of mixer circuit which gives the characteristics of the mixer. To find these figures of merit, we need to undergo further analysis of the circuit using Spectre RF Simulator. They are:

4.3 Periodic Analysis

It includes periodic large and small-signal analyses in addition to Spectre simulation. This analysis consists of:

Periodic Steady-State Analysis(PSS): It is a large-signal analysis that directly computes the periodic steady-state response of a circuit. With PSS, simulation times are independent of the time constants of the circuit, so it can quickly compute the steady-state response of circuits with long time constants, such as high-Q filters and oscillators [Sys07]. It is required prior to any frequency analysis.

After completing a PSS analysis, the Spectre RF simulator can model frequency conversion effects by performing one or more of the periodic small-signal analyses such as:
Periodic AC Analysis (PAC): It analyses AC behavior based on linearization around the operating point obtained at PSS analysis.
Periodic S-Parameter Analysis, (PSP): It analyses Periodic S-Parameters of the circuit.
Periodic Transfer Function Analysis,(PXF): It analyses Periodic Transfer Function of the circuit.
Periodic Noise Analysis, (Pnoise): It analyses Periodic Noise of the circuit.
This periodic small-signal analyses is applied to periodically driven circuits that exhibit frequency conversion (example mixer).

Quasi-Periodic Analysis: It is to include harmonic effects and periodic distortion in the PSS and PAC analysis. They are referred as QPSS and QPAC.

4.4 Figures of Merit of Mixer

Figures of merit are often defined for particular materials or devices in order to determine their relative utility for an application. The following are the figures of merit of mixer which are to be characterized in this project using the above mentioned analysis in Spectre RF:

1. Power Consumption
2. RF to IF Conversion Gain
3. LO to RF and LO to IF Isolation
4. Input and Output Impedance Matching
5. Noise and Noise Figure
6. Linearity

4.5 Simulation Set up of the Mixer

For running the PSS simulation, we need to define the following parameters in the Test bench:

At the RF port source

- Resistance = 50 Ohms
- Port number = 1
- Source type = DC
- Enable the option display small signal parameter
- PAC Magnitude field = pacmag
- Frequency name 1 field = f_{rf}
- Frequency 1 field = f_{rf}
- Amplitude1 (dBm) = p_{rf}

At the LO port source

- Resistance = 50 Ohms
- Port number = 2
- Source type = sine
- Frequency name 1 = f_{lo}
- Frequency 1 = f_{lo}
- Amplitude1(dBm) = p_{lo}

At the IF port source

- Resistance = 50 Ohms
- Port number = 2
- Source type = DC

Values of Components in TestBench

- All LO port VCVS (Type: linear, Gain=0.5, gain =0.5)
- IF port VCVS (Type: linear, Gain=1, gain =1)
- Balun (Single input Impedance= 50 Ω, Balanced output
- Impedance= 50Ω, Insertion loss = 0db)

With these parameters, we are providing a signal at LO port in order to obtain switching between LO and RF. Since we are not giving a DC value for IF and RF, we get the default value (0V). With PAC magnitude, we apply a small signal at RF port to observe the IF/RF gain. This obtains the operating point and runs the small signal analysis.
Set flo at the frequency of interest. We considered 1GHz as flo in this simulation. Activate the PSS analysis option at ADE. Choose "Large" in the fundamental tones segment. Give the value of flo as the beat frequency. Choose the number of harmonics you want for the analysis. Take into account that the time step of the simulation must be smaller than the period of the highest frequency harmonic. If the time step is not appropriate, you will obtain a warning at the simulation output log file stating that trapezoidal signal ringing has been detected. This means the simulated signals are too fast for being correctly simulated with the specified simulation time step.
The first thing to notice is that the behavior of the circuit depends on the power applied at the LO port. Thus, we must determine what is the optimum LO power to obtain maximum gain and apply that power during the PAC. If the LO power is defined by the application or an existing LO generator, then use this power to set the value of p_{lo}, taking into consideration that the power at the port source must be twice the power delivered to the matched load. Beat frequency defines the stop time simulated during PSS.

4.6 Voltage Conversion Gain(VCG)

It is the ratio (in dB) between the IF signal and the RF signal or it is the ratio of the RMS voltages of the IF and RF signals. The power conversion gain is the ratio of the power delivered to the load and the available RF input power. When the mixer's input impedance and load impedance are both equal to the source impedance, the power and voltage conversion gains, in decibels, are the same. So, input and output equivalent resistances of the circuit must be taken into account to achieve a certain power transfer.

Conversion gain can be obtained using a small signal analysis, like PSS together with a PAC or a PXF analysis. But other gains such as VCG referred to RF frequency are typically obtained when simulating. [CD06]

4.6.1 Voltage Conversion Gain versus the LO Signal Power (swept PSS with PAC)

- RF Port Parameters in the Schematic :
  Resistance = 50Ω, Source Type = DC

- LO Port Parameters in the Schematic:
  Resistance = 50Ω, Source Type = sine (flo,flo,plo)

- IF Port Parameters in the Schematic:
  Resistance = 50Ω, Source Type = DC

- Design variables values in the affirma window should be:
  frf = 1 GHz, flo = 1.1 GHz,
  prf = -50 and plo = 10 both in dbm field,
  pacmag = 1 , not in dbm range

- In the affirma window, select Analysis -> Choose

- The Choose Analysis window shows up

  Select PSS for Analysis,
  Uncheck the Auto Calculate Box,
  Set fundamental tone –> flo flo 1GHz (press update from schematic button), look like: **flo flo 1G Large PORT2**,
  Beat Frequency = 1GHz, Output Harmonics = 10 ,
  Accuracy Default : Moderate, Sweep : variable (p_{lo}),
  Sweep Range : -10 to 20, Sweep Type : Linear,
  No of steps = 10 , Enable and apply

- Now at the top of choosing Analysis window
  Select PAC for Analysis,
  Frequency Sweep Range = 1GHz,

Sideband –> Max Sideband =2,
Enable and apply

- In the affirma window click on Simulation-> Netlist and Run to start the simulation, make sure that simulation completes without errors
- In the affirma window click on the Results-> Direct plot (main form)–> PSS
- The PSS results window appears
  Analysis Type : PAC,
  Function : Voltage, Select: net,
  Sweep : Variable, Signal Level : Peak,
  Modifier : dB20, Output Harmonics : -1,
  Select mixout node in schematics,
  You will see the plot as shown in Figure 4.1

The PAC analysis calculates the gain directly when the pacmag parameter is 1V. If this is not the case take the ratio of input and output.[Ras07]

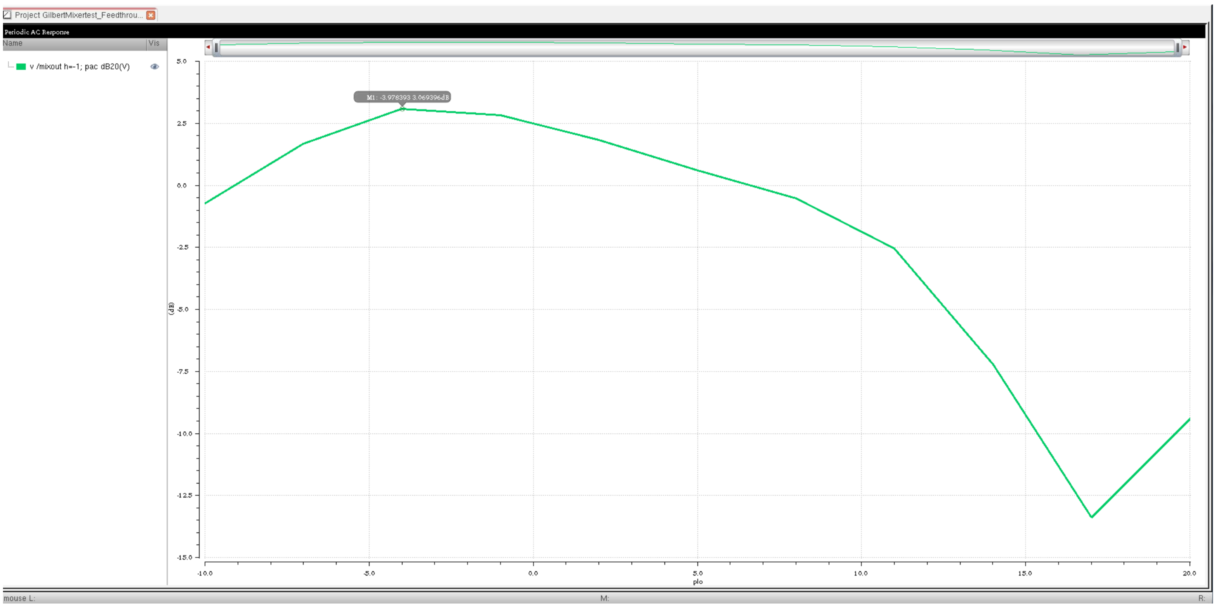

Fig. 4.1. VCG vs LO Signal Power

The plo for maximum gain is -4dBm in this case. We will use this value in the subsequent simulations.

4.6.2 Voltage Conversion Gain versus RF Frequency (PSS with swept PAC)

Test bench parameters are same as above part

- In Design variables, Change plo = -4
- Now at the top of choosing Analysis window
  Select PAC for Analysis
  Frequency Sweep Range –> 1GHz to 1.1GHz,
  Sideband : Max Sideband = 2,
  Enable and apply
- The Choose Analysis window shows up
  Select PSS for Analysis,
  Uncheck the Auto Calculate Box,
  Set fundamental tone –> flo flo 1GHz (press update from schematic button) , look like **flo flo 1G Large PORT2**
  Beat Frequency = 1G, Output Harmonics : 10 ,
  Accuracy Default : Moderate ,
  Switch off the sweep option,
  Enable and apply
- In the affirma window click on Simulation –> Netlist and Run to start the simulation, make sure that simulation completes without errors
- In the affirma window click on the Results –> Direct plot (main form) –> PSS
- The PSS results window appears.
  Analysis Type : PAC,
  Function : Voltage, Select : net Sweep : Sideband, Signal Level : Peak, Modifier : dB20 , Output Harmonics : -1 0 -10M ,
  Select mixout node in schematics ,
  You will see the plot as shown in Figure 4.2

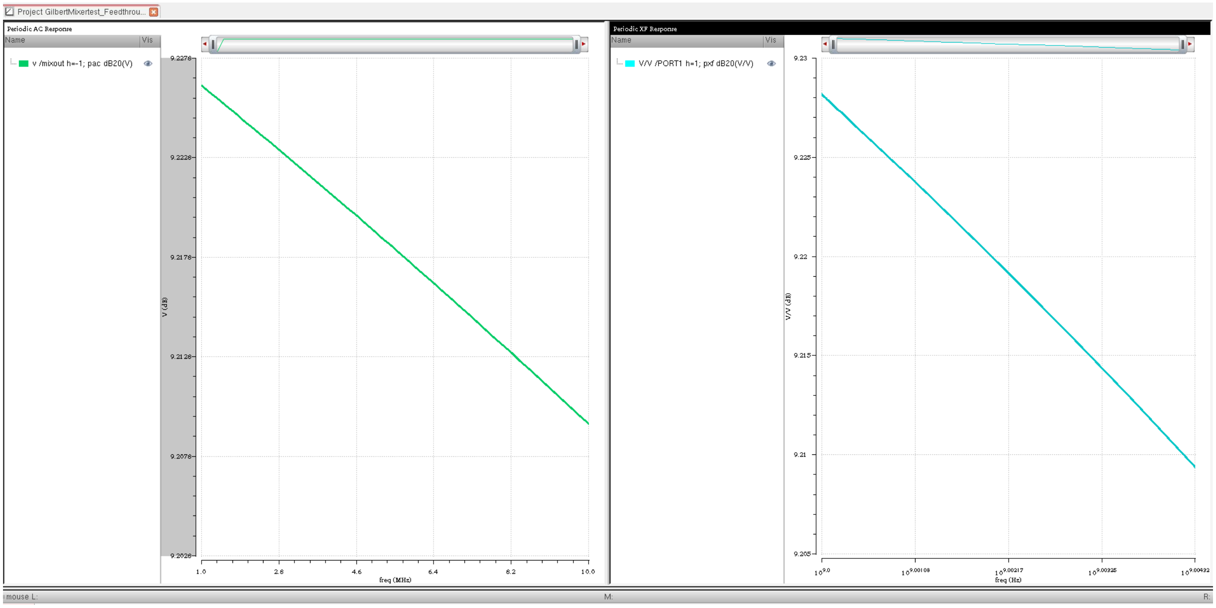

Fig. 4.2. VCG vs RF frequency using PAC and PXF

4.6.3 Voltage Conversion Gain versus RF Frequency (PSS with swept PXF)

Test Bench Parameters are same as above part

- In Design variables, Change plo = -4
- Now at the top of choosing Analysis window
  The Choose Analysis window shows up
  Select PSS for Analysis,
  Uncheck the Auto Calculate Box,
  Set fundamental tone –> (press update from schematic button) , it should look like
  flo flo 1G Large PORT2
  Beat Frequency = 1.0G,
  Output Harmonics = 10, Accuracy Default : Moderate ,
  Sweep option: off ,
  Enable and apply
- Now at the top of choosing Analysis window
  Select PXF for Analysis
  Frequency Range = 1KHz to 10MHz,
  Sideband –> Max Sideband =2,
  Sweep Type : automatic, Output : voltage ,

Positive output node : mixout (from schematic) ,
Negative output node : gnd (from schematic) ,
Enable and apply

- In the affirma window click on Simulation –> Netlist and Run to start the simulation, make sure that simulation completes without errors
- In the affirma window click on the Results–> Direct plot (main form) –> PSS
- The PSS results window appears
  Analysis Type : PXF ,
  Function : Voltage, Sweep : Sideband, Modifier : dB20 ,
  Output Harmonics : 1 1G -1.01G ,
  Select RF port in schematics,
  You will see the plot as shown in the figure 4.2

Consequently, we can state that the Gain of the mixer designed is
Power Gain (dB) = Voltage Gain (dB) = 9.3 dB
Generally, an active mixer like this should have a VCG greater than 0 dB. So, our mixer design is good in terms of power gain and Voltage Conversion Gain.

4.7 Port-to-Port Isolation

The isolation between the three ports of the mixer is important, especially at high operating frequencies of the mixer. It is also another important characteristic to measure in the mixer. The LO to RF isolation measures how much of the local oscillator signal appears at the RF port. Any LO leakage to the RF port can cause DC offsets in the output due to self-mixing, which can corrupt the output of a mixer. Also, LO-IF feed through must be limited to avoid the desensitization problem in the stage following the mixer.
The PAC and PXF analysis can be combined to produce the transfer function from different ports to each other. Here we will simulate the RF-LO, RF-IF and LO-IF feed through [Ras07].
Test bench is almost same as voltage conversion gain analysis except
RF port type: Resistance = 50Ω, Source Type: sine ,
Make sure plo = -4 in design variables

- Now at the top of choosing Analysis window
  The Choose Analysis window shows up
  Select PSS for Analysis

Uncheck the Auto Calculate Box,
Set fundamental tone: (press update from schematic button) , it looks like
flo flo 1G Large PORT2,
frf frf 1G Large PORT1
Beat Frequency = 1G,
Output Harmonics = 10, Accuracy Default: Moderate,
Switch off the sweep option,
Enable and apply

- Now at the top of choosing Analysis window
  Select PAC for Analysis
  Frequency Sweep Range = 1GHz to 1.1GHz,
  Sideband –> Max Sideband = 2, Sweep Type : Automatic ,
  Enable and apply

- Now at the top of choosing Analysis window Select PXF for Analysis
  Frequency Range: 1GHz to 1.03GHz,
  Sideband –> Max Sideband = 2, Sweep Type: automatic,
  Output : voltage ,
  Positive output node: mixout (from schematic),
  Negative output node: gnd (from schematic),
  Enable and apply

- In the affirma window click on Simulation–> Netlist and Run to start the simulation, make sure that simulation completes without errors

RF-to-LO Feedthrough:

- In the affirma window click on the Results–>Direct plot (main form)–> PSS
  The PSS results window appears
  Analysis Type: PAC, Function: Voltage,
  Select: net, Sweep: Sideband,
  Signal Level: Peak, Modifier: dB20,
  Output Harmonics: -1 0 to -10M (This represents the down converted RF signal at LO port),
  Select LO port; see the results in the Figure below.

RF-to-IF Feed through:

- Now just change Output Harmonics: 0 1G -1.1G (This represents the RF signal to IF port without down conversion),
- Select IF port, see the results in the Figure 4.3

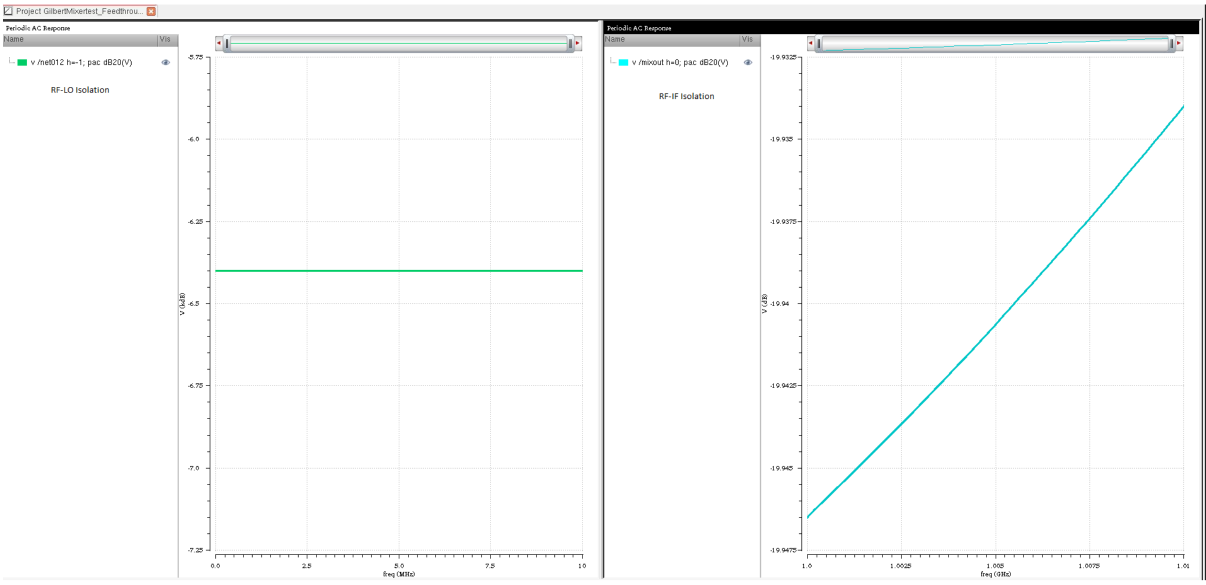

Fig. 4.3. RF-LO Isolation(Right) , RF-IF Isolation (Left)

With this observation from graphs for the Isolation, we can clearly understand that the mixer is providing good isolation among its ports and thus results in increase in the quality of the output signal.

LO-to-IF Feedthrough:

- In the affirma window click on the Results–> Direct plot (main form)–> PSS
- The PSS results window appears
  Analysis Type : PXF,
  Function : Voltage, Sweep : Sideband, Modifier : dB20,
  Output Sideband : 0 1G -1.03G,
  Select LO port in schematics, see the results in the Figure 4.4

LO-to-RF Feedthrough:

- Now Select RF port instead of LO port in schematics (Figure 4.5)

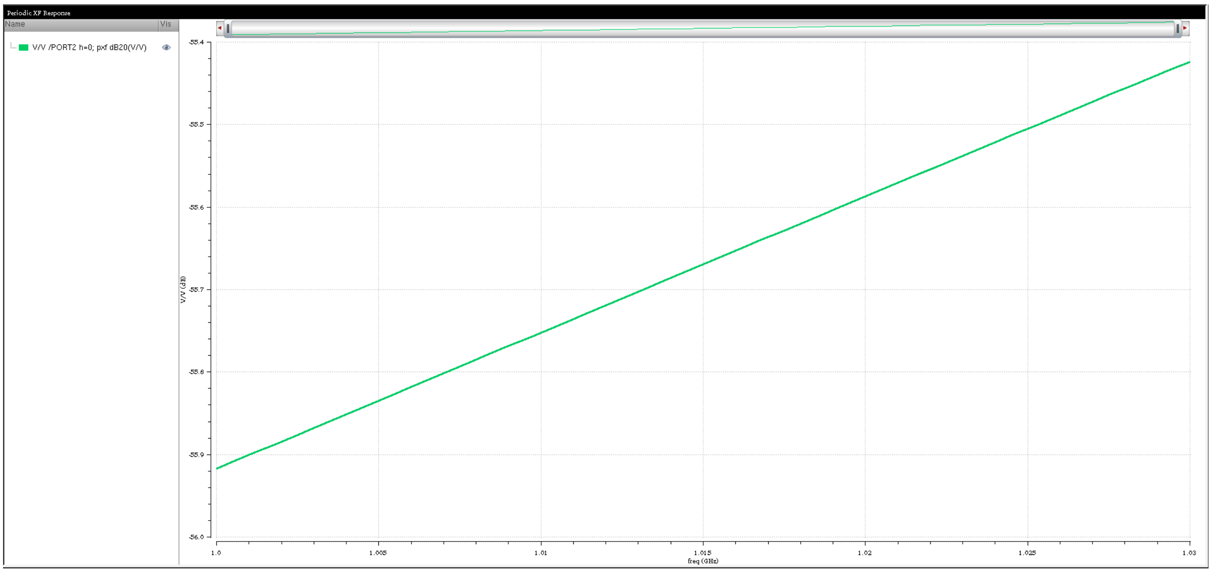

Fig. 4.4. LO-IF Isolation

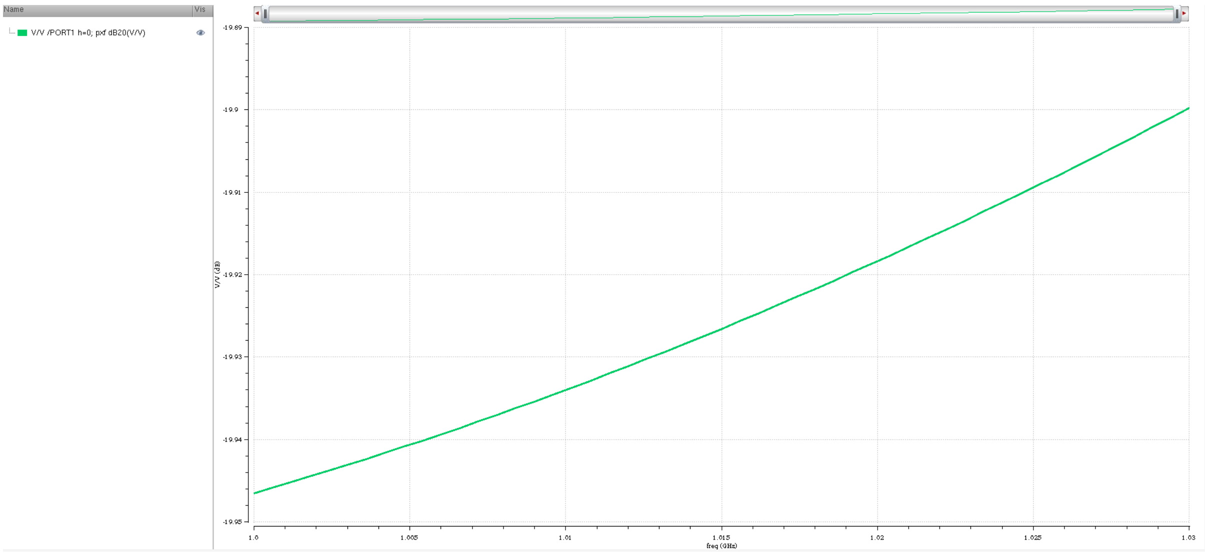

Fig. 4.5. LO-RF Isolation

4.8 Power Dissipation and Large Signal Power Conversion Gain using QPSS

Another interesting characteristic of a mixer resides on how much power it is able to transfer from the injected power at RF and LO to the desired output (main harmonics of IF).By using a QPSS analysis we have been able to identify this parameter in our circuit [CD06]

QPSS (Quasi Periodic Steady State Analysis) is an analysis that invokes a series of PSS-like analyses over all the input frequencies, their harmonics and the intermodulation products of the input frequencies. QPSS allows arbitrary signal inputs, including sum of sinusoids which are not periodic, so called quasi periodic extension of PSS. Similar to PAC (Periodic AC analysis) it calculates the responses of the circuits that exhibit the frequency translation like mixer, oscillator etc. Unlike PAC, PSS is not explicitly required before QPSS as it simulates the moderate and large signal behavior instead of small signal behavior [Ras07]

- Disable all other analysis
- RF Port Parameters in the Schematic
  Resistance = 50 Ω, Source Type = sine (frf,frf,prf)
- LO Port Parameters in the Schematic
  Resistance = 50 Ω, Source Type = sine (flo,flo,plo)
- IF Port Parameters in the Schematic
  Resistance = 50 Ω, Source Type = DC
- Verify that the Design variables values in the affirma window are frf = 1.01 GHz, prf = -30 , flo = 1GHz, plo = -4 , pacmag = 1
- In the affirma window, select Analysis –> Choose The Choose Analysis window shows up
  Select QPSS for Analysis
  Click –> update from schematic,
  You should see the lines below (change the harmonics manually to 5 and 3. your port numbers may be different)
  flo flo 1G large port2 5
  frf frf 1.01 moderate port1 3
  Accuracy: moderate
  Enable and apply
- In the affirma window click on Simulation–>Netlist and Run to start the simulation, make sure that simulation completes without errors
- In the affirma window click on the Results–>Direct plot (main form)–>QPSS
- The QPSS results window appears Analysis Type : qpss, Function : power
  Select –> instance with two terminal, Modifier : dB10
  Select V_{DD} source terminal in schematics
  You will see the plot as shown in Figure 4.6

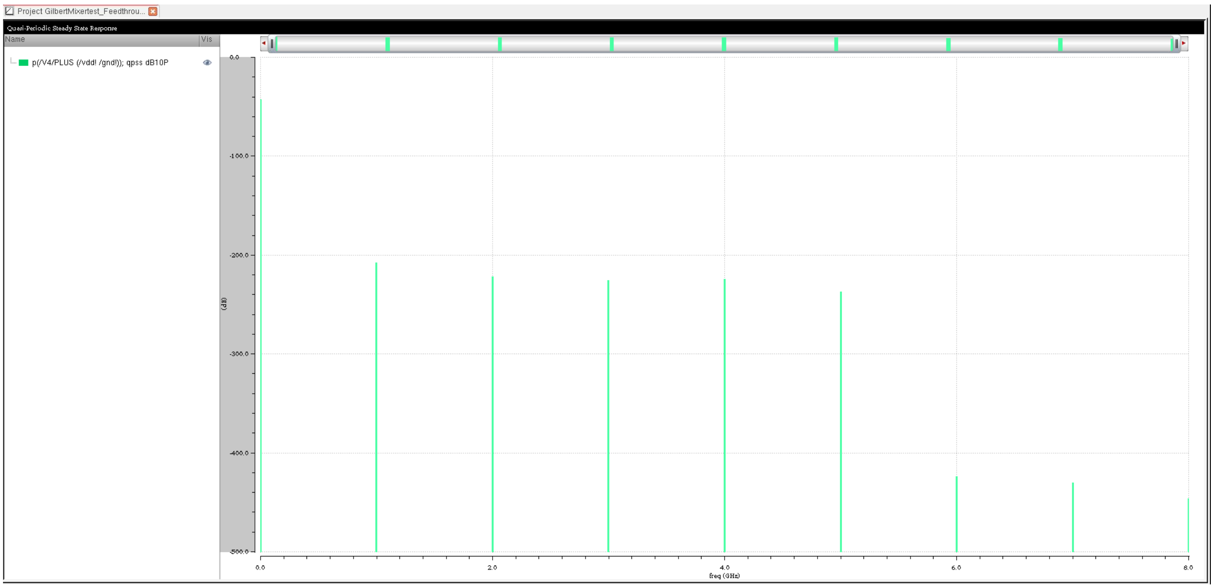

Fig. 4.6. QPSS Analysis for Large signal Voltage Conversion Gain

It is observed that QPSS as PSS provide the spectrum, not scalar values. So if we want to give a value to the power consumption, a good approach relies on the summation of the main fundamental harmonics presented in the foregoing figure. We can state, thus, that our circuit accomplishes a good behavior referring to power consumption [Ras07].

4.9 S-parameters (PSP)

Scattering parameters or S-parameters (the elements of a scattering matrix or S-matrix) describe the electrical behavior of linear electrical networks when undergoing various steady state stimuli by electrical signals .

Generally, circuit theory provides many methods for describing electronic networks. Those methods, however, best describe DC and low-frequency circuits. They fall short when the wavelengths of the signals of interest shrink to become comparable to the physical dimensions of the circuit of interest. To characterize high-frequency circuits, you can employ S-parameters (or scattering parameters) in place of the impedance or admittance parameters that describe low-frequency circuits. Each parameter is typically characterized by magnitude, decibel and phase. The expression in decibel is 20log(S_{ij}) because s-parameters are voltage ratios of the waves.

S11: input reflection coefficient at RF terminal,

S12: reverse transmission coefficient at terminated RF input,

S13: Power transfer from LO port to RF port,

S21: forward transmission coefficient at terminated output(Voltage Conversion Gain),
S22: output reflection coefficient at IF terminal,
S23: LO-IF Feed through,
S31: RF-LO Feed through,
S32: reverse transmission coefficient at terminated LO input,
S33: input reflection coefficient at LO terminal,

The following is the assumed order of the ports:
PORT 1 –> RF port
PORT 2 –> IF port
PORT 3 –> LO port

The advantage of S-parameters does not only lie in the complete description of the device performance at microwave frequencies but also the ability to convert to other parameters such as hybrid (H) or admittance (Y) parameters. A QPSS analysis has been required as well to obtain the S-parameters [Ras07].

- In Design variables,Change RF port : DC
- Verify the variable values in the affirma window flo = 1GHz (frf, prf, pcmag are meaningless in this analysis),plo= -4
- Disable previous QPSS analysis; Now at the top of choosing Analysis window
- The Choose Analysis window shows up Select PSS for Analysis
  Uncheck the Auto Calculate Box,
  Set fundamental tone : (press update from schematic button)
  flo flo 1GHz Large PORT2
  Beat Frequency = 1G, Output Harmonics = 10
  Accuracy Default : Moderate,
  Enable and apply
- The Choose Analysis window shows up Select PSP for Analysis
  Sweep type : absolute (If you choose relative , you can see results on scale of 1 GHZ and onward)
  Start-stop : 1K – 10M, Sweep Type : Automatic,
  Press Select port button and point to the RF, IF and LO ports in schematic, and enter the desired data
  1 PORT0 1 1G - 1.1G

2 PORT3 0 1K - 10M

3 PORT1 1 1G - 1.1G

Order of ports is important, in our case Port0 (RF) is numbered 1 and port 3 (IF) is numbered 2. These are considered as input and out ports for noise analysis respectively. Do Noise : Yes, Maximum sidebands = 10,
Enable and apply

- In the affirma window click on Simulation–>Netlist and Run to start the simulation, make sure that simulation completes without errors
- In the affirma window click on the Results–>Direct plot (main form)–> QPSS
- The PSS results window appears Analysis Type : psp, Function : SP or NF or NFdsb, Plot Type: Rectangular, Modifier : db20,
You will see the plot as shown in figure 4.7

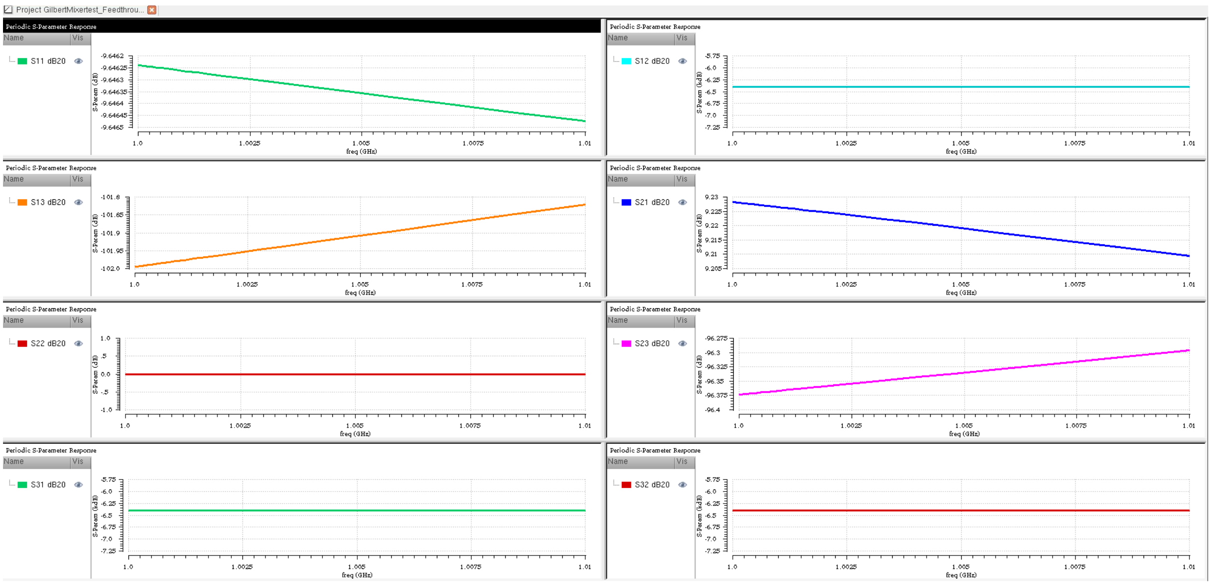

Fig. 4.7. S-Parameter Plots

We can also calculate noise figure in S-Parameter analysis. But, to calculate the output noise, we need to do the following Pnoise analysis.

4.10 Noise Figure (PSS and Pnoise)

Noise figure (NF) and noise factor (F) are measures of degradation of the signal-to-noise ratio (SNR), caused by components in a radio frequency (RF) signal chain. Noise factor is defined as the ratio of SNR at the input (RF port) to the SNR of the output (IF port). The lower values of Noise figure of a device indicating better performance of device. [Tec10] The noise figure is simply the noise factor expressed in decibels [Ras07].

$$NoiseFactor, F = \frac{SNR_{in}}{SNR_{out}} \tag{4.1}$$

$$NoiseFigure, NF = 10log(F) = 10log(\frac{SNR_{in}}{SNR_{out}}) = SNR_{in,dB} - SNR_{out,dB} \tag{4.2}$$

- In schematic RF port –> dc (prf, frf , pcmag are not needed)
  LO port : sine (flo,flo,plo)
- Verify the variable values in the affirma window flo = 1 GHz , plo= -4
- Now at the top of choosing Analysis window
- The Choose Analysis window shows up Select PSS for Analysis
  Uncheck the Auto Calculate Box,
  Set fundamental tone : **flo flo 1GHz** (press update from schematic button)
  Beat Frequency = 1G, Output Harmonics = 10 ,
  Accuracy Default : Moderate, Sweep : variable ,
  Variable name : plo, Sweep Range : -10dBm to 20dBm ,
  Sweep Type : Linear, No of steps = 10 ,
  Enable and apply
- The Choose Analysis window shows up Select Pnoise for Analysis
  Sweep type : absolute,
  Start-stop = 10M (noise is calculated at this frequency, the 1/f noise effect will not present, to see that make this frequency 10K or 1K) ,
  Maximum side band = 10 ,
  Output–>voltage–>select mixout and gnd ,
  Input source–> port–>select RF port ,

Reference sideband = -1 ,Noise Type : sources,
Enable and apply

- In the affirma window click on Simulation–>Netlist and Run to start the simulation, make sure that simulation completes without errors
- Now in the affirma window click on the Results–>Direct plot (main form)–> Pnoise
- The PSS results window appears Analysis Type : Pnoise
  Function : NF or NFdsb or Output Noise
  You will see the plot as shown in Figures 4.8, 4.9

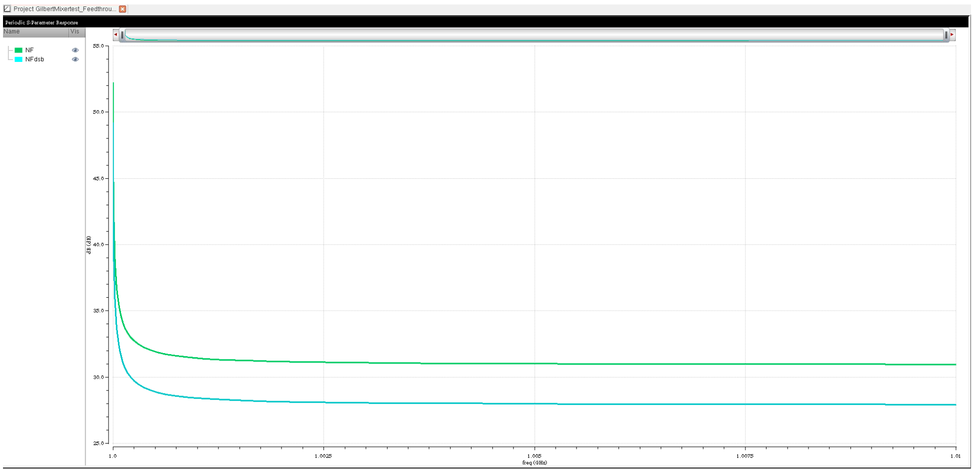

Fig. 4.8. Noise Figure and NF$_{dsb}$ Plots

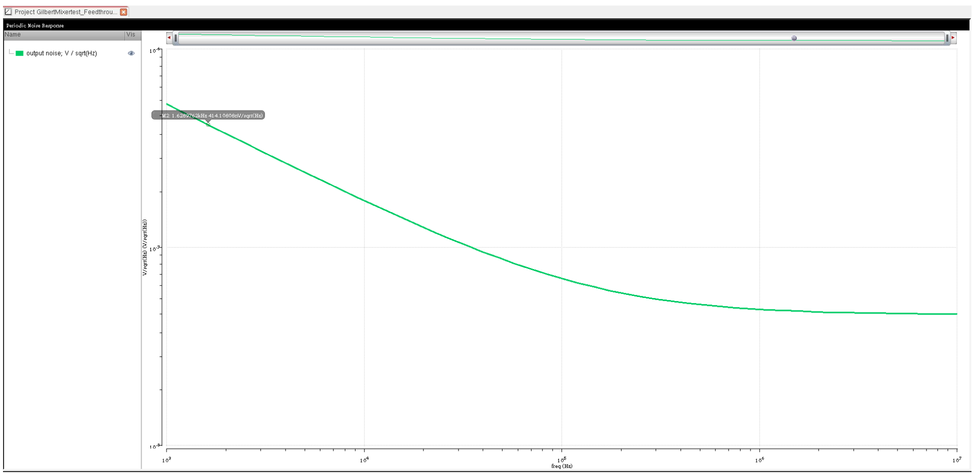

Fig. 4.9. Periodic Noise Response of Output Noise

We define output noise as the amount of undesired signal power found at the output signal frequency. If you select output as probe instead of voltage and point to IF port, you can get all types of NFs, noise correlation matrices and equivalent noise parameters.

4.11 Linearity of Mixer

The mixer linearity can be measured in two ways:

1DB Compression Point: In small signal conditions output power increases linearly with increase in the input signal power. When circuits shift toward large signal operation this relation is no longer linear. The 1dB compression point is a measure of this non-linearity. This is input power where the output of the fundamental crosses the line that represents the output power extrapolated from small signal conditions minus 1dB.

Third Order Intercept Point (IP3) : Due to the non linear behavior of mixers, two adjacent channels (or interferers) will generate intermodulation products at the output. These third order intermodulation products can corrupt a desired output signal if these fall within the desired channel. A mixer's ability to suppress third order intermodulation products is measured by its 3rd order intercept point which is defined as the input power when the 3rd order intermodulation products are equal to the linear products (the IF channel and the down converter interferer). This is also called as input 3rd order intercept point (IIP3). The magnitude of the 3rd order intermodulation products depends on the linearity of the mixer. The more linear the mixer, the better it is at suppressing the 3rd order intermodulation products [CT02]

The recommended approach to calculate the 1dB compression point and IIP3 is to apply large LO and one medium RF tone and perform the QPSS analysis. Then the second tone as a small tone close to the RF signal frequency is applied to perform afterwards the QPAC analysis. The power of the 2nd small RF signal tone, pacmag, has to be small enough that IMP1 (First order Intermodulation Products) and IMP3 (Third order Intermodulation Products) are in their asymptotic ranges [Ras07].

- Change/Check the LO Port Parameters in Schematic Window
  LO port: sine (flo,flo,plo),
  IF port: DC and 50 Ω,

- Change the RF Port Parameters in Schematic Window Source Type: Sine,
  Frequency name 1 field = frf, Frequency 1 field = frf ,
  Amplitude1(dBm)= prf ,
  Click on the Box: Display Signal Parameters,
  PAC Magnitude field (dB field): pacmagdb ,

- Verify the variable values in the affirma window flo = 1 GHz, frf =1.001 GHz, prf = -10 ,plo= -4, pacmagdb=prf

- In the affirma window, select Analysis–>Choose

- Disable previous analysis; The Choose Analysis window shows up Select qpss for Analysis
  In Fundamental Tones, the following lines should be visible (if its different please change them)
  flo flo 1G Large PORT2 5
  frf frf 1.001G modrate PORT1 4
  Accuracy Default : Moderate ,
  High light the Sweep Button ,
  Select Design Variable, small window appears, choose prf in it ,
  Sweep Range–>Choose the start : -70dBm and Stop: 10dBm ,
  Sweep Type : Linear and No of Steps =15 ,
  Enable Box in the bottom should be checked.

- Now at the top of choosing Analysis window Select QPAC for Analysis Sweep Type : absolute, Freq : 1.0011GHz ,
  Max Clock Order = 2, Enable and apply

- Click OK in the affirma window click on Simulation–>Netlist and Run to start the simulation

- In the affirma window, select Results–>Direct plot (main form)–> Main Form Analysis : QPSS Select Function : Compression Point ,
  Gain Compression : 1dB ,
  Extrapolation Point : -70dB ,
  1st Order Harmonic : -1 1 (1M) ,
  Select Port (Fixed R (Port))–>click IF PORT ,
  The resulting plot is shown in Figure 4.10

- In the affirma window, select Results–>Direct plot (main form)–>Main Form Analysis : QPAC , Function : IPN Curves ,
  Select Port (Fixed R (Port)) ,
  Highlight variable Sweep Prf ,
  Extrapolation Point = -60dB ,
  Highlight Input Referred IP3, Order : 3rd 3rd Order Harmonic : 1 -2 (900K) ,
  1st Order Harmonic : -1 0 (1.1M) ,
  Activate the Schematic Window and click on IF port to view the results as shown in Figure 4.11

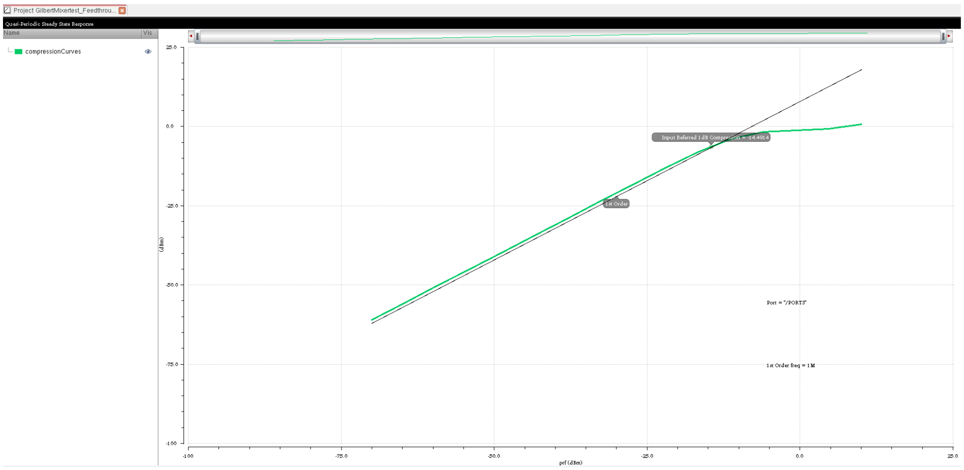

Fig. 4.10. 1 DB Compression Point Plot

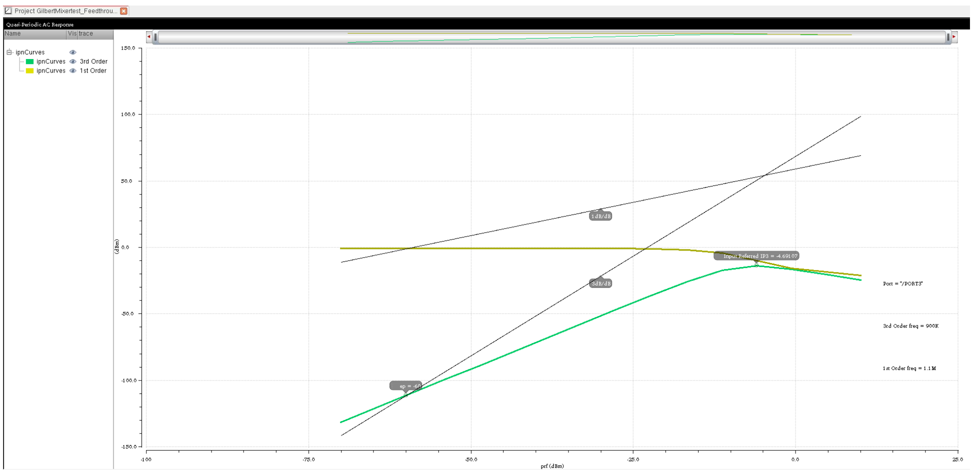

Fig. 4.11. IIP3 Plot using QPSS, QPAC

5 Layout and Post Layout Simulations

5.1 Layout of the Gilbert Mixer

The layout of the mixer was implemented in the CMOS 130 nm IHP technology process. The software used for layout was Virtuoso which was part of the Cadence Design Environment. While designing layout, we should be aware of DRC (Design Rule Check) to avoid errors. Following these rules guarantee proper transistor and interconnect fabrication despite various tolerances in each processing step. [Raz01] The main design rules are categorized as minimum: width, spacing, enclosure and extension. All of which can be checked for violation by running a DRC (Design Rule Check) in Virtuoso. In addition, proper design techniques should be followed to minimize effects such as feed through/ leakage, mismatches and noises.

Multi-finger Transistors: The layout is implemented using multi-finger transistors. Large transistors are usually broken up into multiple small transistors called “fingers”. This reduces both the S/D junction area and the gate resistance. However, too many parallel fingers can lead to increase in the capacitance associated with the perimeter of the source and drain regions. Generally, the width of each finger is chosen such that the resistance of the finger is less than the inverse of the transconductance associated with the finger [Raz01] The table below shows the division of each transistor into fingers.

Layout Symmetry: Designing a Layout in a symmetrical way is very important to reduce to size of the chip. It also reduces the usage of metal wires and contacts that in turn reduces the resistance in the circuit. A symmetric circuit suppresses the effect of common-mode noise and even-order non linearity minimizing any port-to-port feed through. The environment surrounding the devices must also be symmetrical to prevent mismatch between the devices because of the imperfection in fabrication process [Rog]

Transistors	Width (W)	Length (L)	Number of Fingers (N)
M_1	$7\mu m$	500 nm	2
M_2	$7\mu m$	500 nm	2
M_3	$9\mu m$	500 nm	3
M_4	$9\mu m$	500 nm	3
M_5	$9\mu m$	500 nm	3
M_6	$9\mu m$	500 nm	3
M_7	$5.2\mu m$	650 nm	2
M_8	$2\mu m$	500 nm	1
M_9	$2\mu m$	500 nm	1
M_{10}	$10\mu m$	500 nm	3

Table 5.1. Transistor Specifications of Gilbert Mixer with its finger details

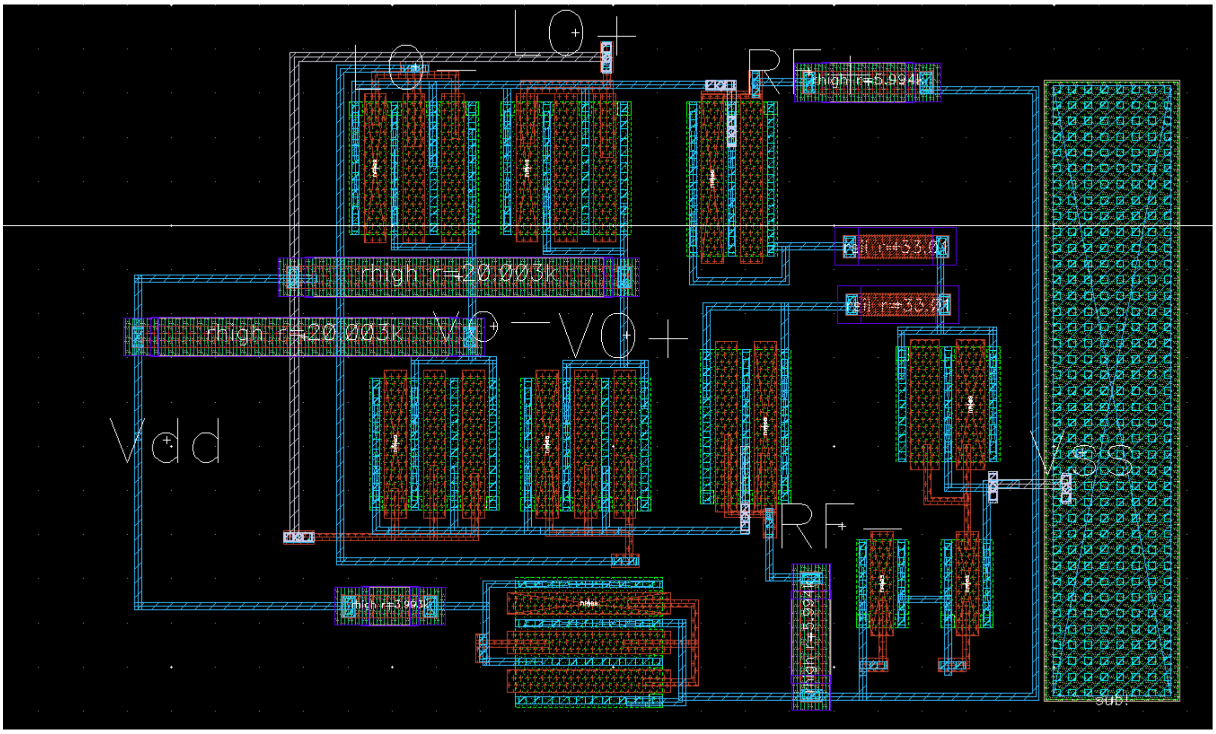

Fig. 5.1. Symmetric Layout View of Gilbert Mixer

5.2 Post Layout Simulations of the Gilbert Mixer

The following are the results of post layout simulation that are performed to find the characteristics of the Gilbert mixer.

In order to analyze the characteristics of the Gilbert mixer after layout, the simulations were carried out using the same procedure described in Chapter 4. After layout design, the schematic was changed to specify the use of multi-finger tran-

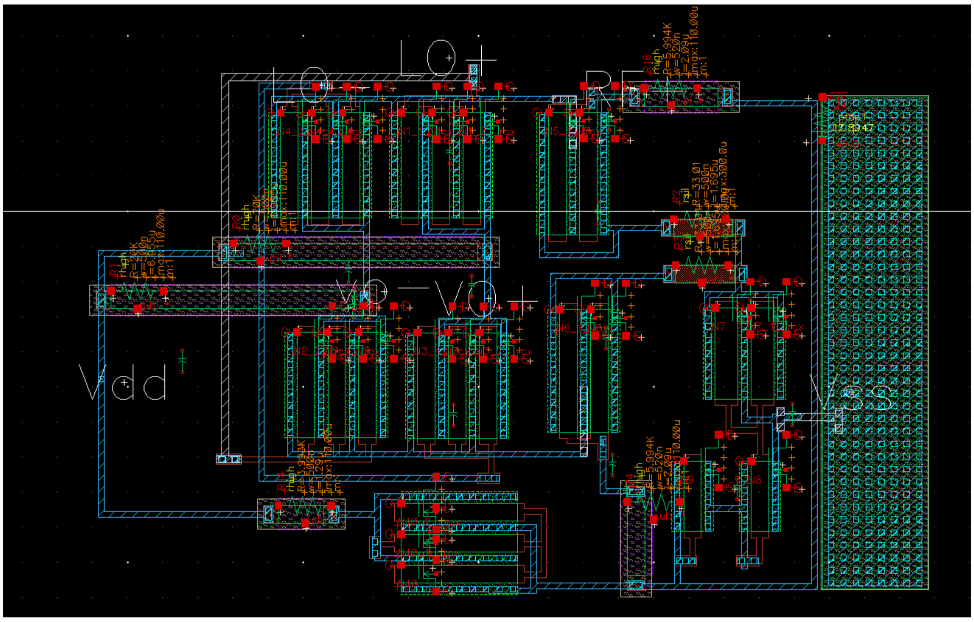

Fig. 5.2. Parasitic extraction View of layout

sistors. The post layout simulation results are presented in the following figures.

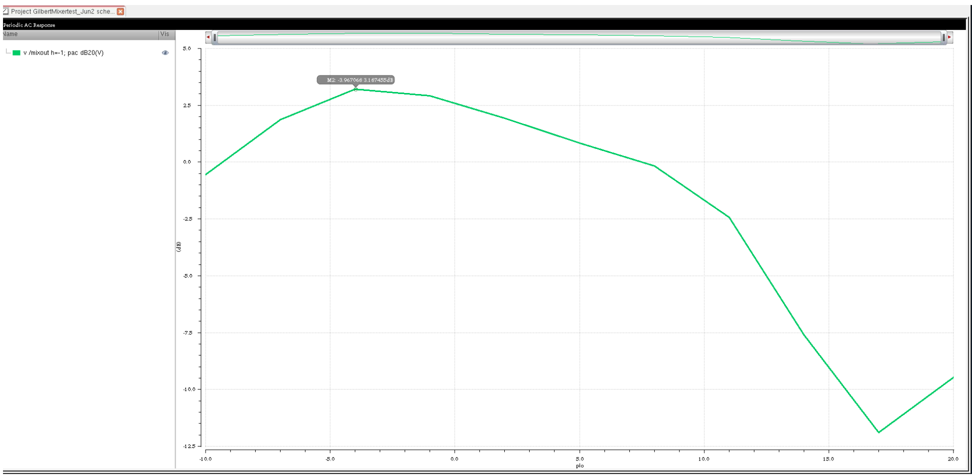

Fig. 5.3. VCG vs LO Signal Power

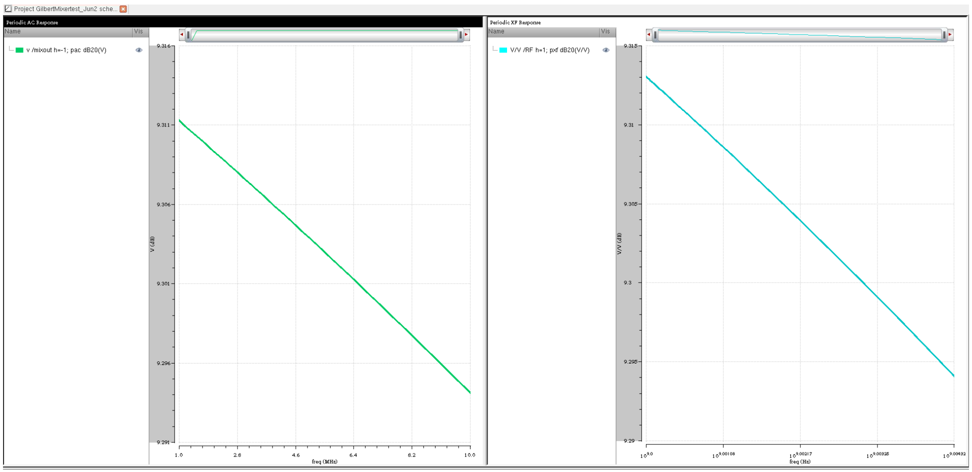

Fig. 5.4. VCG vs RF frequency using PAC and PXF

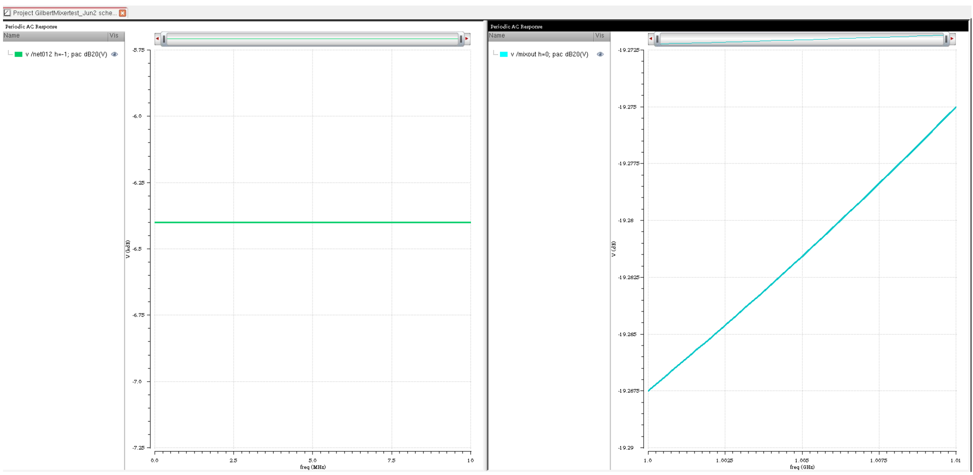

Fig. 5.5. RF-LO Isolation(Right) , RF-IF Isolation (Left)

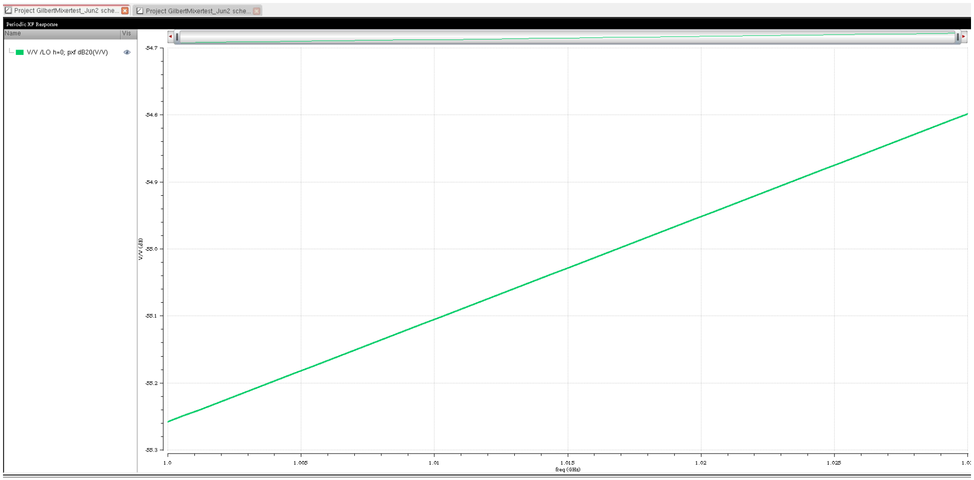

Fig. 5.6. LO-IF Isolation

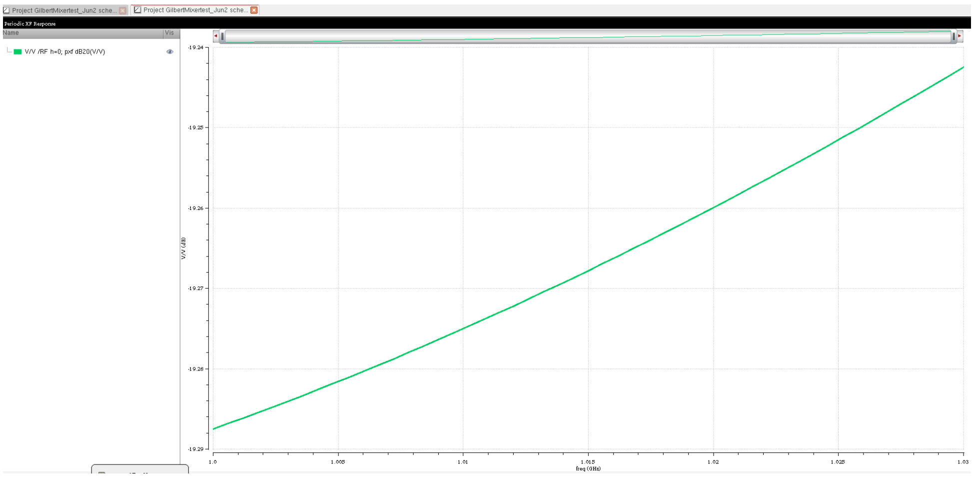

Fig. 5.7. LO-RF Isolation

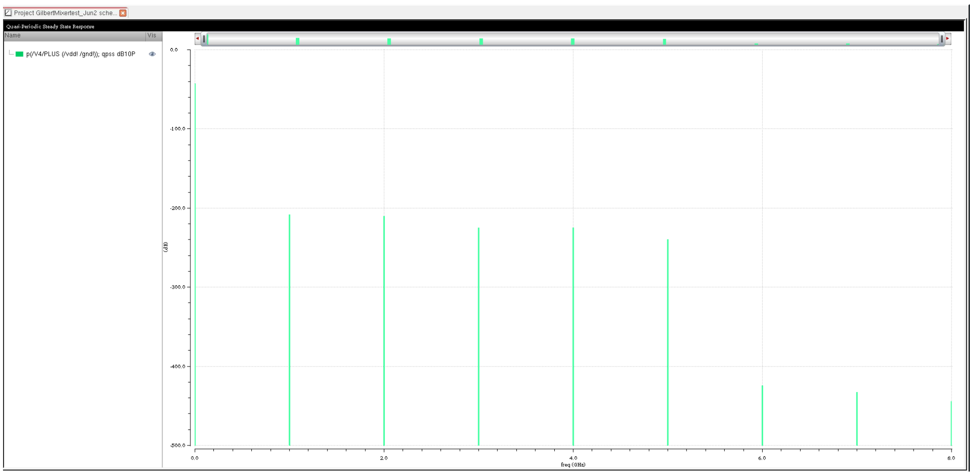

Fig. 5.8. QPSS Analysis for Large signal Voltage Conversion Gain

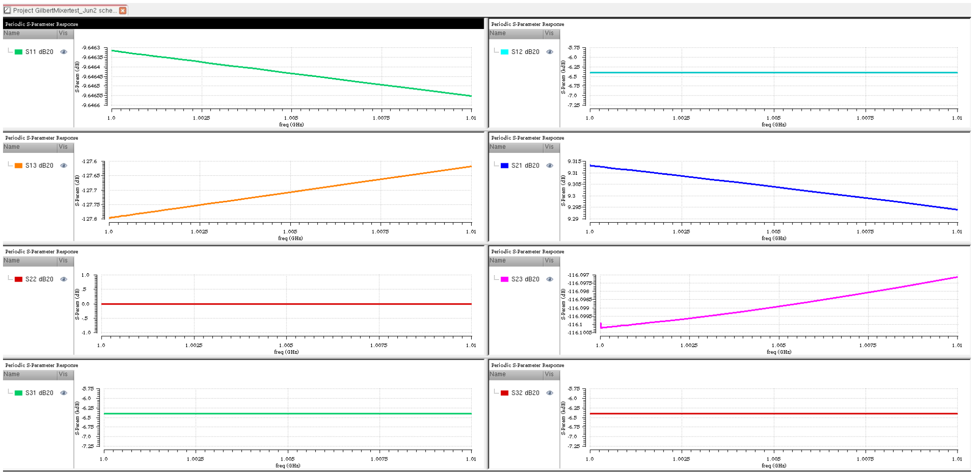

Fig. 5.9. S-Parameter Plots

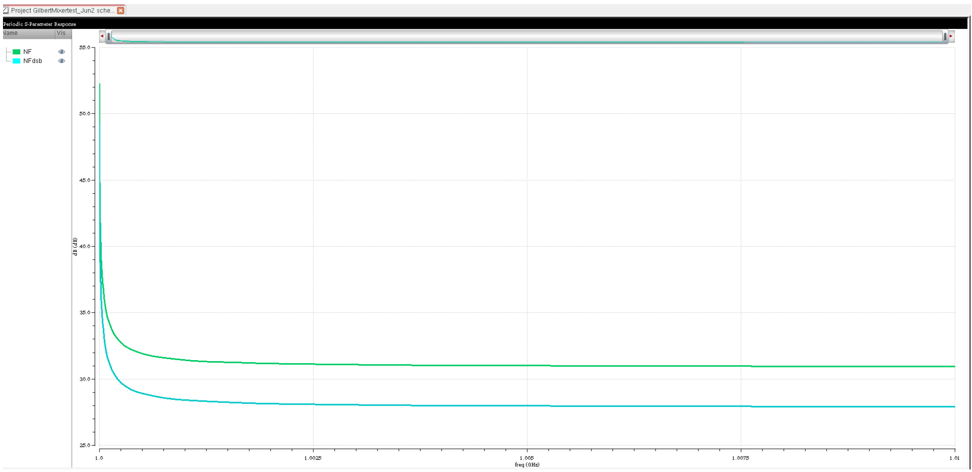

Fig. 5.10. Noise Figure and NF$_{dsb}$ Plots

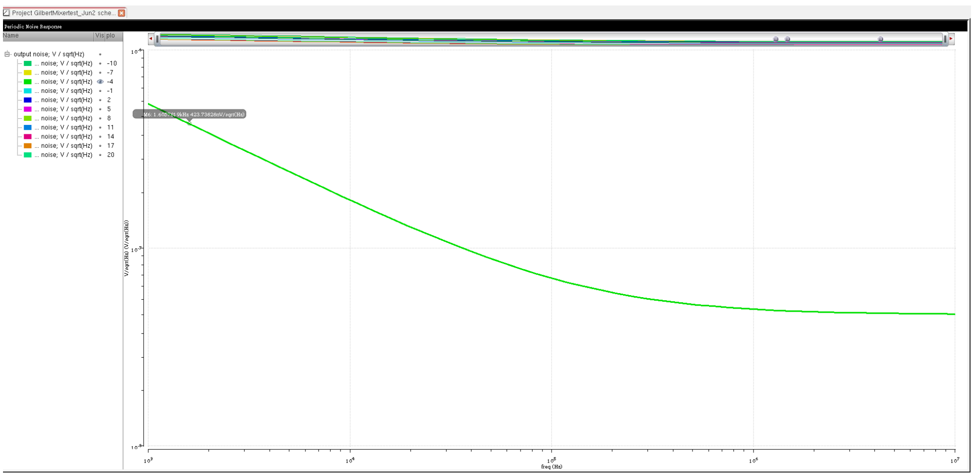

Fig. 5.11. Periodic Noise Response of Output Noise

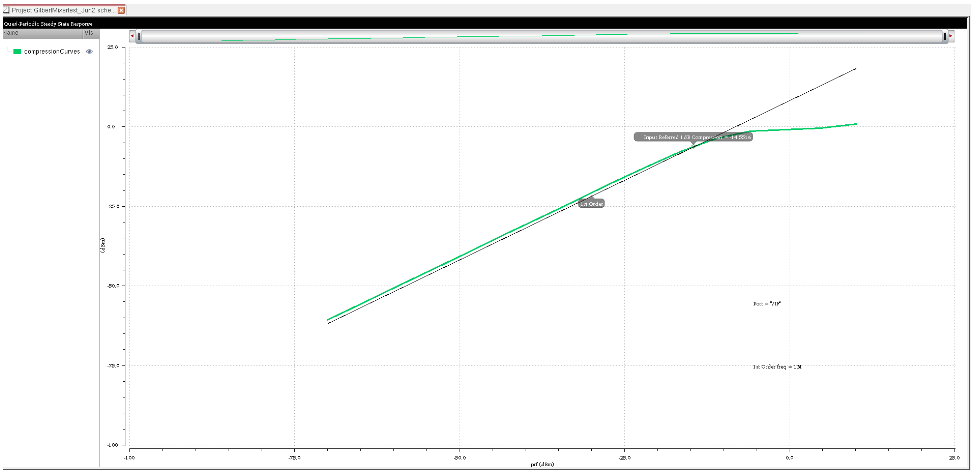

Fig. 5.12. 1 DB Compression Point Plot

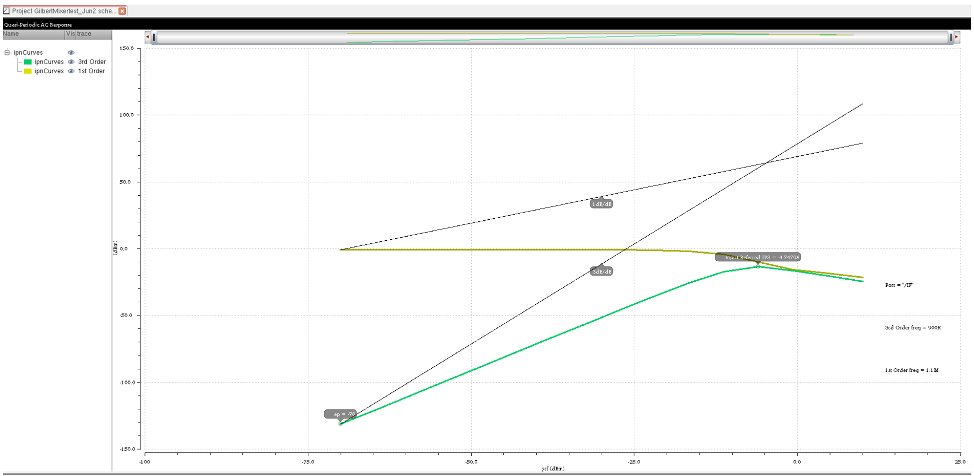

Fig. 5.13. IIP3 Plot using QPSS, QPAC

6 Conclusion

Finally, we found that there is no significant difference between Schematic and Layout simulations at 1GHz operating frequency. The Design of the mixer complies with the requirement of our project. Also, it is working as expected as it is simulated and all figures of merit were analyzed using Cadence Sprectre RF Simulator. The procedure to undergo different types of analyses while characterizing the Gilbert mixer is clearly explained such that this report can be used as a good reference to those who would like to resume the work in the project. It also gives a good understanding of Gilbert mixer to the beginners. Till now, there is no document that gives complete information from the scratch of the basics of mixer, design of the mixer, layout design and performing different simulations in a lucid way for characterizing the Gilbert mixer. Although, many existing documents and tutorials were taken as a reference in doing this project, lots of corrections that are needed in those documents were done in this report.

Regarding the applications of the design, as this mixer is going to be a part of the impedance measurement system of human cell, once the design of the chip is completed and submitted to fabrication, we can do further testing of the fabricated chip and check whether all simulations are in synchronous with the physical measurements of the integrated chip. Thus, the work done in this project is concluded.

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Declaration of Authenticity

I, Guru Kartheek Pedapalli, hereby declare under penalty of perjury, that this project is my own original work which has not been carried out in any other project. I have completed my work without unauthorized help from sources other than those mentioned in the bibliography.

Hamburg, 16th July 2014 Guru Kartheek Pedapalli