

Gilbert Cell Mixer Design in 65nm CMOS Technology

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Abstract—The article reports the design of Gilbert cell mixer using 65 nm CMOS technology. Cadence software is used to process the circuit design. The proposed down-conversion mixer uses a double balanced Gilbert cell to provide the required performance in gain conversion and isolation among ports. The supply voltage of 1.8V uses a new degenerating structure to improve linearity. The resonant frequency is around 1.9 GHz. The target in this work is minimizing size as well the power consumption (2.17mW). Acceptable linearity with 1dB compression point is -2.54 dBm. The third intercept point (IIP3) is optimized to 6 dBm. The conversion gains of LNA and Mixer is 10 dB when one IF port is terminated to 50Ω . The noise figure obtained at the output is 22dB.

Keywords-intercept point (IIP3); noise figure; gain; resonant frequency

I. INTRODUCTION

The major role of the down conversion mixers in the communication systems such as WIMAX, consists in translating the input radio frequency signal to an intermediate one (IF) to cover an area of around 30 to 50 kilometers [1], [2], see Fig. 1. There are several types of a mixer; we can list for example multiplier-based mixers, ring mixers, sub-sampling mixers and potentiometric mixers. In this work, we focused on the active mixer Gilbert's cell. Gilbert cell mixer is considered one the most important stage in RF architecture due to its high isolation among input and output ports and high conversion gain. The double balanced type is characterized by its fully differential structure and its high rejection at the RF and local oscillator (LO) ports.

In fact, the mixer should be linear, which means the third-order intercept point (IP3) should be greater than 0dBm. This linearity is proven by good isolation of all ports from each other in the device. To reduce power supply and maximize gain. CMOS 65 nm technology was chosen, in other hand, we should increase to minimize noise and the footprint of the circuit. The width was chosen to be maximum with respect to the current consumption [3], [4]. Unfortunately, the signal loss that is inherent in switching or multiplying by a sine wave gives us a mixer suffering from poor noise performance, mainly due to typical values of noise figure ranging 10 to 15 dB [4].

This paper is organized as follows. In the first part we realized theoretical study of double balanced mixer. For the second part, we focused on design procedure of the device

and its components. Finally, the third part discusses the simulation results obtained by cadence environment.

II. GILBERT CELL MIXER OPERATING MODE

A. Circuit Design of Proposed Mixed

The Gilbert cell mixer is composed mainly of three different stages. In the trans-conductance stage the RF signal is applied to the transistors M_2 and M_3 which convert the voltage to current, this transistor providing \pm RF current, see Fig. 2. The second stage is switching stage; this part is composed of two parts which complement each other [5].

The Transistors M_4 and M_7 form a multiplication function of the linear signal current RF from M_2 and M_3 with local oscillator signal applied across M_4 - M_7 . Finally load stage is defined by (R_d) transforming the current to the voltage at the output of the mixer giving differential output IF signal.

The switch between transistors M_4 and M_6 provides the inverted RF signal towards the load connected with M_4 . Same process happens for the load R_d connected with transistor M_7 receiving inverted RF signal due to the switch between the transistor M_7 and M_5 [6], [2].

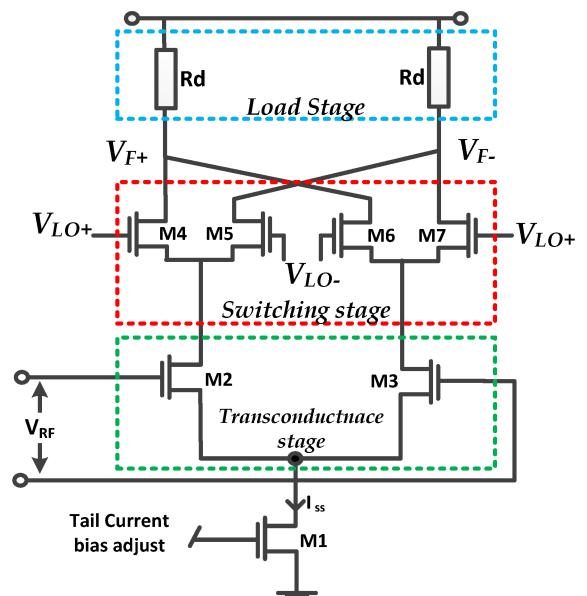


Figure 1. Double-balanced Gilbert-type mixer [5].

B. Third Harmonic Relative to the Fundamental

The quantification of the MOS differential behavior in function of the input differential voltage and is achieved by [7]:

$$V_{\text{out}}^+ = V_{dd} - R_d I_{D2} \quad \text{and} \quad V_{\text{out}}^- = V_{dd} - R_d I_{D3} \quad (1)$$

Then

$$V_{\text{out}} = R_d (I_{D2} - I_{D3}) \quad (2)$$

I_{D2} and I_{D3} are the drain currents of transistors M_2 and M_1 . So, we should find these currents in terms of V_{RF1} and V_{RF2} . The circuit is symmetric, and both transistors M_1 and M_2 are saturated. This saturation is achieved when the output g_o is as high as V_{dd} and less than $V_{in} - V_{th}$. Since the voltage at the node N is equal to $V_{RF1} - V_{GS2}$ and $V_{RF2} - V_{GS3}$, with respect to square law the device voltage are found

$$V_{GS2} = \sqrt{\frac{I_{D2}}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L}}} + V_{th} \quad (3)$$

Substituting Eq. (3) and (4) we found that:

$$V_{GS3} = \sqrt{\frac{I_{D3}}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L}}} + V_{th} \quad (4)$$

$$V_{RF1} - V_{RF2} = \sqrt{\frac{I_{D2}}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{I_{D3}}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L}}} \quad (5)$$

Our target is to calculate the differential output current $I_{D2} - I_{D3}$ expressed in the equation 2, and that to find the amplitude ratio of the third harmonic of the output signal relative to the fundamental.

$$I_{D2} - I_{D3} = \frac{(V_{RF1} - V_{RF2}) \mu_n C_{ox} W}{2L} \sqrt{\frac{\frac{4I_{SS}}{\mu_n C_{ox} W}}{L} - (V_{RF1} - V_{RF2})^2} \quad (6)$$

From the equation 6, we can see that $I_{D2} - I_{D3}$ is an odd function of $V_{RF1} - V_{RF2}$. Also we should to mention that I_{D1} and I_{D2} are even functions of their perspective gate source. ISS is equal to the double of the drain current of transistors M_1 leading to:

$$2I_{D1} = I_{SS} \Rightarrow I_{SS} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (7)$$

By definition trans-conductance of CMOS in saturation is expressed as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \quad (8)$$

As we can see from RF signal, V_m is too small, so much so, that it's ten times greater than $3V_m^3/32(V_{GS} - V_{th})^2$, allowing us to find the amplitude ratio of the output (V_{out})

and the third harmonic (A_{h3}) relative to the amplitude of the fundamental (A_F):

$$\frac{A_{h3}}{A_F} = \frac{3V_m^3}{32(V_{GS} - V_{th})^2} \quad (9)$$

C. Design Procedure

By using a technique based on the minimum noise to optimal size of the width, we can identify the width of the RF transistor as follows [8]:

$$W = W_{\text{opt}} = \frac{1}{3\omega L R_s C_{ox}} \quad (10)$$

here L and W presents the width of the active area of the transistor and minimum length of the used technology respectively. C_{ox} specifies the surface capacitor of the gate, R_s define the resistor of the matching which equals to 50 ohm, and The component ω define the pulsation, in the operating frequency (1.9GHz) we found that:

$$\omega = 2 \cdot \pi \cdot f = 11.932 \text{ rad/s} \quad (11)$$

and

$$C_{ox} = \frac{K_{ox} \epsilon_0}{t_{ox}} = 1.941 \times 10^{-5} \text{ F/m}^2 \quad (12)$$

here ϵ_0 define the absolute permittivity equal to $(8.463 \times 10^{-14} \text{ F/cm})$, K_{ox} is constant at approximately 3.9 and t_{ox} is a gate oxide of thickness 17.77 nm. An adjustment is made after the simulation to achieve the desired performance. To operate all transistors forming the mixer, we should operate at saturation region. One of the features of this region is large gain and also the current is less susceptible to change the voltage across the transistors. The Signal current in the nmos transistor working in saturation mode is [9]:

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (13)$$

Here, μ_n presents the electron mobility in the nmos transistor type [10]. The trans-conductance of a transistor is dependent on the ratio of the width, channel length and gate source voltage, with μ_n and C_{ox} representing the electron mobility and oxide capacitor respectively:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (14)$$

The condition for saturation is $V_{DS} = V_{GS} - V_T$ and $V_{GS} > V_T$.

D. Calculation of R_d and R_s

To drive the mixer a current sink of $I_{SS} = 0.6 \text{ mA}$ was chosen at the node N, therefore each branch of the mixer receives 0.3 mA. To preserve good marge, the Resistor R_s was chosen such that 0.1V drop cross resistor. To prohibit the compression at the IF port, a voltage of 1.8 V is selected, and then the R_d resistor is calculated as follows [9]:

$$R_{\text{deg}} = \frac{0.1V}{0.333mA} = 300\Omega \quad (15)$$

$$R_d = \frac{V_{DD} - V_D}{0.333mA} = \frac{1.8V - 0.6V}{0.333mA} = 400\Omega$$

The values of different components constituting the mixer are summarized in the Table I.

E. RF Stage Design

Gain at this level is proportional to the trans-conductance of the RF pairs [9]. Then, the value of the gm gives us the opportunity to find the width of the transistor

$$W_{2,3} = \frac{g_m^2 L}{2\mu_n C_{ox} I_{DS}} = 4.367\mu m \quad (16)$$

The overdrive voltage $V_{gs} - V_t$ is about 300 mV, then V_g become

$$V_g = V_s + V_t + 300mV = 0.5 + 0.7 + 0.3 = 1.5V \quad (17)$$

F. Desing of LO Stage

For the switching, the gate source voltage of the LO stage should be greater than threshold voltage, and also the gate width should be large. Assuming V_t is equal about 0.7 V then we can choose $V_{GS} = 0.8$ or 0.9 V. Width can be express as:

$$W = \frac{LI_{DS}}{K(V_{GS} - V_T)^2} = 2.712\mu m \quad (18)$$

The differential conversion gain is defined as the deference between the input and output powers and hence it equals approximately 13 dB. Here parameter k depends on transistor width and channel length, so the width of the gate voltage is approximately 2.6V

III. SIMULATION RESULTS

A. DC Analysis and Spectrum Responses

DC simulation is performed to find an operating point of the mixer. Using this method we can show that all transistors work in linear region [11]. Fig. 3 shows transistors operating in linear region producing a current in response to the gates sources overdrive voltage. DC simulation, provides us the possibility to measure the power consumption of the mixer;

in our case, it is 1.07mV, with $V_{dd} = 1.8V$. As we can see from the graph the output resistance increased instead when using a length of 65nm.

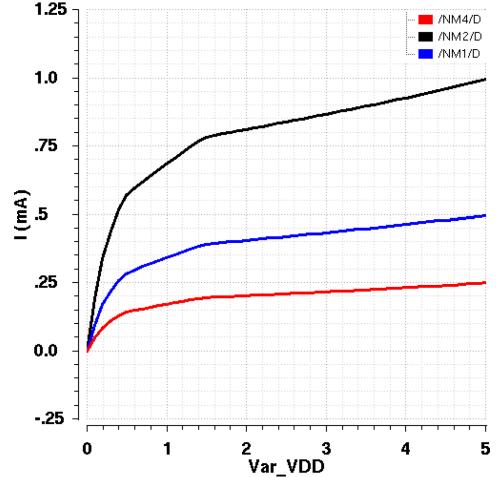


Figure 2. Drain current of transistors.

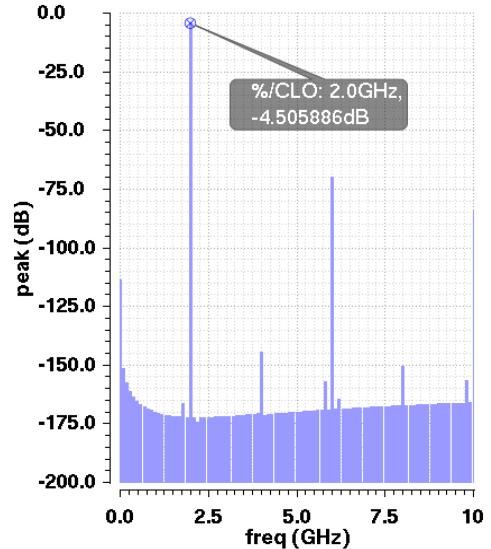


Figure 3. LO signal located at 2 GHz.

TABLE I. COMPARISON MIXER CHARACTERISTICS

Technology CMOS (μm)	frequency (GHz)	Noise Figure (dB)	IIP3 (dBm)	CG (dB)	Supply voltage (V)	DC power (mW)	1 dB compression point (dBm)	Ref.
0.18	2.4	21.7	4.6	5.3	1	N/A	-7.4	[1] [7]
0.065	1.9	4.12	11.6	8.75	1.8	2.17	-13	[6]
0.180	1.56	7.35	-4.34	6	1.8	3.4	-26	[8]
0.5	1.9	9.07	2.17	3.35	2.5	10	-8.2	[12]
0.8	1.9	7.8	-6	0.5	1.8	4.3	-15	[13]

Fig. 4 shows the frequency spectrum at 1.9 GHz, as we can see, there is also another harmonic that is due to non-linearity of the circuit. This simulation is used to find the transient response of the circuit when the radio frequency signal and local oscillator signal.

The LO power that leads to the largest IF frequency is about -4.50 dB and the operating frequency of the component is about 2 GHz. Fig. 5 shows the voltage gain and the power gain of the mixer. Fig. 6 and 7 shows the frequency spectrum of the output signal and the time varying

input signals of the located oscillator, respectively. The intermediate frequency for down word mixer is located at 0 with values equal to -43dB. The difference between signal level at the RF frequency and the signal level at the IF frequency defines the gain of the device. The differential conversion gain is defined as the deference between the input and the output power hence equaling to about 10dB.

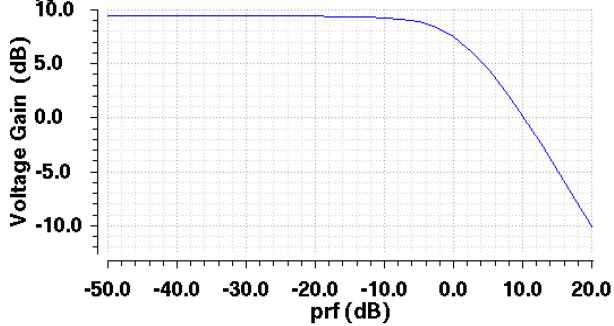


Figure 4. Power and voltage gains.

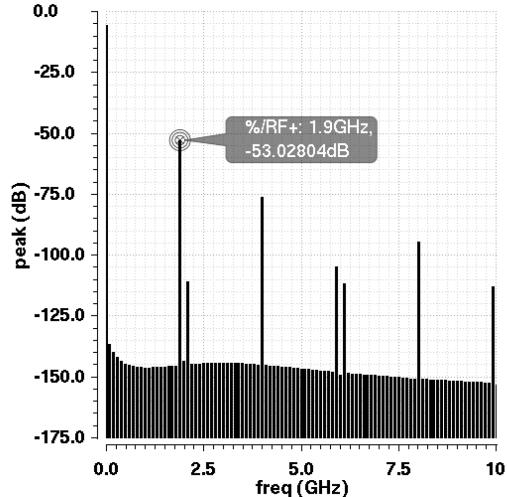


Figure 5. Spectrum of RF signal located at 1.9 GHz.

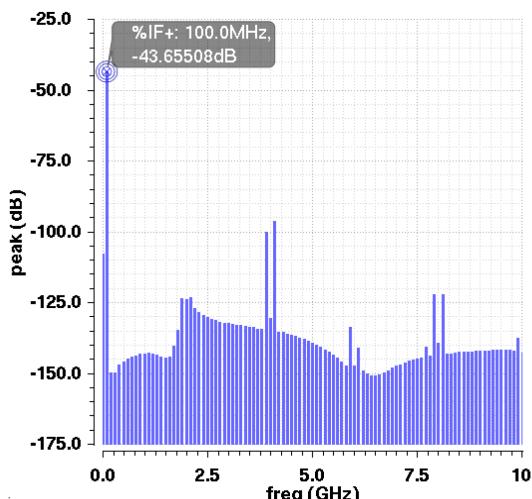


Figure 6. Frequency spectrum of output signal.

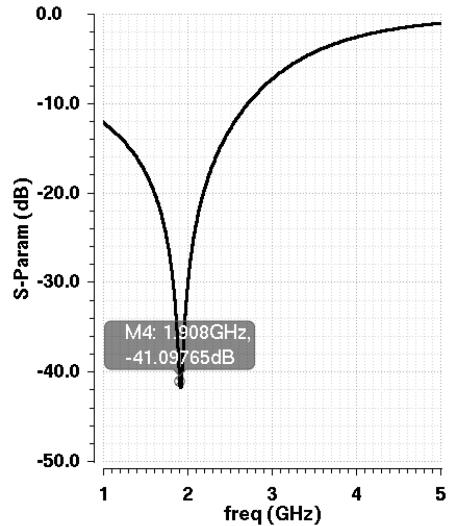


Figure 7. Simulated return loss.

B. Return LOSS and Noise Figure

Frequency response features are defined by the ratio of L_L/R_L and R_L/C_p [14]. However the Return loss at 1.9 GHz is plotted in the Fig. 9. S11 is about -40dB at desired frequency. The results prove that the input is perfectly matched. In the case of the mixer, we defined the noise figure as the total SNR at radio frequency divided by SNR at IF frequency. The Noise figure specifies the performance of the mixer [4], see Fig. 8. Pnoise analysis is used, and it expects the used of DC source to sweep all frequencies. Here, The Pnoise Improving the noise figure of the mixer is difficult because of the cyclostationary nature of the sources. LO stay because Pnoise uses this frequency as a reference for down-conversion. The device doesn't show a good noise figure. Usually, the noise figure should be minimal, yet with the mixer design, it is quite difficult. Because conserving good linearity of the circuit with small noise figure is not easy. We kept the latter at around 20dB to improve the linearity.

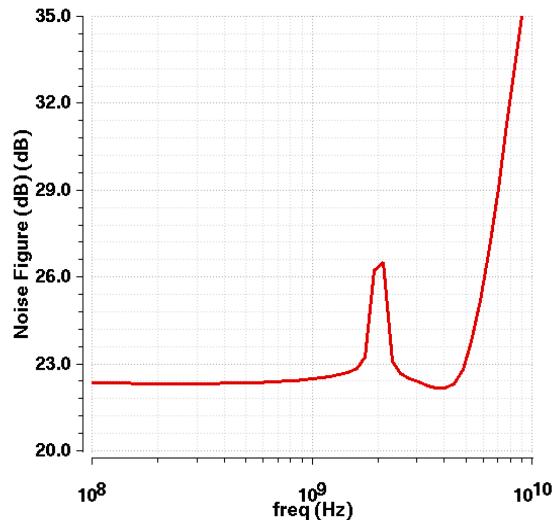


Figure 8. Simulated noise figure.

C. Linearity

Linearity is characterized by describing an operational region in which the output signal changes proportionally to the input signal [15]. In active Gilbert's cell mixer, linearity is related mainly to radio frequency stage, switched stage and load stage. As described previously the RF source is defined by RF transistors. In fact, the transducer is the most important factor influencing mixer performance such as gain, linearity noise figure and in the end, the third intercept point IIP3 [4].

To improve linearity, there are several techniques used to reduce the noise, like for example the inductance degeneration, which is usually used because there is no thermal noise generated by this component, which influence the noise figure (KF). Resistor, is also used as source degeneration and that to minimize the size of the circuit. In the case of the R degeneration, we can see from the equation (19) that the increase of R_s induces reduction in the gain of circuit, which conflicts with the evaluation of the circuit parameter [6], [3].

$$G_v = \frac{g_m}{1 + g_m R_s} \quad (19)$$

The use of R_L degeneration component can resolve this constraint [16]. $V_{GS} = -UR$, then when the Resistor R increases, the voltage V_{GS} will also rise, leading to a high third intercept point. The equivalent trans-conductance of the circuit is described by Eq. (20). Also, the inductance L has very small value, therefore, no influence of this component on trans-conductance, hence $G_v = -G_m R_d$.

$$G_m = \frac{g_m}{1 + L\omega g_m} \quad (20)$$

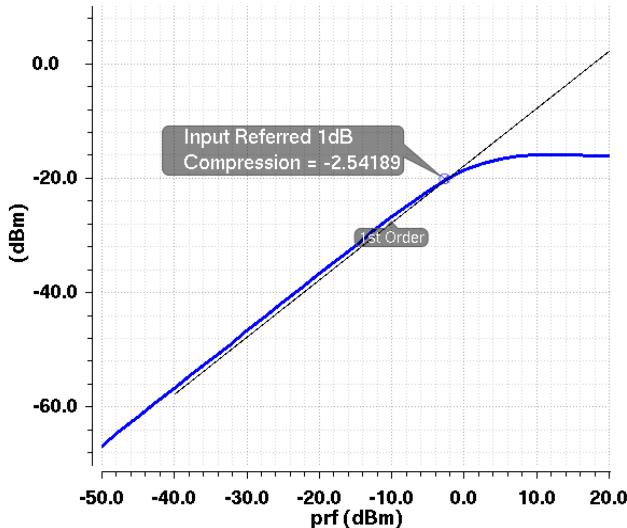


Figure 9. 1-dB compression point

Like any electronic device with non-linear active components, the mixer has an output power curve based on the entry and presenting a saturation zone. The linear operation of the circuit is defined by the 1-dB compression point. The strong input powers induce saturation at the

output power influencing the mixer. As shown in Fig. 9, is defined by the point of the power for which the gap between output power and its linear extrapolation reaches 1dB [6]. The third intercept point in this work (6 dBm) is less the one published in the article (11dBm), see Fig. 10.

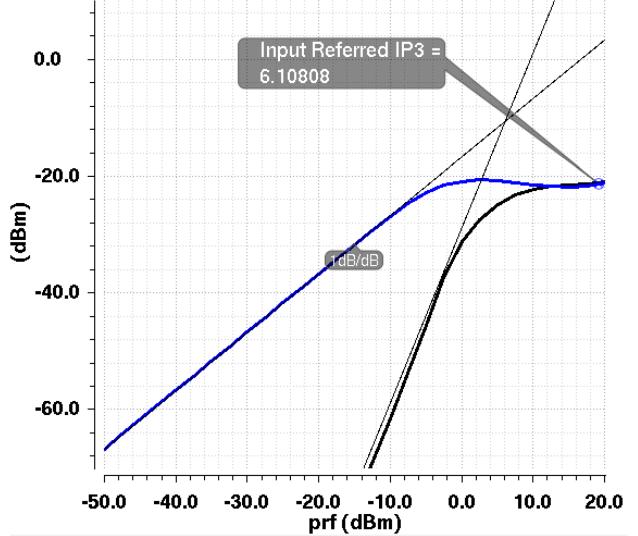


Figure 10. Third order interception point (IIP3).

IV. CONCLUSION

These papers discuss the double balanced mixer using 65 nm CMOS technology. The most important parameters characterizing the gilbert cell mixer was performed by simulation. The circuit shows good trade between IIP3, and the conversion gain, and the other parameters. We tried to have good noise figure, but the use of degeneration resistor and load resistor in addition to the geometry of the transistor induced a very high noise.

REFERENCES

- [1] Bao-Lin Wei, Yu-Jie Dai, "Analysis and design of a 1.0-V CMOS mixer based on variable load technique," *Microelectronics Journal*, 43 (2012) 1003–1009.
- [2] Ro-Min Weng, Shu-Wei Liu, "A 1.5 V Low Noise Figure Mixer for 3.5GHz WiMAX Systems," *IEEE*, 2010.
- [3] O. Mitrea, C. Popa, A. M.Manolescu, M. Glesner, "A LINEARIZATION TECHNIQUE FOR RADIO FREQUENCY CMOS GILBERT - TYPE MIXERS," *ICECS*, 2003 IEEE.
- [4] Khalid Faitah, Raja Mahmou, "High linearity, low power RF mixer design in 65 nm CMOS technology," 2014.
- [5] David Cordova, Sergio Bampi, Eric Fabris, "A CMOS Down-Conversion Mixer with High IIP2 and IIP3 for Multi-Band and Multiple Standards," *ACM*, September 01 - 05 2014.
- [6] Khalid Faitah, Raja Mahmou, "Design of 1.9 GHz Gilbert-Cell Down-Conversion Mixer With good linearity in 0.18 μ m CMOS Technology," *AMSE J Model Meas ContrGen Phys Electr Appl*, pp. 85(1-2), 2012.
- [7] L. T.H, "The Design of CMOS Radio Frequency Integrated Circuits," Cambridge University Press 1998.
- [8] Dengjun Lai, Yingmei Chen, Xiaodong Wang , Xuehui Chen, "A CMOS Single-Differential LNA and current bleeding CMOS mixer for GPS Receivers," 2010 IEEE.

- [9] Kumar Munusamy and Zubaida Yusoff, "A Highly Linear CMOS Down Conversion Double Balanced Mixer," ICSE 2006 Proc. 2006, Kuala Lumpur, Malaysia.
- [10] "BSIM3v3.3 Manual," UC Berkeley, Copyright © 2005.
- [11] M. Pifferia, M. Borgarinoa, R. Codeluppia, F. Alimentib, "High linearity CMOS mixer for domotic 5GHz WLAN sliding-IF receivers," Microelectronics Journal 37 (2006) 1012–1017.
- [12] Habib Kilicaslan, Hong-Sun Kim, and Mohammed Ismail, Fellow, IEEE, "A 1.9 GNx CMOS RF Down-conversion Mixer," 1997 IEEE
- [13] P. J. Sullivan, B. A. Xavier, D. Costa and W. H. Ku, "A Low Voltage Evaluation of a 1.9 GHz Silicon MOSFET GILBERT Cell Down-Conversion Mixer," 1996 IEEE.
- [14] Raheleh Hedayati, Sanaz Haddadian, Hooman Nabovati, "A 0.18 μ m CMOS High Linearity Flat Conversion Gain Down conversion mixer for UWB Receiver," IEEE, 2008.
- [15] Delong Ful, Lu Huangl, Hongliang Du, Haiquan Yuanl, "A 0.18pm CMOS High Linearity Flat Conversion Gain Down-conversion Mixer for UWB Receiver," IEEE 2008.
- [16] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill International Edition, 2001, p. 20.