Analog Integrated Circuits

# Titolo serio

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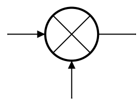
DATA

# Contents



# 1 Introduction

An analog multiplier, also known as mixer, is a circuit that performs the product between two signals. As we will see, this feature can be exploited to convert informations from a certain frequency band to another by means of the intrinsic non-linear behaviour of this net. Supposing to have two sinusoidal signals and to

$$x_1(t) = A_1 \cos(\omega_1 t + \varphi_1)$$
$$x_2(t) = A_2 \cos(\omega_2 t + \varphi_2)$$

and the ideal mixer shown in figure one has that the out coming signal $z(t)$ is given by:

$$\begin{aligned} y(t) &= x_1(t) \cdot x_2(t) \\ &= A_1 A_2 \cos(\omega_1 t + \varphi_1) \cos(\omega_2 t + \varphi_2) \\ &= \frac{A_1 A_2}{2} \{\cos[(\omega_1 - \omega_2)t + \varphi_1 - \varphi_2] + \cos[(\omega_1 + \omega_2)t + \varphi_1 + \varphi_2]\} \\ &= A \cos(\omega_{LF} t + \varphi_{LF}) + A \cos(\omega_{HF} t + \varphi_{HF}) \end{aligned}$$

where

$$\begin{aligned} \omega_{LF} &= |\omega_1 - \omega_2| \\ \omega_{HF} &= |\omega_1 + \omega_2| \\ \varphi_{LF} &= \varphi_1 - \varphi_2 \\ \varphi_{HF} &= \varphi_1 + \varphi_2 \end{aligned}$$

Therefore, it comes that two signals with different frequency allocations are obtained at the output port: the former at $\omega_{LF} < \omega_1, \omega_2$ will be the down-converted component whereas the latter with $\omega_{HF} > \omega_1, \omega_2$ will be the up-converted one. Moreover, it is possible to select only one of these two signals by properly filtering out the unwanted part. Overall one can read the process as a modulation of an input signal by means of a carrier. Since the mixer is a bidirectional three-port, one can distinguish:

- The high frequency signal, RF. In case of down-conversion this is one input of the circuit, vice-versa it is the output (after filtering).

- The intermediate frequency signal, IF. In case of up-conversion this is one input of the circuit, vice-versa it is the output (after filtering).

- The local oscillator, LO. This is the carrier and it is always an input with known frequency.

Based on the above, it turns out that to mix-up two signals a non-linear device is needed, since the input components are at different frequency with respect to the output and a non-linear relation between voltages and currents appears. In general, mixing can be carried out by time-varying systems that can be implemented using:

**passive devices** typically switches (diodes and transistors). In this case the mixing process introduces a *loss* since the output power is always less than the input one.

**active devices** amplifying devices are used in active region providing then possibility of *gain*.[1] They are more power consuming and less noisy than passive mixers.

Another way to classify mixers is the following:

**Single balanced mixers** One or both input signals can pass to output, but it is not possible to suppress both of them,

**Double balanced mixers** Thanks to symmetry in the net both the input and the LO are rejected from the output port. They have show better isolation between ports than SBM.

To understand why a transistors can be used, let's consider the non-linear quadratic model for a nMOSFET, supposing to drive that by injecting a two tone signal $v_{GS}(t) = v_{RF}(t) + v_{LO}(t)$ in the gate (down-conversion configuration). One has:

$$
\begin{aligned}
i_D(t) &= k(v_{GS}(t) - V_{th})^2 \\
&= k(v_{RF}(t) + v_{LO}(t) - V_{th})^2 \\
&= k[v_{RF}^2(t) + v_{LO}^2(t) + 2v_{RF}(t)v_{LO}(t) - 2(v_{RF}(t) + v_{LO}(t))V_{th} + V_{th}^2)]
\end{aligned}
$$

Supposing now $v_{RF} << v_{LO}$:

$$
\begin{aligned}
i_D(t) &\simeq k(v_{LO}(t) - V_{th})^2 + 2k(v_{LO}(t) - V_{th})v_{RF}(t) \\
&= I_D(t) + g_m(t)v_{RF}(t)
\end{aligned}
$$

hence, the model becomes a *quasi-linear* time-varying *small signal model* and the device operates in the *Small Signal Large Signal* regime (SSLS), because we still have the product of the two input signals through the transconductance. It is worth it to notice that depending on the amplitude of the RF (the LO is always driven in large signal), mixing can be obtained

[1]The definition of the gain and loss in mixer will be presented further.

both in linear region or through second order non-linearity (fully non-linear device). A more detailed analysis about how to drive a mixer follows in section 2.

Similarly to linear circuits, even in case of mixers it is possible to define the gain. Actually, gain is defined only in case of linear systems, but this figure of merit is necessary to qualify the performance of the conversion stage. In case of non-monochromatic signals one defines the *voltage conversion gain* as:

$$A_v = \frac{V_{IF,rms}}{V_{RF,rms}}$$

moreover, one has that the output power is proportional to LO power (that is also called a *pump*).

**DA FINIRE CON FIGURE DI MERITO**

# 2 Analysis of a Gilbert cell-based analog multiplier

## 2.1 Gilbert cell overview

A CMOS-based technology Gilbert cell-based mixer is shown in figure **AGGIUNGI IMMAGINE**. This circuit exploits a differential topology to implement a double-balanced cell providing:

- Reasonable conversion gain (from one to some tens);
- Thanks to the double-balanced topology if performs good rejection of input frequency components to the output port along with high linearity;[2]
- Good isolation between ports is provided by the high suppression of spurious frequency components;
- Thanks to the CMOS architecture it can be integrated.

## 2.2 Gilbert cell circuit analysis

To analyse the circuit it is necessary to give some informations about its topology, polarization and driving. Looking a FIGURA DOVE C'E' MIXER COMPLETO it is possible to identify five main blocks that are described in what follows.

**Bias net** This net is made up of the current mirror (transistors M1 and M2) and the voltage reference generation branch (transistor M5, R1, R2, R3, R4, R5).

Transistor M1 is the strong branch of the current mirror and it acts as a current sink for the differential pair made up by M3 and M4, fixing the polarization current for the whole circuit. M2 sinks instead the current from the voltage reference section of the bias net. Generally transistors in current mirrors are polarized in saturation region, so that an high output resistance is seen from the stage above: this means that M1 should appear as a good current sink. Given $V_{G1} = V_{GS1}$ the gate voltage in M1 we have that the transistor remains in saturation if:

$$V_{GS} \geq V_{th} \tag{1}$$

$$V_{DS} > V_{od} = V_{GS} - V_{th} \tag{2}$$

The same holds for M2, that is always in saturation condition since it is diode connected (provided 1). In saturation (neglecting channel modulation

[2] The linearity is meant with respect to the conversion gain.

effects), one has that the drain current only depends on gate voltage and it is given by:

$$I_D = \mu_{n,eff} \frac{C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{\beta_n}{2} V_{od}^2 \tag{3}$$

hence M1 remains in saturation till when:

$$V_{DS1} \geq V_{od1} = V_{th} - \sqrt{\frac{2I_0}{\beta_n}} \tag{4}$$

therefore to have a low value of the overdrive voltage one should have large transistors, i.e. large W. The output resistance in instead defined by:

$$r_o = \frac{1}{\lambda I_0} \propto L \tag{5}$$

where $\lambda$ takes count of the channel modulation. It appears that we need long transistors to have better current sink's properties. By looking at FIGURE 2, one has (supposing both M2 and M1 in saturation, and $V_{GS1} = V_{GS2} = V_{DS1} = V_{DS2}$):

$$I_0 = \frac{\beta_{n1}}{2} (V_{GS1} - V_{th})^2 (1 + \lambda_1 V_{DS1})$$
$$I_{REF} = \frac{\beta_{n2}}{2} (V_{GS1} - V_{th})^2 (1 + \lambda_1 V_{GS1})$$

hence, supposing to have equal transistors:

$$\frac{I_0}{I_{REF}} = \frac{W_1/L_1}{W_2/L_2} \tag{6}$$

Ideally the current mirroring is only depending on geometrical parameters, this means that a very good matching is required. Even if the two devices are very close to each other within the same chip, it exists the possibility to have a variation in parameters that depend on temperature, i.e. $V_{th}$ and $\mu_{n,eff}$. Supposing to have equal devices with everything constant but:

$$K_{n1} = K_n + \Delta K_n$$
$$V_{th,1} = V_{th} + \Delta V_{th}$$

one eventually finds that:

$$\frac{I_0}{I_{REF}} \simeq 1 + \frac{\Delta K_n}{K_n} + 2\frac{\Delta V_{th}}{V_{od}}$$

Then, some of the possible mismatch causes are:

- $k_n$, that can varies a lot in case of wide circuits;

- $V_{od}$ that usually is set low and varies with $V_{th}$, whose small variation can produce large differences in the two currents;

- difference between $V_{DS1}$ and $V_{DS2}$.

Assuming as maximum variations:

$$\frac{\Delta K_n}{K_n} = \pm 5\%$$
$$\frac{\Delta V_{th}}{V_{GS} - V_{th}} = \pm 10\%$$

one has:

$$\frac{I_0}{I_{REF}} = 1 \pm 15\%$$

A cascaded voltage divider is connected as M2's load:

- M5 is diode connected and it is used to generate the right gate bias voltage for the gain stage.

- A resistive voltage divider made up of R2 and R4 is used to polarize the mixing stage.

- Resistors R1 and R3 are used to connect the bias net to the gain and mixing stages' gates. They also acts as high impedance for the RF and LO signals coming from outside the circuit and prevents them to enter the bias net.

- Capacitors C1 and C2 shunt possible non-DC disturbances coming from the Gilbert Cell, improving the bias isolation.

Noise issues will not be analysed within this treatise, it should be considered for a more complete design though. As a rule of thumb, narrow gate and low overdrive voltages should used to lower noise contribution.(FONTE) Using a resistive voltage reference can be detrimental in case of voltage supply fluctuation, since a resistive voltage divider cannot reject current variations. However using active devices we would produce much more noise injection within the net though.

**Gain stage** The gain stage (shown in figure 3) is the linear part of the mixer, it must handle without distortion and corruptions the power coming from the RF signal giving some amplification. The topology is suited for a low noise amplifying purpose (FONTE): a differential stage with source degeneration. The stage is made up of two transistors (M3 and M4) in common source configuration directly polarized by M1 and two source degeneration resistances $R_S$.

The RF differential signal modulates the current flowing into each of the two transistors, that has to be polarized in saturation region. For both of them it must be ensured an high output voltage range and a quite low overdrive voltage, along with a large drain to source bias voltage (required to maintain the stage in saturation during the swing of the LO stage).

To have an idea on the gain that can be obtained by this stage, one can look at the stage in FIGURE 3. Removing the degeneration resistances one has that the gate-to-gate mesh gives:

$$V_{in,1} - V_{in,2} = V_{GS3} - V_{GS4}$$

from equation 3, recalling that $I_1 + I_2 = I_0$ and squaring:

$$(V_{in,1} - V_{in,2})^2 = \frac{2}{\beta_n}(I_0 - 2\sqrt{I_1 I_2})$$

that once inverted yields

$$I_1 - I_2 = \sqrt{\beta_n I_0}(V_{in,1} - V_{in,2})\sqrt{1 - \frac{\beta_n}{4I_0}(V_{in,1} - V_{in,2})^2}$$

writing the previous equation in term of $\Delta I = I_1 - I_2$ and $\Delta V_{in} = V_{in,1} - V_{in,2}$ and computing the value of the slope ot this characteristic, one obtains that the maximum differential voltage gain in equilibrium condition $\Delta V_{in} = 0$ is given by:

$$|A_v| = \sqrt{\beta_n I_0} R_1 \tag{7}$$

This suggest that it is better to polarize the stage exactly with $V_{GS1} = V_{GS2}$. The complete expression for equation 7 also gives that the differential transconductance is a strongly non-linear function of the gate bias voltage.

As we said before there it is the possibility to have a mismatch between the transistors and the loads due to circuit dimensions, temperature distribution and process tolerances, then looking at FIGURE 3:$M3 \neq M4$ and $R1 \neq R2$. It can be demonstrated that the offset output voltage due to differences in the circuit parameters and dimensions is:

$$V_{o,offset} = \Delta Vth + \frac{V_{GS} - V_{th}}{2}\left( - \frac{\delta R}{2R}\frac{\Delta W/L}{2W/L}\right)$$

To reduce this error a common centroid topology should be used in layout. Besides, it is important to notice that R1 and R2 are both the source output conductance of a common gate stage (mixing stage of the Gilbert cell) and that the actual gain for the RF stage is a current gain.

The small signal equivalent transconductance of the stage, once we added the source degeneration, (APPENDICE?) is given by:

$$G_{eq} = \frac{g_m}{1 + g_m R_S} \tag{8}$$

By adding $R_S$ we lower the RF stage's gain, however we also get a more linear behaviour of the stage reducing gain's dependency with respect to bias (this fact will be demonstrated later).

An important figure of merit concerning mixers is given by the -1dB compression point of the $V_{in}/V_{out}$ characteristic. By increasing the value of the RF signal the amount of harmonics at the output besides to the fundamental IF frequency increases as well, eventually saturating the output signals (gain compression or flatness). This is due to the fact that power is no more mainly carried by the fundamental output tone (i.e. the IF tone), but it is rather shared by all the growing up harmonics. In other words the conversion gain stops to be constant a reduces. Supposing to have input and output impedance matching one has that:

$$\begin{aligned}
A_{v,conv} &= \frac{V_{IF}}{V_{RF}} \\
20\log_{10} A_{v,conv} &= 20\log_{10}\frac{V_{IF}}{V_{RF}} \\
20\log_{10} V_{IF} &= 20\log_{10} A_{v,conv} + 20\log_{10} V_{RF} \\
V_{IF}|_{dB20} &= A_{v,conv}|_{dB20} + V_{RF}|_{dB20}
\end{aligned}$$

That suggest both that the output characteristic looks linear in log scale and that the -1dB compression point can be defined as the output IF voltage at which:

$$V_{IF}|_{-1dB} = A_{v,conv}|_{dB20} + V_{RF}|_{dB20} - 1dB$$

hence:

$$V_{IF}|_{-1dB} = V_{IF}|_{dB20,ideal} - 1dB$$

### 2.3 Mathematical analysis: conversion gain

## 3 Design by hand

# 4 Design by simulation

# 5 Layout of the Gilbert Cell

## 6 Simulation vs schematic comparison

## 7 Conclusions