EN811100 LINEAR CIRCUIT ANALYSIS
Mid-Term Examination
Academic Year 2564 Semester 2

Instructions:

1. There are 5 problems. Full scores require all 5 problems solved.
   คำถามมี 5 ข้อ ทุกข้อนับรวมเป็นคะแนนเต็ม
2. **During the exam session, communication is only allowed for submitting the answers to the designated submission system, monitoring the exam, and contacting the exam administrator.**
   ระหว่างการสอบ อนุญาตการสื่อสารเฉพาะสำหรับ ส่งคำตอบ และดูแลการสอบ และติดต่อกรรมการคุมสอบ
3. All materials and general numerical computation tools are allows.
   หนังสือ ตำรา เอกสาร หรือแหล่งข้อมูลใด ๆ รวมถึงเครื่องมือโปรแกรมคำนวณเชิงเลขทั่ว ๆ ไป สามารถใช้ได้
4. Circuit simulator of any kind is **NOT** allowed. Consulting human being (but exam administrator) through any mean or media is **NOT** allowed. Posting, sharing, or disseminating any question or answer or part of it is **NOT** allowed.
   ไม่อนุญาตให้ใช้โปรแกรมวิเคราะห์วงจรไฟฟ้า. **ไม่อนุญาต**ให้ติดต่อกับบุคคลอื่น (นอกเหนือจากกรรมการคุมสอบ). **ไม่อนุญาต**ให้โพสต์ แชร์ หรือเผยแพร่ ส่วนหนึ่งส่วนใดของคำถามหรือคำตอบ
5. Students are expected to comply with KKU code of conduct throughout the exam as well as to declare their integrity through the provided system.
   นักศึกษาควรปฏิบัติตนตามพฤติกรรมที่เหมาะสมของนักศึกษามหาวิทยาลัยขอนแก่น และให้นักศึกษาประกาศยืนยันความซื่อสัตย์ผ่านระบบที่ได้จัดเตรียมไว้
6. Any conduct that may violate such code should be consulted with the exam administrator and obtained a permission before carrying out.
   การกระทำใดที่สงสัยว่าอาจละเมิดพฤติกรรมที่เหมาะสมดังกล่าว ควรได้รับอนุญาตจากกรรมการคุมสอบก่อนกระทำ

The submission is through Autolab (https://autolab.en.kku.ac.th).

The submission system allows an infinite number of submissions. A student can submit as many as 5 versions without any penalty. After that, each version over 5 is subjected to 5% penalty.
Due time is shown on the system.
Late submission will be penalized 50%.

How to write an acceptable answer

Student's answers will be graded with policy: `lca2022` (tolerance < 0.001).

`Grading option: e` (engineering prefix) means (1) text must be exactly matched. (2) Each number must be well spaced (there is space before and after a number). (3) A number can be written in a regular format, using engineering prefix or scientific notation.

E.g., Given reference: `vx = -12.4 V; ix = 18.5 mA`

```
vx = -12.4 V; ix = 18.5m A          GOOD FORMAT /
vx = -12.4 V; ix = 18.5 mA          GOOD FORMAT /
vx = - 12.4 V; ix = 0.0185 A        GOOD FORMAT /
vx = -12.4 V; ix = 18.5e-3 A        GOOD FORMAT /
vx = - 12.4009 V; ix = 0.0185 A     GOOD FORMAT / (Still within tolerance)
vx = - 12.401 V; ix = 0.0185 A      GOOD FORMAT × (Over tolerance)
vx = -12.4 V; ix = 18.5 e-3 A       BAD FORMAT! ×
vx = -12.4V; ix = 18.5mA            BAD FORMAT! ×
vx =-12.4V; ix =18.5mA              BAD FORMAT! ×
vx =-12.4V ix =18.5mA               BAD FORMAT! ×
vx =-12.4V. ix =18.5mA              BAD FORMAT! ×
```

`Grading option: l` (linear equation) means a linear equation must be written with each term well-spaced.

Each term can be written as a constant, a single variable, or a coefficient-variable pair. A coefficient-variable pair must start with coefficient following by a space then a variable. Constants and coefficients can be written in a regular format, using engineering prefix or scientific notation.

E.g., given reference: `-10 + v1 + 4 i2 = 0`

```
- 10 + v1 + 4 i2 = 0                GOOD FORMAT /
v1 + 4 i2 = 10                      GOOD FORMAT /
2 v1 + 8 i2 = 20                    GOOD FORMAT /
2k v1 + 8k i2 = 20k                 GOOD FORMAT /
2e3 v1 + 8e3 i2 = 20e3              GOOD FORMAT /
8e3 i2 = 20e3 - 2e3 v1              GOOD FORMAT /
- 10 + 2 v1 + 4 i2 = v1             GOOD FORMAT /
- 10 + v1 + 4.0009 i2 = 0           GOOD FORMAT / (Still within tolerance)
- 10 + v1 + 4.001 i2 = 0            GOOD FORMAT × (Incorrect)
- 10 + v1 + 3.999 i2 = 0            GOOD FORMAT × (Incorrect)
- 10 + 4 i2 = 0                     GOOD FORMAT × (# terms mismatches)
- 10 + 4 i2 + v1 + v2 = 0           GOOD FORMAT × (# terms mismatches)
- 10 + 4 i2 + v2 = 0                GOOD FORMAT × (Miss v1)
- 10 + 4 i2 + v1 = v1               GOOD FORMAT × (Incorrect)
- 10 + 4 i2 + v1 = v1               GOOD FORMAT × (Incorrect)
-10e-8 + 1e-8 v1 + 4e-8 i2 = 0      GOOD FORMAT × (Magnitude too small)
- 10 + v1 + 4i2 = 0                 BAD FORMAT! ×
-10+v1+4i2 = 0                      BAD FORMAT! ×
- 10 + v 1 + 4 i 2 = 0              BAD FORMAT! ×
- 1 0 + v1 + 4 i2 = 0               BAD FORMAT! ×
```

How to read Autograder feedback

```
lca2022: report mode: Hint ; tol: 0.001 ; grading mode: le
lca2022: # reference lines: 2
lca2022: # submitted lines: 2
lca2022: feedback: line 0
lca2022: * student   : - V1 + 100 i2 + Vx - 12.002 = 0
lca2022: * feedback: Linear: incorrect
lca2022: feedback: line 1
lca2022: * student   : i1 = 23.14e-3 A; V1 = 12.402 V
lca2022: * difference: ______________________######
```

`tol: 0.001 ; grading mode: le`

`tol: 0.001` means all numbers are graded with tolerance 0.001.

`grading mode: le` means two lines are expected in the answer.

- `l` means the (first) line is graded as a linear equation.
- `e` means the (second) line is graded in an engineering prefix mode.

`- V1 + 100 i2 + Vx - 12.002 = 0` is the submitted answer.
`Linear: incorrect` means this equation is incorrect.

`i1 = 23.14e-3 A; V1 = 12.402 V`
`______________________######`
means the first spot where the mismatch is found is there on the 12.402.

Q1. Given Figure 1, answer the following questions:
Line 1. Write KCL equation at node *a*. Use values if available, otherwise use variable names as provided.
Line 2. Deduce voltage V_y.
Line 3. Deduce current i_x.
Line 4. Deduce power dissipating on R1.
Line 5. Deduce power dissipating on R2.
Line 6. Deduce power dissipating on R3.
Line 7. Deduce energy expended on R1 over a period of 1000 hours.
Line 8. Deduce energy expended on R2 over a period of 1000 hours.

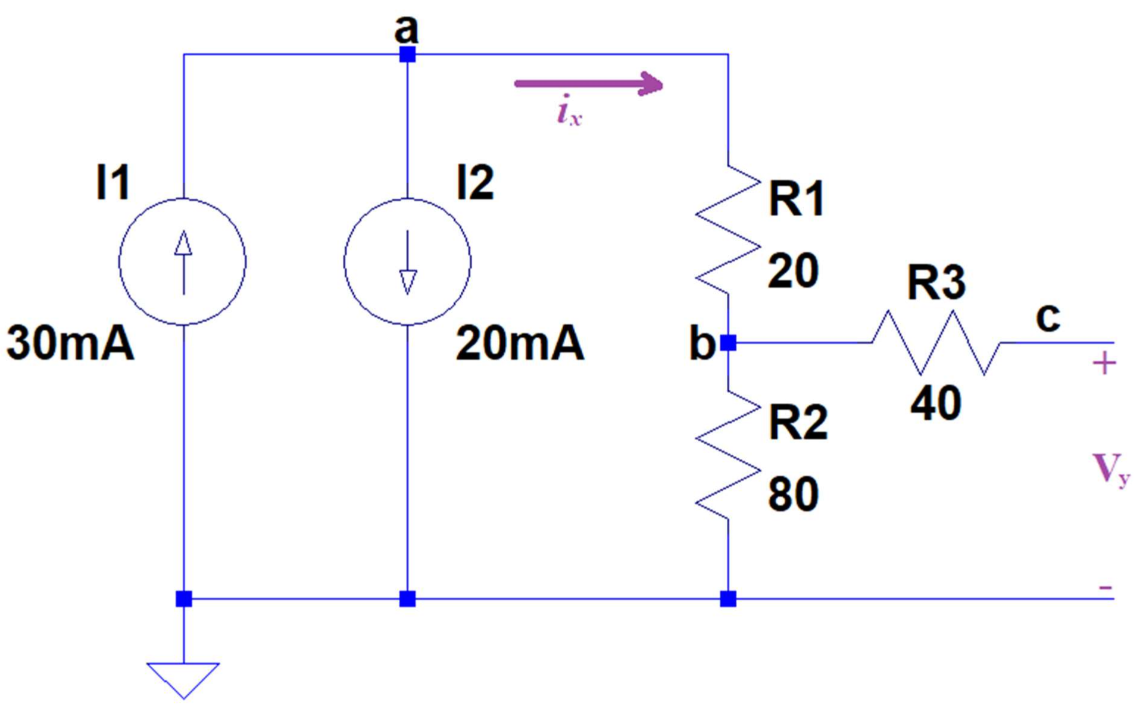

Figure 1

Write your answers in the following format. (Edit the red, but keep the navy blue.)

Line	Answer
1	0 v1 + 0 v2 + 0 v3 + 0 v4 + 0 v5 + 0 i1 + 0 i2 + 0 + 0 + 0 = 0
2	Vy = 0 V
3	ix = 0 A
4	P(R1) = 0 W
5	P(R2) = 0 W
6	P(R3) = 0 W
7	E(R1,1000) = 0 Wh = 0 J
8	E(R2,1000) = 0 Wh = 0 J

Grading: leeeeeee
Report: Hint

Q2. Given Figure 2, answer the following questions:
Line 1. Write KVL equation of loop 1. Use values if available, otherwise use variable names as provided.
Line 2. Write KVL equation of loop 2. Use values if available, otherwise use variable names as provided.
Line 3. Deduce currents i_x, i_y and i_z.
Line 4. Deduce powers dissipating on R1 and on R2.
Line 5. Deduce energies expended on R1 and on R2 over a period of 30 minutes.

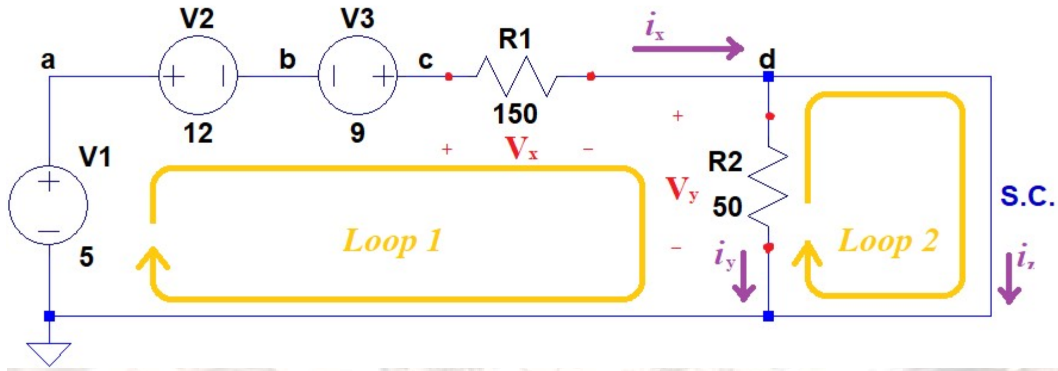

Figure 2

Write your answers in the following format. (Edit the red, but keep the navy blue.)

Line	Answer
1	0 v1 + 0 v2 + 0 v3 + 0 v4 + 0 v5 + 0 i1 + 0 i2 + 0 + 0 + 0 = 0
2	0 v1 + 0 v2 + 0 v3 + 0 v4 + 0 v5 + 0 i1 + 0 i2 + 0 + 0 + 0 = 0
3	ix = 0 A; iy = 0 A; iz = 0 A
4	P(R1) = 0 W; P(R2) = 0 W
5	E(R1,30min) = 0 Wh; E(R2,30min) = 0 Wh

Grading: lleee
Report: Hint

Q3. Given Figure 3, answer the following questions:
Line 1. Deduce nodal voltage *V(a)*.
Line 2. Deduce nodal voltage *V(b)*.
Line 3. Deduce nodal voltage *V(c)*.
Line 4. Deduce nodal voltage *V(d)*.

Notation *V(n)* means a nodal voltage of node *n*.

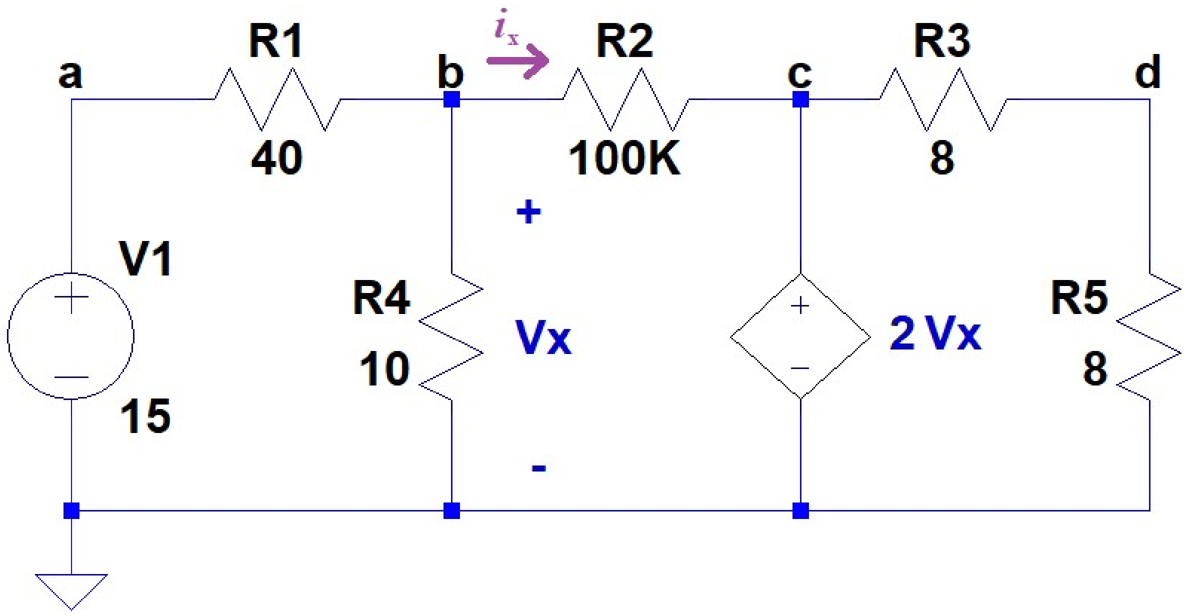

Figure 3

Write your answers in the following format. (Edit the red, but keep the navy blue.)

Line	Answer
1	V(a) = 0 V
2	V(b) = 0 V
3	V(c) = 0 V
4	V(d) = 0 V

Grading: eeee
Report: Hint

Q4. Common emitter is one of widely used configuration for transistor amplification circuit. Here we analyze a simplified version of it. Given Figure 4, answer the following questions:
Line 1. Deduce currents *ib* and *ic*.
Line 2. Deduce nodal voltage *V(b)*.
Line 3. Deduce nodal voltage *V(c)*.
Line 4. Deduce power dissipating on RL.

Hint: It can be solved through various approaches, but nodal or mesh analysis gives a systematic approach.

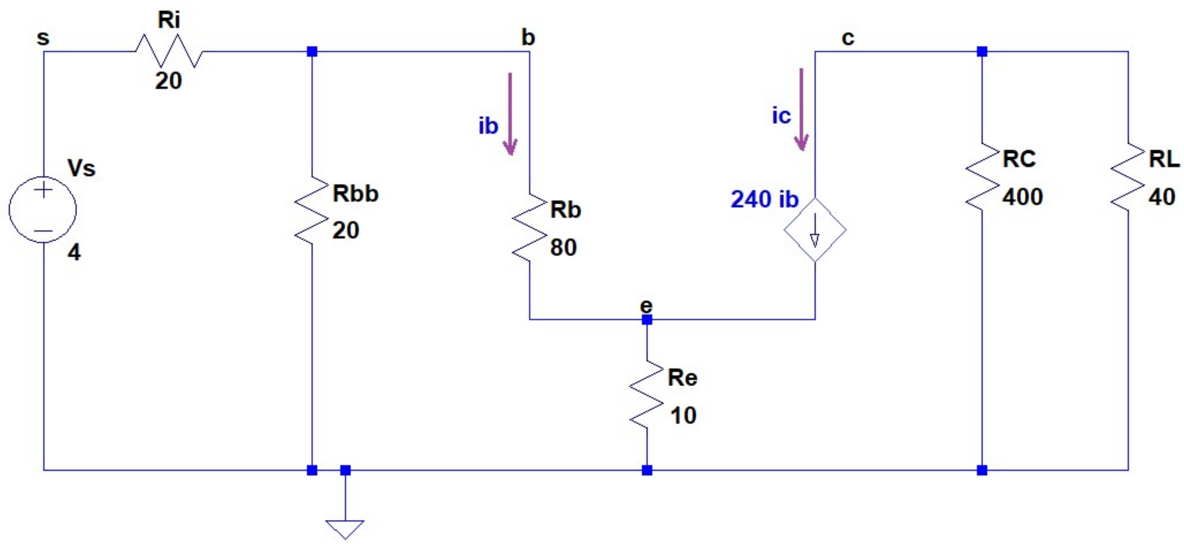

Figure 4

Write your answers in the following format. (Edit the red, but keep the navy blue.)

Line	Answer
1	ib = 0 A; ic = 0 A
2	V(b) = 0 V
3	V(c) = 0 V
4	P(RL) = 0 W

Grading: eeee
Report: Hint

Q5. A bus system is a crucial part of a computer system allowing communication among digital components. One of its key device is a tri-state gate, from LCA perspective tri-state gates can be modeled using switches. Here we analyze a simplified version of it. Given Figure 5, answer the following questions:
Line 1. When all switches are off, deduce nodal voltages *V(B0)* and *V(B1)*.
Line 2. When switches SWa0 and SWa1 are off, but SWb0 and SWb1 are on, deduce nodal voltages *V(B0)* and *V(B1)*.
Line 3. When switches SWa0 and SWa1 are on, but SWb0 and SWb1 are off, deduce nodal voltages *V(B0)* and *V(B1)*.

Hint: Break down a big problem into smaller sub-problems: redraw a circuit, remove what does not cast an effect, and each sub-problem will be much easier to analyze. (This is actually an easy problem.)

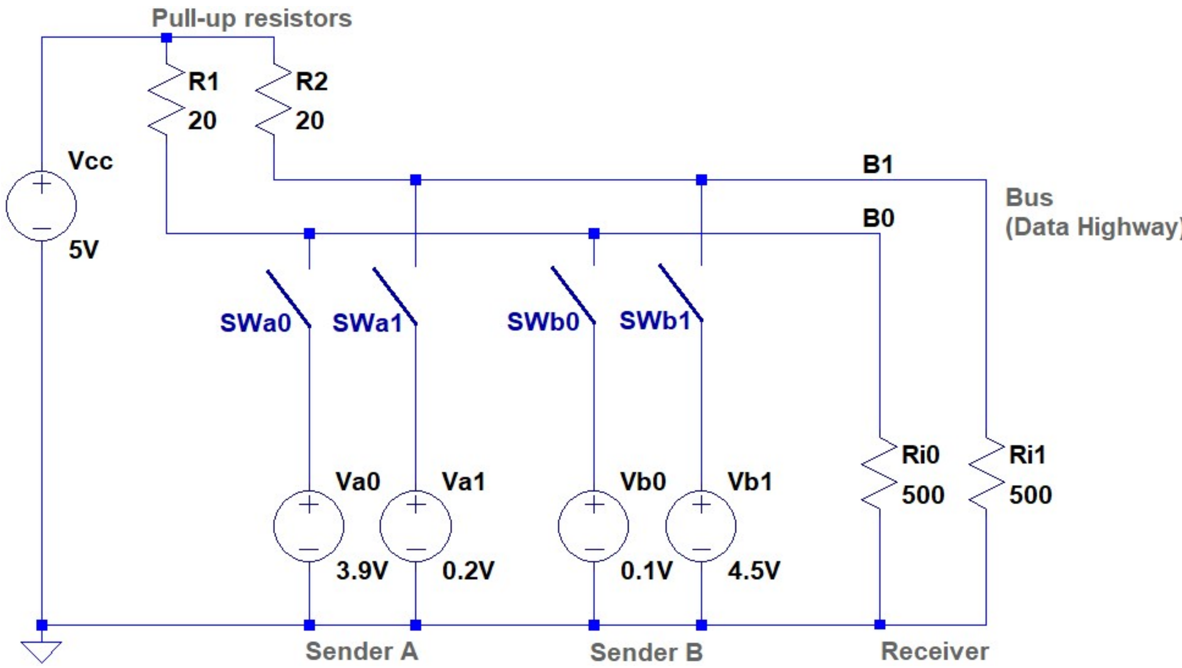

Figure 5

Write your answers in the following format. (Edit the red, but keep the navy blue.)

Line	Answer
1	off, off, off, off; V(B0) = 0 V; V(B1) = 0 V
2	off, off, on, on; V(B0) = 0 V; V(B1) = 0 V
3	on, on, off, off; V(B0) = 0 V; V(B1) = 0 V

Grading: eee
Report: Hint

THE END