

STATIC TIMING ANALYSIS NOTES

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graph LR; subgraph STA [Static Timing Analysis]; LM[Launch Mode] --> D[Delay]; D --> ARR1[ARR]; ARR1 --> ARR2[ARR]; ARR2 --> ARR3[ARR]; ARR3 --> C1[comb1]; ARR3 --> C2[comb2]; ARR3 --> C3[comb3]; C1 --> OM1[Output 1]; C2 --> OM2[Output 2]; C3 --> OM3[Output 3]; C4[comb4] --> OM4[Output 4]; end; C1 --> LM; C2 --> LM; C3 --> LM; C4 --> LM; CL[Clock] --> LM;
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Engineer

Static Timing Analysis:-

Why Timing Analysis:-

Three important design constraints are

→ Timing.

→ Power Consumption

→ Area of silicon chip.

Definition: Timing analysis is the methodical analysis of digital circuit to determine if the timing constraints defined in specifications are met.

I want to,



3.0 GHz
Expectation

But,



2.8 Hz

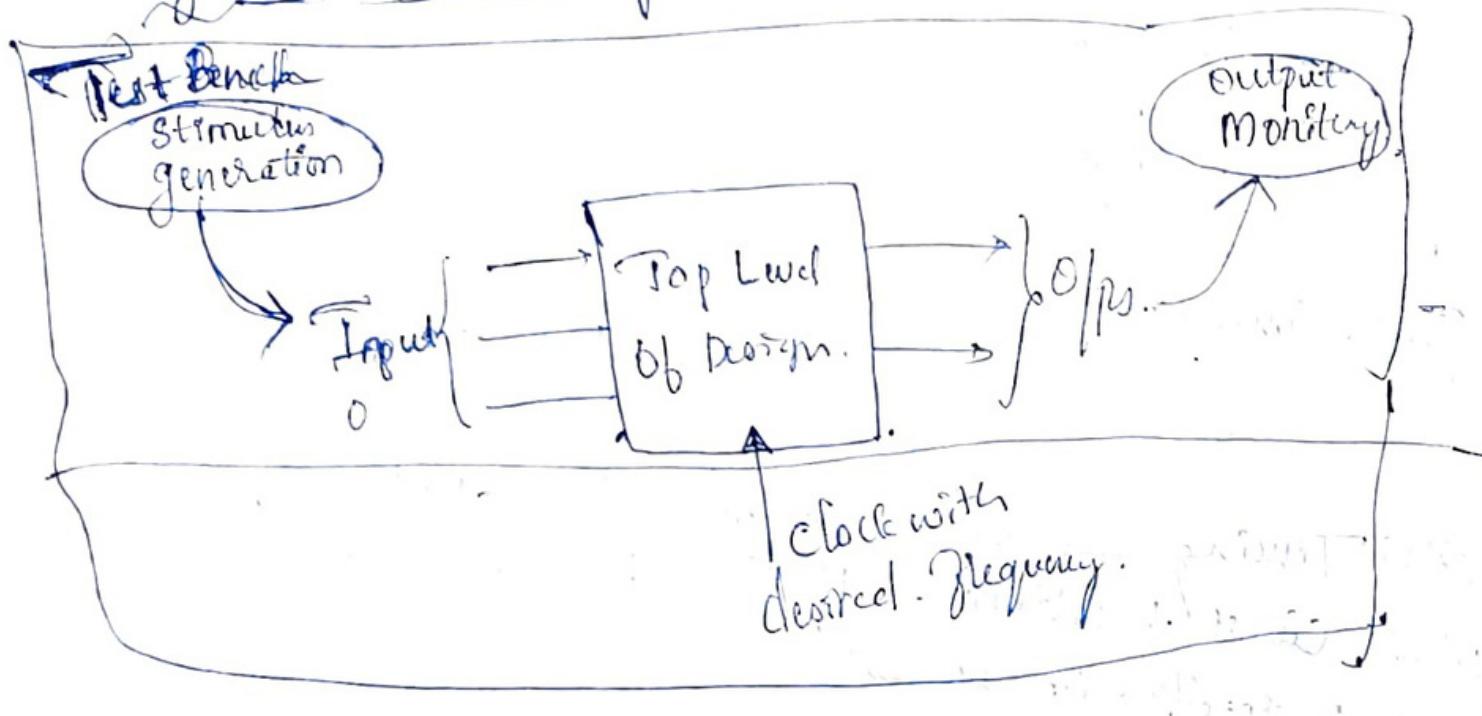
Reality

Types of timing Analysis

Two types.

- Dynamic timing analysis - Verifies timing in the functional context by applying stimulus.
- Static timing analysis - Verifies timing in each path of the logic circuit without applying stimulus.

Dynamic Timing Analysis



Advantages:-

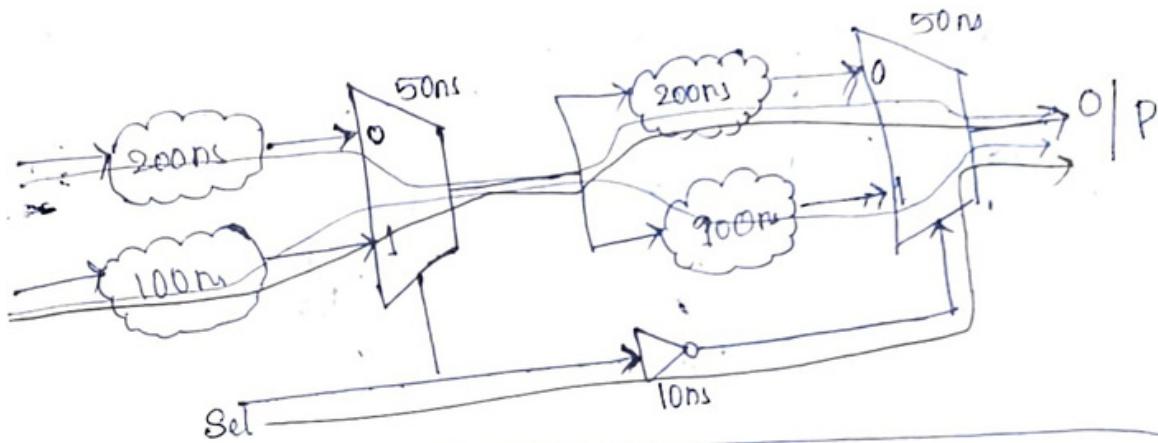
- Can be very accurate (Spice-level)
- Simulator calculates the logic value and delays

Disadvantages:-

- Vector creation takes too long, slow.
- Incomplete timing coverage.
- Analysis quality depends on stimulus vectors.
- Requires more memory and CPU resources over STA.

Static Timing Analysis:

↳ STA is capable of verifying every path.



→ The main goal of static timing analysis is to verify that all signals will arrive neither too early nor too late, and hence proper circuit operation can be assured.

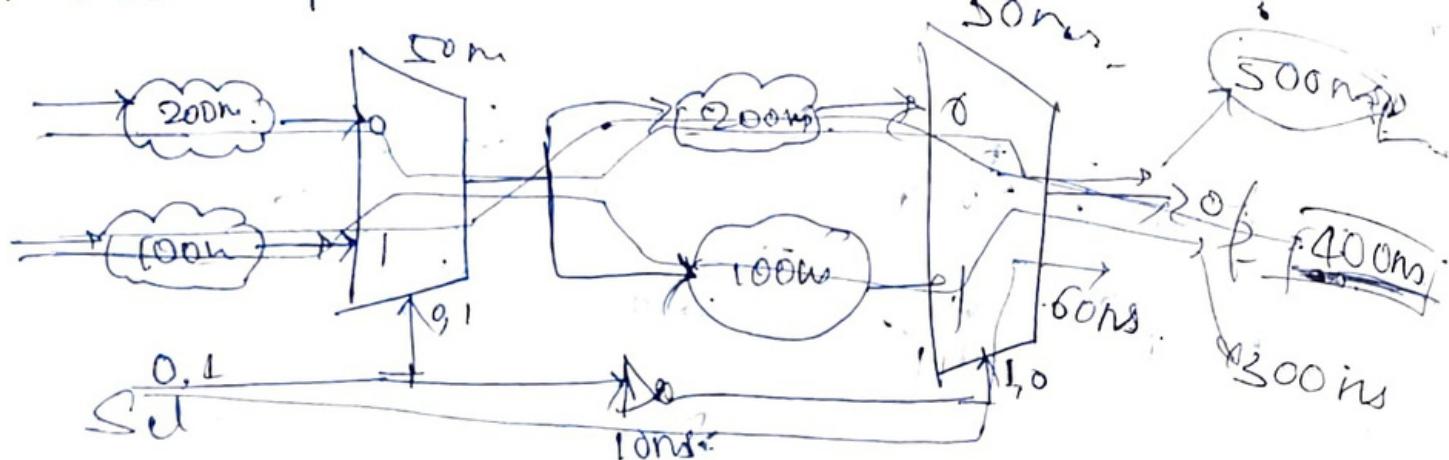
Advantages:-

- Much faster than timing-driven, gate level simulation.
- Exhaustive timing coverage.
- Does not require input vectors.
- More efficient than DTA in memory and CPU resources.
- Capacity for millions of gates.

Limitations:

- Works best with synchronous (not asynchronous) logic.
- Complex to learn.
- Must define timing requirements / exceptions.
- Difficulty in handling:
 - Multiple clocks
 - false paths
 - Multicycle paths.

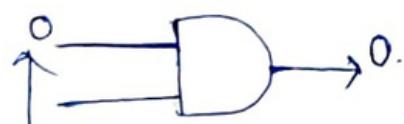
False Path :



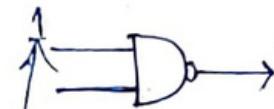
400ns path, based on MUX

~~400~~. So, here 500ns path will never occur, so it is called False path.

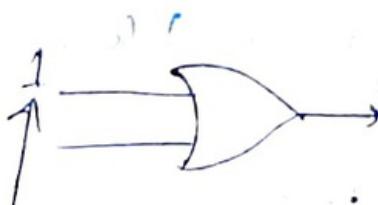
Controlling / Non-Controlling Values.



Controlling AND gate



Non-Controlling AND gate

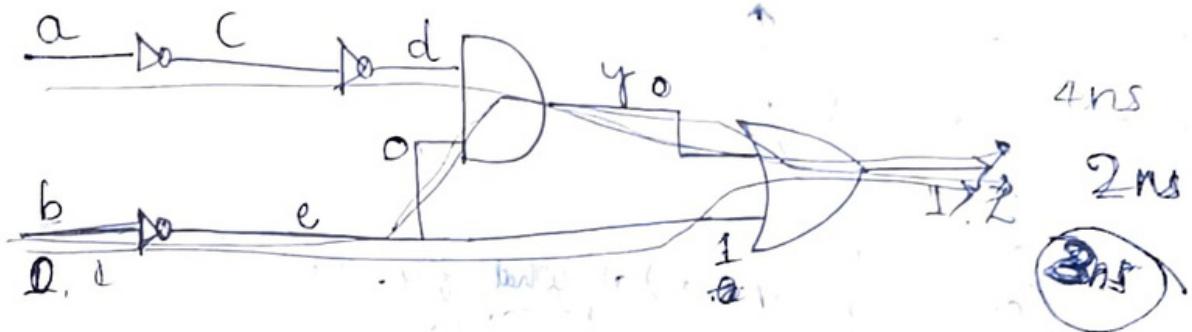
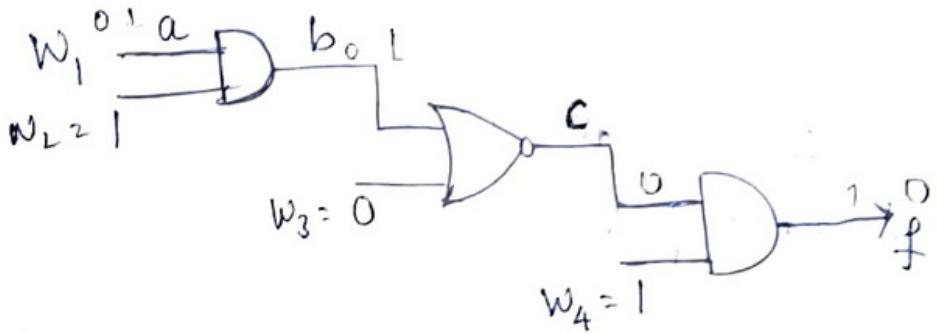


Controllable OR gate



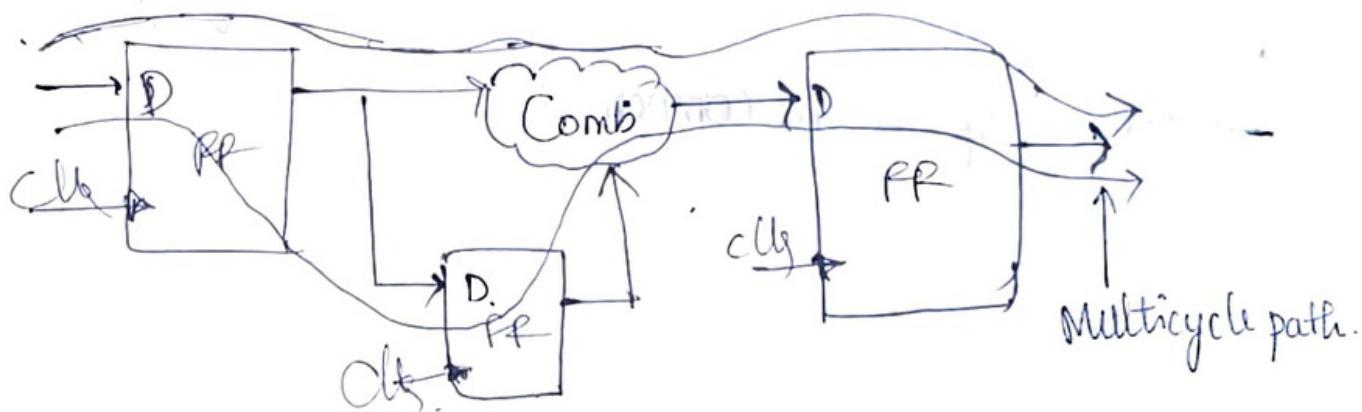
uncontrollable NOR gate

Path Sensitization -



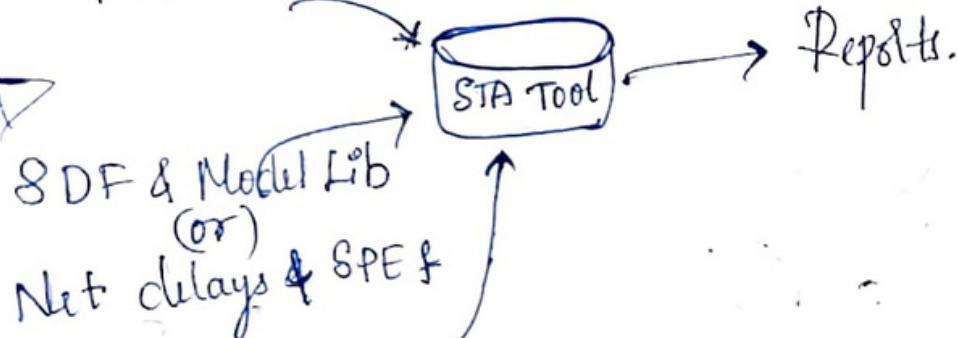
Multicycle path :

→ Path ^{internally} required more than one clock cycle to propagate.



Inputs & outputs of STA

(Describes circuit ~~structure~~ architecture in terms of gates and switches)
Netlist (gate level netlist or routed netlist)

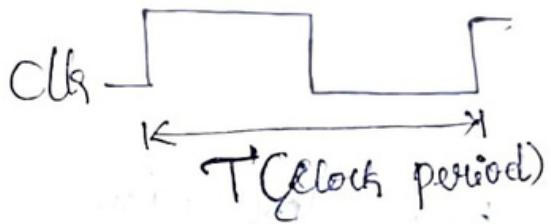


SDF → Standard delay Format file

After circuit Architecture we have to find the delay so we will use SDF & Model Lib, Netdelay & SPE-f.
↳ delay of each component

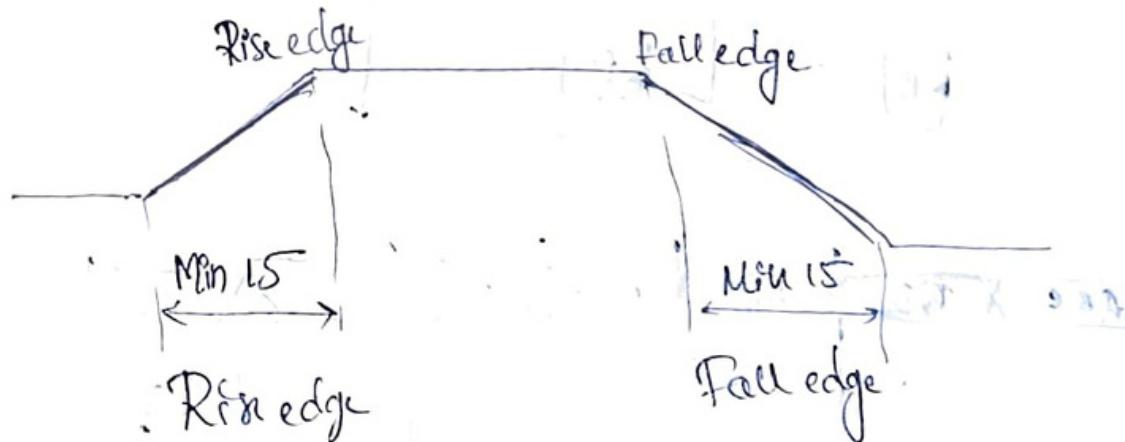
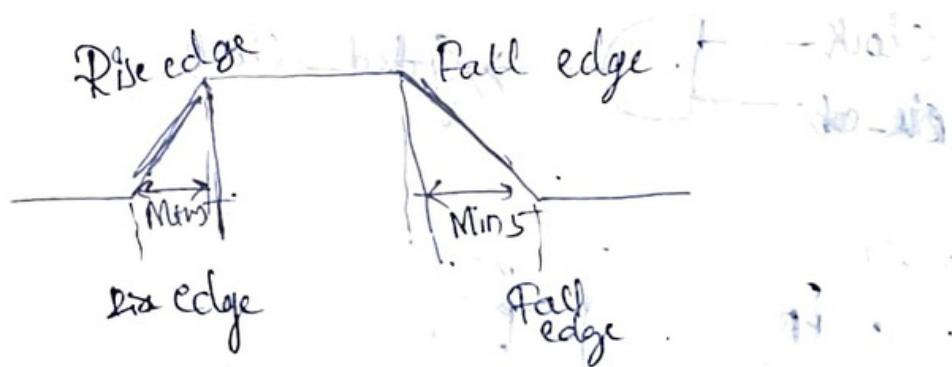
Clock :-

- The Clock is a periodic synchronization signal used as a time reference for data transfers in synchronous digital systems.



Slew :-

- Amount of time it takes for a signal transition to occur
- Accounts for uncertainty in rise and fall time of the signal
- Slew rate is measured in Volts/Sec



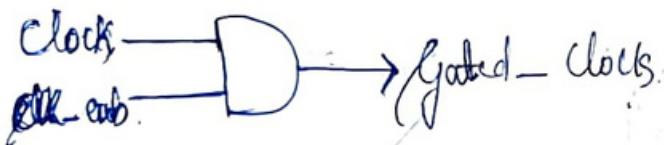
Types of Clocks :-

- Gated Clock
- Virtual Clock
- Generated (Derived) Clock.

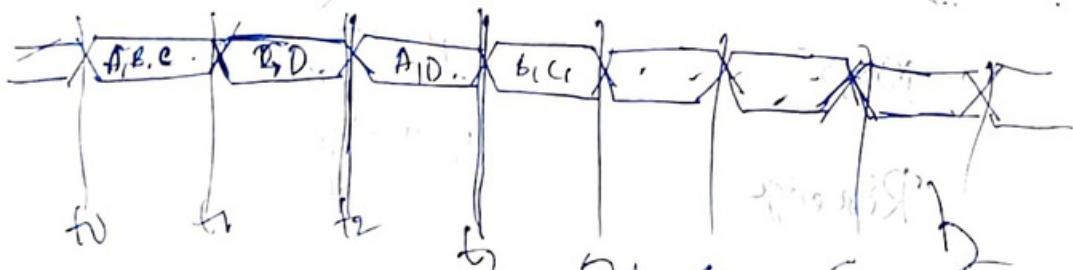
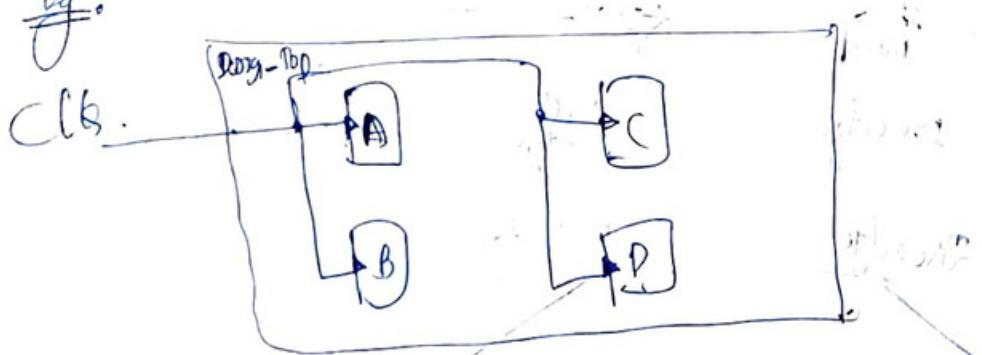
Gated Clock:

→ It is used mainly in "low power applications".

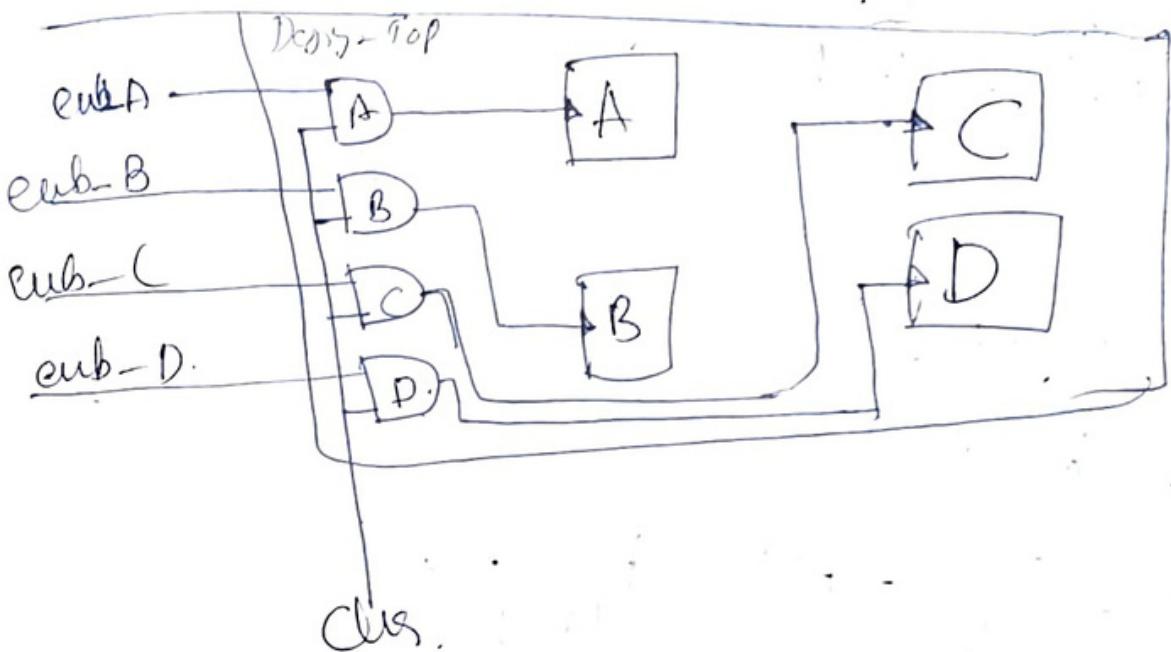
→ Clock gating reduces power consumption by switching off the clock to flipflops when the value of those flipflops does not change.



Eg:



In f1 to f3 only A, B, C should be operated.
But in begin we are giving clock to all four A, B, C, D
So by this it follows unnecessary power consumption

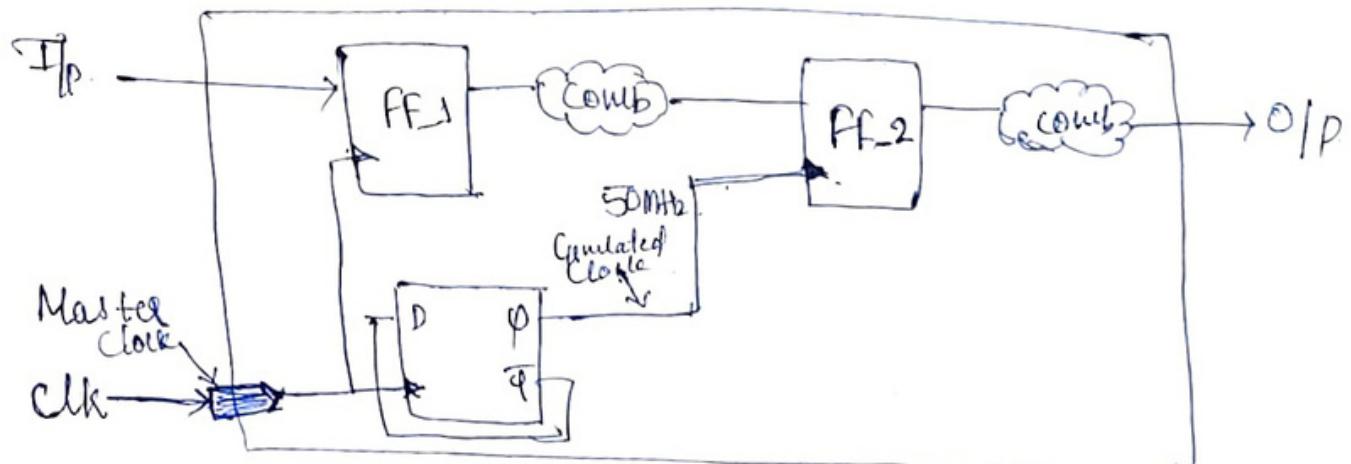


2) Virtual Clocks :-

- Virtual clock . has no source .
- Not connected to any port or pin within the current design .
- Mainly used to model the I/O timing specifications .
- Serves as a reference for i/p or o/p delays .

3) Generated Clock :-

- A design includes clock dividers or other structures that produce a new clock from a master source clock .

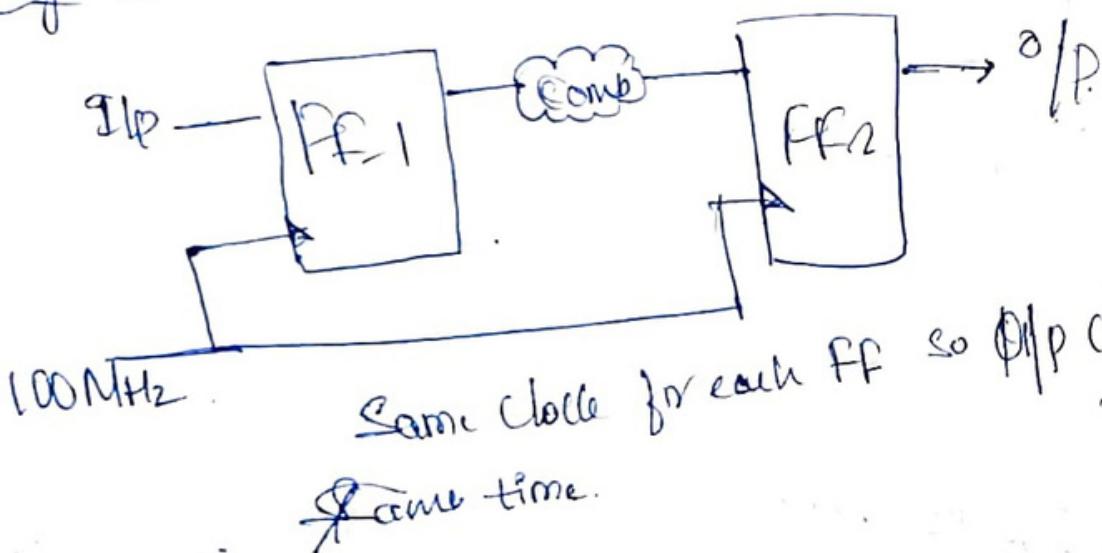


Master Clocks:

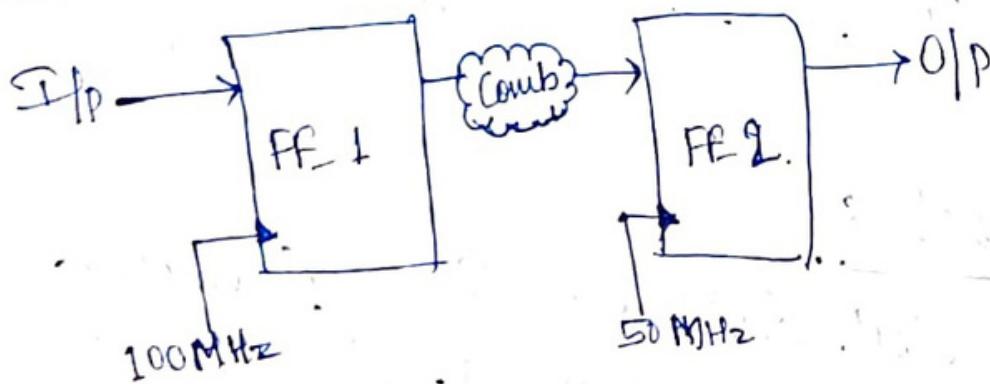
- # \Rightarrow Astable multivibrator.
 - \rightarrow Bistable multivibrator
 - \rightarrow Monostable multivibrator
- } Intel/few
purpose.

Clock domains:

Single clock domain:

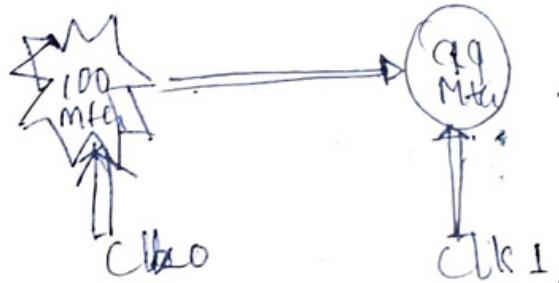


Double clock domain:

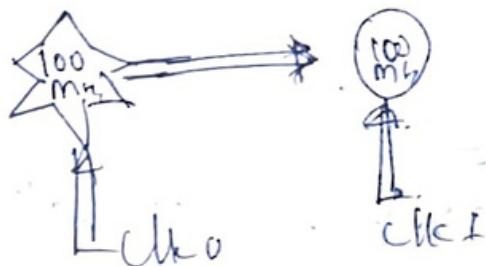


Synchronizing clock domains :-

- When they operate at two different frequency

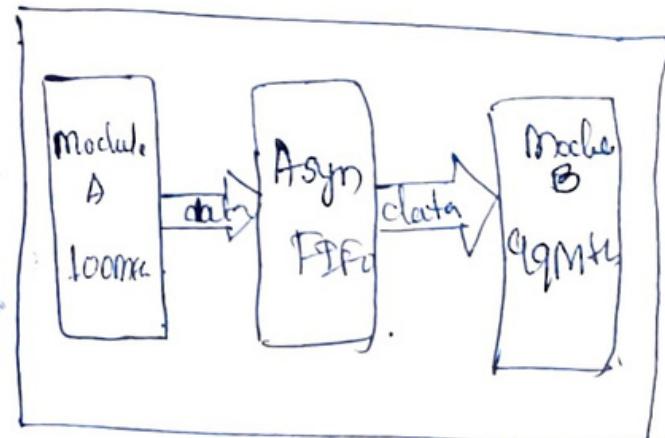
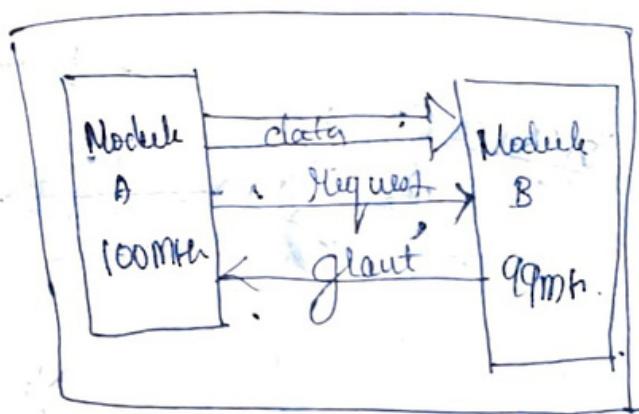


- When they operate at same frequency but at two different clock phase angles.



Techniques:-

- Use handshake signals to pass data b/w clock domains or,
- Use FIFO's to store data using one clock domain and to retrieve data using another clock domain.

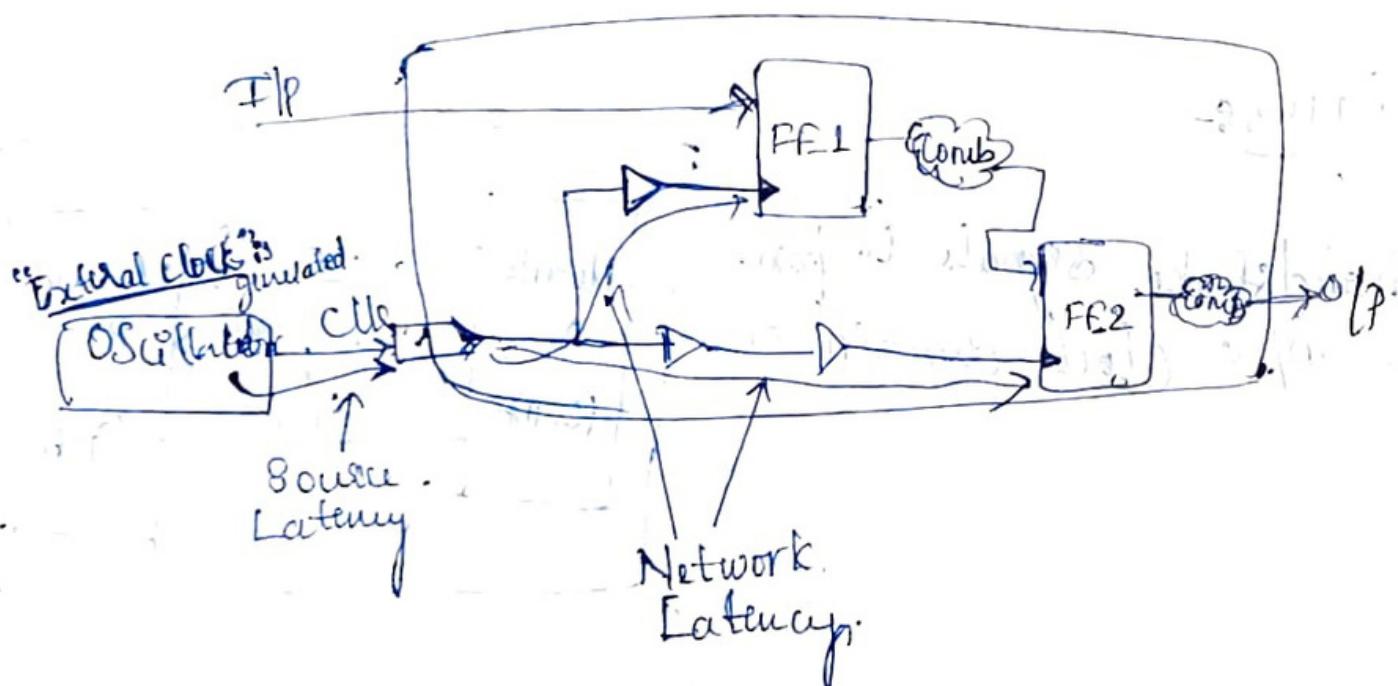


Clock Variations (Uncertainty)

- The possible uncertainties in clock are
 - ↳ Latency
 - ↳ Skew
 - ↳ Jitter

Latency :-

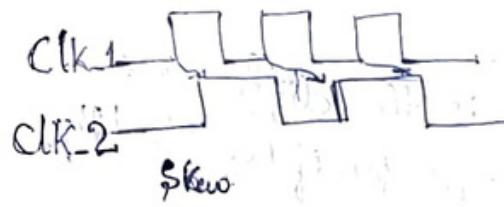
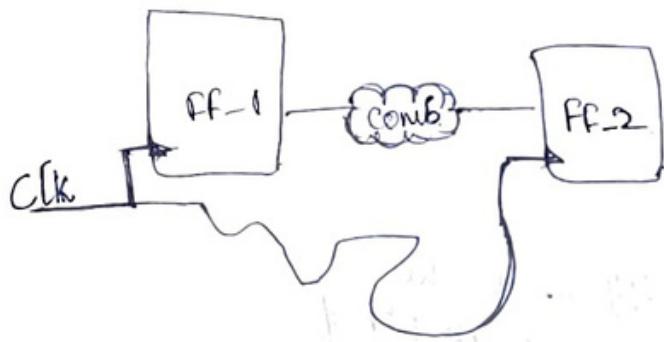
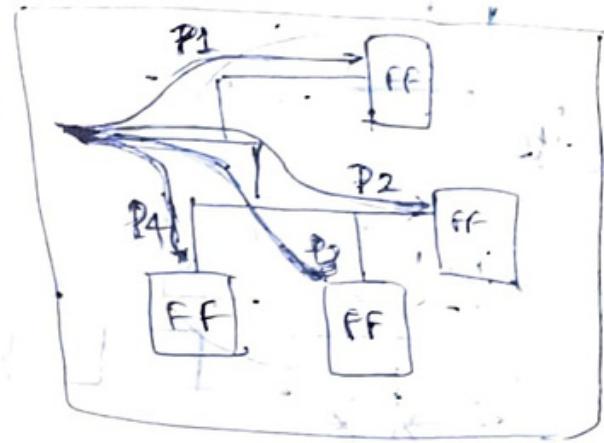
Clock source latency:-



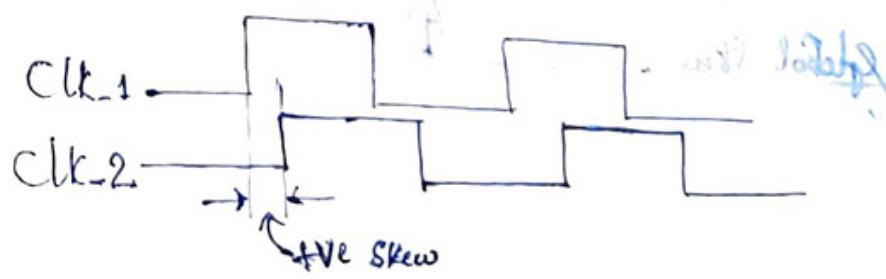
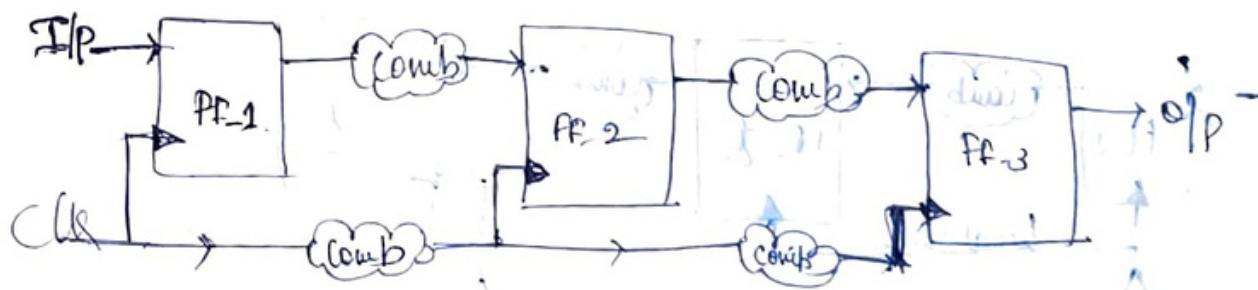
Clock Skew :-

→ Difference b/w arrival time of the clock at different devices is called clock skew.

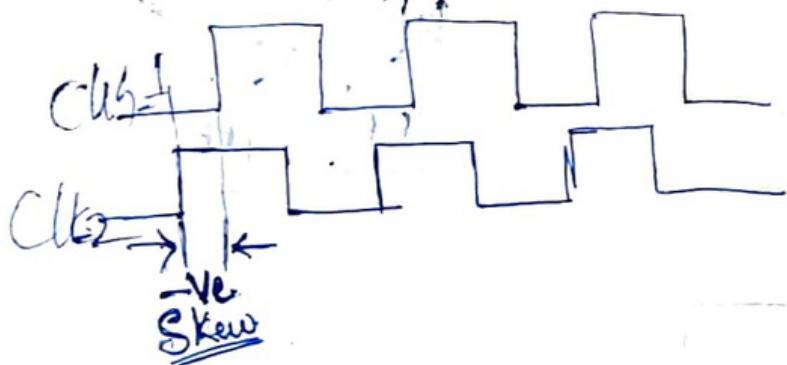
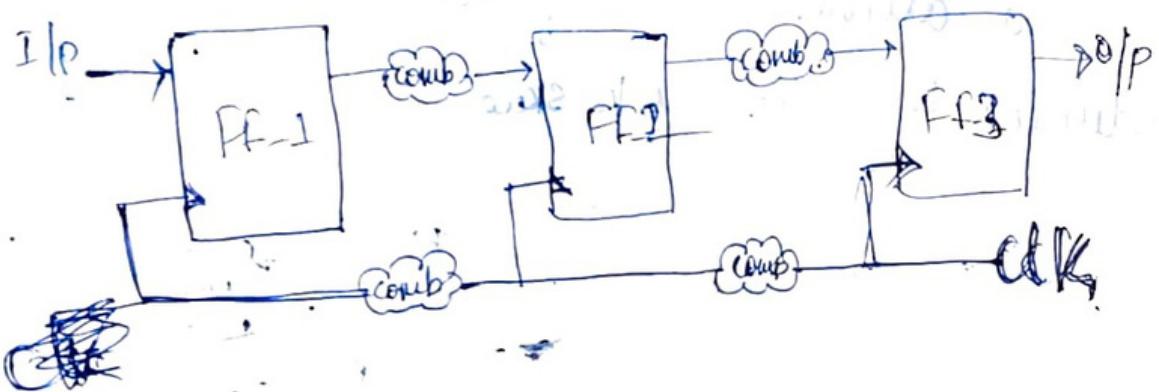
Dif b/w arrival time of the clock at diff devices is called Clock Skew.



Positive Skew :-



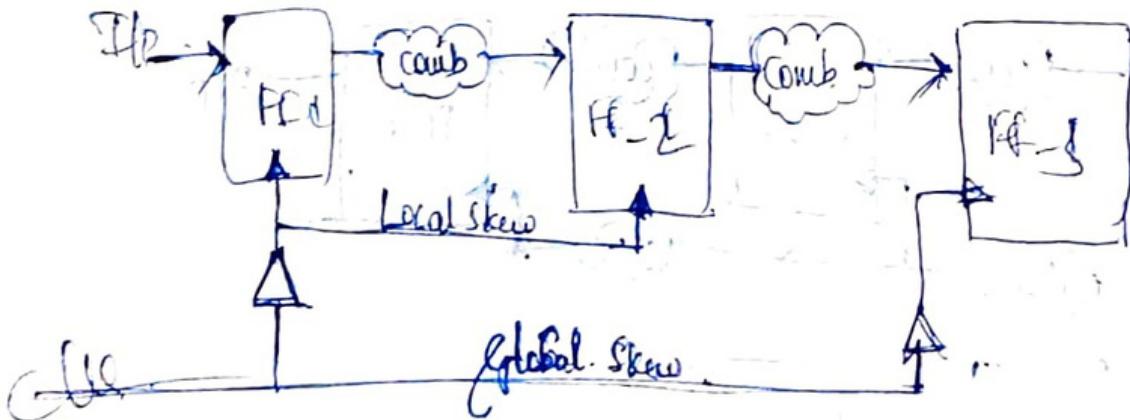
Negative Skew :-



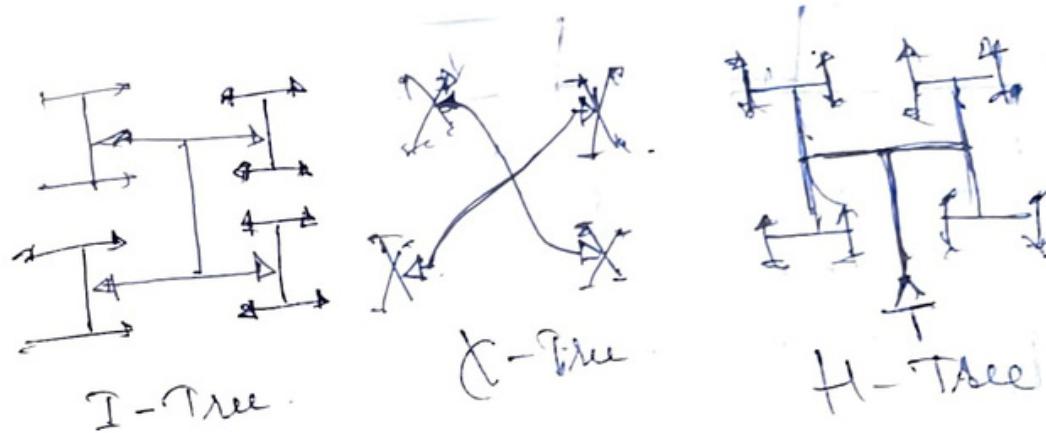
Local and Global Skew :-

• Local Skew :- Local skew is the difference in the arrival of clock signal at the clock pin of related flops.

• Global Skew :- Global skew is the difference in the arrival of clock signal at the clock pin of non-related flops.

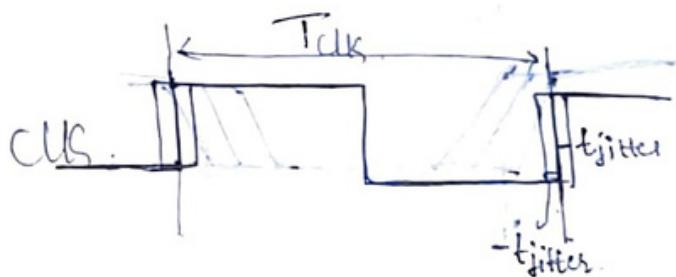


Strategies to minimize Clock Skew



Jitter :-

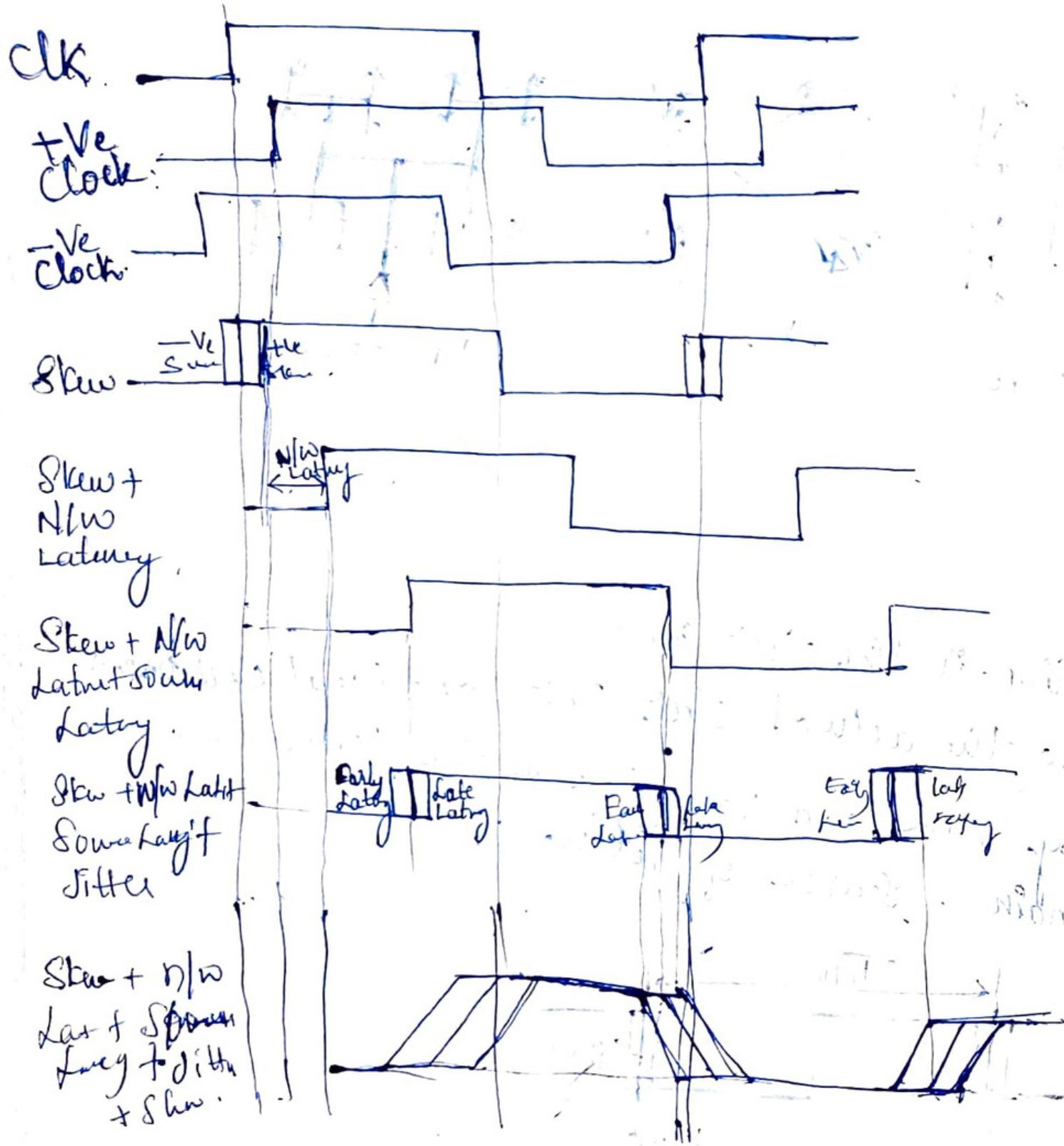
- Freq. variation in the clock source.
- Difference b/w the actual clock period and ideal clock period.
- Difference b/w the actual clock period and variations in the temperature.
- Power Supply noise and variations in the temperature are the main source of jitter.



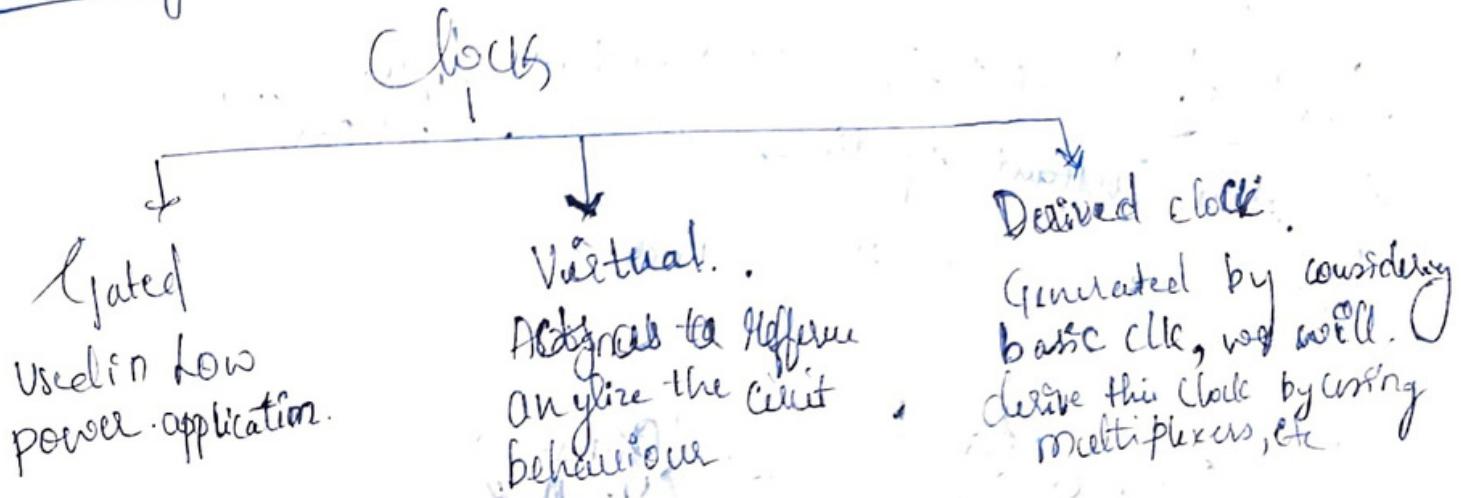
Skew and Jitter :-

- Skew is the permanent change in the clock arrival times.
 - ↳ Variation in when the same clock edge is seen by two diff FF
- Jitter is temporary variation in clock arrival times.
 - ↳ Variation in when two successive clock edges are seen by the same flip flop.

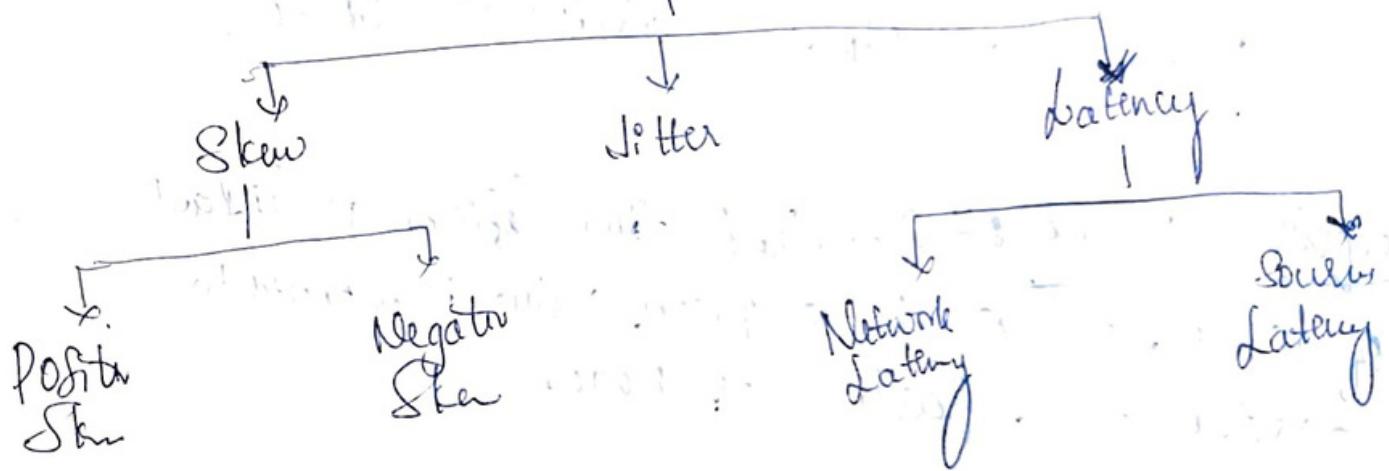
Clock :-



Summary :



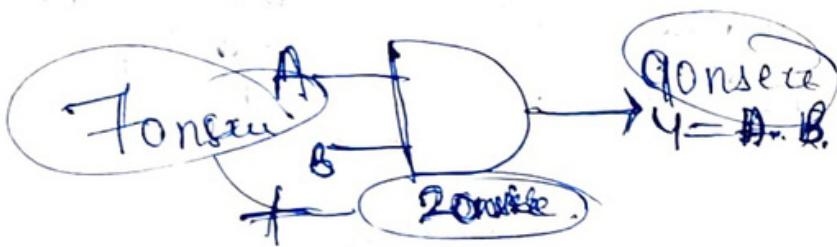
Uncertainty of Clock



Intrinsic skew
Main CLK freq.

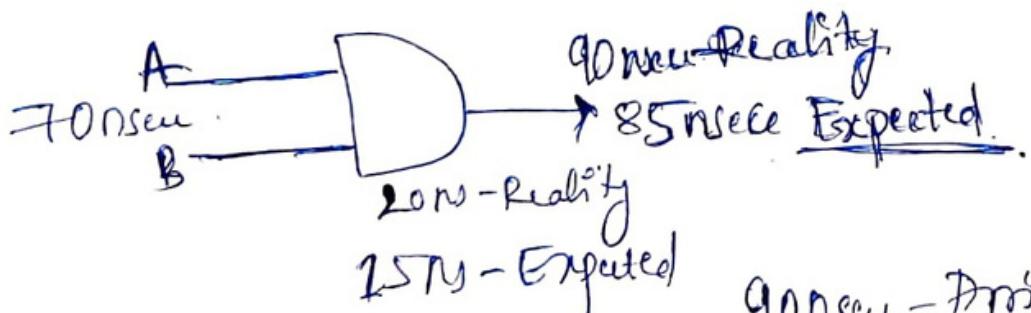
Timing Parameters in STA :-

Arrival time :- An arrival-time defines the instant of time, at which a proper value will arrive at a particular node.



we will get i/p & T_{Arrive} , and subsequently
20ns so o/p will arrive at 90nsec.

Required Time :- Required time defines the instant of time, at which a proper value is expected to arrive at a particular node.



90nsec - Arrival time
85ns - Required time

Slack and Critical path:-

Slack :-

→ The difference b/w the required time and Arrival time is.

$$\text{Slack} = \text{Req. time} - \text{Arrival time}$$

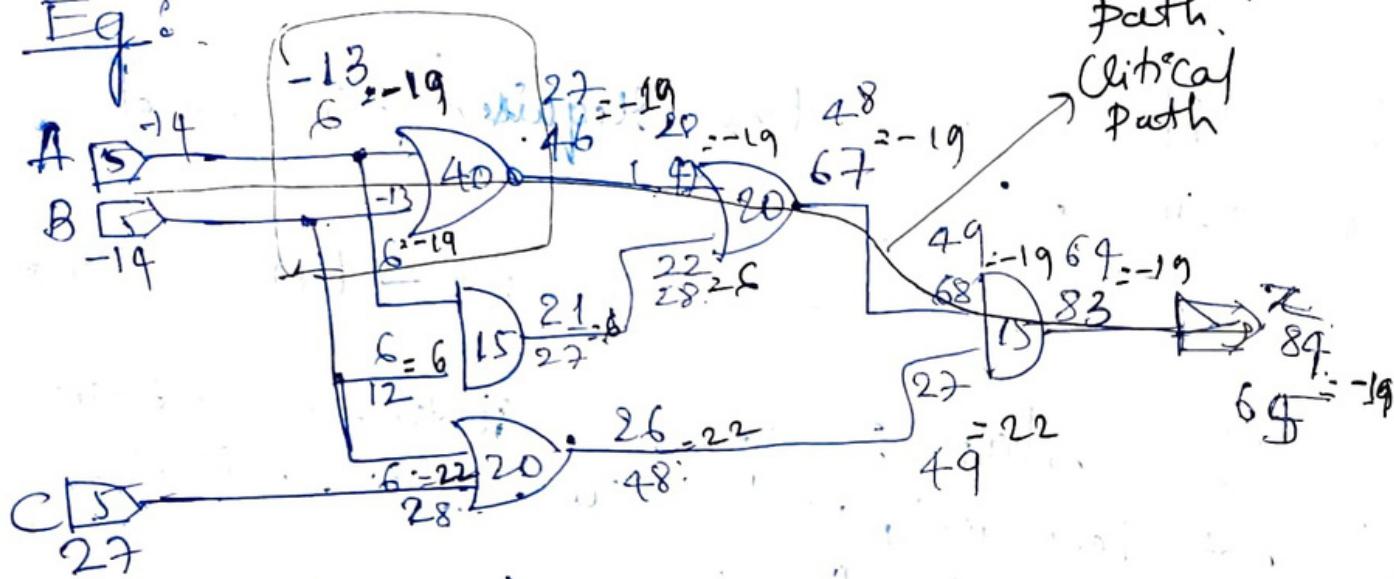
- If the Slack is negative, indicates constraints have not been met, while positive slack indicates that constraints have been met.
- Slack analysis is used to identify timing critical paths.

Critical path :-

- Any logic path in the digraph that violates the timing constraint.
- Path violating a negative slack, that violates the timing constraints is called is critical path.

Slack Analysis :-

Eg:-



* Wire delay is 1ns

* TIP arrival Time is 5hrs.

$$T_{pd}(\text{Actual}) = 84 - 5 = 79 \text{ ns.}$$

$$T_{pd}(\text{Expected}) = 60 \text{ ns.}$$

O/P required time is 165

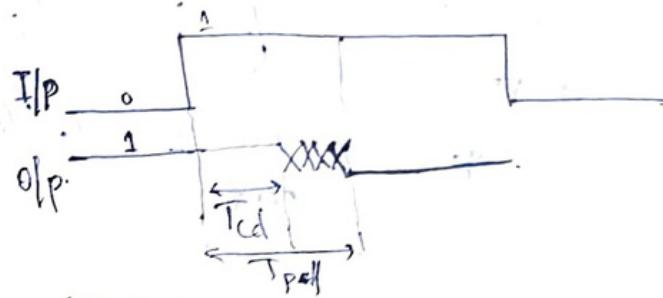
$$\text{Slack} = RT - AT$$

Timing is met ?

Timing is met when Slack is greater than or equal to zero

FIFO & Delays in Combinational Circuits

I/P \rightarrow O/P

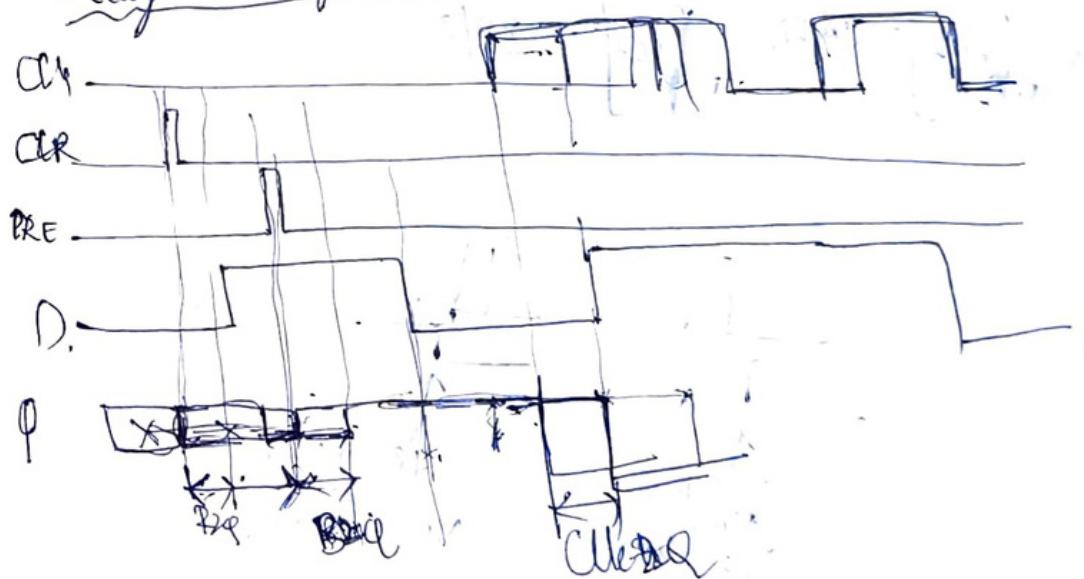


Combination Delay (T_{cd}):

The amount of time needed to change in the logic input to the result of initial change in output

Propagation Delay (T_{pd}): The amount of time need to change in the logic I/P to result permanent change in the O/P.

Delays in Sequential Circuits



R2Q Delay: It is the time taken by F.Flip flop to come to SET state after application of asyn. clear

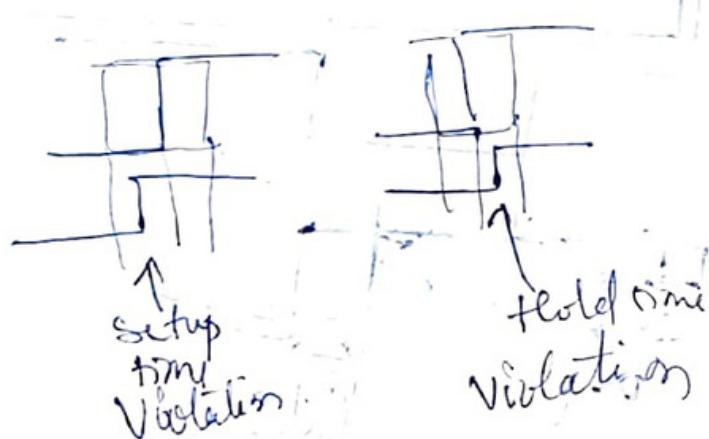
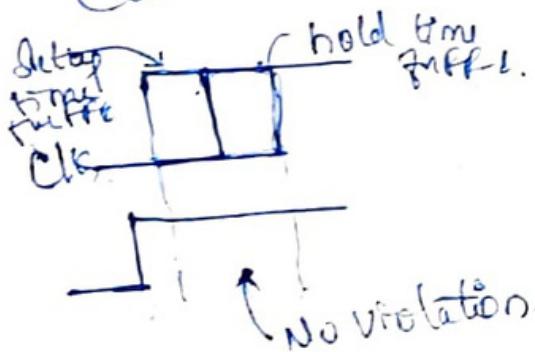
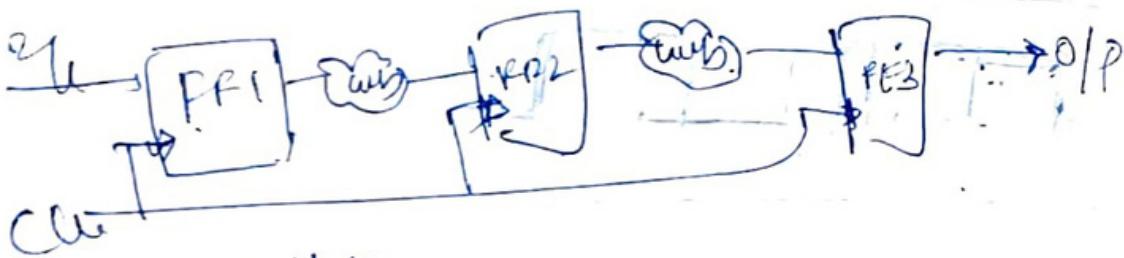
S2Q Delay: It is the time taken by flip flop to come to SET state when we apply PRESET.

CLR 2Q Delay: The time taken by the flip flop to change to the stable of.

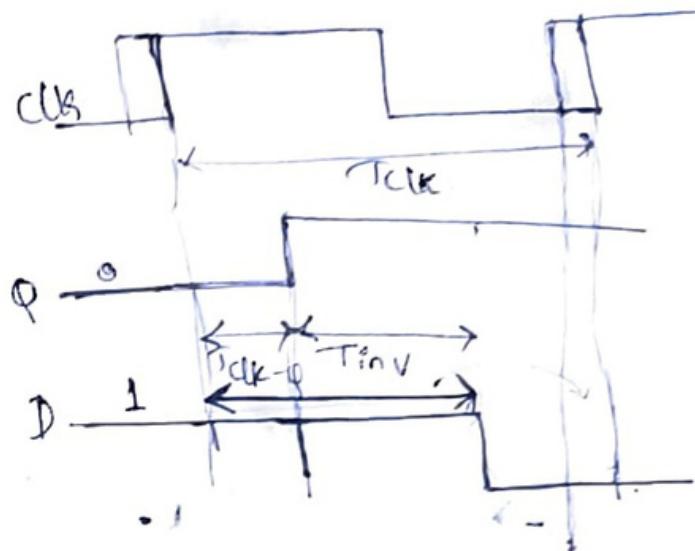
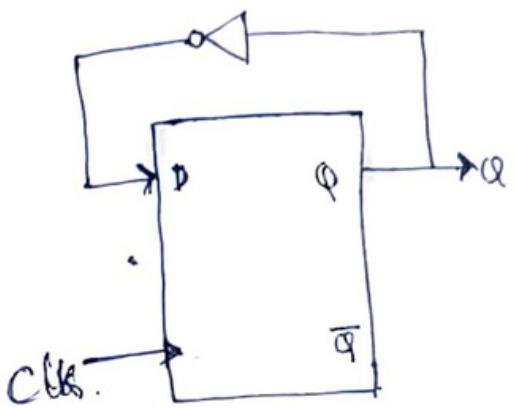
Timing parameters for sequential logic:

- Setup time (t_{su}): is the minimum time interval for which the I/P must be stable or unchanged prior to the sampling instant of the clock for its sign to be correctly recorded.
- Hold time (t_h): is the minimum time interval the I/P sig must be stable & unchanged following to the sampling inst of the clock if P. signal to change.

Setup time and hold time violations:



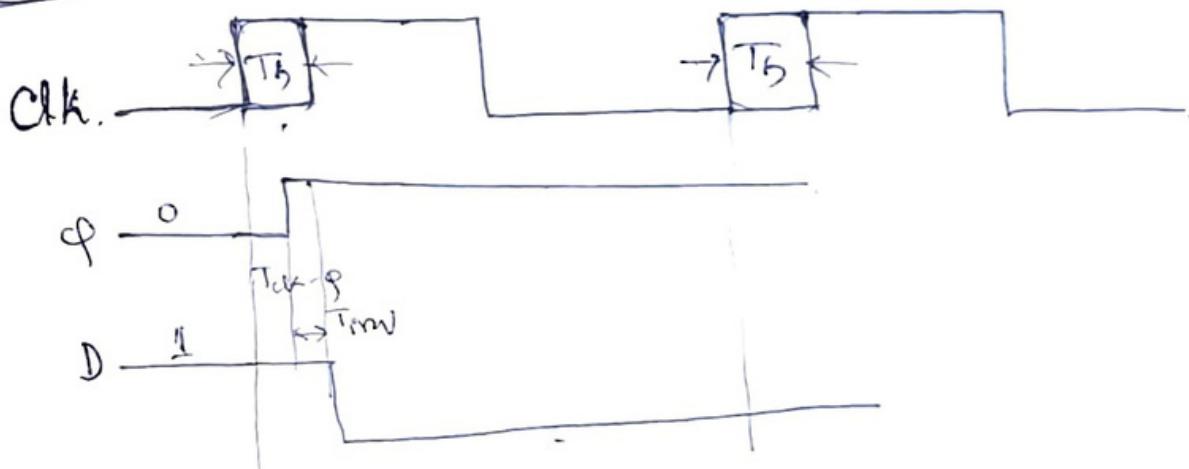
Setup time :-



$$T_{clk} - T_{setup} \geq T_{clk-Q} + T_{inv}$$

$$T_{clk} \geq T_{clk-Q} + T_{inv} + T_{setup}$$

Hold time :-

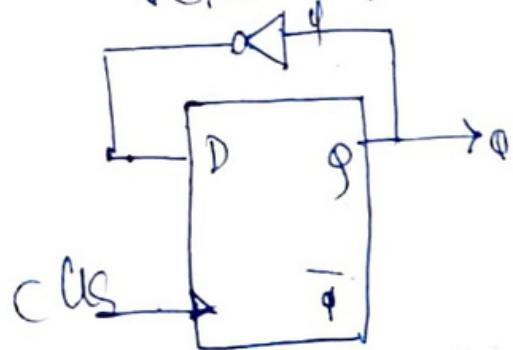


$$T_{clk-Q} + T_{inv} \geq T_{hold}$$

Ex: 1:

- Determine the maximum frequency of operation of the given circuit.

$$T_{CPD\text{-inv}} = 3 \text{ ns}$$



$$T_{CLK - Q} = 5 \text{ ns}$$

$$T_{Setup} = 2 \text{ ns}$$

$$T_{Hold} = 1 \text{ ns}$$

$$\rightarrow T_{Clock} \geq T_{CLK-Q} + T_{Inv} + T_{Setup}$$

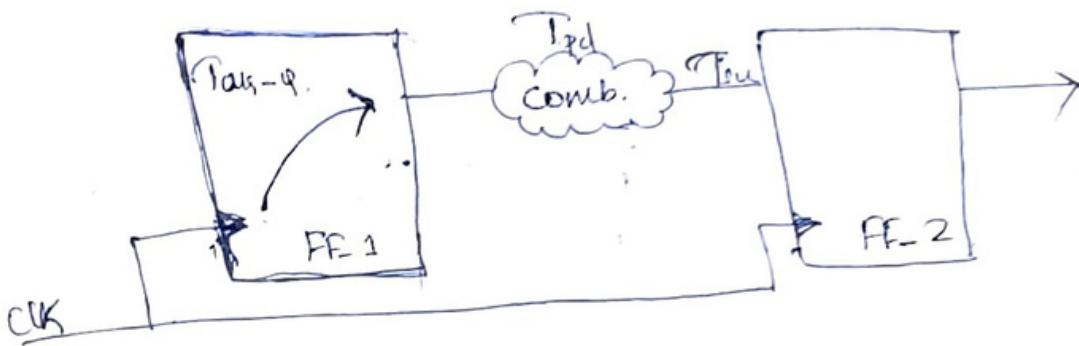
$$T_{Clock} \geq 5 + 3 + 2$$

$$T_{Clock} \geq 10 \text{ ns}$$

$$f_{max} = 1/T_{Clock} = 1/10 \text{ ns} = \underline{\underline{100 \text{ MHz}}}$$

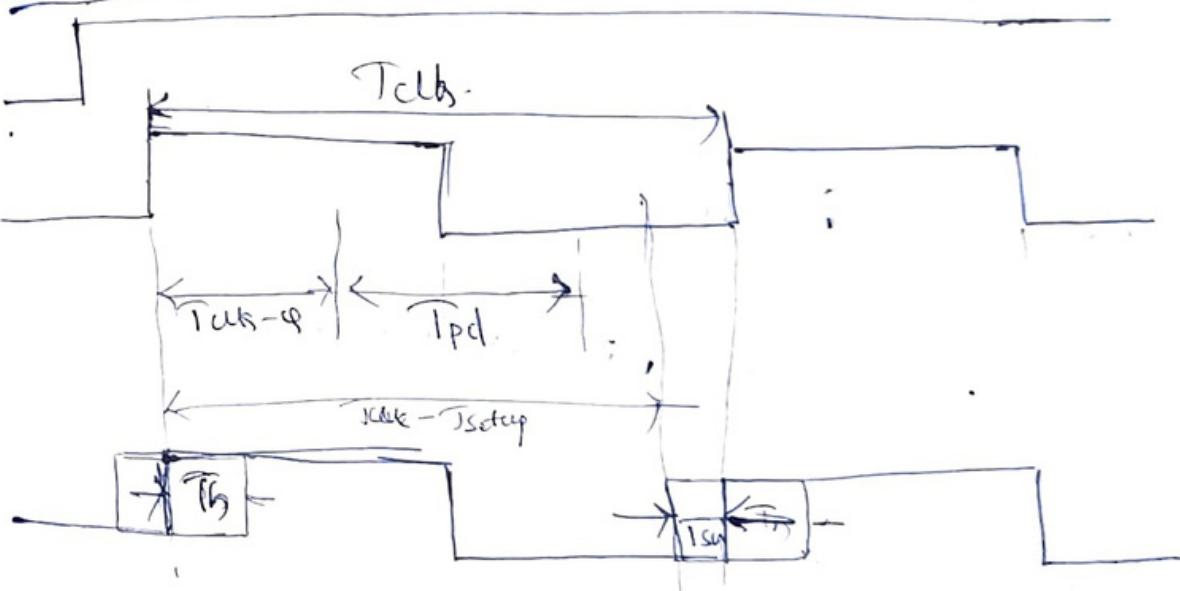
~~100 MHz~~

Timing Analysis



Flip flop: T_{setup} , T_{hold} & $T_{\text{clock-Q}}$.

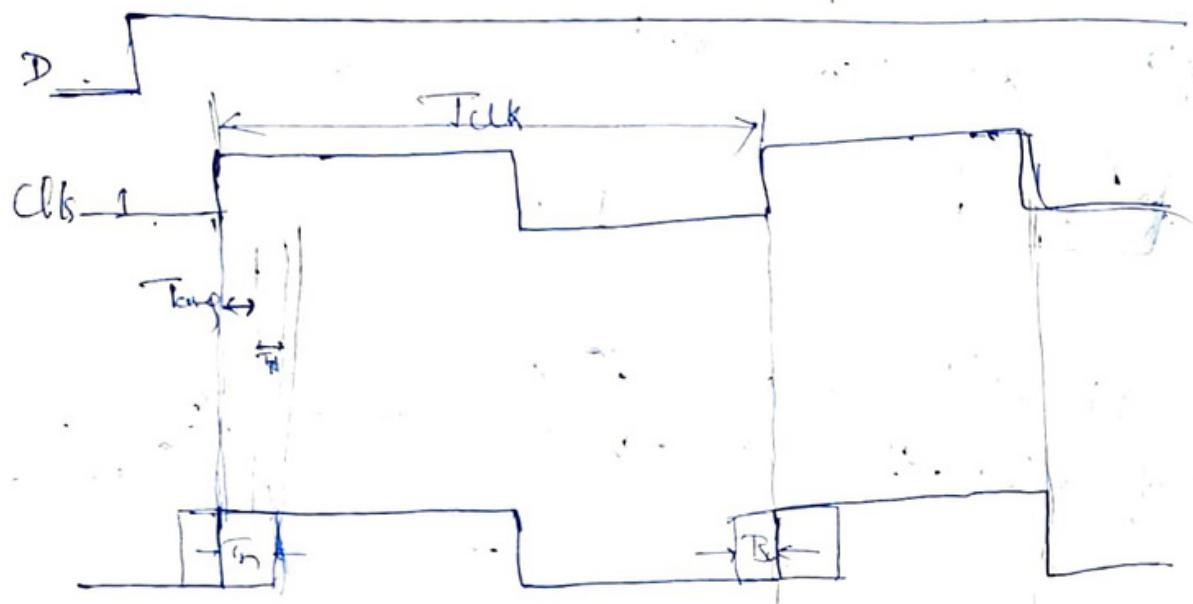
Calculation of setup time const without CLK skew: "Zero Skew"



$$T_{\text{ck}} - T_{\text{setup}} \geq T_{\text{clock-Q}} + T_{\text{pd(max)}}$$

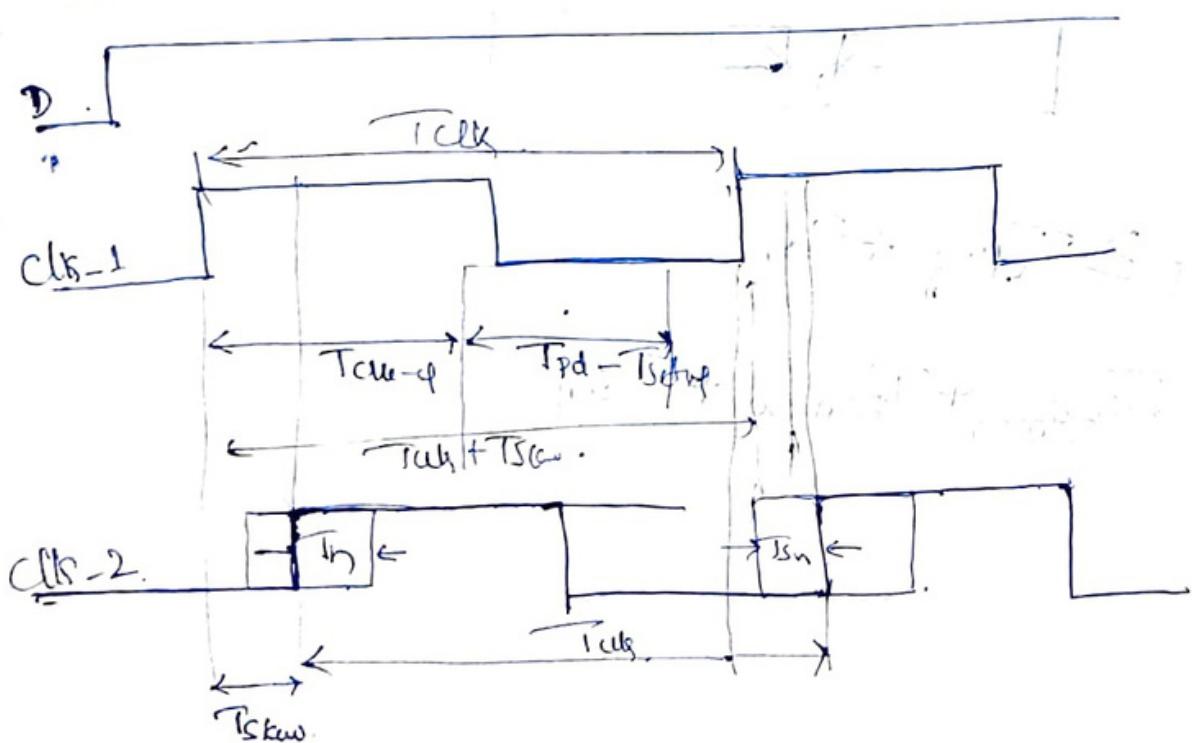
$$T_{\text{ck}} \geq T_{\text{clock max}} + T_{\text{pd(max)}} + T_{\text{setup}}$$

Calculation of hold time constraint with skew



$$T_{\text{Clk}-q(\min)} + T_{\text{d}(\min)} \geq T_{\text{Hold}}$$

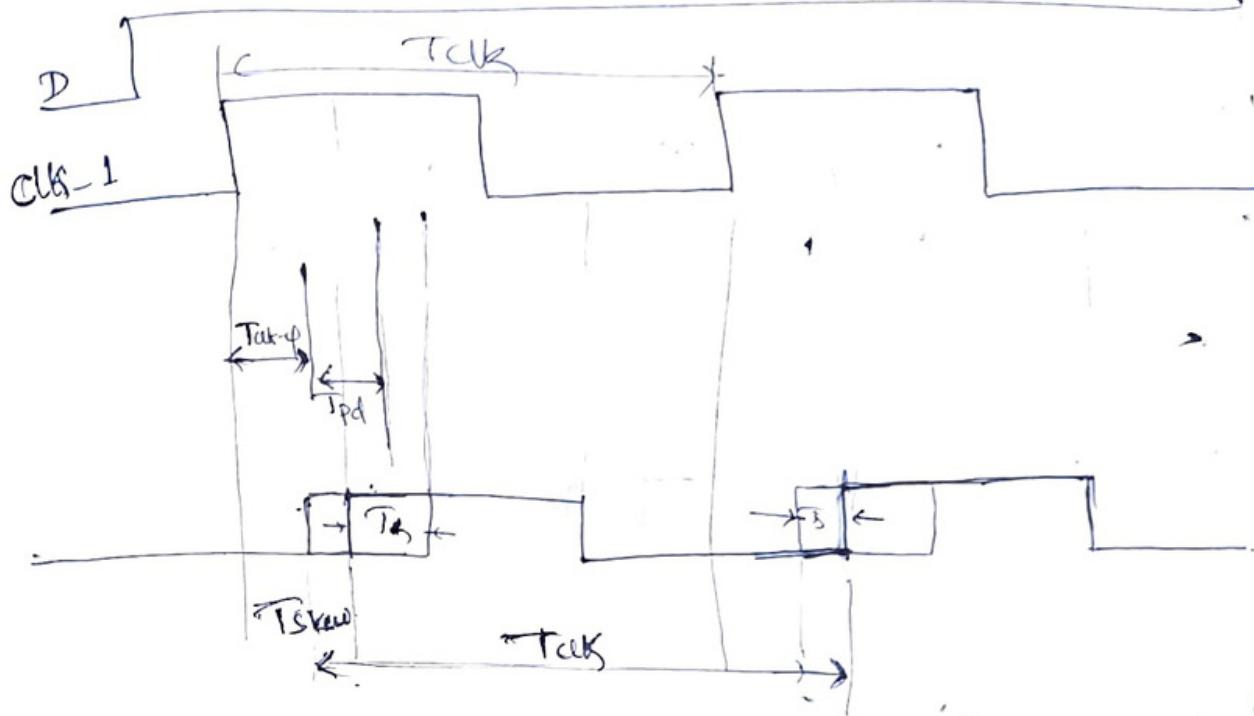
Calculation of Setup time const with the skew.



$$T_{\text{Clk}} + T_{\text{Skew}} - T_{\text{Setup}} \geq T_{\text{Clk}-q(\max)} + T_{\text{d}(\max)}$$

$$T_{\text{Clk}} + T_{\text{Skew}} \geq T_{\text{Clk}-q(\max)} + T_{\text{d}(\max)} + T_{\text{Setup}}$$

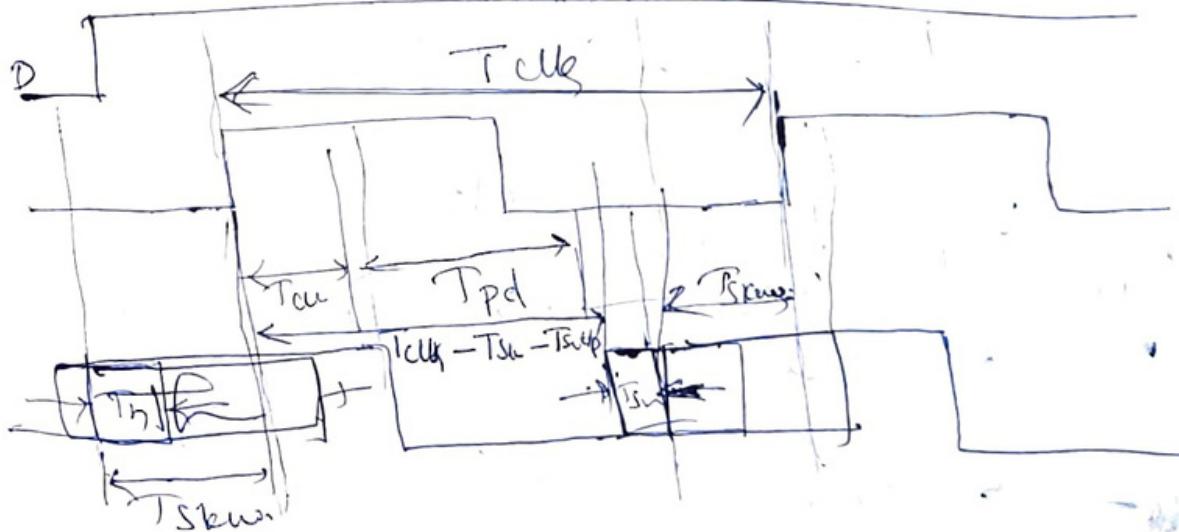
Calculation of hold time constraints with +ve skew



$$\text{Hold}_{\min} \leq T_{CK, A} + T_{PD, \min} - T_{S, \max}$$

$$\text{Hold}_{\max} \leq T_{CK, B} + T_{PD, \max} - T_{S, \min}$$

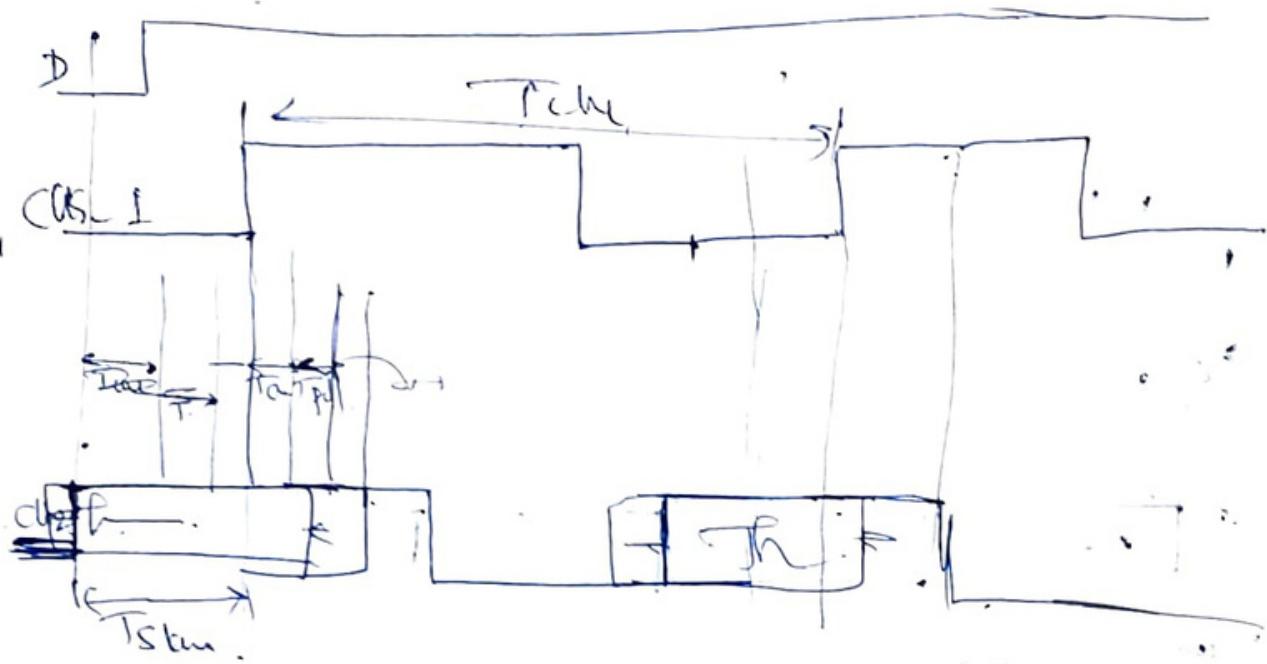
Calculation of setup time constraints with +ve Skew:



$$T_{CK} - T_{SKW} - T_{Setup} \geq T_{CQ, \min} + T_{PD, \max}$$

$$T_{CK} - T_{SKW} \geq T_{CQ, \min} + T_{PD, \max} + T_{Setup}$$

Calculation of hold time constraints



$$T_{\text{hold}} \rightarrow T_{\text{skew}} \leq T_{\text{clk_qmin}} + T_{\text{pd_min}}.$$

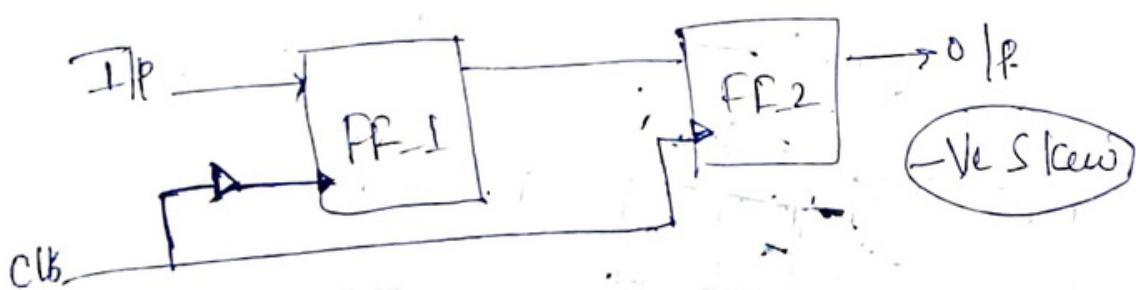
$$T_{\text{hold}} \leq T_{\text{clk_qme}} + T_{\text{pdmax}} + T_{\text{skew}}.$$

? Ex 2: Setup & hold time of FF are 5ns and 4ns

$$\cdot T_{\text{spl}} = 5 \text{ ns} \\ T_n = 1 \text{ ns}$$

$$, T_{\text{pd}} = 4 \text{ and } 7 \text{ ns.}$$

$$, T_{\text{gate}} = 2 \text{ and } 6 \text{ ns.}$$



$$- T_{\text{clock}} + T_{\text{skew}} \geq T_{\text{clk_dmax}} + T_{\text{pdmax}} + T_{\text{setup}}$$

$$T_{\text{hold}} \leq T_{\text{clk_qmax}} + T_{\text{pdmax}} + T_{\text{skew}}$$

$$\text{Talk} \rightarrow T_{\text{slow}} \geq T_{\text{talk-q(max)}} + T_{\text{pd(max)}} + T_{\text{Setup}}$$

$$T_{\text{talk}} - 6 \geq 7 + 0 + 5$$

$$T_{\text{talk}} \geq 7 + 0 + 5 + 6$$

$$T_{\text{talk}} \geq 18 \text{ ns} \quad f_2 \quad \frac{1}{T_{\text{talk}}} = \underline{\underline{55 \text{ MHz}}} \quad f < \underline{\underline{55 \text{ MHz}}}$$

$$T_{\text{hold}} \leq T_{\text{PLL-q(min)}} + T_{\text{pd(min)}} + T_{\text{Setup}}$$

$$T_{\text{hold}} \leq 4 + 0 + 2$$

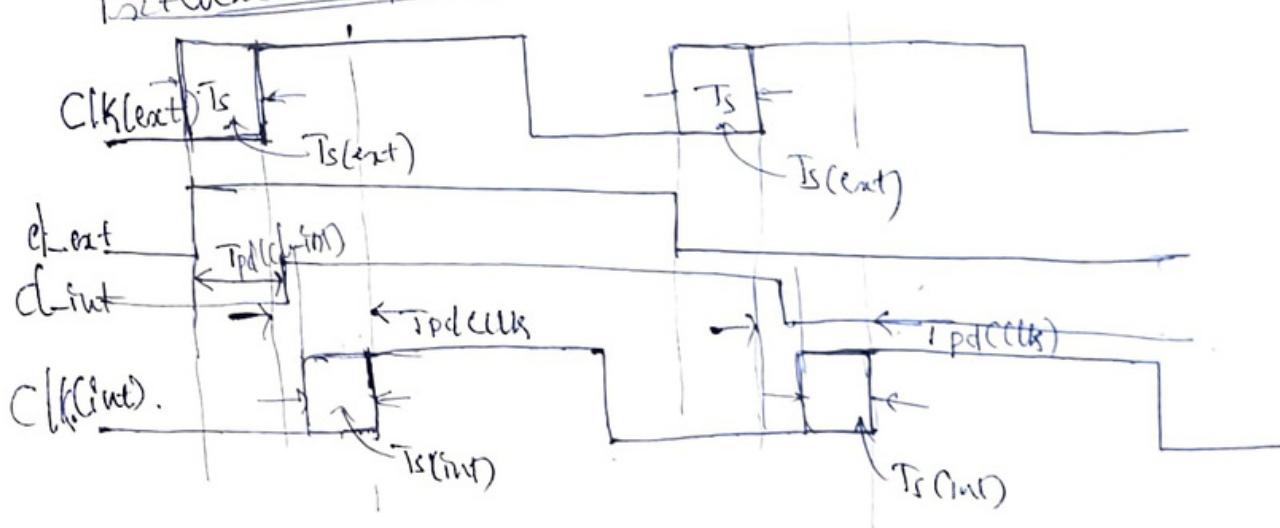
~~$$T_{\text{hold}} \leq 6 \text{ ns}$$~~

~~Setup~~

$$T_{\text{ins}} \leq 6 \text{ ns} \quad \text{No hold violation}$$

External setup time & hold time :-

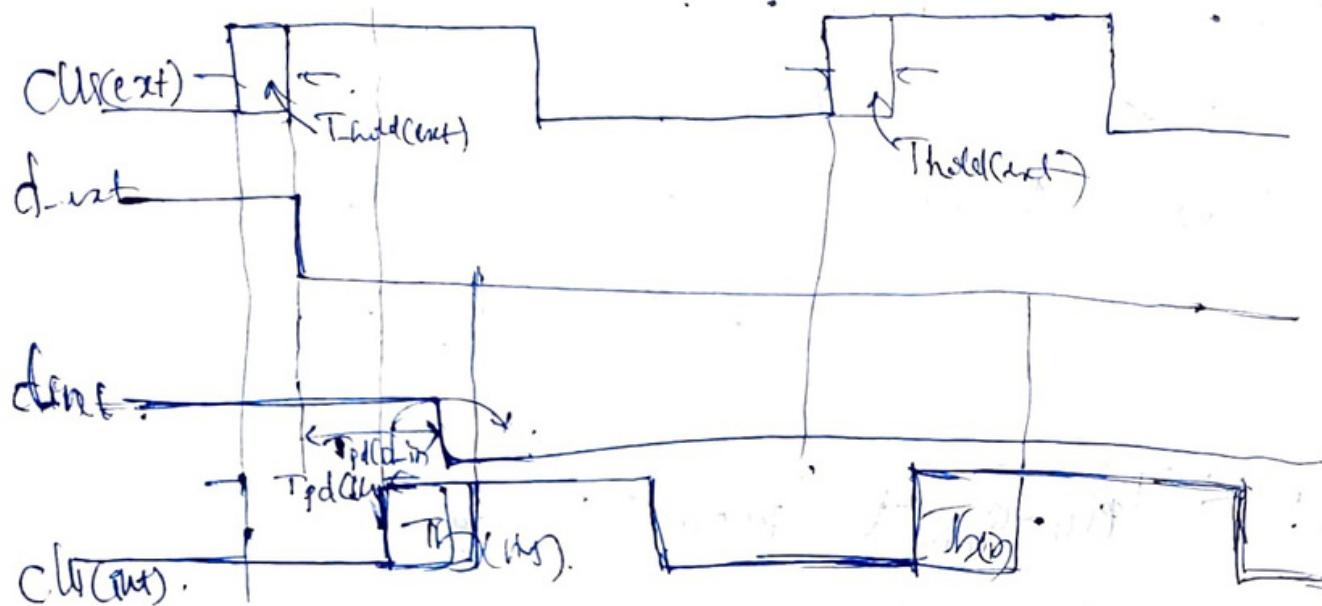
External setup time :-



$$T_{\text{setup(ext)}} + T_{\text{pd(Clk)}} - T_{\text{setup(int)}} \geq T_{\text{pd}(d_{\text{in}})}$$

$$\Rightarrow T_{\text{setup(int)}} \geq T_{\text{pd}(d_{\text{in}})} + T_{\text{pd}(Clk)} + T_{\text{setup}(d_{\text{in}})}$$

External Hold time :-



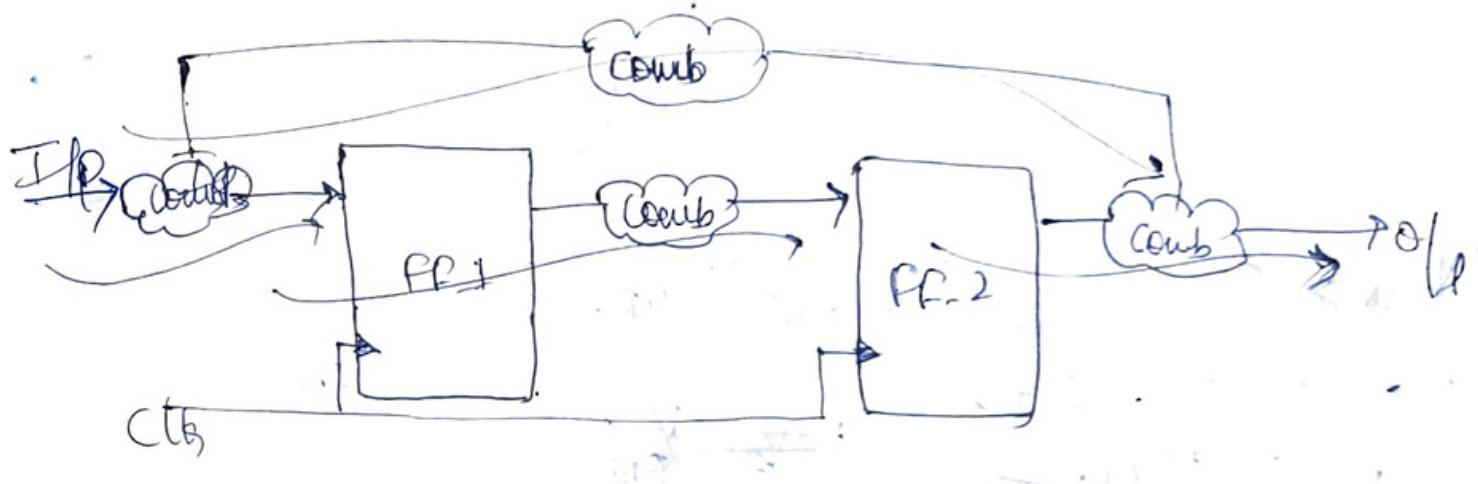
$$T_{pd}(cl_in) \geq T_{pd}(clk) + T_{hold(int)} - T_{hold(ext)}$$

$$T_{hold(ext)} \geq T_{pd}(clk) + T_{hold(int)} + T_{pd}(cl_in)$$

STA Procedure :-

Three steps in Static Timing Analysis :-

- ↳ Break the design into sets of timing paths.
- ↳ Calculate the delay of each path.
- ↳ Check all path delays to see if the given timing constraints are met.

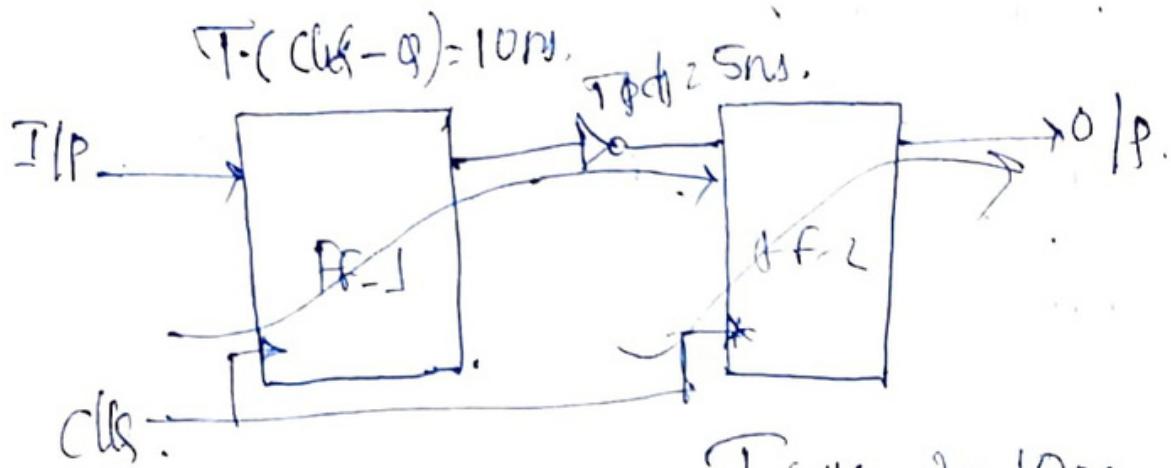


Types of timing path

- ↳ Primary I/P to Register path (PFs).
- ↳ Registers FF to primary O/P.
- ↳ Registers to Registers path.
- ↳ Primary I/P to primary O/P.

Ex 6.3:

Determine Maximum clock frequency.



$$T_{(Clk-Q)} = 10\text{ns}$$

$$T_{(\text{Setup})} = 2\text{ns}$$

$$T_{(\text{Hold})} = 2\text{ns}$$

$$\text{FF-1} \Rightarrow T_{Clk} \geq T_{Clk-Q(\max)} + T_{Qdt(\max)} + T_{\text{Setup}}$$

$$T_{Clk} \geq 10 + 5 + 2$$

$$T_{Clk} \geq \underline{17\text{ns}}$$

~~17 ns~~

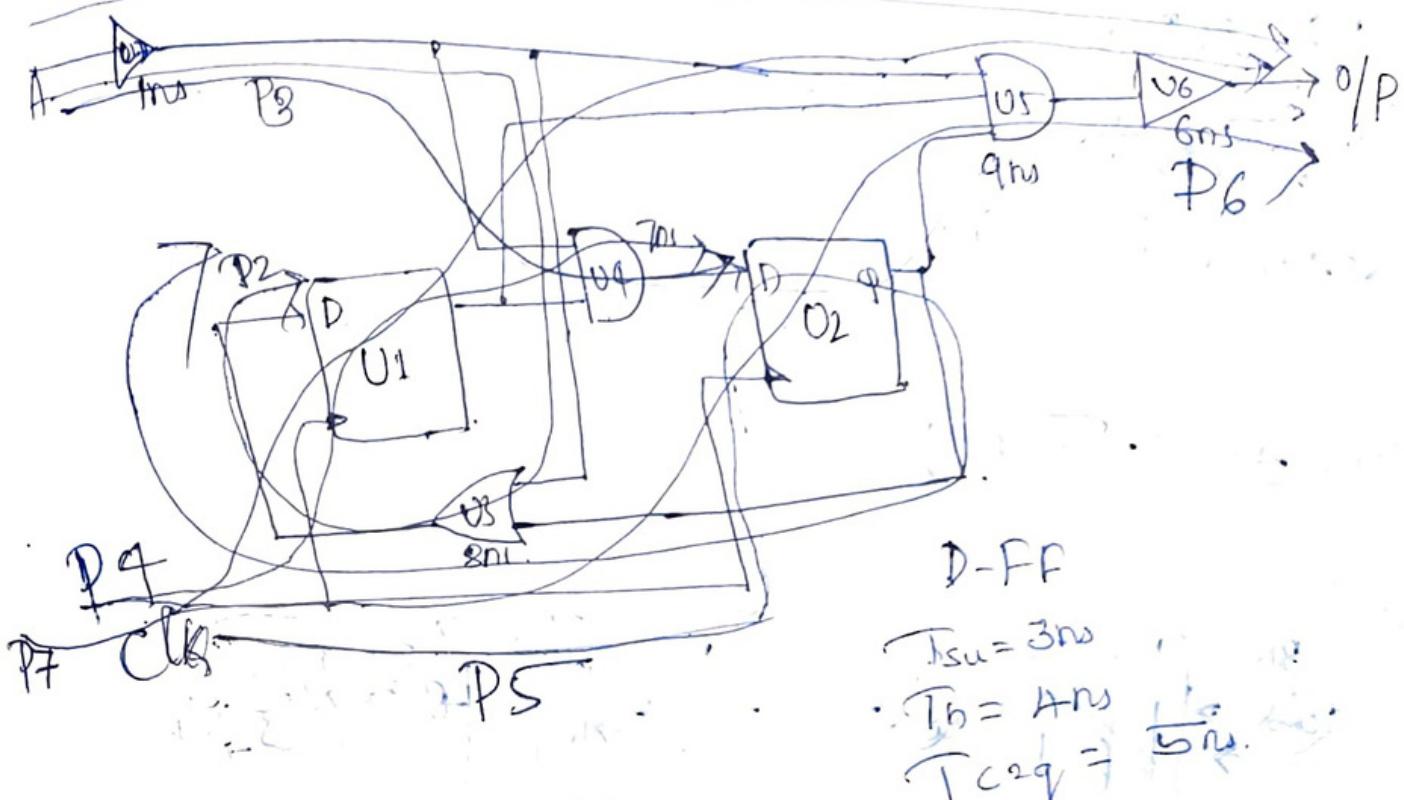
$$\text{FF-2} \Rightarrow T_{Clk} \geq T_{Clk-Q(\min)} + T_{Qdt(\min)} + T_{\text{Setup}}$$

$$T_{Clk} \geq 10$$

$$f = \frac{1}{17\text{ns}} = \underline{\underline{58.8\text{MHz}}}$$

Determine maximum clock frequency.

P1



D-FF

$$T_{su} = 3\text{ns}$$

$$T_b = 4\text{ns}$$

$$T_{C2q} = \frac{1}{5}\text{ns}$$

$P_1 - O/P$ to O/P Combinational path

$$\hookrightarrow U_7, U_5, U_6 \rightarrow T_{\text{comb}} = 1 + 9 + 6 = 16\text{nsec}$$

$P_2 = I/P$ to Register path: $U_7, U_3, U_1 = T_{\text{comb}} + T_{su} = 1 + 8 + 3 = 12\text{nsec}$

$P_3 = \text{Primary } I/P$ to Register path: $U_7, U_4, U_2 \rightarrow T_{\text{comb}} + T_{su} = 1 + 7 + 3 = 11\text{nsec}$

$P_4 = \text{Register to Register} - U_1, U_4, U_2 \rightarrow T_{\text{clk-q}} + T_{\text{comb}} + T_{su} = 5 + 7 + 3 = 15\text{nsec}$

$\cancel{P_5} = \text{Register to Register path} - U_2, U_3, U_1 \rightarrow T_{\text{clk}} + T_{\text{comb}} + T_{su} = 5 + 8 + 3 = 16\text{nsec}$

~~P5~~

$\cancel{P_6} = \text{Register to primary } O/P = U_2, U_5, U_6 \rightarrow T_{\text{clk-q}} + T_{\text{comb}} = 5 + 9 + 6 = 20\text{nsec}$

$\cancel{P_7} = \text{Register to primary } O/P = U_1, U_5, U_6 \rightarrow T_{\text{clk}} + T_{\text{comb}} = 5 + 9 + 6 = 20\text{nsec}$

Path P1 P2 P3 P4 P5 P6 P7

Delay 16 12 11 15 16 20 20

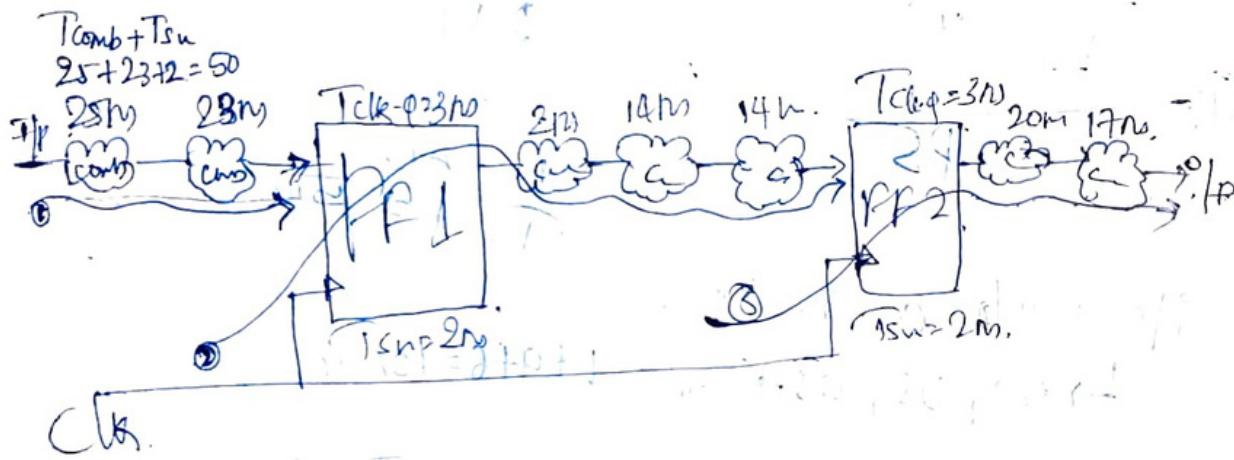
Methods to improve timing:-

→ Pipelining

→ Retiming

→ Time borrowing

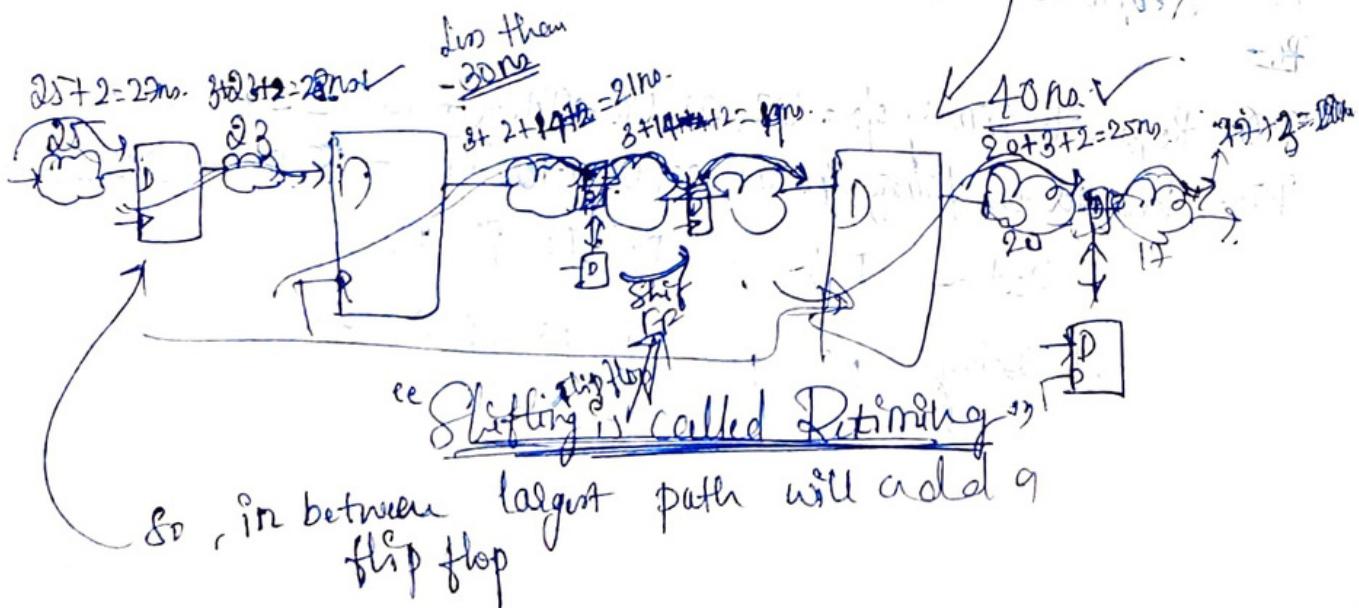
Pipelining Techniques:-



① $T_{Comb} + T_{Sw} = 25 + 23 + 2 = 50 \text{ ns}$

② $T_{Clock} + T_{Setup} + T_{Comb} = 30 + 2 + 25 = 57 \text{ ns}$

③ $T_{Clock} + T_{Setup} + T_{Comb} = 30 + 20 + 17 = 67 \text{ ns}$



Advantage and Disadvantages:-

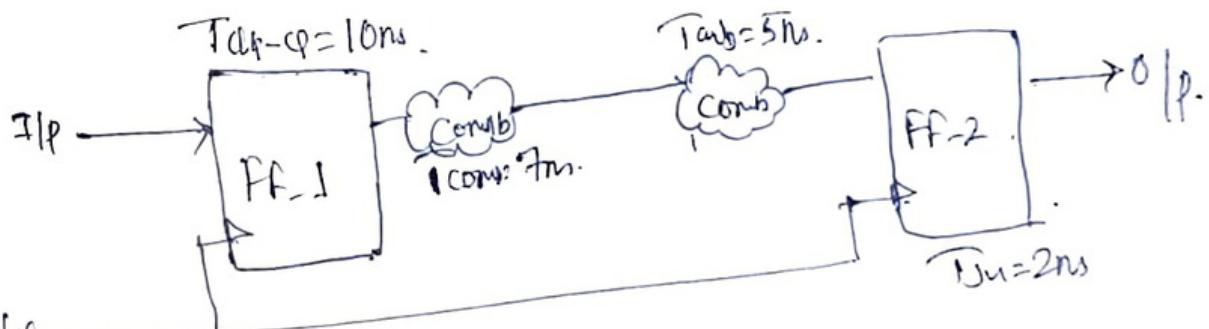
Advantages:-

- ↳ Higher throughput than Combinational System
- ↳ Different parts of the logic work with different set of I/Ps, so debug is easy.

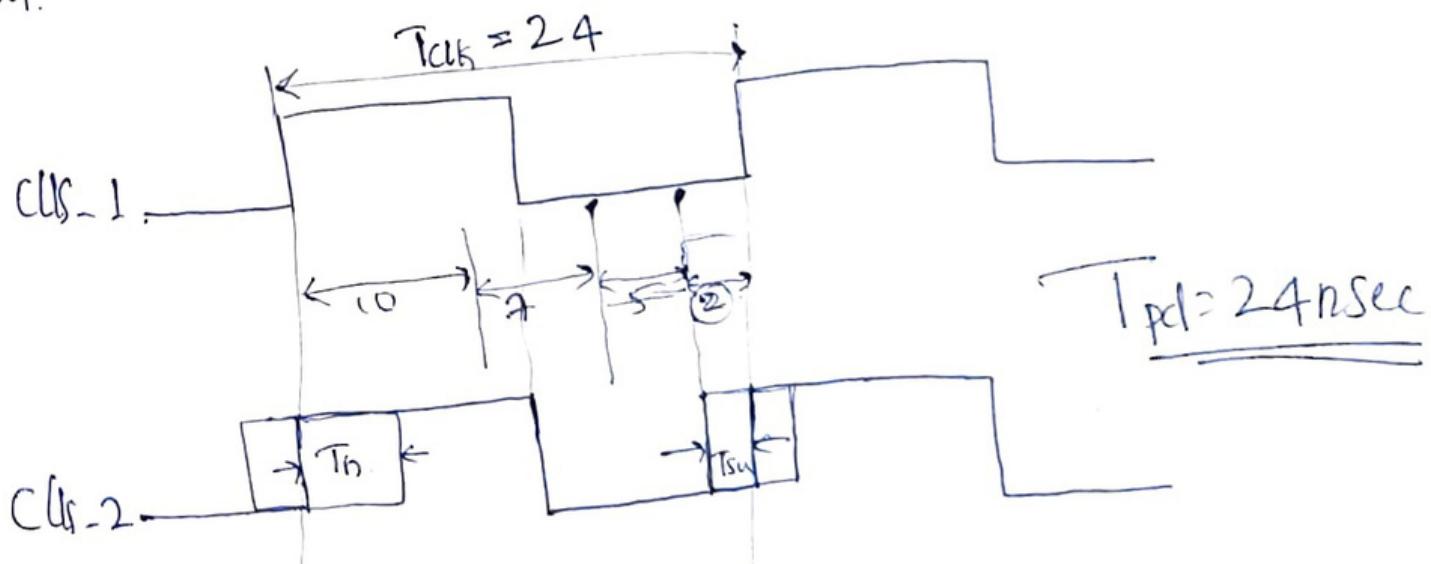
Disadvantages:-

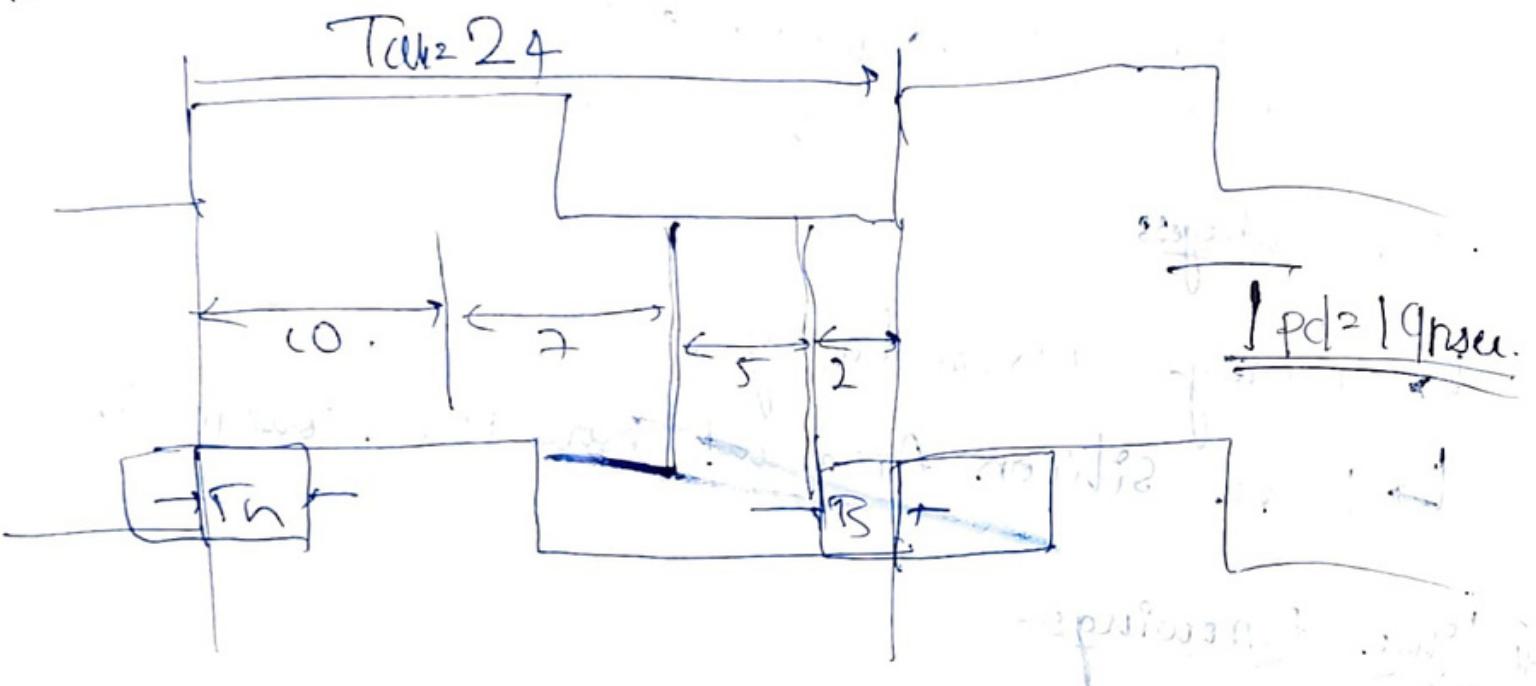
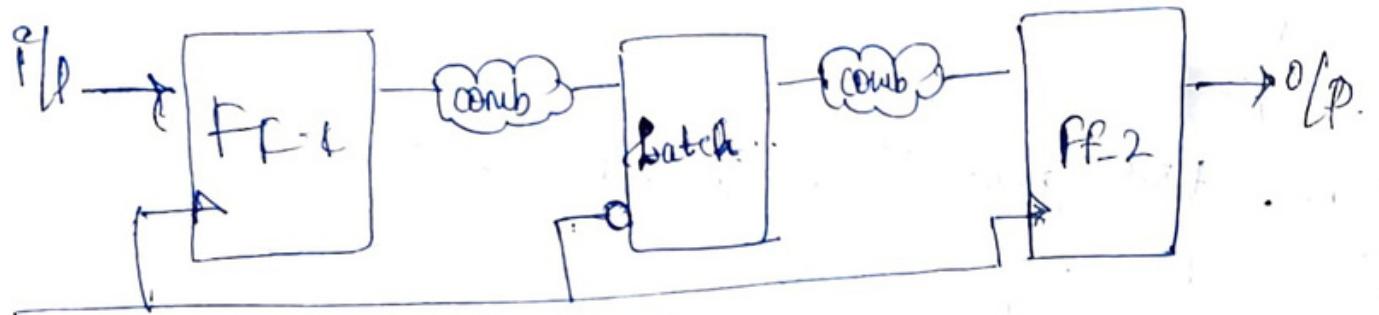
- ↳ Generally, increase latency.
- ↳ More silicon Area and More power consumption.

Time Borrowing:-



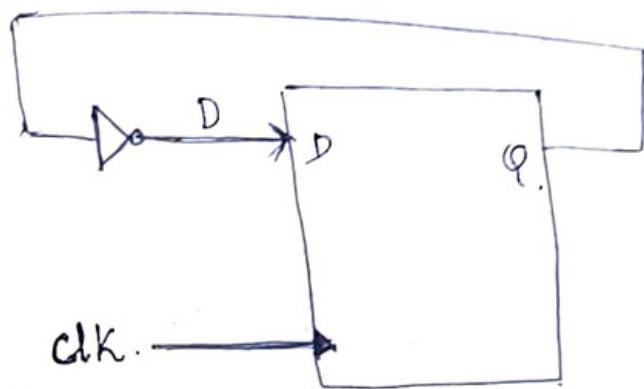
Clk.





Timing diagram for $T_{dw2} 24$ showing four stages with widths 1, 2, 5, and 7. The total width is labeled $T_{pd} = 19 \text{ nsec}$.

Timing diagram for $T_{dw2} 24$ showing four stages with widths 1, 2, 5, and 7. The total width is labeled $T_{pd} = 19 \text{ nsec}$.



$$T_{inv} = 5 \text{ ns}$$

$$T_{clock} = 8 \text{ ns}$$

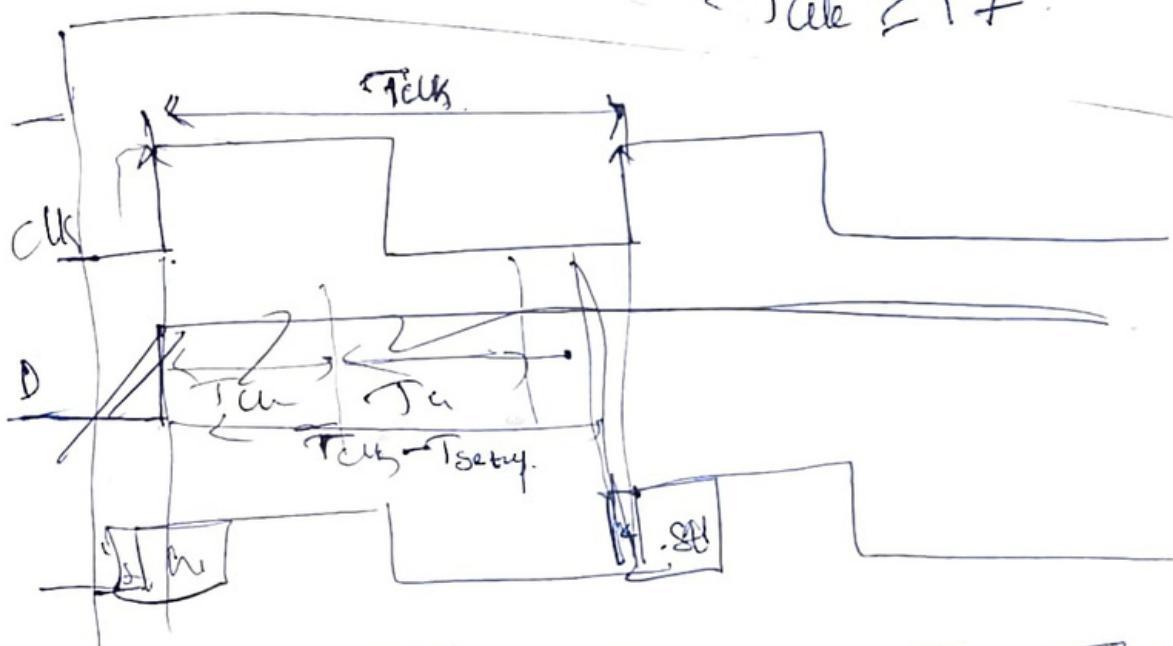
$$T_{su} = 4 \text{ ns}$$

$$T_h = 2 \text{ ns}$$

$$T_{clk} \geq T_{clock_q(max)} + T_{inv(max)} + T_{setup}$$

$$T_{clk} \geq 8 + 5 + 4$$

$$T_{clk} \geq 17$$



$$T_{clk} \geq T_{clock_q(max)} + T_{inv} + T_{setup}$$

$$8 + 5 + 4$$

$$T_{clk} \geq 17$$

$$f_2 = 1/T_2 = 1/f_1 = 58.82 \text{ MHz}$$

1. What Is Positive Slack?

The difference between required arrival time and actual arrival time is positive, then it is called as positive slack. If there is positive slack, the design is meeting the timing requirements and still it can be improved.

2. In Back-end Design Which Violation Has More Priority? Why?

In back-end design, Hold violation has more priority than Setup Violation. Because hold violation is related to data path and not depends on clock. Setup violation can be eliminated by slowing down the clock (Increasing time period of the clock).

3. What Is Negative Slack?

The difference between required arrival time and actual arrival time is Negative, then it is called as Negative slack. If there is negative slack, the design is not meeting the timing requirements and the paths which have negative slack called as violating paths. We have to fix these violations to make the design meeting timing.

4. What Is Slack?

The difference between Required Arrival Time and Actual Arrival Time is called as Slack. The amount of time by which a violation (Either setup or Hold) is avoided is called the slack.

5. How Can You Avoid Hold Time Violations?

By adding delays using buffers

By adding lockup-latches

6. What Is Static Timing Analysis(sta)?

Static timing analysis is a method for determining if a circuit meets timing constraints without having to simulate. So, it validates the design for desired frequency of operation, without checking the functionality of the design.

7. What Is Setup Time?

Setup time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is properly accepted on the clock edge.

Digital Communication Tutorial Continuous Integration 8.

8. What Is Hold Time?

Hold time is the amount of time after the clock edge that the input should be stable to guarantee it is properly accepted on the clock edge.

9.

9. What Is Setup And Hold Time Violations?

Violating above setup and hold time requirements is called setup and hold time violations. If there is setup and hold time violations in the design does not meet the timing requirements and the functionality of the design is not reliable. STA checks this setup and hold violations.

10. How Can You Avoid Setup Time Violations? Play with clock (Useful) skew.

Redesign the flip flops to get lesser setup time

The combo logic between flip flops should be optimized to get minimum delay

Tweak launch flip-flop to have better slew at the clock pin, this will make a launch flip-flop to be fast thereby helping fixing setup violations.

Setup time constraint

$$T_{\text{setup_time}} + T_{\text{clock_Q}} + \text{delay} \leq T_{\text{minimum}}$$

Which says the overall sum of flop setup time and clock to Q delay and other delays such as jitter must be less than or equals to the minimum clock time period.

Hold time constraint

$$T_{\text{hold_time}} \leq T_{\text{clock_Q}} + \text{delay}$$

The hold time must be less than or equals to the sum of the clock to Q delay and other delays such as clock jitter.

Note:

If a situation comes to have a choice between setup violation fix and hold violation fix after the chip design is completed and fabricated, then it is a better option to chose hold violation fix.

The reason is to fix the setup time violation we need to modify T_{minimum} . As we saw above setup time constraint involves clock time period parameter which decides the overall chip speed which cannot be modified after the chip come from the foundry.

Let us discuss STA Problems

STA Problem 1

Given the following flip-flop circuit with a delay dly between input and output. And the clock CLK is applied to the flip flop.

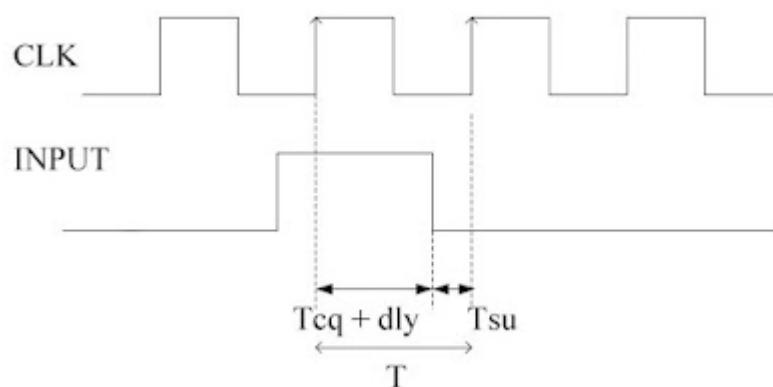
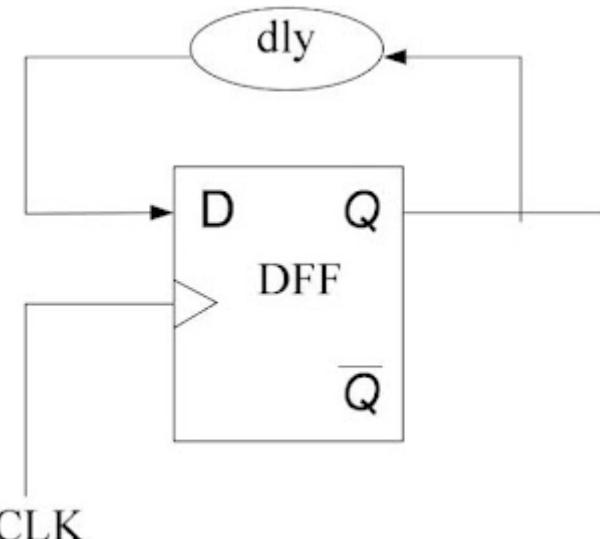
- What will be the expression for the minimum time period (T_{minimum}) or maximum clock frequency (f_{maximum})? Derive it by considering clock to Q delay ($T_{\text{clock_Q}}$), setup time ($T_{\text{setup_time}}$), and hold time ($T_{\text{hold_time}}$) of the flipflop.
- If the value of $dly = 1\text{ns}$, and given three flipflop values as per the table below, Which of the flip flops are a good fit when the minimum required time period is 5ns, 8ns, and 15ns.

Flip Flops	FF1	FF2	FF3
$T_{\text{clock_Q}}$	5	6	8
$T_{\text{setup_time}}$	3	4	2

Thold_time	2	1	1
------------	---	---	---

STA Problem Solution

a. From the above-given circuit



1. The output Q will be changed only after the clock event and till the clock to Q delay elapsed.

2. Also the input data has an external delay of dly will add up to Tclock_Q
So the expression will be for minimum clock period will be as below,

$$T_{\text{minimum}} \geq T_{\text{setup_time}} + T_{\text{clock_Q}} + dly$$

b. By using the above T_{minimum} expression let us calculate the minimum time periods for flip flops FF1, FF2, and FF3 respectively.

$$T_{\text{minimum}} \text{ for FF1} = T_{\text{setup_time of FF1}} + T_{\text{clock_Q of FF1}} + dly$$

$$T_{\text{minimum}} \text{ for FF1} = 3\text{ns} + 5\text{ns} + 1\text{ns}$$

$$T_{\text{minimum}} \text{ for FF1} = 8\text{ns}$$

$$T_{\text{minimum}} \text{ for FF2} = T_{\text{setup_time of FF2}} + T_{\text{clock_Q of FF2}} + dly$$

$$T_{\text{minimum}} \text{ for FF2} = 6\text{ns} + 4\text{ns} + 1\text{ns}$$

$$T_{\text{minimum}} \text{ for FF2} = 10\text{ns}$$

$$T_{\text{minimum}} \text{ for FF3} = T_{\text{setup_time of FF3}} + T_{\text{clock_Q of FF3}} + dly$$

$$T_{\text{minimum}} \text{ for FF3} = 8\text{ns} + 2\text{ns} + 1\text{ns}$$

$$T_{\text{minimum}} \text{ for FF3} = 10\text{ns}$$

For the time period requirement of 5ns none of the above flops can be used, and for 8ns flop FF1 alone can be used. Whereas for the time period requirement of 15ns any one of the above flip flops can be used.

STA Problem 2

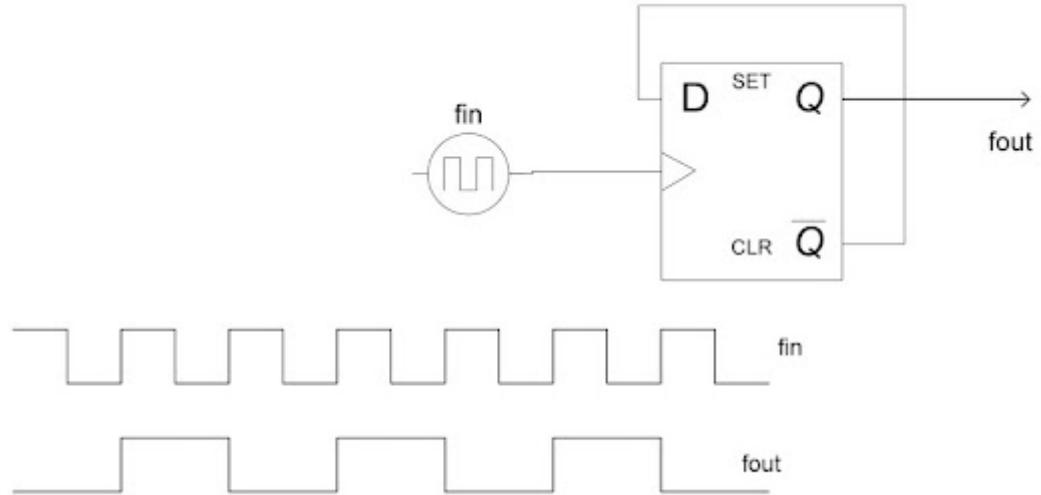
Given the data setup time of the flop is 6ns, the hold time of the flop is 2ns, and the clock to Q delay is given as 10ns.

- Calculate the minimum clock period required to handle the circuit by drawing a digital logic circuit for function clock frequency divided by 2.
- Also determine the status of hold time violation and give a proper reason.

STA Problem Solution

- The logic diagram for clock frequency divided by 2 would be as shown below.

The waveform of fin and fin/2 are as shown below



By using above discussed Tminimum expression let us calculate the minimum time period,

$$T_{\text{minimum}} \geq T_{\text{setup_time}} + T_{\text{clock_Q}} + \text{dly}$$

$$T_{\text{minimum}} \geq 6\text{ns} + 10\text{ns} + 0$$

$$T_{\text{minimum}} \geq 16\text{ns}$$

$$f_{\text{maximum}} \geq 1/16\text{ns}$$

$f_{\text{maximum}} \geq 62.5\text{MHz}$ is the maximum possible frequency of operation for an above circuit with given timing requirements.

- Let us check for the hold violation, we have the hold time constraint as discussed at the starting of this article,

$$T_{\text{hold_time}} \leq T_{\text{clock_Q}} + \text{delay}$$

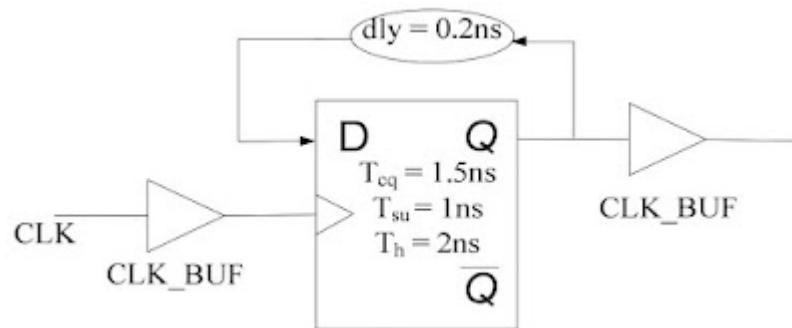
$$2\text{ns} \leq 10\text{ns} + 0$$

$2\text{ns} \leq 10\text{ns}$

As we are satisfying the above condition there is no hold time violation in the circuit as per the given timing requirements.

STA Problem 3

Consider the circuit diagram and the timing requirement as shown for the flip flop. Two clock buffers are added at the clock pin and the output pin. Also a combination delay of $dly = 0.2\text{ns}$ in the input to the output path.



Check for any violation in the circuit with the given timing requirements, and If there any violation then what would be the updated value of dly ? Also is there any effect on $f_{maximum}$ due to added clock buffers.

STA Problem Solution

1. Let us check for the hold violation in the circuit. We know the constraint to be checked that is,

$$\text{Thold_time} \leq T_{clock_Q} + \text{delay}$$

$$2\text{ns} \leq 1.5\text{ns} + 0.2\text{ns}$$

$2\text{ns} \leq 1.7\text{ns}$, as the condition fails we can say there is a hold time violation in the circuit.

2. To remove the above hold violation we can vary the dly to

$$\text{Thold_time} \leq T_{clock_Q} + \text{delay}$$

$$dly \geq \text{Thold_time} - T_{clock_Q}$$

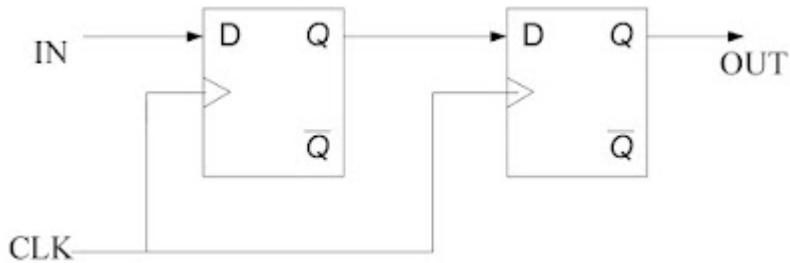
$$dly \geq 2\text{ns} - 1.5\text{ns}$$

$dly \geq 0.5\text{ns}$ The dly must be greater than or equals to 0.5ns to avoid hold violation in the above circuit.

3. The clock buffer delays do not affect the $f_{maximum}$ of the circuit.

STA Problem 4

Consider the below flip flop pair logic diagram and the table with three different flip flops FF1, FF2, and FF3 with their timing specifications.



Which combination of flip flops should be replaced in the below flip flop pair to get the maximum clock frequency of operation.

Flip Flops	FF1	FF2	FF3
Tclock_Q	5	6	8
Tsetup_time	3	4	2
Thold_time	2	1	1

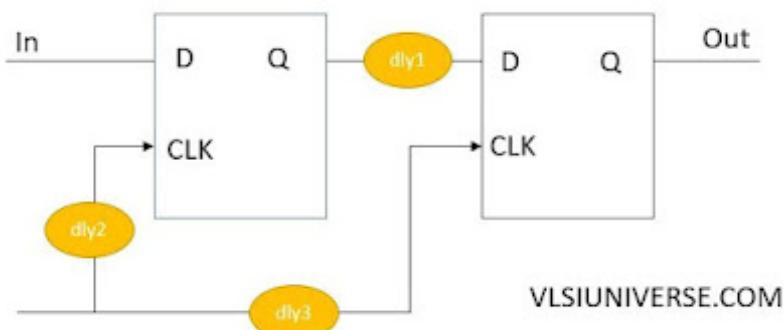
STA Problem Solution

The hint here is to replace the first flop place with the flip flop which has the minimum clock to Q (Tclock_Q) delay and replace the second flop place with the flip flop having the minimum setup time (Tsetup_time) among all of them.

So FF1 and FF3 flip flop pairs can be used in the logic circuit to have the maximum frequency of operation.

STA Problem 5

Consider the below logic circuit with delays dly1, dly2, and dly3 at different places shown and determine the constraints to avoid setup time and hold violation.



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Also for the given timing specifications calculate the maximum clock frequency of operation or minimum required clock time period.

dly2 = 0.5ns and dly3 = 3ns. and

Tclock_Q1 = Tclock_Q2 = 2.5ns.

Tsetup_time1 = Tsetup_time2 = 2ns

Thold_time1 = Thold_time2 = 1ns

STA Problem Solution

a. Assume timing parameters for FF1 and FF2 as Tclock_Q1, Tsetup_time1, Thold_time1 and Tclock_Q2, Tsetup_time2, Thold_time2 respectively.

Let us assume positive clock skew and calculate delta = dly2 - dly3.

The setup time constrain when a pair of flops circuits is given will be,

$$| \quad T_{\text{minimum}} \geq T_{\text{setup_time2}} + T_{\text{clock_Q1}} + dly_1 - \text{delta}$$

**Note the setup time of the second flip flop will be considered here.

And the hold time constraint for the same will be,

$$| \quad Thold_{\text{time2}} \leq T_{\text{clock_Q1}} + dly_1 - \text{delta}$$

**Note that the hold time of the second flip flop is considered.

b. We must calculate delta and dly1 values first

$$\text{delta} = \text{delta}_2 - \text{delta}_3$$

$$\text{delta} = 3\text{ns} - 1\text{ns}$$

$$\text{delta} = 2.5\text{ns}$$

and the dly1 value by considering there is no hold violation. therefore

$$Thold_{\text{time2}} \leq T_{\text{clock_Q1}} + dly_1 - \text{delta}$$

$$dly_1 \geq Thold_{\text{time2}} - T_{\text{clock_Q1}} + \text{delta}$$

$$dly_1 \geq 1\text{ns} - 2.5\text{ns} + 2.5\text{ns}$$

$$dly_1 \geq 1\text{ns}$$

Now by using setup time constraint we can compute minimum required clock period,

$$T_{\text{minimum}} \geq T_{\text{setup_time2}} + T_{\text{clock_Q1}} + dly_1 - \text{delta}$$

$$T_{\text{minimum}} \geq 2\text{ns} + 2.5\text{ns} + 1\text{ns} - 2.5\text{ns}$$

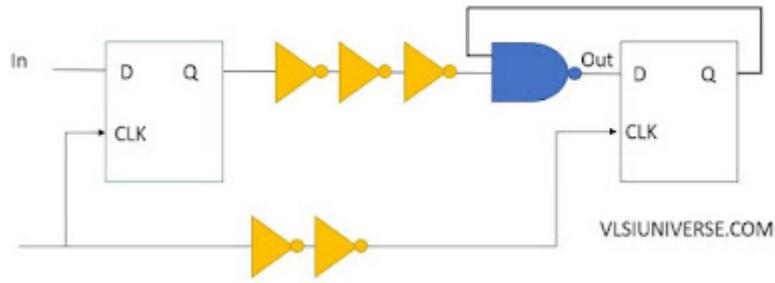
$$T_{\text{minimum}} \geq 3\text{ns}$$

therefore

fmaximum = 1/3ns = 333.33MHz is the **maximum frequency of operation**.

STA Problem 6

Consider the following circuit and given timing specifications to check whether there are any violations. If there is any violation vary the delay values accordingly and calculate the required minimum clock period.



Given timing specifications,

$$T_{clock_Q1} = T_{clock_Q2} = 2\text{ns}$$

$$T_{setup_time1} = T_{setup_time2} = 3\text{ns}$$

$$T_{hold_time1} = T_{hold_time2} = 6\text{ns}$$

The inverters have a delay of 1ns each and the NAND gate propagation delay is given as 2ns.

STA Problem Solution

After comparing this problem with the previous one we can observe that,

$$dly1 = 3 \text{ NOT gate delay} + 1 \text{ NAND gate delay}$$

$$dly1 = 1\text{ns} + 1\text{ns} + 1\text{ns} + 2\text{ns}$$

$$dly1 = 5\text{ns}$$

$$dly2 = 2 \text{ NOT gate delay}$$

$$dly2 = 2\text{ns}$$

$$dly3 = 0\text{ns}$$

$$\text{delta} = dly2 - dly3$$

$$\text{delta} = 2\text{ns} - 0\text{ns}$$

$$\text{delta} = 2\text{ns}$$

Substituting all the values in the setup time constraint equation,

$$T_{minimum} \geq T_{setup_time2} + T_{clock_Q1} + dly1 - \text{delta}$$

$$T_{minimum} \geq 3\text{ns} + 2\text{ns} + 5\text{ns} - 2\text{ns}$$

$$T_{minimum} \geq 8\text{ns}$$

$$f_{maximum} \leq 1/8\text{ns}$$

$f_{maximum} \leq 125\text{MHz}$ is the maximum possible operating frequency for the above circuit as per the given timing constraints.

Solve as many possible problems on STA to get confidence in the concept. Leave a comment if you are not getting any of the above solutions or for any doubts.