

FPGA NOTES



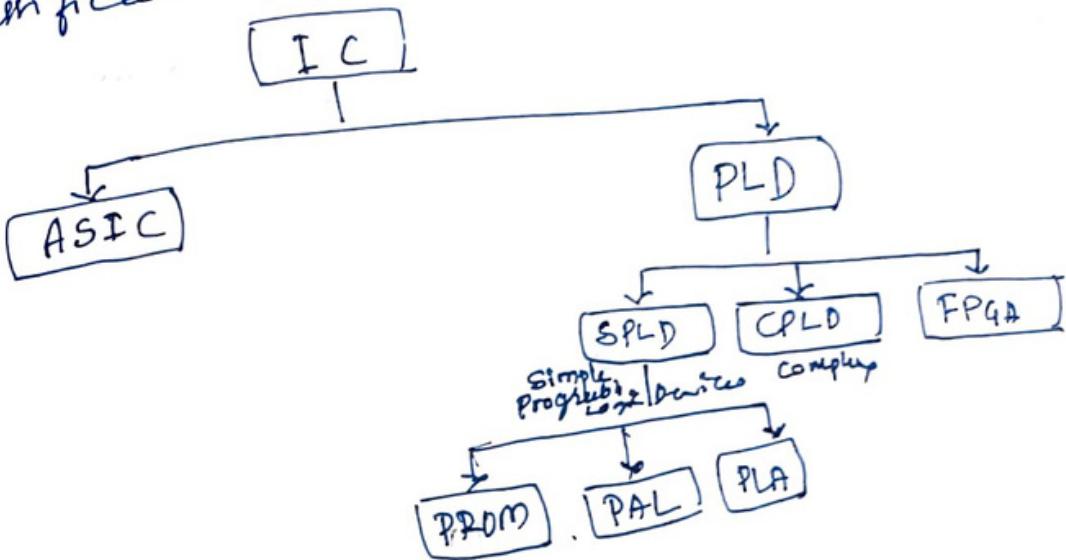
Jairaj Mirashi
Design Verification
Engineer



FPGA

FPGA Based System Design

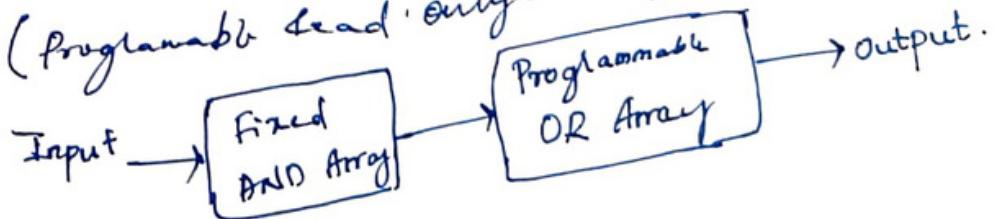
Classification of IC's.



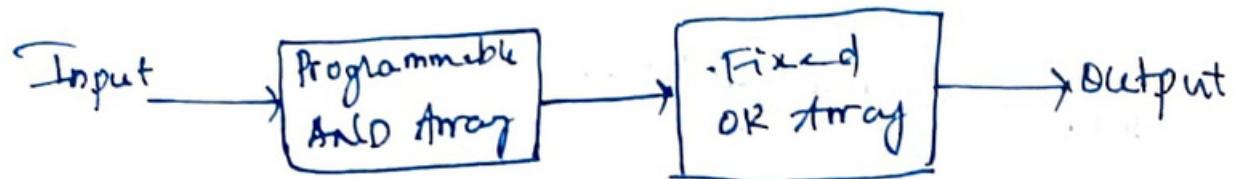
- # Why we need to use FPGA?
 - Once after the fabrication of VLSI chips, we cannot do any alteration to the design.
 - If there is any bug in the design, the fabricated chip is a waste.
 - It's a wastage of money, time, manpower.
 - If it is working properly in FPGA, we can think about converting into a hardware (VLSI chip)

Programmable Logic Devices (PLD)

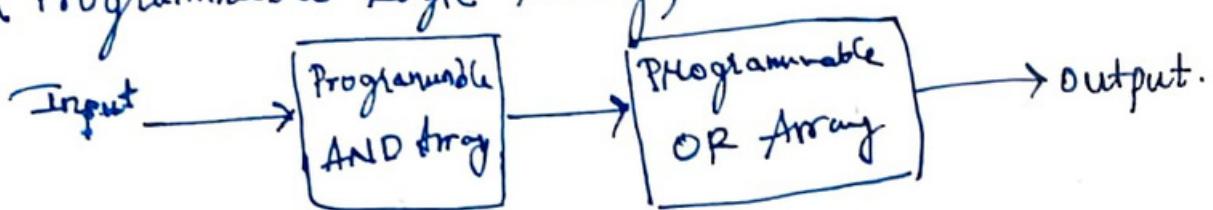
PROM (Programmable read-only memory)



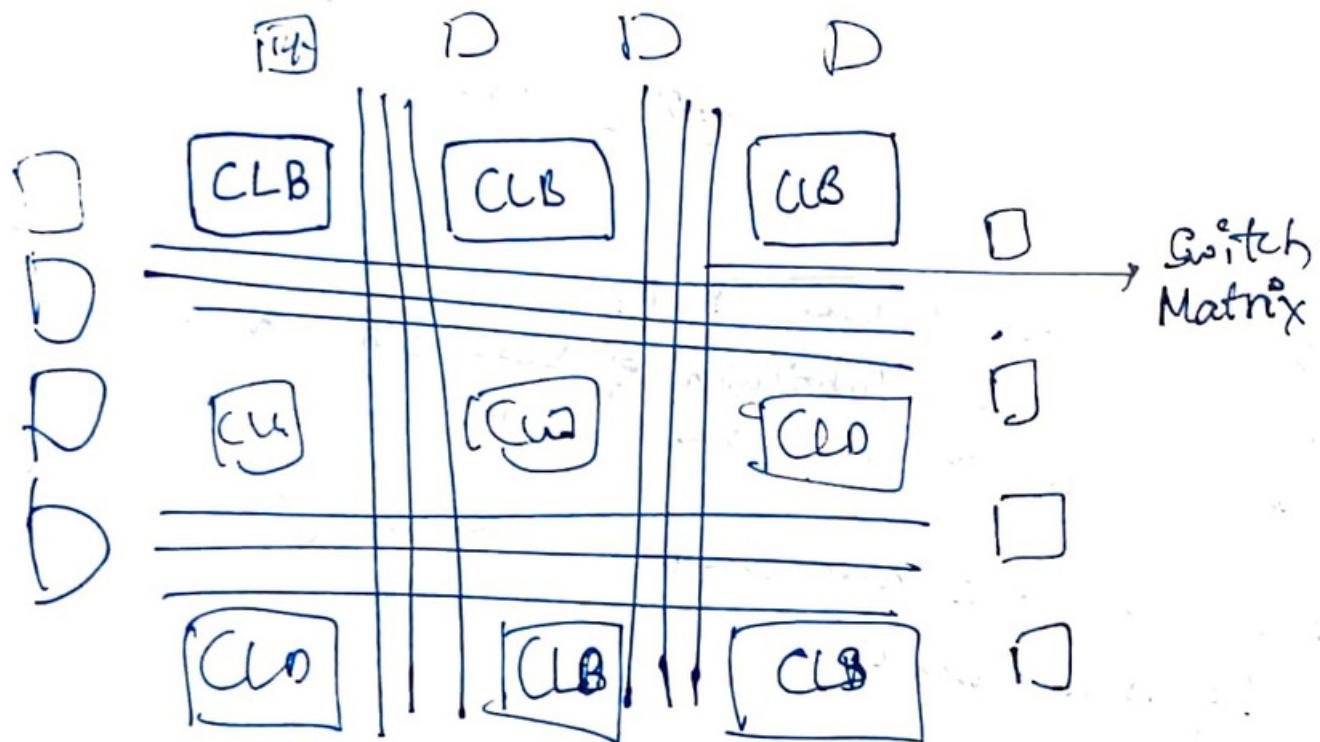
PAL (Programmable Array Logic)



PLA (Programmable Logic Array)



FPGA Block Diagram :-



- Configurable Logic Block

- I/O Block

- Switch Matrix

FPGA Fabric:

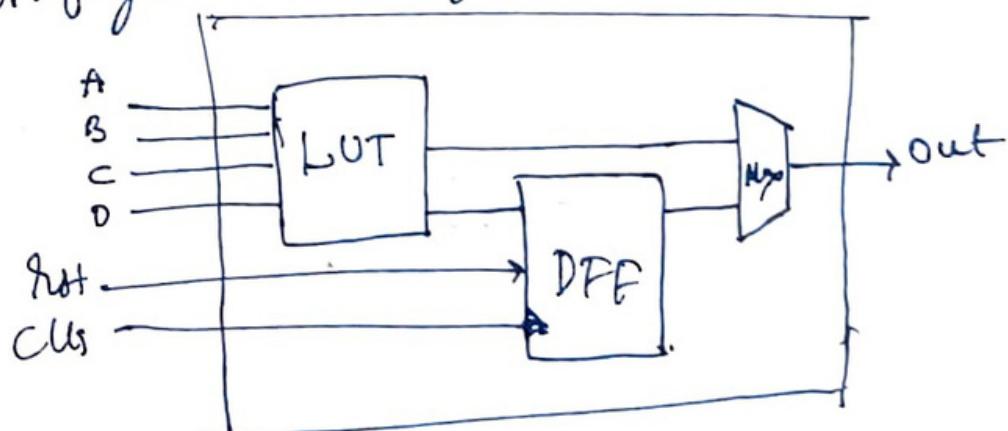
- Every FPGA consists of following blocks:
 - ↳ Configurable Logic Block: It is made up of
 - ↳ Logic element (LE) Flip-flop + I/P LUT (Combinational logic)
 - ↳ Embedded logic (Distributed RAM, multipliers...etc)
 - ↳ Other logic - fast carry logic, PS/F6 mux, etc.
- Input Output Blocks:
 - ↳ Logic blocks communicate with external world, by means of programmable IO

Programmable Interconnects:

- Programmable Interconnects:
 - ↳ Connects internal logic as well as I/O blocks.

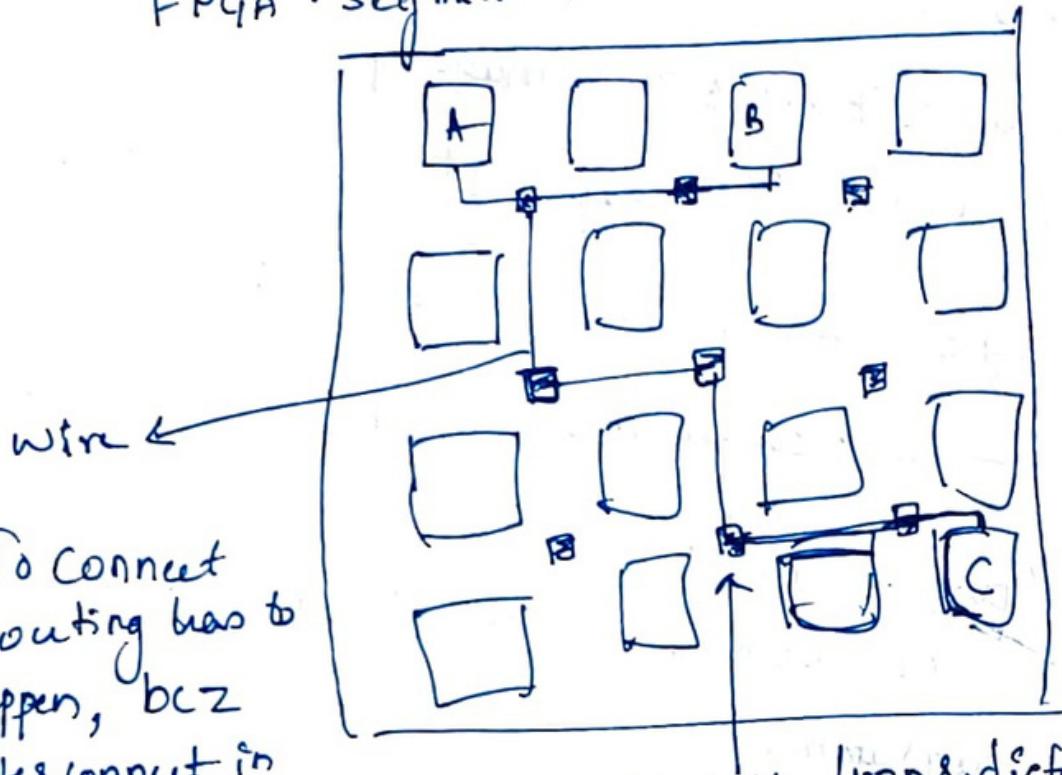
Architecture of FPGA:

- Configurable logic Block.



Programmable Interconnect:

FPGA · Segmented Interconnect · Architecture

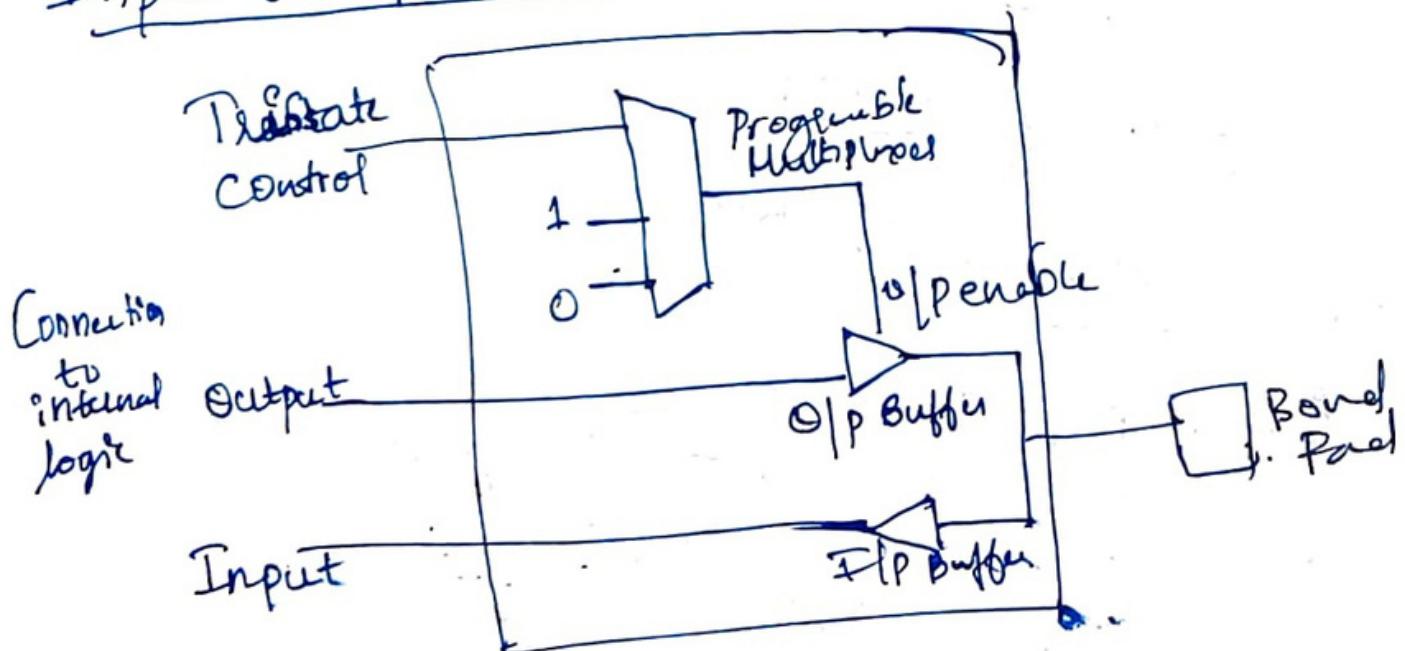


To connect
routing has to
happen, bcz
interconnect in
FPGA is Segment type

(Lines are not
continuous)

Variable / Unpredictable Delay

Input Output Block:



SRAM based FPGA:

- The configuration memory is volatile & re-programmable.
- Requires external non-volatile memory to store the bit-stream due to the volatile nature of internal configuration memory.
- Implements look up tables (LUTs) in logic blocks to implement combinational functionality, along with flip-flops.
- Xilinx, Lattice, Atmel vendors major in SRAM based FPGAs

Anti-fuse programmed FPGA

- Anti-fuse programmed FPGAs, non-volatile in nature.
- One time programmable FPGAs, non-volatile in nature.
- Switches are normally open and are of anti-fuse type.
- In its unprogrammed state, an antifuse has such a high resistance that it may be considered an open circuit.
- Connection is established by passing programming current through the switches, to fuse (close) them.
- Atmel, Microsemi, vendors major in antifuse FPGAs.

Flash Based FPGA :-

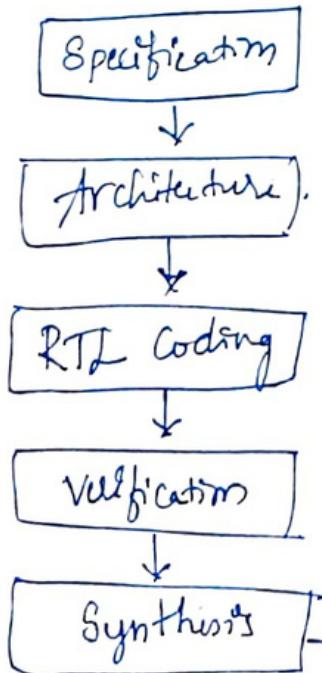
- FLASH FPGAs are non volatile like antifuse FPGAs, but they are also reprogrammable like SRAM FPGAs.
- Xilinx, Lattice. Vendor major in flash based FPGAs.

FPGA Vs ASIC :-

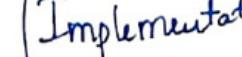
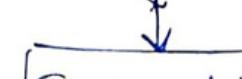
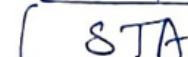
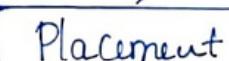
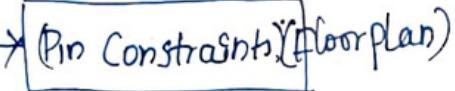
FPGA	ASIC
Field Programmable Gatearray	Application Specific Integrated Circuits
Faster Time to Market	Slower Time to Market
Reprogrammable	Specific Application
Relatively Slower than ASIC (MHz)	Faster than FPGA (GHz)

FPGA Design Flow:

FRONT END



Back END



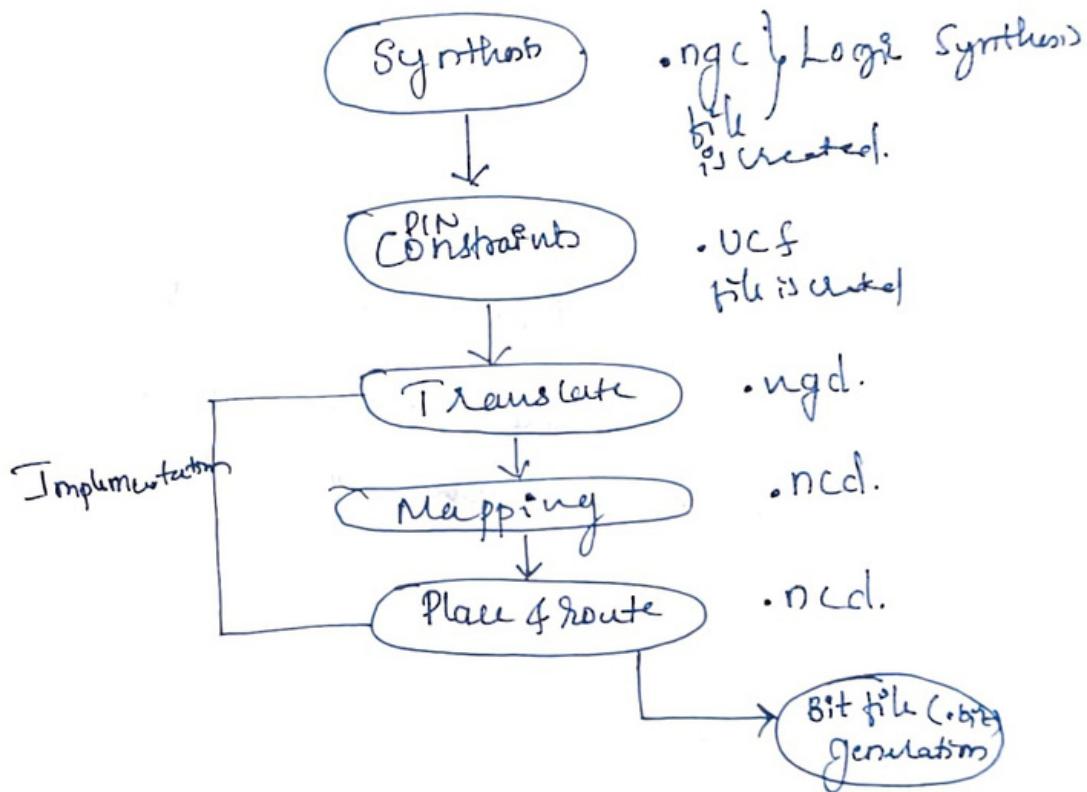
~~part~~ Files Generated during the FPGA Design Flow.

ngc: native generic constraint.

ucf: user constraint file.

ngd: native generic database.

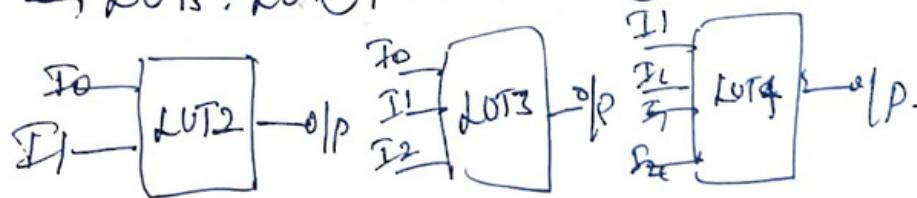
ncd: native circuit description.



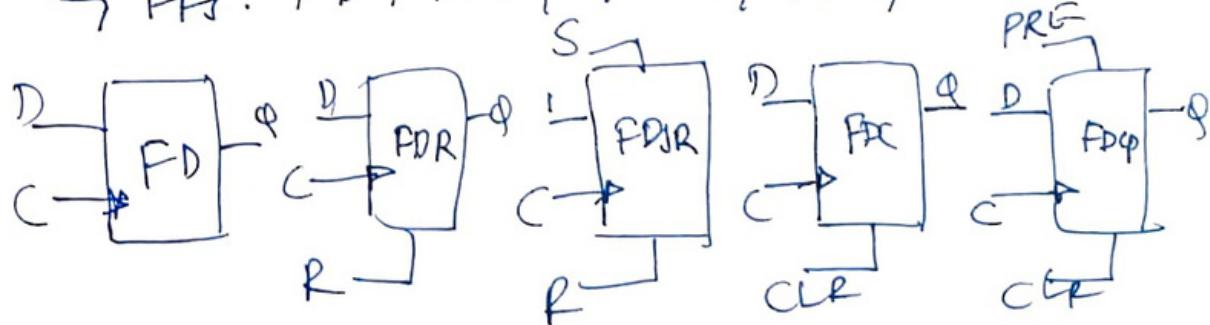
Design Implementation on FPGA :

→ FPGA Basic primitives.

↳ LUTs: LUT₂, LUT₃, LUT₄.



↳ FFs: FD, FDR, FPR, FDC, FCCP.



Xilinx Spartan 3 Series FPGA:

Xilinx · Spartan 3 Features:

↳ Spartan 3 is the first FPGA produced on the Advanced 90nm process technology.

↳ 4 Input LUT

↳ It is Industry's lowest cost FPGA.

↳ Packages available for the Spartan-3 family:

↳ TQFP44, PQ208, FT256 and FG456.

Thin
Quad
Structure

Plastic
Q's

Total No. of PDNs supported.

↳ Software available to support the Spartan-3 family: Xilinx ISE v 5.2i and higher version.

SPARTAN 3 FPGA:

Σ C2INP
8Pins
XC3S500E™
PQG208 PG41141
D43099 D43099
AC

Device type → XC3S50 → Speed grade → PQ → package Type (Plastic quad) → 208C → Temperature Range

↓
No. of
PDNs

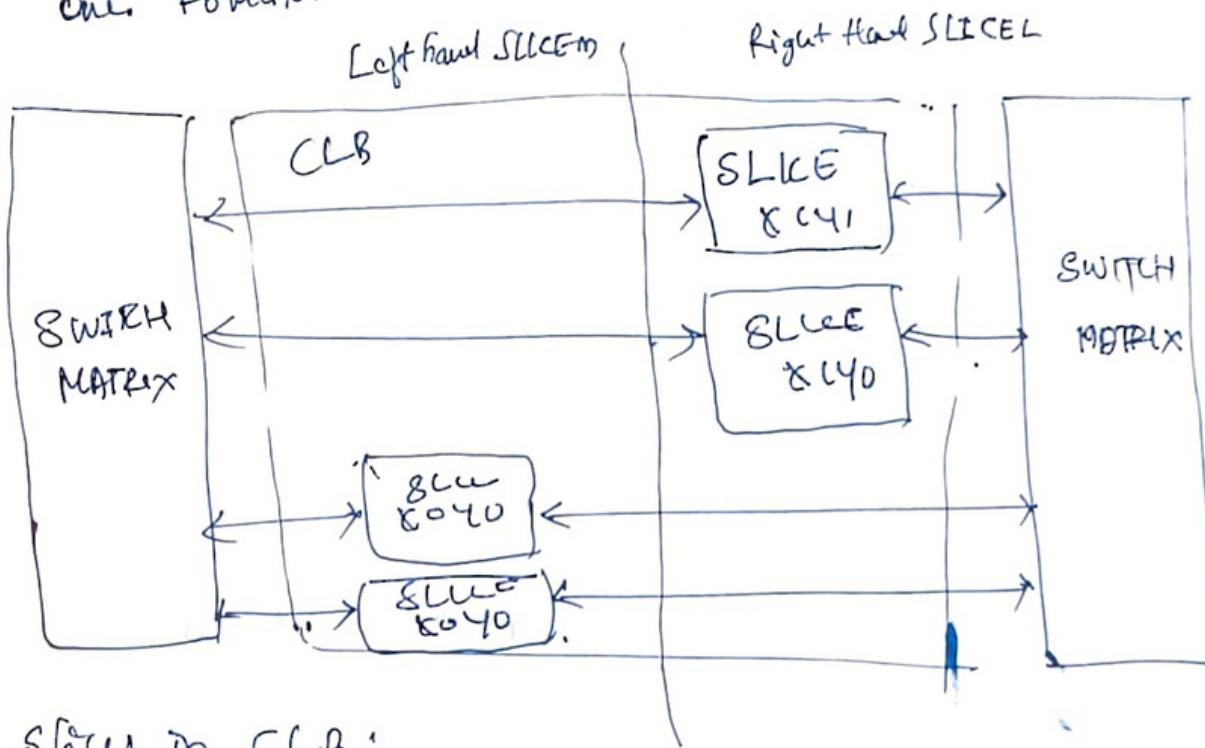
Architectures:

Configurable Logic Blocks:-

→ Configurable Logic Block.

↳ Each CLB contains four slices

↳ Each slice contains two Look-up Tables (LUTs) to implement logic, two dedicated storage elements that can be used as D flip-flops, one F5MUX & one F6MUX.



Slice in CLB:

→ SLICE have the following elements.

↳ Two 4-Input LUT

↳ Two Storage elements (D FF)

↳ Two dedicated mux (eg) P5MUX, F6MUX

↳ CARRY and arithmetic logic

→ SLICEM have the following elements apart from the basic logical elements

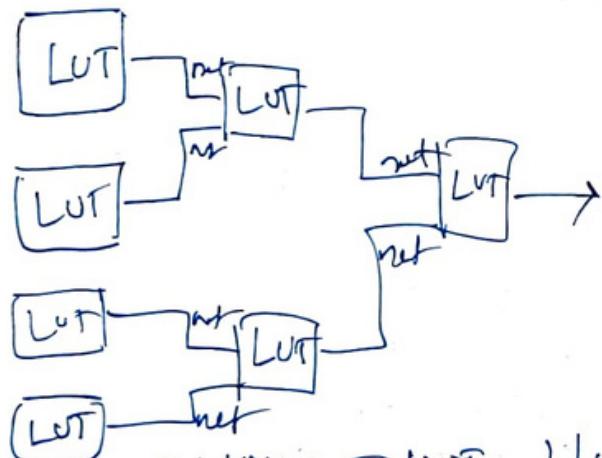
↳ Two 16x1 distributed RAM blocks, RAM16

↳ Two 16-bit shift registers, SRL16

↳ Two 16-bit shift registers, SRL16

- # Dedicated Multiplexers
- These are special multiplexers which has zero wiring delay compared to LUTS.
 - The largest mux supported by a LUT of dedicated mux is 2:1 mux.
 - The main advantage of Dedicated mux is that they can be used to reduce the logic to 1 level.

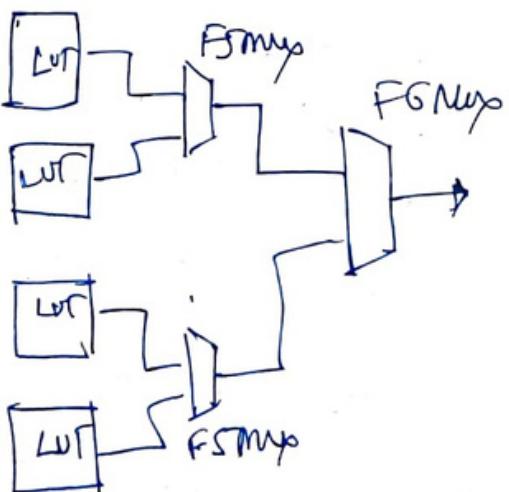
8:1 Mux using LUTS:



8:1 Mux, 7 LUTs, 3 Levels of Logic.

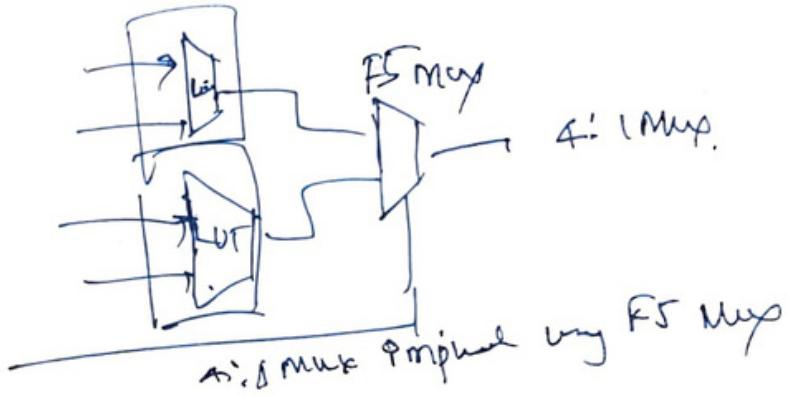
8:1 Mux using Dedicated Mux:

Dedicated mux have zero connection delay

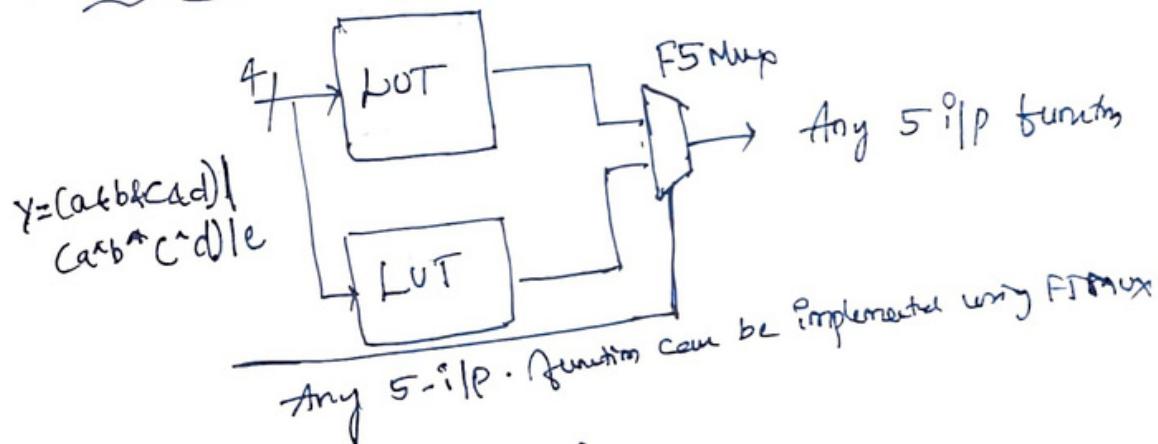


8:1 Mux, 4 LUTs, 1 level of Logic

4.1 Map any Dedicated User.



Function Expander :-



Input / Output Block (IOB)

Programmable Interconnect

Internal Resources.

→ Distributed RAM :-

Each CLB contains 32 bit of dual-port RAM.

↳ The SLCM optionally implemented as LUT or RAM as

RAM 32x1s

RAM

Difference b/w Block RAM and Distributed RAM
(CLUT Based RAM)

→ Block RAM: Data is synchronously read and written into the RAM.

→ Distributed RAM: Data is synchronously written and asynchronously read in case of distributed RAM

Shift register:

always@ (posedge r)

begin

if (cl)

{ b, c, d, x } = 0;

else

begin

b <= a;

c <= b;

d <= c;

x <= d;

end

end

Logic Utilization	Used
No. of Slice FF	4
No. of Occupied Slice	4
No. of Slices containing only Register	4
No. of Slice Containing WORD	0
No. of bonded IOB's	4
No. of Buffer	1

SRL16 (Shift Register):

→ Each LUT can be configured as SRL16 1 bit register.

// Without Reset

No. Slice -	1
No. of Slice FF	1
No. of 14 bit word	1
No. of bond IOB	1

Digital clock manager in FPGAs :-

→ A clock signal typically originates in the outside world, comes into the FPGA via a special clock I/O pin

→ Then it is routed through the device and connected to the appropriate registers.

Features of DCM:

- Jitter Removal → Frequency Synthesis → Frequency Division
- Phase Shifting → Auto-Skew correction.
- ↳ DCM blocks can be mapped by programming an IP core within the Spartan3.

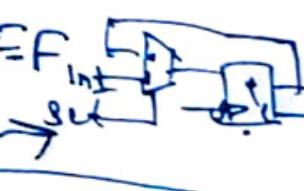
Spartan 3 Coding Techniques:

- HDL Coding Techniques for Improving Speed.
- ↳ Design should be such that it is fast, uses fewer resources & memory.
- ↳ If-else branch is slower in execution compared to case branches.
- ↳ For access to the dedicated carry chain, the HDL has to use arithmetic operators like "+, -, *, <, >"
 $a = x \cdot y \rightarrow$ will not infer carry chain
 Eg: $a = x + y \rightarrow$ will infer carry chain.
- ↳ One-hot encoding is recommended to Binary as one-hot is faster.

Coding Techniques for Area Minimization:

- The area optimization of unwanted logic will be useful in large FPGAs.
- Removing unwanted area not only reduces silicon area but also reduces switching activity, and hence, the power.
- Verilog uses constructs like 'if-else', 'else-if' for performing area minimization.
- Reset can be avoided to design Shift Registers to improve area.

Coding Techniques for Power Reduction:

- Lesser is the power dissipation, greater is the lifespan of the chip.
- ↳ Reduce switching of the data input to the FF.
 Eg: 

1. What is FPGA?

FPGA Stands for Field Programmable Gate Array. FPGA is a semiconductor device containing programmable logic components called logic blocks, and programmable interconnects.

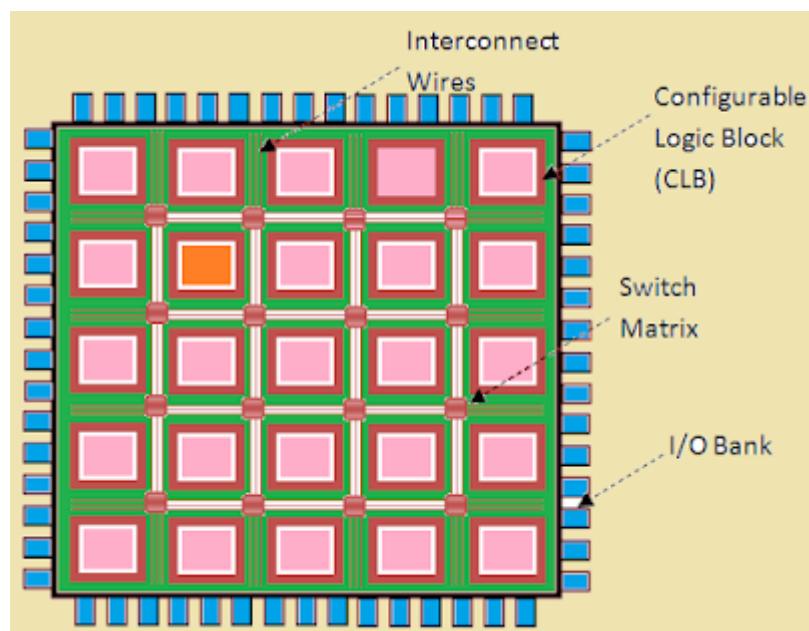
Logic blocks can be programmed to perform the function of basic logic gates such as OR, AND, and XOR, or more complex combinational functions such as decoders or mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Advantages of FPGA:

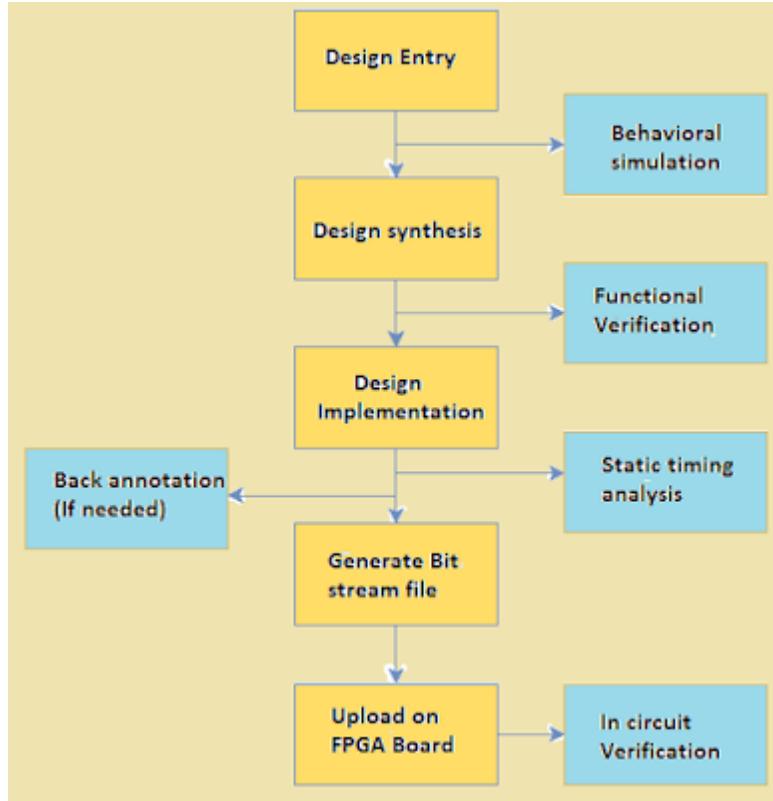
Faster time to market.

Ability to reprogram in the field to fix bugs.

2. Draw the general structure of FPGA.



3. Explain FPGA design flow.



4. What are DCM's? Why they are used?

Digital clock manager (DCM) is a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage. That is clock output of DCM is stable over wide range of temperature and voltage, and also skew associated with DCM is minimal and all phases of input clock can be obtained.

The output of DCM coming from global buffer can handle more load.

5. What is the purpose of a Phase lock loop(PLL)?

PLL stand for Phase locked loop and is commonly used inside FPGAs to generate desired clock frequencies. PLLs are built-in to the FPGA fabric and are able to take an input clock and derive a unique out-of-phase clock from that input clock. They are very useful if your design requires several unique clocks to be running internally.

6. What is the purpose of a DSP tile in an FPGA?

DSP stands for Digital Signal Processor but it is really a dedicated piece of hardware inside the FPGA that is very good at performing fast multiplication and addition operations. Normal FPGA logic is able to perform multiplies, but not at fast data rates of say 200 MHz or faster. This is where dedicated Digital Signal Processor(DSP) tiles are used. They are common in filter design or image processing pipelines that require many fast multiplication operations to be performed on input data.

7. What is the purpose of the synthesis tools?

The synthesis tools are provided by the FPGA vendor and are used to translate your VHDL or Verilog code into logic that the FPGA is built from example Flip-Flops, Look-Up Tables, Block RAMs, etc.

8. What is metastability, how would you prevent it?

Metastability means that a signal is in an unpredictable or unknown state. It occurs most often when bringing in a signal external to the FPGA into the internal logic. In general it

should be avoided. There are several methods to prevent metastability inside your FPGA, a common suggestion is to "double-flop" all inputs into the local clock domain.

9. Explain differences between SRAM and DRAM.

SRAM means Static Random Access Memory, DRAM stands for Dynamic Random Access Memory. Both SRAM and DRAM are volatile, that means their information written to them is cleared when power is removed.

DRAM also needs to be refreshed in order to maintain the values written to it, whereas SRAM being static does not need this.

The refreshing is usually handled by the memory controller. As far as use-cases, SRAM is better when there are short non-sequential reads and writes to memory required, and DRAM is better when there are large burst reads/writes of sequential memory.

10. What are differences between DLL and PLL?

PLL stand for Phase lock loop and DLL stand for Delay lock loop.

These are two techniques to minimize the clock skew.

1. DLL have less clock skew as compared to PLL.
2. DLL have step errors but hybrid PLL does not have it.
3. PLL have voltage-controlled oscillator (VCO) and DLL use delay line.
4. PLL are hybrid analog and digital whereas DLL are all digital.

11. What are the differences between FPGA and CPLD?

FPGA:

1. SRAM based technology.
2. Must be reprogrammed once the power is off.
3. Usually used for complex logic circuits.
4. Costly
5. Segmented connection between elements.

CPLD:

1. Flash or EPROM based technology
2. Continuous connection between elements
3. Usually used for simpler or moderately complex logic circuits.
4. Need not be reprogrammed once the power is off.
5. Cheaper

12. What is CLB and Slice?

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinational circuits. CLB are configurable logic blocks and can be configured to combo, ram or rom depending on coding style. CLB consist of 4 slices and each slice consists of two 4-input LUT (look up table) F-LUT and G-LUT.

The memory assignment is a clocked behavioral assignment, Reads from the memory are asynchronous, and all the address lines are shared by the read and write statements.

13. Explain LUT and CLB of FPGA.

Look Up Table(LUT): Each slice contains four or six input look up table ,storage elements,multiplexers and carry logic. These elements are used to provide logic functions and arithmetic functions and ROM functions.

Configurable Logic Block(CLB): The Configurable Logic Blocks (CLBs) constitute the

main logic resource for implementing synchronous as well as combinational circuits. A CLB elements contain a pair of slices. They don't have direct connection to each other.

14. What is the purpose of DRC?

In ASIC there are some sets of rules which depends on technology used to design. They are parameters set aside by the concerned semiconductor manufacturer with respect to how the masks should be placed, connected, routed keeping in mind that variations in the fab process does not effect normal functionality.

In FPGA , tool like Vivado check the correctness of the design before synthesis which is also said DRC check.

15. What are the different modes of programming the FPGA?

- 1.Flash
- 2.SRAM via JTAG or programmable cable.
- 3.USB and SD card.

16. What is minimum and maximum frequency of DCM in Spartan-3 series FPGA?

Spartan-3: Minimum frequency is 24 MHz and maximum frequency is 248 MHz.

17. Can a CLB configured as RAM?

Yes. In Xilinx CLB has two slices which is slice-L and slice-M. Function generators(LUT) in slice-M can be implemented as a synchronous RAM called distributed RAM.

18. Can you suggest some ways to increase clock frequency of design in FPGA?

- 1.Check critical path and optimize it.
- 2.Proper timing constraints.
- 3.Pipeline architecture.

19. What is the significance of FPGAs in modern day electronics?

- 1.Less time to Market when comparing with ASIC.
- 2.It is better for start-up companies to design their projects using FPGA rather than ASIC.
- 3.Less cost and reconfigurable as many require number of times.

20. What are the different reports we need to look while FPGA designing?

1. Synthesis report
2. Place and route report
3. Timing report after bit file generation.

In synthesis report we need to check signals or registers which are optimized and latches in design.

In PnR report and timing report we need to look Set Up and Hold violation and gate count and are clock constraints applied properly.

21. What are the inputs required for FPGA prototyping?

Inputs required for FPGA prototyping which synthesizable RTL design.

22. What is a Block RAM?

Block RAM is a specific part of an FPGA that is usually a 16k or 32k bits storage element. It can have dynamic width and depth and is useful for many applications inside of an FPGA. They are used in Dual-port memories, FIFOs, and LUTs.

23. What happens during place and route?

The synthesis process is usually followed by place & route which takes the primitives and places them inside the FPGA and checks that the entire design meets your timing

constraints. The timing constraints tell the FPGA the clock rates and the specific I/O to use, and the place & route process ensures that your design is able to work at those speeds.

24. What are the different type of RAM in FPGA?

1.Distributed Memory: Array of register.

2.Block Memory: Dedicated memory

Synthesis tool use any memory depends on your coding.

1.When it require to make small amount of data memory like small registers then use distributed memory.

2.When it require to make large amount of data memory like large LUT then use block memory. Block memory depends on FPGA series.

25. What is the difference between a hard processor core and soft processor core?

1.Hard Processor Core: Some part of fpga has fixed block like processor core and other standard IPs and little space for other logic implementation. It can work on high speed due to better optimization.

2.Soft Processor Core: User need to implement soft processor core if required. Full FPGA can be used for logic implementation. It can be easily modified and have more logic.

26. Name of FPGA companies.

1.Xilinx

2.Altera

3.Microsemi

4.Lattice Semiconductor

27. How to generate clocks on FPGA?

1.We need clock source regardless to drive FPGA

2.Inside we can use PLL to generate specific frequencies

3.We can use counters to scale down clock

28. What is synthesis?

Synthesis is the stage in the design flow which translating your Verilog code into gates. Synthesis tool gives a netlist of the design that you have synthesized that represents the chip which can be fabricated through an ASIC or FPGA vendor.

29. Draw a rough diagram of how clock is routed through out FPGA?

30. Tell me some of features of FPGA you are currently using?