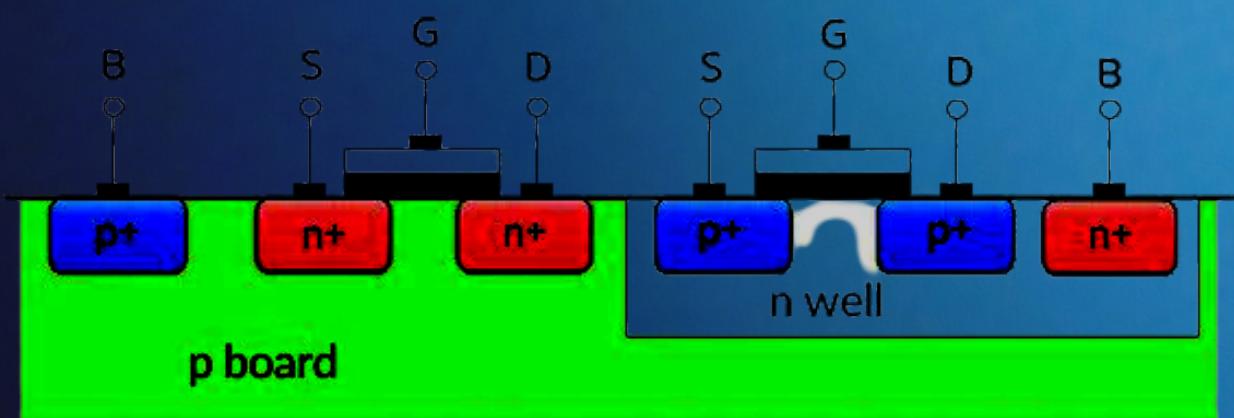




STICKY  
NOTES

# CMOS NOTES

NMOS



PMOS



## Difference b/w BJT and MOSFET

BJT has 3 terminals (base, collector, emitter) and MOSFET has 3 terminals (gate, drain, source).

- \* Bipolar junction Transistor
- \* Metal Oxide Semiconductor field effect transistor
- \* 3 terminals - emitter, base, collector
- \* 3 terminals - Gate, drain, source
- \* Current controlled device
- \* Voltage controlled device
- \* Negative temperature coefficient
- \* Positive temperature coefficient
- \* Low input impedance
- \* High input impedance
- \* Used in low current application
- \* Used in high power application.
- \* Higher output resistance compared to Mos
- \* Lower output resistance per unit current than BJT
- \* Not efficient for digital logic
- \* Quite efficient for digital logic.

## Introduction to design flow:

- Design flow is the explicit combination of electronic design automation (EDA) tools to accomplish the design of an IC.

We define flow as -

"An effective methodology of capturing & verifying a useable representation of an idea such that the final result exhibits the appropriate what is a ch. for its intended use".

### Effectingve methodology -

• series of understood and efficient steps.

#### Capturing design (step 1)

• Evaluation

#### Verifying design (step 2)

• Useable representation  
• Database is fully compatible with follow on steps.

#### Appropriate characteristics .

"A flow is an encapsulation of knowledge of how things should be done". A flow defines a sequence of steps & a set of CAD tools for specific design styles".

- Why have flows evolved?
- Time to market pressures
  - Full custom flow isn't practical for large designs
  - Size & complexity of new chips
  - Lack of skilled personnel
  - Automation and productivity gains
  - 3D extraction (New issues from shrinking geometry)
  - System on chip [SoC] - Intellectual property (IP)

- 3 types of design flows
- Full custom flow - schematic & layout done by hand (for performance)
    - eg: high speed A to D converter
  - ASIC flow {to put as many transistors in less time}
    - are application specific
    - eg: Mobile chips
  - Memory flow {to optimise area}.
    - Memories

- CAD tools-
- Design entry
  - Design validation

→ Why there are so many tools in market?

based on:- Design tools: up, analog, memory, RF, ...

Capture technique: Polygon, symbolic, Floorplan

Design size & complexity: place & route

Degrees of specialisation: P&R, chip assembly

Interface points: Feedback & Feed forward

Accuracy: Requirements

Acceleration techniques: Model order reduction

Database format support: GDS II, CIF, DEF, proprietary

Business opportunities: Niche markets

### Custom IC Design flow -

registration of a concept of task

"definit" of design

comparison → implementation ← comparison with design spec.



simulation



layout entry



layout verification



parasitic extraction



fabrication

# Testing & verification

## Product

Popular tools for design entry & simulation-

Cadence tools

→ Schematic Entry → Composer

simulation → Virtuoso Analog design

environment

No

OK

Yes

→ Layout Design

Virtuoso

↓

Layout Verification

Virtuoso LVS

(core & LVS errors)

No

OK?

Yes

Post-layout Simulation

Virtuoso BCX + ADE

(no post-layout errors)

(No)

OK

Yes

(is there any error in layout)

(no errors in layout)

## ASIC design flow:-

- For functionality {many transistors in one chip}
- Highly automated but requires Flow expertise

Diff. b/w ASIC & Full custom -

In Full custom - schematic is done through  
transistors.

In ASIC - First RTL code is written & is simulated  
using digital simulator.

18/19

## Introduction to CMOS fabrication-

### Fabrication-

Process of manufacturing something, where an item is made or manufactured from raw materials to finished products.

Raw material → Sand (has  $\text{SiO}_2$ )

### Sand to silicon -

- poly silicon nuggets From sand → (Metallurgically pure silicon) Semiconductor pure silicon ie 99.9999% pure silicon by crystal pulling. ie we get crystal → Si Ingot [dip the Si crystal inside molten Si & slowly pull it out with rotation to get required size of ingot → slice the ingot into wafers → Klafer polishing (to get mirror finish Si) → Create macro ckt's on wafers by patterning

polysilicon.— is polycrystalline ie orientation of all atoms ~~not~~

normal silicon — is a single crystal silicon  
ie orientation of all atoms is same

① To make polysilicon nuggets— sand is put into furnace ( $2000^{\circ}\text{C}$ ) & put coke (charcoal) to create metallurgical grade silicon & get semiconductor grade pure Si ( $99.99999\%$ ) (silicon ingots)

② Use "Czochralski process" to create silicon wafer  
Czochralski process—

Step 1: preparation of high quality purity molten silicon (heating sand)

Step 2: Dipping seed crystal [a small piece of single Si crystal will be dipped into high purity molten silicon]

Step 3: Pulling seed upwards [the seed crystal is pulled upwards while rotating, the seed crystal and crucible will rotate in opposite direction]

This large rod ( $300-400\text{mm}$ ) of Si will be called ingot.

Melting point of silicon —  $1200$  to  $1400^{\circ}\text{C}$ .

→ Why semiconductor?

- Electrical conductivity between conductor & an insulator
- "Bandgap" for semiconductors can be adjusted with doping

→ lead to creation of miniature device

• High level of integration & low power consumption

Why Silicon?

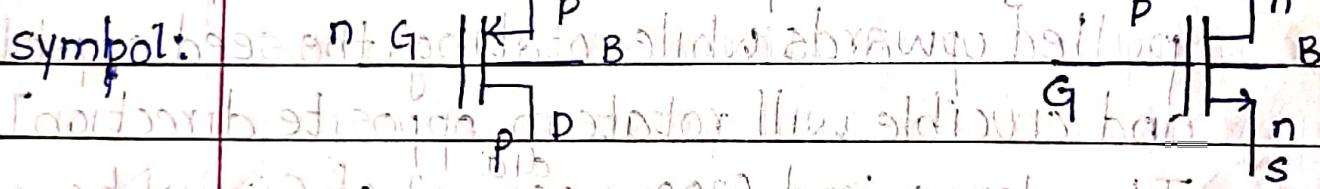
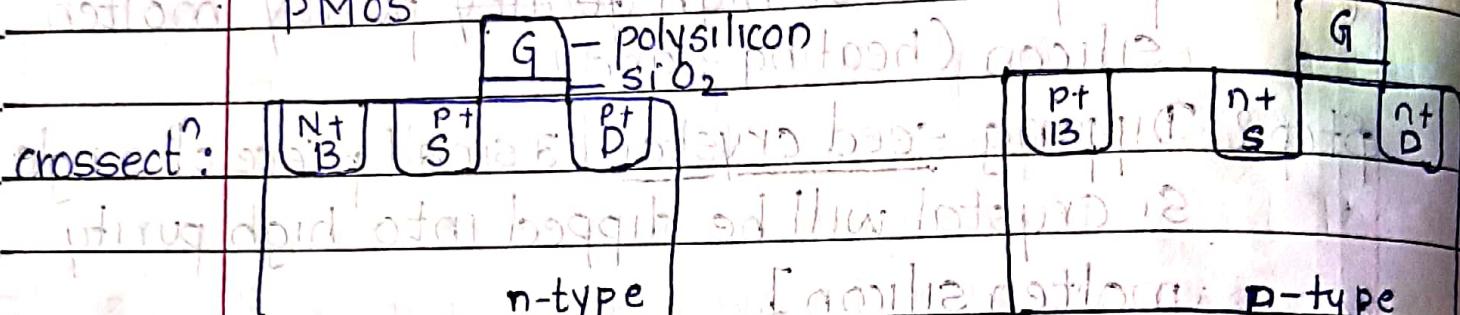
• More abundant  $\Rightarrow$  low cost

• Higher bandgap voltage than Ge  $\Rightarrow$  lesser free electrons at any given temperature  $\Rightarrow$  lower leakage.

- stable operation for wider temp. range.
- silicon can be easily oxidised to form thin layer of  $\text{SiO}_2$  and also thick oxide which helps to isolate components or well from one another.

### MOS Transistor-

bottom: PMOS (bottom to top)



- Gate, Source, Drain, Bulk (n type) • Gate, Source, Drain, Bulk (p type)

How can we create multiple transistors on silicon?

Process of creating patterns on semiconductor crust

- also to produce integrated circuits

→ Photolithography [optical or UV lithography]

• used in micro fabrication

• light is used to transfer pattern from a photo mask to a light-sensitive "photo resist" on substrate.

## Photolithography - instant and sequential

- Photolithographic sequence is repeated for each physical layer used to construct the IC.

Sequence is -

(i) Photo resist application

The photo resist which is photosensitive is applied on wafer's surface. (first  $\text{SiO}_2$  is deposited, which acts as a mask by blocking impurities from entry)

(ii) Printing or Exposure -

Printing mask on photoresist through exposure of uv light

(iii) Development

Pattern which is transferred from mask to photoresist is developed by removing the soluble part of photoresist.

(iv) Etching

Pattern on photoresist is transferred to the  $\text{SiO}_2$  layer below it to which it was supposed to be transferred.

Photolithography : Patterning & ION implantation.

Patterning - To deposit a layer on Si wafer.

ION implantation - To implant ions.

Wafer is first coated with resist and patterned.

①

## Patterning & ion implantation

② photo resist

Step 1: Spin-coating with photo resist

A circular photoresist is applied with photo resist and spun. The speed of spinning decides the thickness of photoresist. [first  $\text{SiO}_2$  applied]

Mask

Step 2: Expose photoresist to UV light

unexposed

Pass UV light through mask & wherever there's opening, UV falls on photoresist & that exposed part of photoresist becomes soluble.

③

Step 3: Remove the soluble photoresist. The patterned photoresist will now serve as an etching mask for the  $\text{SiO}_2$ .

④

Step 4:  $\text{SiO}_2$  below the removed photoresist is etched away leaving substrate exposed.

The patterned resist is used as the etching mask.

⑤

Step 5: Substrate is subjected to highly energized donor or acceptor atoms.  $\text{SiO}_2$  acts as a

mask & only when there's an opening the atoms go inside the mask, rest all places it's blocked. Atoms impinge on surface &

travel below it. Patterned  $\text{SiO}_2$  serves as an "implant" mask.

diffusion

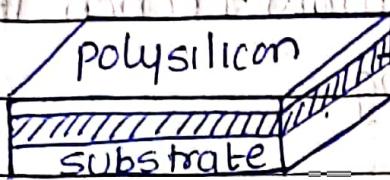
Step 6: Doping is further driven into bulk by thermal cycle-annealing

substrate

(to deposit a layer of polysilicon or any other)

① Depositing and patterning a layer above surface.

① polysilicon deposition



SiO<sub>2</sub>

substrate

SiO<sub>2</sub>

substrate

SiO<sub>2</sub>

substrate

to be deposited is

deposited before photoresist

② Photoresist development

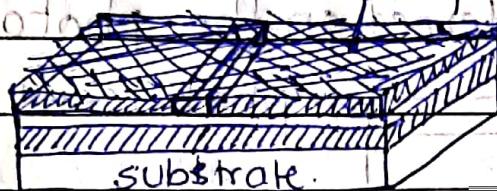
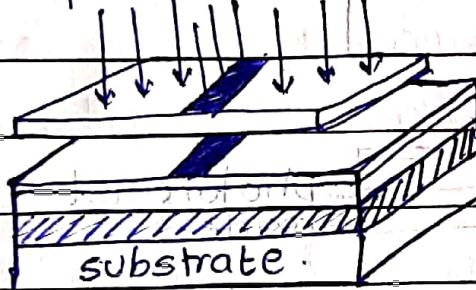


photo resist

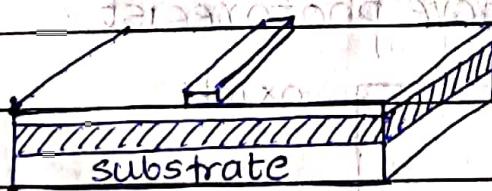
substrate

③ Exposure, uv light



substrate

④ Photo resist development



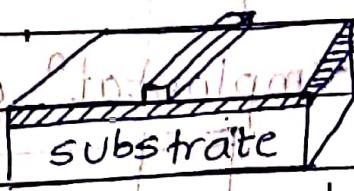
substrate

⑤ Polysiliconic etching

⑥ Final polysiliconic pattern



substrate



substrate

removing photo resist

int. Overview of process steps - Fabrication of CMOS inverters

• Local oxidation of silicon process [LOCOS]

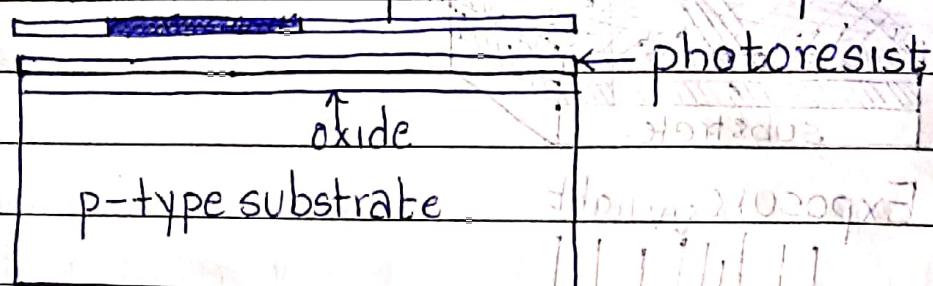
currently used STI - shallow trench isolat<sup>n</sup> process  
is used for manufacturing

LOCOS - step 1 -

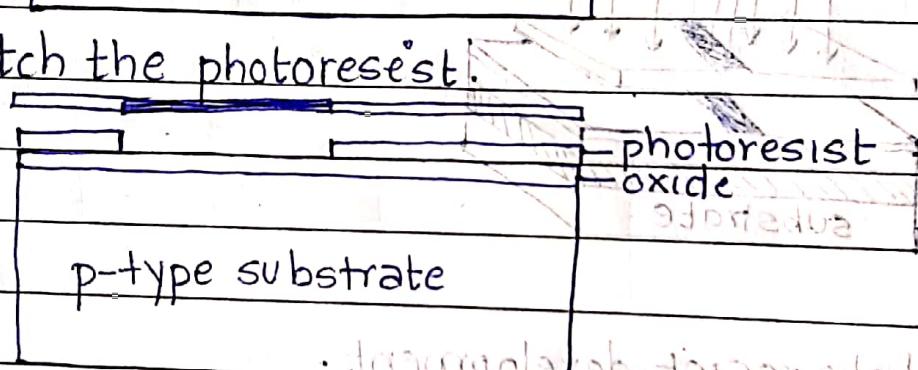
① Form N-well regions: agohabha dhaarabodq (ii)

High temp. process.

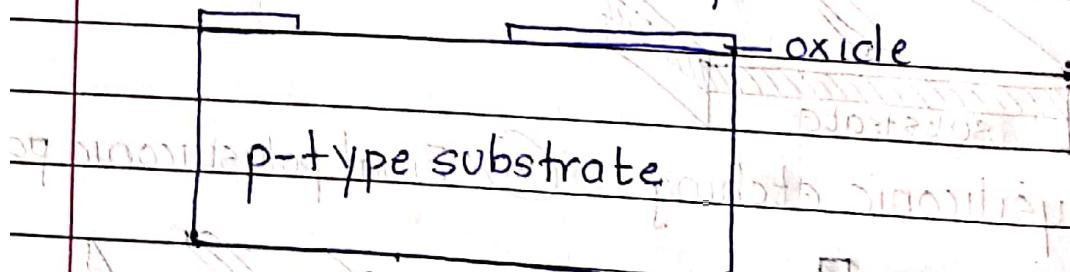
• N-well mask is patterned on the photoresist



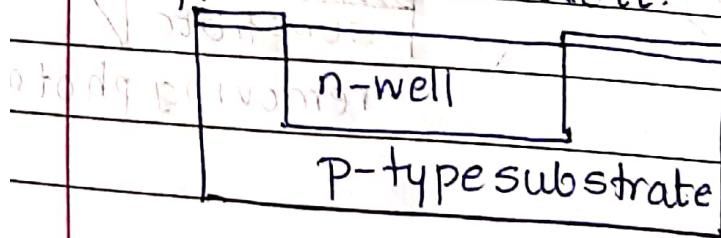
• etch the photoresist:



• etch the oxide & remove photoresist.



• implantat<sup>n</sup> of n well.

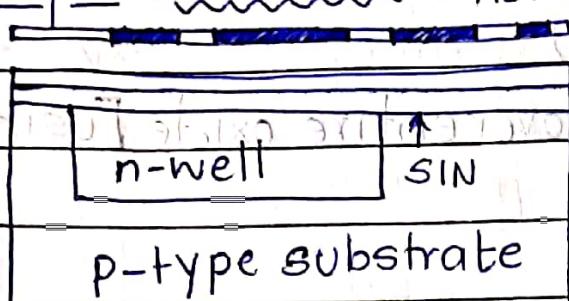


diffuse n-type dopants through oxide mask layers.

## Step 2 - Form Active regions

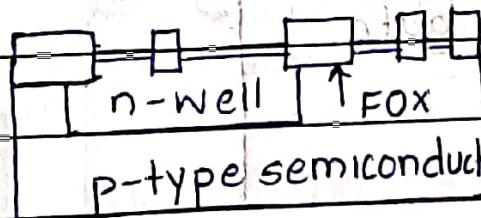
Active mask

SiN - silicon nitride



Active areas: in p substrate we have N-MOS & in n well there's PMos, source & drain of MOS's are active area.

- Form active regions, deposit SiN over wafer, & photo resist over SiN layer
- pattern photoresist
- Etch SiN in exposed areas - leaves SiN mask which blocks oxide growth.



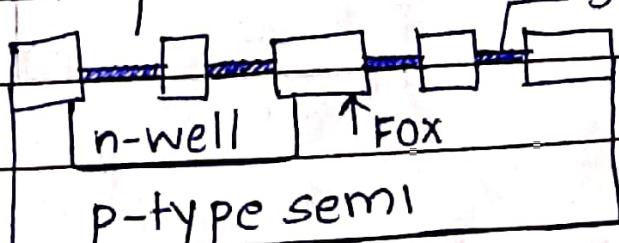
Grow Field Oxide(FOX) by thermal oxidation.

Field oxide - wet oxidation

i.e. in presence of steam, temp. of furnace is raised to 900°C and H<sub>2</sub>O permeates into Si & combines & forms SiO<sub>2</sub>. Oxygen escapes this gives FOX which is porous & not of high quality

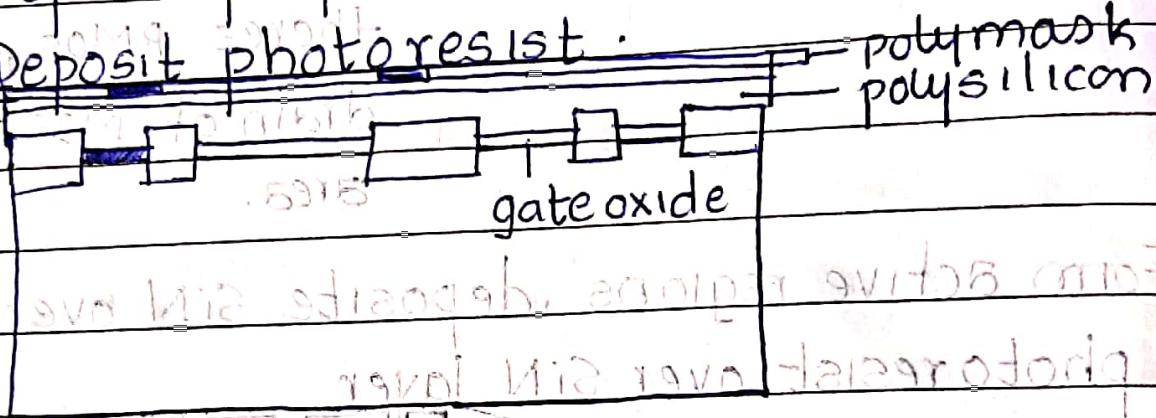
- Remove SiN

& grow SiO<sub>2</sub> over entire surface

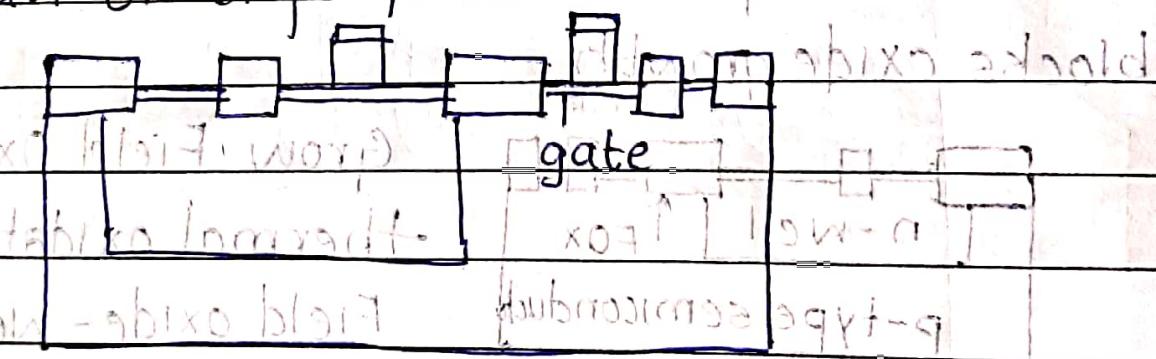


SiO<sub>2</sub> grown after removal of SiN.

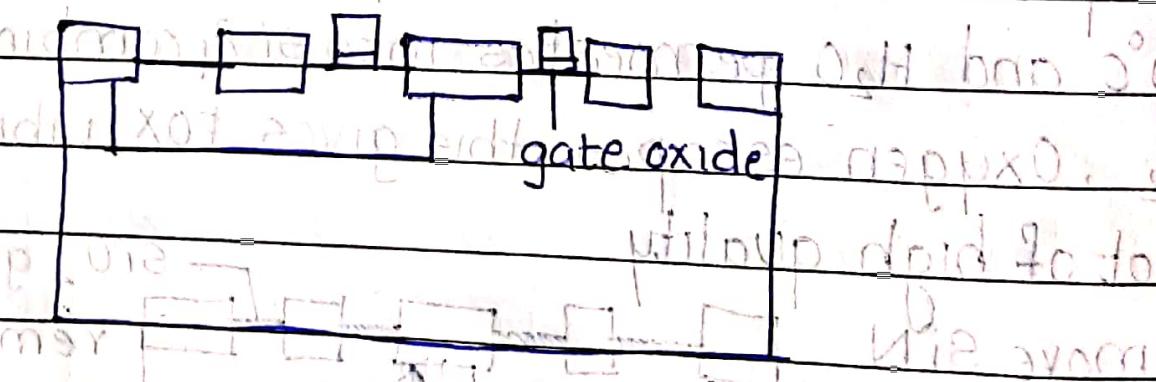
- ~~11317-1~~
- LOCOS - step 3 :
- Form Gate (poly layer)
  - Grow thin gate oxide over entire oxide [using dry oxide]
  - Deposit polysilicon
  - Deposit photoresist



- Pattern polymask, once patterned - remove all other poly.



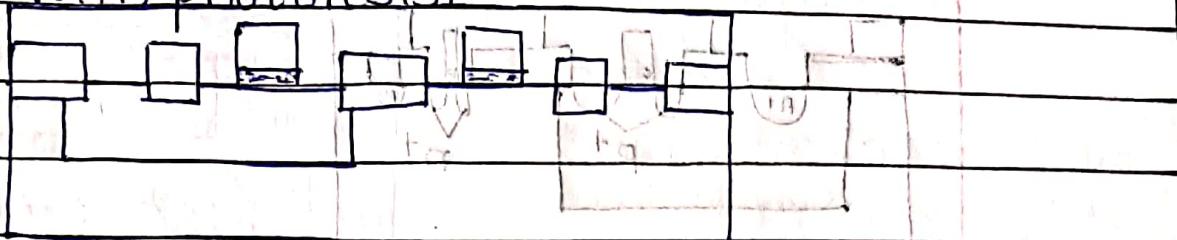
- Remove photoresist mask to remaining



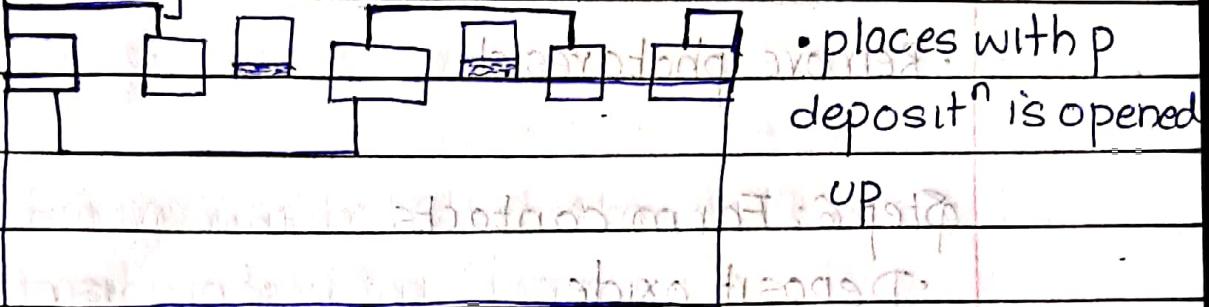
- Remove gate oxide from remaining

## Step 4 - Forming of PMOS SLOTH and its formation

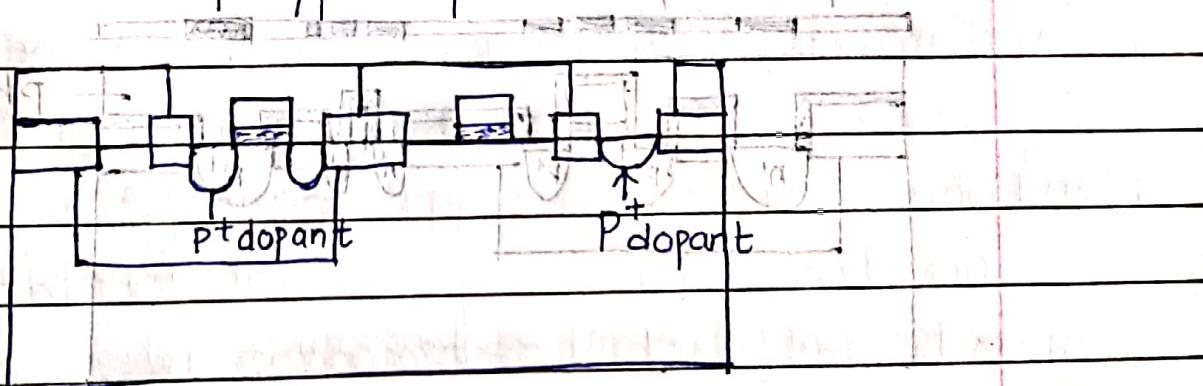
- Cover with photoresist



- pattern using PSELECT MASK



- implant p type dopant

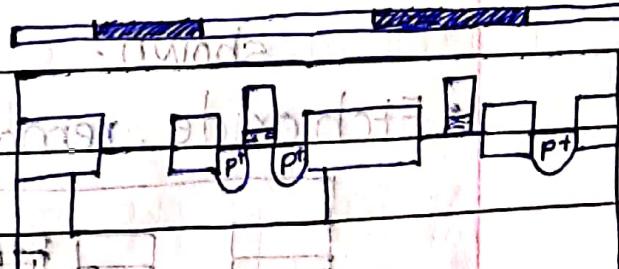


- Remove photoresist

From mask 8 with photoresist removed

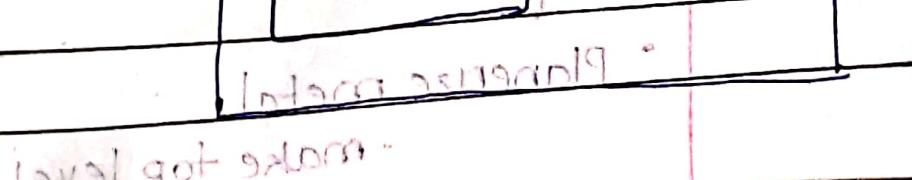
## Step 5: For n-mos SLO.

- Cover with photoresist

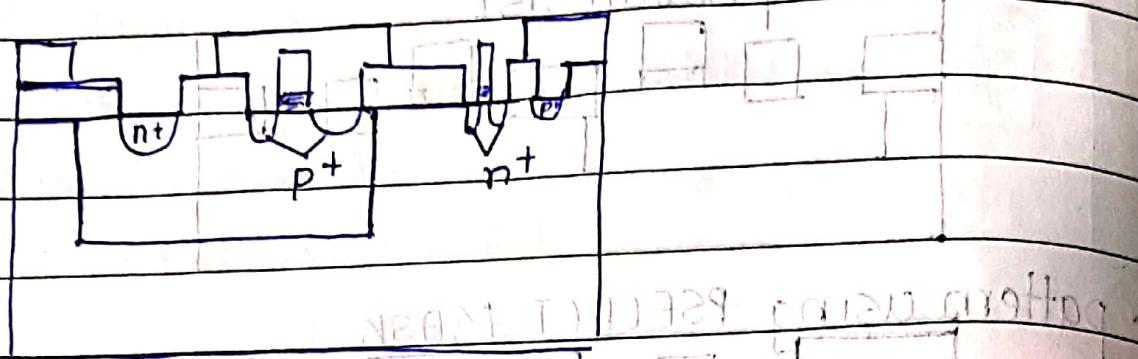


- pattern photo resist

using Nselect mask.



- implant the dopant

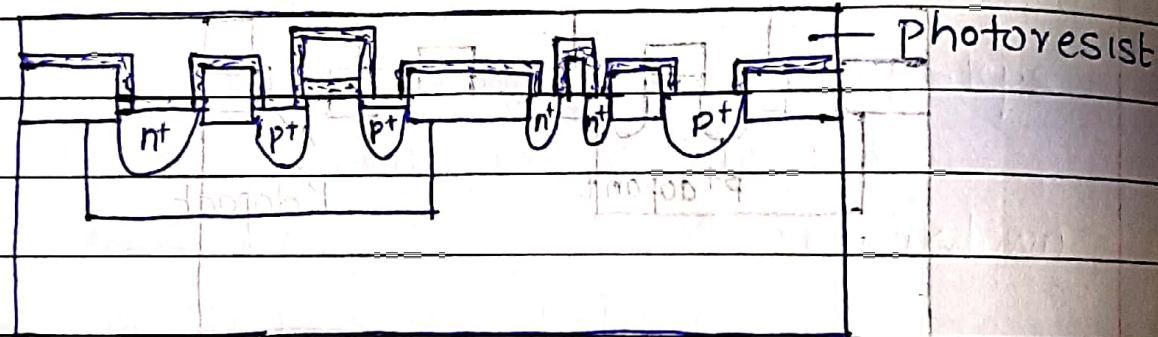


- Remove photoresist

### Step 6: Form contacts

- Deposit oxide

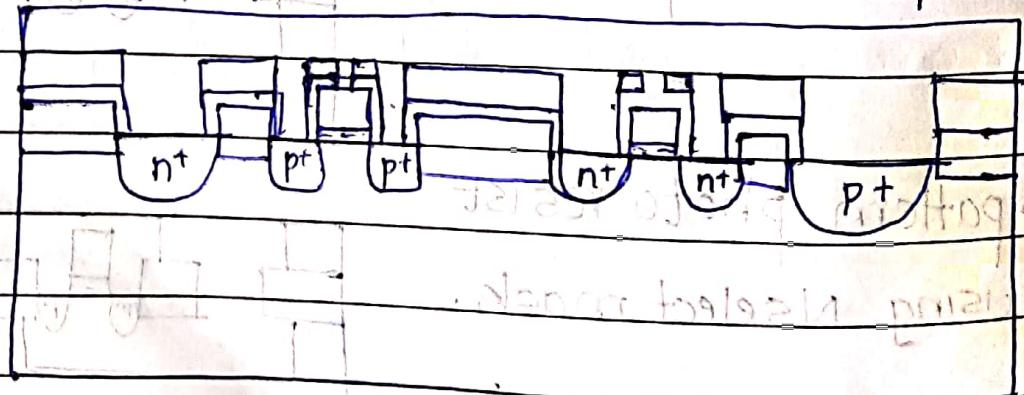
- Deposit photoresist



- pattern photo resist for contacts

- One mask for both active & poly contact shown

- Etch oxide, remove photoresist & deposit metal



- Planarize metal

- make top level

~~Step 1: Form metal 1 traces~~

Form metal 1 traces

- Deposit photoresist
- pattern
- Metal 1 mask
- Etch metal
- Remove photo resist.

~~Step 8: Form Vias to Metal 1~~

- Deposit oxide
- Planerize oxide
- Deposit photoresist
- pattern VIA mask
- VIA Mask
- Etch oxide
- Remove photoresist

~~• Deposit Metal 2 traces~~

~~Step 9: Form Metal 2 traces~~

- Deposit Photoresist
- pattern
- Metal 2 mask
- Etch Metal
- Remove photoresist

## Step 10: Form additional traces

- Deposit oxide
- " photoresist
- pattern "
- Etch oxide
- Deposit metal
- " photoresist
- pattern "
- Etch metal
- Repeat for each additional metal

## Simplifications from complete process -

- Skipped several substrate doping steps
  - channel implant to adjust  $V_t$
  - surface "  $\uparrow V_{breakdown}$
- no LDD, lightly doped drain
- no deposit<sup>n</sup> of contact interface materials
- metal patterning simplified
- no overglass (thick top dielectric) layer
- no bonding pad layer
- Simplified use of dark/clear field masks & +ve photoresist.

## Advancement in CMOS Fabrication Technology

### Different process Technology

#### NWELL -

Here NWELL is created in p substrate. PMOS are built in NWELL and nMOS in p substrate.

#### PWELL -

prior to NWELL process, this process was used. PWELL is created in the n substrate & NMOS in PWELL.

#### Twin tub / WELL -

p-well and n-well have created for NMOS & PMOS respectively in twin well or twin tub technology.

Both transistors can be optimised separately.

#### SOT - System on Insulator

Fabricated on <sup>(SiO<sub>2</sub> or sapphire)</sup> insulating substrate eliminates capacitance between the source drain & body, resulting in higher speed devices & low leakage currents.

### Advanced CMOS Process Techniques

• Shallow trench isolat<sup>n</sup> - Use of SiO<sub>2</sub> trenches for noise isolation

↳ Instead of growing field oxide on surface of SiO<sub>2</sub>, wherever field oxide is to be grown, SiO<sub>2</sub> is etched out so that SiO<sub>2</sub> can be grown inside top layer of silicon which helps in noise.

• n<sup>t</sup> & p<sup>t</sup> doped polysilicon gates - To build low threshold voltages

to avoid off to off

In small geom. when S&D are heavily doped & closer, the E-field is very high

- Source-drain extensions LDD - lightly doped drain structure used to reduce hot e<sup>-</sup> effects in smaller geometry design
- Self aligned silicide (spacers) on sides on gate (III<sup>tar</sup> to LDD)
- Non uniform channel doping (short channel effect)

### Process enhancements - I

- Up to 10+ metal levels in modern processes.

Copper for metal levels 2 & higher

stacked contacts and vias

chemical Mechanical polishing for technologies with several metal levels

For analog processes I application some processes

offer: analog mixed signal and memory

### Resistors

### Bipolar transistor [BiCMOS]

### Process enhancements - SOT

• SOT is gaining lot of currency in high speed UDSM processes.

Ultrathin SOI microprocesses

Reduces parasitics: Substrate capacitor

- Enhances speed 25-30% or
- Lower power ~50%, or
- Mix of both above.

- Reduces substrate cross talk and MOS strip, R, L, C losses at high frequency
- Better RF capability of CMOS. Up to 10GHz

Two types of SOT:

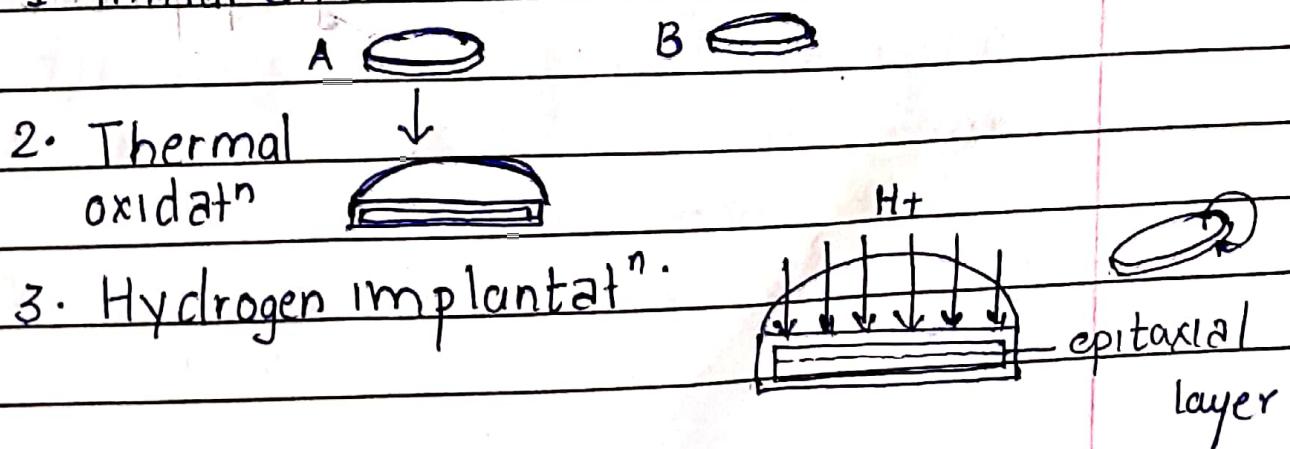
- SIMOX → Oxygen implant / Anneal process
- BE-SOT → Bond / Etch back process

Both processes use silicon as substrate & thin layer of  $\text{SiO}_2$  as isolation between substrate & thin SO - called epitaxial layer

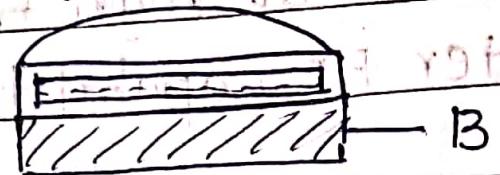
• Process -

1. Take 2 monolithic silicon wafers
2. Oxidise wafer A
3. Implant hydrogen to depth of epitaxy
4. Bond wafer B with reversed wafer A
5. Split or smartcut wafer A
6. Annealing & polishing of bonded wafers
7. Cut wafer A becomes new wafer for new SOI wafer creation.

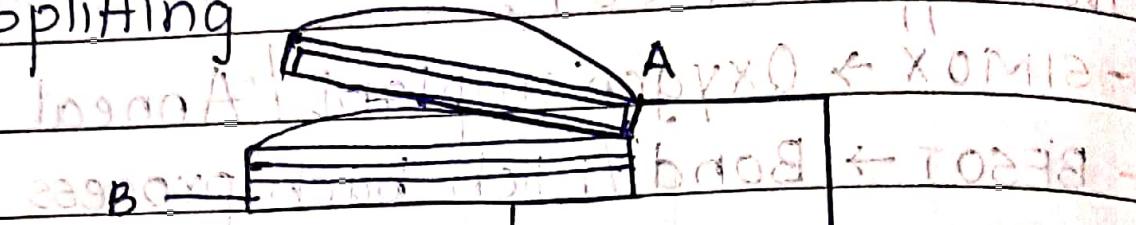
diagram: 1. Initial silicon wafers



#### 4. Cleaning & bonding

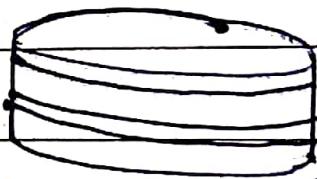


#### 5. Splitting

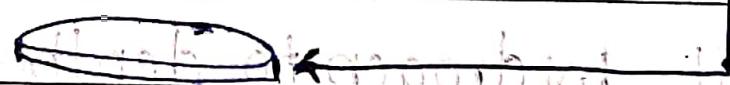


#### 6. Annealing & CMP planarization

touch & polishing



soi wafer



A becomes a new A.

Advantages of soi processes -

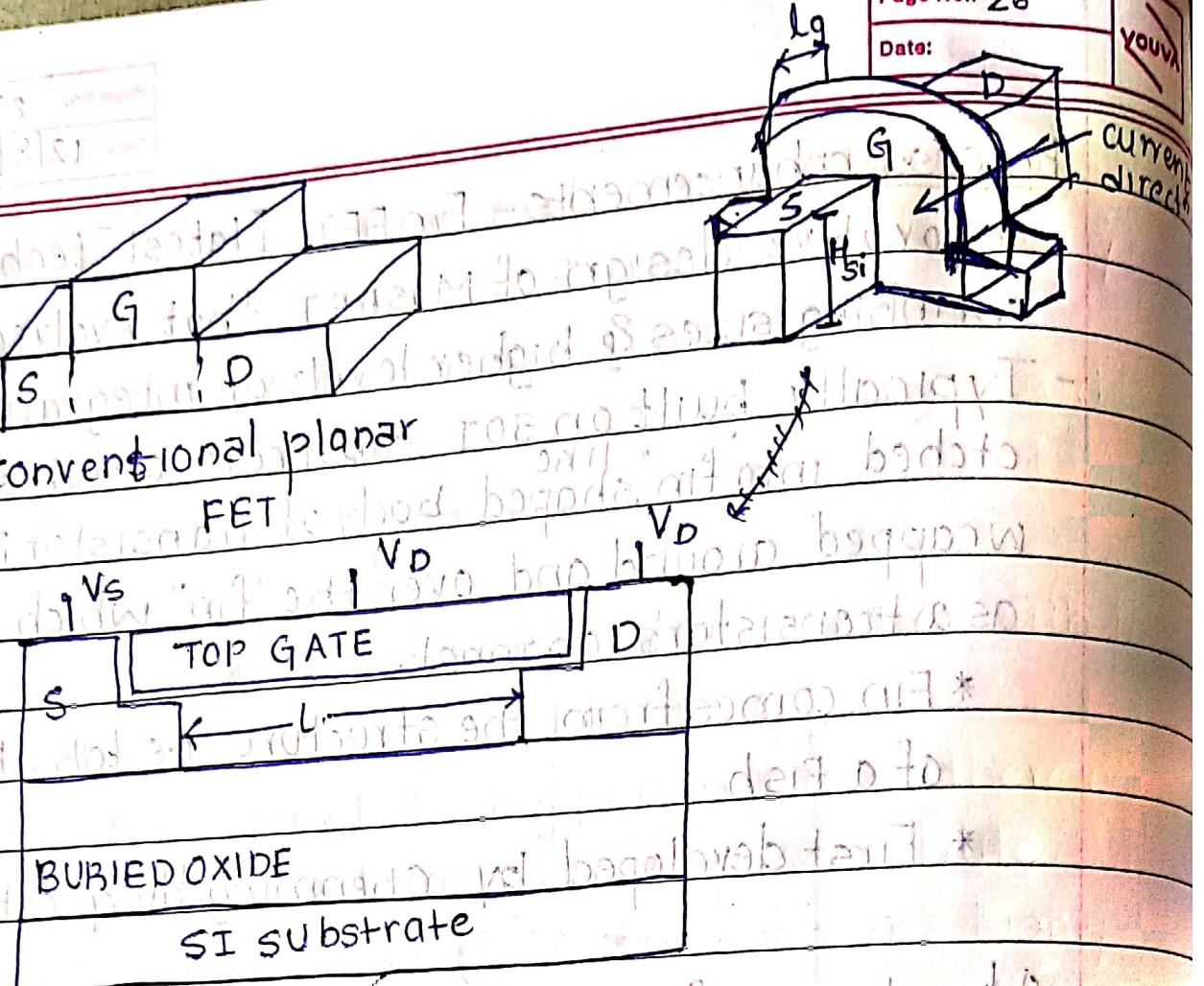
- This SOI creation technique relies on standard microelectronics manufacturing equipment.

## Process enhancements - FinFET [latest technology]

- Innovative design of MOSFET that evolved with shrinking sizes & higher levels of integration.
- Typically built on SOI substrate on which Si is etched into "fin" shaped body of transistor; gate is wrapped around and over the "fin" which also acts as a transistor's channel.
- \* Fin comes from the structure i.e. looks like fins of a fish
- \* First developed by Chenming Hu & colleagues.

### Advantages of FinFET:

- (power) ★ Much lower power consumption allows high integration levels. Early adopters reported 150% improvements.
- (Op. Volt) ★ FinFET operates at lower voltage as a result of their lower threshold voltage.
- (feature size) ★ Possible to pass through 20nm barrier previously thought as an end point.
- (static leakage current) ★ Typically reduced by 90%.
- (operating speed) ★ In excess of 30% faster than the non-FinFET versions.



What's difference b/w wet & Dry Oxidation?

Goal of oxidation is to have a high quality oxide layer

on silicon substrate.

wet Oxidation

Faster



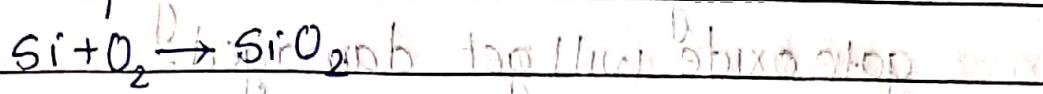
Temp: 900°C

Disadvantages

- Whenever  $H_2$  needs to come out of  $SiO_2$  layer defects gets formed and trapped  $H_2O$  molecules remain in layer.
- Not so controlled thickness
- Can not get thin oxides consistently.

## Dry Oxidation

Very slow oxidation rate at low temp.



Temp: 1200°C

- clean

- Controlled thickness

- High quality of Oxide (no defects)

When electrical and chemical properties of film are not critical, wet oxidation is used, most commonly for thick oxide layers.

For gate oxide - high quality & consistent thickness

we use dry oxidation even at higher

why is p substrate more commonly used compared to n-substrate?

NMOS has high mobility & creating NMOS in Psubstrate would be more than in p-n-substrate

P-substrate resistance is very low compared to N-well, more resistance  $\Rightarrow$  more power supply.

Oxidation sequence: What'll happen if we change the sequence to: gate oxide  $\rightarrow$  poly  $\rightarrow$  FOX?

Originally: FOX  $\rightarrow$  gate oxide  $\rightarrow$  poly

high temp.  $\rightarrow$  low temp.

involution process  $\rightarrow$  annealing process.

If the sequence Gate oxide  $\rightarrow$  poly  $\rightarrow$  FOX then -  
• FOX will get created below gate oxide &  
gate oxide will get damaged.  
• Poly at high temperature will get oxidised &  
get damaged.

Q) Why is p-epitaxial layer created when substrate  
itself is p-type for N-well process?  
For latchup not to happen in CMOS, there need  
to be very small resistance p-substrate. But if  
very low resistance p-substrate means highly  
doped p-substrate  $\Rightarrow$  highly doped p-substrate,  
if need to invert & create NMOS into it then  
NMOS p threshold voltage will increase & will be  
very high.  $\therefore$  we create low resistance, slightly highly  
doped p-substrate & lowly doped & high resistance  
epitaxial layer.

(\*) Why do we create oxide ( $SiO_2$ ) below nitride  
layer used for field oxidation (FOX) as Mask?  
Thermal coefficient of expansion of silicon nitride  
& silicon are different that leads to tremendous  
stress created (at surface level of silicon when  
oxidation is created at high temp), which damage  
surface of silicon & MOS being a surface device

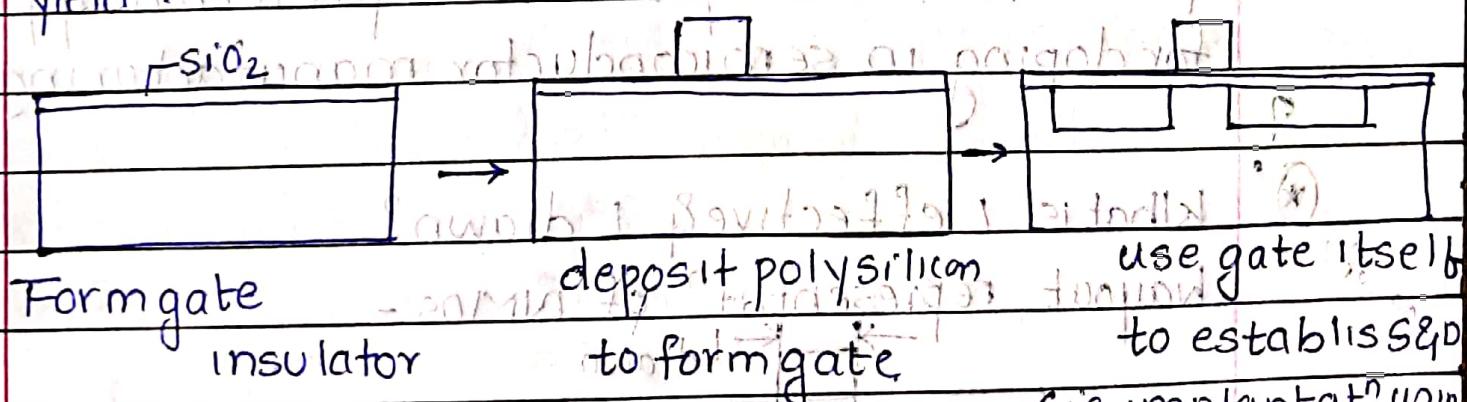
performance will be hampered,  $\text{Si}_3\text{N}_4$  layer which takes the stress is created.

Q) Why do we etch the oxide below nitride layer mask after field oxidation and create new thin oxide?

- The  $\text{SiO}_2$  undergoes stress & defects are created, :-  
When removing silicon nitride, if we use stressed  $\text{SiO}_2$ , then the gate oxide will not be as pure as & performance of MOS will be affected.

Q) What's meant by self aligned CMOS process?

- Gate itself is used as mask that establishes the source & drain, resulting in precise alignment of source, drain & gate regions. This results in simplification of processing steps, better performance & better yield.



First commercial product using self aligned silicon gate technology was the Fairchild 3708 8-bit analog MUX, designed in 1968.

★

What's diffusion & ion implantation?

- Diffusion & ion implantation are two methods for semiconductor doping.

- Diffusion is a process where concentration gradient causes movement of atoms. It can be used for introducing dopants in a semiconductor.

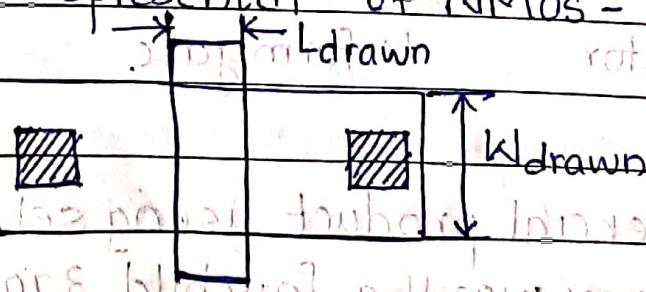
Typically conducted in systems called diffusion furnace at high temperature.

- Ion implantation: An alternative to high temp. diffusion for introducing dopants. High energy acceleration is used to introduce dopants. Implantation is done at ambient temp. and then high temperature annealing is done to form uniform doping and reduce crystal defects caused by implantation.
- In 1970, ion implantation is preferred approach for doping in semiconductor manufacturing.

★

What is L effective & L drawn?

Layout representation of NMOS -



To plot parametric graph - short on minimum time  
 $V_t = DV < 2DV$  getting  $V_{ds}$ ,  $V_{ls}$ ,  $I_d$  for diff.  $V_{ds}$ .

After getting the plot -

Go to ADE-L → tools → parametric analysis → Advanced choices  
 (For input ch.) →  $V_{ds}$  → From 0 to 1.8V, total steps  
 10 → Run.

In Virtuoso (R) Visualisatn & Analysis XL-0  
 browser → result → psf (double click) → dc Opinfo  
 → MO (device, double click) → select  $V_{th}$  (right click)  
 → table

$V_{ds}$	MO: $V_{th}(V)$
0	0.458
0.2	0.450
0.4	0.442
0.6	0.434
0.8	0.426
1.0	0.418
1.2	0.410
1.4	0.402
1.6	0.394
1.8	0.386

To get various  $V_t$  values for diff.  $V_{ds}$ .

Again in dc Opinfo → MO → region

$V_{ds}$	MO: region	$V_{ds}$	$V_t$	just below $V_{th}$
0	1	1	2	1 → cutoff
0.2	1	1.2	2	1 → Triode
0.4	1	1.4	2	2 → saturat <sup>n</sup>
0.6	1	1.6	2	3 → subthreshold
0.8	2	1.8	2	

$$(0) \quad (1.8 - 0.4)$$

NOTE:- Initially in triode because  $V_{ds} < V_{gs} - V_t$

Later not saturat' because  $V_{ds} > V_{gs} - V_t$   
 $(0.8) > (1.8 - 0.426)$

When  $V_{gs} = 0.2$  which is not true  
 $V_{ds} = V_{th}$   $V_{gs} > V_t$  we try to get device in cutoff

by varying  $V_{gs}$  in APE L

0 0.4587 0.2 " 0 to 0.2V

0.2 IX 0.4506 : A-0.2 " 3 low V (s) boundary of

0.4 ← (0.4425 to 0.2) ← forward

0.6 ← 0.4344 = 0.2 (A-3) subthreshold region ←

0.8 0.4263 " 3 — subthreshold region.

1 0.4182 " 3 Just above 'below threshold'

1.2 0.4101 " 3 3.0

1.4 0.4021 " 3 5.0

1.6 0.3940 " 3 7.0

1.8 0.3859 " 3 9.0

such DV gap OT

bV of OT gap DV

2.0

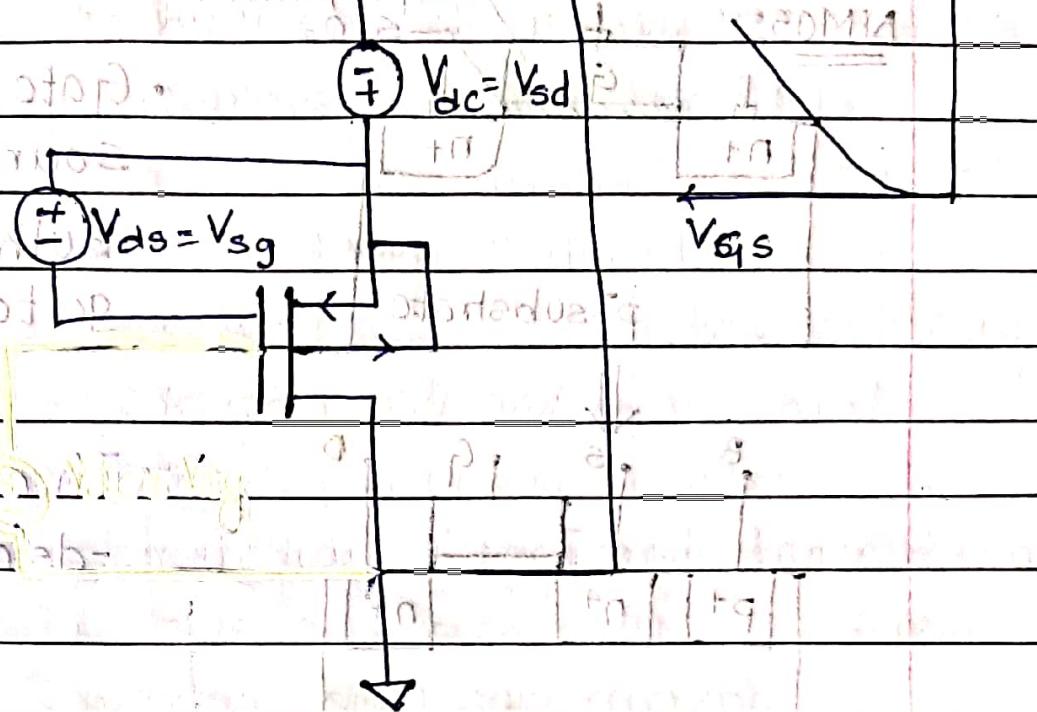
8.0

0.1

8.1

1.1

For PMOS -  $V_{ds} = V_{sg}$



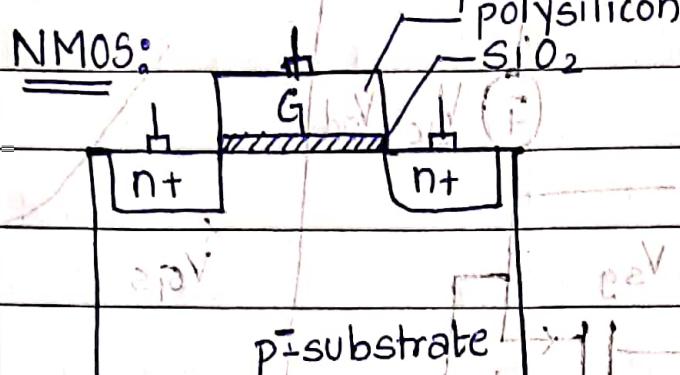
$$V_{sg} \rightarrow 1.8 \text{ V}$$

$$V_{sd} \rightarrow 1.8 \text{ V}$$

$V_{dc} \rightarrow V_{sg}$  : sweep 0 to 1.8

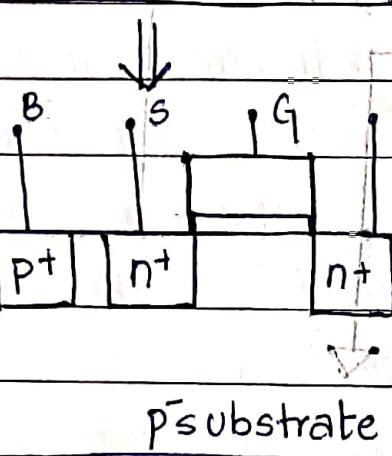
# Electronic Analysis Of CMOS logic Gates-

NMOS:



- Gate is fabricated before source & drain.

• Bulks of NMOS should go to source.

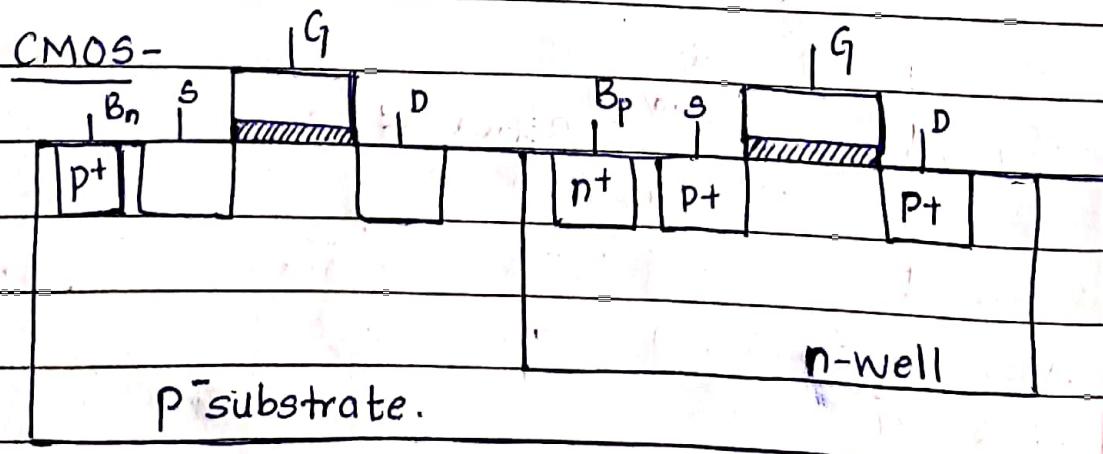


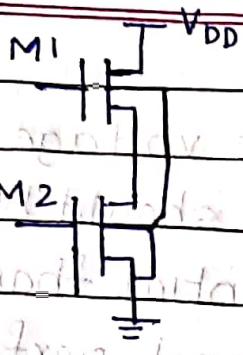
$V_{t0} = f(V_{SB})$   
Threshold voltage depends on process parameters  
source to bulk voltage.

$$V_{t0} = f(V_{SB}) \\ \Rightarrow V_{SB} \uparrow \Rightarrow V_{t0} \uparrow$$

\* (PMOS: in N WELL)  $V_{SB} \downarrow \Rightarrow V_{t0} \downarrow$

\* As  $V_t$  decreases, leakage increases. { i.e standby (OFF) power }, but if  $V_t$  increases then device becomes low.





Bulk of  $M_2$  = Source = Ground = 0

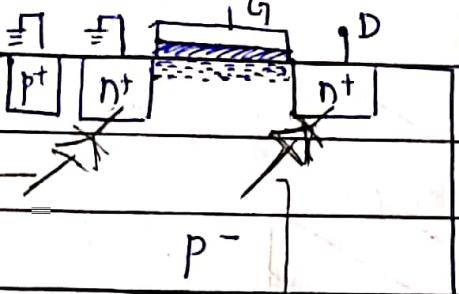
bulk of  $M_1 > 0 \Rightarrow V_{th}$  is more &  $M_1$  is comparatively slow than  $M_2$

P-substrate  $\rightarrow$  silicon doped with trivalent acceptor dopants  
dielectric  $\rightarrow$   $\text{SiO}_2$

Gate  $\rightarrow$  poly crystalline silicon [conductance b/w metals & insulators], this is used <sup>(in place of metal)</sup> because MOS is Field effect transistor & we don't need gate current.

For NMOS -

$V_G > 0$  is applied &  $V_G > V_t \rightarrow$  channel starts to form but no current but when  $V_D$  applied current flows from D to S.



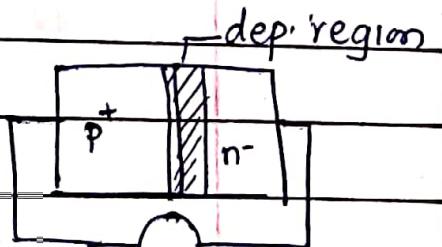
- Depth of channel is dependent on  $V_{GS}$  applied.

- As  $V_{DS}$  increases, pinchoff happens

acts as pn junction, at drain

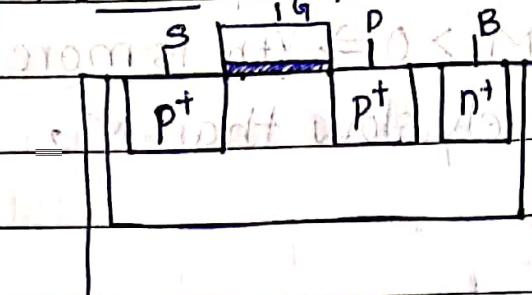
as  $V_{DS}$  increases ( $R_B$  increases), depletion region increases & pinchoff occurs.

$\rightarrow$  Profile of channel, doesn't change at source & so pinchoff doesn't occur at source.



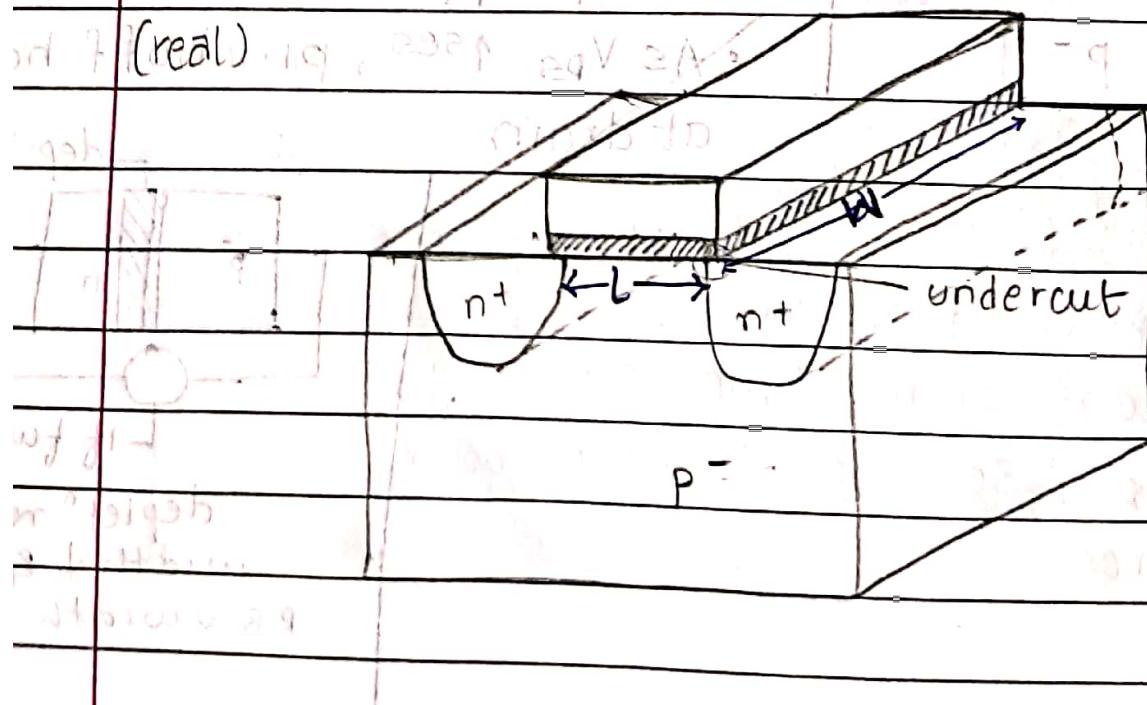
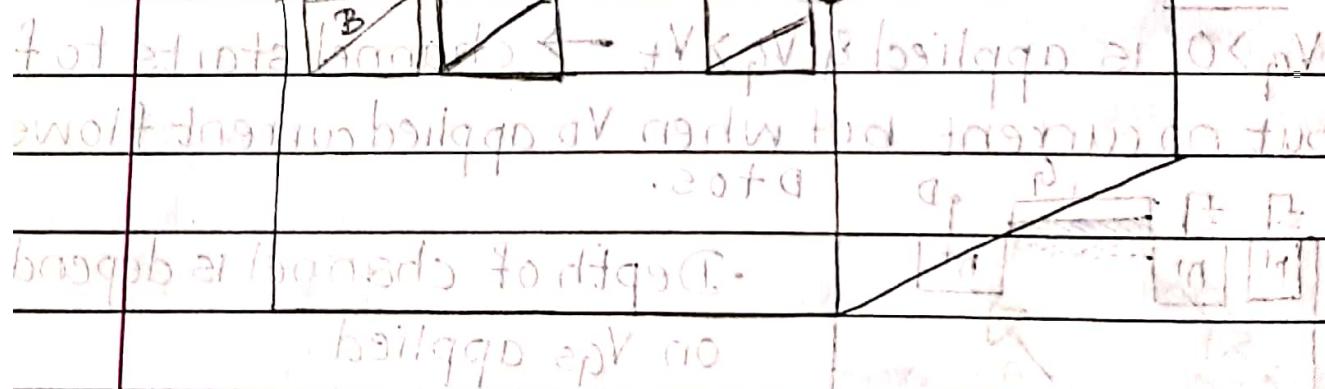
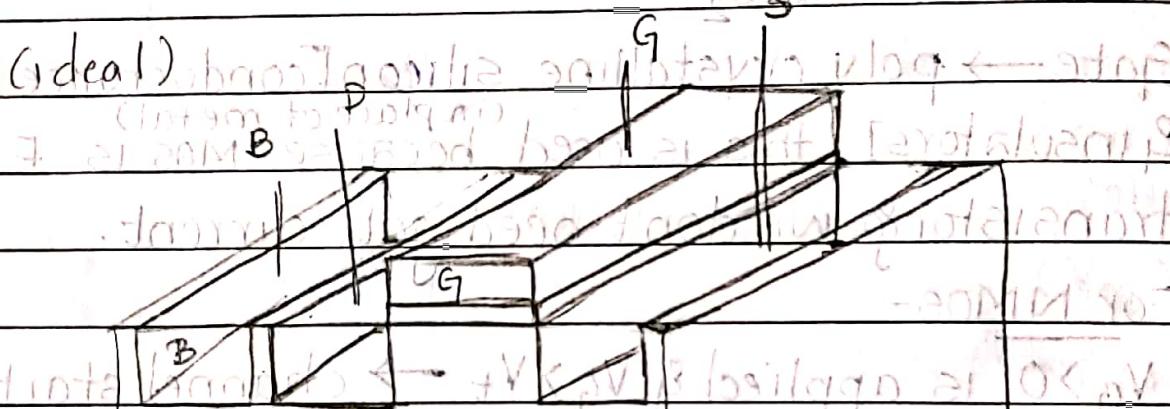
Lif fwd-bias  
depletion region width  $\propto$   $I_f^2$   
 $R_B \propto$  width  $\propto$

Form PMOS -



Gate voltage  $< 0$  or  
gate should be at lower  
potential than bulk for  
channel performance.

## Parasitic Capacitance of MOS -



## Capacitances -

\* b/w gate & bulk [because of its structure ie MOS] called intrinsic capacitance.

$$C = \frac{EA}{d} = \epsilon_0 \epsilon_r A$$

A → Area of plate =  $w \times l$

d → separat<sup>n</sup> - thickness of  $\text{SiO}_2$  [in terms of  $\text{\AA}$ ]

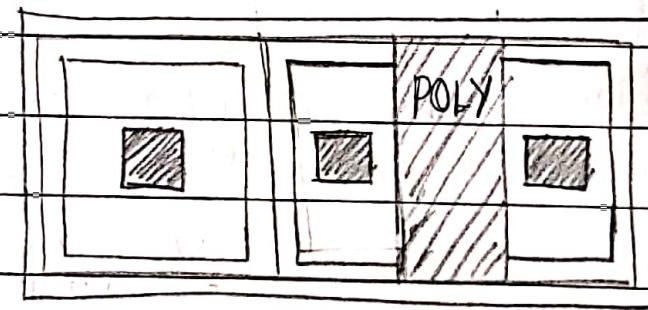
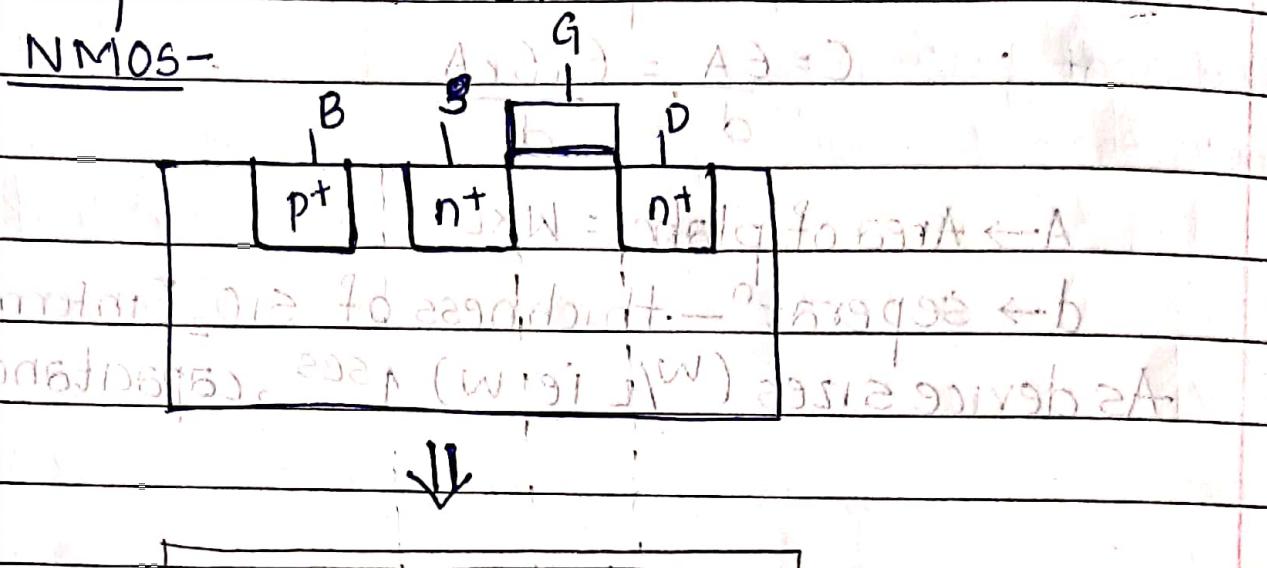
As device sizes ( $w/L$  ie  $w$ ) ↑ses, capacitance ↑ses

## Summary of videos -

MOSFET structure to ground d<sub>1</sub> d<sub>2</sub> d<sub>3</sub> d<sub>4</sub> width (W)

### \* Layout of MOSFET -

NMOS -



### \* Photolithographic sequence is -

    i) Photo resist application

    ii) Printing or Exposure

    iii) Development

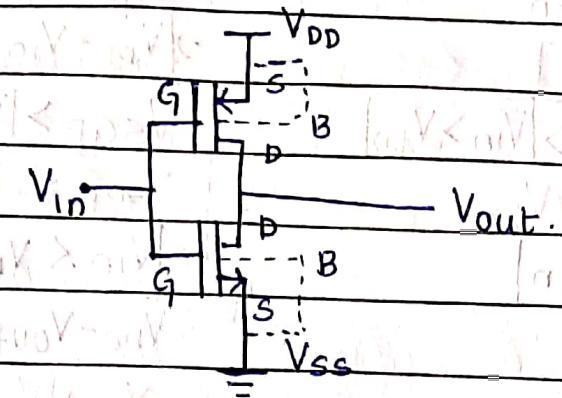
    iv) Etching

photoresist → +ve photoresist (when exposed to sun light, it softens / hardens)  
 → -ve " (when exposed to UV, it hardens)

- Metal mask is used to pattern photoresist, solidified photoresist acts as a mask to pattern  $\text{SiO}_2$ . Lastly,  $\text{SiO}_2$  acts as a mask to pattern the silicon.

(dynamic)  
Transient ch. of CMOS  $\rightarrow V_{out}$  vs time

### CMOS Inverter -



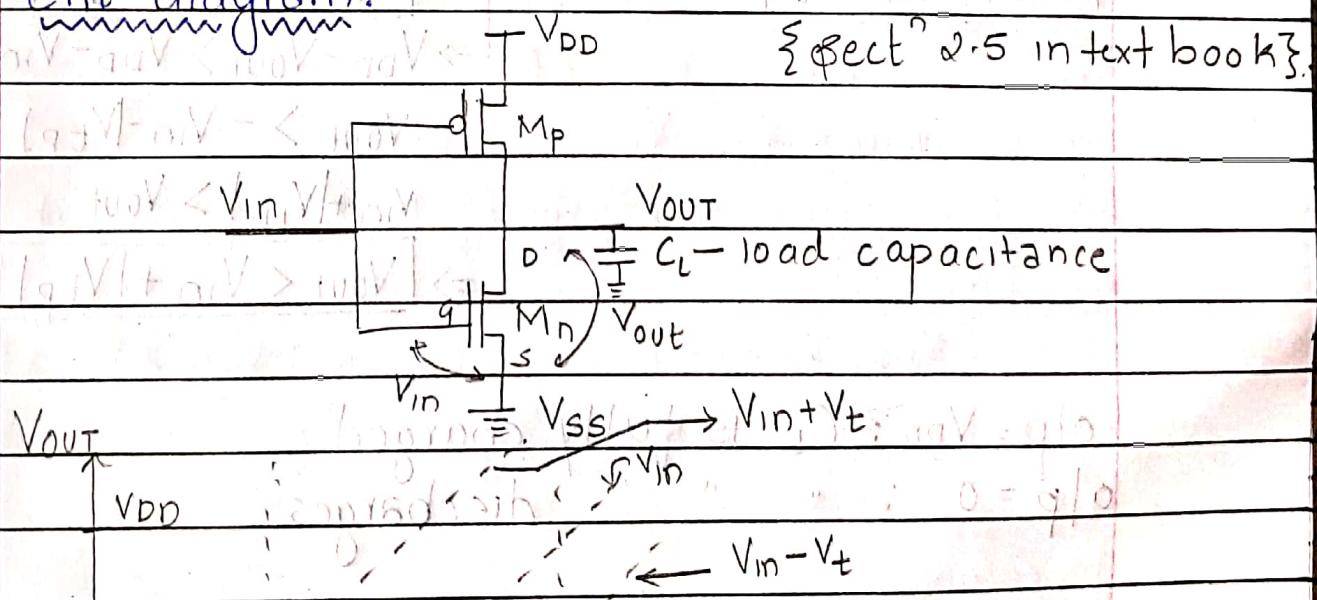
(static)

### DC characteristics of CMOS inverter:-

(or transfer characteristics)  $\rightarrow V_{in}$  vs  $V_{out}$ .

- Voltage levels, switching points, Noise margin.

Ckt. diagram:-



noise margin  $(V_{in} - V_t)$   $\rightarrow$   $(P.T.O)$

output noise margin  $(V_{DD} - V_{out})$   $\rightarrow$   $(V_{DD} - V_{out})$

input noise margin  $(V_{in} - V_t)$   $\rightarrow$   $(V_{in} - V_t)$

input recovery period  $\rightarrow$   $(V_{in} - V_t)$   $\rightarrow$   $(V_{in} - V_t)$

saturation time  $\rightarrow$   $(V_{in} - V_t)$   $\rightarrow$   $(V_{in} - V_t)$

N-MOS :-

cutoff :-

$$V_{GSn} \leq V_{tn}$$

P-MOS :  $V_{SGP} = V_{DD} - V_{in}$

$$(V_{SP} - V_{AP}) = V_{DD} - V_{in}$$

$$V_{SGP} \leq |V_{tp}| \Rightarrow V_{in} \geq V_{bp}$$

$$\Rightarrow V_{DD} - V_{in} \leq |V_{tp}|$$

Triode :-

$$(V_{in}) V_{GSn} > V_{tn} \Rightarrow V_{in} > V_{tn}$$

$$V_{SGP} > |V_{tp}| \Rightarrow$$

$$V_{SDP} < V_{SGP} - |V_{tp}|$$

$$\Rightarrow V_{in} < V_{DD} - |V_{tp}|$$

$$V_{DD} - V_{out} < V_{DD} - V_{in} - |V_{tp}|$$

$$V_{in} + |V_{tp}| < V_{out} \Rightarrow V_{out} > V_{in} + |V_{tp}|$$

Saturation:..  $(V_{in}) V_{GSn} > V_{tn} \Rightarrow V_{in} > V_{tn}$

$$V_{SGP} > |V_{tp}|$$

$$V_{SDP} > V_{SGP} - |V_{tp}|$$

$$\Rightarrow V_{in} < V_{DD} - |V_{tp}|$$

$$V_{DD} - V_{out} > V_{DD} - V_{in} - |V_{tp}|$$

$$-V_{out} > -V_{in} - |V_{tp}|$$

$$V_{in} + |V_{tp}| > V_{out}$$

$$\Rightarrow V_{out} < V_{in} + |V_{tp}|$$

$\alpha_{lp} = V_{DD} : C_L$  is fully charged

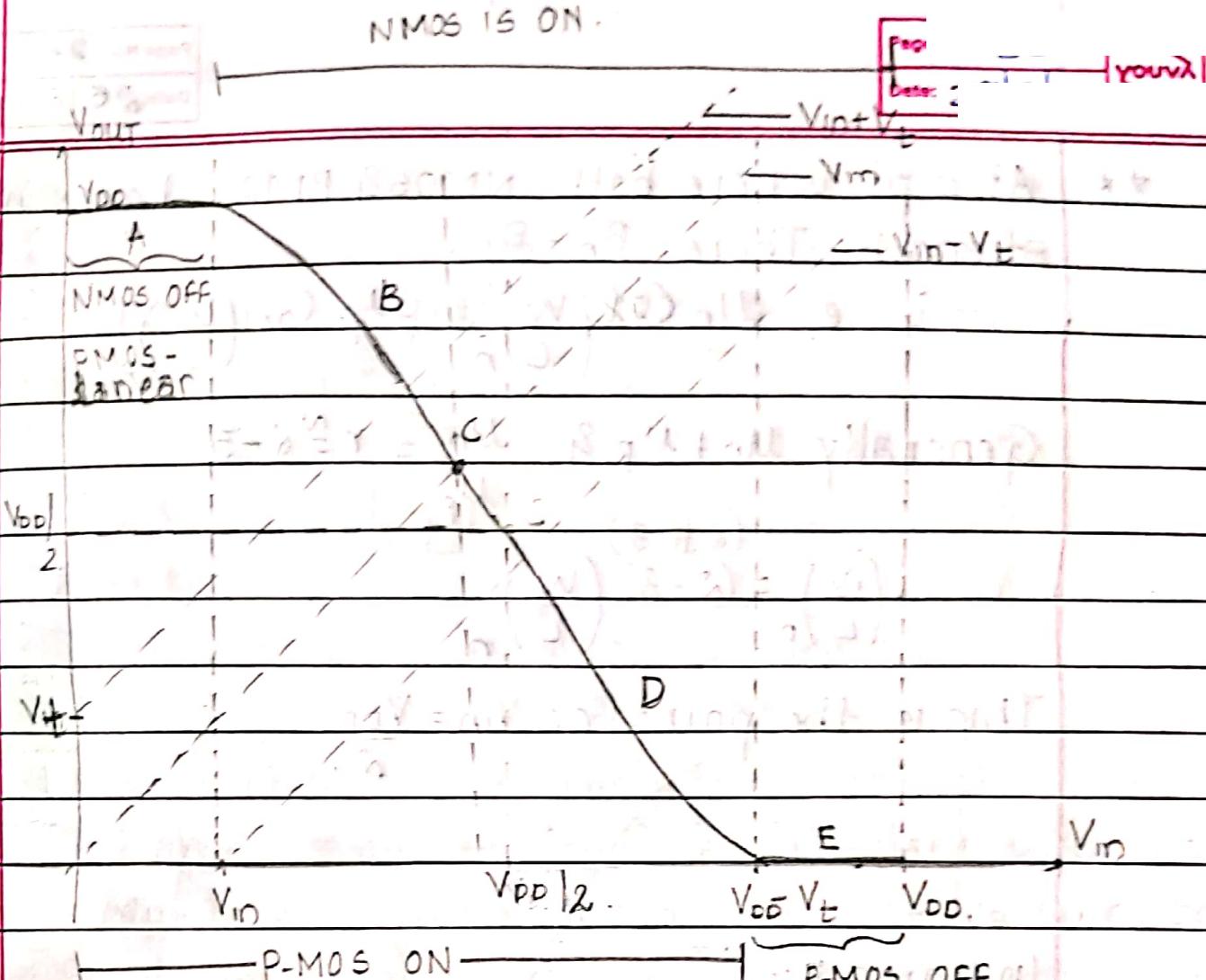
$\alpha_{lp} = 0 : " " "$  discharges

\*\* In region blw A & E -

$\Rightarrow$  since  $V_{AS}$  is  $\uparrow$ ing  $\Rightarrow I \propto (V_{AS} - V_t)$  since gatedrive is  $\uparrow$ ing, N-MOS is becoming more stronger whereas

$V_{SGP} = V_{DD} - V_{in}$ ,  $V_{SGP}$   $\downarrow$ es & P MOS becomes  $\downarrow$  less stronger compared to NMOS. At apt. both have same strength  $[\beta_n = \beta_p]$   $\Rightarrow \mu_n Cox(\frac{W}{L}) = \mu_p Cox(\frac{W}{L})_p$

NMOS IS ON.



In region A:

- $V_{in} < V_t \Rightarrow$  NMOS is OFF & PMOS is ON

$V_{in} < V_{DD} - V_t \Rightarrow$  PMOS is ON.

- For region A  $\rightarrow V_{out} = V_{DD}$

Now in region A - for all  $V_{in} \in 0$  to  $V_t$ ,  $V_{out} > V_{in} + V_t$

$\therefore$  PMOS is in linear region.

In region E:

- $V_{in} > V_{DD} - V_t$

PMOS is cut off & NMOS is ON.

$$V_{out} = 0$$

- $V_{in} > V_{DD} - V_t \& V_{out} = 0 < V_{in} - V_t$

$\therefore$  NMOS is in linear region.

★ At a pt where both NMOS & PMOS have same strength. There  $B_n = B_p$ .  
 ie  $\mu_n C_{ox} \left(\frac{W}{L}\right)_n = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$

Generally  $\mu_n + \mu_p \approx \mu_p$  &  $\mu_n = r \approx 2-3$

$$\therefore \left(\frac{W}{L}\right)_p = (2-3) \left(\frac{W}{L}\right)_n$$

This is the point c:  $V_{in} = \frac{V_{DD}}{2}$ .

In region B:-

•  $V_{in} > V_t \Rightarrow$  NMOS is ON

& also  $V_{out} > V_{in} - V_t$  till pt c.

∴ Till pt c [also in region c] NMOS is in saturation

• For PMOS:-

$V_{in} < V_{DD} - V_t \Rightarrow$  PMOS is ON and  $V_{out} > V_{in} + V_t$

∴ PMOS is in linear region.

In region c:-

•  $V_{in} > V_t \rightarrow$  NMOS is ON

and  $V_{out} = V_{in} - V_t \rightarrow$  NMOS is in saturation.

•  $V_{in} < V_{DD} - V_t \rightarrow$  PMOS is ON

•  $V_{out} = V_{in} + V_t$

∴ PMOS is in saturation.

DC static transfer characteristics  $\rightarrow$  switching pt

→ Noise margin  
Voltage levels

In region D:

- $V_{in} > V_t \rightarrow$  NMOS ON

•  $V_{out} < V_{in} - V_t \rightarrow$  NMOS is in linear region.

- $V_{in} < V_{DD} - V_t \rightarrow$  PMOS ON

•  $V_{out} < V_{in} - V_t \rightarrow$  PMOS is in saturation region.

CMOS ckt:

- To extend  $V_{out}$  → press **ctrl** → extend & double click to terminate. Press **p** to add pin → enter pin name → OK.
- Now to check by changing the width of PMOS.

click on **PMOS** → properties → declare total width as  $W_p$ . Now do parametric analysis of  $W_p$  [240n to 2μ] → Point where o/p curve &  $V_{in}$  curve intersects, the pt is called switching point.

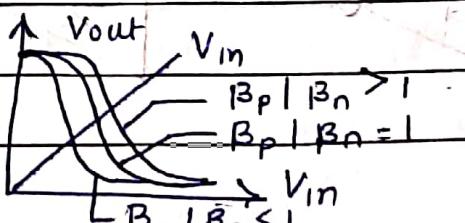
$$\frac{B_p}{B_n} = \frac{W_p}{W_n} = \frac{1.16\mu}{240n} = 4.83$$

\* When  $B_p/B_n = 1 \rightarrow$  switching pt is at  $V_{DD}/2$ .

\* If  $B_p/B_n > 1 \Rightarrow$  PMOS is more stronger  $\therefore$  NMOS needs more drive to pull voltage down. (more  $V_{in}$ )

$\therefore$  o/p will be at  $V_{DD}$  for more time  $\therefore$  the curve shifts right.

\* If  $B_p/B_n < 1 \Rightarrow$  NMOS is stronger,  $\therefore$  PMOS needs to be having larger drive.  $\therefore$  curve shifts to left & o/p curve will be more at 0V.



## Voltage levels -

Symbols :-

- $V_{OL}$  → Worst case output voltage low (near 0 but not 0)
- $V_{OH}$  → " " high (slightly  $< V_{DD}$ )
- $V_{IL}$  → " " low (slightly  $> 0$ )
- $V_{IH}$  → " " high (slightly  $< V_{DD}$ )

$V_{out}$

Plot of  $V_{out}$  vs  $V_{in}$  showing slope = 0 at  $q = q_2$  &  $q_1$  against

slope = -1 at  $q = q_3$

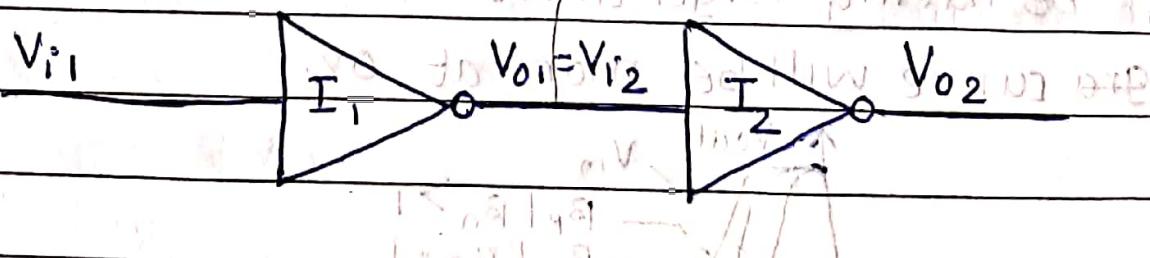
$V_{OH}$  is plotted using  $I_{DD} = 20mA$  on graph paper.

$V_{OD}$  for  $V_{DD} = 18V$  is also plotted on graph paper.

$V_{OL}$  is plotted using  $I_{DD} = 20mA$  on graph paper.

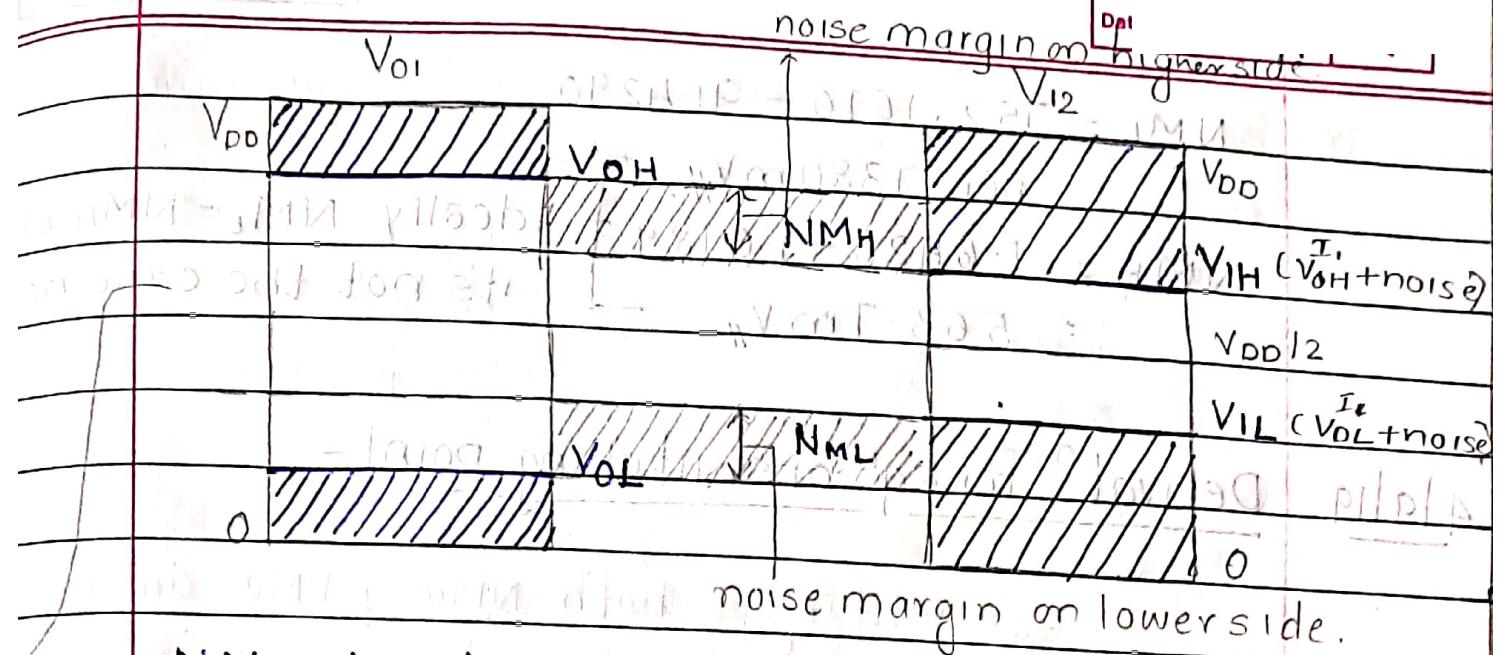
Margins for voltage (lop) levels are pts on curve where the slope =  $-1$ .

Noise margin :-



$V_{O1}$  is not completely equal to  $V_{I2}$  because of the channel.

Pac  
Dat



$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

For a symmetric inverter ( $B_p = B_n = 1$ )  $\rightarrow NM_H = NM_L$   
 {when  $B_p \neq B_n \neq 1 \rightarrow$  skew inverter}

For getting the switching pt at  $V_{DD}/2 \rightarrow w_p = 1.16\mu$

For finding noise margin:

On curve mark a pt (M) & another by clicking "d" (delta), move the point so that the 2 pts coincide when curve is fit to screen.

The two marked pts for first pt with slope -1 are A(746.683m, 1.64812V) & B(757.651m, 1.63705V)

$$\text{To get } V_{OH} = 1.64812 + 1.63705 = 1.6426V$$

$$22V - 21V = 1V - 2V^2$$

$$V_{IL} = 746.683m + 757.651m = 752.1670mV$$

2

The two marked pts for 2nd pt with slope = -1 are C(1.07593, 94.3929mV), D(1.08184, 88.4651)

$$V_{OL} = 91.4290mV \quad V_{IH} = 1.0789.$$

$$NM_L = 752.1670 - 91.4290$$

$$= 660.7380 \text{ mV}_H$$

$$NM_H = 1.6426 - 1.0789$$

$$= 563.7 \text{ mV}_H$$

Ideally  $NM_L = NM_H$  but it's not the case here

## 4.9.19 Derivat' foreq' of switching-point-

V<sub>DD</sub>

At switching pt. both NMOS & PMOS are on & current (crossbar/crowbar current) flows b/w

V<sub>DD</sub> & V<sub>SS</sub>  $\Rightarrow V_{DD} - V_{SS} = HV - NOV = NMH$

For switching point-

$$V_M = V_{in} = V_{out}$$

Both N & PMOS are in saturation

Current through PMOS-

$$I_{DS(p)} = \frac{\mu_p C_{ox} (w)}{L} [V_{GS} - V_{tp}]^2 = \beta_p [V_{GS} - V_{tp}]^2$$

Current through NMOS-

$$I_{DS(n)} = \frac{\mu_n C_{ox} (w)}{L} [V_{GS} - V_{tn}]^2 = \beta_n [V_{GS} - V_{tn}]^2$$

$$\beta_p = \frac{V_{GS} - V_{tn}}{V_{GS} - V_{tp}} = \frac{V_{GS} - V_{tn}}{[V_{GS} - V_{tp}] + V_{GS} + V_{tp}}$$

$$\beta_n = \frac{V_{GS} - V_{tn}}{V_{GS} - V_{tp}} = \frac{V_{GS} - V_{tn}}{[V_{GS} - V_{tp}] + V_{GS} + V_{tp}}$$

$$\beta_n [V_{tn} - V_{GS}] = V_{GS} + V_{tp}$$

$$V_{GS} = V_{tp} - V_{tn}$$

$$V_{tn} \frac{B_n - |V_{tp}|}{B_p} = V_{GS} \left[ 1 + \sqrt{\frac{B_n}{B_p}} \right] \text{ (1)}$$

$$V_{GS} = V_{tn} \sqrt{\frac{B_n - |V_{tp}|}{B_p}}$$

$$1 + \sqrt{\frac{B_n}{B_p}} = \frac{V_{GS} + V_t}{|V_{tp}|}$$

$$V_G - V_S = V_{tn} \sqrt{\frac{B_n - |V_{tp}|}{B_p}}$$

$$1 + \sqrt{\frac{B_p}{B_n}} = \frac{V_S + V_t}{|V_{tp}|}$$

$$V_M = V_G = V_{DD} - |V_{tp}| + V_{tn} \sqrt{\frac{B_n}{B_p}}$$

$$1 + \sqrt{\frac{B_n}{B_p}} = \frac{V_M + V_t}{|V_{tp}|}$$

$$\text{if } B_p = B_n \text{ & } V_{tn} = |V_{tp}| \quad 1 + \sqrt{\frac{B_n}{B_p}} = 1$$

$$V_M = \frac{V_{DD}}{2}$$

Q) Calculate switching pt. of CMOS inverter which has-

$$B_n = \text{device transconductance} = 2 \cdot 1mA/V^2$$

$$B_p = 1.8mA/V^2 \quad * V_M = V_{DD}/2 \Rightarrow \text{curve shifts toward}$$

$$V_{tn} = 0.6V \quad \text{-ards left.}$$

$$V_{tp} = -0.7V \quad 10 - 0.7 = 9.3V - 1V = 8.3V = 1.0801$$

$$V_{DD} = 5V \quad 5 - 0.7 = 4.3V - 1V = 3.3V = 1.0801$$

$$\rightarrow V_M = V_{DD} - |V_{tp}| + V_{tn} \sqrt{\frac{B_n}{B_p}} = 5 - 0.7 + (0.6)(1.0801)$$

$$1 + \sqrt{\frac{B_n}{B_p}} = \frac{2.0801}{1.0801} = 2.379V$$

★ For noise Margin of a symmetric inverter-  
Assume for a symmetric inverter-

$$V_{OL} \approx 0V$$

$$V_{OH} \approx V_{DD}$$

$$V_{tn} \approx |V_{tp}| = V_t$$

$$V_{IL} = \frac{1}{8} [3V_{DD} + 2V_t]$$

$$V_{IH} = \frac{1}{8} [5V_{DD} - 2V_t]$$

Q) Find Noise margin for-

$$V_{DD} = 3.3V \quad |at V_I + |at V_O - |at V = 0V = MV$$

$$V_{tn} = |V_{tp}| = 0.7V$$

$$V_{OL} = 0V$$

$$V_{OH} = V_{DD} = 3.3V$$

$$V_{IL} = \frac{1}{8} [3V_{DD} + 2V_t]$$

$$= 1.4125V$$

$$V_{IH} = \frac{1}{8} [5V_{DD} + 2V_t] \quad \text{for condition A (10)}$$

$$= 1.8875V$$

$$NML = V_{IL} - V_{OL} = 1.412 - 0 = 1.412V$$

$$NMH = V_{OH} - V_{IL} = 3.3 - 1.8875 = 1.4125V$$

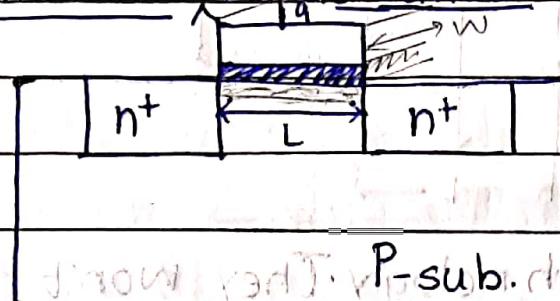
$$NML + NMH = 2.825V$$

$$1.080 \cdot 5$$

## Transient Analysis -

Capacitance - intrinsic (wanted capacitance)  
parasitic (unwanted " )

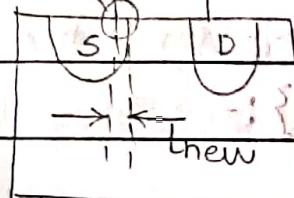
### Intrinsic Capacitance -



$$C_{gb} \text{ (gate to bulk) at cutoff} = \frac{C = EA = \epsilon_{SiO_2} \times (L \times w)}{d}$$

$$= E_{ox} \frac{(w \times L)}{t_{ox}}$$

For an undercut, there is a constant



IS Cgs & Cgd during  
out off too called

$$C_{gb} = C_{ox} (w \times l) = C_0$$

Cgs(overlap) & Cgd(coverlapped) oxide capacitance

$$C_{gb} = \frac{C_{ox} (w \times l_{new})}{t_{ox}} \text{ per unit area.}$$

Cutoff,  $C_{gb} = 0$  since no ch. formed so no connect blw S or D from G.

triode  $0 \quad C_{ol/2} \quad C_{ol/2}$

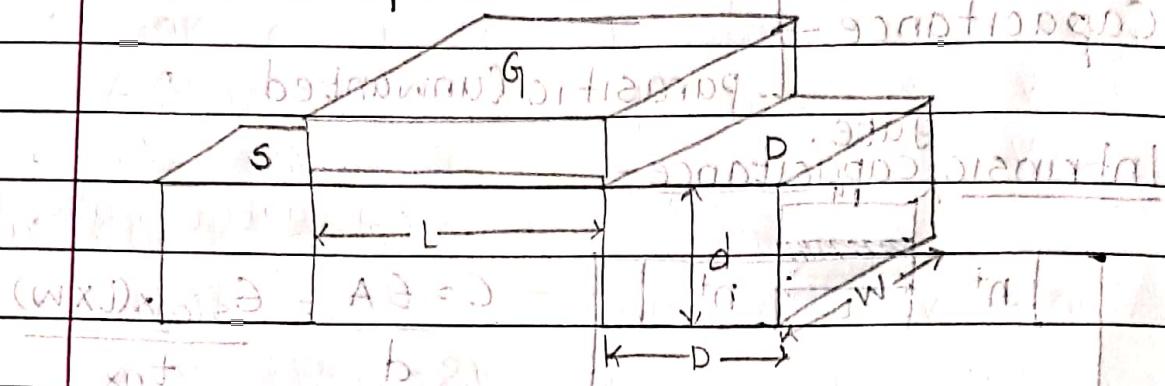
Saturation  $0 \quad 2/3 C_0 \quad 0$

- In triode, a uniform channel will form beneath  $SiO_2$ , So connect blw G and S/D is established & blw G & D is cut off. Capacitance won't change since  $C_{ox}$ ,  $w$  or  $L$  aren't changed & is equally distributed as  $C_{gs}$  &  $C_{gd}$

- In saturation, pinchoff happens and connect blw G & D is cut off and  $C_{gd} = 0$  but  $C_{gs} \neq C_0$  since area of bottom place < area of top plate because of pinchoff so now  $C_{gs} = \frac{2}{3} C_0$ .

Typically thickness of gate dielectric is determined

## Parasitic Capacitance



(d & D are fixed for a technology. They won't change if device size changes. If device size changes only L & W may change.)

$C_s = C_d$  {similar for Drain} :-

constant Area of source =  $A_s = D \cdot W$

for a technology Perimeter of source =  $P_s = 2D + 2W$

junct capo  $C_{jbs} = \text{bottom wall capacitance of source per unit area}$

junct  $C_{jbs-sw} = \text{sidewall capacitance of source per unit length}$

Overall bottom wall capacitance =  $C_{jbs} \times A_s$

Overall sidewall capacitance =  $C_{jbs-sw} \times P_s$

In sidewall  $\rightarrow$  3 faces face bulk & one faces the gate. So, there are 2 diff. capacitances

$C_{jbs-sw} = \text{sidewall capacitance which faces the gate per unit length.}$

∴ Overall capacitance =  $C_s$  (bulk) +  $C_{jbs}$  (bottom)

$$C_s = (C_{jbs}) A_s + C_{jbs-sw} W + C_{jbs-sw} (2D + W)$$

To minimize total cap to min.  $\Rightarrow$  single method to min.

If there's Reverse bias  $\rightarrow$  as dep. layer increases with  
 $\uparrow$  in RB :  $C = \epsilon A / d$   $\downarrow$  ses.

$$\therefore \text{The junct. capacitance} = C_{jbs} = C_j [1 + V_{sb}]^{-M_J}$$

$\rightarrow$   $V_{sb}$  at (forming) long tunnel bias  $\Psi_0$

$100V$  at (forming) junction gradient coefficient

$$\therefore C_s = [1 + V_{sb}]^{-M_J} C_{jbs} As + C_{jbs} swg \cdot W [1 + V_{sb}]^{-M_{JSW}} \frac{\Psi_0}{\Psi_0}$$

$$+ C_{jbs} sw (2D + W) [1 + V_{sb}]^{-M_{JSW}}$$

(Bulk gradient & short channel fringe effect)

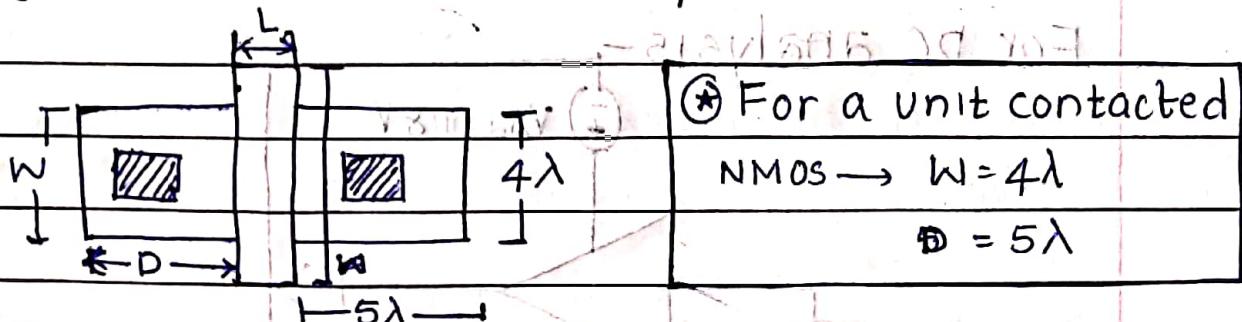
found how to add drain offset and short

Q) Calculate the diffusion parasitic  $C_{ab}$  of drain of a unit sized contacted NMOS transistor in a 180nm process, when the drain is at  $0V$ , at  $V_{DD} = 1.8V$ .

Assume the substrate is grounded. Transistor characteristics are  $\rightarrow C_j = 0.98 fF/\mu m^2$

$$C_{JSW} = 0.22 fF/\mu m \quad \& \quad C_{JSW-G} = 0.33 fF/\mu m$$

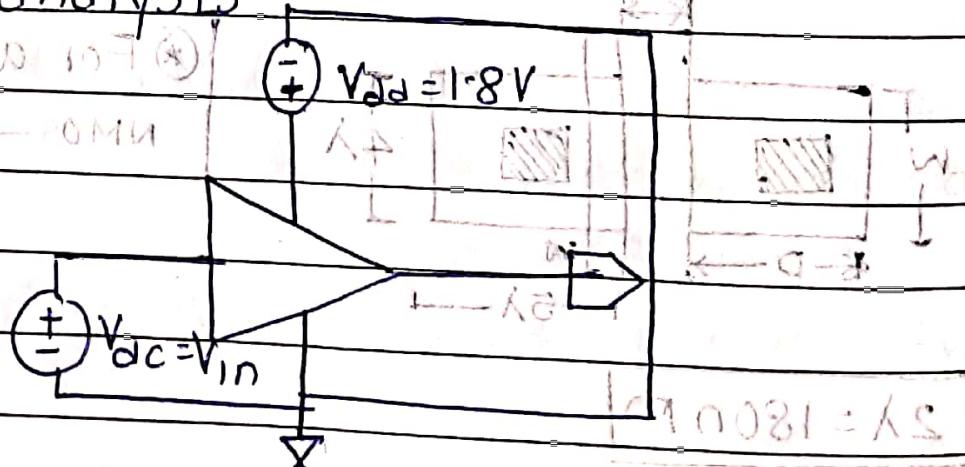
$$M_J = 0.36 \text{ and } M_{JSW} = M_{JSWg} = 0.1 \quad \& \quad \Psi = 0.75V$$



## Making symbol (inverter) from schematic:

- Make a sch. w/o the power supply & ground.
- Add input pin (press p) to  $V_{in}$ ,  $V_{DD}$ ,  $V_{SS}$
- " output " (" → output) to  $V_{out}$ .
- Check & save
- Create → cell view → From cellview → OK → (respectively enter details) → OK → (one box with some rectangular box is generated) → (Delete the outer box & also inner box if you want sch. of diff. type) → [Now to create {>} inverter symbol] create → shape → polygon (& draw required shape) → (Save the symbol)
- Go to virtuoso tool → Tools → library manager → In your library create a new file (cell-view) & by pressing I - select your symbol & do the dc

For DC analysis -



For transient Analysis → run in simulation

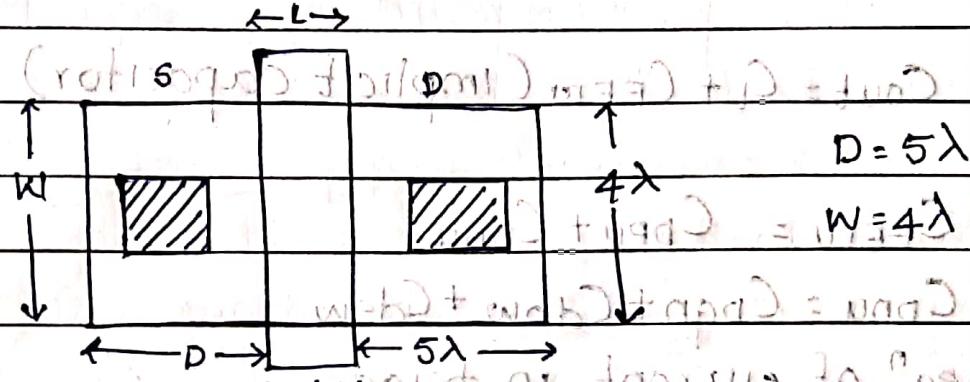
Replace ( $V_{ac} = V_{in}$ ) by  ~~$V_{pulse}$~~   $V_{pulse} \rightarrow$  Voltage 1 = 0V

Voltage 2 = 1.8V period = 100 ns & pulse width = 50 ns

Goto Analyses → trans → stop time = 200 ns, accuracy defaults = moderate → OK → output → to be plotted (select ilp & olp net) → (plot) → (in graph) split all str.

Fig

3).



$$2\lambda = 180 \text{ nm}$$

$$\lambda = 90 \text{ nm}$$

$$D = 5\lambda = 450 \text{ nm} = 0.45 \mu\text{m}$$

$$W = 4\lambda = 360 \text{ nm} = 0.36 \mu\text{m}$$

$$C_{db} = C_J \cdot W \cdot D + C_{Jswg} \cdot W + C_{Jsw} (2D + W)$$

$$C_{JWD} = 0.98 \times 10^{-15} * 0.4 \times 0.36 \times 10^{-12}$$

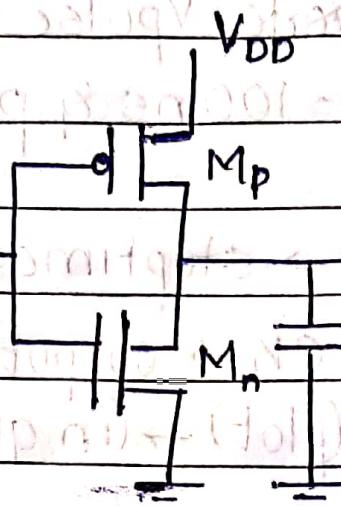
$$= 0.15876 \text{ fF}$$

$$C_{Jswg} \cdot W = 0.33 \times 10^{-15} \times 0.36 \times 10^{-12} = 0.1188 \text{ fF}$$

$$C_{Jsw} (2D + W) = 0.22 \times 10^{-15} (2 \times 0.45 \times 10^{-12} + 0.36 \times 10^{-12}) \\ = 0.2772 \text{ fF}$$

$$C_{db}(0V) = 0.15876 + 0.1188 + 0.2772 \\ = 0.55476 \text{ fF}$$

# Modelling of inverter using R&C



$$C_{out} = C_L + C_{FETU} \text{ (implicit capacitor)}$$

$$C_{FETU} = C_{DPU} + C_{DNU}$$

$$C_{DNU} = C_{DGNT} + C_{DBW} + C_{DSW}$$

eq<sup>n</sup> of current in triode -

$$I_D = \beta \left[ (V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$V_{DS} \ll V_{DD}$$

$$\therefore I_D \approx \beta \left[ (V_{GS} - V_{TN}) V_{DS} \right]$$

$$\frac{\partial I_D}{\partial V_{DS}} = \beta_n [V_{DD} - V_{TN}]$$

$$R_n = 1$$

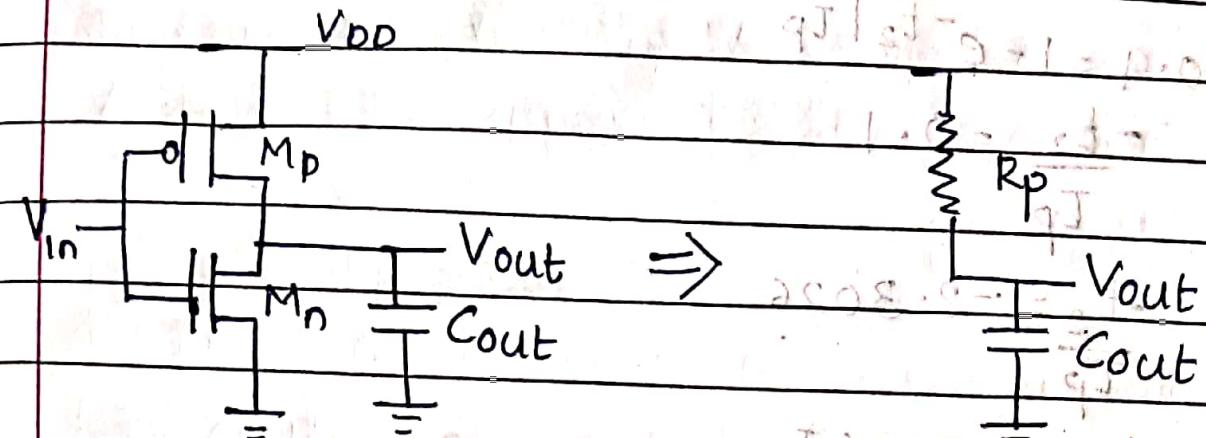
$$97.891 \beta_n (V_{DD} - V_{TN}) \times 10^{-12} = 77.258 \times 10^{-12}$$

$$(2 \times 10^{-12} \times 8.8 \times 10^{-12} + 2 \times 10^{-12} \times 0.4 \times 10^{-12}) \times 10^{-12} \times 8.8 \times 10^{-12} = 1.6 \times 10^{-12}$$

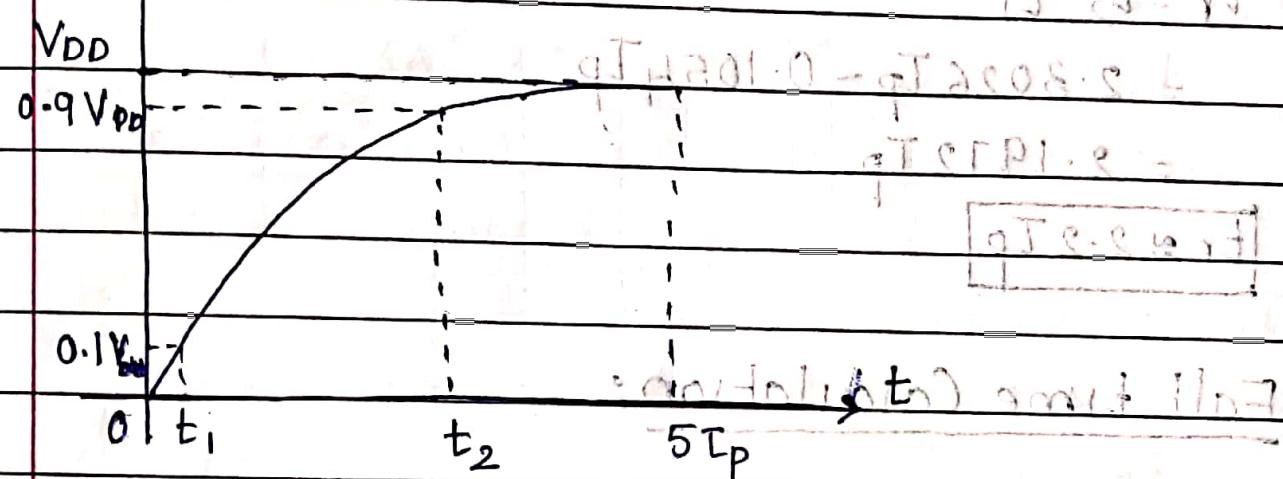
$$R_p = 1$$

$$\frac{B}{P} (V_{DD} - V_{TN})$$

## Rise time calculation:-



$$\text{Time constant } T_p = R_p C_{out}$$



$$t_r = t_2 - t_1$$

$$V_{\text{charging}} = V_{out} = V_{DD} [1 - e^{-t_1/T_p}]$$

$$0.1V_{DD} = V_{DD} [1 - e^{-t_1/T_p}]$$

$$0.1 = 1 - e^{-t_1/T_p}$$

$$e^{-t_1/T_p} = 0.9$$

$$\frac{-t_1}{T_p} = -0.1054$$

$$t_1 = 0.1054 T_p$$

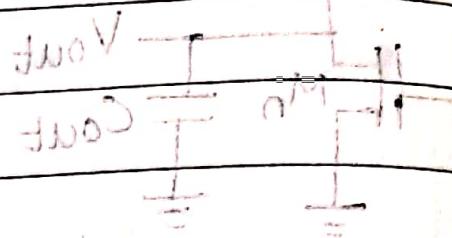
$$0.9V_{DD} = V_{DD}(1 - e^{-t_2/T_p})$$

$$0.9 = 1 - e^{-t_2/T_p}$$

$$\frac{-t_2}{T_p} = 0.1$$

$$\frac{-t_2}{T_p} = -2.3026$$

$$t_2 = 2.3026 T_p$$



$$t_r = t_2 - t_1$$

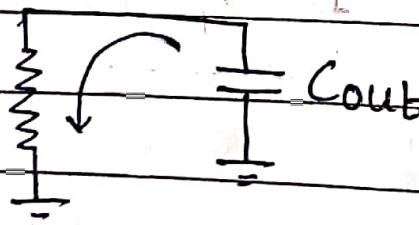
$$= 2.3026 T_p - 0.1054 T_p$$

$$= 2.1972 T_p$$

$$t_r \approx 2.2 T_p$$

### Fall time Calculation:

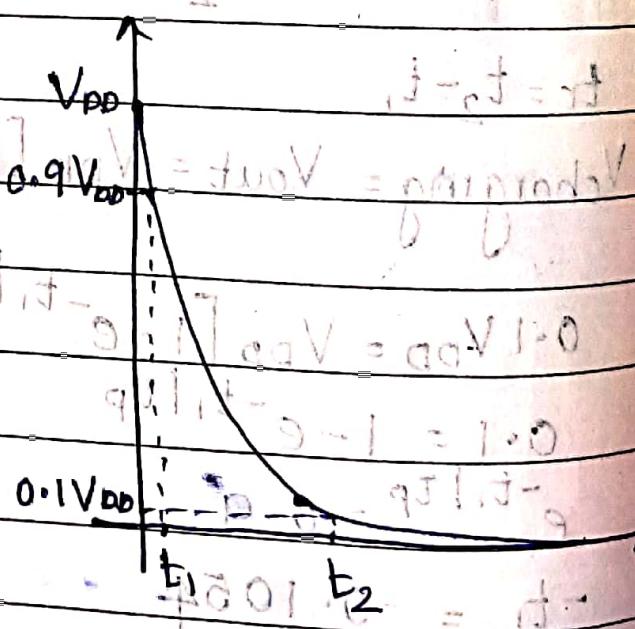
$$V_{out} = V_{DD} [e^{-t/T_n}]$$



$$0.9V_{DD} = V_{DD} [e^{-t_1/T_n}]$$

$$0.9 = e^{-t_1/T_n}$$

$$\frac{-t_1}{T_n} = -0.1054$$



$$qJ + 201.0 = 1.0$$

1468 00009

3.10/10 000

$$t_1 = 0.1054 T_n \text{ (from question 1a part 2001) } \quad \text{and} \quad t_2 = -0.3026 T_n \quad (Q)$$

$$0.1 V_{DD} = V_{DD} [e^{-t_2/T_n}] \quad (0.1 = 0.1) \quad 8 = e^{-t_2/T_n} \quad (1W)$$

$$0.1 = e^{-t_2/T_n} \quad (t_2 = -0.3026 T_n) \quad \sqrt{8} = \sqrt{0.1} \quad \sqrt{23.07} = 0.1V$$

$$e^{-t_2/T_n} = 0.1$$

$$\frac{-t_2}{T_n} = -0.23026$$

$$T_n$$

$$(0.1V - 0.0V) \text{ qf}$$

$$t_2 = 2.3026 T_n$$

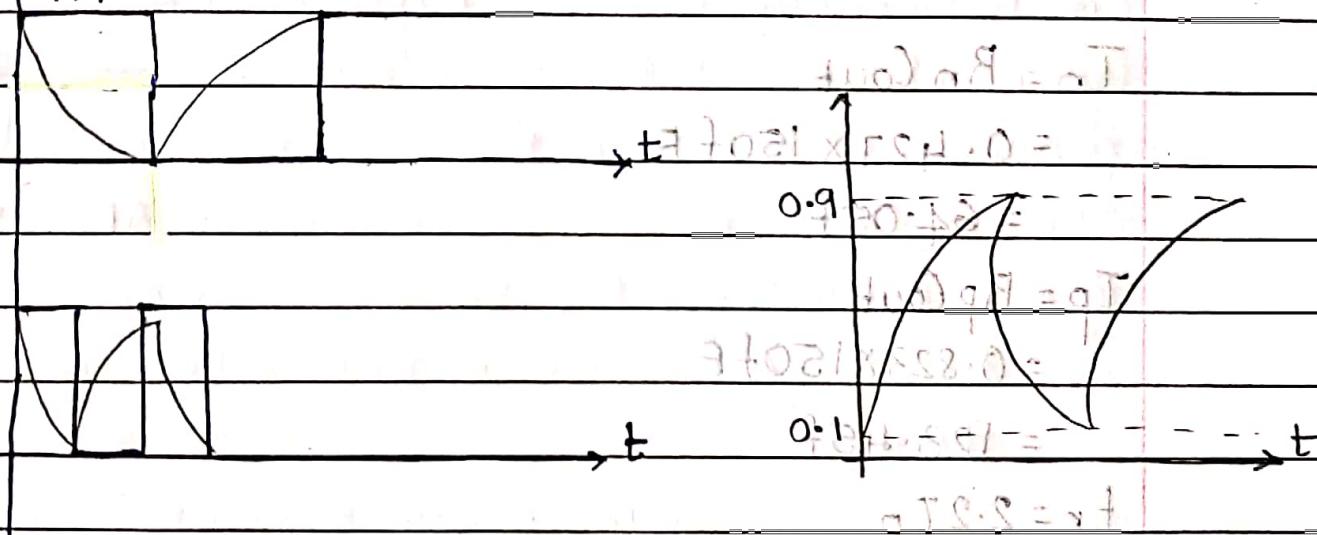
$$t_f = t_2 - t_1$$

$$= 2.3026 T_n - 0.1054 T_n = 2.1972 T_n$$

$$t_f = 2.1972 T_n$$

$$t_f \approx 2.2 T_n$$

$$V_{out}$$



$$t_{min} = t_r + t_f$$

$$f_{max} = 1 = 1$$

$$t_{min} = t_r + t_f \quad \text{MAX} \cdot 0.1 = 0.78 \cdot 2 = 23$$

$$23 \cdot 0.1 = 2.3 \text{ ms}$$

$$= 2.3 \text{ ms}$$

Q) The CMOS inverter of parameter  $[W/L]_{n\text{-mos}} = 6$   
 $[W/L]_{p\text{-mos}} = 8$ ,  $k_n' = 150 \mu A/V^2$ ,  $k_p' = 62 \mu A/V^2$ ,  $V_{tn} = 0.7V$   
 $V_{tp} = -0.85V$ ,  $V_{DD} = 3.3V$ ,  $C_{out} = 150fF$ . Find maximum  
 1/p frequency.

$$B_n = \frac{1}{B_n(V_{DD} - V_{tn})}$$

$$= \frac{1}{390 \times 10^{-6} \times 6} = 0.427 \Omega$$

$$B_p = \frac{1}{B_p(V_{DD} - V_{tp})} = \frac{1.519 \times 10^{-4} \times 8}{0.823 \Omega}$$

$$T_n = R_n C_{out}$$

$$= 0.427 \times 150fF$$

$$= 64.05f$$

$$T_p = B_p C_{out}$$

$$= 0.823 \times 150fF$$

$$= 123.45f$$

$$t_r = 2.2 T_p$$

$$= 2.2 \times 123.45$$

$$= 271.59fs$$

$$t_f = 2.2 T_n = 2.2 \times 64.05f = 140.91fs$$

$$f_{max} = \frac{1}{t_r + t_f} = \frac{1}{271.59fs + 140.91fs}$$

$$= 2.4GHz$$

$$tpdIH = t_0 - 0.5V_{in}$$

$$tpdHL = t_0 + 0.5V_{in} - 0$$

$$\therefore tpd = tpdIH + tpdHL$$

$$tpd = 0.35(T_n + T_p)$$

$V_{in}$

$0.5V_{in}$

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

$t_1$

$t_2$

$tpdIH$

$tpdHL$

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

onset of turn-on = 0A

saturation = 1A

onset of turn-off = 0A

saturation = 0A

## RC-analysis-

Capacitor  $\rightarrow$  500fF to 1pF

From symbol to schematic - select symbol  $\rightarrow$  shift+E  $\rightarrow$  enter

To come back to symbol - check & save  $\rightarrow$  cntl+E

Rise time  $\rightarrow$  10% to 90% (0.1p)

Fall "  $\rightarrow$  90% to 10% (0.1p)

Rise delay  $\rightarrow$  time when 0.1p is 50% - time when 1p is 50%  
(while rising)

To plot risetime - & get value of rise time.

In ADE-L  $\rightarrow$  outputs  $\rightarrow$  setup [give name then go to calculator  $\rightarrow$  open  $\rightarrow$  clear buffer & stack  $\rightarrow$  wave  $\rightarrow$  (in the plot select the wave (say risetime))  $\rightarrow$  In function panel  $\rightarrow$  special funct<sup>ns</sup>  $\rightarrow$  risetime [finalvalue=1,  $\rightarrow$  OK]  $\rightarrow$  send buffer expression to ADE-L

In ADE-L we'll get the value as 17.82n

For 500fF & min. size of MOS  $\rightarrow$  17.82n

1pF "  $\rightarrow$  35n

$\Rightarrow$  more cap  $\Rightarrow$  more risetime

To get parametric analysis of risetime with temperature-

Parametric analysis  $\rightarrow$  variable(temp) E-40 to 120  
 $\Rightarrow$  k<sub>lith</sub>  $\uparrow$  in temp, risetime  $\uparrow$  ses

For fall time →

→ initial value = 1.8 & final value = 0

Fall time for  $C_{out} = 500p$  & min. size = 5.48ns

Fall time ( $t_f$ ) < Rise time ( $t_r$ ) because fall time is concerned with NMOS and here NMOS is stronger ( $\beta_n > \beta_p$ ) so falltime < Risetime.

- If I make PMOS leak  $t_f$  also changes since  $C_{out} = C_L + C_F$  & on changing dimensions of PMOS,  $C_F$  changes  $\Rightarrow C_{out}$  also changes  $\Rightarrow t_f$  also changes.  
→ make total width of PMOS as 1.16u.

(i) When PMOS is changed keeping NMOS constant -

$$t_r = 3.7n \quad [\text{total width of PMOS} = 1.16u]$$

$$t_f = 5.4n$$

(ii) When total width of PMOS = 800n & NMOS const. -

$$t_r = 5.471n$$

$$t_f = 5.491n$$

Total width of PMOS after  $t_r$  &  $t_f$  remain same

$$810 \quad 1.16u \quad 5.348n \quad 5.491n$$

$$(790 \mu V) \quad 5.535n$$

$$820n \quad 1.16u \quad 5.409n \quad 5.491n$$

~~know~~ ~~time~~ ~~rise time~~ ~~load cap. ( $C_L$ )~~  
 pressing & ~~fall~~ ~~intermediate~~ ~~time~~

$$t_{pd} = t_{pLH} + t_{pHL}$$

$$\text{slope} = \alpha_p = 2 \cdot \alpha R_p \quad (2)$$

$$t_r = 2 \cdot 2 T_p$$

$$\text{slope} = \alpha_n = 2 \cdot 2 R_n = 2 \cdot 2 R_p C_{out}$$

$$\frac{t_{ro}}{t_{fo}} > \alpha_p > \alpha_n$$

$$t_r = 2 \cdot 2 R_p [C_{FET} + C_L]$$

initial transient (if)  $t_{ro} > t_{fo}$   $\Rightarrow t_r = 2 \cdot 2 R_p [C_{FET}]$

$$t_r = 2 \cdot 2 R_p \underbrace{[C_{FET} + 2 \cdot 2 R_p C_L]}_{C_{in}}$$

$$\boxed{\text{slope} = 2 \cdot 2 R_p} = \alpha_p \text{ and } 2 \cdot 2 R_p C_{FET} = t_{ro}$$

$$\boxed{t_r = t_{ro} + \alpha_p C_L}$$

For Fall time -

$$\text{from } \text{equation } t_f = t_{fo} + \alpha_n C_L \text{ to obtain fall time}$$

For minimum size inv (ie width of  $P\&N$  MOS = 240 nm)  
 ie PMOS is weak ie  $B_p < B_n \Rightarrow R_p > R_n$

$$R_p = \frac{1}{B_p} \quad \text{and} \quad R_n = \frac{1}{B_n}$$

$$B_p (V_{DD} - V_{tp}) \quad B_n (V_{DD} - V_{tn})$$

$$\Rightarrow R_p > R_n \therefore t_r \text{ will be more.}$$

$$\Rightarrow t_r > t_f \text{ ie } t_{ro} > t_{fo}$$

$$\text{since } R_p > R_n ; \alpha_p > \alpha_n$$

~~Q~~

Q) For the previous example, taking  $C_{FET} = 150\text{fF}$ .

$$t_{ro} = t_{ro} + 2 \cdot 2 R_p C_L$$

$$t_{ro} = 2 \cdot 2 R_p C_{FET}$$

$$= (2 \cdot 2) (0.823\text{k}) (150\text{f})$$

$$= 271.59\text{fF} \times 10^3$$

$$= 271.59\text{pF} = 0.27159\text{ns}$$

$$t_{fo} = 2 \cdot 2 R_n C_{FET}$$

$$= (2 \cdot 2) (0.427\text{k}) (150\text{f})$$

$$= 140.91\text{pF} = 0.14091\text{ns}$$

$$t_r = (0.217) + (2 \cdot 2 \times (0.823\text{k}) \times 150\text{fF})$$

$$= 0.217 + 271.59 + (2 \cdot 2 \times 0.823 \times 150)$$

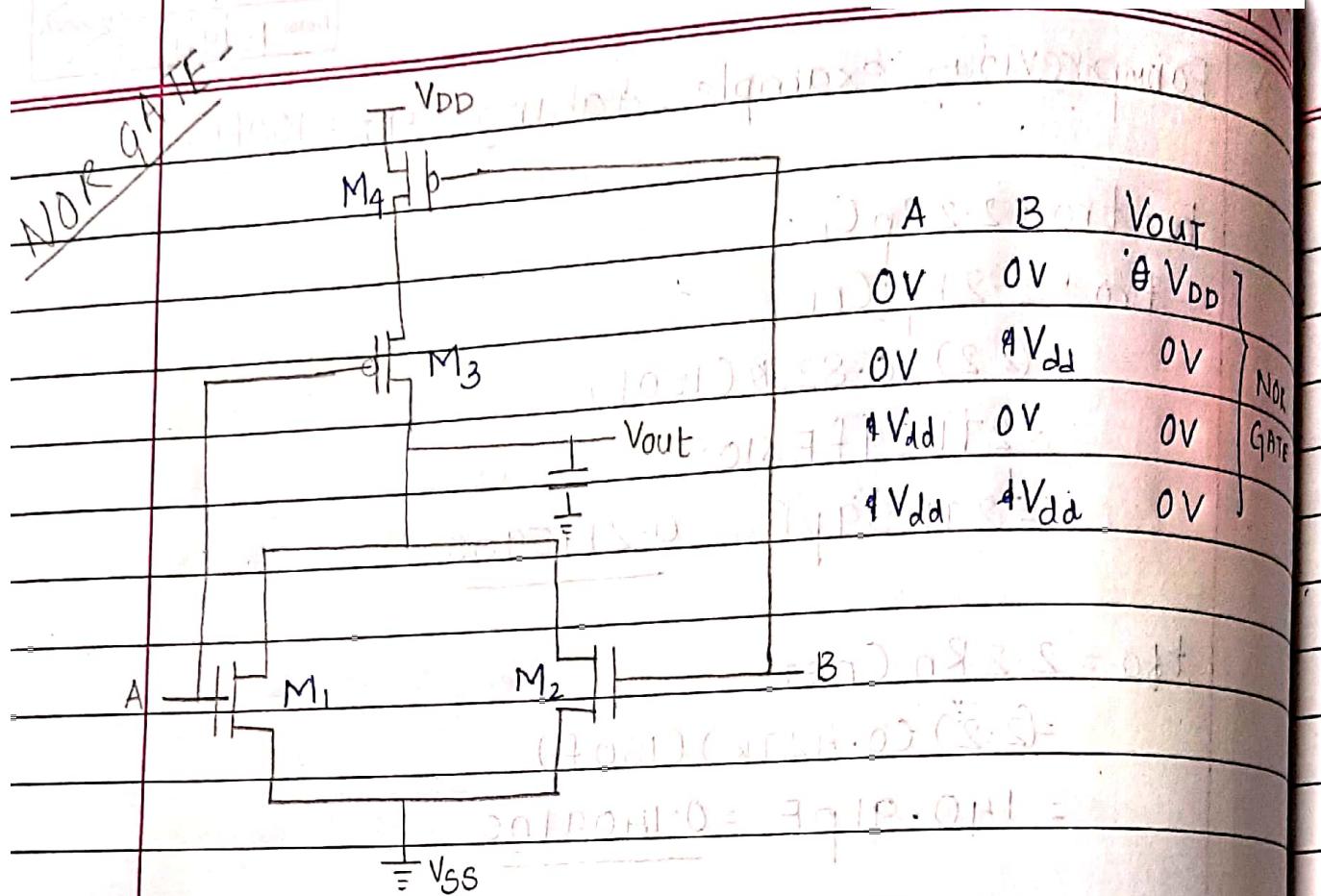
$$= 543.18\text{pF}$$

$$| t_r = 0.54318\text{ns}.$$

$$t_f = 140.91 + (2 \cdot 2 \times 0.427 \times 150)$$

$$t_f = 281.82\text{pF}$$

initial current ... 770 at 7.87V bias via 10k resistor



Case 1:  $A = 0V \& B = 0V \Rightarrow (0 \cdot 0) + (0 \cdot 0) = 0V$

$M_1 \& M_2$  OFF and  $M_3 \& M_4$  ON  $\therefore$  there is a path for capacitor to charge  $\therefore V_{out} = V_{DD}$

Case 2:  $A = 0V \& B = V_{DD}$

$M_1 \& M_4$  OFF and  $M_2 \& M_3$  ON  $\therefore$  there is a path for capacitor to discharge  $\therefore V_{out} = 0V$

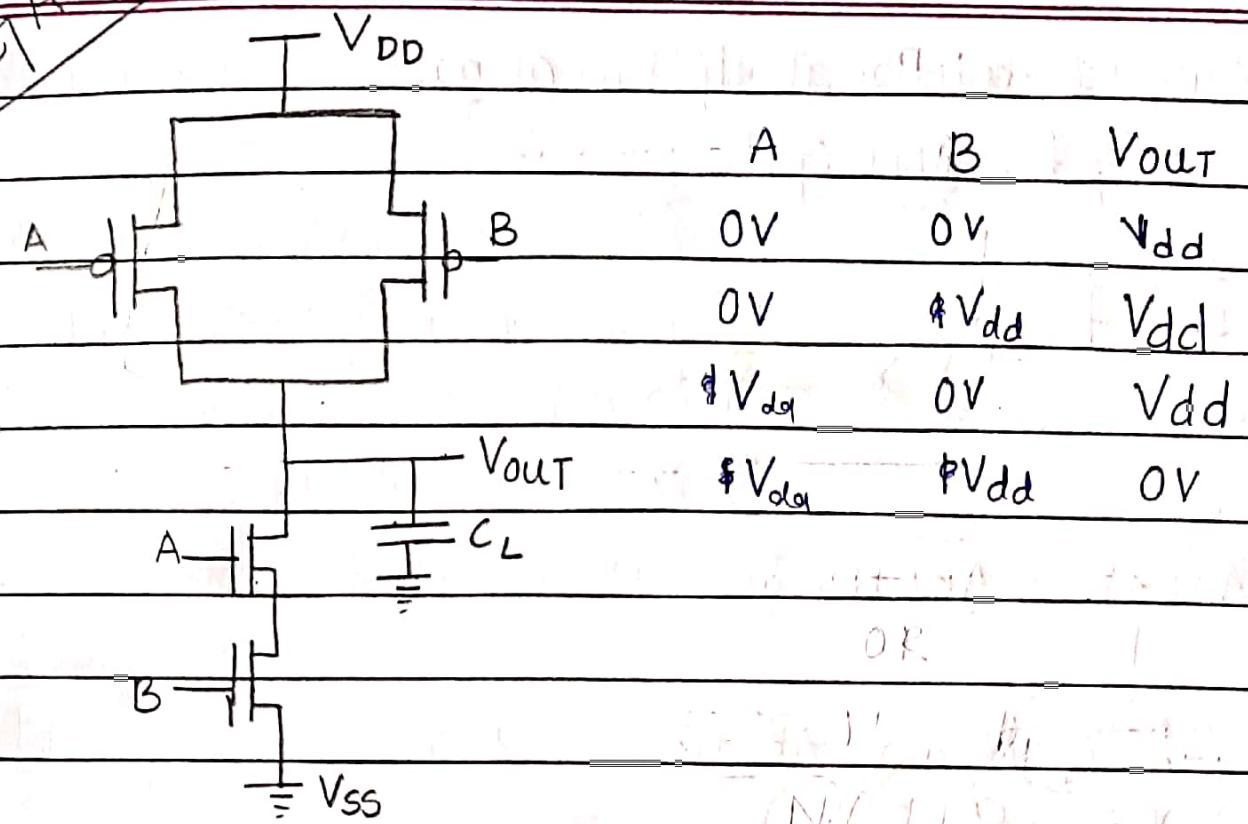
Case 3:  $A = V_{DD} \& B = 0V$

$M_1 \& M_4$  ON and  $M_2 \& M_3$  OFF  $\therefore$  there is a path for capacitor to discharge  $\therefore V_{out} = 0V$

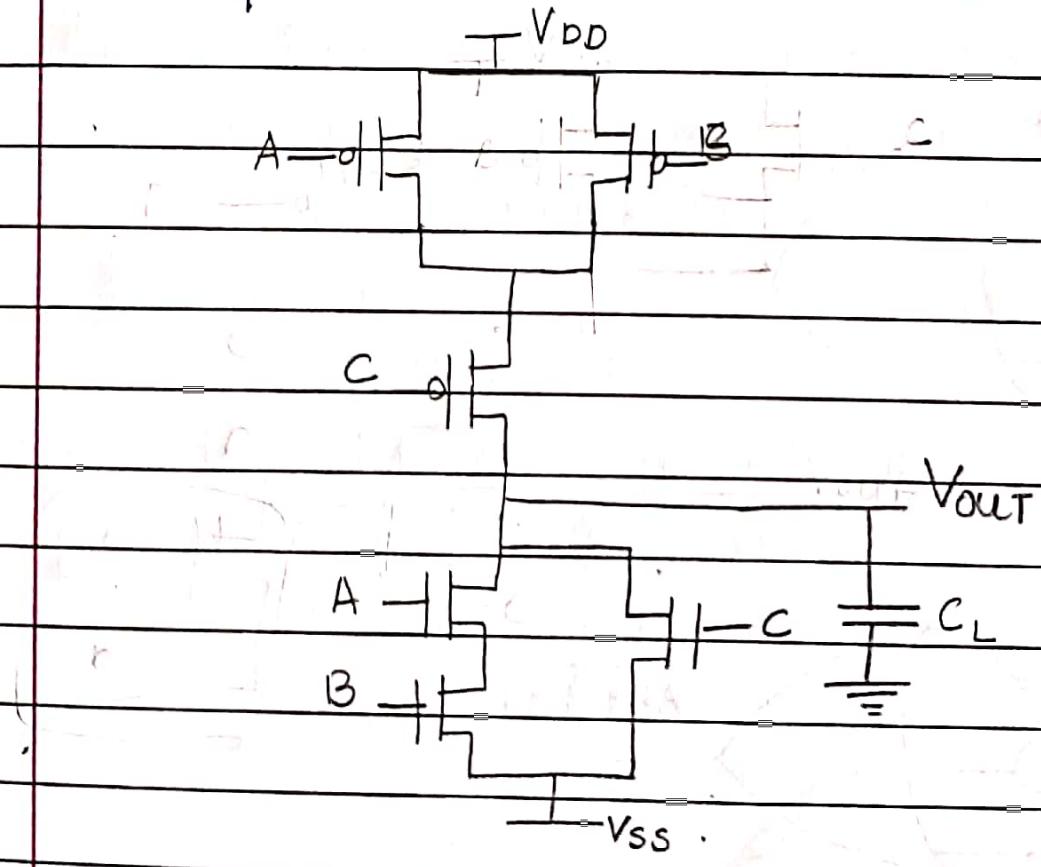
Case 4:

$M_1 \& M_2$  ON and  $M_3 \& M_4$  OFF  $\therefore$  there's a path for capacitor to discharge  $\therefore V_{out} = 0V$

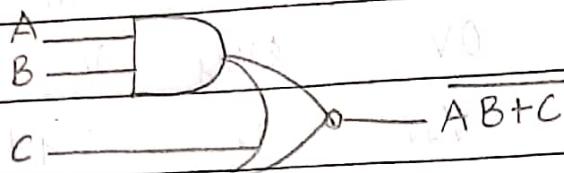
~~UPDATE~~  
NAND



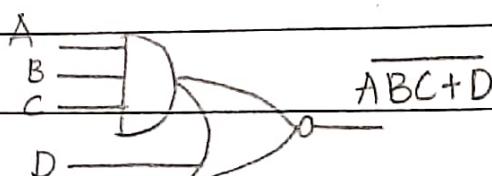
AOI Gates - AB+C



- AOI 22 - additional 1/p for OR gate  
2 1/p for AND Gate

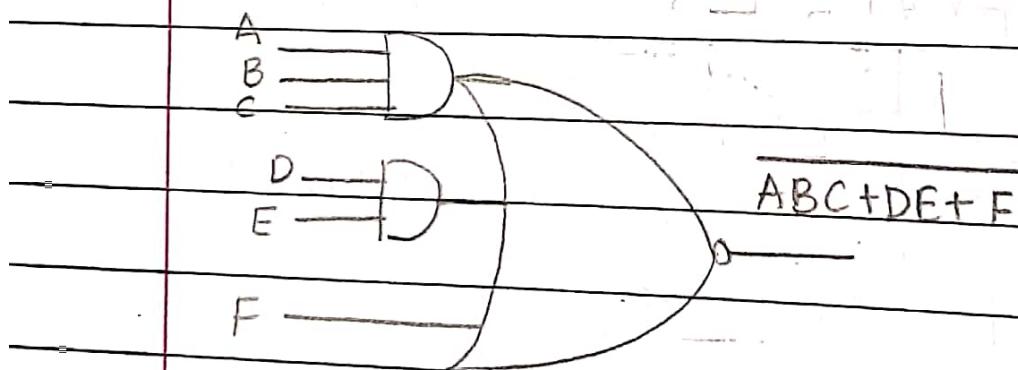


- AOI 31 —  $\overline{ABC+D}$

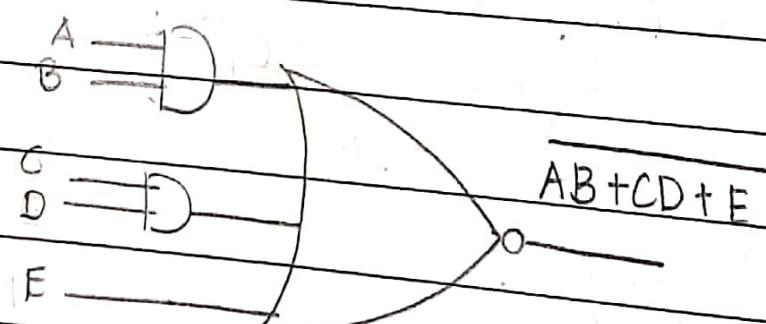


- first And gate  
2nd AND gate

AOI 321 — OR

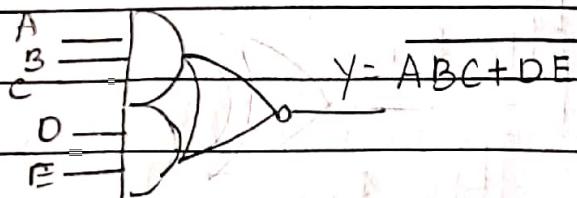


AOI 221

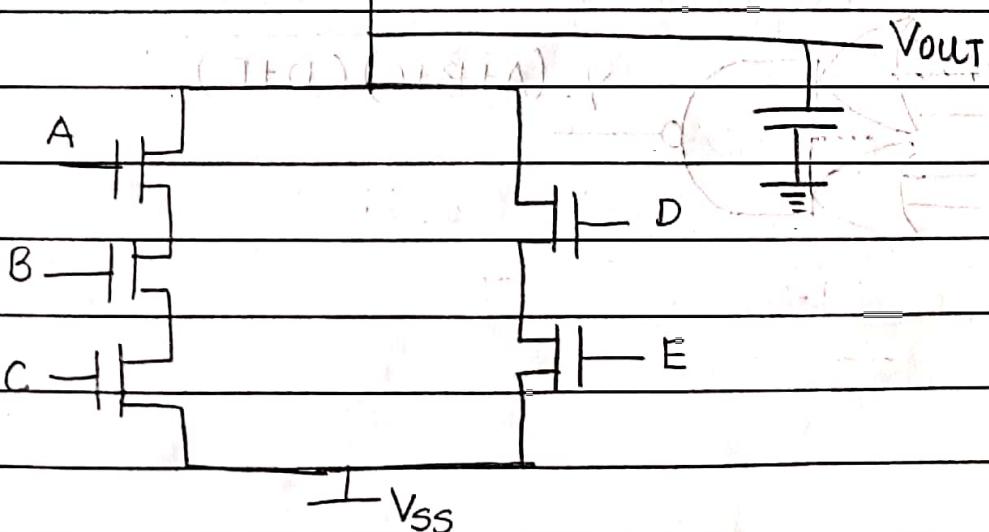
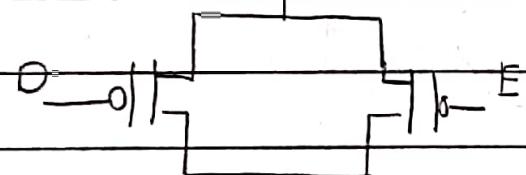
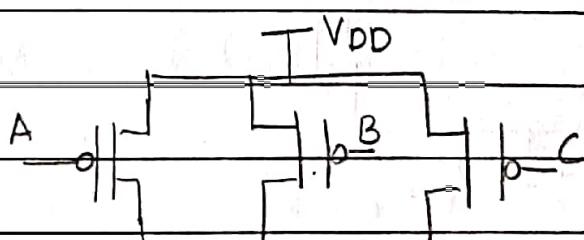
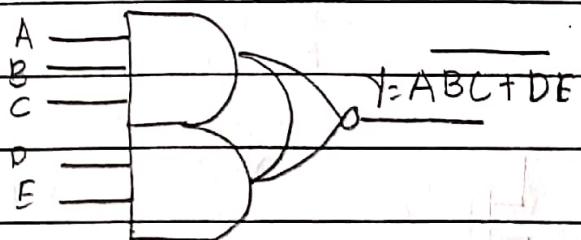


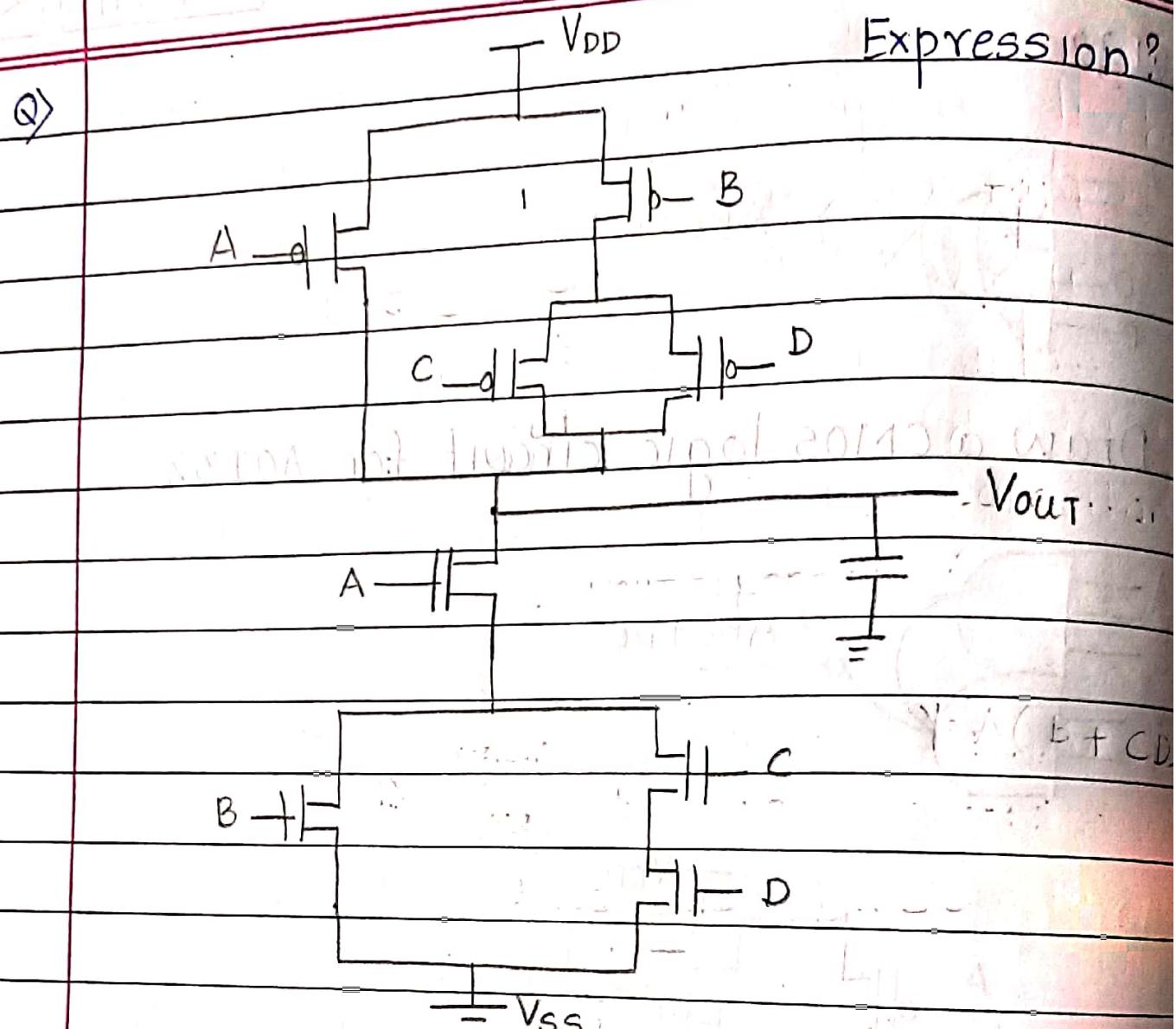
If last number is not 1

AOI29



Draw a CMOS logic circuit for AOI32

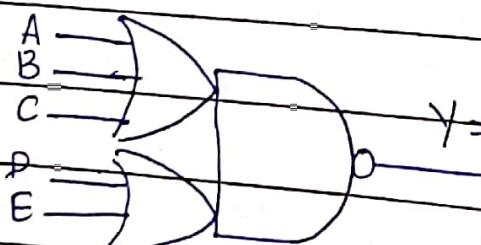




$$Y = \overline{A} \overline{[B+CD]}$$

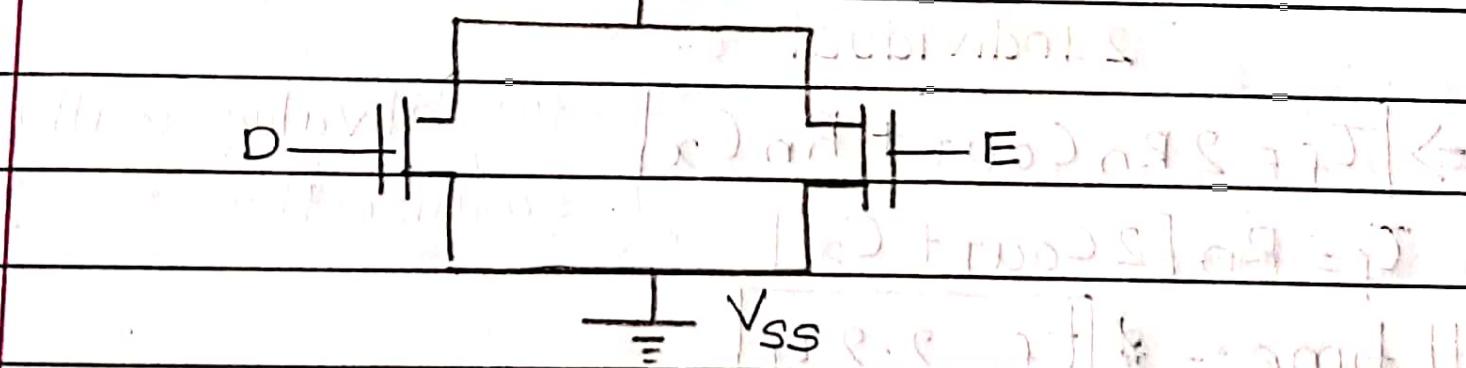
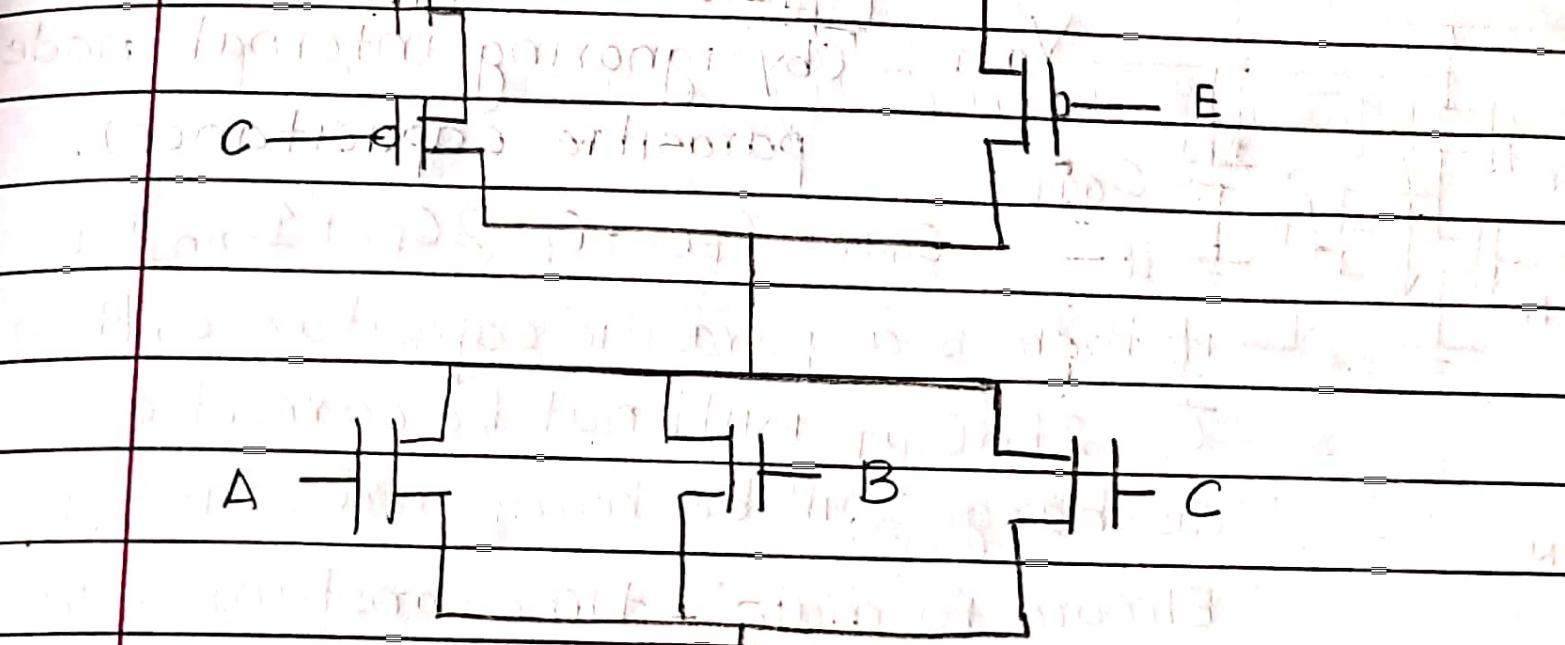
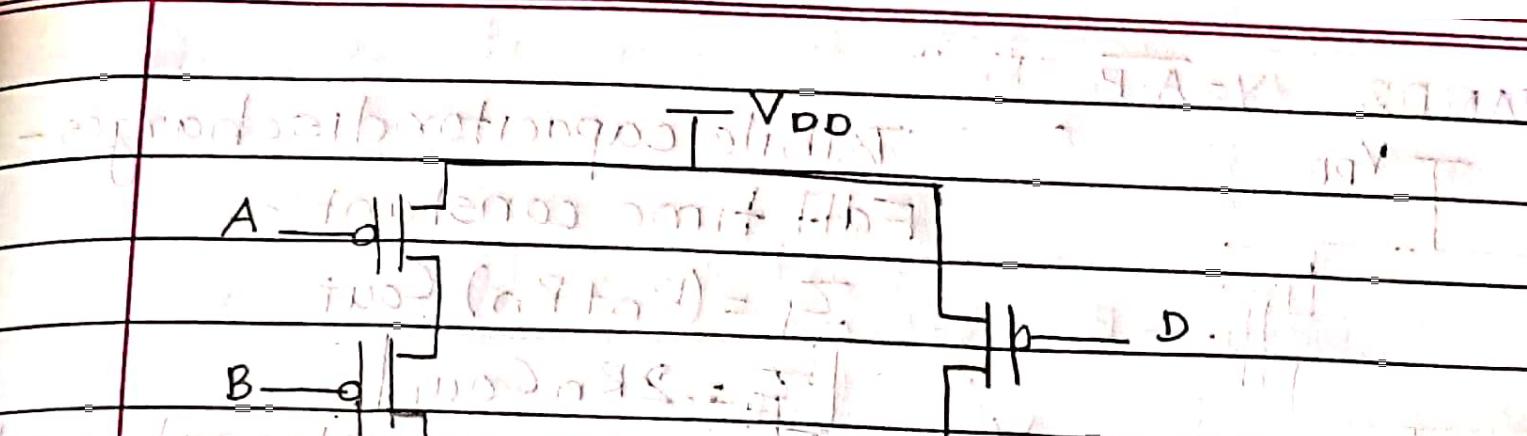
★

OAI32



$$Y = \overline{(A+B+C)(D+E)}$$

QUESTION

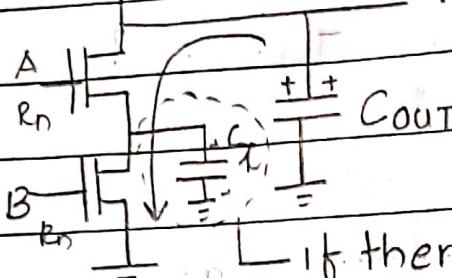


(so  $f_1 = f_2 = f_3 = \frac{1}{2} \cdot \frac{V_{DD}}{R_L + R_s}$ )

P.T.O



NAND2  $y = \overline{A \cdot B}$



While capacitor discharges.

Fall time constant:-

$$\tau_f = (R_n + R_n) C_{out}$$

$$\tau_f = 2 R_n C_{out}$$

by ignoring internal node parasitic capacitance).

$$C_{out} = C_{FET} + C_L = (2C_{DPT} + 1C_{bn})C_L$$

If there is a parasitic capacitance, then

$\tau_f = 2 R_n C_{out}$  will not be correct as

discharge will be hampered. ∵ we use

"Elmore formula" - time constant = sum of

2 individual  $\tau$ .

$$\Rightarrow \tau_f = 2 R_n C_{out} + R_n C_x \quad \left\{ \text{typical values will be smaller than this} \right\}$$

$$\tau_f = R_n [2 C_{out} + C_x]$$

Fall time :-  $t_f = 2 \cdot 2 \tau_f$

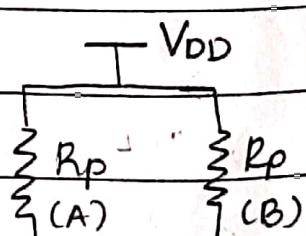
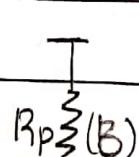
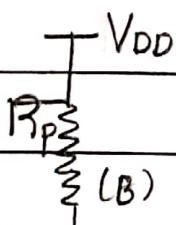
While capacitor charges — (ie risetime)

path :-  $V_{DD} - A^{on} - C_{out}$

$V_{DD} - B^{on} - C_{out}$

$V_{DD} - \text{both } A \& B^{on} - C_{out}$  [best case since  $R = R_p/2$ ]

i.e. -



(best case) =  $\frac{1}{2} \tau_2$

Scapacitance - at internal nodes

Int nodes - all nodes except  
 $V_{DD}, V_{SS}, C_{OUT}$

$C_{OUT}$

$2C_D$

$$Y = A + B$$

-  $V_{DD}$

$$\rightarrow C_{OUT} = (2C_{DOP} + C_{DP}) + C_L$$

$$\rightarrow C_L = 2C_{DOP}$$

A ——————

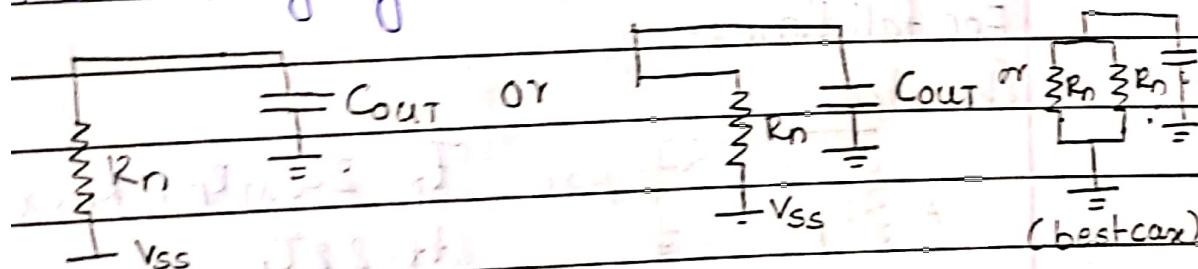
B ——————

A ——————

$\frac{1}{V_{SS}}$

$C_{OUT}$

idle discharging :- (fall time)



$$T_f = R_n C_{OUT}$$

$$T_f = 2 \cdot 2 T_f$$

While charging :-

$$\sum R_p \parallel V_{DD} = \tau_r = (R_p + R_p) C_{OUT} = 2 R_p C_{OUT}$$

$$\sum R_p \parallel t_r = 2 \cdot 2 (\tau_r)$$

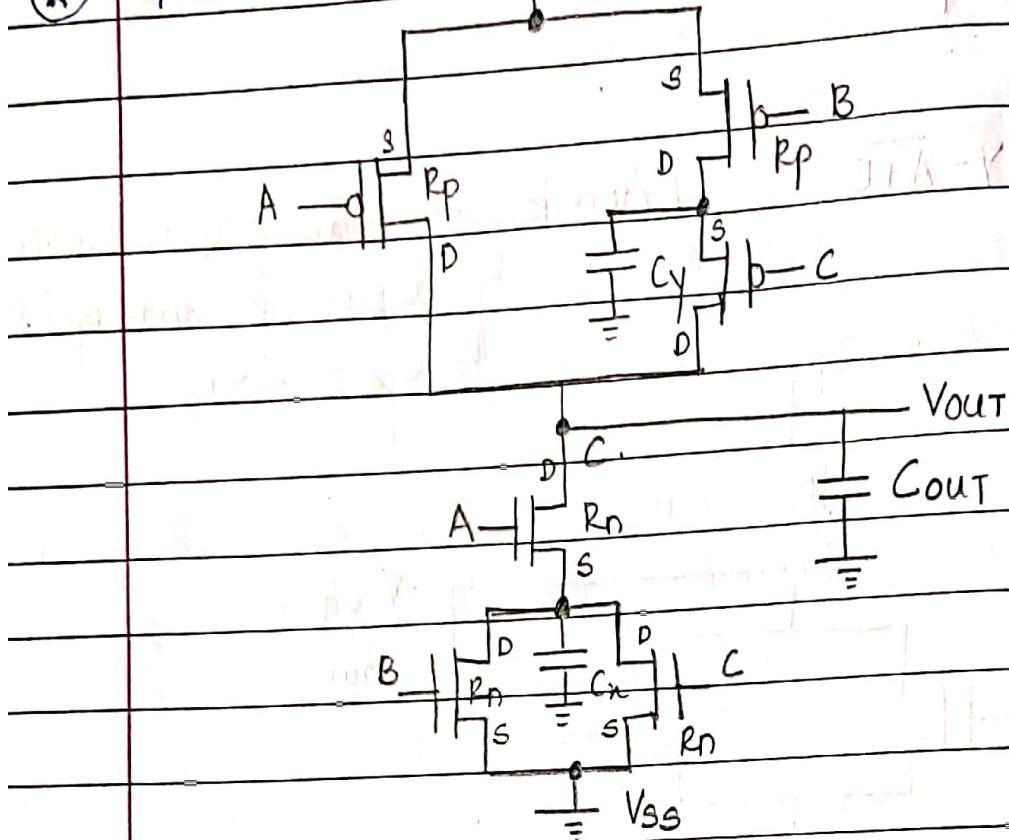
Using Elmore formula -

$$\tau_r = 2 R_p C_{OUT} + R_p C_{OUT}$$

$$t_r = (2 \cdot 2) (\tau_r)$$



$$Y = \overline{A(B+C)} \quad \text{annotate the capacitance.}$$



$$C_x = 3 C_{DN}$$

$$C_y = 2 C_{DP} \quad (\text{switch time})$$

For fall time:-

(worst case)

$$T_f = 2 C_{OUT} R_n + R_n C_x$$

$$t_f = 2 \cdot 2 T_r$$

For rise time:-

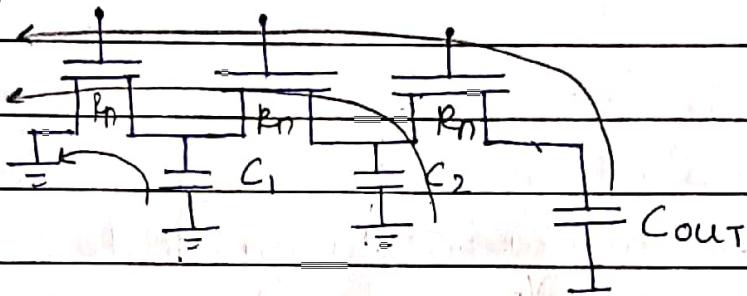
(worst case)

$$T_r = 2 R_p C_{OUT} + R_p C_y$$

$$t_r = 2 \cdot 2 T_r$$

II LP Q) A circuit designer has a choice to implement combinational logic using NAND/NOR nlw, justify select if performance is criterion & analyse speed of 1 to 0 transition as shown below. o/p cap = 130fF, while internal values are,  $C_1 = C_2 = 36fF$ , transistors are identical with  $B = 2.0 \text{ mA/V}^2$ ,  $V_{DD} = 3.3V$  &  $V_{tn} = 0.7V$ .

- Find  $T_f$  for  $C_{out} = 130fF$  using ladder RC nlw.
- " time constant if we ignore  $C_1$  &  $C_2$ . What's % error introduced if we don't include the internal capacitors.



$$R_n = 1$$

$$\beta_n [V_{DD} - V_{tn}]$$

$$= 1 = 192 \Omega = 0.192k\Omega // \\ (2 \times 10^{-3}) (3.3 - 0.7)$$

$$a) T_f = 3R_n C_{out} + 2R_n C_2 + R_n C_1 \\ = (3)(0.192k)(130f) + 2(0.192k)(36f) + (0.192k)(36f)$$

$$T_f = 95.76 \text{ ps.}$$

$$b) T'_f = 3R_n C_{out}$$

$$= 75 \text{ ps}$$

$$\% \text{ error} = \frac{T_f - T'_f}{T_f} \times 100 = 20.76\%$$

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rise & time constant  
same as inverter.

## Gate design for transient performance - A

[Ignore internal node capacitances]

$$\Rightarrow \text{NAND gate} \quad T_r = R_p C_{out}$$

$$V_{in} \quad T_f = R_n C_{out}$$

$$\text{why } T_f \text{ is not } T_r \text{ when } R_p = R_n \text{ and } C_{out} \text{ is same}$$

For:  $T_r$  for NAND =  $T_r$  for inverter

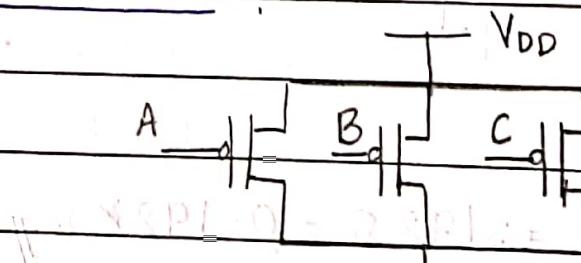
For  $T_f$   $\Rightarrow B_p$  in inverter  $\Rightarrow$  Both PMOS in NAND  $= B_{p4} = B_p$

$$T_r(\text{NAND}) = T_r(\text{INV})$$

$$T_r(\text{NAND}) = 2 T_r(\text{INV}) \Rightarrow 2 R_n = R_{na}$$

$$\Rightarrow B'_n = \frac{2 B_{nu}}{2}$$

For PVAND3:

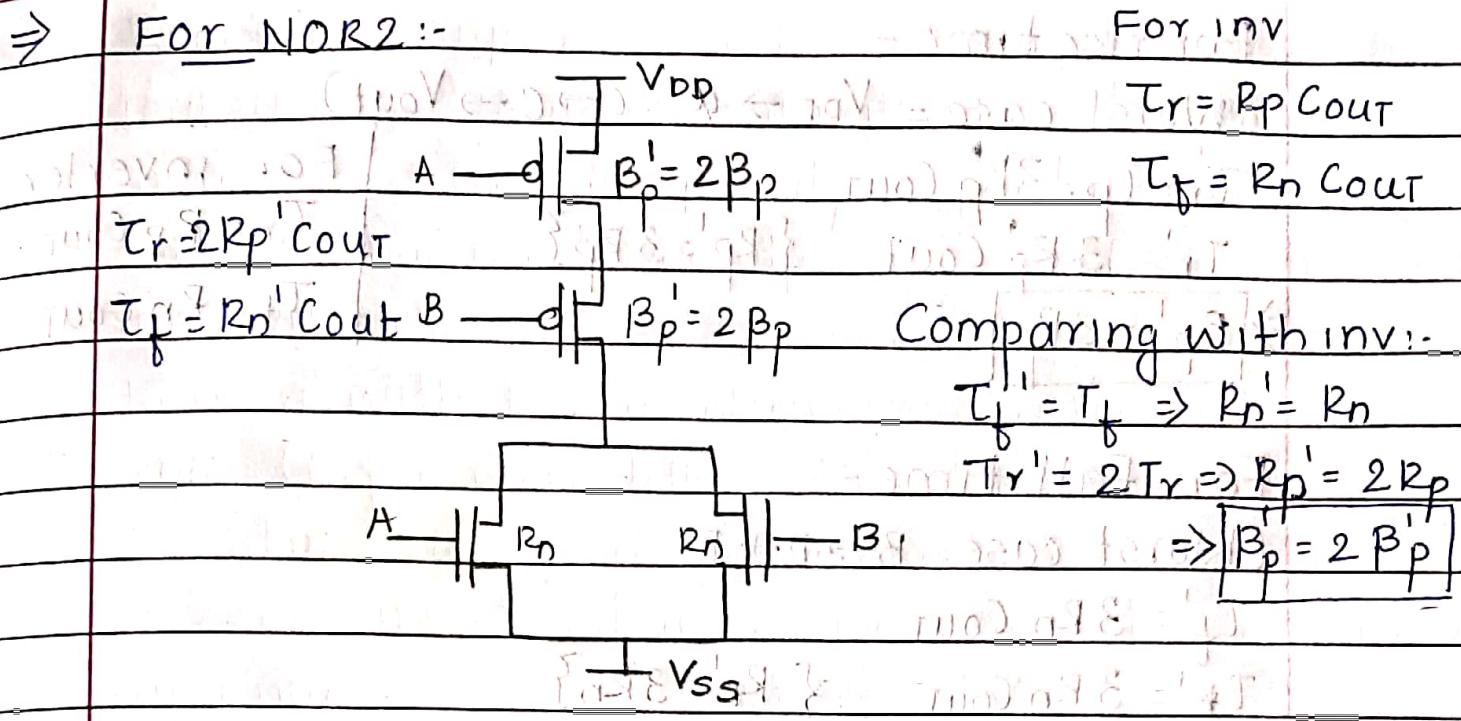


$$[out] = \bar{a} \bar{b} \bar{c}$$

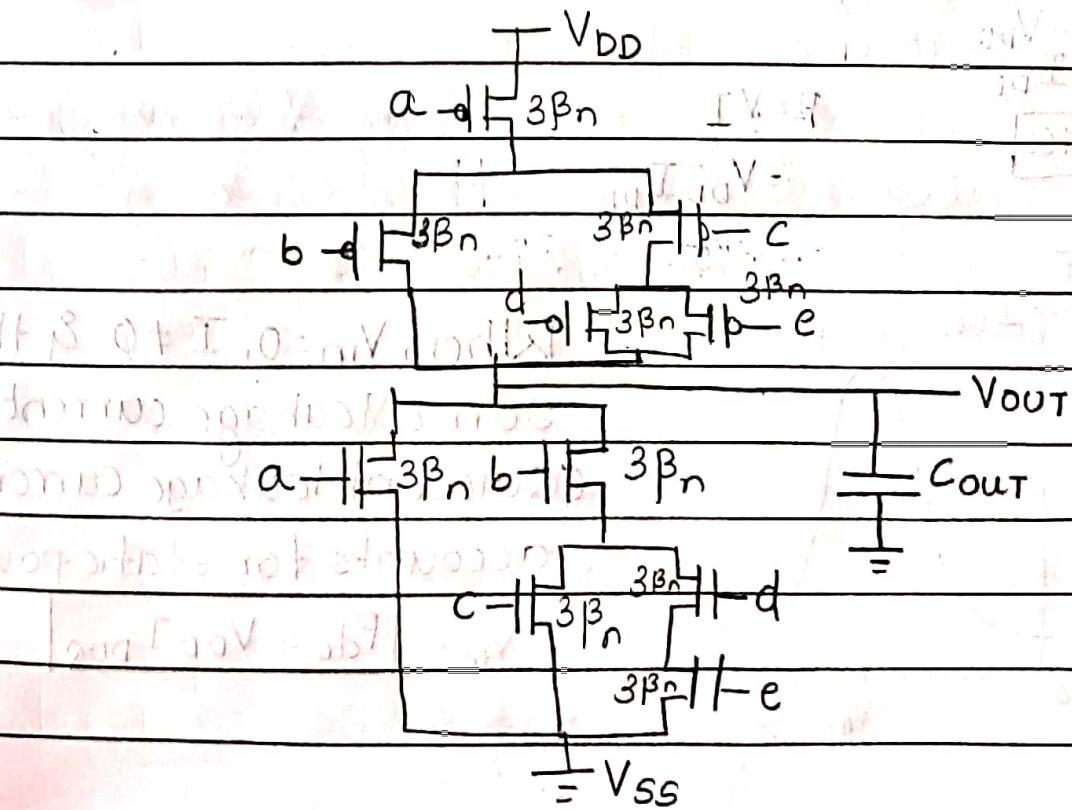
$$R'_n = 3 R_n$$

$$R_n = 3 R_n$$

$$R'_n = 3 R_n$$



Q) Design a combinational circuit using fully CMOS logic for given function  $f = x(y+z)$  implemented as  $f = (a+b(c+de))'$ . Design goal is to achieve same transient performance as that of a ref. CMOS inverter.



For risetime -

(Worst case =  $V_{DD} \rightarrow a \rightarrow c \rightarrow e \rightarrow V_{out}$ )

$$T_r = T_p = 3 R_p C_{out}$$

$$T_r = 3 R_p C_{out} \quad \{ R_p = 3 R_p \}$$

$$\Rightarrow B_p = 3 B_p$$

For inverter,

$$T_r = R_p C_{out}$$

$$T_f = R_n C_{out}$$

For Fall time -

(Worst case =  $B \rightarrow D \rightarrow E$ )

$$T_f = 3 R_n C_{out}$$

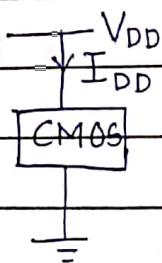
$$T_f = 3 R_n C_{out} \quad \{ R_n = 3 R_n \}$$

$$\Rightarrow B_n = 3 B_D$$

Power dissipation -

- static power dissipation. ( $P_{dc}$ ) - is lost.
- dynamic power dissipation. ( $P_{dynamic}$ )

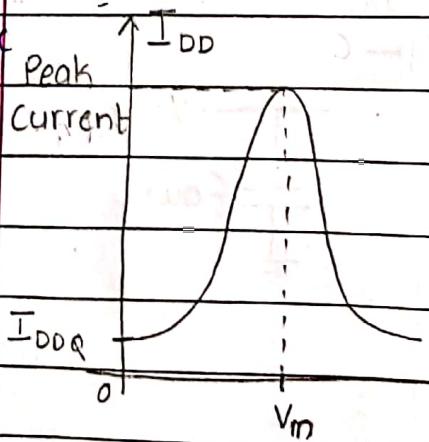
$$P = P_{dc} + P_{dyn}$$



$$P = VI$$

$$= V_{DD} I_{DD}$$

For static power -

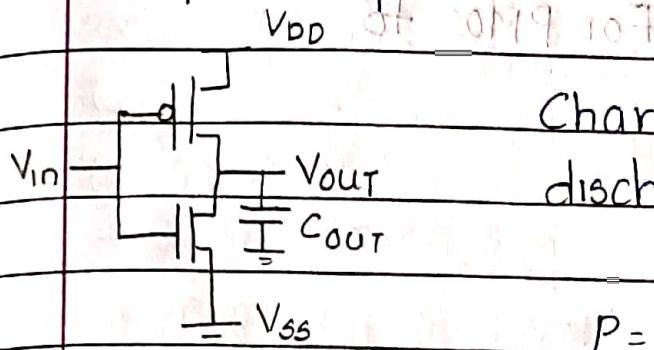


When  $V_{in} = 0$ ,  $I \neq 0$  & there is some leakage current  $I_{DDQ}$  (Quiescent leakage current) which accounts for static power.

$$P_{dc} = V_{DD} I_{DDQ}$$

For dynamic power:-

If  $I_{lp}$  is a square wave with time period  $T$ . [ $f = 1/T$ ]



Charge in capacitor which charging & disch.  $\Rightarrow Q = CV$

$$Q = C_{out} \cdot V_{DD}$$

$$P = V_{DD} I_{DD}$$

$$= V_{DD} Q \frac{1}{T}$$

$$= V_{DD} \cdot C_{out} \cdot V_{DD} \frac{1}{T}$$

$$P_{dyn} = V_{DD}^2 C_{out} f$$

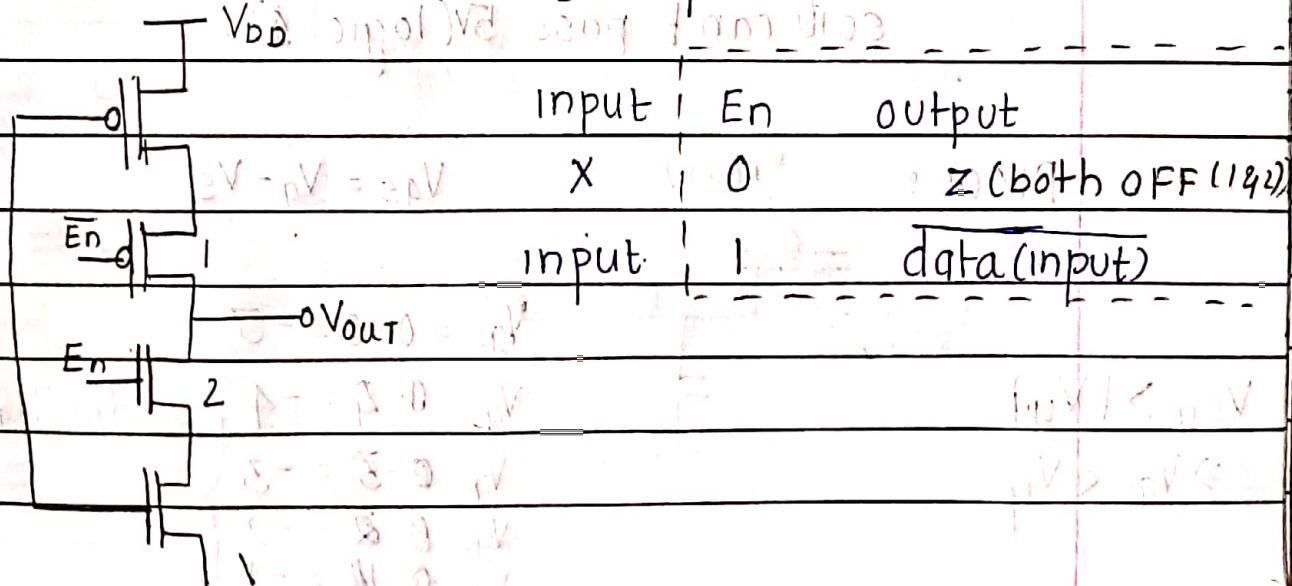
$$\text{Total power} = P = P_{dc} + P_{dyn}$$

$$= V_{DD} I_{DD} Q + V_{DD}^2 C_{out} f$$

$$P \propto f$$

Tristate Inverter - three operations loop

- Three states  $\rightarrow 0, 1, Z$  (high impedance)

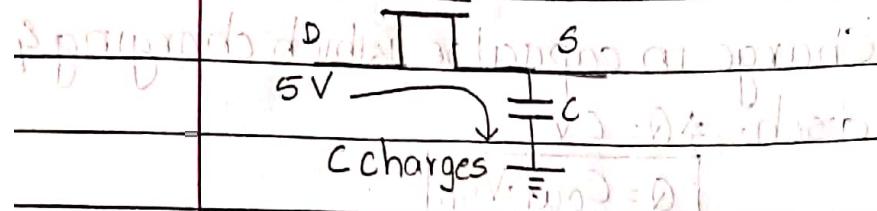


Pass transistor:-

NMOS: having drain after source makes it off

$$V_g = 5V$$

For PMOS to



$$G \& D \text{ voltage} = 5V$$

since  $D \Rightarrow 5V$ , capacitor charges  $\Rightarrow S$  voltage will increase

$$V_{gs} = V_g - V_s = 5 - 0 = 5V$$

$$V_{gs} = V_g - V_s = 5 - 1 = 4V$$

$$V_{gs} = V_g - V_s = 5 - 2 = 3V$$

$$V_{gs} = V_g - V_s = 5 - 3 = 2V \quad \begin{cases} \text{capacitor charges} \\ \text{S voltage increases} \end{cases}$$

$$V_{gs} = V_g - V_s = 5 - 4 = 1V$$

$$V_{gs} = V_g - V_s = 5 - 5 = 0V$$

Transistor OFF

NMOS - Good zero & bad one

Good zero passer since for  $V_s = 0$ , we get  $V_{gs} = 5V$ .  
It can pass 0 value but when  $V_s = 5V$ , NMOS is OFF.  
so it can't pass 5V (logic 1).

PMOS:

$$V_g(0V)$$

$$V_{gs} = V_g - V_s$$



$$V_{gs} = 0 - 5 = -5V$$

$$V_{sg} > V_{tp}$$

$$V_{gs} = 0 - 4 = -4V \quad \begin{cases} S \text{ discharges} \end{cases}$$

$$\Rightarrow V_{gs} < V_{tp}$$

$$V_{gs} = 0 - 3 = -3V$$

$$V_{gs} = 0 - 2 = -2V$$

$$V_{gs} = 0 - 1 = -1V$$

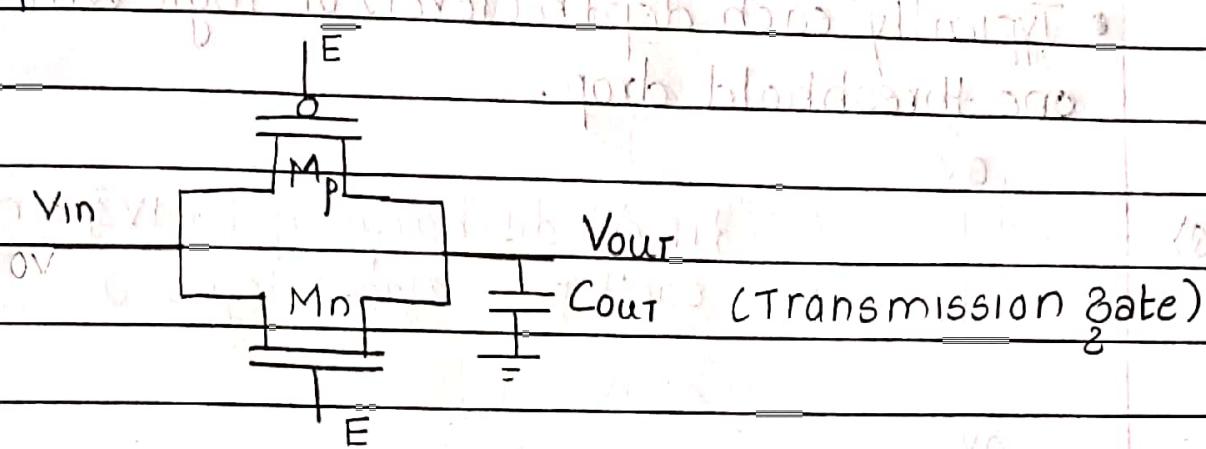
$$V_{GS} = V_0 - (0) \downarrow$$

PMOS OFF

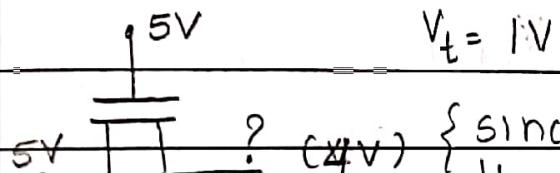
= 0 — PMOS OFF since  $V_{GS} > V_{TP}$

PMOS - Good 1 passer, bad 0 passer.

So since P & N MOS can't yield Good 0 & 1 resp., a transmission gate is formed using both of them in parallel.



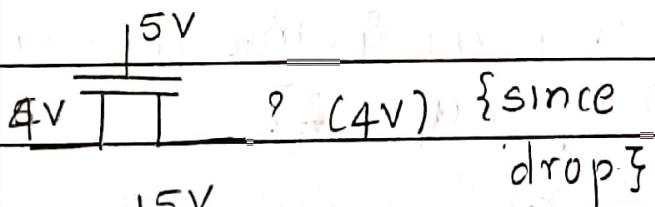
Q)



$$V_t = 1V$$

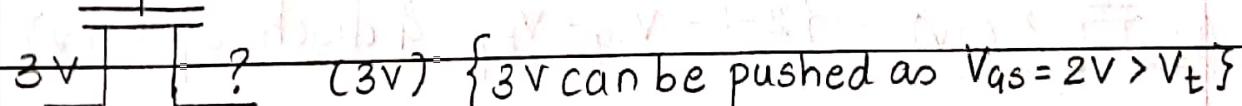
{since not a good 1 passer. ∴ one threshold drop}

Q)



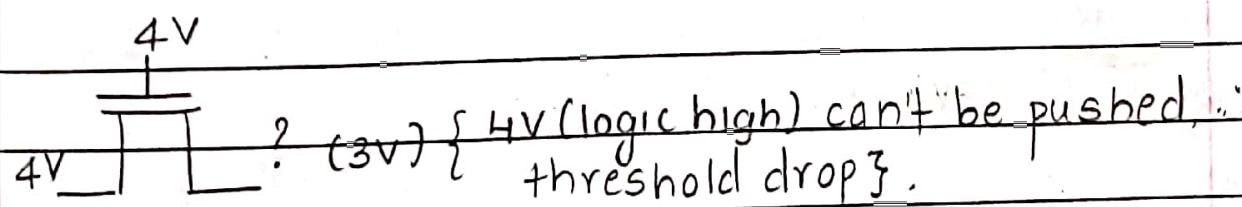
{since it can pass 4V, ∴ no threshold drop}

Q)



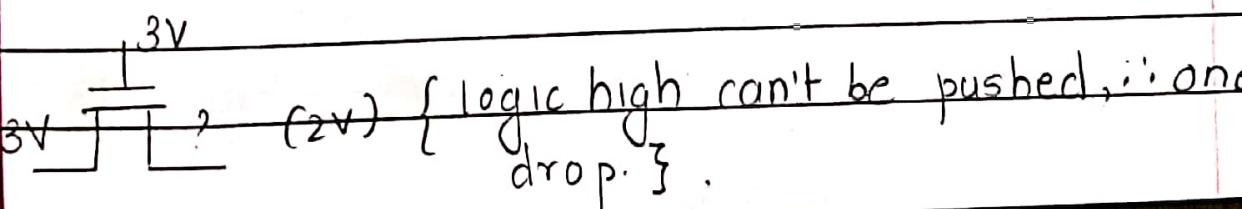
{3V can be pushed as  $V_{GS} = 2V > V_t$ }

Q)

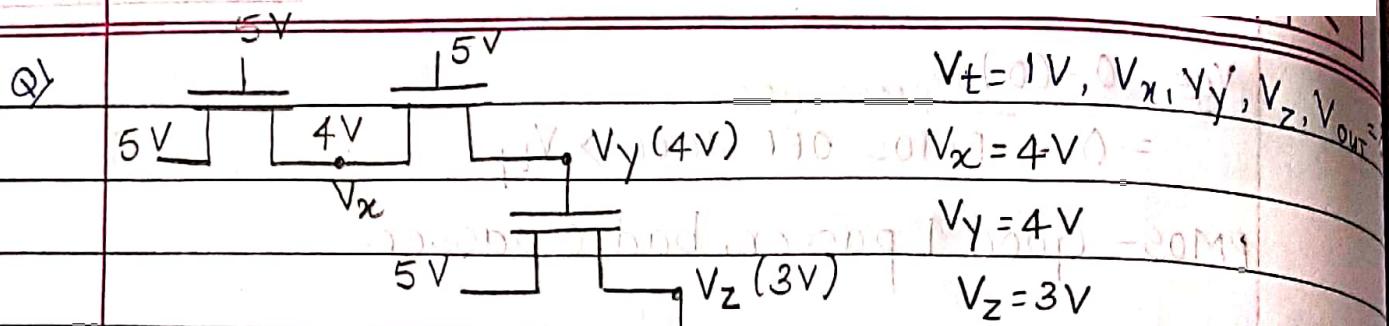


{4V (logic high) can't be pushed, ∴ one threshold drop.}

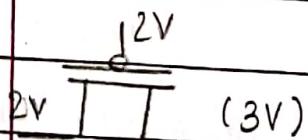
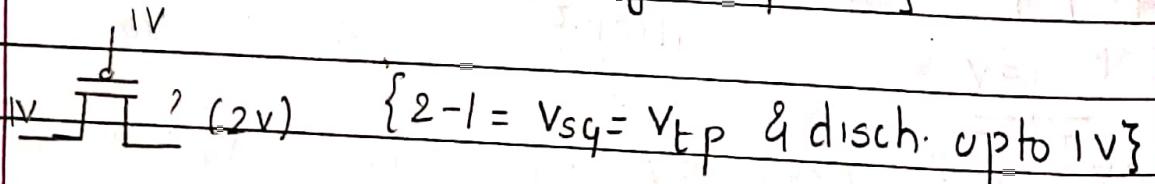
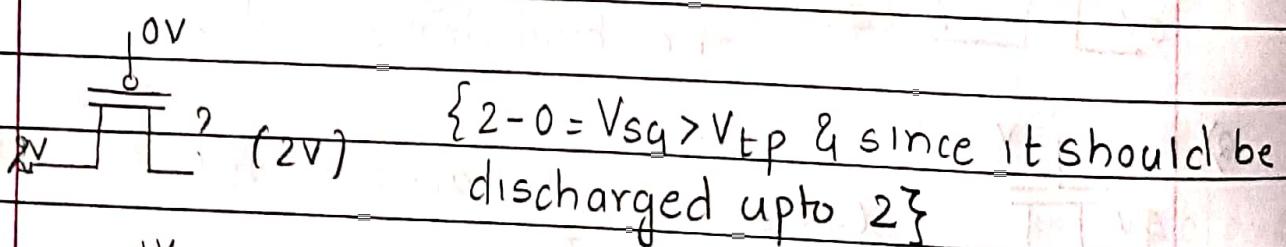
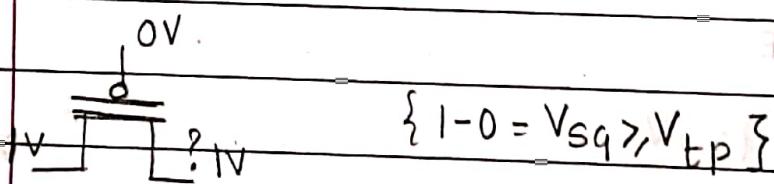
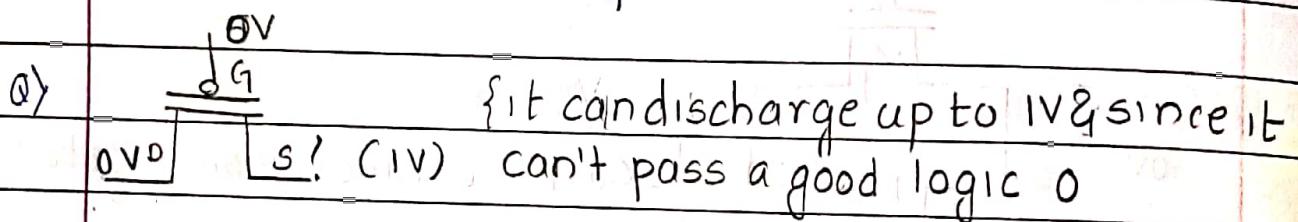
Q)

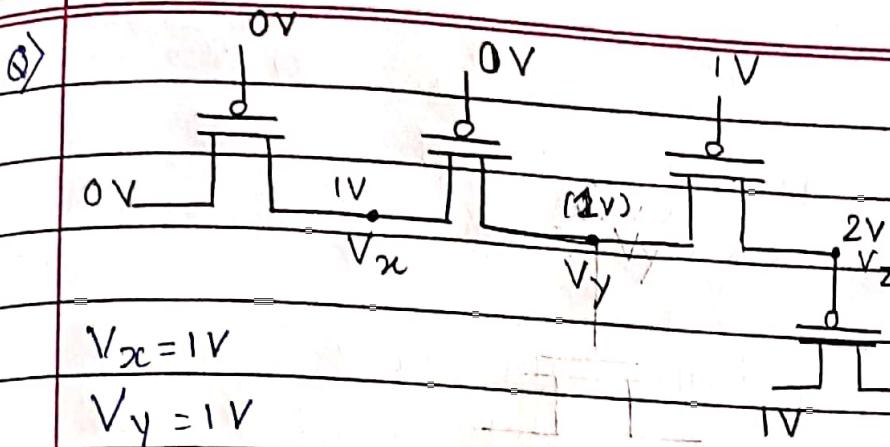


{logic high can't be pushed, ∴ one threshold drop.}



- Typically each depth (level) of logic will lead to one threshold drop.





$$V_x = 1V$$

$$V_y = 1V$$

$$V_z = 2V$$

$$V_{OUT} = 3V$$

Given a choice b/w NAND/NOR which one is better.

- based on speed, area, power → both have same power  
 ↳ for both performance is same as reference inverter.

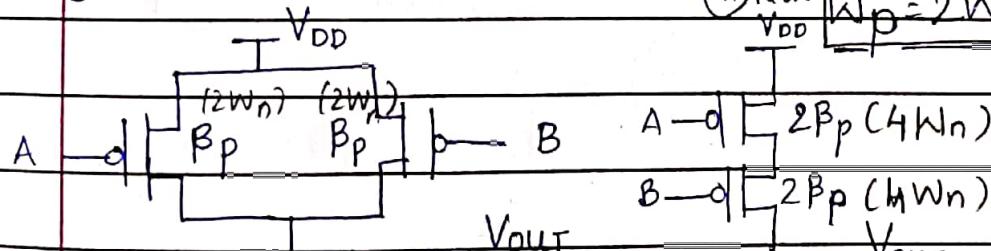
∴ Area is the only parameter to decide.

For a reference inverter:  $B_p = B_n$

$$\Rightarrow W_p = r W_n$$

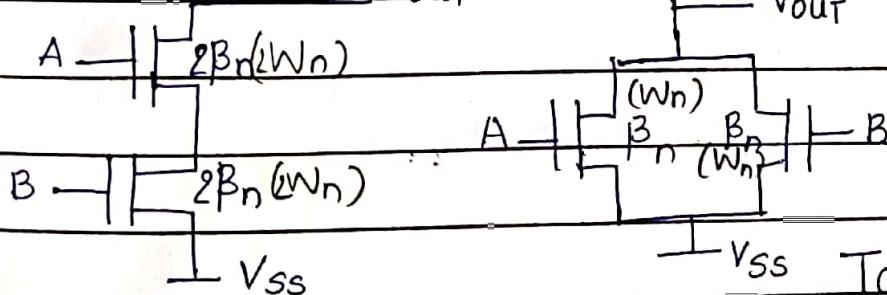
↳ mobility ratio  $(\frac{m_p}{m_n})$

i) NAND



ii) NOR

$W_p = 2W_n$  assuming  $r = 2$ .



Total width =  $8W_n$

$(Width)_{NAND} < (Width)_{NOR}$  ∵ NAND is better.