Computer-Aided VLSI System Design
Innovus Lab (2/3)

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Data Preparation

1. Extract data from the folder **Innovus_Lab**.
2. The extracted directory contains
   - **design_data**
     A. CHIP.v
     B. CHIP.ioc
     C. CHIP.sdc
     D. CHIP_scan.sdc
   - **celtic**
     A. fast.cdB
     B. slow.cdB
   - **tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **gds**
     A. tsmc13gfsg_fram.gds
     B. tpz013g3_v2.0.gds
   - **lef**
     A. tsmc13fsg_8lm_cic.lef
     B. tpz013g3_8lm_cic.lef
     C. RF2SH64x16.vclef
     D. antenna_8.lef
   - **lib**
     A. slow.lib
     B. fast.lib
     C. tpz013g3wc.lib
     D. tpz013g3lt.lib
     E. RF2SH64x16_slow_syn.lib
     F. RF2SH64x16_fast@0C_syn.lib
   - streamOut.map
   - tsmc013.capTbl
   - mmmc.view
   - addIoFiller_tpz.cmd

Introduction

In this lab, you will learn how to use Innovus to run the APR flow, and generate the required data for demonstration.

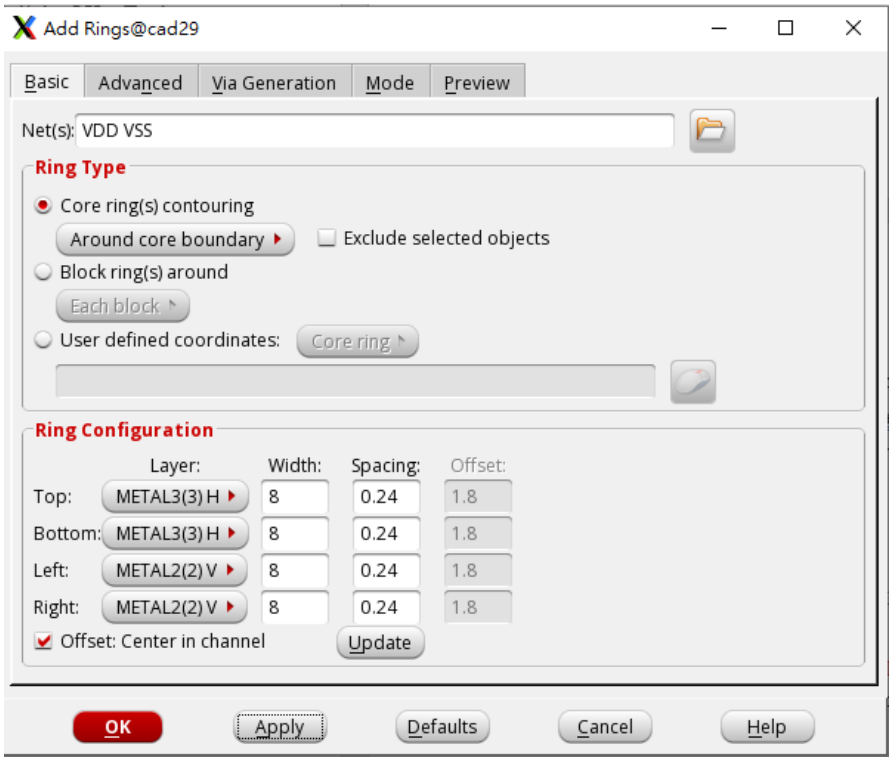
Power Planning

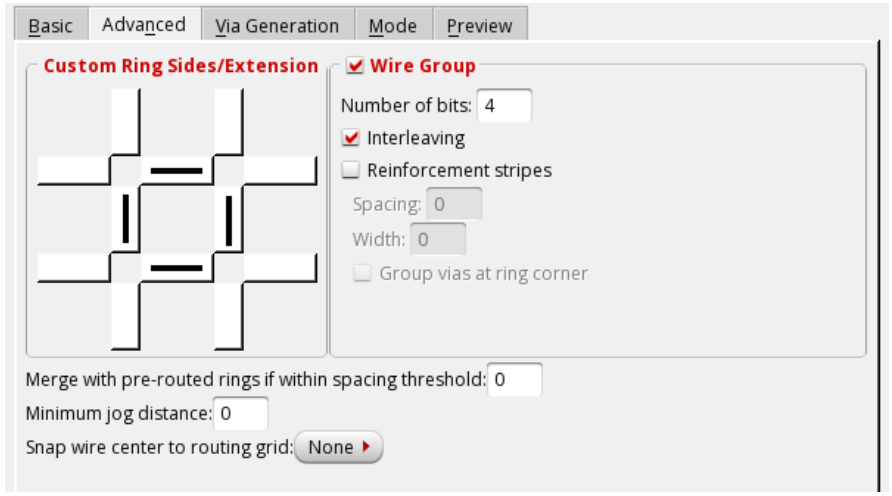
1. Start Innovus:
   1.1 % **innovus** (remember do not use background execution)
   1.2 Fail to open Innovus:
   % **source /usr/cad/innovus/CIC/license.cshrc**
   % **source innovus.cshrc**
   (In this class, source innovus.cshrc from NTU COOL instead)
2. Restore file
   - Open ***File → Restore Design…***
   - Choose ◆ Innovus
3. Restore Design File: **DBS/floorplan**
4. Add Power Rings
   4.1 Open ***Power → Power Planning → Add Ring…***
   4.2 In the Basic tab:
      4.2.1 Fill in Net(s) names: **VDD VSS**
      4.2.2 Specify metal layers and width
      - Top Layer: **METAL3 H** Width: **8**
      - Bottom Layer: **METAL3 H** Width: **8**
      - Left Layer: **METAL2 V** Width: **8**
      - Right Layer: **METAL2 V** Width: **8**

      4.2.3 Click Update button
      4.2.4 Choose ◆ **Offset: Center in channel**
   4.3 In the Advanced tab:
      4.3.1 Configure wire group
      - ◆ Use wire group
      - Number of bits: **4**
      - ◆ Interleaving

   4.4 Apply the specification:
      4.4.1 Click Apply button
      4.4.2 Click Cancel button

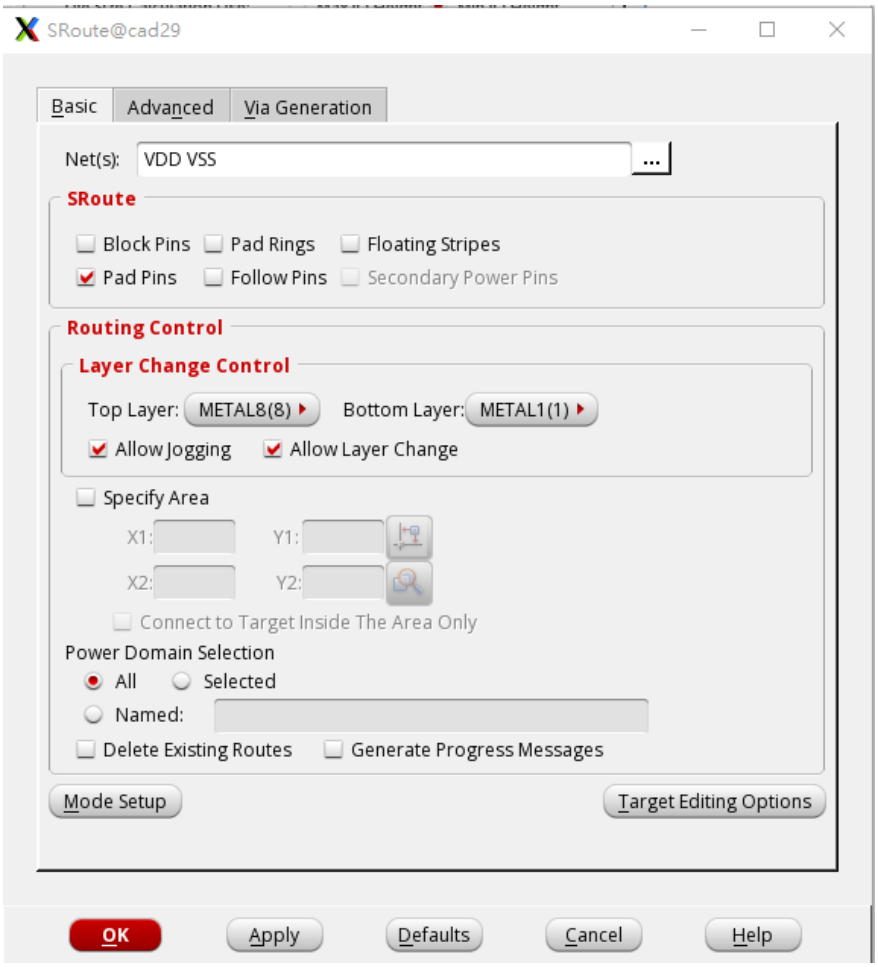
Check if the ring is correctly created. If not, click **undo** button (in Innovus toolbar) and repeat step 1.2~1.4 again.





5. Connect Core Power Pin
   5.1 Open ***Route → Special Route…***
   5.2 Fill in Net(s): **VDD VSS**
   5.3 Set the following configuration
   - ◦ Block pins
   - ◆ Pad pins
   - ◦ Pad rings
   - ◦ Follow pins

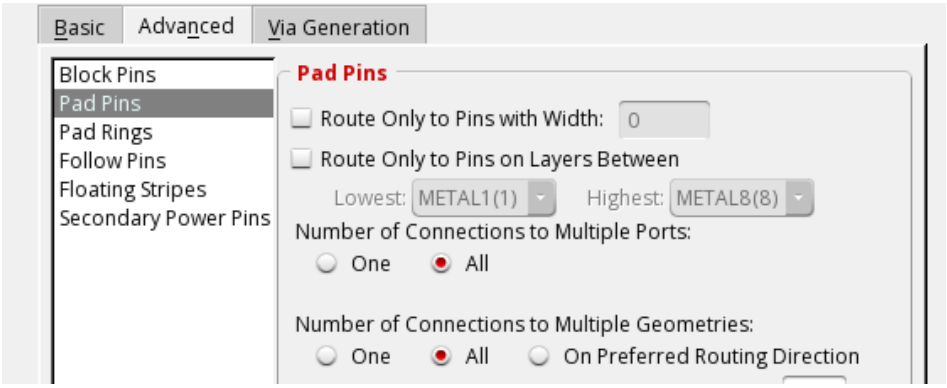
Ignore errors of core power pad here.



5.4 In the Advanced page:

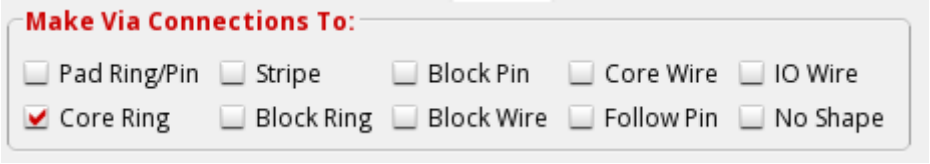
5.4.1 Select **Pad Pins**

5.4.2 Number of Connections to Multiple Geometries: ◆ All



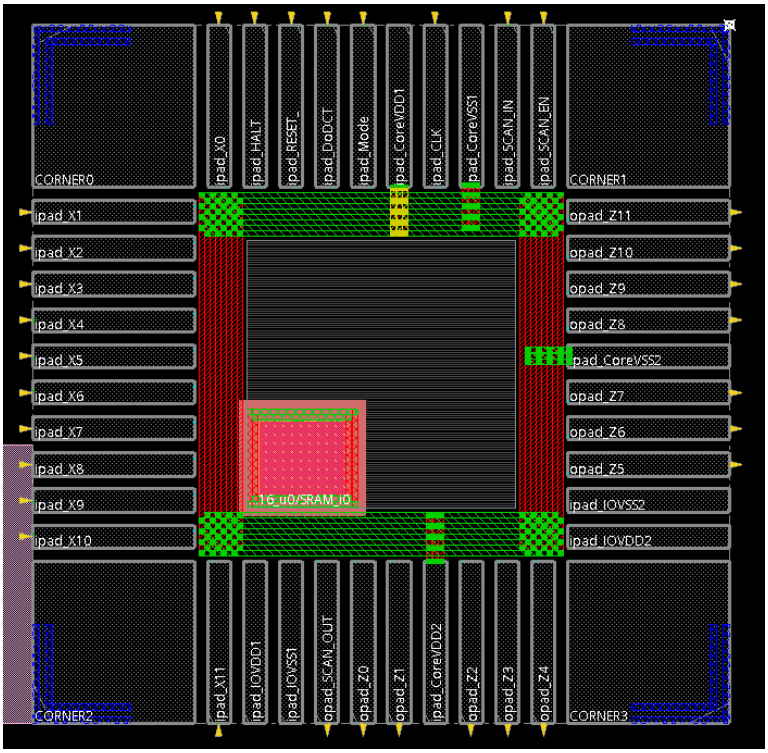
5.5 In the Via Generation page:

➢ Make Via Connections To: ◆ Core Ring



5.6 Click OK button

6. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/powerring**



7. Add Stripes

   7.1 Open ***Power → Power Planning → Add Stripes…***

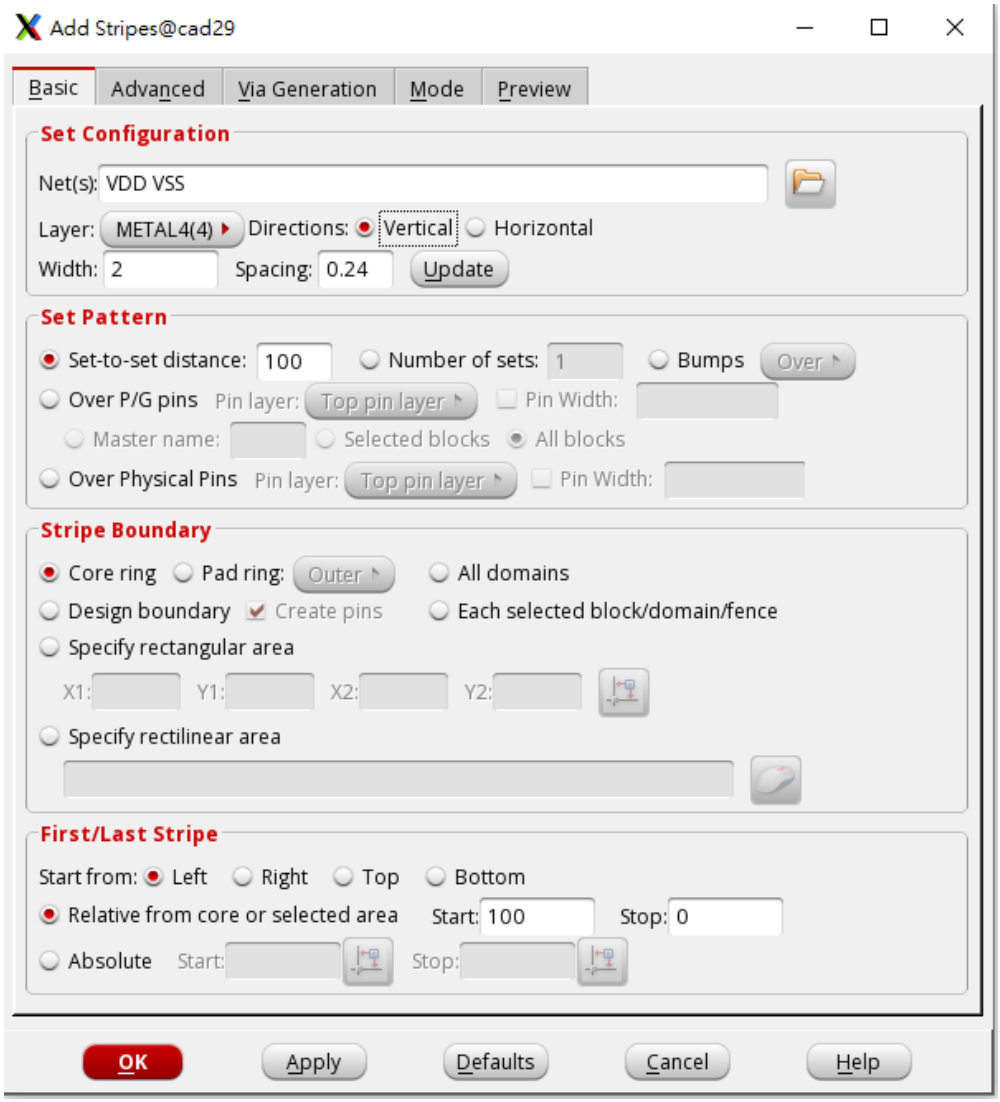
   7.2 Create vertical power stripes:

      7.2.1 Specify metal layer, width, direction and spacing
      - Net(s): **VDD VSS**
      - Layer: **METAL4**
      - Directions: **Vertical**
      - Width: **2**
      - Click Update Button

      7.2.2 Specify set-to-set distance
      - Set-to-set distance: **100**

      7.2.3 Specify locations by Relative from core or selected area
      - Start from: ◆ **Left**
      - Relative from core or selected area Start: **100** Stop: **0**

      7.2.4 Click Apply button



7.3 Create horizontal power stripes:

7.3.1 Specify metal layer, width, direction and spacing

- Net(s): **VDD VSS**
- Layer: **METAL5**
- Directions: **Horizontal**
- Width: **2**
- Click Update Button

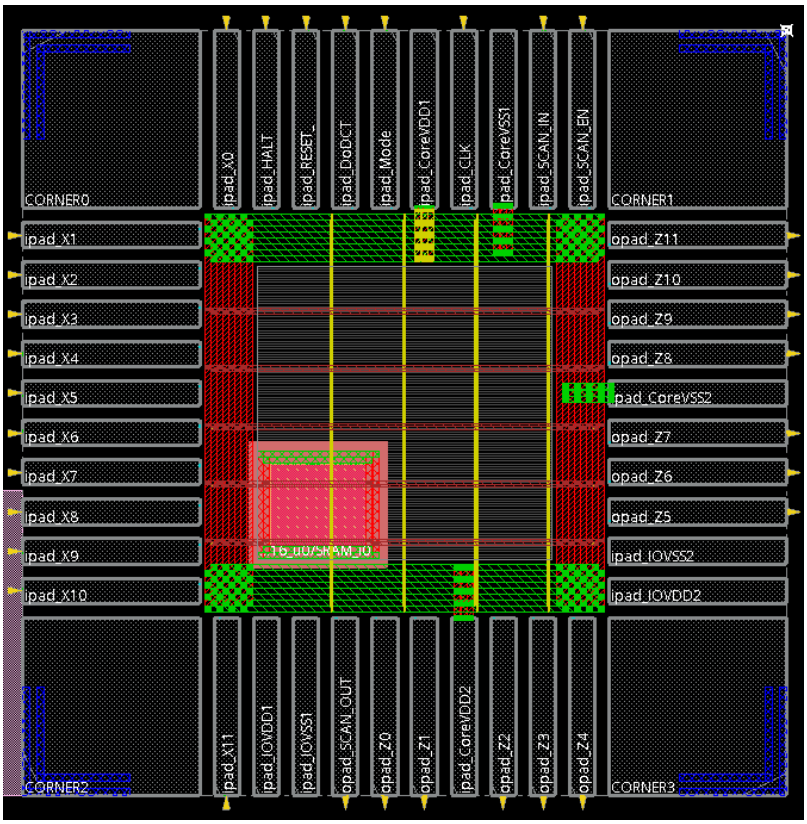
7.3.2 Specify set-to-set distance

- Set-to-set distance: **80**

7.3.3 Specify locations by Relative from core or selected area

- Start from: ◆ **Bottom**
- Relative from core or selected area Start: **20** Stop: **0**

7.3.4 Click Apply button



8. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/powerstripe**
9. Connect Standard Cell Power Line

   9.1 Open ***Route → Special Route…***

   9.2 Fill in Net(s): **VDD VSS**

   9.3 Set the following configuration
   - ◇ Block pins
   - ◇ Pad pins
   - ◇ Pad rings
   - ◆ Follow pins

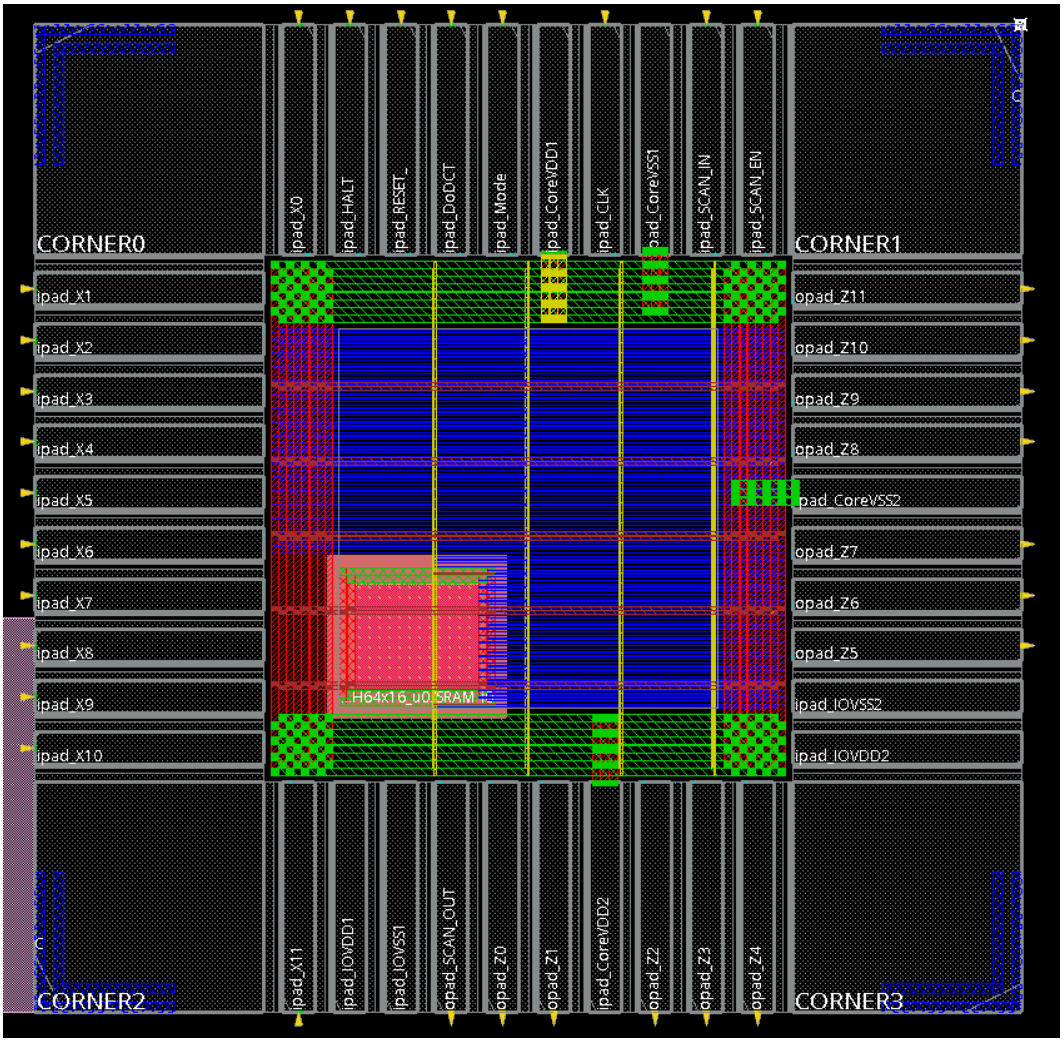
9.4 In the Via Generation page:

- Make Via Connections To: ◆ Core Ring ◆ Stripe ◆ Block Ring

9.5 Click OK button

Add IO Filler

1. innovus # > **source library/addIoFiller_tpz.cmd**



Verify Geometry & Connectivity

1. Verify geometry
   1.1 innovus # > **verify_drc**

```
Verification Complete : 0 Viols.
```

2. Verify connectivity
   2.1 Open ***Verify → Verify Connectivity …***
   2.2 Net Type ◆ **Special Only**
   2.3 Nets ◆ Named: **VDD VSS**
   2.4 Click OK button

```
Begin Summary
  Found no problems or warnings.
End Summary
```

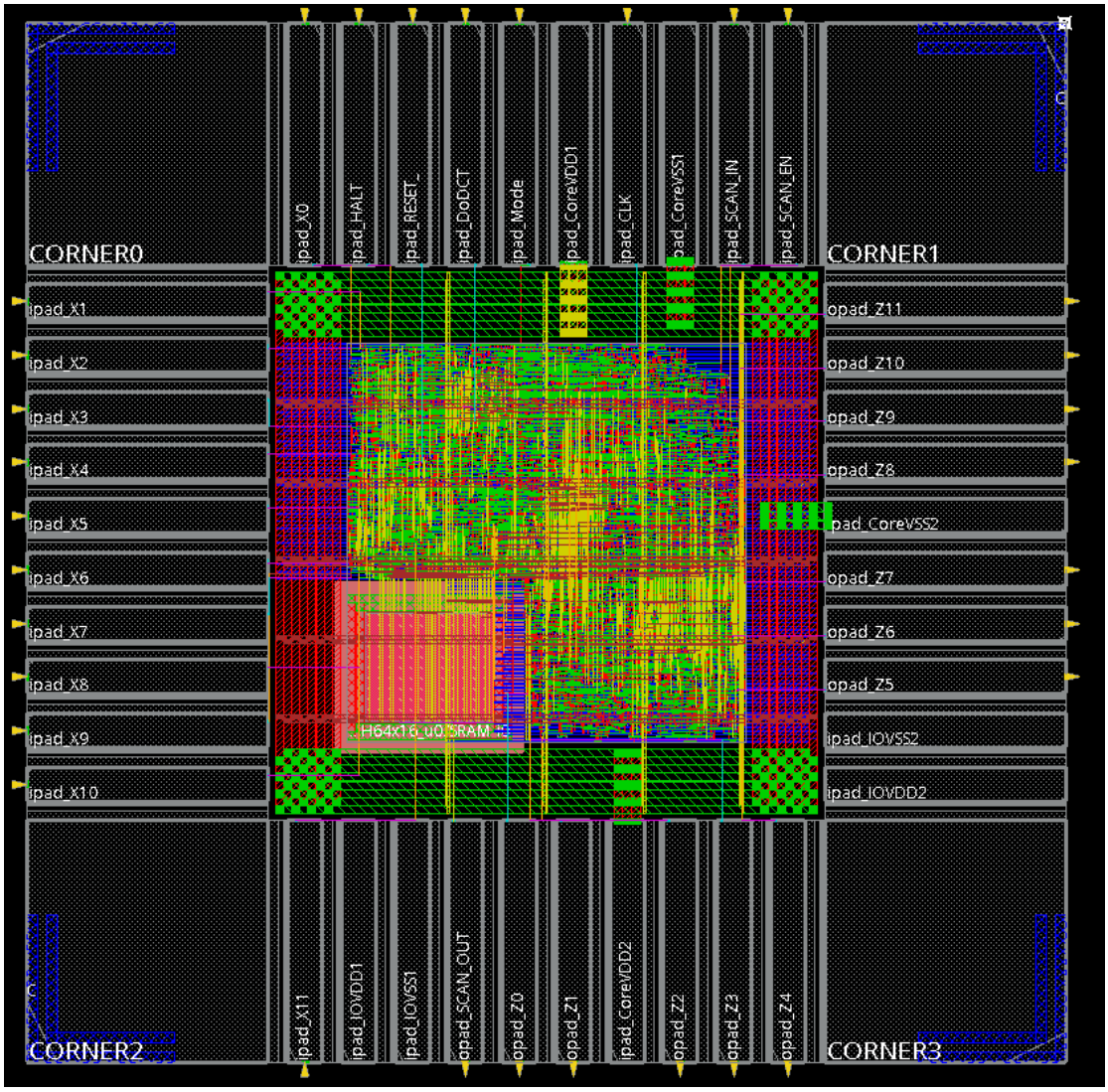
3. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/powerplan

If there are dangling wires, use hot key T (shift + t) to fix it.

Placement

1. innovus # > **createBasicPathGroups -expanded**
2. innovus # > **get_path_groups**
3. innovus # > **place_opt_design**

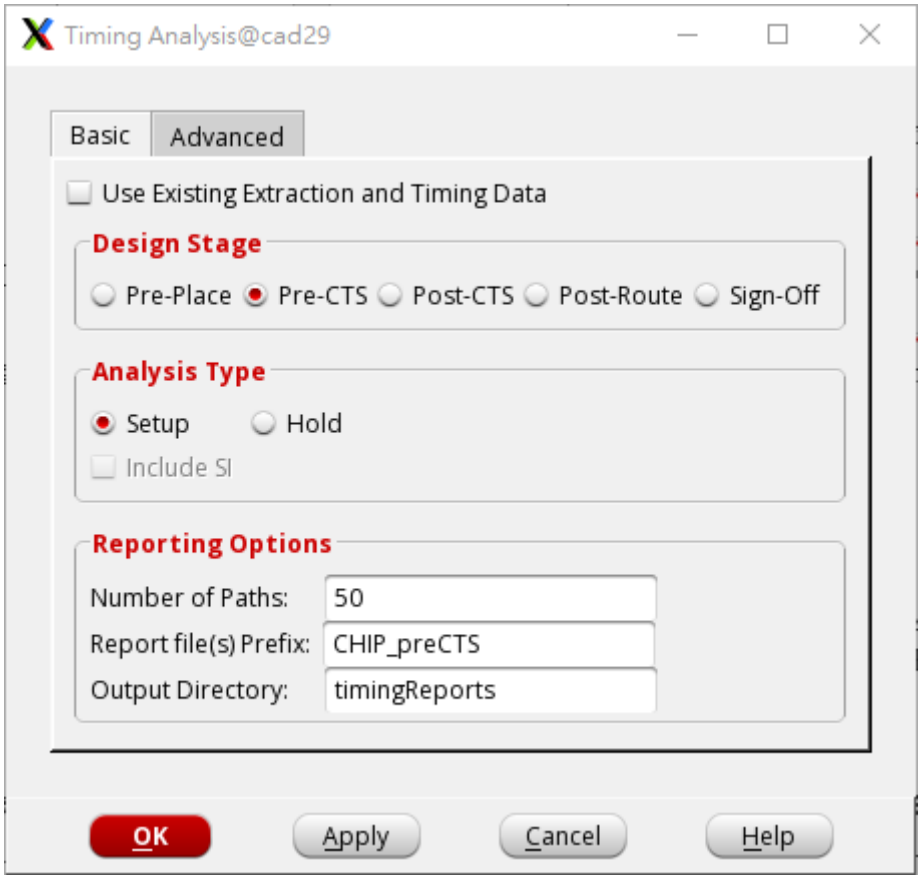
Change to **Physical view**  to check if the cells are placed correctly.



4. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/place
5. In-Place Optimization – Before Clock Tree Synthesis

   5.1 Open ***Timing → Report Timing…***

   5.2 Perform First Encounter trial route to model the interconnection RC effects
   - Design Stage ◆ pre-CTS
   - Analysis Type ◆ Setup
   - Click OK button




```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.010  |  0.010  |  3.446  |  0.218  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |    109 (109)     |    -55     |    110 (110)     |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

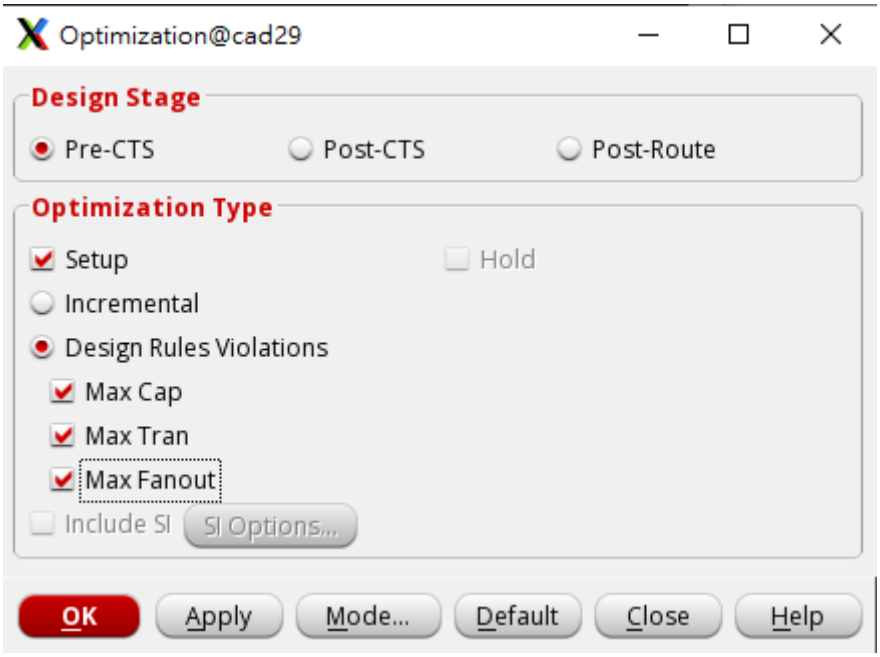
5.3 If the timing slack is negative, or there are DRVs, open ***ECO → Optimize Design…***

5.4 Perform pre-CTS IPO

- Design Stage ◆ pre-CTS
- Optimization Type

- Setup
- Design Rule Violations
- Max Cap
- Max Tran
- Max Fanout

➢ Click OK button

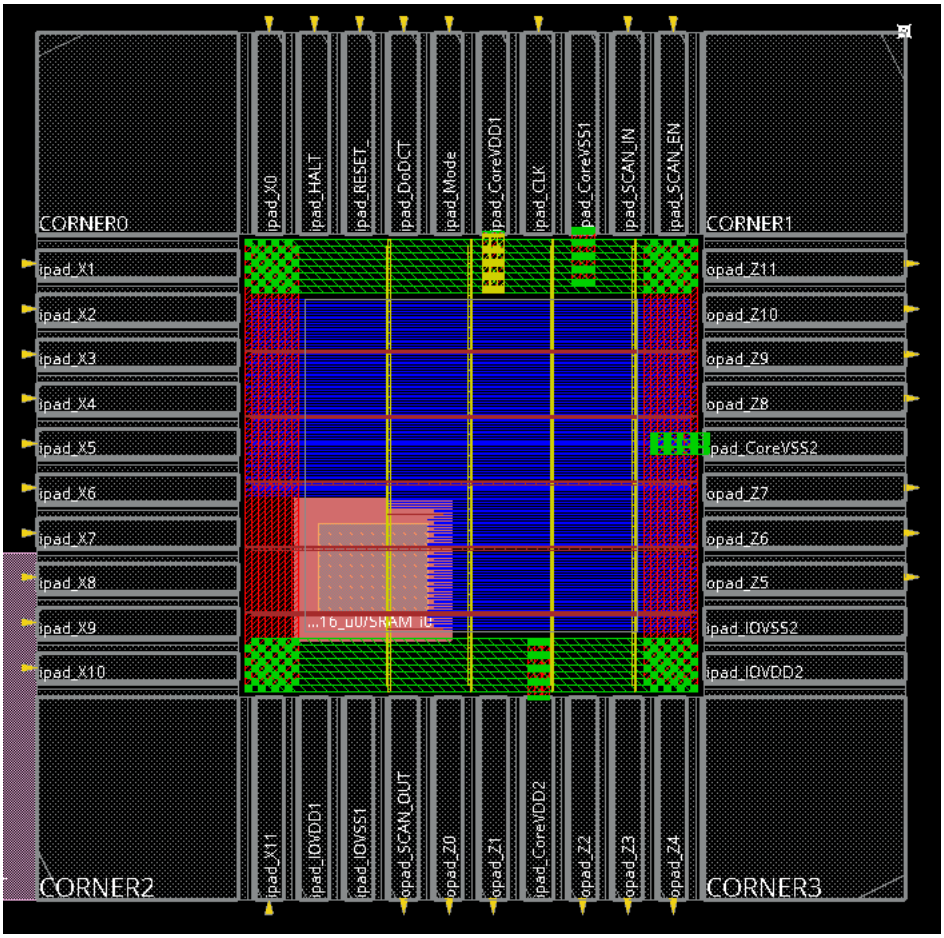



```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.005  |  0.005  |  3.491  |  0.235  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      1 (1)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+
```

6. Save file
   - ➢ Open ***File*** → ***Save Design…***
   - ➢ Choose ◆ Innovus
   - ➢ File Name: DBS/place

Checkpoints

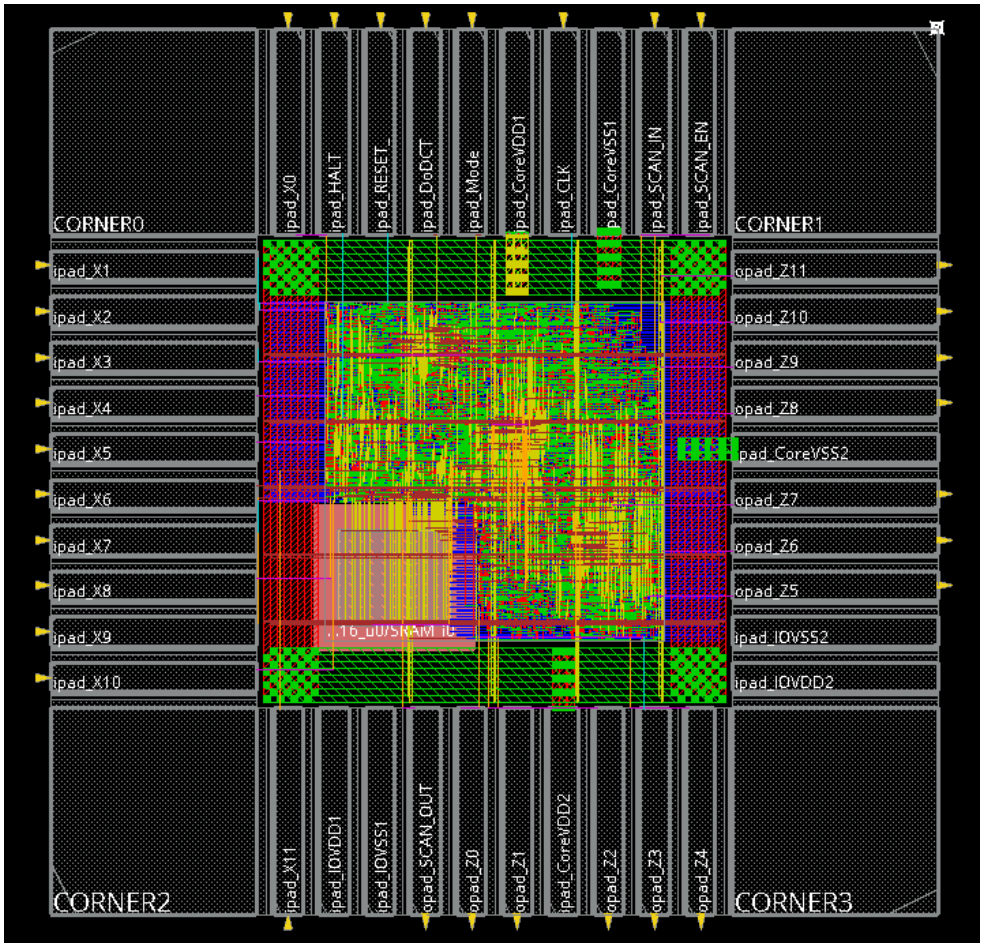
1. Take a screenshot after powerplan (IO filler is added) and show verification results of DRC and connectivity.



```
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 530.400 353.600 707.200} 20 of 36
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 530.400 530.400 707.200} 21 of 36
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 530.400 707.200 707.200} 22 of 36
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {707.200 530.400 884.000 707.200} 23 of 36
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {884.000 530.400 1058.820 707.200} 24 of 36
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 707.200 176.800 884.000} 25 of 36
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 707.200 353.600 884.000} 26 of 36
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 707.200 530.400 884.000} 27 of 36
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 707.200 707.200 884.000} 28 of 36
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {707.200 707.200 884.000 884.000} 29 of 36
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {884.000 707.200 1058.820 884.000} 30 of 36
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 884.000 176.800 1058.620} 31 of 36
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 884.000 353.600 1058.620} 32 of 36
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 884.000 530.400 1058.620} 33 of 36
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 884.000 707.200 1058.620} 34 of 36
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {707.200 884.000 884.000 1058.620} 35 of 36
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {884.000 884.000 1058.820 1058.620} 36 of 36
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.2  ELAPSED TIME: 0.00  MEM: 3.0M) ***
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Nov 20 21:20:22 2022

Design Name: CHIP
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1058.8200, 1058.6200)
Error Limit = 1000; Warning Limit = 50
Check specified nets
*** Checking Net VDD
*** Checking Net VSS

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Nov 20 21:20:22 2022
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

2. Take a screenshot after placement (physical view) and show pre-cts setup time analysis report (ensure the slack of setup time >= 0 and no DRVs)




```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.001  |  0.001  |  3.479  |  0.280  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |    0.000       |      0 (0)       |
|   max_tran     |      0 (0)       |    0.000       |      0 (0)       |
|   max_fanout   |      0 (0)       |      0         |      1 (1)       |
|   max_length   |      0 (0)       |      0         |      0 (0)       |
+----------------+------------------+----------------+------------------+
```

3. **Due Tuesday, Nov. 21, 19:00**
4. Submit to NTU COOL in pdf format.