

Computer-Aided VLSI System Design

Verilog Simulation & Debugging Tools

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DCSL



Outline

- ❖ Environment Setup
- ❖ Basic commands in Unix/Linux
- ❖ VCS
- ❖ nWave
- ❖ SpyGlass Lint
- ❖ Text editors



Login to Linux Server

- ❖ Many EDA tools are provided only for the Linux OS

- ❖ Use software like PuTTY/PieTTY/**MobaXterm** on our local computer to login to the Linux server



NTUEE Linux Servers

- ❖ IC Design Lab (TA: 楊登燊)
 - <http://cad.ee.ntu.edu.tw/wordpress>
- ❖ Server list
 - <http://cad.ee.ntu.edu.tw/wordpress/?p=33>

* IP	Name	Type	CPU	CPU Clock	Memory	OS	Note
59	cad16	IBM X3500	Intel Xeon 64	1.2 GHz * 24	40 GB	CentOS 7	
60	cad17	IBM X260	Intel Xeon 64	1.2 GHz * 24	32 GB	CentOS 7	
63	cad20	IBM x260	Intel Xeon 64	2.4 GHz * 16	20 GB	CentOS 7	
64	cad21	DELL R620	Intel Xeon 64	2 GHz * 32	48 GB	CentOS 7	
66	cad23	DELL R620	Intel Xeon 64	2 GHz * 16	96 GB	CentOS 7	
70	cad27	DELL R640	Intel Xeon Silver 4110	2.1 GHz * 32	128 GB	CentOS 7	



Account Application for IC Design LAB Server

❖ Website

— <https://reurl.cc/Ny1kk9>



授課教授 / 指導教授 *

您的回答

楊家驤

課號 (請查詢過後填寫, 修課者填錯一律不通過; 研究&專題則不需填寫)

(<https://nol2.aca.ntu.edu.tw/nol/guest/index.php>)

您的回答

EEE5022

課程名稱 (Ex: 積體電路設計; 若為研究請打研究用; 若為專題請打專題用) *

您的回答

電腦輔助積體電路系統設計



X Window System

- ❖ X Window System (X11, X, and sometimes informally X-Windows) is a windowing system for bitmap displays, common on UNIX-like (ex: Linux) operating systems

- ❖ Microsoft Windows is not shipped with support for X, but many third-party implementations exist, as free and open source software such as Cygwin/X, and proprietary products such as Xming



X11 Installation for Mac User

- ❖ Website for installation
 - <https://www.xquartz.org/>
- ❖ Use following command to login from terminal to server

```
ssh -X YOUR_ID@cad##.ee.ntu.edu.tw
```



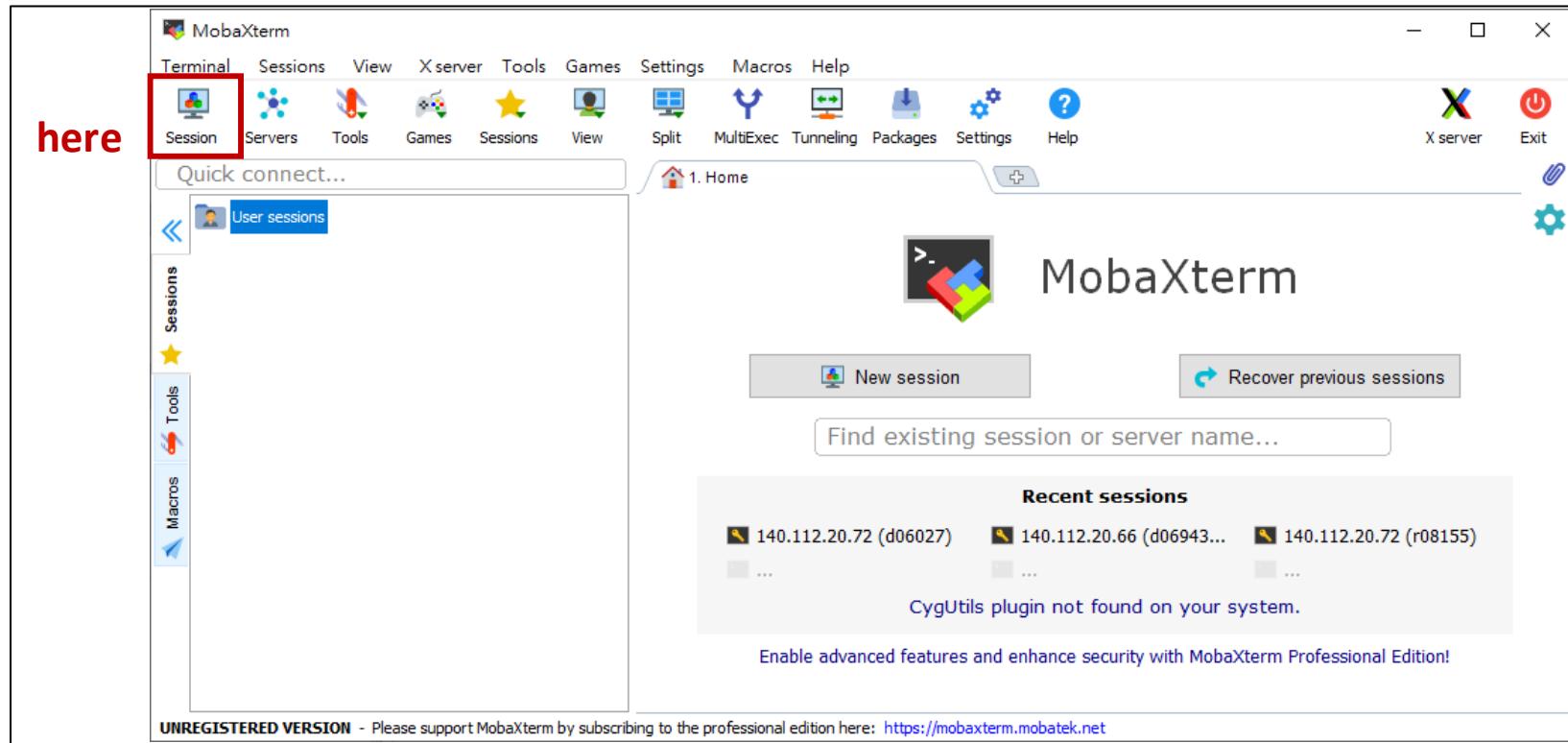
Introduction to MobaXterm

- ❖ MobaXterm is free software that can be installed onto your local Windows or Mac computer which provides a graphical user interface and a command line shell for the server.
- ❖ Official website
 - <https://mobaxterm.mobatek.net/>
- ❖ MobaXterm provides useful features for developers
 - **Multitab terminal** with embedded Unix commands (ls , cd, ...)
 - **Embedded X11 server** for easily exporting your Linux display
 - **Passwords management** for SSH, SFTP, etc (on demand password saving)
 - ...



Session Settings

- ❖ Click the Session button and specify which session you want. Usually this will be **SSH**. For that click SSH.





Session Settings

Session settings

SSH Telnet Rsh Xdmcp RDP VNC FTP SFTP Serial File Shell Browser Mosh Aws S3 WSL

Basic SSH settings **Server IP** Your account ID

Remote host * **140.112.20.70** Specify username **r08001**

Port **22**

Advanced SSH settings Terminal settings Network settings Bookmark settings

X11-Forwarding Compression Remote environment: **Interactive shell** Do not exit after command ends Follow SSH path (experimental) Use private key Adapt locales on remote server Execute command:
SSH-browser type: **SFTP protocol** Execute macro at session start: **<none>**



Session Settings

The screenshot shows the MobaXterm application window. The menu bar includes Terminal, Sessions, View, Xserver, Tools, Games, Settings, Macros, and Help. The toolbar contains icons for Session, Servers, Tools, Games, Sessions, View, Split, MultiExec, Tunneling, Packages, Settings, and Help. On the right, there are buttons for X server and Exit, along with a gear icon for settings. A sidebar on the left has tabs for Sessions, Tools, and Macros. The main area displays a session titled "1. Home" with a "New session" button and a search bar for "Find existing session or server name...". A "Recent sessions" list includes "140.112.20.70 (r08001)" and other entries. A message at the bottom states "CygUtils plugin not found on your system." and "Enable advanced features and enhance security with MobaXterm Professional Edition!". A note at the bottom says "UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>".



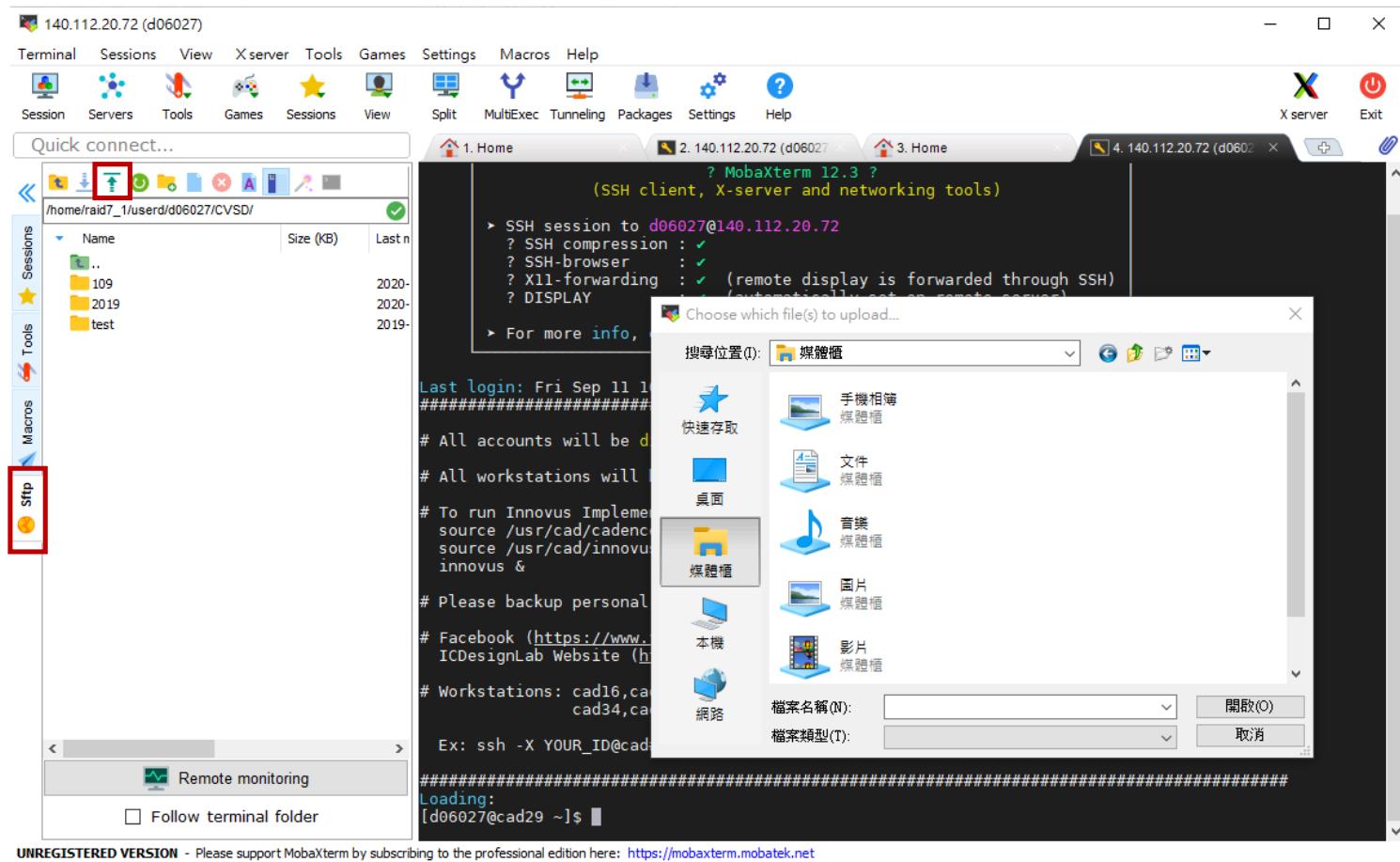
Command Line Shell

- ❖ We can also use the command line shell to login to the server
 - ssh r08001@140.112.20.70 [-p 22]



Upload Files

- ❖ Upload files from your local PC to the server.

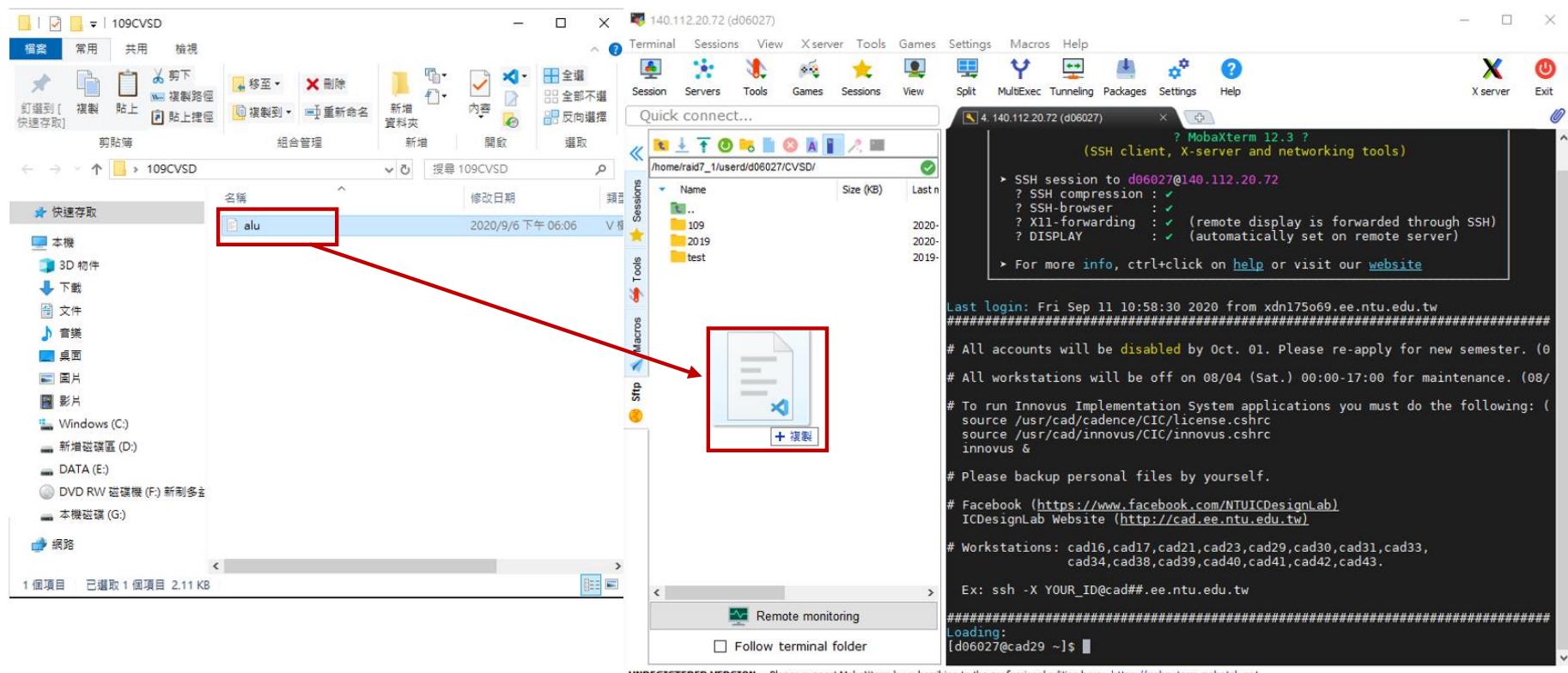


UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>



Upload Files

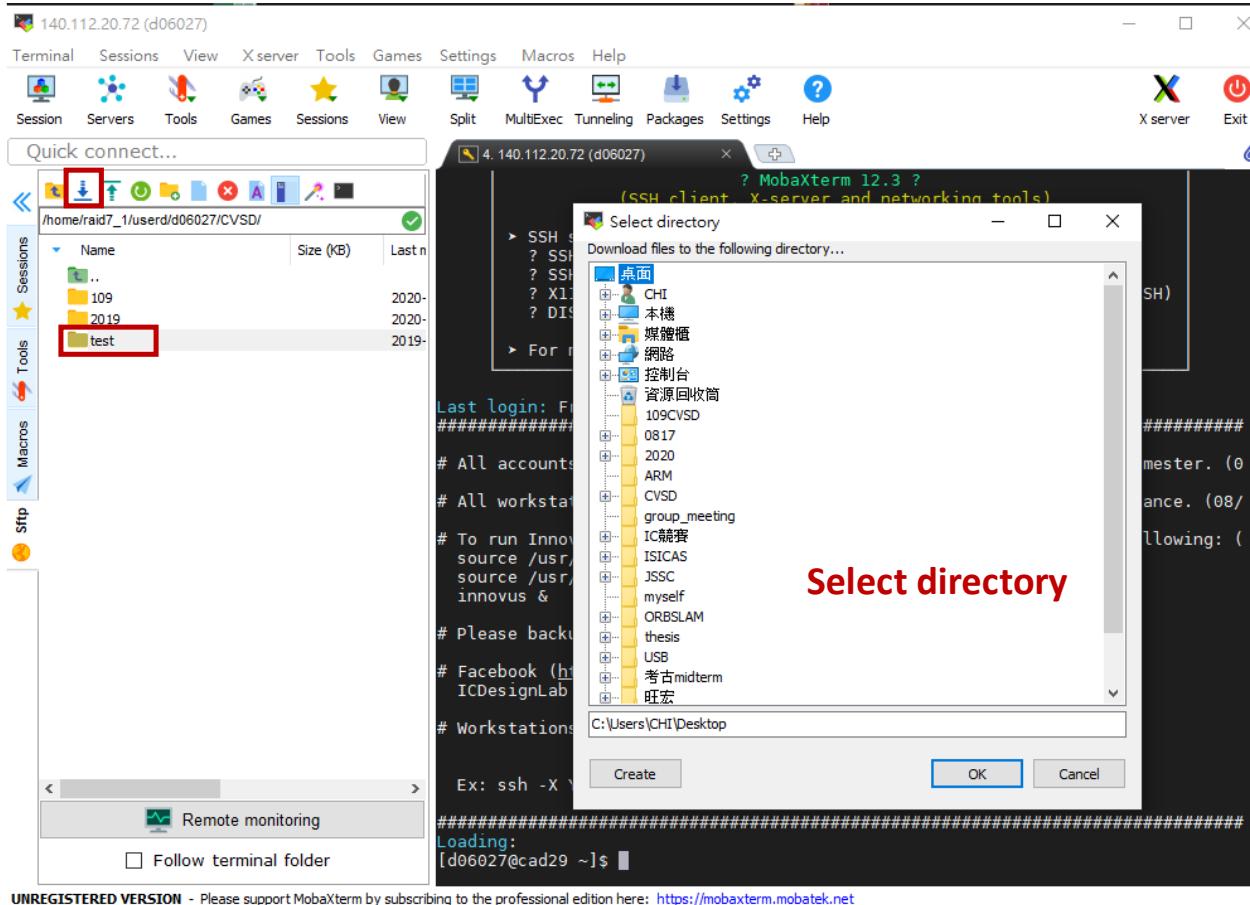
- ❖ You can also move and copy files by using the drag-and-drop





Download Files

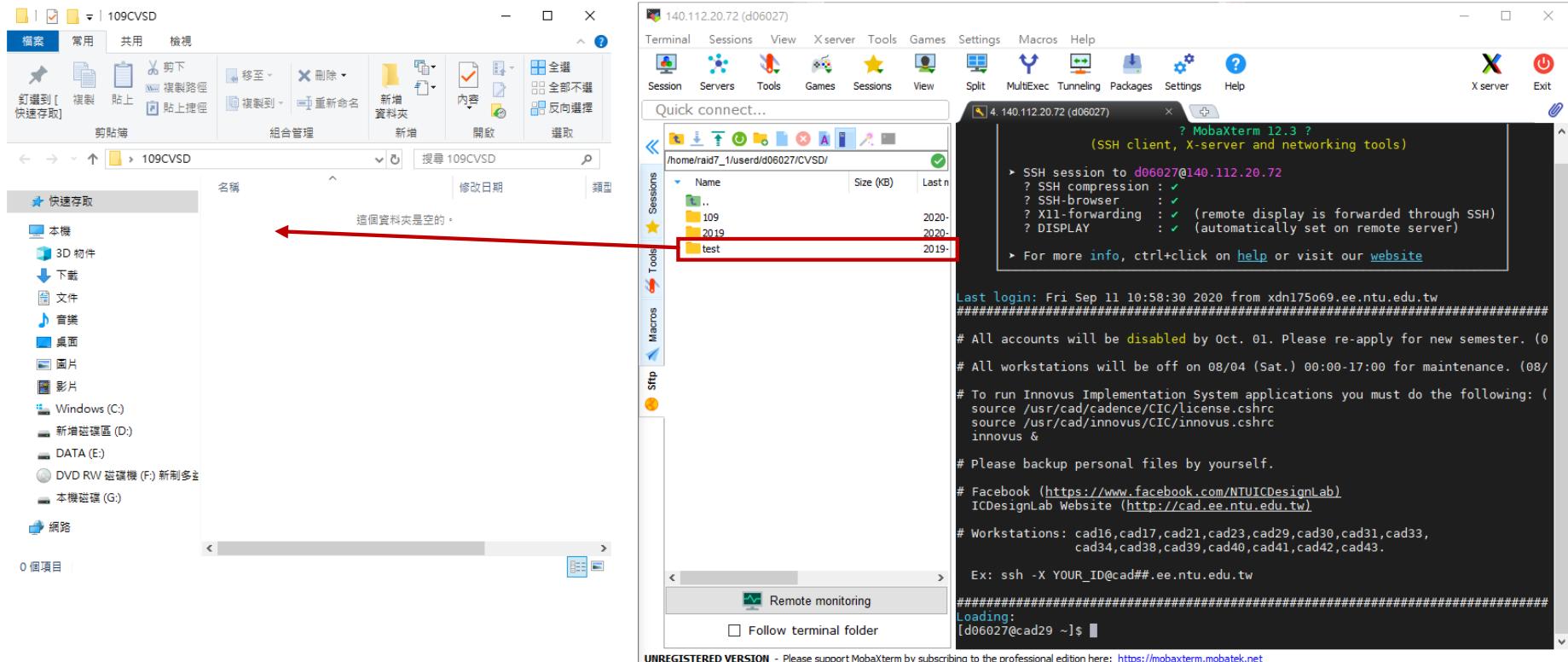
- ❖ Download files from the server to local PC





Download Files

- ❖ Move and copy files by using the drag-and-drop





Basic Commands

- ❖ **ls** : list files
- ❖ **cd** : change directory
- ❖ **pwd** : show current path
- ❖ **cp** : copy
 - File: cp <source file> <destination>
 - Folder: cp -rf <source folder> <destination>
- ❖ **mv** : revise file's name/ move files
 - Revise: mv <source name> <new name>
 - Move: mv <source name> <destination>
- ❖ **rm** : delete files
 - File: rm <source file>
 - Folder: rm -rf <source folder>



Basic Commands

- ❖ **mkdir** : create folder
 - mkdir <folder name>
- ❖ **tar** : compress/decompress
 - Compress (*.tar): tar -cvf <file.tar> <folder>
 - Decompress (*.tar): tar -xvf <file.tar>
- ❖ **more** : show content of the text file
- ❖ **ln** : link
 - ln -s <source file> <target file>



Introduction to VCS

- ❖ The Synopsys® VCS® is a high-performance, high-capacity Verilog simulator

- ❖ We can use VCS to
 - Compiling your source files into an executable binary file
 - Running the executable binary file



Before Using VCS

- ❖ Download **cvsd.cshrc** file from NTU cool

- ❖ Source the environment settings of CAD tools in terminal

```
source cvsd.cshrc
```

- ❖ If you try entering the command “**vcs**” but it turns out “**command not found**,” it means there's something wrong with the “***.cshrc**” file or the software license is out of date



Running Verilog

- ❖ Run the Verilog simulation

```
vcs -full64 testbench.v design.v +v2k -R -debug_access
```

- ❖ “**-debug_access**” is added to enable waveform file dumping
 - *.fsdb or *.vcd



Simulation Results

- ❖ Check the simulation result to see if the Verilog design is finished correctly

```
*Verdi* Loading libsscore_vcs202206.so
FSDB Dumper for VCS, Release Verdi_T-2022.06, Linux x86_64/64bit, 05/29/2022
(C) 1996 - 2022 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file m
.
*Verdi* : Create FSDB file 'qubit.fsdb'
*Verdi* : Begin traversing the scope (tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
-----
Congratulations! All data have been generated successfully!
-----PASS-----
$finish called from file "./th.v", line 491
$finish at simulation time 1364000
V C S   S i m u l a t i o n   R e p o r t
Time: 1364000 ps
CPU Time: 1.020 seconds;          Data structure size: 0.1Mb
Thu Aug 31 10:43:14 2023
CPU time: 2.643 seconds to compile + .606 seconds to elab + .636 seconds to lin
```



Introduction to nWave

- ❖ nWave is one of the best waveform (*.vcd or *.fsdb) viewer
- ❖ We can debug easily by checking the waveform file dumped during simulation
- ❖ Before using nWave, source the environment settings of CAD tools

```
source cvsd.cshrc
```



Start nWave

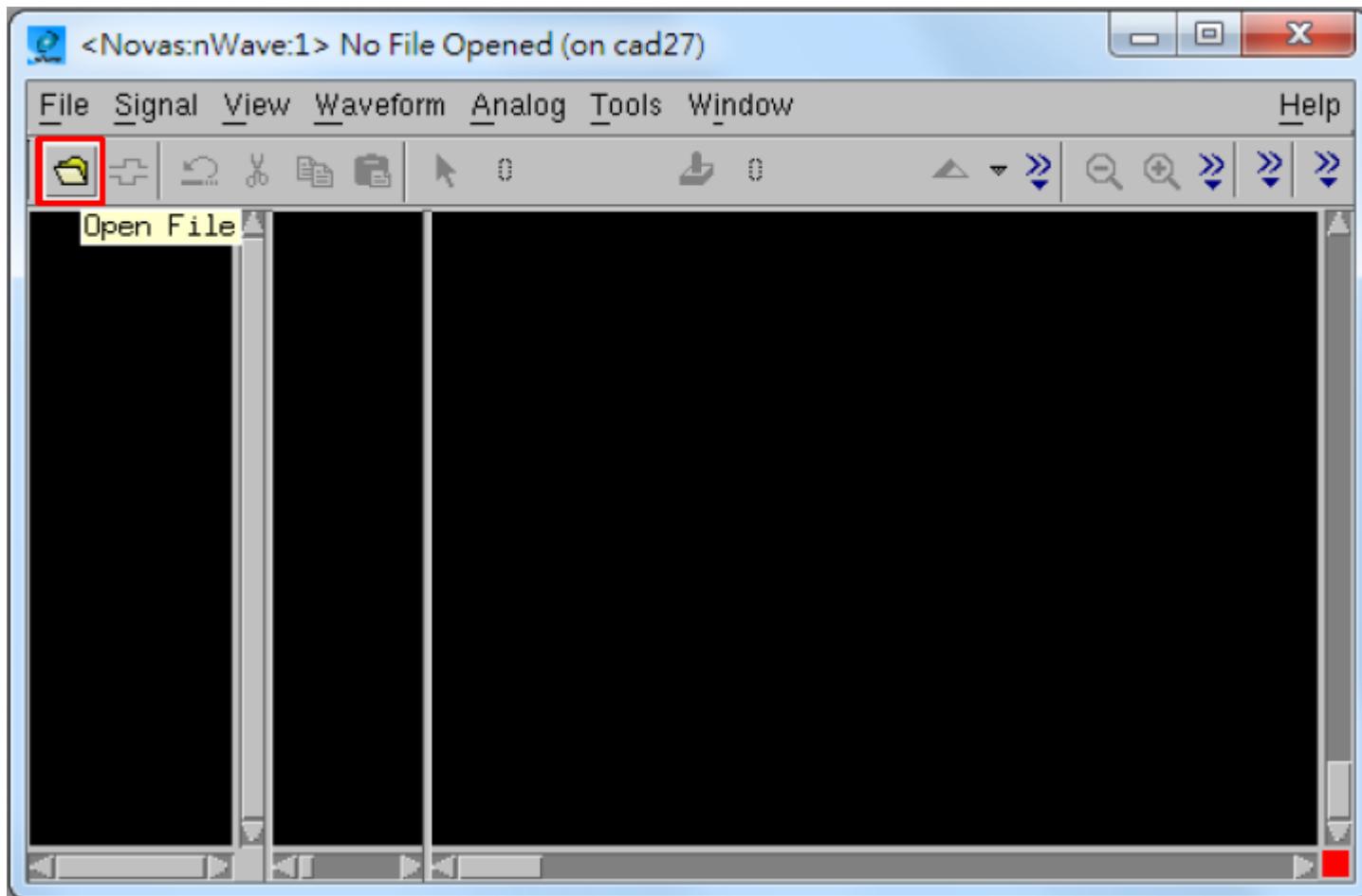
- ❖ Type the following command

```
nWave &
```

- ❖ The token “&” enable you to use the terminal while nWave is running in the background

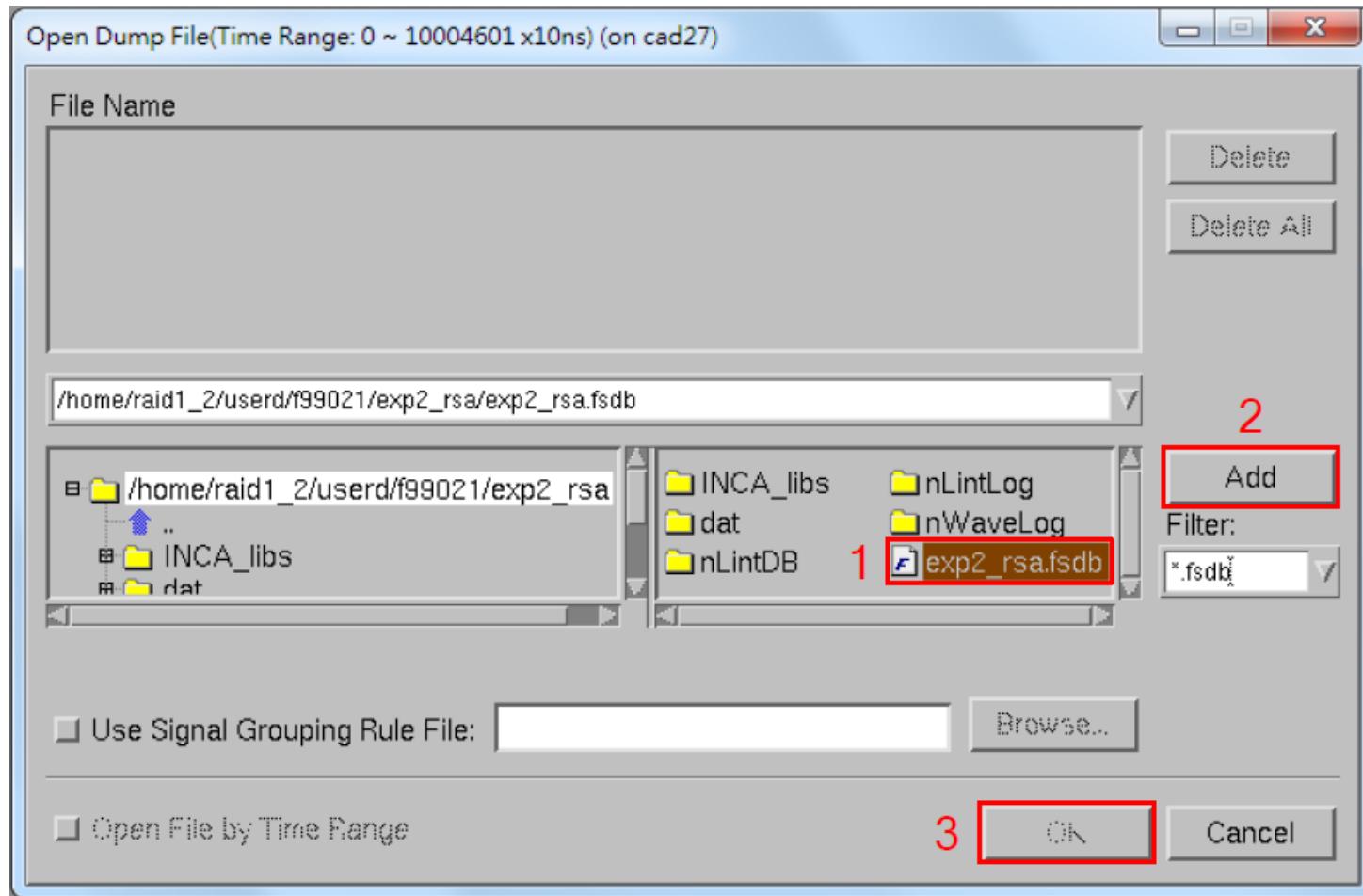


Open .fsdb File



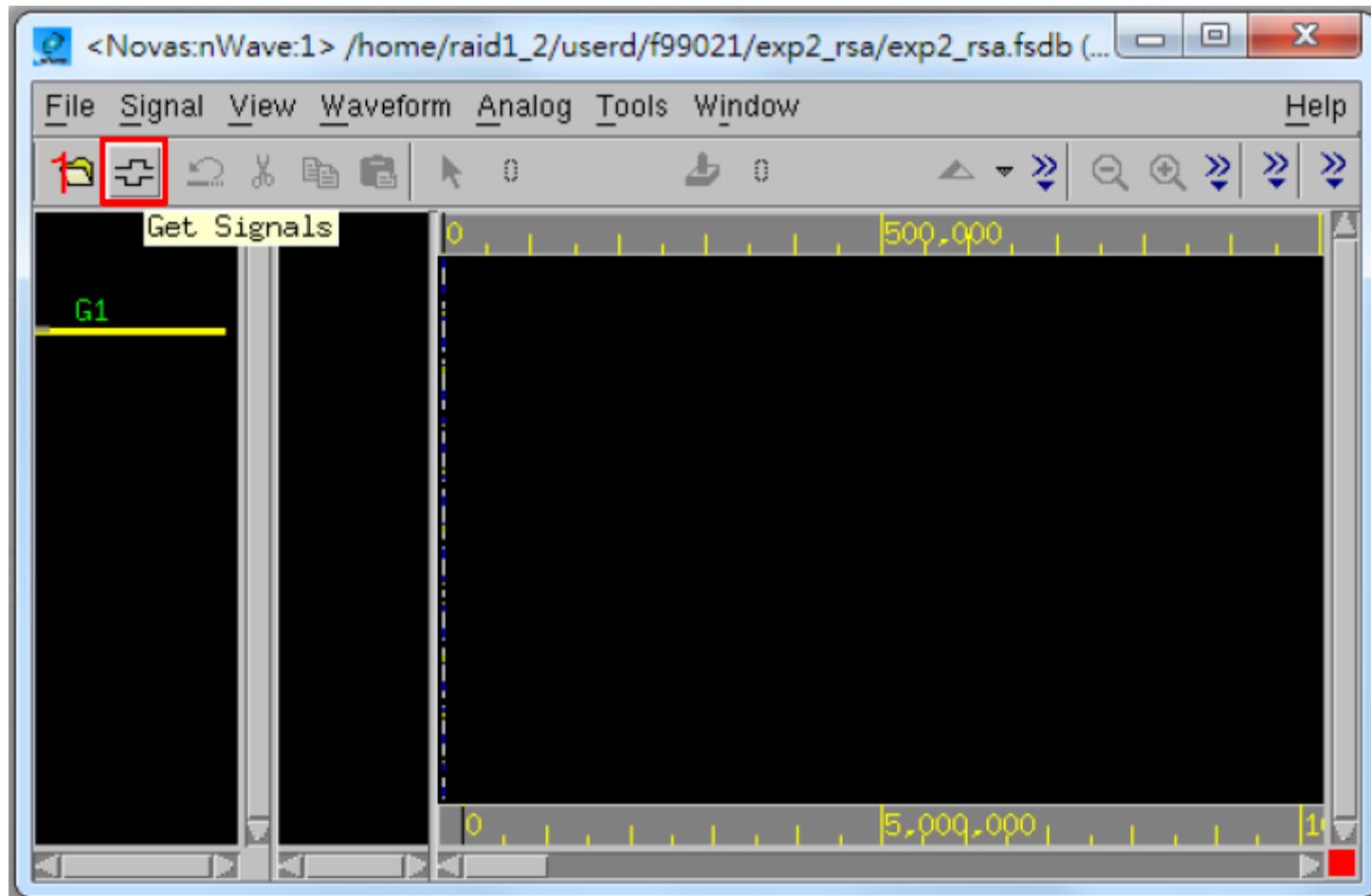


Open .fsdb File



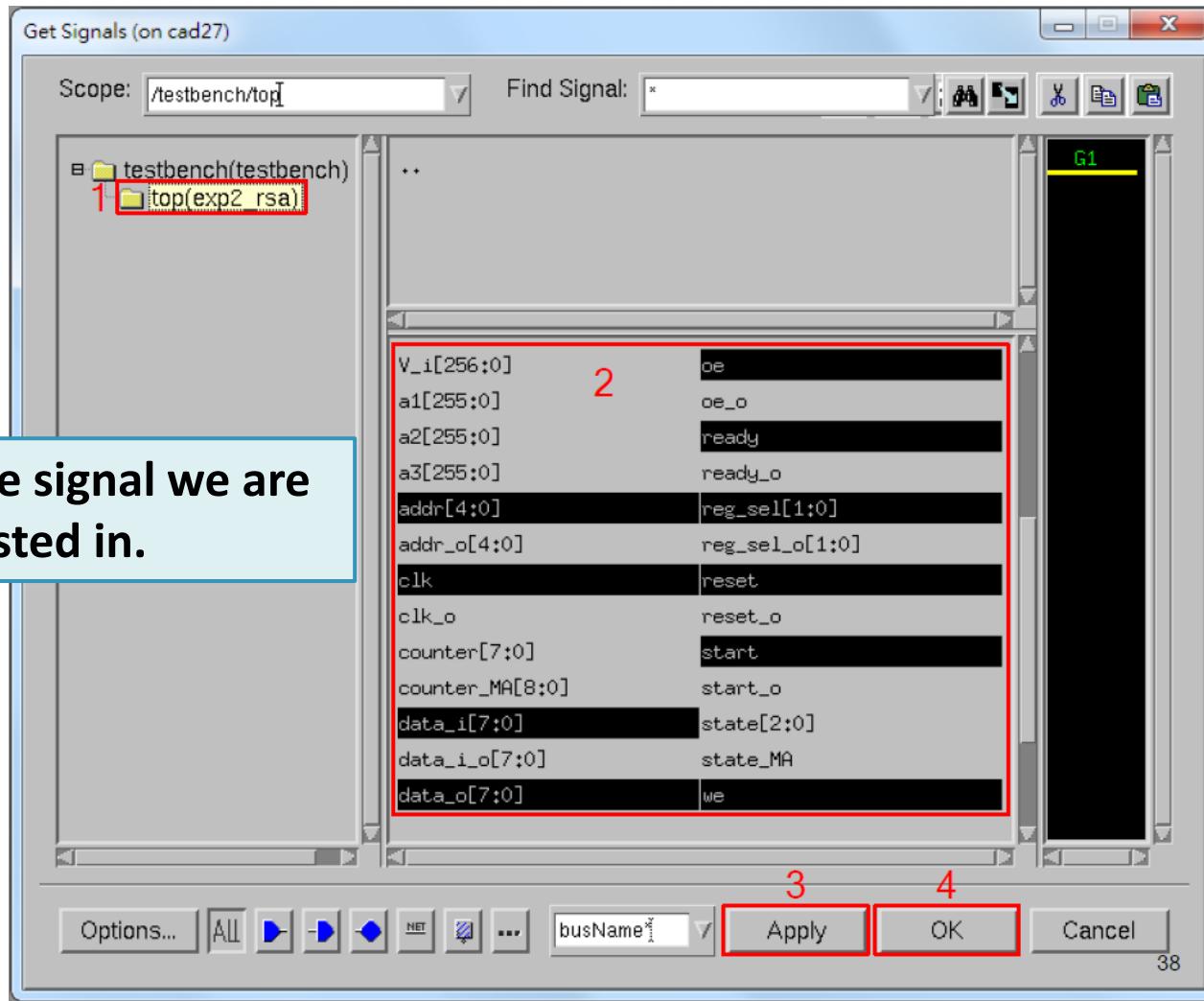


Choose Signal



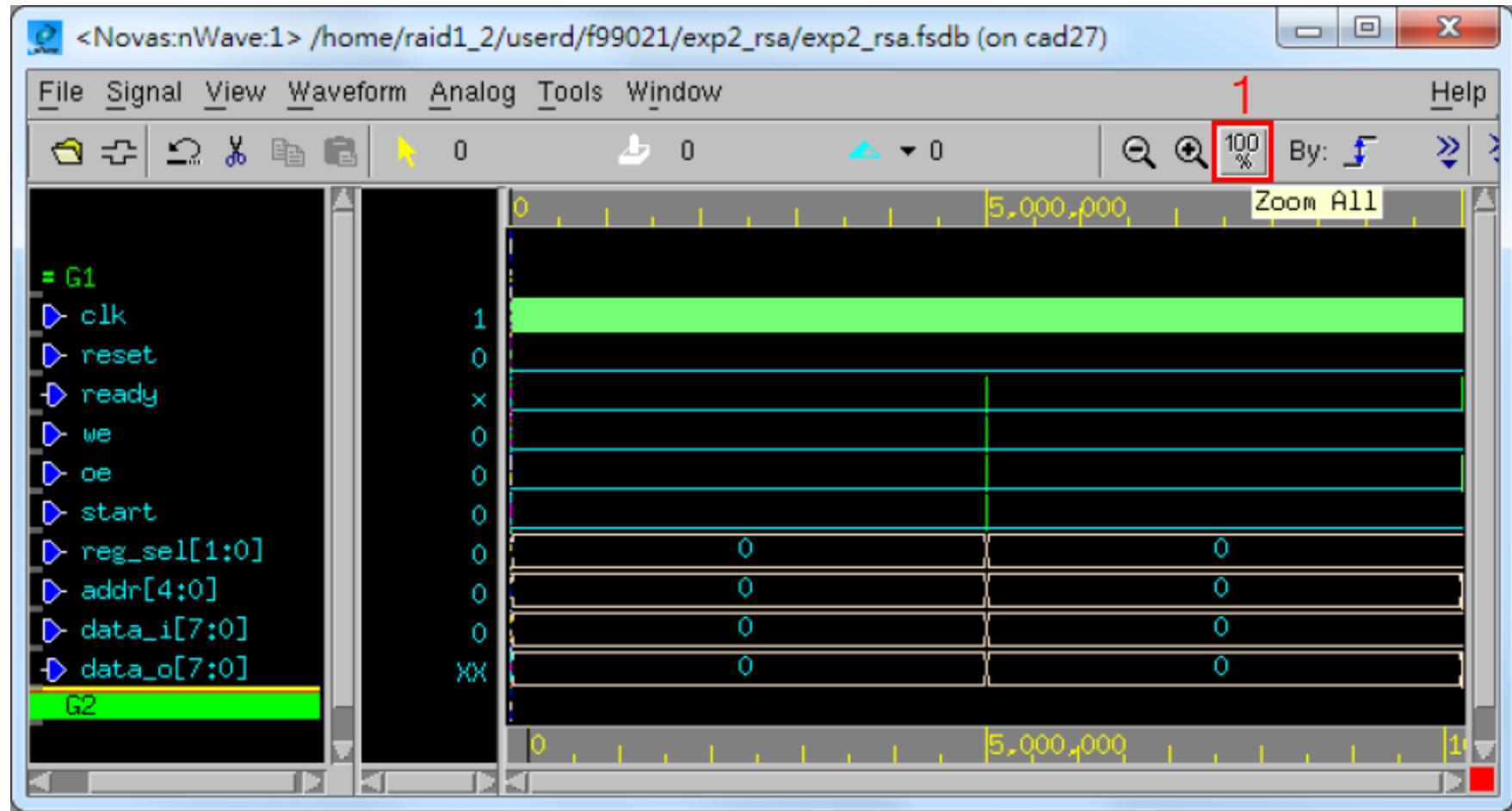


Choose Signal



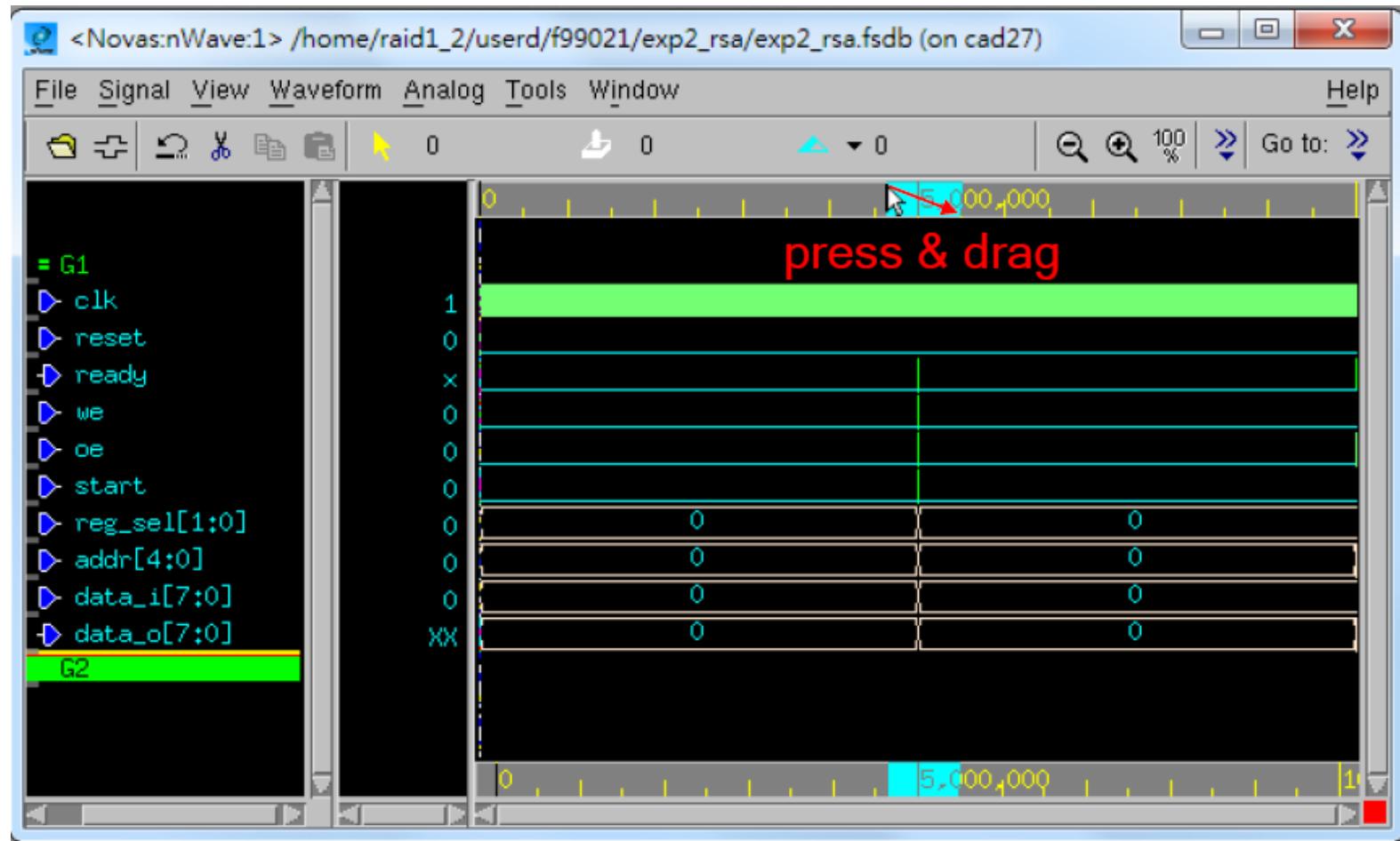


Browse the Whole Waveform



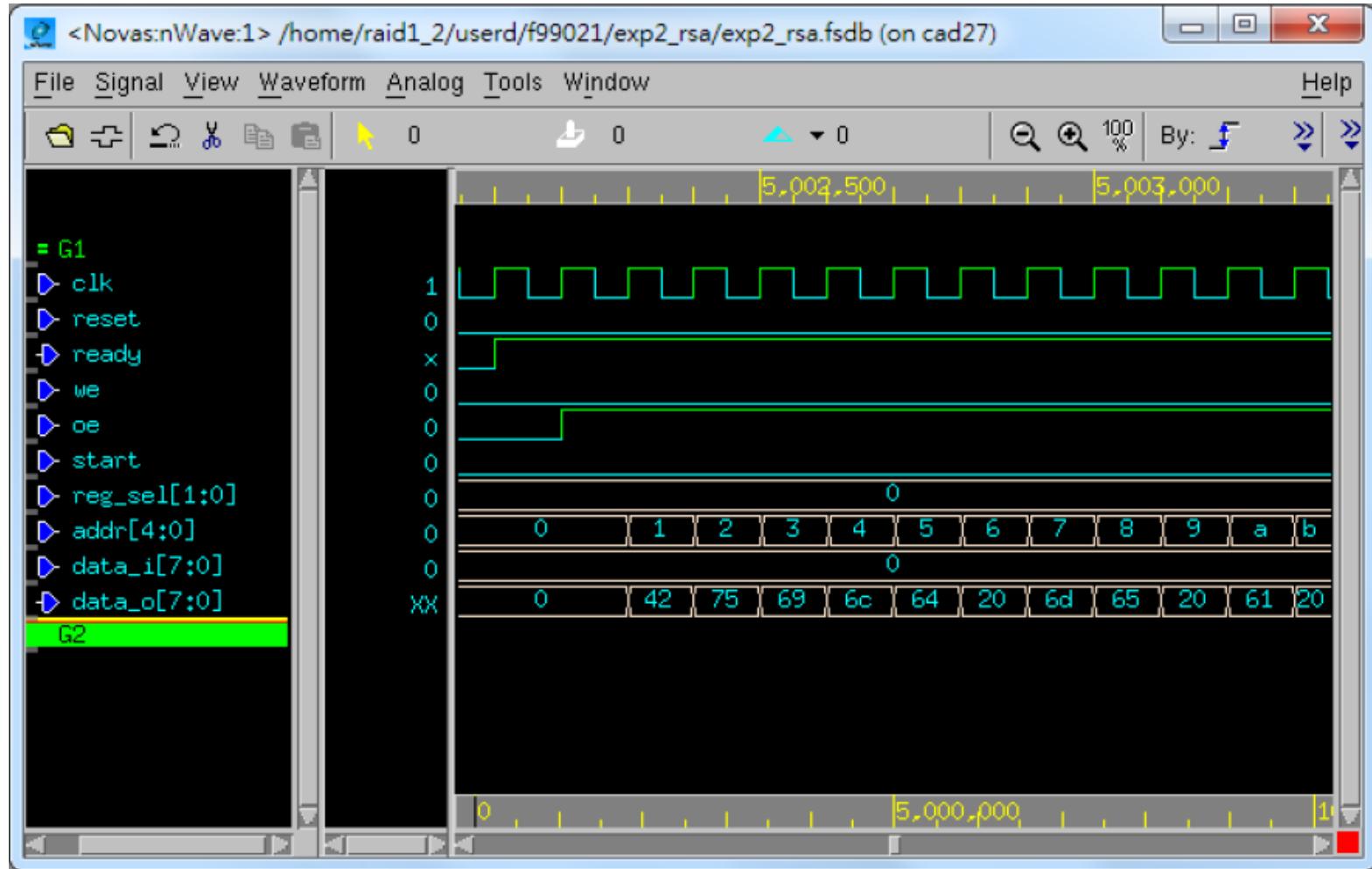


Browse the Specified Interval



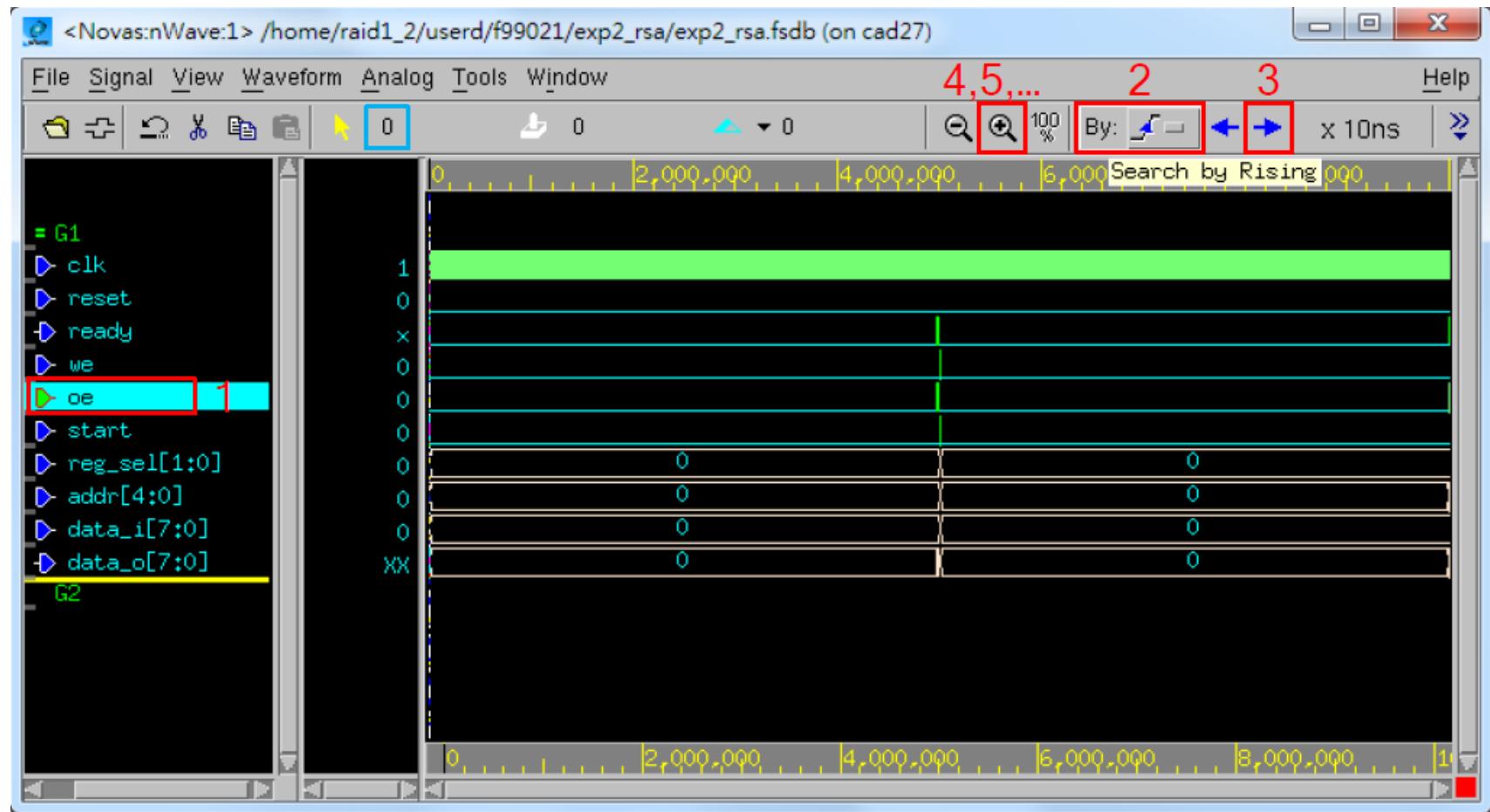


Browse the Specified Interval



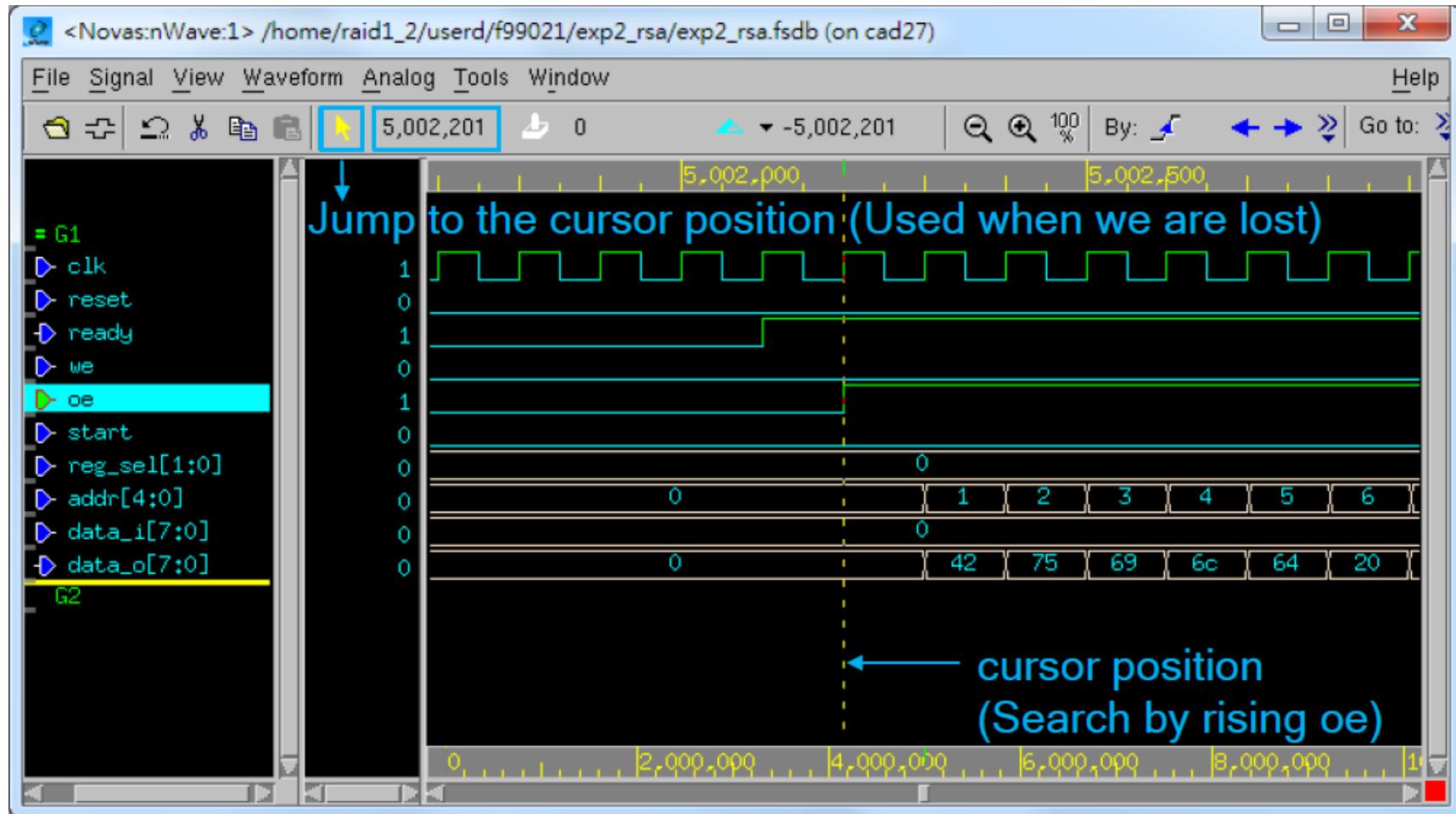


Search for Specified Signal



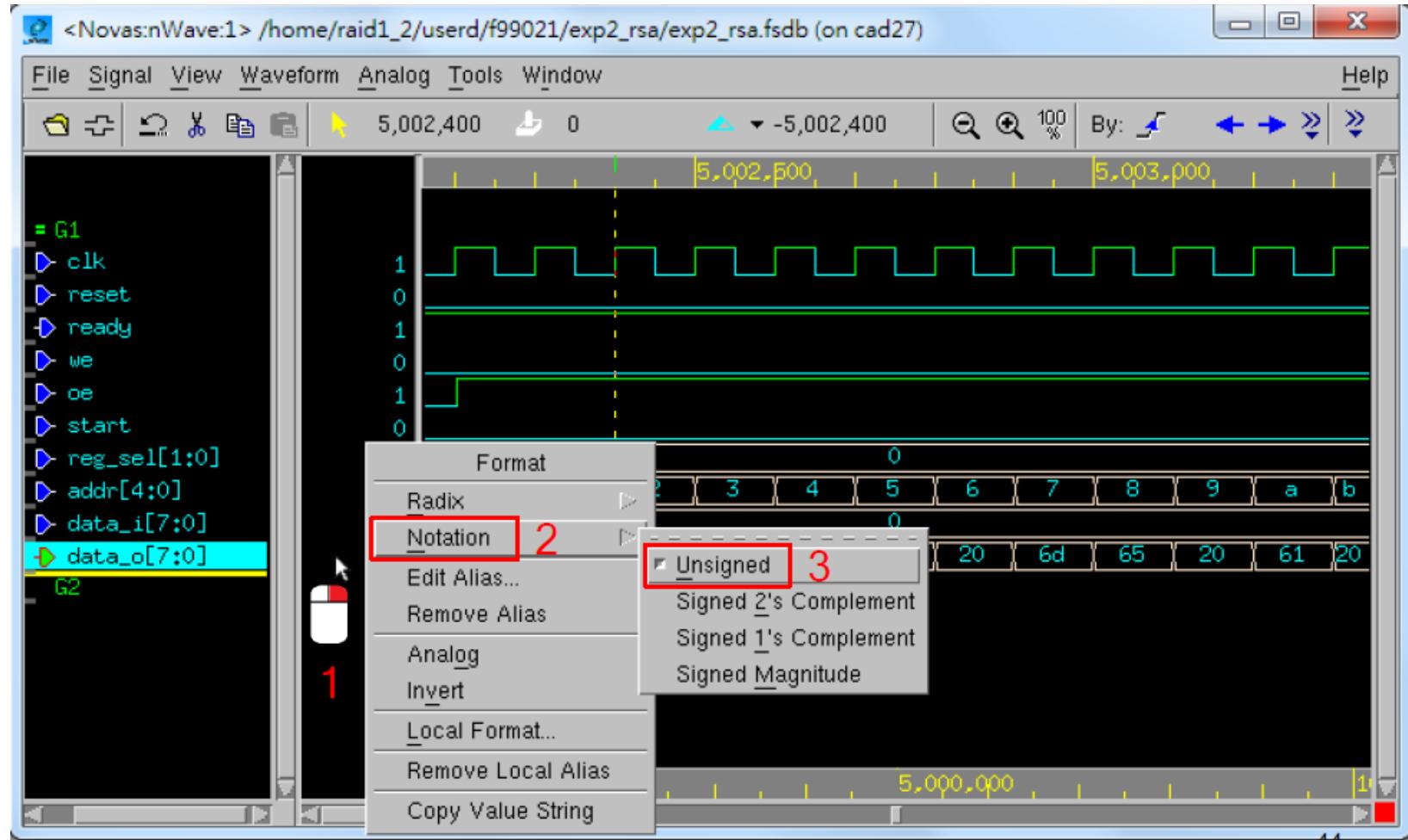


Search for Specified Signal



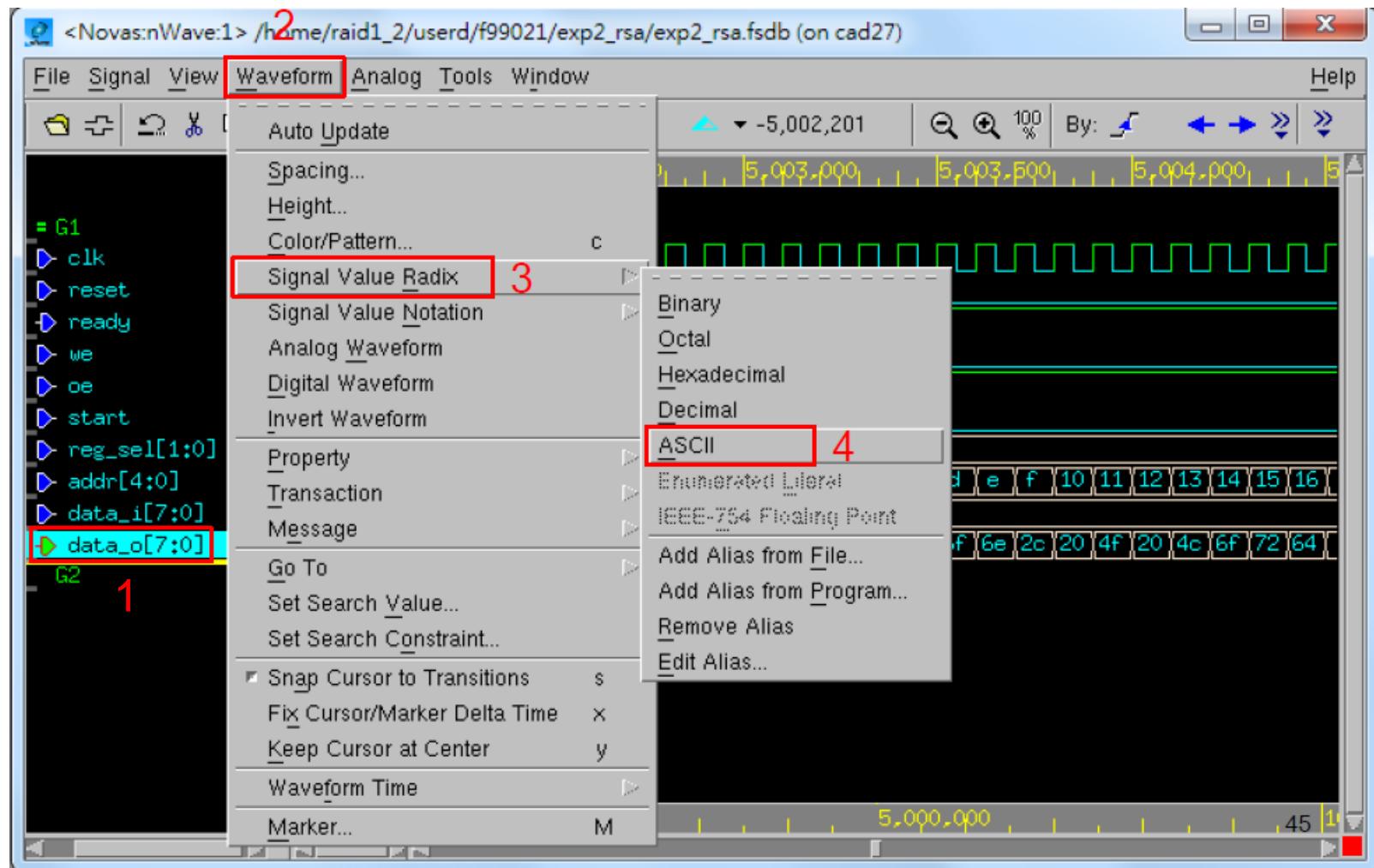


Change Sign Representation



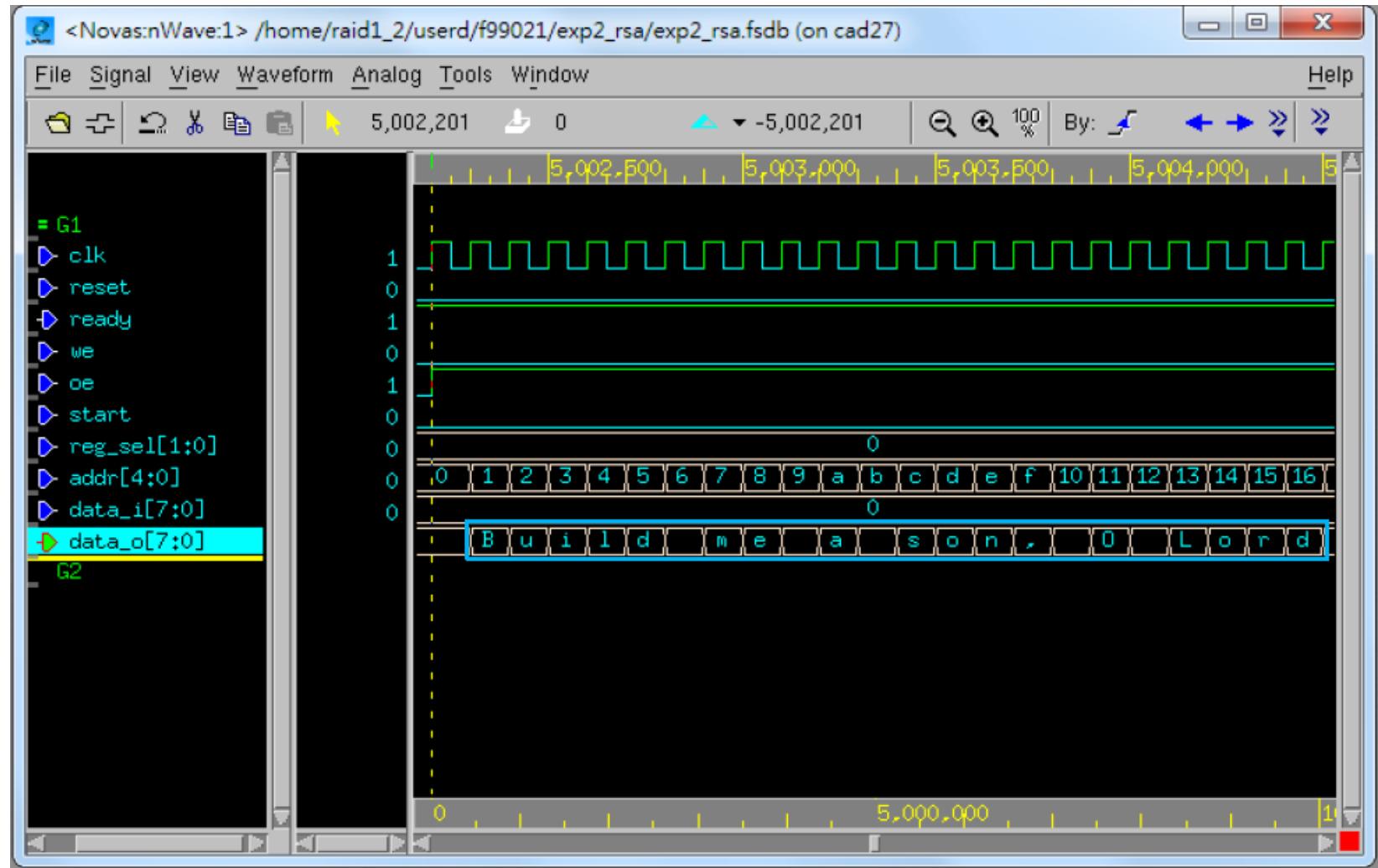


Change Radix Representation



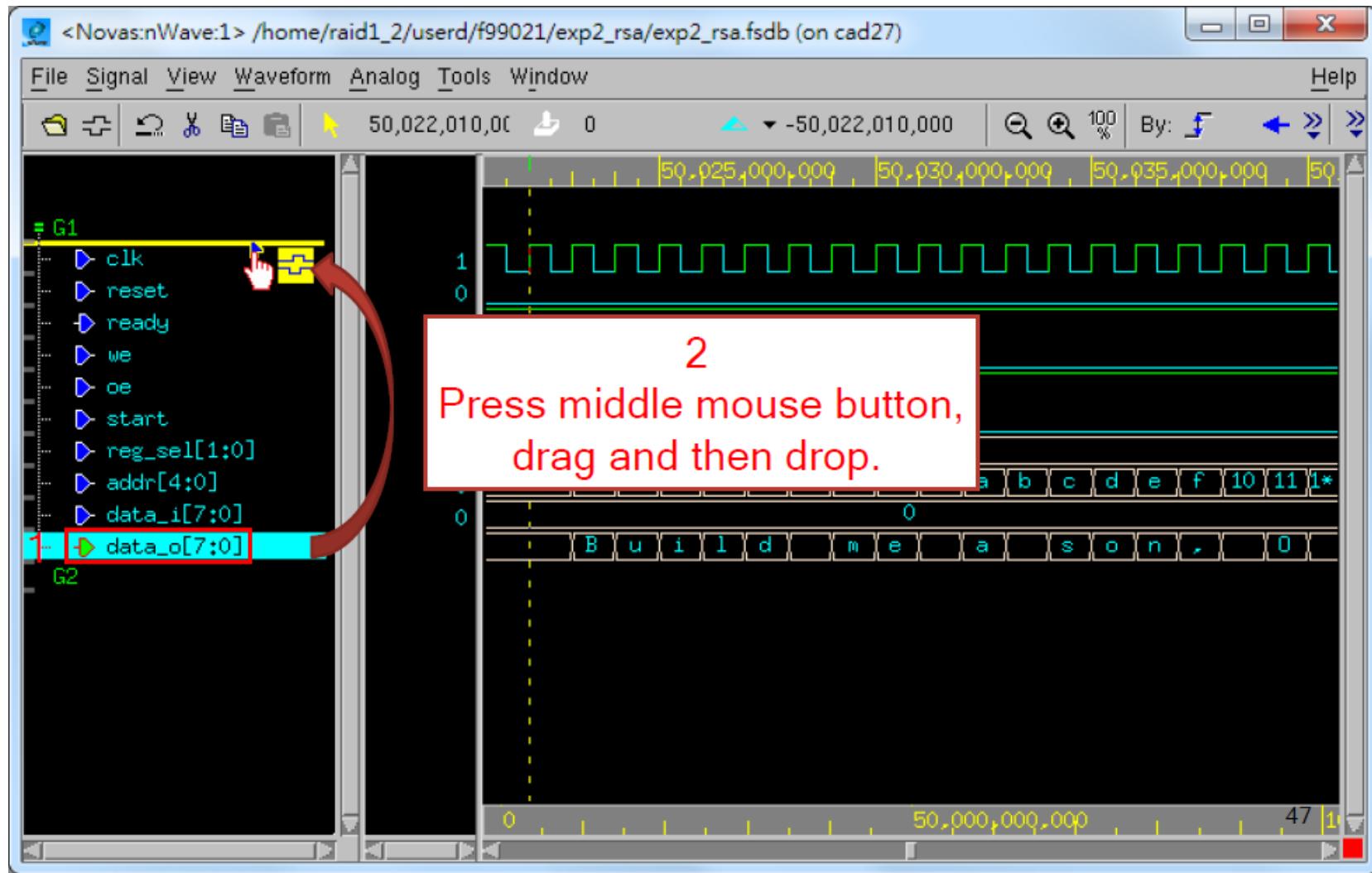


Change Radix Representation



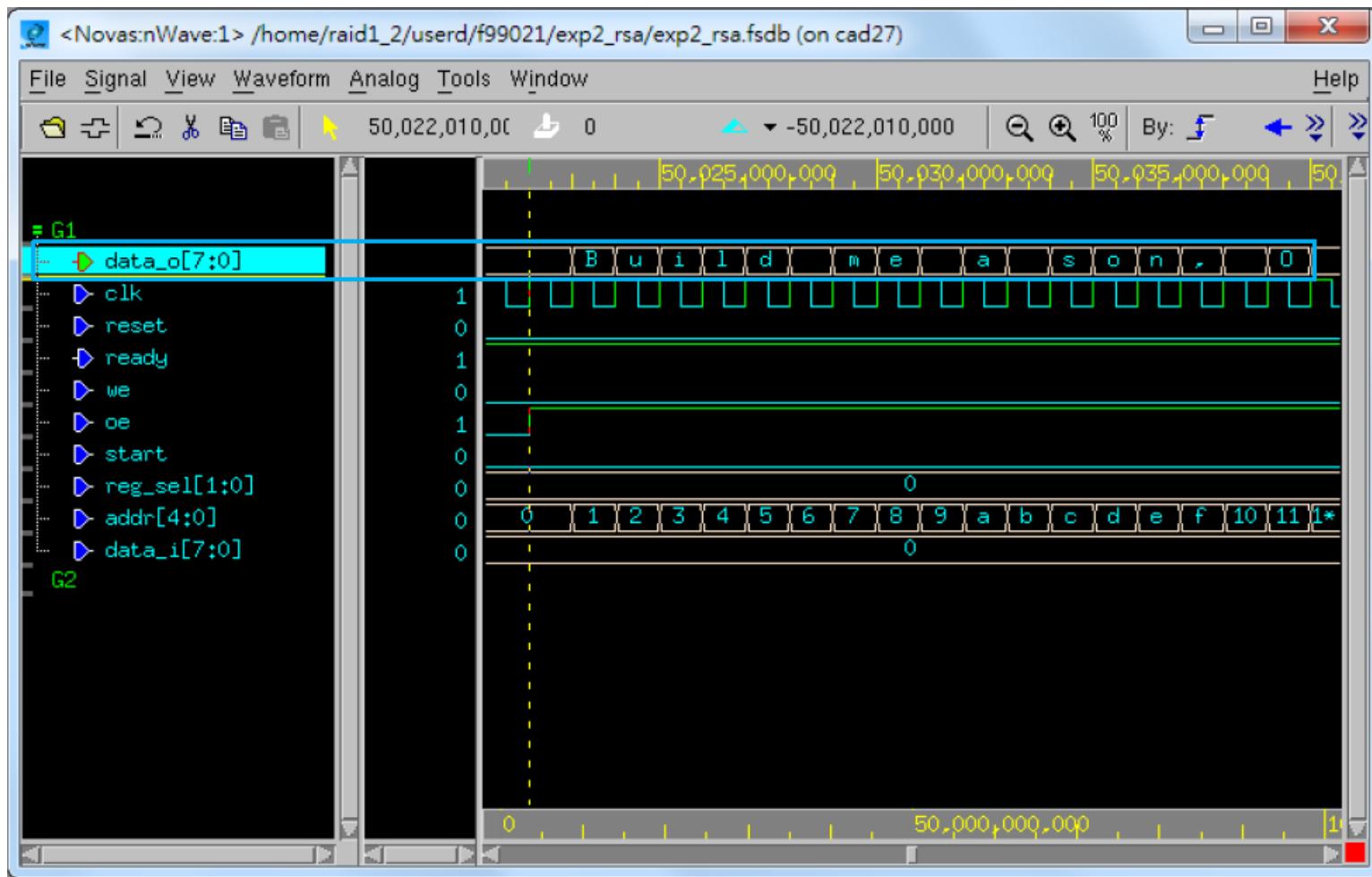


Change Signal Position





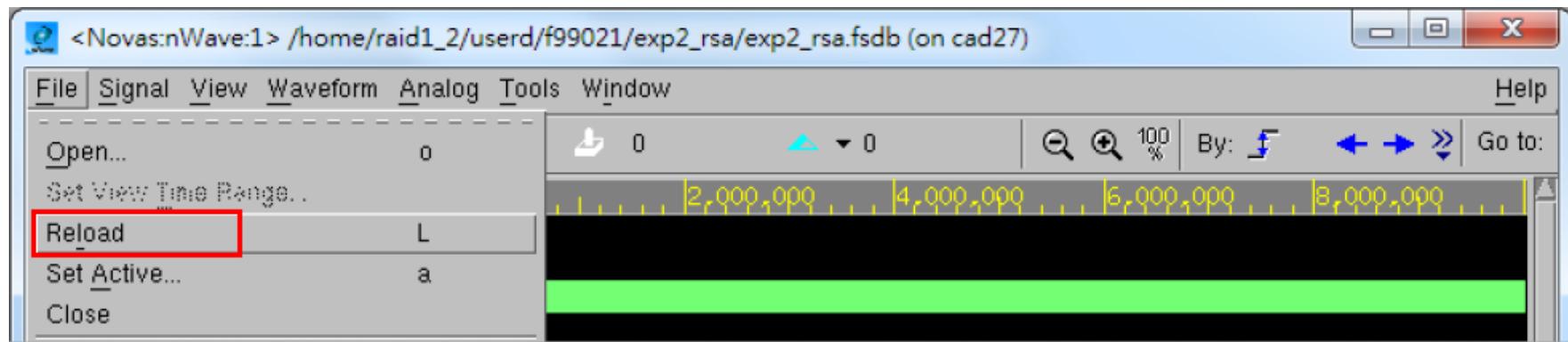
Change Signal Position





Reload the Waveform

- ❖ Remember to reload the waveform whenever finishing another Verilog simulation





Introduction to SpyGlass Lint

- ❖ The SpyGlass platform provides designers with insight about their design, early in the process at RTL
- ❖ SpyGlass Lint is a comprehensive HDL design rule checker
- ❖ We can use SpyGlass Lint to check the **coding style** of our design and if it is **synthesizable**



Start SpyGalss

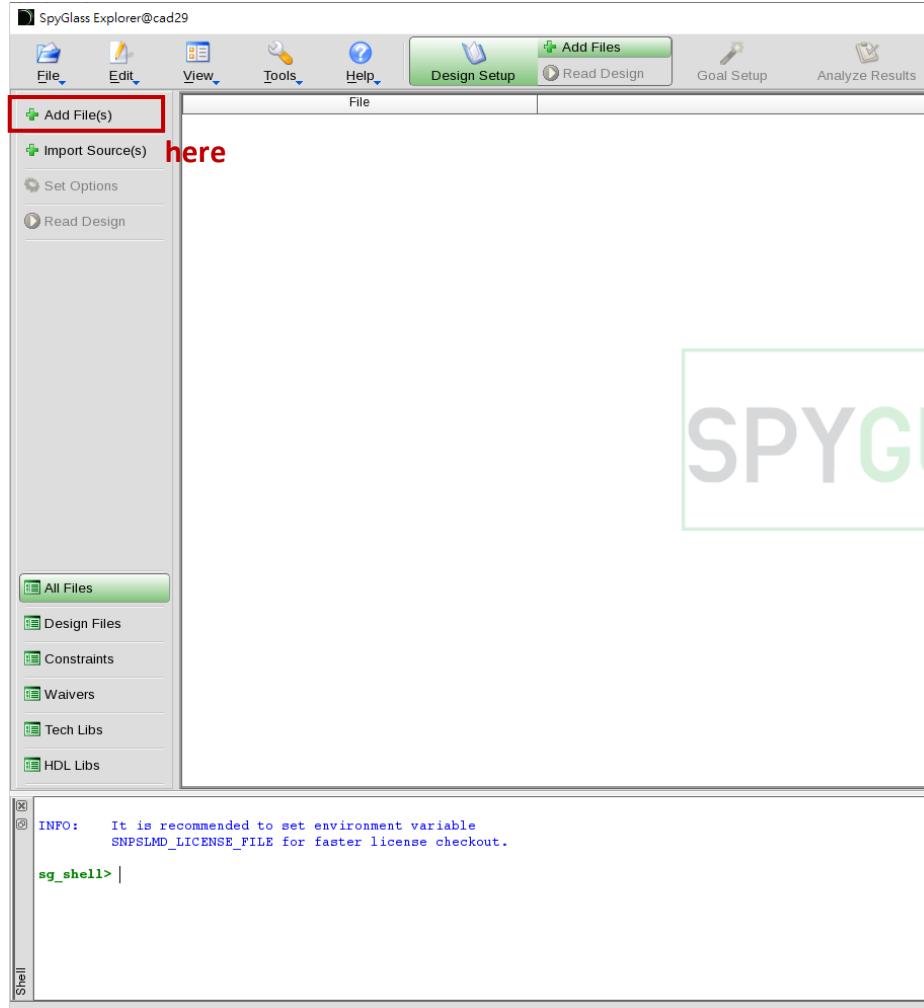
- ❖ Type the following command

```
spyglass &
```

- ❖ The token “&” enable you to use the terminal while Verdi is running in the background.



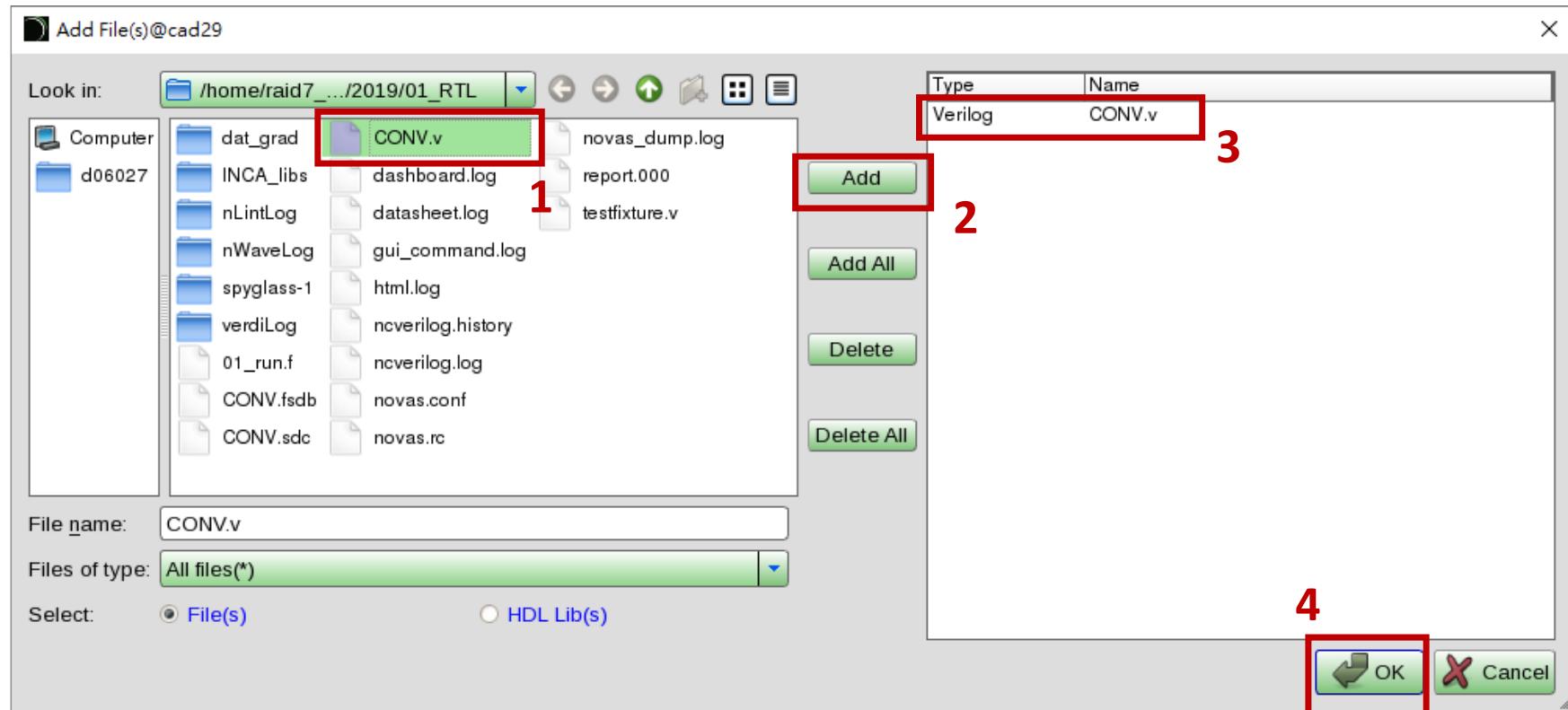
Specify the Design File



SPYGL



Specify the Design File





Specify Top Module Name

The screenshot shows the SpyGlass Explorer software interface. The title bar reads "SpyGlass Explorer: spyglass-1.prj@cad29". The menu bar includes File, Edit, View, Tools, Help, Design Setup (highlighted in green), Read Design, Goal Setup, and Analyze Results. On the left, there's a sidebar with buttons for Add File(s), Import Source(s), Set Options (highlighted with a red box), and Read Design. The main pane shows a file tree under "Design Files" with a single item "CONV.v" selected, indicated by a yellow highlight. To the right, the word "verilog" is displayed. A red box highlights the "Set Options" button in the sidebar, with the word "here" written in red next to it. In the bottom right corner, there is a large watermark-like text "SPYGLASS".



Specify Top Module Name

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Add Files Read Design Goal Setup Analyze Results

Add File(s) Import Source(s) Set Options Read Design

Advanced Options

Option	Value
Top Level Design Unit	CONV
Stop Design Unit(s)	<input type="checkbox"/>
Ignore Design Unit(s)	<input type="checkbox"/>
Diveable Block Abstracted Design Unit(s)	<input type="checkbox"/>
Interpret Pragma(s)	<input type="checkbox"/>
Ignore VHDL code within pragma block 'translate'	<input type="checkbox"/>
Ignore VHDL code within pragma block 'synthesis'	<input type="checkbox"/>
Enter Macros for Analysis	<input type="checkbox"/>
Set HDL Parameter(s) Value	<input type="checkbox"/>
Searches the specified paths for include files	<input type="checkbox"/>
Specify the library files in the source design	<input type="checkbox"/>
Specify the library directories containing libraries	<input type="checkbox"/>
Specify library file extensions	<input type="checkbox"/>
Enable System Verilog Processing	<input type="checkbox"/>
Enable auto-compilation of gateslib into sglib	<input type="checkbox"/>
Allow Duplicate Module Names in Verilog Designs	<input type="checkbox"/>
Disable Verilog 2k Processing	<input type="checkbox"/>
Run in VHDL87 Compatibility Mode	<input type="checkbox"/>
Automatically Sort VHDL File(s)	<input type="checkbox"/>



Read Design

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Add Files Read Design Goal Setup Analyze Results

Add File(s) Import Source(s) Set Options Read Design

Advanced Options

Option	Value
Top Level Design Unit	CONV
Stop Design Unit(s)	
Ignore Design Unit(s)	
Diveable Block Abstracted Design Unit(s)	
Interpret Pragma(s)	
Ignore VHDL code within pragma block 'translate'	<input type="checkbox"/>
Ignore VHDL code within pragma block 'synthesis'	<input type="checkbox"/>
Enter Macros for Analysis	
Set HDL Parameter(s) Value	
Searches the specified paths for include files	
Specify the library files in the source design	
Specify the library directories containing libraries	
Specify library file extensions	
Enable System Verilog Processing	<input type="checkbox"/>
Enable auto-compilation of gateslib into sglib	<input type="checkbox"/>
Allow Duplicate Module Names in Verilog Designs	<input type="checkbox"/>
Disable Verilog 2k Processing	<input type="checkbox"/>
Run in VHDL87 Compatibility Mode	<input type="checkbox"/>
Automatically Sort VHDL File(s)	



Read Design

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Add Files Read Design Goal Setup Analyze Results

Add File(s) Import Source(s) Set Options Read Design

Advanced Options

Option	Value
Top Level Design Unit	CONV
Stop Design Unit(s)	
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Diveable Block Abstracted Design Unit(s)	
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Ignore VHDL code within pragma block 'synthesis'	<input type="checkbox"/>
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Specify the library files in the source design	
Specify the library directories containing libraries	
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Enable System Verilog Processing	<input type="checkbox"/>
Enable auto-compilation of gateslib into sglib	<input type="checkbox"/>
Allow Duplicate Module Names in Verilog Designs	<input type="checkbox"/>
Disable Verilog 2k Processing	<input type="checkbox"/>
Run in VHDL87 Compatibility Mode	<input type="checkbox"/>
Automatically Sort VHDL File(s)	



Read Design

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Add Files Read Design Goal Setup Analyze Results

Run Design Read Synthesize Netlist Incremental Mode

Click on the 'Run Design Read' button to start the design read.
After the design read is completed, review the results and resolve critical design issues.
The results are displayed as list of messages that can be selected to show additional debug information and features.



Goal Setup

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Goal Setup Select Analyze Results

Run Goal(s): 1/49 1

Methodology : GuideWare Reference Methodology for rtl_handoff stage of New RTL Block development

Goal	Run Status
GuideWare/latest/block/rtl_handoff	Run Complete (F:0, E:3,...)
lint	Not Run Yet
lint_rtl	2
lint_turbo_rtl	Not Run Yet
lint_functional_rtl	Not Run Yet
lint_abstract	Not Run Yet
adv_lint	
constraints	
txv_verification	
cdc	
rdc	
dft	
power	
power_verification	
physical	
physical_aware_power	
rtl2netlist	
connectivity_verify	

1: Goal Setup button
2: Selected goal in the tree view
3: Run Goal(s) button



Message Window

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help Design Setup Goal Setup Analyze Results Reports

Run Goal: lint/lint_rtl Incremental Mode MS IS Waiver Design

Instance CONV

```
1  `timescale 1ns/10ps
2
3  module CONV(
4      input    clk,
5      input    reset,
6      output   reg busy,
7      input    ready,
8
9      output   reg [11:0] iaddr,
10     input   [19:0] idata,
11
12     output   cwr,
13     output   [11:0] caddr_wr,
14     output   reg [19:0] cdata_wr,
15
16     output   crd,
17     output   reg [11:0] caddr_rd,
18     input   [19:0] cdata_rd,
19
20     output   [2:0] csel
21 );
22
23
24 //*****
25 // Parameters
26 //*****
27
28
29 //*****
30
```

CONV.v

Instances Modules Instances Files Constraints

Group By: Goal by Rule Message File Line

Violations

Message Tree (Total: 9, Displayed: 9, Waived: 0)

- Design Read (2)
- lint.lint.rtl (7)
 - W123 (2) : A signal or variable has been read but is not set
 - UndrivenInTerm-ML (1) : Undriven but loaded input terminal of an instance detected
 - W528 (4) : A signal or variable is set but never read

Not all the warnings or errors are valuable

Shell Violations Waiver Tree



Text Editors

- ❖ In terminal
 - gedit, vi, vim
- ❖ Sublime Text
- ❖ Visual Studio Code



Vim

- ❖ Base on vi editor, which is native support by Linux
- ❖ A basic understanding to vim command would be helpful
 - Minor change to file on work station
 - Read text files on work station
- ❖ Two modes: edit & normal
 - Key “i” to switch to edit and “Esc” to switch to normal
 - Edit file in edit mode





Sublime Text

- ❖ Sublime Text is a sophisticated text editor for code, markup and prose. You'll love the slick user interface, extraordinary features and amazing performance.

A composite image showing the Sublime Text website and a screenshot of the Sublime Text application. The website header includes 'Sublime Text', 'Download', 'Buy', 'Support', 'News', and 'Forum'. The main text area says 'A sophisticated text editor for code, markup and prose'. It features a 'DOWNLOAD FOR WINDOWS' button, a link to 'Sublime Text 3 (Build 3207)', and a 'Changelog' link. To the right is a small window titled 'Introducing our Git client Sublime Merge' showing its interface. Below the website is a screenshot of the Sublime Text application window, displaying a file tree on the left with folders like 'tensorflow', 'third_party', 'tools', 'util', '.gitignore', 'ACKNOWLEDGMENTS', 'ADOPTERS.md', 'AUTHORS', 'BUILD', 'CODEOWNERS', 'configure', 'CONTRIBUTING.md', 'ISSUE_TEMPLATE.md', 'LICENSE', 'models.BUILD', and 'README.md'. The main workspace is empty. To the right of the application window is a large orange 'S' logo on a dark background.



Visual Studio Code

The screenshot shows the official Visual Studio Code website and a running instance of the VS Code editor.

Website Header:

- Visual Studio Code logo
- Docs, Updates, Blog, API, Extensions, FAQ links
- Search Docs input field
- Download button

Text on Website:

- Version 1.38 is now available! Read about the new features and fixes from August.
- Code editing. Redefined.
- Free. Built on open source. Runs everywhere.
- Download for Windows (Stable Build), Other platforms and Insiders Edition buttons
- By using VS Code, you agree to its license and privacy statement.

Running Instance (Editor View):

- Extensions Marketplace sidebar (highlighted in yellow) showing Python, GitLens, C/C++, ESLint, Debugger for Chrome, Language Support, vscode-icons, Vetur, and C# extensions.
- Main editor area showing code for serviceWorker.js, index.js, and serviceWorker.js.
- Terminal panel at the bottom showing the command to run the application.



Extension

Terminal



References

- [1] “MobaXterm User Manual” by The Centre for eResearch , University of Auckland
- [2] “VCS®/VCSI™ User Guide” by Synopsys
- [3] “Quick Start: an nLint Tutorial” by NOVAS