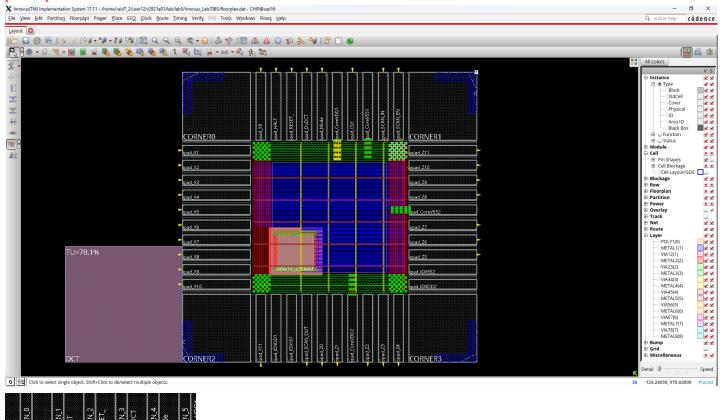
CVSD Lab6

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1. Take a screenshot after powerplan (IO filler is added) and show verification results of DRC and connectivity.

powerplan:



IOFILLER, N.J. pad, ZG. IOFILLER, N.J. IOFILLER, N.

(IO filler is added)

```
VERIFY DRC .... Sub-Area : 31 complete 0 Viols.

VERIFY DRC .... Sub-Area : {179.520 884.000 359.040 1051.240} 32 of 36

VERIFY DRC .... Sub-Area : 32 complete 0 Viols.

VERIFY DRC .... Sub-Area : 33 complete 0 Viols.

VERIFY DRC ... Sub-Area : 33 complete 0 Viols.

VERIFY DRC ... Sub-Area : 33 complete 0 Viols.

VERIFY DRC ... Sub-Area : 34 complete 0 Viols.

VERIFY DRC ... Sub-Area : 34 complete 0 Viols.

VERIFY DRC ... Sub-Area : 34 complete 0 Viols.

VERIFY DRC ... Sub-Area : 37 complete 0 Viols.

VERIFY DRC ... Sub-Area : 36 complete 0 Viols.

VERIFY DRC ... Sub-Area : 35 complete 0 Viols.

VERIFY DRC ... Sub-Area : 35 complete 0 Viols.

VERIFY DRC ... Sub-Area : 35 complete 0 Viols.

VERIFY DRC ... Sub-Area : 36 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 2.0M) ***
```

(results of DRC)

```
******* Start: VERIFY CONNECTIVITY ******
Start Time: Tue Nov 21 17:11:23 2023

Design Name: CHIP
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1066.6400, 1051.2400)

Error Limit = 1000; Warning Limit = 50
Check specified nets
*** Checking Net VDD
*** Checking Net VSS

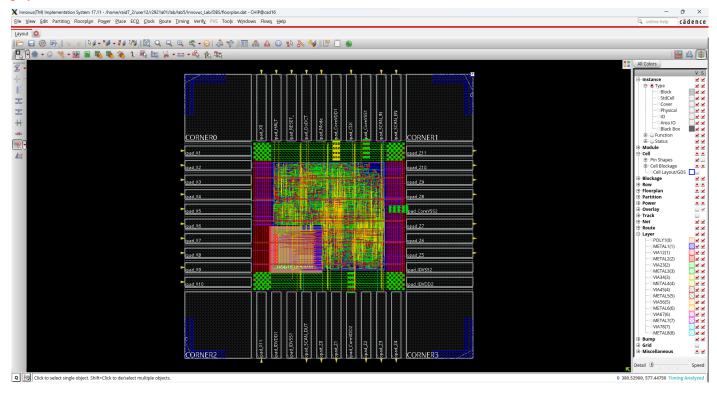
Begin Summary
Found no problems or warnings.
End Summary
End Time: Tue Nov 21 17:11:23 2023
Time Elapsed: 0:00:00.0

********* End: VERIFY CONNECTIVITY *******
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)
```

(results of connectivity)

2. Take a screenshot after placement (physical view) and show pre-cts setup time analysis report (ensure the slack of setup time ≥ 0 and no DRVs)

physical view:



pre-cts setup time analysis report:

