Midterm1-2021 Solution

1) The seven great ideas in computer architecture are similar to ideas from other fields. Match the four ideas from computer architecture.

Solution:

Assembly lines in automobile manufacturing	-> Performance via Pipelining
Suspension bridge cables.	-> Dependability via Redundancy
Express elevators in buildings	-> Make the Common Case Fast
Library reserve desk	-> Hierarchy of Memories

2)
Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5s.

a) (1 point) Find the average CPI for each program, given that the processor has a clock cycle time of 2ns.

Solution:
CPI=Texec*f/Nbinst
f=1/2ns = 0.5*10^9
Compiler A CPI=1.1*0.5*10^9/1*10^9 = 0.55
Compiler B CPI=1.5*0.5*10^9/1.2*10^9 = 0.6255

b) (1 point) Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

Solution:
fb/fa = (1.2E9*0.6255)/(1.0E9*0.55) = 1.36

3)
Some microprocessors are designed to have adjustable voltage, and reduction in voltage may cause a reduction in frequency. What is a power reduction if voltage is reduced by 14% and frequency is reduced by 12.5%.

Solution:
P=1/2*V^2*f*C
Vnew = 0.86Vold, fnew=0.875fold
Pnew=(1/2)*Vnew^2*fnew*C = 1/2*(Vold*0.86)^2*fold*0.875*C
Pold=(1/2)*Vold^2*fold*C
Pnew/Pold=0.86^2*0.875=0.6471

4)
The table below shows some machine code of RISC-V RV32I in memory

Address	+0	+1	+2	+3
0x00000018	00	00	00	00
0x00000014	00	00	00	00
0x00000010	00	00	00	00
0x0000000c	00	00	00	00
0x00000008	13	05	32	00
0x00000004	33	05	52	00
0x00000000	93	42	43	00

Translate machine code at address 0x00000000 into assembly instruction. You need to use RISK V Instruction Set Manual to identify each component of the instruction like "opcode", "rd"...etc.
Solution:
RISC-V is little endian so the instruction at memory 0x00000000
is:
0x00434293
in binary
0000 0000 0100 0011 0100 0010 1001 0011
where
opcode = 0010011
rd = 0010 1 (x5)
func3 = 100
rs1 = 00110 (x6)
imm[11:0] = 0000 0000 0100 (4)
that is
`XORI x5, X6, 4`

5)
Translate C code into RISC-V RV32I base integer instructions assembly language.

r = A[n]*2 + B[n-1]

Where x11 is a pointer to base address of array A, x12 is a pointer to base address of array B, and "n" is the value in register x13, and "r" register x10.

Please comment each line of your code.

Solution:

```
slli      x13, x13, 2     # x13 = x13*4
add       x11, x11, x13   # x11 = &A[n]
lw        x10, 0(x11)     # x10 = A[n]
slli      x10, x10, 1     # x10 = x10*2 = A[n]*2
addi      x13, x13,-4     # x13 = x13-4
add       x12, x12, x13   # x12 = &B[n-1]
lw        x5,  0(x12)     # x5  = B[n-1]
add       x10, x10, x5    # x10 = x5 + x10 = A[n]*2 +  B[n-1]
```

6)
x12 is RV32I register. Assume x12 =-6
a) (1 mark)
What is the hexadecimal representation of x12?
b) (1 mark)
Assume we execute the following instruction

```
srai x12,x12,1
```

what is now the value of x12 in hexadecimal and decimal?

Solution:
a)
x12 = 0xfffffffa
b)
After
srai x12,x12,1
x12 = 0xfffffffd
0xfffffffd = -0x80000000 + 0x7ffffffd
= - 2147483648 + 2147483645
= -3