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COMP SCI 2GA3
Sheet 1 — 2018-09-07
Solution Hints

Computer Architecture

Exercise 1.1

Consider two different implementations, M_1 and M_2, of the same instruction set. There are four classes (A, B, C and D) of instructions in the instruction set.

M_1 has a clock rate of 2500 MHz, and M_2 has a clock rate of 3000 MHz. The average number of cycles for each instruction class on the two machines are as follows:

Instruction Class	**CPI on M_1**	**CPI on M_2**
A	3	4
B	4	4
C	6	7
D	9	10

(a) If the number of instructions executed in a certain program is divided equally among the classes of instructions in Exercise 1, what is the speedup of M_2 over M_1?

Solution Hints: Find the CPI of each machine first. CPI for M_1 is 5.5; CPI for M_2 is 6.25

CPU time for M_1 is $\frac{\text{InstructionCount}\cdot 5.5}{2500 MHz}$

CPU time for M_2 is $\frac{\text{InstructionCount}\cdot 6.25}{3000 MHz}$

M_2 has a smaller execution time; the speedup is the inverse ratio of the execution times, or $\frac{5.5\cdot 3000}{6.25\cdot 2500} =$ 1.056.

(b) Assuming the instruction distribution from (a), at what clock rate would M_1 have the same performance as the 3000 MHz version of M_2?

Solution Hints: M_1 would be as fast if the clock rate were 1.056 higher.

$2500 MHz \cdot 1.056 = 2640 MHz$ — slightly overclocking could perhaps do it...

Exercise 1.2

We are interested in two implementations of a machine, one with and one without special floating-point hardware.

- Machine M_{FP} (Machine with Floating Point) has floating-point hardware and can therefore implement the floating-point operations directly.
- Machine M_{NFP} (Machine with No Floating Point) has no floating-point hardware and so must emulate the floating-point operations using integer instructions. (The integer instructions all take 4 clock cycles.)

We consider a program P, containing a mix of operations as indicated in the following table, which also lists the number of *clock cycles* required by for each instruction class on M_{FP}, and the *number of integer instructions* needed on M_{NFP} to implement each of the floating-point operations:

Instruction Class	**Frequency in P**	**CPI on M_{FP}**	**# of integer instr. on M_{NFP}**
floating-point add	20%	6	16
floating-point multiply	15%	8	28
floating-point divide	5%	24	52
integer instructions	60%	4	

Both machines have a clock rate of 1000 MHz.

(a) Find the native MIPS ratings for execution of program P on both machines.

Solution Hints: MIPS $= \frac{\mathit{Clockrate}}{\mathit{CPI} \cdot 10^6}$

CPI for M_{FP} is $0.2 \cdot 6 + 0.15 \cdot 8 + 0.05 \cdot 24 + 0.6 \cdot 4 = 6$

CPI for M_{NFP} is 4

MIPS for $M_{\mathrm{FP}} = \frac{1000}{6} = 166.\overline{6}$

MIPS for $M_{\mathrm{NFP}} = \frac{1000}{4} = 250$

(b) If the machine M_{FP} needs 240 millon instructions for program P, how many integer instructions does the machine M_{NFP} require for the same program?

Solution Hints:

Instruction Class	Frequency on M_{FP}	Count on M_{FP} in millions	Instruction Count on M_{NFP} in millions
Floating point add	20%	48	768
Floating point multiply	15%	36	1008
Floating point divide	5%	12	624
Integer Instructions	60%	144	144
Totals:	100%	240	2544

(c) Assuming the instruction counts from (b), what is the execution time (in seconds) for the program P run on M_{FP} respectively M_{NFP}?

Solution Hints: Execution time $= \frac{\mathit{InstructionCount} \cdot 10^6}{\mathit{MIPS}}$

M_{FP} execution time is $\frac{240}{166.\overline{6}} = 1.44s$

M_{NFP} execution time is $\frac{2544}{250} = 10.176s$

Exercise 1.3

You are the lead designer of a new processor. The processor design and compiler are complete, and now you must decide whether to produce the current design as it stands or spend additional time to improve it. You discuss this problem with your hardware engineering team and arrive at the following options:

- *Leave the design as it stands.* Call this base machine M_{base}. It has a clock rate of 2800 MHz.
- *Optimize the hardware.* The hardware team claims that it can improve the processor design to give it a clock rate of 3200 MHz. Call this machine M_{opt}.

The following table shows the frequency of instructions of the different classes in the test suite used for evaluating the designs, and the CPI values for both machines:

Instruction class	**Frequency**	**CPI on M_{base}**	**CPI on M_{opt}**
A	40%	3	3
B	25%	4	3
C	20%	4	4
D	15%	6	5

(a) What is the CPI for each machine?

Solution Hints: CPI for M_{base}: $3 \cdot 0.4 + 4 \cdot 0.25 + 4 \cdot 0.2 + 6 \cdot 0.15 = 3.9$

CPI for M_{opt}: $3 \cdot 0.4 + 3 \cdot 0.25 + 4 \cdot 0.2 + 5 \cdot 0.15 = 3.5$

(b) What are the native MIPS ratings for M_{base} and M_{opt}?

Solution Hints: MIPS for M_{base}: $\frac{2800}{3.9} = 717.95$

MIPS for M_{opt}: $\frac{3200}{3.5} = 914.29$

(c) What is the speedup of M_{opt} over M_{base}?

Solution Hints: Since they have the same architecture, we can compare native MIPS ratings. The speedup of M_{opt} is the ratio $\frac{914.29}{717.95} = 1.27$, that is, it is 27% faster.

(d) The compiler team has heard about the discussion to enhance the machine discussed in (a)–(c). The compiler team proposes to improve the compiler for the machine to further enhance performance. Call this combination of the improved compiler and the base machine M_{comp}. The instruction improvements from this enhanced compiler have been estimated as follows:

Instruction class	Percentage of instructions executed vs. base machine
A	90%
B	90%
C	85%
D	95%

For example, if the base machine executed 500 class A instructions, M_{comp} would execute $0.9 \cdot 500 = 450$ class A instructions for the same program.

What is the CPI for M_{comp}?

Solution Hints: Ratio of instructions: $0.9 \cdot 0.4 + 0.9 \cdot 0.25 + 0.85 \cdot 0.2 + 0.15 \cdot 0.95 = 0.8975$

$\text{CPI} = \frac{3 \cdot 0.4 \cdot 0.9 + 4 \cdot 0.25 \cdot 0.9 + 4 \cdot 0.20 \cdot 0.85 + 6 \cdot 0.1 \cdot 0.95}{0.8975} = 3.9164$

(e) What is the speedup of M_{comp} over M_{base}?

Solution Hints: M_{base} CPU $= \frac{IC \cdot 3.9}{Clockrate}$

M_{comp} CPU $= \frac{0.8975 \cdot IC \cdot 3.9164}{Clockrate}$

$\text{Ratio} = \frac{M_{\text{base}}\ \text{CPU}}{M_{\text{comp}}\ \text{CPU}} = \frac{3.9}{0.8975 \cdot 3.9164} \approx 1.10953$

The speedup is about 1.11, that is, M_{comp} is 11% faster than M_{base}.

(f) The compiler group points out that it is possible to implement both the hardware improvements of (a) and compiler enhancements described in (d). If *both* the hardware and compiler improvements are implemented, yielding machine M_{both}, how much faster is M_{both} than M_{base}?

Solution Hints: M_{both} CPI $= \frac{3 \cdot 0.4 \cdot 0.9 + 3 \cdot 0.25 \cdot 0.9 + 4 \cdot 0.2 \cdot 0.85 + 5 \cdot 0.15 \cdot 0.95}{0.8925} = 3.51$

$$\frac{\text{Performance } M_{\text{both}}}{\text{Performance } M_{\text{base}}} = \frac{\frac{IC \cdot 3.9}{\text{Clock rate } M_{\text{base}}}}{\frac{IC \cdot 0.8925 \cdot 3.51}{\text{Clock rate } M_{\text{both}}}} = \frac{\frac{3.9}{2800 MHz}}{\frac{3.15}{3200 MHz}} \approx 1.4150$$

(g) You must decide whether to incorporate the hardware enhancements suggested in (a) or the compiler enhancements of (d) (or both) to the base machine. You estimate that the following time would be required to implement these optimizations:

Optimization	Time to implement	Machine name
Compiler	4 months	M_{comp}
Hardware	6 months	M_{opt}
Both	8 months	M_{both}

Assuming that CPU performance improves by approximately 50% per year, or about 3.4% per month. and also assuming that the base machine has performance equal to that of its competitors, which optimizations (if any) would you choose to implement? **Solution Hints:** Compute the performance growth after 4, 6, and 8 months:

- after 4 months: $1.034^4 = 1.14$
- after 6 months: $1.034^6 = 1.22$
- after 8 months: $1.034^8 = 1.31$

The best choice is to implement either M_{both} or M_{opt}.