COMPSCI 2GA3 Fall, 2021

Assignment/Homework 3, Oct. 30th 2021
Assignment due date: Nov. 14th, 23:59:59.
Note: Please work on this assignment individually. Students copying each other's answer will get a zero and will perform poor on midterm and final.

Written Exercises

Complete the following questions from *Computer Organization and Design: The Hardware Software Interface: Computer Organization and Design The Hardware/Software Interface: RISC-V Edition*

Chapter 3: Arithmetic for Computers

1. (4 Marks) IEEE 754-2008 contains a half precision that is only 16 bits wide. The leftmost bit is still the sign bit, the exponent is 5 bits wide and has a bias of 15, and the mantissa is 10 bits long. A hidden 1 is assumed. Calculate

$$3.984375 \times 10^{-1} + (3.4375 \times 10^{-1} + 1.771 \times 10^{3})$$

by hand, assuming each of the values is stored in the 16-bit half precision format. Assume 1 guard, 1 round bit, and 1 sticky bit, and round to the nearest even. Show all the steps, and write your answer in both the 16-bit floating point format and in decimal.

Solution:

3.33 $3.984375 \times 10^{-1} + (3.4375 \times 10^{-1} + 1.771 \times 10^{3})$

$3.984375 \times 10^{-1} = 1.1001100000 \times 2^{-2}$

$3.4375 \times 10^{-1} = 1.0110000000 \times 2^{-2}$

$1.771 \times 10^{3} = 1771 = 1.1011101011 \times 2^{10}$

shift binary point of smaller left 12 so exponents match

```
(B)         .0000000000 01 0110000000 Guard = 0,
                           Round = 1, Sticky = 1
(C)       +1.1011101011
          -------------
(B+C)     +1.1011101011
```

```
(A)        .0000000000  011001100000
          --------------
A + (B + C) + 1.1011101011 No round
A + (B + C) + 1.1011101011 × 2^10 = 0110101011101011 = 1771
```

2. Exercise 3.41-3.4.2 (4 Marks)

   (a) Using the IEEE 754 floating point format, write down the bit pattern that would represent -1/4. Can you represent -1/4 exactly?

   (b) What do you get if you add -1/4 to itself four times? What is -1/4 $\times$ 4? Are they the same?

Solution:

3.41

Answer	sign	exp	Exact?
1 01111101 00000000000000000000000	-	−2	Yes

3.42 b+b+b+b = −1

b × 4 = −1

They are the same

Chapter 4: The Processor

3. Exercise 4.7.1-6 (8 Marks) Problems in this exercise assume that the logic blocks used to implement a processor's datapath have the following latencies:

I-Mem / D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Sign extend	Control
250 ps	150 ps	25 ps	200 ps	150 ps	5 ps	30 ps	20 ps	50 ps	50 ps

"Register read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

4.7.1: What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)?

4.7.2: What is the latency of `ld` ?

4.7.3: What is the latency of `sd`?

4.7.4: What is the latency of `beq`?

4.7.5: What is the latency of an I-type instruction?

4.7.6: What is the minimum clock period for this CPU?

Solution:

4.7.1 R-type : $30 + 250 + 150 + 25 + 200 + 25 + 20 = 700$ps

4.7.2 ld : $30 + 250 + 150 + 25 + 200 + 250 + 25 + 20 = 950$ps (We can also accept as correct 925, if the assumption that lead to this result is correct)

4.7.3 sd : $30 + 250 + 150 + 200 + 25 + 250 = 905$ps

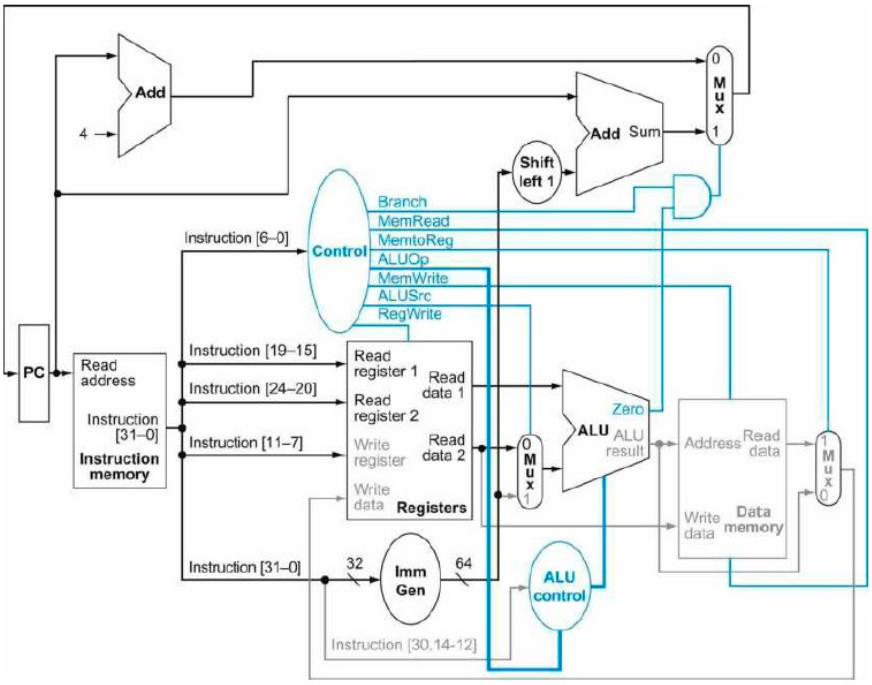
4.7.4 beq : $30 + 250 + 150 + 25 + 200 + 5 + 25 + 20 = 705$ps

4.7.5 I-type : $30 + 250 + 150 + 25 + 200 + 25 + 20 = 700$ps

4.7.6 950ps

4. Exercise 4.8 (4 Marks)

Suppose you could build a CPU where the clock cycle time was different for each instruction. What would the speedup of this new CPU be over the CPU presented in below (Figure 4.21).



given the instruction mix below? (Hint: Use the results from Problem 4.7)

R-type/I-type (non-ld)	ld	sd	beq
52%	25%	11%	12%

Solution:
Using the results from Problem 4.7, we see that the average time per instruction is
.52*700 + .25*950 + .11*905 + .12 * 705 = 785.6ps
In contrast, a single-cycle CPU with a *normal* clock would require a clock cycle time of 950.
Thus, the speedup would be 950/787.6 = 1.206 (We also accept as correct 925/787.6 = 1.174)