N.B. Assignments are individual work, due as pdf format. Submit through avenue, by 18th November at 11:59 PM. Your assignment should contain you name and student number and the name of the file should follow the naming convention, i.e., fistname_lastname_studentNumber.pdf.

Assignment Question 1 (2 + 2 + 4 + 2 + 4 Marks):

Consider the following sequence of instructions, and assume that it is executed on a 5-stage pipeline datapath:

```
add  r5, r2, r1
lw  r3, 4(r5)
lw  r2, 0(r2)
or  r3, r5, r3
sw  r3, 0(r5)
```

a) If there is no forwarding or hazard detection, insert **nops** to ensure correct execution.
b) Repeat **question a** but now use **nops** only when a hazard cannot be avoided by changing or rearranging these instructions. You can assume register r7 can be used to hold temporary values in your modified code.
c) If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units in Figure 4.60.
d) If there is no forwarding, what new inputs and output signals do we need for the hazard detection unit in Figure 4.60? Using this instruction sequence as an example, explain why each signal is needed.
e) For the new hazard detection unit from **question d**, specify which output signals it asserts in each of the first five cycles during the execution of this code.

Assignment Question 2 (4 + 2 + 4 Marks):

Consider Figure 4.17 (Simple datapath with Control unit). It has two control units, the main control and the ALU control. The input to the main control is the 6-bit OpCode field form the instruction. The output consists of several 1-bit and one 2-bit signals. The input to the ALU control is the 2-bit output (ALUOp) form the main control. This ALUOp along with the 6-bit function field from the instruction (if exist) identifies the **operation control** of the ALU.

1. For the following instructions identify the output bits that required to set (1) and does not require to set (0).
2. Also identify the operation controls.
3. Which resources (blocks) perform a useful function for this instruction?
4. The instruction set for the above two questions are: add, sub, AND, OR, beg, j, lw, sw

Assignment Question 3 (2 + 2 + 6 Marks):

Assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

alu	beq	lw	sw
45%	20%	20%	15%

a) What is the clock cycle time in a pipelined and non-pipelined processor?
b) What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
c) Instead of a single-cycle organization, we can use a multi-cycle

organization where each instruction takes multiple cycles but one instruction finishes before another is fetched. In this organization, an instruction only goes through stages it actually needs (e.g., ST only takes 4 cycles because it does not need the WB stage). Compare clock cycle times and execution times with singlecycle, multi-cycle, and pipelined organization.