Tutorial 7
Chapter 8 – Main Memory – Part 2 And virtual Memory part I
Operating Systems CS 3SH3 Term 2, Winter 2022
Prof. Neerja Mhaskar

Tutorials are not mandatory. They are simply a tool for you to understand the course concepts better.

Tutorial Format: The questions will be posted a day before or on the day of the tutorial on the course website. You can choose to solve these problems before hand and come in with your solutions. I or one of the TAs helping me will check your solutions. If you have all of the questions correct you can choose to leave. If you have any of them incorrect, it is recommended that you stay and understand the solutions.

Solutions to the tutorial will not be posted online.

1. The BTV operating system has a 21-bit virtual address, yet on certain embedded devices, it has only a 16-bit physical address. It also has a 2-KB page size. How many entries are there in each of the following?
    a. A conventional, single-level page table.
    b. An inverted page table.

2. What is the maximum amount of physical memory in the BTV operating system?

3. Consider a computer system with a 32-bit logical address and 4-KB page size. The system supports up to 512 MB of physical memory. How many entries are there in each of the following?
    a. A conventional single-level page table
    b. An inverted page tables

4. Consider a paging system with the page table stored in memory.
    a. If a memory reference takes 50 nanoseconds, how long does a paged memory reference take?
    b. If we add TLBs, and 75 percent of all page-table references are found in the TLBs, what is the effective memory reference time? (Assume that finding a page-table entry in the TLBs takes 2 nanoseconds, if the entry is present.)

5. Consider the hierarchical paging scheme used by the VAX architecture. How many memory operations are performed when a user program executes a memory-load operation?

6. Assume a program has just referenced an address in virtual memory. Describe a scenario how each of the following can occur: (If a scenario cannot occur, explain why.)
    a. TLB miss with no page fault

b. TLB miss and page fault
c. TLB hit and no page fault
d. TLB hit and page fault

7. Consider Hierarchical paging, with logical address space of 2^{48} bytes, page size = 1024 = 2^{10} bytes and each page table entry takes 8 bytes. A multi-level page table is used because each table must be contained within a page.
   a. How many levels of page table are required?
   b. What is the distribution of no. of bits to represent each level of the multi-level page table, and the page offset?

8. Consider the page table shown below for a system with 12-bit virtual and physical addresses and with 256-byte pages. The list of free page frames is D, E, F (that is, D is at the head of the list, E is second, and F is last). Convert the following virtual addresses to their equivalent physical addresses in hexadecimal. All numbers are given in hexadecimal. (A dash for a page frame indicates that the page is not in memory.)

Page	Page Frame
0	–
1	2
2	C
3	A
4	–
5	4
6	3
7	–
8	B
9	0

   a. 9EF
   b. 111
   c. 700
   d. 0FF

9. Consider the following page reference string:
   7, 2, 3, 1, 2, 5, 3, 4, 6, 7, 7, 1, 0, 5, 4, 6, 2, 3, 0, 1.

Assuming demand paging with three frames, how many page faults would occur for the FIFO replacement algorithm?