Midterm 2

Q1

Arithmetic for Computers. (Please show your calculation steps) Write down the binary and hexadecimal representation of the decimal number 21.125 assuming the IEEE 754 single precision format.

Answer:

$21.125 \times 10^0 = 10101.001 \times 2^0$

normalize, move binary point four to the left

1.0101001×2^4

sign = positive,

exp = 127+4 = 131

0 1000 0011 0101 0010 0000 0000 0000 000

= 0100 0001 1010 1001 0000 0000 0000 0000

= 0x41A90000

Q2

Assume 161, 214 and 91 are signed 8-bit decimal integers stored in two's complement format. Calculate

161 – 214 - 91

using saturating arithmetic. The result should be written in decimal.

Do we have any overflow or underflow?

Answer:

161 = 1010 0001 = -128 +32+1 = -95

214 = 1101 0110 = -128 +64+16+4+2 = -42

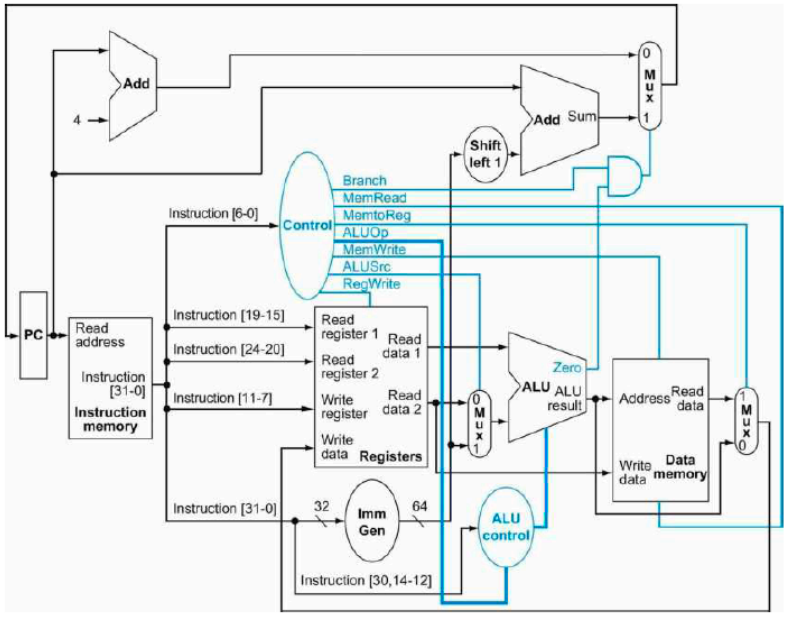
91 = 0101 1011 = 91

-95 – (-42) - 99 = -95 + 42 - 91 = -144

Overflow (result = −144, which does not fit into an signed 8-bit format)

Q3

In this exercise, we examine how an instruction is executed in a single-cycle data-path.



Assume x11 is initialized to 0x0000000B and x12 to 0x00000015
The processor fetches the instruction:

```
or x10, x11, x12
```

a) What are the values of the ALU control unit's inputs for this instruction?

Answer:

ALUOp=10

b) What is the output of ALU control unit

Answer:

0001

c) For MUX, at input to ALU show the values of its three inputs (two data inputs and selection input) during the execution of this instruction.

Answer:

Input 0 = x12 = 0x00000015
Input 1 = <undefined>
ALUSrc = 0

e) What are the input values for the ALU and the two Add units?

Answer:

ALU inputs: 0x0000000B and 0x00000015
PC + 4 adder inputs: PC and 4
Branch adder inputs: PC and <undefined>

f) What are the values of all inputs for the Registers unit?

Answer:

During IF step
Read register 1 = 01011 (11)
Read register 2 = 01100 (12)
Write register = 01010 (10)
Write data = <ignore>
Reg write = 0

During WB step
Read register 1 = 01011 (11)
Read register 2 = 01100 (12)
Write register = 01010 (10)
Write data = 0x0000001F (`X11 or X12`)
Reg write = 1

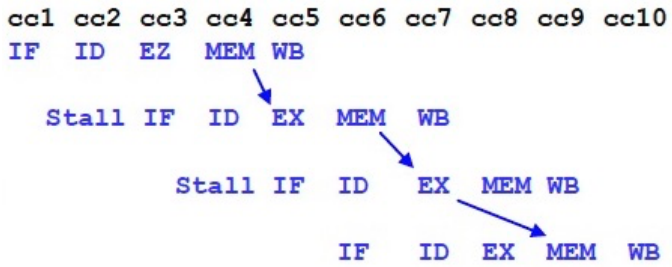
Q4

Assume the following RISC-V assembly code

```
i1   lw    x12,60(x11)
i2   lw    x11,40(x12)
i3   slt   x11,x11,x12
i4   sw    x11,20(x12)
```

a) Write in the form of textual representation stages of execution of instructions and indicate data hazards.
b) Calculate the pipeline CPI. Please show your calculation steps.

Answer:



a)
(i1,cc1)=IF(i1,cc2)=ID,(i1,cc3)=EX,(i1,cc4)=MEM->,(i1,cc5)=WB
(i2,cc3)=IF(i2,cc4)=ID,(i2,cc5)=->EX,(i2,cc6)=MEM->,(i2,cc7)=WB
(i3,cc5)=IF(i3,cc6)=ID,(i3,cc7)=->EX->,(i3,cc8)=MEM,(i3,cc9)=WB
(i4,cc6)=IF(i4,cc7)=ID,(i4,cc8)=EX,(i4,cc9)=->MEM,(i4,cc10)=WB

b)
In total there were 10 cycles, and 4 instructions. Thus, CPI = 10 / 4 = 2.5 cycles per instruction.