OS Concepts Overview

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Based on: "Operating Systems Concepts", 10th Edition Silberschatz Et al.

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Operating System

- No universally accepted definition
- Collection of programs that manages hardware resources
- A program that controls the execution of application programs
- An interface between applications and hardware

Convenience, efficiency, ability to evolve

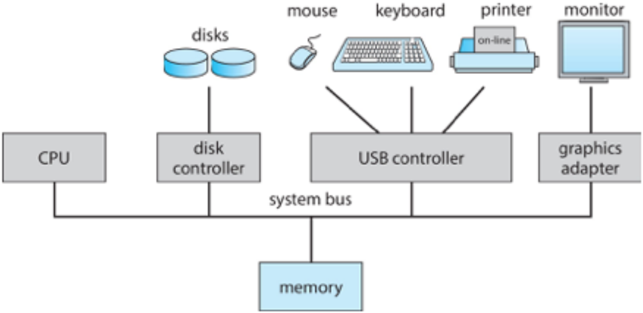
OS Definition

- Everything a vendor ships when you order an OS
- The one program running at all times on the computer is the kernel, part of the operating system
- A system program (`ls, rm, format,..`)
- An application program - not associated with OS (Word, Keynote, ..)
- Middleware - is computer software that provides services to software applications beyond those available from the operating system.

Computer-System Operation

- I/O devices and the CPU can execute in parallel
- Each device controller has a local buffer and is in charge of a particular device type
- Each device controller type has an operating system device driver to manage it
- CPU moves data from/to main memory to/from local buffers
- Device controller informs CPU that it has finished its operation by causing an interrupt

Computer System Organization



Device types?

Difference between controller and adapter?

How device controller informs CPU that it has finished its operation?

Key Aspects of the System

- Interrupts
- Storage structure
- I/O structure

Interrupts

- Interrupt transfers control to the interrupt service routine generally, through the interrupt vector, which contains the addresses of all the service routines
- Interrupt architecture must save the address of the interrupted instruction
- A trap or exception is a software-generated interrupt caused either by an error or a user request
- An operating system is interrupt driven!

I/O Interrupts

The interrupt handler signals the user process upon the completion of I/O.

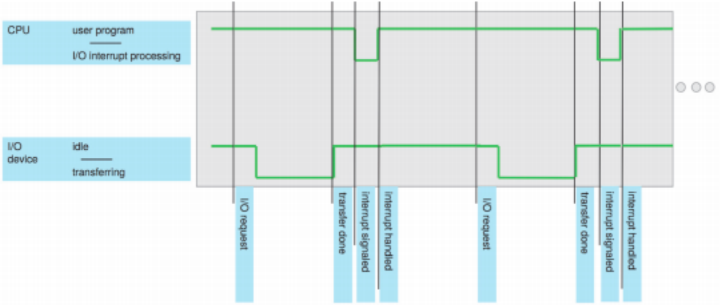
Synchronous

- The user process makes an I/O request and **waits** until the I/O completion.
- The user process must know the I/O latency, so it knows how long it should wait.

Asynchronous

- An I/O request returns **without waiting** for the I/O completion.
- Interrupt scheduled at the completion of I/O.
- The interrupt handler signals the user process when the I/O is done.
- Concurrent I/O operations on several devices.

Interrupt-Timeline



Called indirectly through the table of pointers

The addresses of the interrupt service routines for the various devices.

Interrupt Handling

The operating system preserves the state of the CPU by storing registers and the program counter system.

Determines which type of interrupt has occurred: polling or vectored interrupt system

Maskable (can be turned off by the CPU) and nonmaskable (reserved for events such as unrecoverable memory errors)

What is interrupt response time?

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What is interrupt response time? The time that elapses between the interrupt signal and the execution of the first statement in the corresponding interrupt handler.

Classes of Interrupts

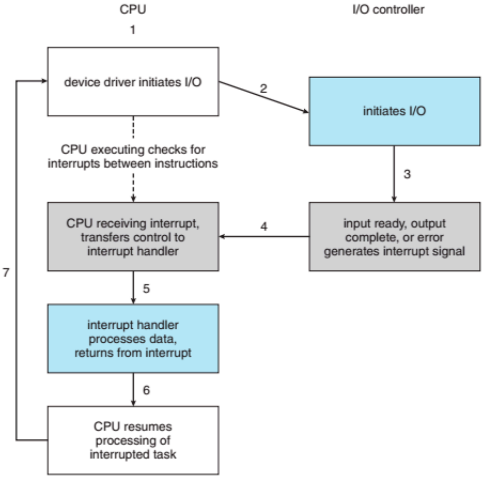
Program - Generated by: arithmetic overflow, division by zero, reference outside a user's allowed memory space, etc., (and other similar things)

Timer - Generated by a timer within the processor.

I/O - Generated by an I/O controller.

Hardware - Generated by power failure or memory parity error.

Interrupt-Driven I/O


CPU
I/O controller
1
device driver initiates I/O
2
initiates I/O
CPU executing checks for interrupts between instructions
3
4
CPU receiving interrupt, transfers control to interrupt handler
input ready, output complete, or error generates interrupt signal
7
5
interrupt handler processes data, returns from interrupt
6
CPU resumes processing of interrupted task

Multiple Interrupts

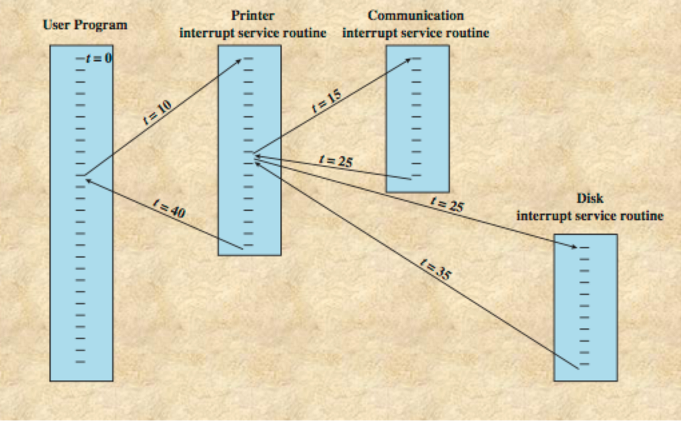

User Program
Printer interrupt service routine
Communication interrupt service routine
Disk interrupt service routine
t = 0
t = 10
t = 15
t = 25
t = 25
t = 35
t = 40

Figure: Transfer of Control With Multiple Interrupts

Storage Structure

Main memory

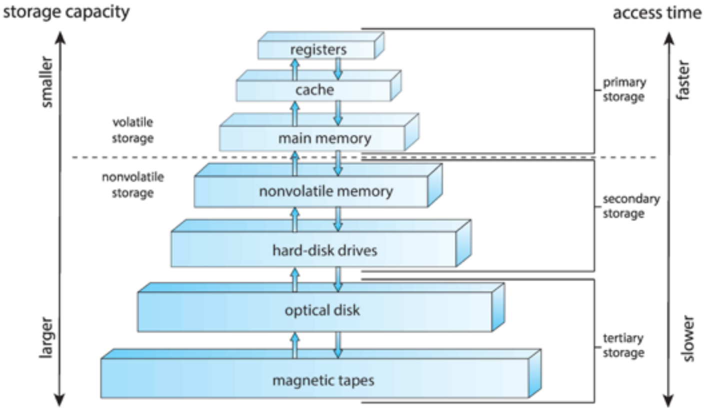
- Random access (DRAM, SRAM)

Secondary storage - extension of main memory that provides large nonvolatile storage capacity

- Hard Disk Drives (HDD)
- Non-volatile memory (NVM), i.e. SSD (solid-state drive) is a type of nonvolatile storage

The difference between non-volatile and volatile memory?

Storage Hierarchy



I/O Techniques

When the processor encounters an instruction relating to I/O, it executes that instruction by issuing a command to the appropriate I/O module

- Programmed I/O
- Interrupt Driven I/O
- Direct Memory Access (DMA)

Programmed I/O

1. The I/O module performs the requested action then sets the appropriate bits in the I/O status register.
2. The processor periodically checks the status of the I/O module until it determines the instruction is complete.

With programmed I/O the performance level of the entire system is severely degraded.

Interrupt-Driven I/O

1. Processor issues an I/O command to module.
2. I/O module will interrupt the processor service when it is ready to exchange data.
3. The processor executes the data transfer.

More efficient than programmed I/O, but still requires active intervention of the processor to transfer data between I/O module and memory.

Direct Memory Access (DMA)

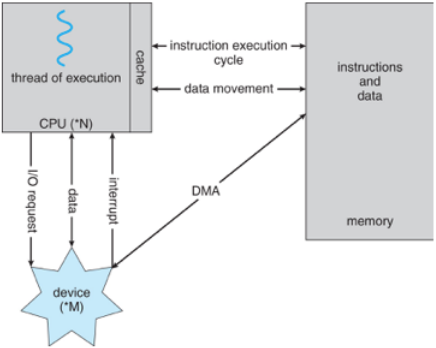
Performed by a separate module on the system bus or incorporated into an I/O module

Transfers the entire block of data directly to and from memory without going through the processor.

- Processor is involved only at the beginning and end of the transfer.
- Processor executes more slowly during a transfer when processor access to the bus is required.

More efficient than interrupt-driven or programmed I/O.

Modern Computer Architecture



Von Neumann architecture - one bus used for both data transfers and instruction fetches.

Harvard architecture - separate data and instruction busses.

Computer-System Architecture

Single general-purpose processor system

Computer-System Architecture

Single general-purpose processor system

Multiprocessors systems

- Advantages: increased throughput, economy of scale, increased reliability
- Issues: data consistency, load balancing, I/O bottle-neck, cache coherency
- Types: (1) Asymmetric multiprocessing - each processor is assigned a specie task; (2) Symmetric - each processor performs all tasks

Symmetric and Dual Core

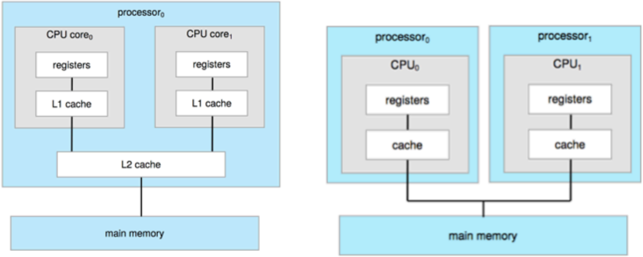
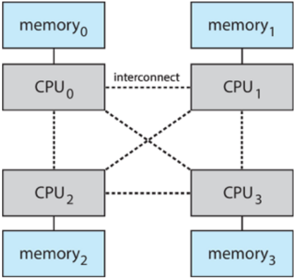


Figure: A Symmetric and Dual-Core Design Multiprocessing Architecture

Exercises: Compare single core, symmetric, multi core

1. Performance
2. Availability
3. Scaling

Non-Uniform Memory Access System (NUMA)

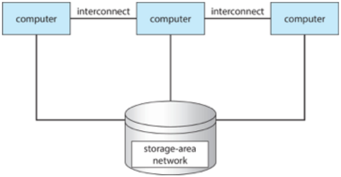


Adding additional CPUs does not scale very well - the system bus becomes a bottleneck.

Provide each CPU (or group of CPUs) with its own local memory.

All CPUs share one physical address space.

Clustered Systems



Usually sharing storage via a storage-area network (SAN)

- **Asymmetric** clustering has one machine in hot-standby mode
- **Symmetric** clustering has *n* multiple nodes running applications, monitoring each other.

Operating-System Operations

Bootstrap program - simple code to initialize the system, load the kernel

Kernel loads

Starts services provided outside of the kernel (system daemons like `syslogd, sshd`)

Kernel is interrupt driven (hardware and software)

- Hardware interrupt by one of the devices
- Software interrupt (exception or trap)

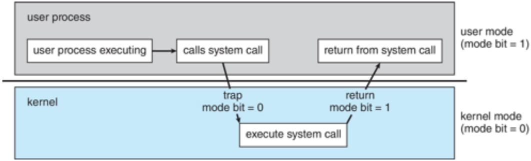


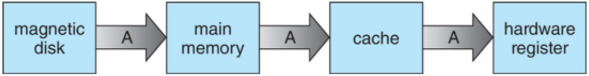
Figure: Transition from user to kernel mode

Caching

Information in use copied from slower to faster storage temporarily

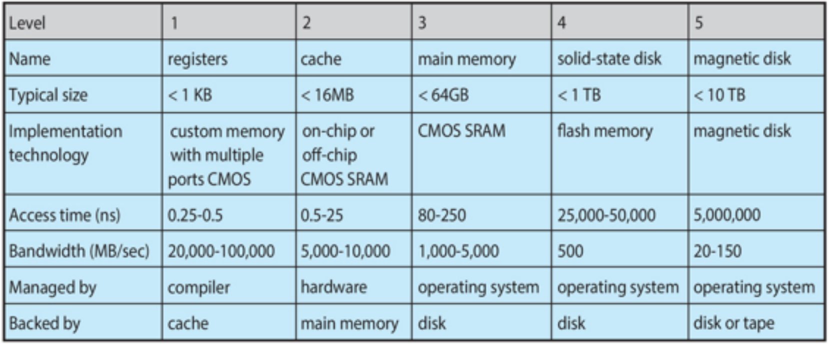
Faster storage (cache) checked first to determine if information is there

- If it is, information used directly from the cache (fast)
- If not, data copied to cache and used there



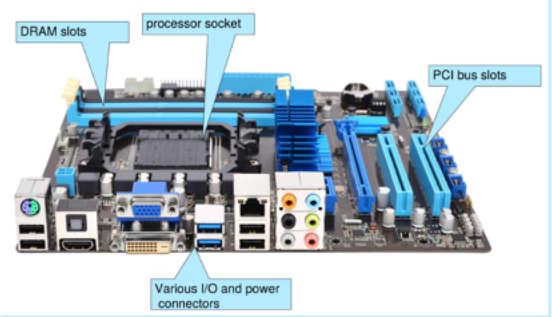
Multiprocessor environment must provide cache coherency in hardware such that all CPUs have the most recent value in their cache.

Characteristics of Various Types of Storage



Level	1	2	3	4	5
Name	registers	cache	main memory	solid-state disk	magnetic disk
Typical size	< 1 KB	< 16MB	< 64GB	< 1 TB	< 10 TB
Implementation technology	custom memory with multiple ports CMOS	on-chip or off-chip CMOS SRAM	CMOS SRAM	flash memory	magnetic disk
Access time (ns)	0.25-0.5	0.5-25	80-250	25,000-50,000	5,000,000
Bandwidth (MB/sec)	20,000-100,000	5,000-10,000	1,000-5,000	500	20-150
Managed by	compiler	hardware	operating system	operating system	operating system
Backed by	cache	main memory	disk	disk	disk or tape

Modern Computer Motherboard



Even the lowest-cost modern general purpose CPU contains multiple cores!

Apollo Guidance Computer

Apollo: 2.048 MHz, 2048 words RAM, 36,864 words ROM

MacBook Pro (mid 2012): 2.5GHz, 4GB RAM, 500GB HDD

Exercises:

Compare speed, size of volatile and size of nonvolatile memory of Apollo vs MacBook Pro (mid 2012)

Thank you