McMaster Univeristy
Department of Computing and Software
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N.B. Assignments are individual work, due as pdf format. Submit through avenue, by 30th September at 11:59 PM

Assignment Question 1.1(5*3=15Marks):

Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Solution Hints:

a)
performance of P1 (instructions/sec) = $3 * 10^9 / 1.5 = 2 * 10^9$
performance of P2 (instructions/sec) = $2.5 * 10^9 / 1.0 = 2.5 * 10^9$
performance of P3 (instructions/sec) = $4 * 10^9 / 2.2 = 1.8 * 10^9$

b)

cycles(P1) = $10 * 3 * 10^9 = 30 * 10^9$ s
cycles(P2) = $10 * 2.5 * 10^9 = 25 * 10^9$ s
cycles(P3) = $10 * 4 * 10^9 = 40 * 10^9$ s

c)

No. instructions(P1) = $30 * 10^9 / 1.5 = 20 * 10^9$
No. instructions(P2) = $25 * 10^9 / 1 = 25 * 10^9$
No. instructions(P3) = $40 * 10^9 / 2.2 = 18.18 * 10^9$
$CPI_{new} = CPI_{old} * 1.2$, then CPI(P1) = 1.8, CPI(P2) = 1.2, CPI(P3) = 2.6
f = No. instr. *CPI/time, then
f(P1) = $20 * 10^9 * 1.8/7 = 5.14$ GHz
f(P2) = $25 * 10^9 * 1.2/7 = 4.28$ GHz
f(P1) = $18.18 * 10^9 * 2.6/7 = 6.75$ GHz

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Assignment Question 1.2(5+2.5+2.5=10Marks):

Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm^2 . Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2 .

a. Find the yield for both wafer.

b. Find the cost per die for both wafers.

c. If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.

Solution Hints:

a)

die $area_{15cm}$ = wafer area/dies per wafer = pi*7.5^2 / 84 = 2.10 cm^2
$yield_{15cm}$ = $1/(1+(0.020*2.10/2))^2$ = 0.9593

die $area_{20cm}$ = wafer area/dies per wafer = pi*10^2 /100 = 3.14 cm^2
$yield_{20cm}$ = $1/(1+(0.031*3.14/2))^2$ = 0.9093

b)

$cost/die_{15cm}$ = 12/(84*0.9593) = 0.1489
$cost/die_{20cm}$ = 15/(100*0.9093) = 0.1650

c)

die $area_{15cm}$ = wafer area/dies per wafer = pi*7.5^2 /(84*1.1) = 1.91 cm^2
$yield_{15cm}$ = $1/(1 + (0.020*1.15*1.91/2))^2$ = 0.9575

die $area_{20cm}$ = wafer area/dies per wafer = pi*10^2 /(100*1.1) = 2.86 cm^2
$yield_{20cm}$ = $1/(1 + (0.03*1.15*2.86/2))^2$ = 0.9082

Assignment Question 1.3(5*3=15Marks):

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For each of the MIPS assembly code fragments in (a), (b), and (c), simulate execution starting in the **"Start state"** given below (written in hexadecimal notation) by writing down the new **register and memory state** after each instruction.

Registers:

a0	0000 0190
a1	0000 03E7
t0	0123 4567
t1	89AB CDEF
s0	1000 0000
s1	251F 326D

Memory:

1000 0000	0000 0000
1000 0004	0000 0000
1000 0008	0123 4567
1000 000C	89AB CDEF
1000 0010	0000 0000
1000 0014	0000 0000

a.

```
lw    $t0 , 0 x8 ( $s0 )
lw    $t1 , 0 xC ( $s0 )
add   $t0 , $t0 , $t1
lw    $t1 , 0 x10 ( $s0 )
add   $t0 , $t0 , $t1
```

b.

```
addi  $s1 , $s0 , 0 x8
lw    $t0 , 0( $s0 )
addi  $s1 , $s0 , 0 x4
lw    $t1 , 0( $s0 )
add   $t0 , $t0 , $t1
addi  $s1 , $s0 , 0 x4
lw    $t1 , 0( $s0 )
add   $t0 , $t0 , $t1
```

c.

```
lui   $t0 , 0 xFEDC
ori   $t0 , 0 xBA98
sw    $t0 , 0( $s0 )
sw    $t0 , 5( $s0 )
sw    $t0 , 0 xA ( $s0 )
```