Tutorial 11 – Week of Nov. 29

**Q1) 5.13**

Mean time between failures (MTBF), mean time to replacement (MTTR), and mean time to failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics:

| MTTF | MTTR |
|---|---|
| 3 Years | 1 Day |

5.13.1 Calculate the MTBF for such a device.
5.13.2 Calculate the availability for such a device.
5.13.3 What happens to availability as the MTTR approaches 0? Is this a realistic situation?
5.13.4 What happens to availability as the MTTR gets very high, i.e., a device is difficult to repair? Does this imply the device has low availability?

Solution

5.13.1
3 years and 1 day = 1096 days = 26304 hours

5.13.2
1095/1096 = 99.90875912%

5.13.3 Availability approaches 1.0. With the emergence of inexpensive drives, having a nearly 0 replacement time for hardware is quite feasible. However, replacing file systems and other data can take significant time. Although a drive manufacturer will not include this time in their statistics, it is certainly a part of replacing a disk.

5.13.4 MTTR becomes the dominant factor in determining availability. However, availability would be quite high if MTTF also grew measurably. If MTTF is 1000 times MTTR, it the specific value of MTTR is not significant.

**Q2) 5.14**

This exercise examines the single error correcting, double error detecting (SEC/DED) Hamming code.

5.14.1 What is the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code?

5.14.3 Consider a SEC code that protects 8 bit words with 4 parity bits. If we read the value 0x375, is there an error? If so, correct the error.

Solution

5.14.1

For SEC, we need to find minimum p such that

$2^p >= p + d + 1$

and then add one.

That gives us p = 8. We then need to add one more bit for SEC/DED.

5.14.3

We can represent 0x375 as

| p1 | p2 | d1 | p4 | d2 | d3 | d4 | p8 | d5 | d6 | d7 | d8 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

where p1-p4 are parity bits and d1-d8 data bits

p1 = d1 or d2 or d4 or d5 or d7 = 1 or 0 or 1 or 0 or 0 = 0
p2 = d1 or d3 or d4 or d6 or d7 = 1 or 1 or 1 or 1 or 0 = 0
p4 = d2 or d3 or d4 or d8 = 0 or 1 or 1 or 1 = 1
p8 = d5 or d6 or d7 or d8 = 0 or 1 or 0 or 1 = 0 (<- error)

Bit 8 is in error so the value would be corrected to 0x365.

**Q3) 5.16**

Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses.

This exercise shows how this table must be updated as addresses are accessed. The following data constitute a stream of virtual byte addresses as seen on a system. Assume 4 KiB pages, a four entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number.

| Decimal | 4669 | 2227 | 13916 | 34587 | 48870 | 12608 | 49225 |
|---|---|---|---|---|---|---|---|
| hex | 0x123d | 0x08b3 | 0x365c | 0x871b | 0xbee6 | 0x3140 | 0xc049 |

**TLB**

| Valid | Tag | Physical Page Number | Time Since Last Access |
|---|---|---|---|
| 1 | 0xb | 12 | 4 |
| 1 | 0x7 | 4 | 1 |
| 1 | 0x3 | 6 | 3 |
| 0 | 0x4 | 9 | 7 |

**Page Table**

| Index | Valid | Physical Page or in Disk |
|---|---|---|
| 0 | 1 | 5 |
| 1 | 0 | Disk |
| 2 | 0 | Disk |
| 3 | 1 | 6 |
| 4 | 1 | 9 |
| 5 | 1 | 11 |
| 6 | 0 | Disk |
| 7 | 1 | 4 |
| 8 | 0 | Disk |
| 9 | 0 | Disk |
| a | 1 | 3 |
| b | 1 | 12 |
| c | 0 | Disk |

5.16.1

For each access shown above, list whether the access is a hit or miss in the TLB, whether the access is a hit or miss in the page table, whether the access is a page fault, the updated state of the TLB.

Solution

| Address | Virtual Page | TLB H/M | TLB | | |
|---|---|---|---|---|---|
| | | | Valid | Tag | Physical Page |
| 4669<br>0x123d | 1 | TLB miss<br>PT hit<br>PF | 1 | b | 12 |
| | | | 1 | 7 | 4 |
| | | | 1 | 3 | 6 |
| | | | 1 (last access 0) | 1 | 13 |
| 2227<br>0x08b3 | 0 | TLB miss<br>PT hit | 1 (last access 1) | 0 | 5 |
| | | | 1 | 7 | 4 |
| | | | 1 | 3 | 6 |
| | | | 1 (last access 0) | 1 | 13 |
| 13916<br>0x365c | 3 | TLB miss<br>PT hit | 1 (last access 1) | 0 | 5 |
| | | | 1 | 7 | 4 |
| | | | 1 (last access 2) | 3 | 6 |
| | | | 1 (last access 0) | 1 | 13 |
| 34587<br>0x871b | 8 | TLB miss<br>PT hit<br>PF | 1 (last access 1) | 0 | 5 |
| | | | 1 (last access 3) | 8 | 14 |
| | | | 1 (last access 2) | 3 | 6 |
| | | | 1 (last access 0) | 1 | 13 |
| 48870<br>0xbee6 | b | TLB miss<br>PT hit | 1 (last access 1) | 0 | 5 |
| | | | 1 (last access 3) | 8 | 14 |
| | | | 1 (last access 2) | 3 | 6 |
| | | | 1 (last access 4) | b | 12 |
| 12608<br>0x3140 | 3 | TLB hit<br>PT hit | 1 (last access 1) | 0 | 5 |
| | | | 1 (last access 3) | 8 | 14 |
| | | | 1 (last access 5) | 3 | 6 |
| | | | 1 (last access 4) | b | 12 |
| 49225<br>0xc040 | c | TLB miss<br>PT hit<br>PF | 1 (last access 6) | c | 15 |
| | | | 1 (last access 3) | 8 | 14 |
| | | | 1 (last access 5) | 3 | 6 |
| | | | 1 (last access 4) | b | 12 |

**Note:** Tag 1 page is on the disk, moved to memory on the location 13, tag 8 to 14, and tag "c" to 15.