COMPSCI 2GA3 Fall, 2021

Assignment/Homework 1, Sep. 18th 2021
Assignment due date: Oct. 3rd, 23:59:59.
Note: Please work on this assignment individually. Students copying each other's answer will get a zero and will perform poor on midterm and final.

Written Exercises

Complete the following questions, most of the questions are from *Computer Organization and Design: The Hardware Software Interface: Computer Organization and Design The Hardware/Software Interface: RISC-V Edition*

Chapter 1:Computer Abstractions and Technology (20 marks)

1. Exercise 1.4 (4 Marks) Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.
   a. (2 marks) What is the minimum size in bytes of the frame buffer to store a frame?
   b. (2 marks) How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

   Solution:
   a. 1280 × 1024 pixels = 1,310,720 pixels => 1,310,720 × 3 = 3,932,160 bytes/frame.
   b. 3,932,160 bytes × (8 bits/byte) /100E6 bits/second = 0.31 seconds

2. Exercise 1.6 (4 Marks) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 (1.0E6 = 1.0 x 10^6) instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2?

   a. (2 marks) What is the global CPI for each implementation?

   b. (2 marks) Find the clock cycles required in both cases.

Solution:

a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. × CPI/clock rate

Total time P1 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s

Total time P2 = $(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s

CPI(P1) = $10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) = $6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$

b. clock cycles(P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$

clock cycles(P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

3. Exercise 1.8 (4 Marks) The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, has a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

   a. (1 mark) For each processor find the average capacitive loads

   b. (1 mark) Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

   c. (2 marks) If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

Solution:

1.8.1 $C = 2 \times DP/(V^2 \times F)$

Pentium 4: $C = 3.2E{-}8F$

Core i5 Ivy Bridge: $C = 2.9E{-}8F$

1.8.2 Pentium 4: $10/100 = 10\%$

Core i5 Ivy Bridge: $30/70 = 42.9\%$

1.8.3 $(S_{new} + D_{new})/(S_{old} + D_{old}) = 0.90$

$D_{new} = C \times V_{new}2 \times F$

$S_{old} = V_{old} \times I$

$S_{new} = V_{new} \times I$

Therefore:

$V_{new} = [D_{new}/(C \times F)]1/2$

$D_{new} = 0.90 \times (S_{old} + D_{old}) - S_{new}$

$S_{new} = V_{new} \times (S_{old}/V_{old})$

Pentium 4:

$S_{new} = V_{new} \times (10/1.25) = V_{new} \times 8$

$D_{new} = 0.90 \times 100 - V_{new} \times 8 = 90 - V_{new} \times 8$

$V_{new} = [(90 - V_{new} \times 8)/(3.2E8 \times 3.6E9)]^{1/2}$

$V_{new} = 0.85\,V$

Core i5:

$S_{new} = V_{new} \times (30/0.9) = V_{new} \times 33.3$

$D_{new} = 0.90 \times 70 - V_{new} \times 33.3 = 63 - V_{new} \times 33.3$

$V_{new} = [(63 - V_{new} \times 33.3)/(2.9E8 \times 3.4E9)]^{1/2}$

$V_{new} = 0.64\,V$

In 3c (1.8.3), dynamic power is calculated according to the formula that is used in some literature

$$Dynamic\ power = C * F * V^2$$

However if you use the formula that is is presented on our slides Ch1, slide 70

$$Dynamic\ power = 1/2 * C * F * V^2$$

the solution is
1.18 for Pentium 4
0.84 for Core i5Ivy Bridge
Both solutions we consider correct as long as you specify which formula you use.

4. Exercise 1.10 (4 Marks) Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm^2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2.

   a. (1 mark) Find the yield for both wafers.

   b. (1 mark) Find the cost per die for both wafers.

   c. (1 mark) If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.

   d. (1 mark) Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm^2.

   Solution:

1.10.1 $\text{die area}_{15\text{cm}} = \text{wafer area/dies per wafer} = \pi \times 7.5^2/84 = 2.10\,\text{cm}^2$

$\text{yield}_{15\text{cm}} = 1/(1 + (0.020 \times 2.10/2))^2 = 0.9593$

$\text{die area}_{20\text{cm}} = \text{wafer area/dies per wafer} = \pi \times 10^2/100 = 3.14\,\text{cm}^2$

$\text{yield}_{20\text{cm}} = 1/(1 + (0.031 \times 3.14/2))^2 = 0.9093$

1.10.2 $\text{cost/die}_{15\text{cm}} = 12/(84 \times 0.9593) = 0.1489$

$\text{cost/die}_{20\text{cm}} = 15/(100 \times 0.9093) = 0.1650$

1.10.3 $\text{die area}_{15\text{cm}} = \text{wafer area/dies per wafer} = \pi \times 7.5^2/(84 \times 1.1) = 1.91\,\text{cm}^2$

$\text{yield}_{15\text{cm}} = 1/(1 + (0.020 \times 1.15 \times 1.91/2))^2 = 0.9575$

$\text{die area}_{20\text{cm}} = \text{wafer area/dies per wafer} = \pi \times 10^2/(100 \times 1.1) = 2.86\,\text{cm}^2$

$\text{yield}_{20\text{cm}} = 1/(1 + (0.03 \times 1.15 \times 2.86/2))^2 = 0.9082$

1.10.4 $\text{defects per area}_{0.92} = (1-y^{-.5})/(y^{-.5} \times \text{die\_area}/2) = (1 - 0.92^{-.5})/(0.92^{-.5} \times 2/2) = 0.043\,\text{defects/cm}^2$

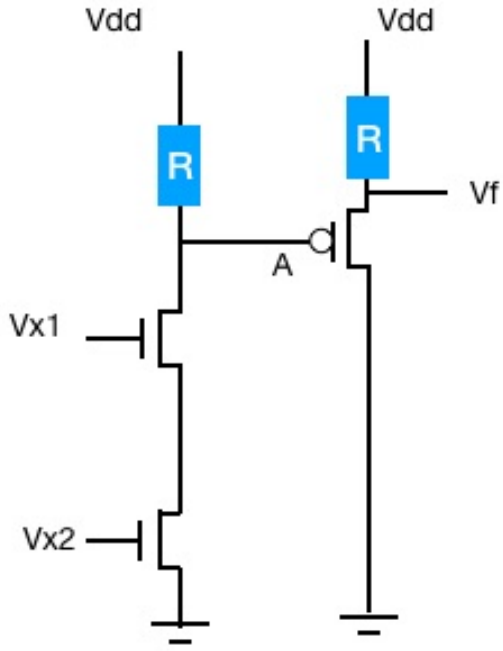
$\text{defects per area}_{0.95} = (1-y^{-.5})/(y^{-.5} \times \text{die\_area}/2) = (1 - 0.95^{-.5})/(0.95^{-.5} \times 2/2) = 0.026\,\text{defects/cm}^2$

5. Logic gates (4 Marks)
   A logic gate shown if figure below is made of two NMOS transistors and one PMOS transistor.

   a. (2 marks) Fill out the truth table

   b. (2 marks) Represent this gate by graphical symbol(s).

Vx1	Vx2	A	Vf
0	0		
0	1		
1	0		
1	1		



Vdd= 5V = “1”
Ground= 0V = “0”

Solution:

a)

Vx1	Vx2	A	Vf
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

b)

This is NOT AND or NAND gate