Homework 4

1. 5 Components of von Neumann model:
   - Memory: stores data in memory locations using the memory's address register (MAR) and memory's data register (MDR).
   - Processing Unit: performs complex operations on information using temporary memory and the Arithmetic and Logic Unit (ALU).
   - Input: Allows information to be entered into the computer.
   - Output: Allows information in computer to be displayed.
   - Control Unit: Keeps track of where we are within process of executing program and where we are within the process of each instruction.

2. For the processing unit to get data from memory, the processing unit writes the address into the MAR, sends a "read" signal to memory, then reads the data from MDR. To get data to the memory, the processing unit writes the data to MDR, writes the address to MAR, then sends a write signal to memory.

3. "Program counter" is misleading because it is not counting anything. "Instruction pointer" is more insightful because the registers "point" to the next instruction to be processed.

4. A word length of a computer is the size of the quantities normally processed by the Arithmetic and Logic Unit (ALU). Word length does not affect what a computer is able to compute but affects how fast a computer can compute.

5. The two components of an instruction are opcodes and operands. Opcodes contains information on what the instruction does. Operands contains the information on which registers to apply the instruction to.

6. The instruction holds only 32 bits. 60 opcodes take up 6 bits because the opcodes would be from 000000 to 111011. 32 registers take up 5 bits because the registers would be from 00000 to 11111. 32 - 6 - 5 - 5 = 16. IMM takes up 16 bits with 2^{16} potential values. Since IMM is a 2's complement it can hold values between -32768 to 32767.

7. Phases of Instruction cycle:
   - Fetch: obtains next instruction from memory and loads it into the instruction register (IR)
   - Decode: examines the instruction in order to figure out what the microarchitecture is being asked to do.
   - Evaluate Address: computes the address of the memory location that is needed to process the instruction.
   - Fetch Operands: obtains source operands needed to process the instruction.
   - Execute: carries out execution of instruction.
   - Store Result: result is written to its designated destination.

8. If the memory's addressibility is 64 bits it tells us that the MDR is 64 bits but does not tell the size of MAR.

9. a. To represent all possible memory locations we find $\log_2(256) = 8$ bits.

b. Because PC-offsets are in 2s complement, in order to allow control transfer between instructions 30 locations away we need 6 bits to account for memory locations -32 to 31 locations away.

c. If the control instruction is in location 5 then the incremented PC is 6. This means that the PC-relative offset of 15 is $15 - 6 = 9$.

10. Because the IMM is 5 bits and 2s complement, the largest possible number we can represent in an ADD instruction is 15.