Christopher Hush

Homework 3

LO RO, INPUT , load INPUT into RO AND RIPI, HO ; Clear R1 AND RZ, RZ, 70; Clear RZ ADD RZ, RZ, HI ; Set 122 to 1 for bit checking regularly they have the systemed By which the AND R3, R3, HD 1 Llow R3 For 166+ counter DO ADD R3, R3, #1; add to counter AND RS, RO, RZ; compare bot from RO and RZ BRP DNE , if bit is I go to ONE ZERO ADD RZ, RZ, RZ ; Shift bits left BR CHECK ONE ADD RI, RI, #1 , increase of bit country BR ZERDMON TO TO GENOX CHELL AND RS, RS, HO ADD RS, R3, #-16; IF country has not checked BR, DO ; all 16 bits keep looping Carolina HALT 10 137 1010 INPUT .FILL \$4976 · END · COLD IO

2. RI is not initialized with AND RI, RI, #O. Detected in run time. SUM is not defined. Perioded in assembly time. 3. Advantages of Hoing 1/0 through a Trap routing distual the programmer dorsit and to know ditails of hardward data register hardward Status registins, and asynchronous nature of input. 4.a. 286 TRAP server routines can be implemental breaux than are 256 TRAP vertor locations from 20000 to xOUFF The Colored per from the on the 6) 2 across to memory are made in a TRAP instruction First is when we are fetching the instruction from Memory. Secure is when we are fetching source operands. 1. 1111000000100001 2. X0430 ST R7, X043B 3. X 0437 RET 4. Hooken Horns OH, 201, 20 and Phons 1. 5 x 6 2.0 7 6 x 4 6 0110/11/11/1010 (-6) 0101 (5) x 0110 (b) OFFICOUPY TOOLOO (4) 00060000 0000 1010/00000000 01010 /111101000 010100 00000000000000 00000000 11101000 (-27) 0011110 (30)

4. -3 x-Z 3- 2x6 0010 (2) 0011 (3) 0110 (6) 1 0010 (2) 1101 1100 0000 1101(-3) 01100 1110 (-2) 000000 (111/10/1 (-3) 00000000 1.1 1 1 1 1 0 (-2) 0001100 (12) 0,000,0000 11111010 11110100 111100000 1110100000 11/0/1000000 100000000 00000110 (6) 5. -8 x 7 11111000 (-8) 1000 (8) 0111 0111 (7) 1000 (-8) (11110000 000000000000000 11001000 (-56)