Priyal Riddhish Chhatrapati

🖥 Website | 📞 404.820.0721 | ✉ priyal.rch@gmail.com | ✉ priyal.rch@gatech.edu | in LinkedIn | ⧉ GitHub

EDUCATION

Georgia Institute of Technology (GPA - 4.0/4.0)   Aug. 2021 – Present
Master of Science in Computer Engineering   Atlanta, GA

- **Coursework**: Deep Learning, Advanced Programming Techniques, Parallel Programming, Interconnection Networks, Advanced Computer Architecture
- **Research**: Accelerating Object Detection and Tracking by exploiting Parallelism

BITS Pilani (GPA - 9.1/10)   Aug. 2016 – May 2020
Bachelor of Engineering in Electronics and Instrumentation Engineering   Goa, India

- **Research**: Approximate Computing for Fault Tolerant Data Storages(National University of Singapore)
- **Coursework**: Computer Architecture, Object Oriented Programming, Real Time Operating Systems(Audit), Algorithms(Audit)

EXPERIENCE

NVIDIA   May 2022 - August 2022
Deep Learning Performance Intern, TensorRT   Santa Clara, USA

- Performance optimizations for **MLPerf** workload using **TensorRT** C/C++ and CUDA libraries
- **Profiling Deep learning Code** using Nsight Systems

Georgia Institute of Technology   August 2021 – May 2022
Research Assistant   Atlanta, USA

- Implementing State of the Art **Computer Vision Object Tracking Models** for Self Driving Cars;
- **Rewriting software stack (Pytorch)** for customized hardware (FPGA accelerator chip);
- Achieved a **speedup of 220x** over a sequential implementation.

SiFive   Sept 2020 – June 2021
Engineer - VLSI   Bangalore, India

- Developed **MIPI CSI-2 v3.0 bus**; Standard Interface between Cameras and Host Processor;
- Co-authored Specification Document for the CSI-2 bus; Co-authored Microarchitectural Document for the CSI-2 bus
- Implemented CSI-2 bus using Verilog; **Saving ~$100,000** in licensing costs and royalties.

PROJECTS

Convolution Neural Network Accelerator

- AXI4 compliant simulator to interface with CPU
- Novel 1 dimensional Weight stationary dataflow

Trace Based L1 Cache Simulator

- Developed a Simulator supporting variable block size, associativity and cache size
- Reports number of hits, misses and latency

SKILLS

Languages : C/C++, Python, Java, Bash

Frameworks, Libraries : Pytorch, CUDA, Multiprocessing, Pthreads, OpenGL, Numpy, Linux

Tools : GitHub, Vivado, MATLAB, Proteus, ModelSim, Jupyter