Memory

This lesson discusses the basic 1 bit DRAM and SRAM. Then expands to discuss the organization of a large scale memory system, including row and column reads and writes. Memory controllers and their role in DRAM is also explained.

Memory Technology: SRAM and DRAM

SRAM = static random access memory. Static = retains data when power is on.
DRAM = dynamic random access memory. Dynamic = loses data unless refreshed.

SRAM requires more transistors than DRAM, but is faster.

Memory Chip Organization

Memory is organized and accessed using Row Decoders and Column Decoders.
So a row can be written and read at the same time, this is called fast page mode.

Using the fast page mode, memory can be read in a more efficient order.

Connecting DRAM to the Processor

DRAM is accessed to the processor through the front-side bus using a memory controller.
The downside of this is the DRAM must be much more standardized and inflexible to work with the on-chip memory controller.