MK3875 and MK38P75

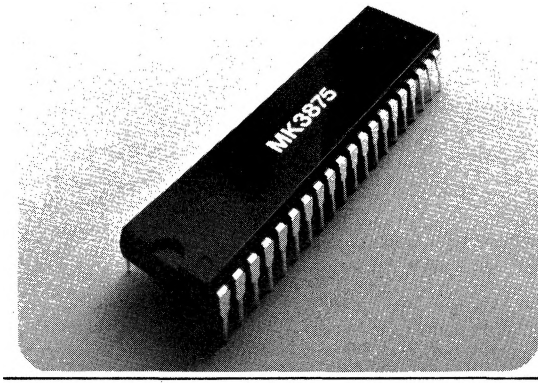
MK3875 FEATURES

- ☐ Available with 2K or 4K bytes of mask programmable ROM memory.
- ☐ 64 bytes scratchpad RAM
- ☐ 64 bytes of Executable RAM
- ☐ Standby feature for low power data retention of executable RAM including:
  Low standby power
  Low standby supply voltage
  No external components required to trickle charge battery.
- ☐ Software compatible with 3870 family
- ☐ 30 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary Timer
  Interval Timer Mode
  Pulse Width Measurement Mode
  Event Counter Mode
- ☐ External Interrupt Input
- ☐ Crystal, LC, RC, or external time base options available
- ☐ Low power under normal operation (285 mW typ.)
- ☐ +5 volt main power supply
- ☐ Pinout compatible with 3870 family

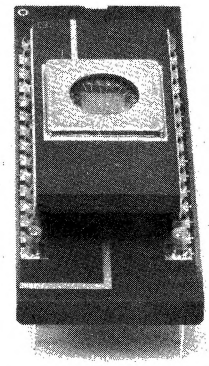
MK38P75 FEATURES

- ☐ EPROM version of MK3875
- ☐ Piggyback RPOM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3875
- ☐ In-socket emulation of MK3875

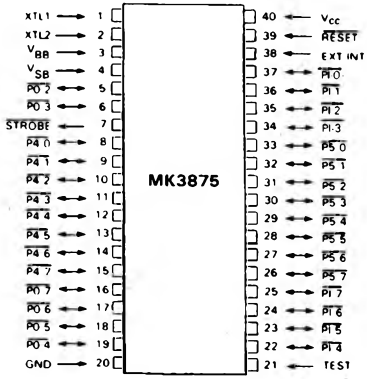
MK3875



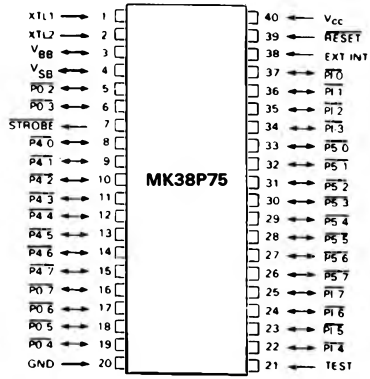
MK38P75



PIN CONNECTIONS
MK3875



PIN CONNECTIONS
MK38P75



PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ - $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input
V_{SB}	Standby Power	Input
V_{BB}	Substrate Decoupling	Input

GENERAL DESCRIPTION

The MK3875 Single Chip Microcomputer offers a Low Power Standby mode of operation as an addition to the 3870 Family. The Low Power Standby feature provides a means of retaining data in the executable RAM on the MK3875 while the main power supply line (V_{CC}) is at 0 volts and the rest of the MK3875 microcomputer is shut down. The executable RAM is powered from an auxiliary power supply input (V_{SB}) while operating in the Lower Power Standby mode. When V_{SB} is maintained at or above its minimum level, data is retained in the executable RAM memory with a very low power dissipation.

The MK3875 retains commonality with the rest of the industry standard 3870 family of single chip microcomputers. It has the same central processing unit, oscillator and clock circuits, and 64 byte scratchpad memory array. Also, the 3870's sophisticated programmable binary timer is included which provides three different operating modes. Two pins on the MK3875 are dedicated to the Low Power Standby mode and are designated as V_{SB} and V_{BB}. The $\overline{RESET}$ line serves to reset the MK3875 and place it in a protected state so that the contents of the Executable RAM will remain unchanged when V_{CC} is being powered down to 0 volts. All other pins on the MK3875 are identical in function to corresponding pins on the MK3870, so that pin compatibility is maintained. The MK3875 executes the entire 3870 instruction set.

The MK38P75 microcomputer is the PROM based version of the MK3875. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28-pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P75 retains the pinout and architectural features as other members of the 3870 family. The MK38P75 is discussed in more detail in a later section.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$ - $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ are 30 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data are present on the $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ - may be used to externally reset the MK3875. When pulled low, the Mk3875 will reset. When allowed to go high the MK3875 will begin program execution at program location H '000'. Additionally, when $\overline{RESET}$ is brought low all accesses of the executable RAM are prevented and the RAM is placed in a protected state for powering down V_{CC} without loss of data.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal (2 to 4 MHz), LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering an MK3875.

TEST is an input used only in testing the MK3875. For normal circuit function this pin may be left unconnected but it is recommended that TEST be grounded.

V_{CC} is the power supply input +5 V.

V_{SB} is the RAM standby power supply input.

V_{BB} is the substrate decoupling pin. A .01 micro-Farad capacitor is required which is tied between V_{BB} and GND.

MK3875 ARCHITECTURE

The basic functional elements of the mask ROM MK3875 single chip microcomputer are shown in the block diagram in Figure 1. A programming model is shown in Figure 2. Much of the Mk3875 architecture is identical with the rest of the devices in the 3870 family. The significant features of the MK3875 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to the 3870 family.

MAIN MEMORY

The main memory section on the MK3875 consists of a combination of ROM and executable RAM.

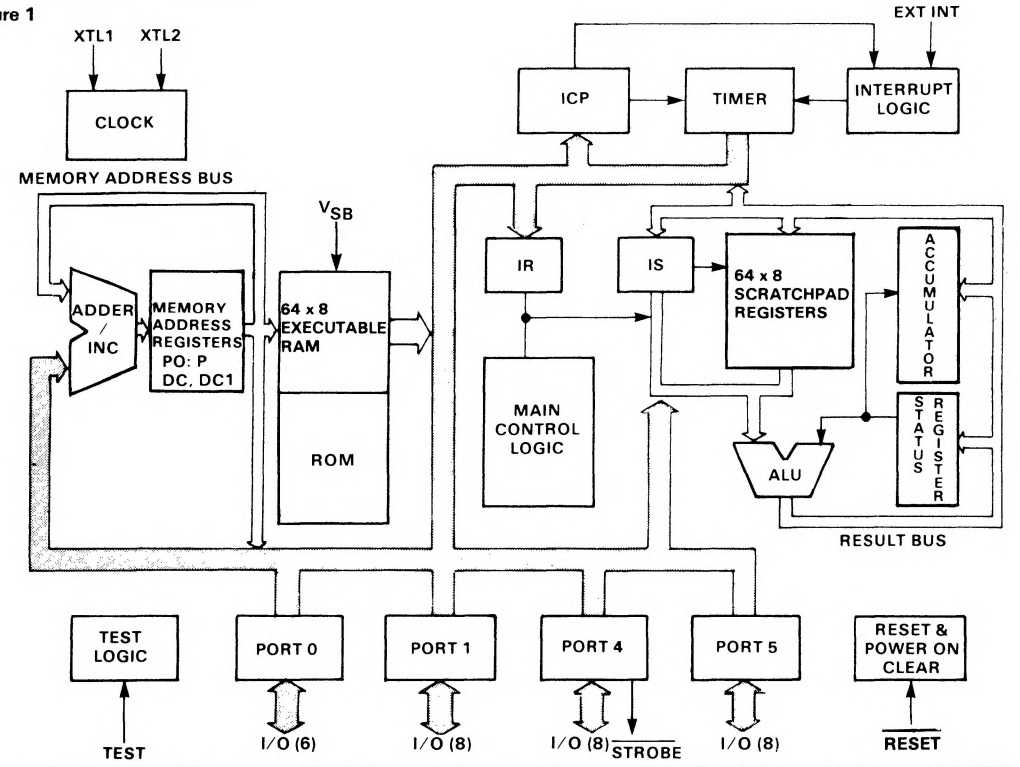
There are four registers associated with the main memory section. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC) and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions during program execution. P is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine.

The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data counters only DC can access the memory. However, the XDC instruction allows DC and DC1 to be exchanged.

The length of the PO, P, DC, and DC1 registers for all MK3875 devices is 12 bits. Figure 3 shows the amounts of

MK3875 BLOCK DIAGRAM

Figure 1



ROM and Executable RAM for each device in the MK3875 family.

EXECUTABLE RAM

The upper bytes of the total address space in all MK3875 devices are RAM memory. As with the ROM memory, the RAM may be addressed by the PO and DC address registers. The executable RAM may be accessed by all 3870 instructions which address main memory indirectly through the Data Counter (DC) register. Additionally, the MK3875 may execute an instruction sequence which resides in the executable RAM. Note that this sequence cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory. The contents of the executable RAM memory are preserved when the Low Power Standby mode is in operation.

I/O PORTS

The MK3875 provides 30 bits of bidirectional parallel I/O. These lines are addressed as Ports 0, 1, 4 and 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pins are covered in the 3870 Family Technical Manual.

Since two pins are dedicated to serve the Standby Power mode (V_{SB}), port 0 has only the upper 6 bits, $\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$, available for use as general purpose I/O pins. Ports 1, 4, and 5 are all a full 8 bits wide.

The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3875 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{STROBE}$ may be used as an input strobe simply by doing a dummy output of H '00' to Port 4 after completing the input operation.

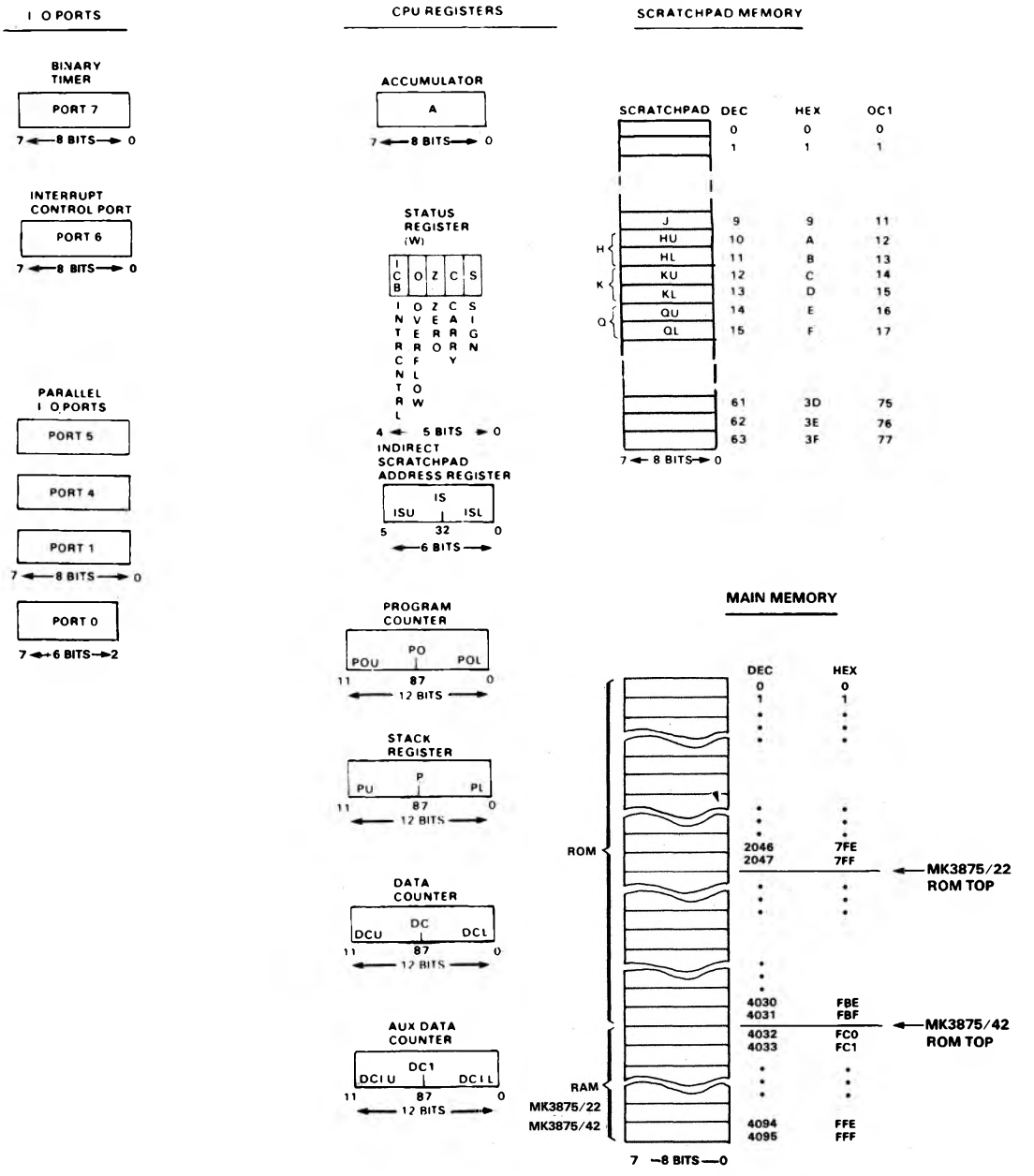
STANDBY POWER MODE

On the MK3875, the contents of the on-chip executable RAM can be saved when the Standby Power mode is operative. The Standby Power mode allows the MK3875's main power supply to drop all way down to 0 volts while the on-chip executable RAM is powered from the auxiliary low power supply input, V_{SB}. Thus, key variables may be maintained within the MK3875 executable RAM during the time that the rest of the microcomputer is powered down.

On the MK3875, two of the pins which are used as bidirectional port pins on the MK3870 are used for the Standby Power feature. Port 0, Bit 0 (PO-0), remains readable and writeable although it is not connected to a package pin. The logic level being applied to the auxiliary

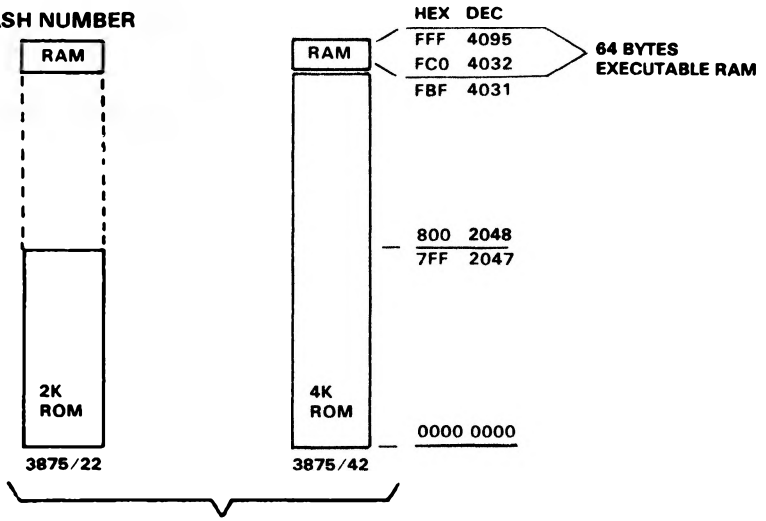
3875 PROGRAMMABLE REGISTERS, PORTS AND MEMORY MAP

Figure 2



MK3875 MAIN MEMORY SIZES AND TYPES BY SLASH NUMBER

Figure 3



All devices contain 64 bytes of scratchpad RAM

Data derived from addressing any locations other than within the specified ROM or RAM space is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0,P,DC,DC1)	ROM Size (Decimal)	Executable RAM Size
MK3875/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3875/42	64 bytes	12 bits	4032 bytes	64 bytes

power supply input (V_{SB}) can be read at Port 0, Bit 1 ($\overline{PO\text{-}1}$). Writing to $\overline{PO\text{-}1}$ has no effect.

A capacitor (.01 microfarads) must be connected between pin 3 (V_{BB}) and ground. V_{BB} is bonded directly to the substrate of the MK3875. The purpose of the capacitor is to decouple noise on the substrate of the circuit when V_{CC} is switched on and off.

It is recommended that Nickel Cadmium batteries (typical voltage of 3 series cells = 3.6V) be used for standby power, since the MK3875 can automatically trickle charge the three NiCads. If more than three cells in series are used, the charging circuit must be provided outside the MK3875.

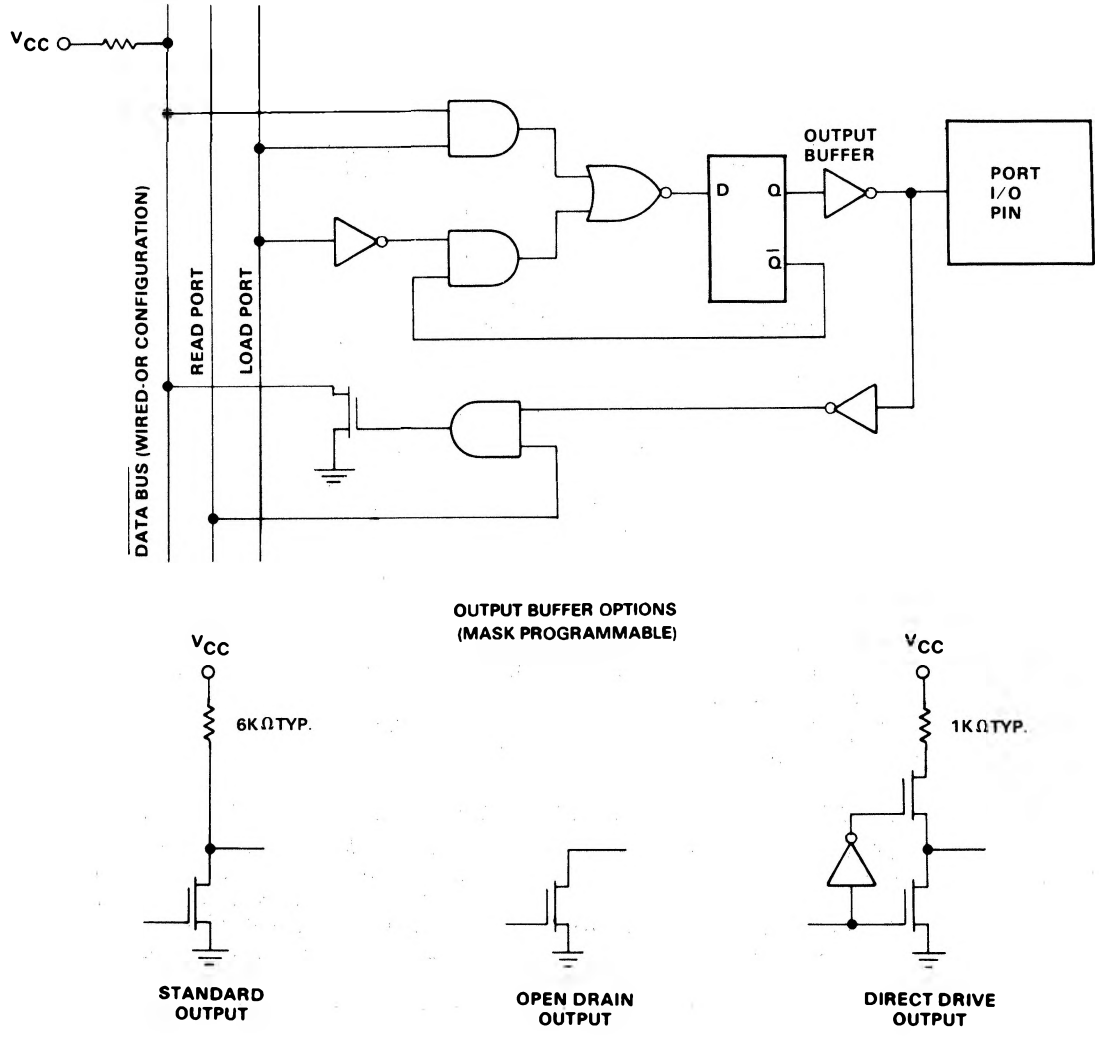
Whenever $\overline{RESET}$ is brought low, the executable RAM is placed in a protected state. Also the RAM is switched from V_{CC} power to the V_{SB} power. When powering down, it may be desirable to interrupt the MK3875 when an impending power down condition is detected, so that the necessary data can be saved before V_{CC} falls below the minimum level. After the save is completed, $\overline{RESET}$ can fall, which prevents any further access of the RAM. The timing for this power down sequence is illustrated in Figure 5A.

A second power down sequence is illustrated in Figure 5B, and may be used if a special save data routine is not needed. The EXT INT line need not be used. Note that for both cases shown in Figures 5A and 5B, $\overline{RESET}$ must be low before V_{CC} drops below the minimum specified operating voltage for the MK3875. This is to ensure that the contents of the executable RAM are not altered during the power down sequence.

There may be a set of variables stored in the RAM memory which is continually updated during the tme when the MK3875 is in its normal operating mode. If a particular variable occupies more than one byte of RAM, there can be a problem if a reset occurs in response to an impending power down condition during the time that the multi-byte variable was being modified. If such a reset occurs, then only part of the variable may contain the updated value, while the rest contains the old value. An example of this case would be when a double precision (2 byte) binary number is being saved in the executable RAM. Suppose that a new value of the number has been calculated in the program, and that this new value is to replace the old value contained in the executable RAM; note that a reset could occur just after the program wrote one byte of the new value

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable). These two inputs have Schmitt trigger inputs with a minimum of 0.2 volts of hysteresis.

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P75.

into the RAM. When power is restored following the Standby Power mode, the double precision variable would contain an erroneous value.

This problem can be avoided if the external interrupt is used to signal the MK3875 of an impending power down condition. The user's system should be designed so that the MK3875 can properly save all variables between the time that the external interrupt occurs and $\overline{\text{RESET}}$ falls. If multi-byte variables must be saved during the Standby Power mode and it is not desirable to use the external interrupt in the manner described above, then each byte of a multi-byte variable may be kept with an associated flag. The method of updating a two byte variable would be as follows:

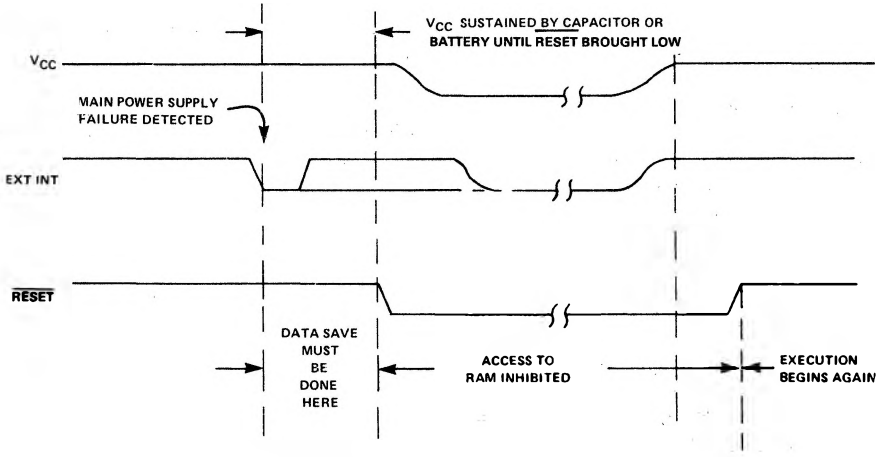
- Clear Flag Word 1
- Update Byte 1
- Set Flag Word 1
- Clear Flag Word 2
- Update Byte 2
- Set Flag Word 2

Now if $\overline{\text{RESET}}$ goes low during the update of a byte of a variable, the flag word associated with that byte of data will be reset. Any byte of the variable where the flag word is "set" is a good byte of data. While this method significantly encumbers the data storage process, it eliminates the need for a power fail interrupt which both reduces external circuitry and leaves the external interrupt pin completely free for other use.

Often it is necessary to distinguish between an initial power-on condition wherein there is no valid data stored in the RAM (or where V_{SB} has dropped below the minimum required stand-by level) and a re-application of power wherein valid RAM data has been maintained during the power outage. One method of distinguishing between these two conditions is to reserve several memory locations for key words and checksums. When V_{CC} is applied and processor operation begins, these locations can be checked for proper contents. However, this method may not be perfectly accurate as those locations holding key codes may be maintained even though V_{SB} drops below its minimum required level while other RAM locations may lose data, or they could power up with the exact data required to match the key codes. Also a checksum may be matched on occasion even though RAM data has been corrupted. The accuracy of this method is improved by increasing the number of memory locations used and the variety of key codes and or checksums used.

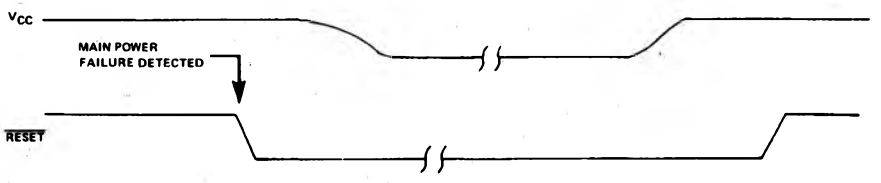
SAVE ROUTINE REQUIRED, $V_{SB} > 3.2$ VOLTS

Figure 5a



NO SAVE ROUTINE REQUIRED, $V_{SB} > 3.2$ VOLTS

Figure 5b

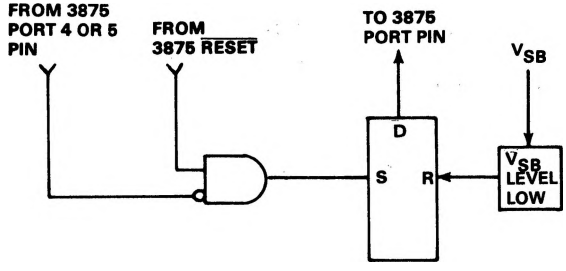


A more reliable method is the external V_{SB} flip-flop. The flip-flop is designed to power up in a known first state and hold that first state until forced into a second state. As long as V_{SB} is above the minimum operating level, the flip-flop can hold the second state, but, if V_{SB} drops below the minimum level, the flip-flop will flip back to the first state. Thus when power is initially applied or if V_{SB} drops below the minimum level during a V_{CC} outage, the flip-flop will be in the first state. The flip-flop output can be read through a port pin by the processor when processor operation begins to determine whether the RAM data is valid (second state) or invalid (first state). If the flip-flop is found to be in the first state it can be forced to the second state by the processor. If it holds the second state, V_{SB} is above the minimum level (batteries are charged).

A conceptual diagram is shown in Figure 6.

CONCEPTUAL DIAGRAM

Figure 6



MK38P75 GENERAL DESCRIPTION

The MK38P75 is the EPROM version of the MK3875. It retains an identical pinout with the MK3875, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P75 is housed in the "R" package which incorporates a 28-pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P75 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3875 devices. Thus, the MK38P75 eliminates the need for emulator board products. In addition, several MK38P75s can be used in prototype systems in order to test design concepts in field service before commiting to high-volume production with mask ROM MK3875s. The compact size of the MK38P75/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P75 can be used as the actual production device.

Most of the material which has been presented for the MK3875 in this document applies to the MK38P75. This includes the description of the pin configuration, architecture, and programming mode. Additional information is presented in the following sections.

MK38P75 I/O PORTS

The MK38P75 is offered with two types of output buffer options on Ports 4 and 5. These are the open drain output buffer and the standard output buffer which are pictured in Figure 4. The open drain version of the MK38P75 is provided so that user-selected open drain port pins on the MK3875 can be emulated prior to ordering those mask ROM devices. Figure 9 lists which version(s) of the MK38P75 has open drain output buffers and which has standard output buffers in parentheses following the specified MK38P75 part ordering number (MK9XXXX).

MK38P75 MAIN MEMORY

As can be seen from the block diagram in Figure 7, the MK38P75 contains executable RAM in the main memory map. The MK38P75 contains no on-chip ROM. Instead, the memory address lines are brought out to the 28-pin socket located directly on top of the 40-pin package, so the external ERPOM memory is addressed as main memory.

There is one memory version of the MK38P75 and it is designated as the MK38P75/02. The MK38P75/02 contains 64 bytes of on-chip executable RAM. The MK38P75/02 can emulate the following devices.

MK3875/22
MK3875/42

The MK38P75/02 cannot exactly emulate the MK3875/40 because of the 64 bytes of executable RAM in the upper ROM space of the MK3875/40.

Addressing of main memory on the MK38P75 is accomplished in the same way as it is for the MK3875. See Figure 8 for main memory addresses and for address register size in the MK38P75.

MK38P75 EPROM SOCKET

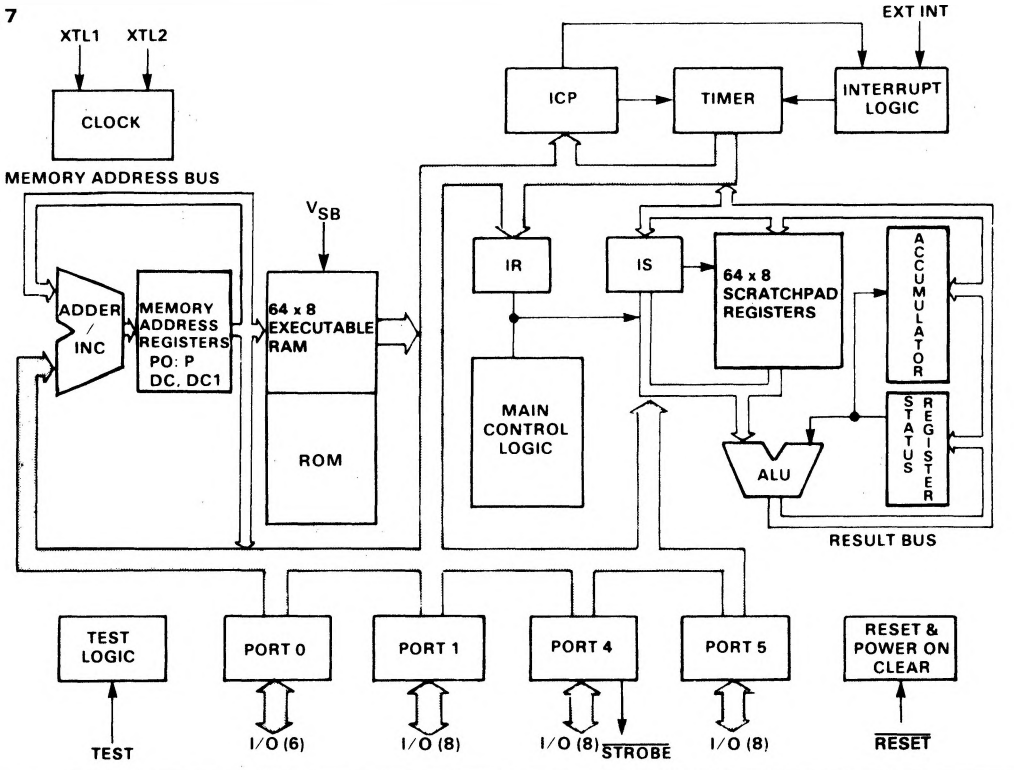
A 28-pin ERPOM socket is located on top of the MK38P75 "R" package. The socket and compatible ERPOM memories are shown in Figure 9. When 24-pin memories are used in the 28-pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24-pin memory should be lower justified in the 28-pin socket).

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P75.

Initially, the MK38P75 that is compatible with the MK2716 is available. The MK38P75 designed to accommodate the 28-pin memory devices will be available at a later date.

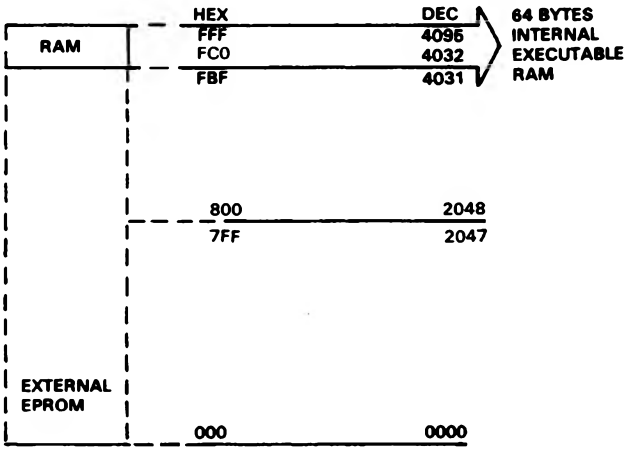
MK38P75 BLOCK DIAGRAM

Figure 7



MK38P75 MAIN MEMORY MAP

Figure 8

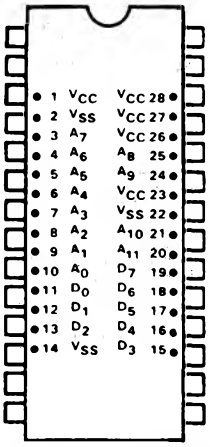


MK38P75/02

Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P73/02 97310	64 bytes	12 bits	0 bytes	64 bytes

MK38P75 "R" PACKAGE SOCKET PINOUT

Figure 9



MK97413 (Open Drain Outputs) Compatible Memories
2758
MK2716
2516
2532

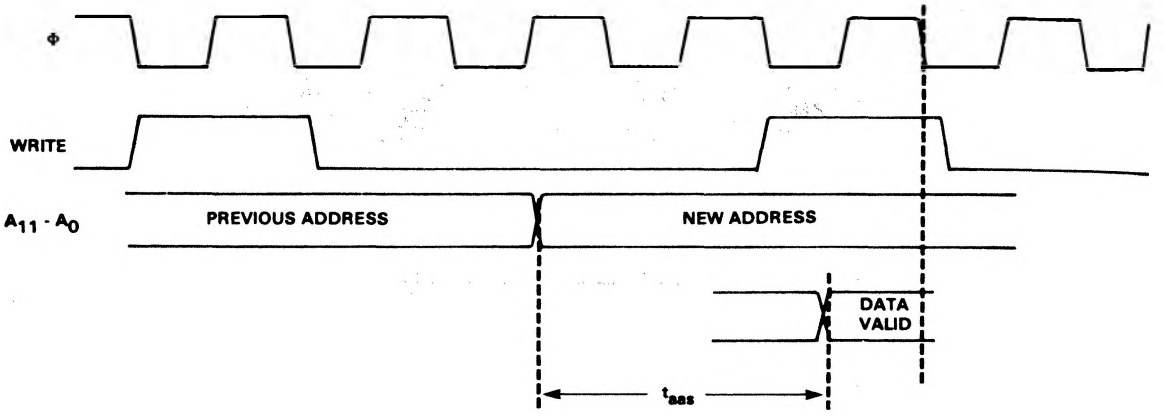
MK97403 (Standard Outputs) Compatible Memories
2758
MK2716
2516
2532

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P75 is shown in the next table. The Φ clock signal is derived internally in the MK38P75 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P75 which corresponds to a machine cycle, during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles, respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is the cycle which is pictured in the timing diagram. After a delay from the falling edge of the WRITE clock, the address lines become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P75 version is shown as t_{aas} or the time when address is stable until data must be valid on the data bus lines. The equation for calculating available memory access time along with some calculated access times based on the listed time base frequencies is shown in the following table.

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P75

Figure 10



Φ Signal is internal to the MK38P75

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850\text{ ns}$$

(FROM ADDRESS STABLE)

	4 MHz	3.5 MHz	3 MHz	2.5 MHz	2 MHz
ACCESS TIME	650 ns	825 ns	1.15 μs	1.55 μs	2.15 μs

3875 TIME BASE OPTIONS

The 3875 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 3875 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3875 must be specified at the time when mask ROM devices are ordered. However, the MK38P75 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26 pF capacitor between XTL 1 and GND and an internal 26 pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

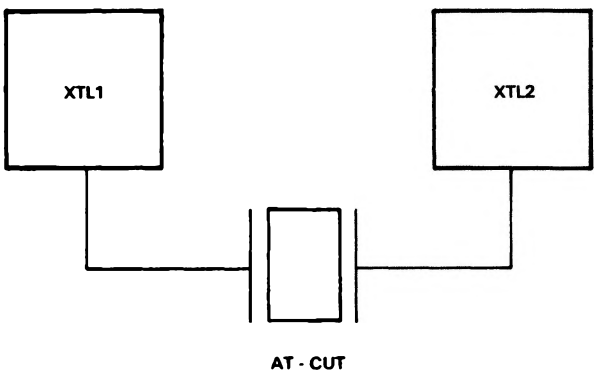
CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproducability from system to system is unsurpassed. The 3875 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 12 lists the required crystal parameters for use with the 3875. The Crystal Mode time base configuration is shown in Figure 11.

Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3875, in the event that a single crystal is to provide the time base for more than just a single 3875.

While a ceramic resonator may work with the 3875 crystal oscillator, it was not designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

CRYSTAL MODE CONNECTION
Figure 11



CRYSTAL PARAMETERS

Figure 12

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

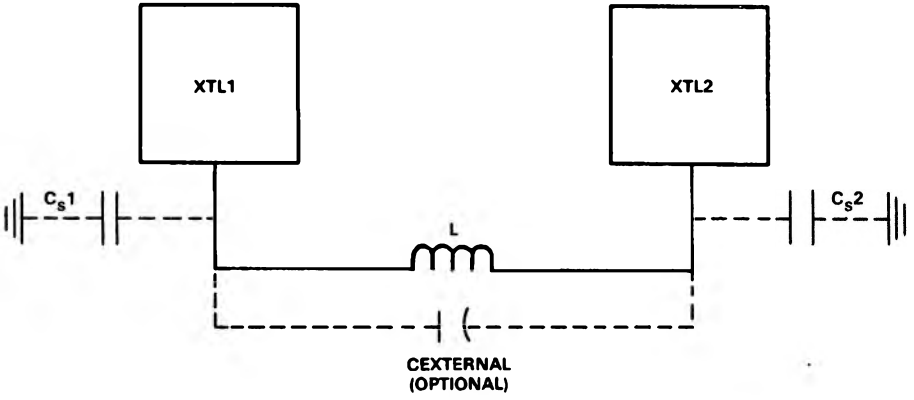
*This holder may not be available at frequencies near the lower end of this range.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3875 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 13. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3875, C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the at XTL1 and capacitance looking into the internal two port network XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

LC MODE CONNECTION

Figure 13

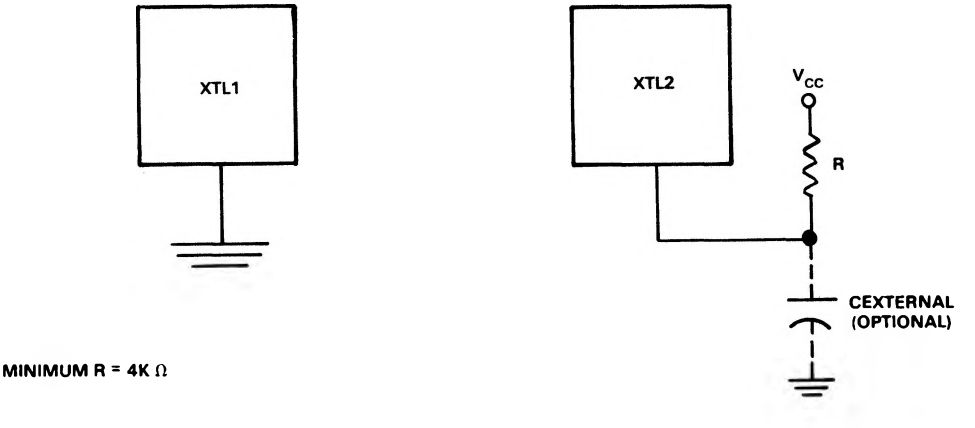


Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3875 at XTL1 and XTL2, and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3875.

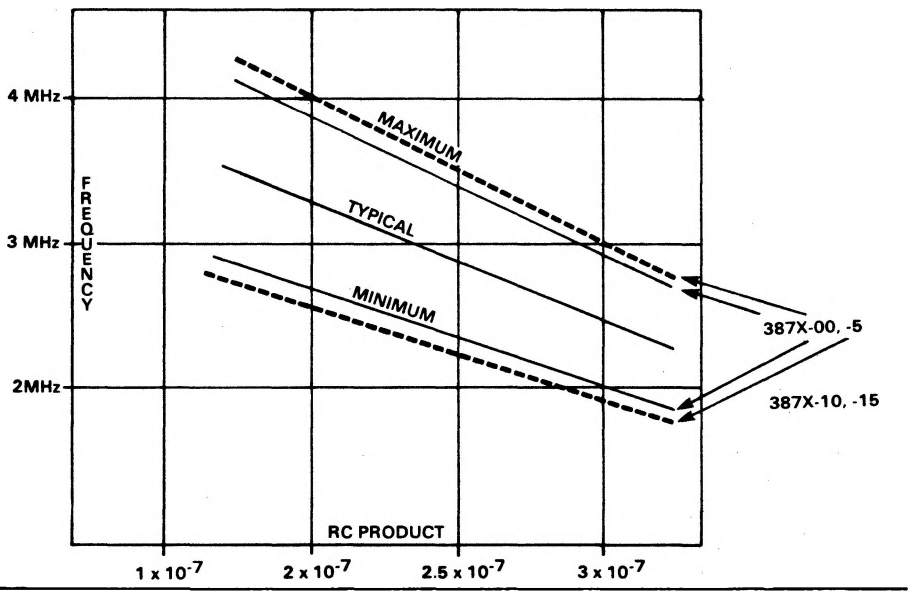
RC CLOCK CONFIGURATION

The time base for the 3875 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 14. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy Mostek recommends the use of the Crystal or LC time base configuration. Figure 15 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3875 devices are also shown in the diagram.

RC MODE CONNECTION
Figure 14



FREQUENCY VS. RC
Figure 15



The designer must select the RC product such that a frequency of less than 2 MHz is not possible taking into account the maximum possible RC product and using the minimum curve shown in Figure 15. Also, the RC product must not allow a frequency of more than 4 MHz taking into account the minimum possible R and C and using the Maximum curve shown. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or - 5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, -05	+6 percent to - 9 percent
387X-10, -15	+9 percent to -12 percent

Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

$$\text{Typical RC} = (\text{R typ})\left(\text{C external typ} + \frac{\{C_{XTL}\ \text{max} + C_{XTL}\ \text{min}\}}{2}\right)$$

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Negative Freq. Variation due to RC Components = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$

Total frequency variation due to all factors:

387X-00, -05	387X-10, -15
= +18 percent plus positive frequency variation due to RC components	= +21 percent plus positive frequency variation due to RC components
= -18 percent minus negative frequency variation due to RC components	= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

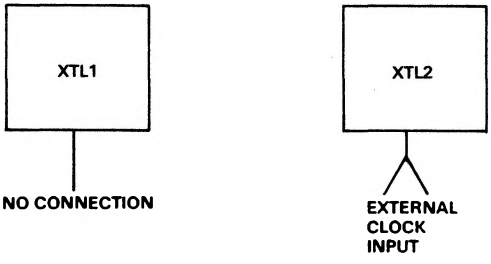
387X-00, -05	387X-10, -15
= + 13 percent	= + 16 percent

EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 16. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3875 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION
Figure 16



OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
- 00	+5V ± 10%	0°C - 70°C
- 05	+5V ± 5%	0°C - 70°C
- 10	+5V ± 10%	-40°C - +85°C
- 15	+5V ± 5%	-40°C - +85°C

See order information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C +85°C	-50°C to 100°C
Storage Temperature	-65°C +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins with Respect to Ground	-1.0V to +13.5V	-1.0V to 13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating and conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation < 100mW (Note 4)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_0$		$2t_0$			
WRITE	t_W	Internal WRITE Clock period	4 t Φ 6 t Φ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50fF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	125Φ +300	ns	$\overline{STROBE}$ load = 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +5.0		power supply rise time +5.5		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

AC CHARACTERISTICS FOR MK38P75

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW. (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11}-A_0 stable until data must be valid at D_7-D_0	650		650		ns	Φ = 2.0 MHz

*See Table in Figure 10

CAPACITANCE

T_A = 25°C All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O $\overline{\text{RESET}}$, EXT INT, TEST		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 4)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	NOTES
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		94		125	mA	Outputs Open (5)
P_D	Average Power Dissipation		440		575	mW	Outputs Open (6)
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	V_{IHEX}=V_{CC}
I_{ILEX}	External Clock input low current		-100		-130	μA	V_{ILEX}=V_{SS}
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard Pull-Up (1,2)
		2.0	13.2	2.0	13.2	V	Open Drain (1,3)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	2.2	5.8	V	Standard Pull-Up(1, 2)
		2.0	13.2	2.2	13.2	V	No Pull-Up (1,3)
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	3.8	V	Standard Pull-Up(1, 2)
		2.0	13.2	2.2	13.2	V	No Pull-Up (1,3)
V_{IL}	I/O ports, $\overline{\text{RESET}}$, EXT INT input low level	-.3	.8	-.3	.7	V	
V_{ILRPT}	$\overline{\text{RESET}}$ input low level to protect RAM during loss at V_{CC}	-.3	.4	-.3	.4	V	
I_{IL}	Input low current, standard pull-up pins		-1.6		-1.9	mA	V_{IN}=0.4V (2)

DC CHARACTERISTICS (Continued)

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 4)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	NOTES
I_L	Input leakage current, open drain pins Reset and EXT INT inputs With no pull-up resistor		+10 -5		+18 -8	μA μA	V_{IN}=13.2V V_{IN}=0.0V (3)
I_{OH}	Output high current, standard	-100		-89		μA	V_{OH}=2.4V
	Pull-Up pins	-30		-25		μA	V_{OH}=3.9V
I_{OHDD}	Output high current	-100		-80		μA	V_{OH}=2.4V
	Direct Drive pins	-1.5		-1.3		mA	V_{OH}=1.5V
			-8.5		-11	mA	V_{OH}=0.7V
I_{OL}	Output low current, I/O ports	1.8		1.65		mA	V_{OL}=0.4V
I_{OHS}	STROBE Output High current	-300		-270		μA	V_{OL}=2.4V
I_{OLS}	STROBE output low current	5.0		4.5		mA	V_{OL}=0.4V

DC CHARACTERISTICS FOR STANDBY POWER PINS

V_{CC}, T_A within operating range I/O Power Dissipation ≤ 100 mW (Note 4)

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
V_{SB}	Standby V_{CC} for RAM	3.2	V_{CC} MAX	3.2	V_{CC} MAX	V	
I_{SB}	Standby Current		6		7.5	mA	V_{SB} = V_{SB} MAX
			3.7		5.0	mA	V_{SB} = V_{SB} MIN
I_{CHARGE}	Trickle charge available on $V_{SB}$with V_{CC} in operating range.	-.8		-.7		mA	V_{SB} = 3.8V
			-15		-19	mA	V_{SB} = 3.2V

DC CHARACTERISTICS FOR MK38P75

(Signals brought out at socket)
T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITION
I_{CCE}	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.8	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100		-90		μA	V_{OH}=2.4 V
		-30		-25		μA	V_{OH}=3.9 V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4 V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

1. $\overline{\text{RESET}}$ and ET INT have internal Schmit triggers giving minimum .2V hysteresis
2. $\overline{\text{RESET}}$ and EXT INT prgrammed with standard pull-up
3. $\overline{\text{RESET}}$ or EXT INT programmed without standard pull-up
4. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL})(|I_{IL}|) + \Sigma (V_{CC} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$
5. I_{CC} exclusive of I_{charge}
6. P_D exclusive of battery charging power. Battery charging power dissipated inside the MK3875 $(V_{CC} - V_{SB})(I_{charge})$

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode

Single interval error, free running (Note 3)	±6tΦ
Cumulative interval error, free running (Note 3)	0
Error between two Timer reads (Note 2)	±(tpsc + tΦ)
Start timer to stop Timer error (Notes 1, 4)	+tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2)	-5tΦ to -(tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3)	-2tΦ to -8tΦ
Load Timer to stop Timer error (Note 1)	+tΦ to -(tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2)	-5tΦ to -(tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3)	-2tΦ to -9tΦ

Pulse Width Measurement Mode

Measurement accuracy (Note 4)	+t Φ to -(tpsc +2t Φ
Minimum pulse width of EXT INT pin	2t Φ

Event Counter Mode

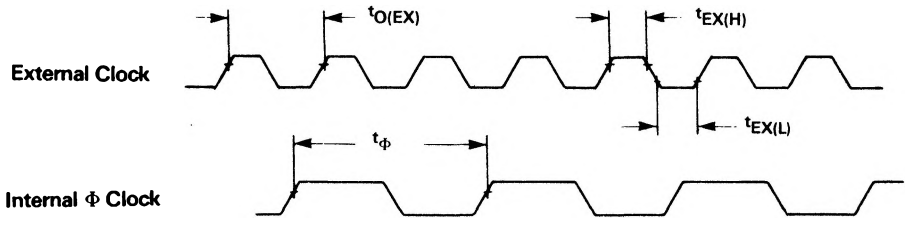
Minimum active time of EXT INT pin	2t Φ
Minimum inactive time of EXT INT pin	2t Φ

Notes:

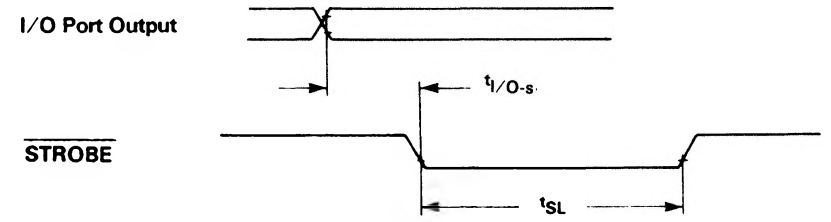
1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

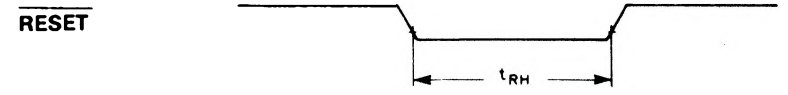
AC TIMING DIAGRAM

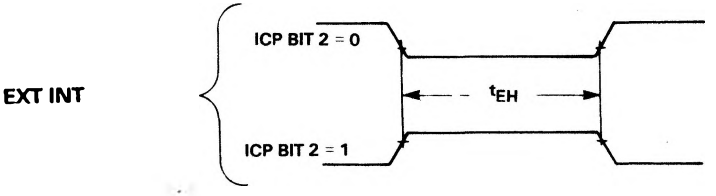
Figure 17



Input capacitance; I/O, $\overline{\text{RESET}}$, EXT INT,



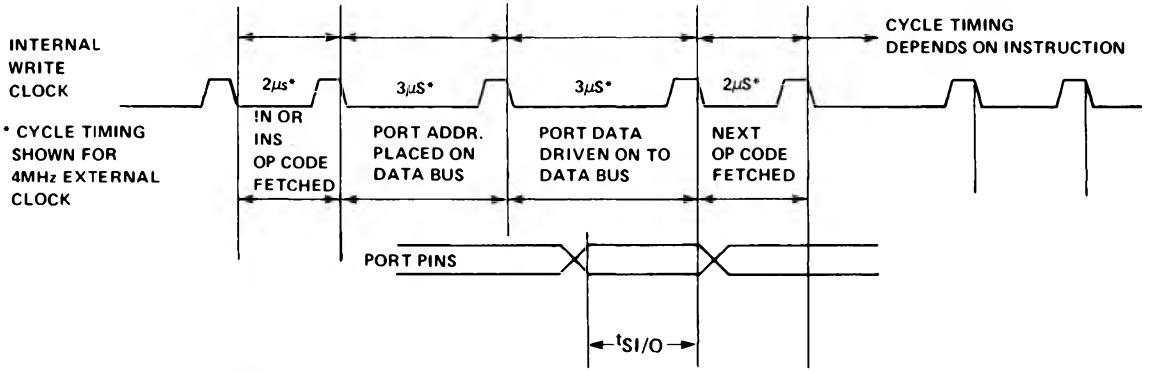




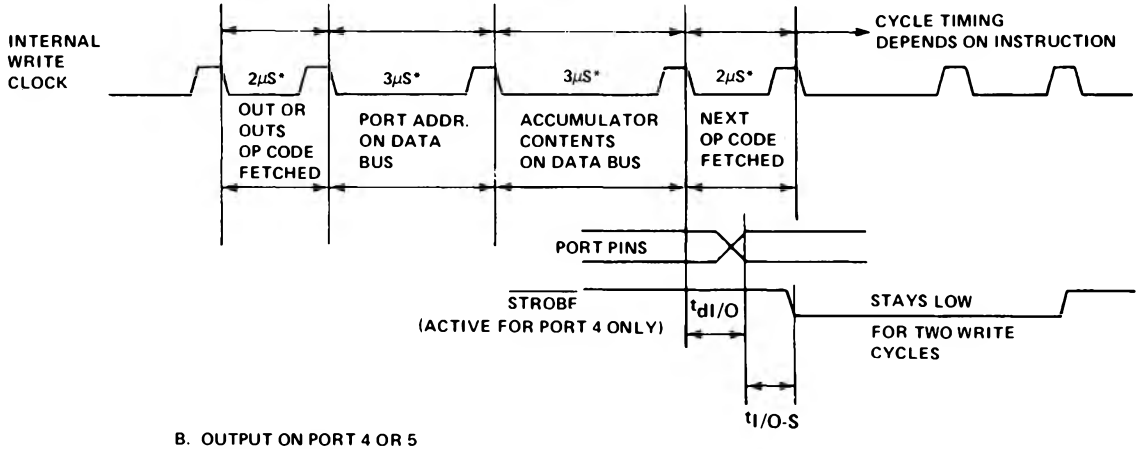
Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

INPUT/OUTPUT AC TIMING

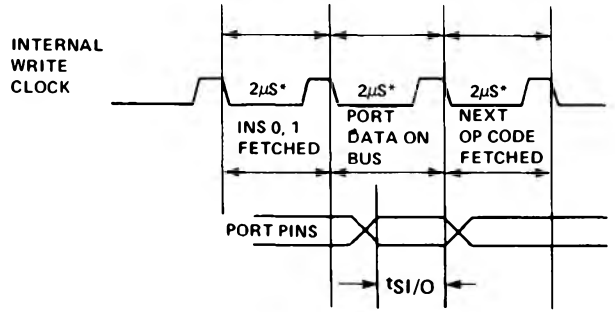
Figure 18



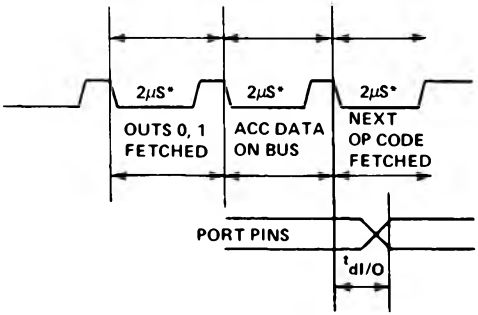
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5

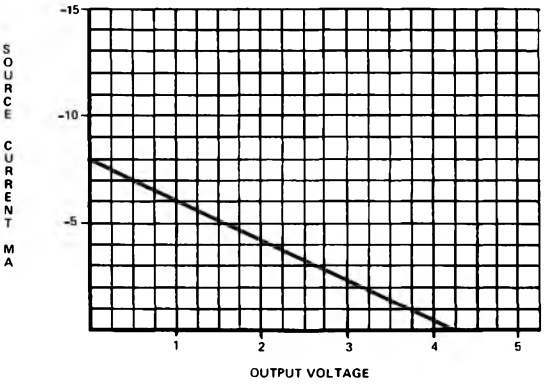


C. INPUT ON PORT 0 OR 1

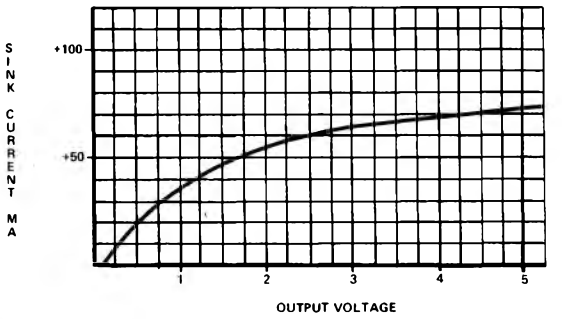


D. OUTPUT ON PORT 0, 1

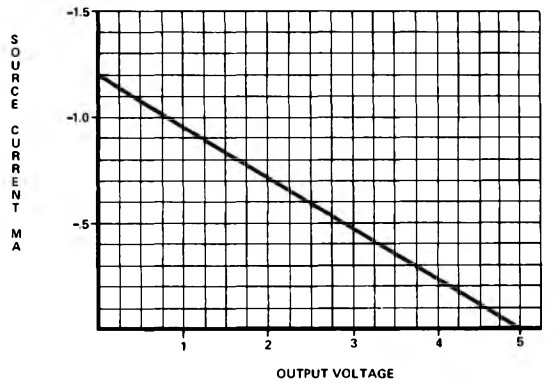
STROBE SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 19



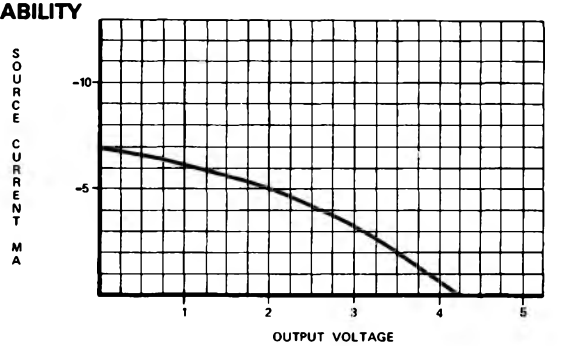
STROBE SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 20



STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 21

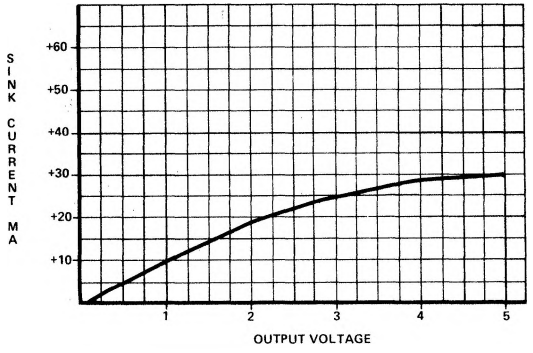


DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 22



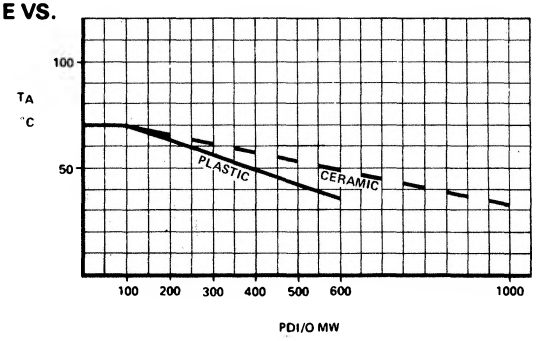
I/O PORT SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 23



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 24

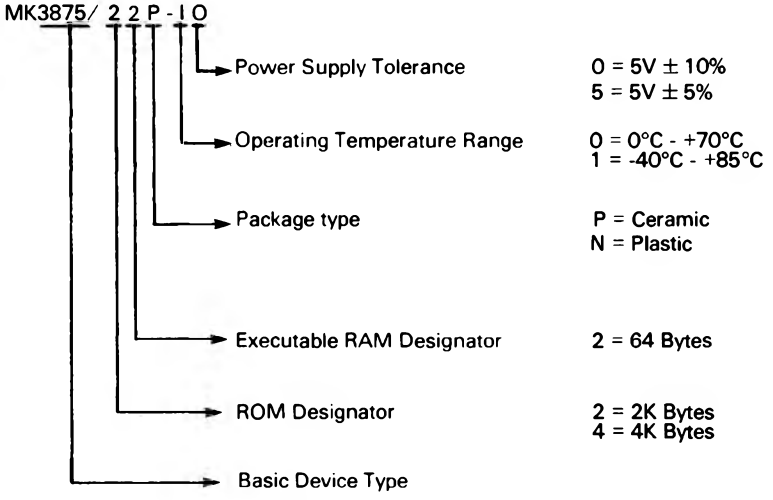


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and executable RAM, the desired package type, temperature range and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

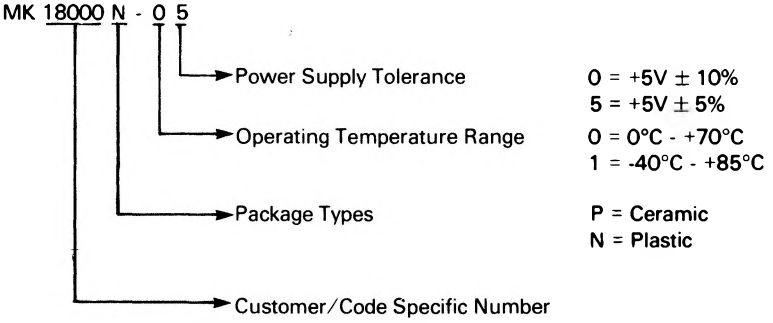
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The customer/code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirement of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.