super computing systems

EMBEDDED COMPUTING CONFERENCE

31. August 2010

A Real-Time Low-Power Stereo Engine Using Semi-Global Matching

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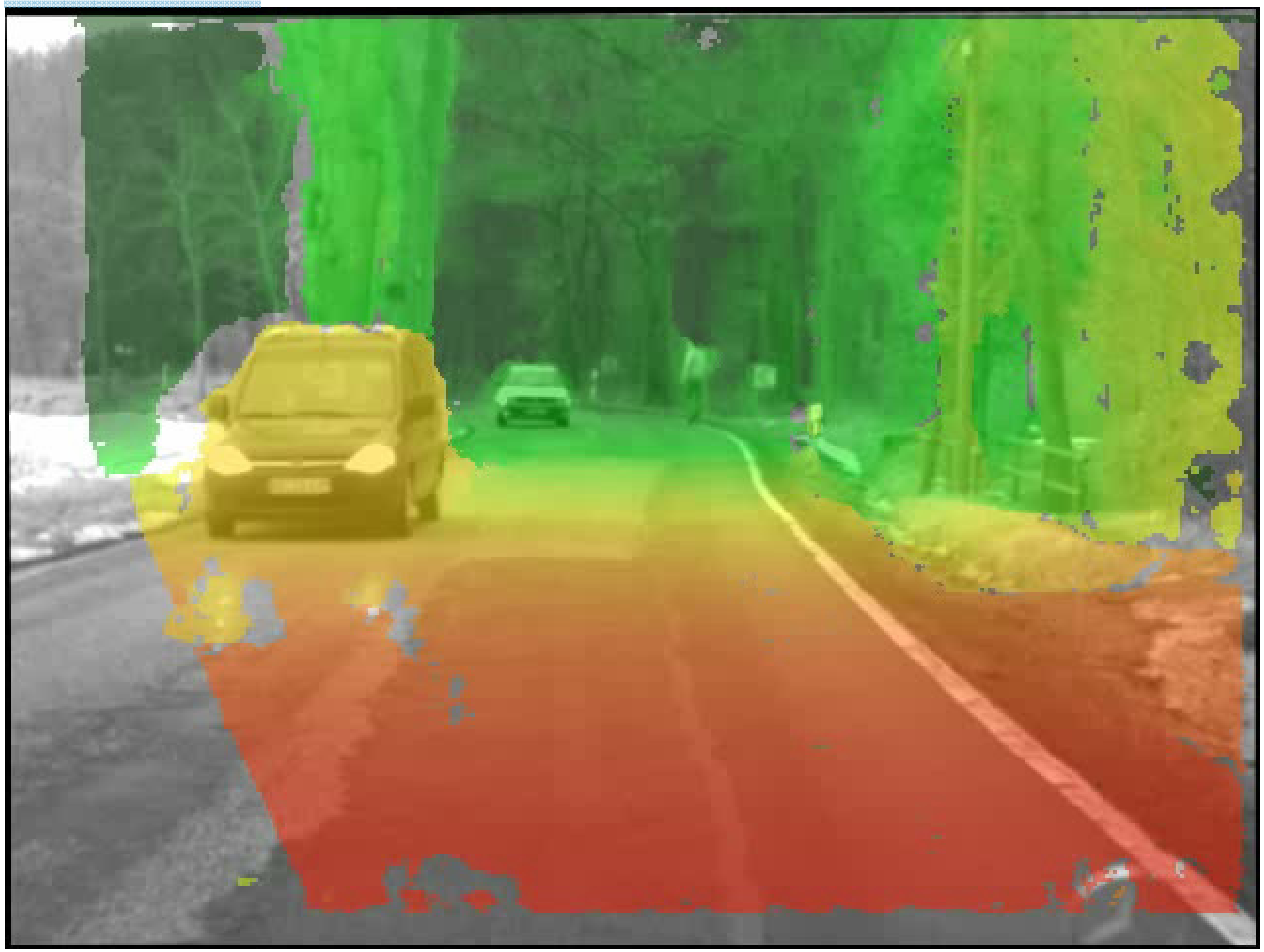
Motivation: 3D Scene Reconstruction

close ..... far



Overview

- **Why FPGA?**
- **SGM Algorithm**
  - Why Semi-Global Matching (SGM)?
  - How does SGM work?
  - Hardware Implementation
  - Results
  - Summary and Conclusions
- **SCS Spartan6 FPGA BOX**
- **EB Assist ADTF Messtechnik**

Why SGM?

- SGM is found 3 times in the top 12 (2009/09/15)
- Most other top-performing algorithms use segmentation which complicates a hardware solution
- Performance tested offline successfully on street scenes with adapted similarity criterion

Middlebury Stereo Evaluation - Version 2

New features and main differences to version 1.
Submit and evaluate your own results.

Open a new window for each link

Error Threshold = 0.5 | Error Threshold...

Sort by nonocc | Sort by all | Sort by disc

Algorithm	Avg. Rank	Tsukuba ground truth nonocc	Tsukuba all	Tsukuba disc	Venus ground truth nonocc	Venus all	Venus disc	Teddy ground truth nonocc	Teddy all	Teddy disc	Cones ground truth nonocc	Cones all	Cones disc	Average percent of bad pixels (explanation)
GC+SegmBorder [57]	5.2	6.87 6	7.30 4	15.3 8	**0.20** 1	**0.31** 1	**2.44** 1	**7.59** 1	**9.14** 1	**17.5** 1	10.5 26	11.2 3	14.4 10	8.56
SubPixDoubleBP [30]	8.7	8.78 13	9.45 11	14.9 6	0.72 3	1.12 3	5.24 3	10.1 4	16.4 4	21.3 2	8.49 20	14.7 20	16.5 15	10.7
BP+DirectedDiff [61]	9.3	6.21 4	7.96 7	24.5 52	1.59 6	2.34 7	6.94 5	7.78 2	17.3 6	22.5 3	**4.73** 1	14.6 18	**10.7** 1	10.6
Undr+OvrSeg [48]	10.2	**4.84** 1	**5.22** 1	9.39 2	2.00 7	2.15 6	5.44 4	12.9 15	17.9 9	27.6 17	9.16 21	14.6 17	17.6 23	10.7
C-SemiGlob [19]	11.2	13.9 26	14.7 25	18.9 25	3.30 10	3.82 9	10.9 11	9.82 3	17.4 7	22.8 5	5.37 5	11.7 4	12.8 4	12.1
CoopRegion [41]	11.8	18.9 33	19.5 33	21.2 37	1.38 4	1.77 4	9.39 8	10.6 6	15.3 3	22.6 4	5.36 4	**10.6** 1	13.0 5	12.5
VarMSOH [54]	11.9	7.18 8	8.56 10	20.1 32	1.46 5	2.12 5	7.87 7	12.9 16	19.4 15	27.5 16	6.22 8	12.6 8	15.8 13	11.8
ImproveSubPix [25]	12.2	8.96 14	9.66 12	16.2 13	4.62 20	5.41 20	16.9 38	11.0 9	17.8 8	24.1 7	4.90 2	10.8 2	12.2 2	11.9
AdaptOvrSegBP [33]	12.8	5.98 2	6.56 2	**9.09** 1	3.66 12	3.96 10	13.2 22	13.0 17	18.9 12	26.4 12	9.48 23	14.9 21	17.2 19	11.9
OverSegmBP [26]	13.7	7.75 11	8.17 8	13.8 4	4.33 16	4.73 14	16.8 36	13.2 18	19.3 14	27.5 15	6.53 11	12.6 9	14.0 8	12.4
AdaptingBP [17]	16.0	19.1 35	19.3 32	17.4 16	4.84 21	5.08 18	7.84 6	12.8 14	16.7 5	26.3 11	7.02 14	13.2 13	14.0 7	13.6
SemiGlob [6]	16.2	13.4 24	14.3 23	20.3 34	4.55 18	5.38 19	15.7 33	11.0 8	18.5 10	26.1 10	4.93 3	12.5 7	13.5 6	13.3

Stereo with Semi-Global Matching (SGM)

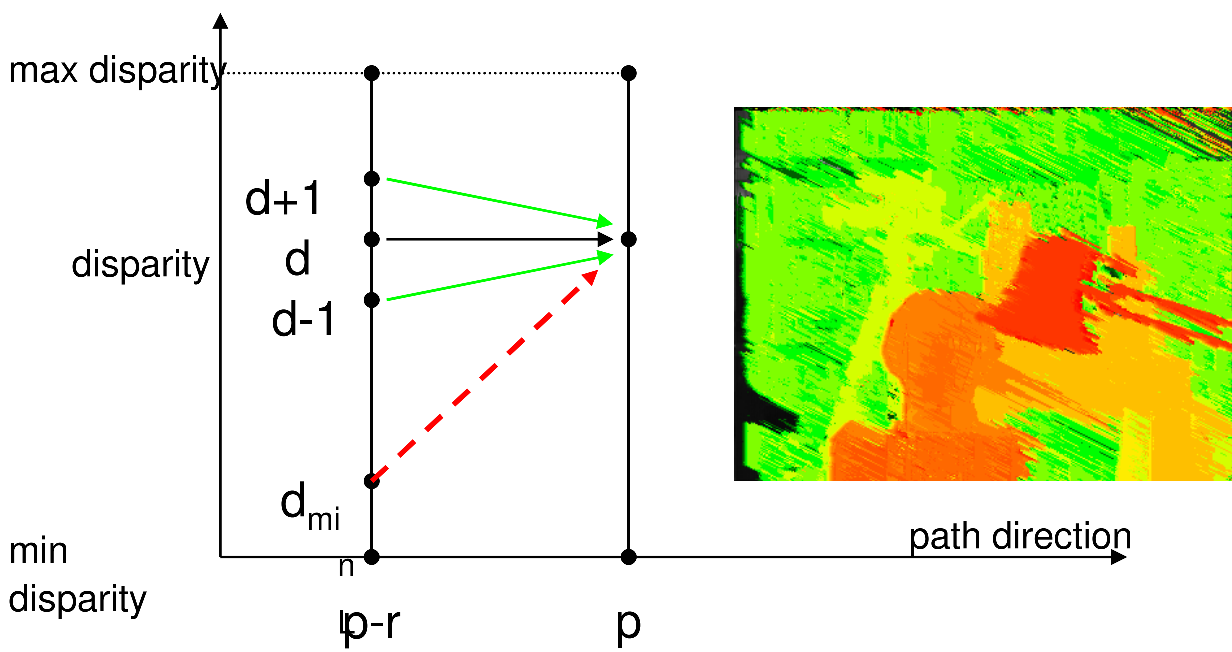
- Local algorithms
  - Estimate correspondence independently at each pixel, typically using correlation between local windows.
  - short-sighted, can fail in poorly textured areas.
- Global algorithms
  - Try to minimize an overall energy term, which usually consists of two parts:

    $$E(f) = E_{similarity}(f) + E_{smoothness}(f)$$

  - In general computationally complex, not suitable for real time application.
- Semi-Global Matching
  - Proposed by Heiko Hirschmüller (CVPR 2005).
  - Minimizes energy similar to global algorithms using smoothness constraint.
  - Approximates a global minimum by propagating the lowest costs from several 1D paths across the image.

Propagating the Lowest Cost Along a 1D Path

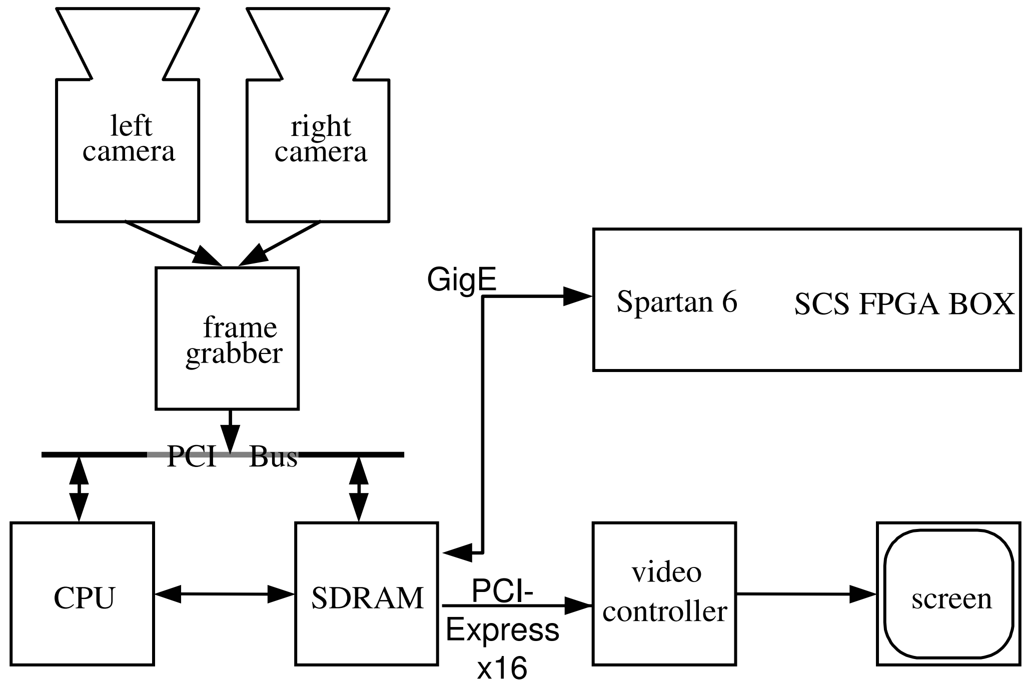
- The global energy to be minimized includes:
  - The dissimilarity costs C(p,d) – data term
  - A small penalty P1 to every slight disparity changes between neighboring pixels
  - A large penalty P2 to every disparity jump – smoothness term
- For one direction in a 1D line, the optimal solution is obtained by propagating the lowest costs similar to dynamic programming (without backtracking).



$$\left\{\begin{array}{l} L(p-r,d) \\ L(p-r,d+1)+p_1 \\ L(p-r,d-1)+p_1 \\ \min L(p-r,i)+p_2 \end{array}\right.$$

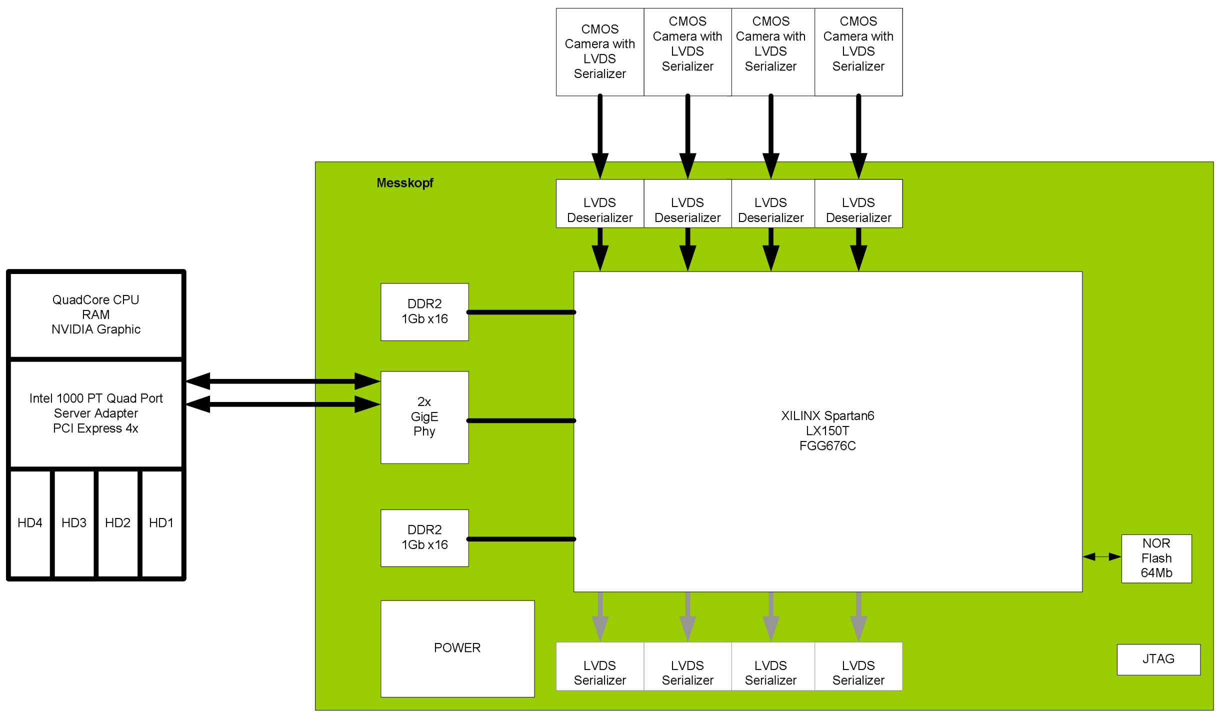
Hardware Implementation II

Experimental System



- SCS Spartan6 FPGA Box used for experimental system
- Target system uses a Xilinx Spartan6 FPGA and is directly connected to the cameras

Example Project: 4 LVDS Cam HIL Interface Box



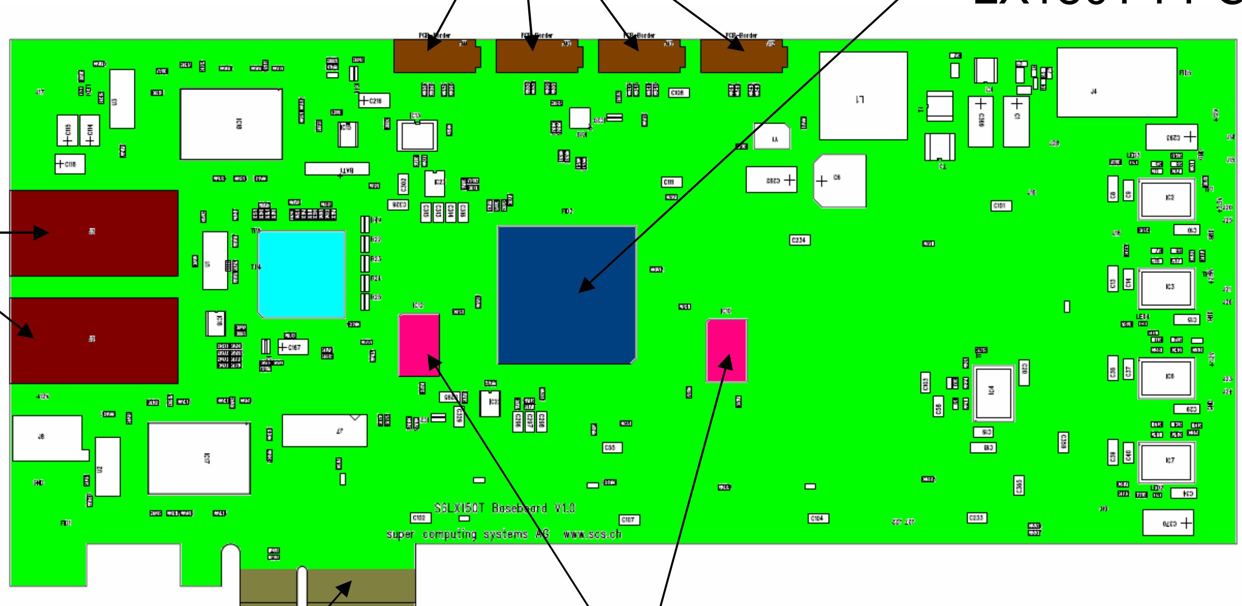
FPGA Board Overview

More than 160 User IO over FMC connectors

4x SATA

Xilinx Spartan6 LX150T FPGA

2x GigE



PCIe 4 Lane

2x DDR2 SDRAM

Main Features

FPGA	1 x Spartan 6 LX 150T
SDRAM	2 x DDR2 128MB (1GBit) (optional 2GBit)
PCIe	4 lane PCIe over Gennum G4124 (optional)
GigE	2 x GigE (Linux driver available / Windows driver optional)
SATA	4 x SATA connector (optional)
User IO	2 x LPC FMC connector (72 I/O and 1 serdes each) 1 special connector (about 40 slow I/O, 2 serdes and supply)
Supply	12V (7-20V) ~10W (depending on AddOn card and algorithm)
Board dimension	24cm x 10 cm
Box dimension	31cm x 20cm x 7cm

FPGA card can be ordered from SCS in two versions:

- OEM card

- with housing and power supply
  (algorithms and interface cards on request)

HIL System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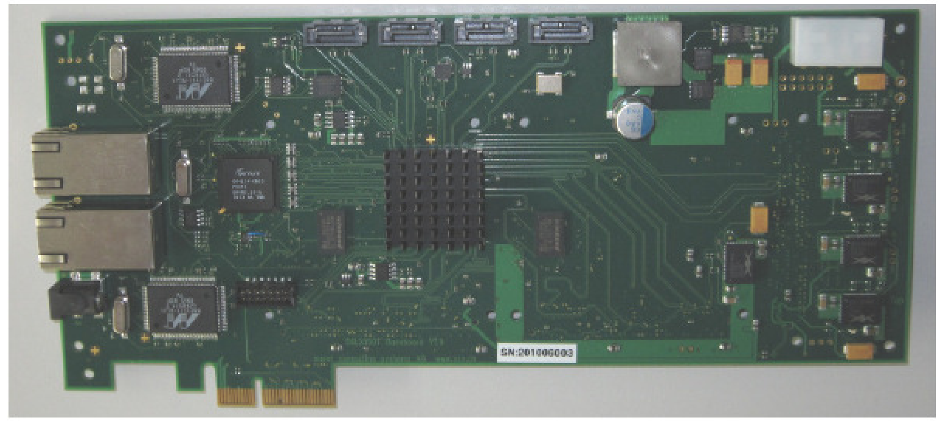
www.scs.ch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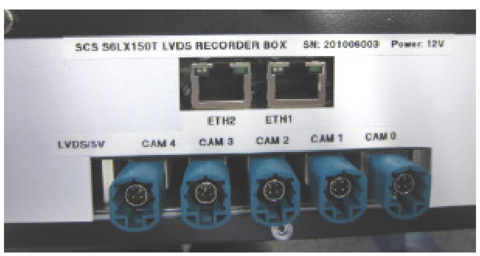
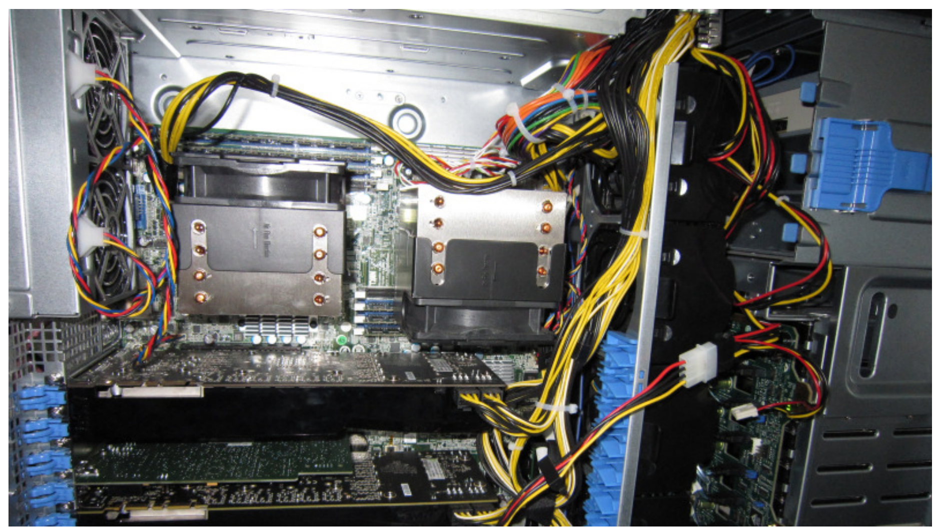
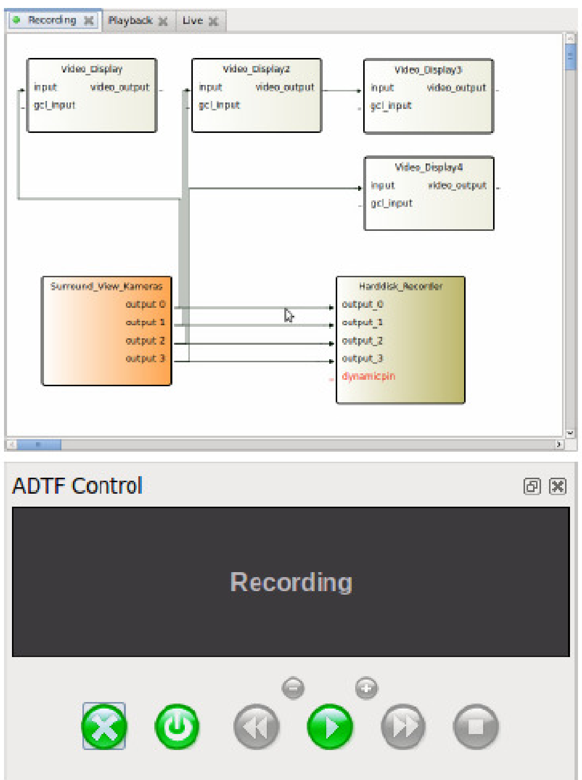
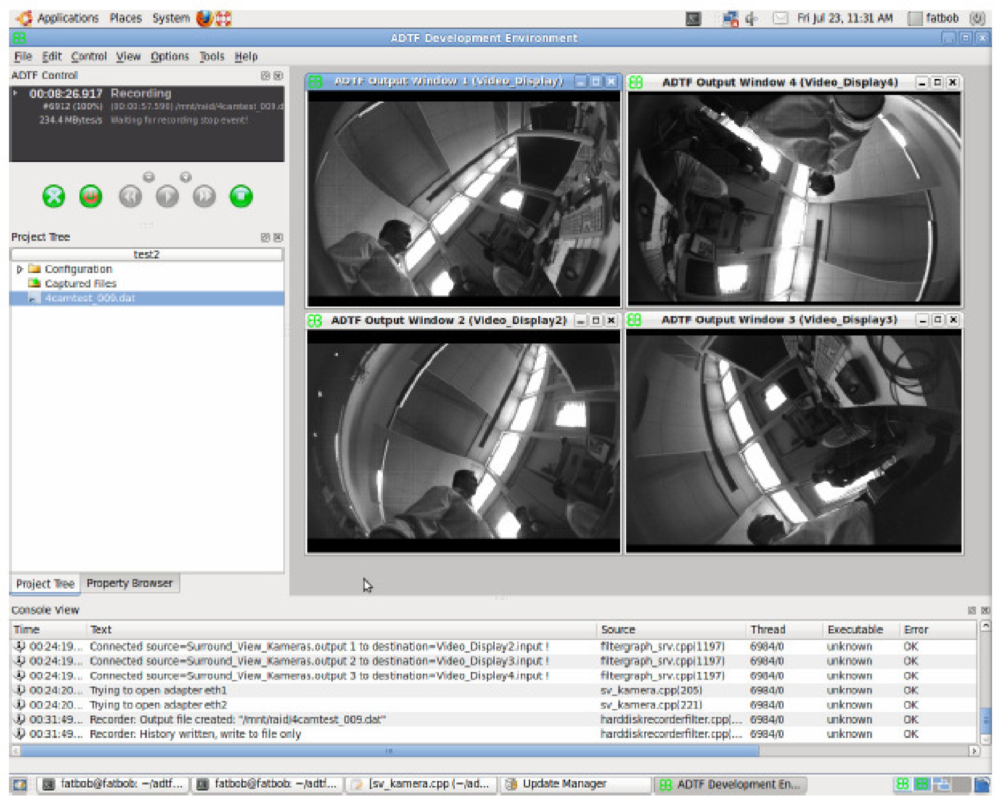

SCS S6LX150T LVDS RECORDER BOX
SN: 201006003
Power: 12V
ETH2
ETH1
LVDS/5V
CAM 4
CAM 3
CAM 2
CAM 1
CAM 0



EB Assist ADTF Integration





SCS

- >15 years of contract develoment of electronics, software and algorithms
- >60 engineers in the fields of
  - Automotive
  - Embedded Systems
  - Vision & Sensors
  - High Performance Computing
  - Enterprise Software

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